CpE 272 Digital Logic Laboratory
Final Quiz Study Guide

The final quiz will be given during the first 30 minutes of lab. Be on time to lab to get the full amount of time to take the quiz. If you are late you will not be given extra time. The quiz will be open notebook, so you can use any notes, lab reports, lab handouts etc. Computers and cell phones are not permitted. The topics below have all been covered in lab, and the quiz will be taken from knowledge required to complete the labs.

- How to connect gates to make other types of gates
- JK/D/T Flip Flops
- Reducing simple K-Maps
- Basic of the Altera board (clock frequency, turning on a segment)
- How multiplexers work
- What is required to make a mux of a particular size
- WINCUPL symbols for AND/OR/ETC
- Converting decimal/binary/hex
- Half adders/full adders
- How port mapping works
- How to create an X-bit adder
- Priority Encoders
- Drawing/analyzing state diagrams
- Memory including address lines, data lines.
- How to address a particular memory location
- Positive/negative-edge triggering
- How flip-flops are made in VHDL
- Mealy/Moore Model