2 Transistor Models

In EEE 41, you studied the fundamental concepts of how transistors can be realized using semiconductors, specifically, the two most popular transistors currently in use: the bipolar junction transistor (BJT) and the metal-oxide field-effect transistor (MOSFET).

In EEE 51, we want to be able to use these transistors (as well as other semiconductor devices such as diodes) to design and implement useful electronic circuits. This means we have to be able to describe, and eventually predict, the behavior of the terminal voltages and currents of these devices. We can accomplish this by using transistor models.

2.1 Large Signal Transistor Models

The large signal transistor models allow us to describe the electrical behavior of the transistor, when a voltage or current is varied over its allowable range. Here, we can see how varying the terminal voltages (and currents) determine the operating region of the transistor. Since there are many combinations of voltages and currents available for us to choose from, it is convenient to standardize which terminal voltages/currents we can use. This makes it easy to compare different transistors, as well as to systematically analyze and design electronic circuits based on these transistors.

The standard large signal transistor characteristics that we use are (1) the transfer characteristics, (2) the output characteristics, and (3) the input characteristics. Note that these models are normally considered as DC or low-frequency models, where we assume that the transistor parasitic capacitances are still negligible.

2.1.1 Transfer Characteristics

Transfer characteristics usually implies an input-output relationship, similar to the transfer function of a two-port network. But where are the input/output terminals or ports of a transistor? As we will see later on, one of the main goals of electronic circuits is to amplify signals (i.e. voltage, current, etc). Thus, it is convenient to choose the input-output terminal pair of a transistor that is commonly used to provide the largest amplification. In the BJT case, it is the common-emitter configuration, and in the MOSFET case, it is the common-source configuration.

The BJT Transfer Characteristic: The BJT common-emitter (CE) configuration is shown in Fig. 2.1a. We define the "input" signal as the base-emitter voltage, V_{BE}, and the "output" signal as the collector current I_C. Therefore, we can model the the BJT transfer characteristic using

$$I_C = I_S \cdot \left(e^{\frac{V_{BE}}{V_T}} - 1 \right) \cdot \left(1 + \frac{V_{CE}}{V_A} \right) \tag{2.1}$$

for a transistor in the forward-active region[a]. Note that I_S is the reverse saturation current of the collector-base junction and dependent on the type and geometry of the transistor, V_A is the Early Voltage, and $V_T = \frac{kT}{q}$, the voltage equivalent of temperature ($V_T = 26\,\text{mV}$ at $T = 300\,\text{K}$). For typical discrete (not integrated) BJTs, the value of V_{BE} is around 0.6 mV, and since V_A is normally in the hundreds of volts, we can simplify Eq. 2.1 into

$$I_C = I_S \cdot e^{\frac{V_{BE}}{V_T}} \tag{2.2}$$

Eq. 2.2, shown in Fig. 2.1b, and superimposed with the transfer characteristic of a real BJT, allows us to approximate the behavior of the "output" signal, in this case the collector current, when we change the base-emitter voltage, our "input" signal.

The MOSFET Transfer Characteristic: The MOSFET common-source (CS) configuration is shown in Fig. 2.2a. As with the BJT, we define the "input" signal as the gate-source voltage, V_{GS}, and the "output" signal as the drain current, I_D. Thus, the MOSFET transfer characteristic can be modeled as

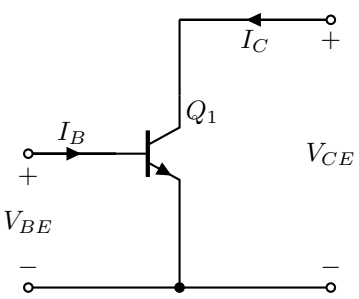
$$I_D = k \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS}) \tag{2.3}$$

in the saturation region[b]. Note that k is a constant dependent on the technology used in the manufacture, and the geometry, of the transistor, V_{TH} is the transistor threshold voltage, and λ is the channel length modulation coefficient. For typical discrete (not integrated) MOSFETs, $\lambda \ll 1$, allowing us to approximate Eq. 2.3 with

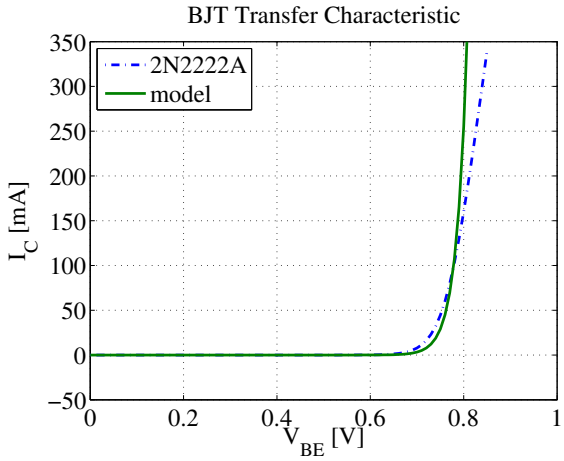
$$I_D = k \cdot (V_{GS} - V_{TH})^2 \tag{2.4}$$

[a] In EEE 51, we will almost always use the BJT in the forward active region. However, in circuits where this is not the case, the transfer characteristic should be modeled with the appropriate relationship between V_{BE} and I_C.

[b] In EEE 51, we will almost always use the MOSFET in the saturation region. However, in circuits where this is not the case, the transfer characteristic should be modeled with the appropriate relationship between V_{GS} and I_D.

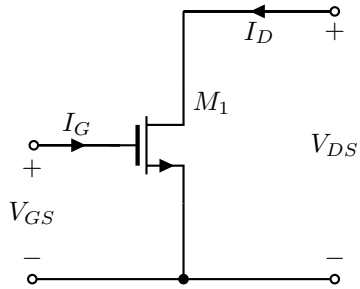


(a) Common-emitter configuration

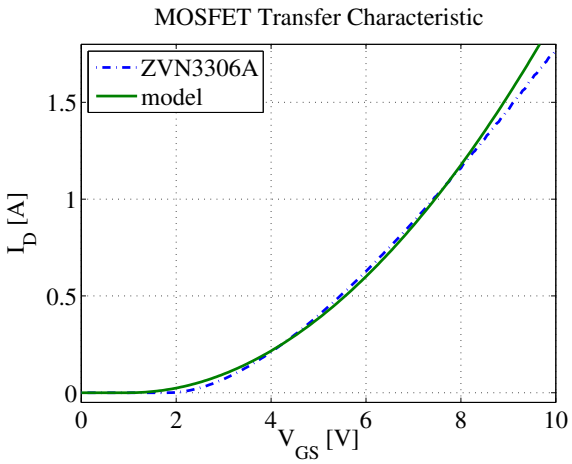


(b) Transfer characteristic

Figure 2.1: The NPN bipolar junction transistor (BJT).



(a) Common-source configuration



(b) Transfer characteristic

Figure 2.2: The N-type metal-oxide field effect transistor (NMOSFET).

And just like the BJT transfer characteristic, Eq. 2.4 allows us to model the behavior of the "output" signal, in this case the drain current, when we change the gate-source voltage, our "input" signal. Fig. 2.2b shows the transfer characteristic of a real MOSFET, together with the plot of Eq. 2.4.

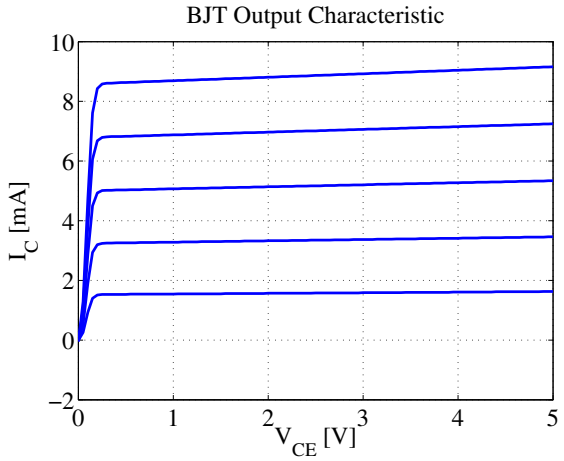
2.1.2 Output Characteristics

In both the BJT and MOSFET, we defined our "output" as either the collector current or drain current. However, from Eqs. 2.1 and 2.3, we can see that both these "output" currents are also dependent on their respective "output" voltages – the collector-emitter voltage, V_{CE} for the BJT and the drain-source voltage, V_{DS} for the MOSFET.

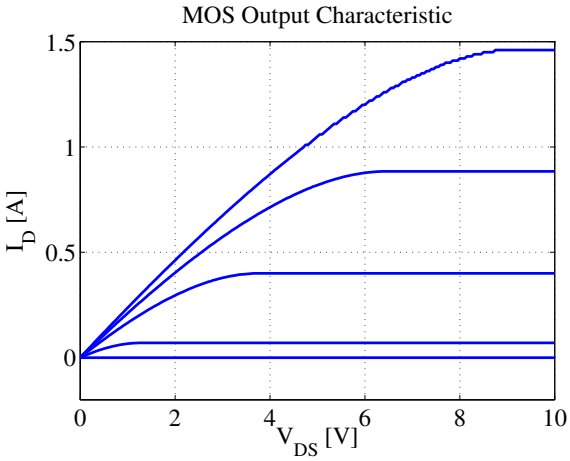
Since we want to be able to describe the transistor behavior completely, we need to take into account all the factors that affect the "output" current. Hence, we use the transistor output characteristic, I_C vs. V_{CE} for a BJT and I_D vs. V_{DS} for a MOSFET, to model the change in "output" current when the "output" voltage is changed.

The output characteristics of a typical BJT is shown in Fig. 2.3a, and Fig. 2.3b shows the output characteristic of a typical MOSFET. Note that in both cases, the output characteristics span several operating regions. In the case of the BJT, the saturation, forward-active and cut-off regions can be seen. The same is true for the MOSFET, where the linear or ohmic region, the saturation region, and the sub-threshold region[c] can be identified.

[c]It is a common simplification to assume that the drain current is zero when $V_{GS} < V_{TH}$, putting the MOSFET in the "cut-off" region. However, keep in mind that below the threshold voltage, the MOSFET behaves like a BJT with very small currents. In very low-power applications, some MOSFETs are intentionally used in this sub-threshold region.



(a) The 2N2222A NPN BJT output characteristic, where I_B is swept from 10 μA to 50 μA in steps of 10 μA.



(b) The ZVN3306A NMOSFET output characteristic, where V_{GS} is swept from 1 V to 9 V in 2 V steps.

Figure 2.3: Transistor output characteristics.

2.1.3 Input Characteristics

Since the BJT and MOSFET[d] can be considered a three-terminal device, to completely describe all the currents and voltages, we will need 2 out of 3 voltages, and 2 out of 3 node currents. This means that in a BJT, if we know V_{BE} and V_{CE}, we automatically know the value of V_{BC} by KVL. By knowing the transfer and output characteristics, we can determine all the voltages in the BJT. The same is true for a MOSFET.

However, if we want to determine all the currents in the transistor, we need another set of current-voltage (I-V) characteristics. It turns out that the most convenient set of I-V characteristics for designing linear electronic amplifiers, is the "input" current vs. the "input" voltage characteristic. In BJTs, this is the V_{BE} vs. I_B characteristic, and for the MOSFET, this is the V_{GS} vs. I_G characteristic. For a BJT, by knowing I_B and I_C, we can easily determine I_E using KCL. Again, the same is true for MOSFETs.

The input characteristics of a BJT can be derived from the BJT transfer characteristics. Since $I_B = \frac{I_C}{\beta}$, we can just divide the BJT transfer characteristic by the transistor β[e]. The input characteristic of a MOSFET is trivial, since $I_G = 0$[f].

In summary, these large signal models allow us to determine the resulting transistor "input" and "output" DC currents when we apply DC voltages across the transistor terminals. Since we can obtain the DC values of the currents and voltages in a transistor, the large signal transistor models are typically used in what is called "DC Analysis".

2.2 Small Signal Modeling

As we have just seen, semiconductor-based transistors are very nonlinear – exponential behavior for BJTs and quadratic behavior for MOSFETs, and these nonlinearities can vary significantly when going from one operating region to another. Analyzing circuits with these devices, by hand, using these large signal models, becomes very complex very quickly, especially when the number of transistors start to increase. Imagine writing your node or loop equations with exponentials and quadratic functions!

In order to analyze, and eventually design, linear electronic circuits, we use two very powerful tools: linearization, and two-port network reduction. These two tools will allow us to (1) use our linear circuit theory skills (taken up in EEE 31 and 33), and (2) break up complex circuits into smaller and simpler ones.

2.2.1 Linearizing the Transistor Transfer Characteristic

In many cases, and often by design, the input signal of an amplifier is made to change by a relatively small amount on top of its DC value. To determine the effect of this disturbance on the rest of the terminal voltages and currents, we can use the large signal models. However, this would result in rather complicated mathematical expressions, with

[d] In EEE 51, we will ignore the MOSFET body effect, and always assume that the body terminal is always connected to the source terminal.

[e] Note that this assumes β is constant over I_C. If the variation in β is significant, then divide the transfer characteristic point-by-point with $\beta(I_D)$.

[f] This ignores MOSFET gate leakage, which will not be taken up in EEE 51.

limited intuitive value. We will use the linearization process to reduce the complexity of the computation, as well as get a better intuitive grasp of the circuit implications, but at the cost of a certain amount of error.

Consider an NPN BJT, in the forward-active region, that is biased with a DC base-emitter voltage of $V_{BE,Q}$. This would result in a DC collector current $I_{C,Q}$, and from Eq. 2.2, is equal to

$$I_{C,Q} = I_S \cdot e^{\frac{V_{BE,Q}}{V_T}} \tag{2.5}$$

Note that we use the subscript Q to indicate that this is the quiescent[g] point DC bias, meaning that this is the purely DC voltage and current of the BJT when there are no disturbances present.

Suppose we add a signal v_{be} on top of $V_{BE,Q}$, such that the total base-emitter voltage is now

$$v_{BE} = V_{BE,Q} + v_{be} \tag{2.6}$$

Assuming that v_{be} is small enough that the transistor does not change its operating region, the collector current then becomes

$$i_C = I_{C,Q} + i_c = I_S \cdot e^{\frac{v_{BE}}{V_T}} = I_S \cdot e^{\frac{V_{BE,Q}+v_{be}}{V_T}} \tag{2.7}$$

where i_c is the collector current deviation away from its quiescent point, due to the addition of the "small" signal v_{be}. Simplifying Eq. 2.7, and using Eq. 2.5, we get

$$I_{C,Q} + i_c = I_S \cdot e^{\frac{V_{BE,Q}}{V_T}} \cdot e^{\frac{v_{be}}{V_T}} = I_{C,Q} \cdot e^{\frac{v_{be}}{V_T}} \tag{2.8}$$

As expected, i_c is a nonlinear function (exponential) of v_{be}. Now, let us try to linearize this relationship. Here we present two methods, but as we will see, they turn out to be equivalent.

Method 1: Recall, that any function that is infinitely differentiable, can be expressed as an infinite sum of terms, and that these terms are calculated from its derivatives at a certain point. We call this infinite sum the Taylor Series representation of a function, such that

$$f(x) = f(a) + \frac{f'(a)}{1!}(x-a) + \frac{f''(a)}{2!}(x-a)^2 + \frac{f'''(a)}{3!}(x-a)^3 + \dots \tag{2.9}$$

where the function $f(x)$ is expanded about point a. Expanding $f(x) = e^x$, about $a = 0$, gives us the well known relationship

$$e^x = e^0 + \frac{e^0}{1!}x + \frac{e^0}{2!}x^2 + \frac{e^0}{3!}x^3 + \dots = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \dots \tag{2.10}$$

Thus, expanding $e^{\frac{v_{be}}{V_T}}$, we get

$$e^{\frac{v_{be}}{V_T}} = 1 + \frac{v_{be}}{V_T} + \frac{1}{2!}\left(\frac{v_{be}}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{v_{be}}{V_T}\right)^3 + \dots \tag{2.11}$$

Substituting Eq. 2.11 into Eq. 2.8 gives us

$$I_{C,Q} + i_c = I_{C,Q} + \frac{I_{C,Q}}{V_T}v_{be} + \frac{1}{2!}I_{C,Q}\left(\frac{v_{be}}{V_T}\right)^2 + \frac{1}{3!}I_{C,Q}\left(\frac{v_{be}}{V_T}\right)^3 + \dots \tag{2.12}$$

We can remove the DC quiescent current term $I_{C,Q}$ from both sides of Eq. 2.12, giving us

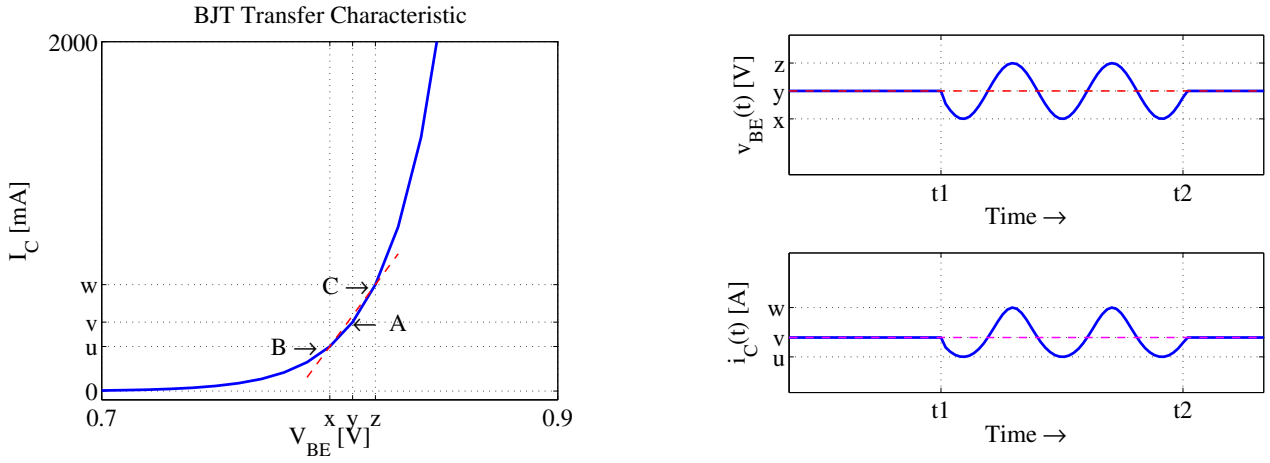
$$i_c = \frac{I_{C,Q}}{V_T}v_{be} + \frac{1}{2!}I_{C,Q}\left(\frac{v_{be}}{V_T}\right)^2 + \frac{1}{3!}I_{C,Q}\left(\frac{v_{be}}{V_T}\right)^3 + \dots \tag{2.13}$$

Eq. 2.13 is a very important result. First, it gives us an alternative to Eq. 2.8 in computing for i_c, but more importantly, it shows us that for $\frac{v_{be}}{V_T} \ll 1$, all the terms of Eq. 2.13 become very much less than the first term. Thus, we can approximate i_c as

$$i_c = \frac{I_{C,Q}}{V_T} \cdot v_{be} \tag{2.14}$$

Note that Eq. 2.14 provides us with a "linear" relationship between i_c and v_{be}, and is a good approximation only when v_{be} is small enough, that is when $v_{be} \ll V_T$. In this case, we can assume that v_{be} is a "small signal". Eq. 2.13 also allows us to compute how much error we are incurring if we use Eq. 2.14, by summing up the remaining terms that we have ignored. Also, a very important observation here is that the relationship between i_c and v_{be} depends on $I_{C,Q}$.

[g] Synonymous to an idle, or rest state.



(a) The BJT transfer characteristic

(b) Time domain view

Figure 2.4: Linearization of the BJT transfer characteristic.

Method 2: Another approach to linearizing the relationship between i_c and v_{be} is by looking at this relationship graphically. Consider the graph of a BJT transfer characteristic shown in Fig. 2.4a.

If point A is the DC quiescent point, then $y = V_{BE,Q}$, and $v = I_{C,Q}$. Also, if $|v_{be}| = |z - x|$, then adding v_{be} on top of $V_{BE,Q}$ would result in the collector current also changing by an $|i_c| = |w - u|$. We are using the absolute value signs to indicate that both v_{be} and i_c can take on negative values. That is, when $v_{be} = 0$, the total base-emitter voltage is $v_{BE} = y = V_{BE,Q}$. When v_{be} is at its maximum value, $v_{BE} = z = V_{BE,Q} + v_{be,\max}$, and the transistor is operating at point C. When v_{be} is at its minimum (negative) value, $v_{BE} = x = V_{BE,Q} - |v_{be,\min}|$, corresponding to point B.

For clarity, a possible time domain view is given in Fig. 2.4b for $v_{BE}(t) = V_{BE,Q} + v_{be}(t)$ and $i_C(t) = I_{C,Q} + i_c(t)$. Note that for time $t < t_1$ and $t > t_2$, $v_{be}(t) = 0$, thus, $i_c(t) = 0$, which means that the transistor is in its quiescent point, that is $v_{BE}(t) = V_{BE,Q}$ and $i_C(t) = I_{C,Q}$.

We can approximate the relationship between v_{be} and i_c using a straight line (linear!) passing through points B and C. If we know the slope, m, of this line, we can estimate the magnitude i_c given v_{be} as $i_c = m \cdot v_{be}$. However, finding the slope of this line is not very straightforward, and as seen in Fig. 2.4a, using the dashed line will result in errors for points between B and C. On the other hand, if v_{be} is small, or equivalently if $x \to y$ and $z \to y$, then the error becomes smaller, and our linear approximation becomes more accurate. The slope of our linear approximation, if we make v_{be} approach zero, can be expressed as

$$m = \lim_{v_{be} \to 0} \frac{i_C(V_{BE,Q} + v_{be}) - i_C(V_{BE.Q})}{V_{BE,Q} + v_{be} - V_{BE,Q}} \tag{2.15}$$

Recall that for a function, $f(x)$, its derivative at a point $x = X_0$ is given as

$$\left.\frac{\partial f(x)}{\partial x}\right|_{x=X_0} = \lim_{\Delta x \to 0} \frac{f(X_0 + \Delta x) - f(X_0)}{\Delta x} \tag{2.16}$$

Thus, for small values of v_{be}, we can approximate i_c as

$$i_c = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{V_{BE}=V_{BE,Q}} \cdot v_{be} = g_m \cdot v_{be} \tag{2.17}$$

where g_m is known as the device or transistor *transconductance*, since it relates small variations in the base-emitter voltage and collector current – the parameters of the transistor transfer characteristic. The transistor transconductance is formally defined as

$$g_m = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{V_{BE}=V_{BE,Q}} \tag{2.18}$$

Note that g_m has units of Siemens (S)[h], and is dependent on the quiescent point. Thus, a different $V_{BE,Q}$ would result in a different $I_{C,Q}$, and hence a different g_m.

By plugging in Eq. 2.2 into Eq. 2.18, we can calculate the value of the transconductance for a BJT as

[h] $1\,\mathrm{S} = 1\,\frac{1}{\Omega} = 1\,\mho$

$$g_m = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{V_{BE}=V_{BE,Q}} = \left.\frac{\partial}{\partial V_{BE}}\left(I_S \cdot e^{\frac{V_{BE}}{V_T}}\right)\right|_{V_{BE}=V_{BE,Q}} = \frac{1}{V_T} \cdot I_S \cdot e^{\frac{V_{BE,Q}}{V_T}} = \frac{I_{C,Q}}{V_T} \tag{2.19}$$

Thus, Eq. 2.19 makes Eq. 2.17 equivalent to Eq. 2.14, which should not be that surprising since the Taylor Series coefficients are obtained using derivatives and we are only approximating the transfer characteristic by the first derivative term.

We have just covered a very important concept: linearizing the BJT transfer function allows us to approximate the relationship of i_c and v_{be} using a linear function, given by Eq. 2.17, instead of using Eq. 2.8, an exponential equation. Also, if the signals we are dealing with are made smaller, then the errors we incur when using this linear approximation is reduced.

So far, we have used the BJT transfer characteristic. The process is exactly the same when dealing with MOSFETs. We can derive the Taylor Series expansion of Eq. 2.4 by just expanding the quadratic term

$$I_{D,Q} + i_d = k \cdot (V_{GS,Q} + v_{gs} - V_{TH})^2 = k \cdot (V_{GS,Q} - V_{TH})^2 + 2k \cdot (V_{GS,Q} - V_{TH}) \cdot v_{gs} + k \cdot v_{gs}^2 \tag{2.20}$$

Since Eq. 2.4 is already a polynomial, the Taylor Series representation shown in Eq. 2.20 is a finite series, and for our purposes, we group these terms into three. The first term in Eq. 2.20 is equal to $I_{D,Q}$. Therefore, we can write out the expression for i_d using the remaining two terms

$$i_d = 2k \cdot (V_{GS,Q} - V_{TH}) \cdot v_{gs} + k \cdot v_{gs}^2 \tag{2.21}$$

Again, if v_{gs} is small, then we can ignore the second term of Eq. 2.21, resulting in the linear relationship

$$i_d = 2k \cdot (V_{GS,Q} - V_{TH}) \cdot v_{gs} \tag{2.22}$$

If we use the definition of transconductance given in Eq. 2.18, and apply it to the MOSFET transfer characteristic given in Eq. 2.4, we would get

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{GS}=V_{GS,Q}} = \left.\frac{\partial}{\partial V_{GS}}\left(k \cdot (V_{GS} - V_{TH})^2\right)\right|_{V_{GS}=V_{GS,Q}} = 2k \cdot (V_{GS,Q} - V_{TH}) \tag{2.23}$$

Using Eqs. 2.4 and 2.23, we can derive the other common forms of the MOSFET transconductance

$$g_m = 2k \cdot (V_{GS,Q} - V_{TH}) = \frac{2 \cdot I_{D,Q}}{V_{GS,Q} - V_{TH}} = \sqrt{4k \cdot I_{D,Q}} \tag{2.24}$$

Once again, we see that our two linearization methods are equivalent, thus

$$i_d = g_m \cdot v_{gs} \tag{2.25}$$

It is very important to remember that even though g_m is a function of the quiescent DC currents and voltages ($V_{BE,Q}$ and $I_{C,Q}$, or $V_{GS,Q}$ and $I_{D,Q}$), the linearized relationships using g_m in Eqs. 2.17 and 2.25 only relates the small signal disturbances superimposed on the DC signals, i_c and v_{be}, or i_d and v_{gs}. Also, the linearization methods presented here are general techniques, independent of the transistor operating region, and can be applied to the large signal characteristic of any device that we may want to linearize.

2.2.2 The Small Signal Equivalent Circuit

From the BJT output characteristic, we know that any small signal disturbance in the collector-emitter voltage will also result in a corresponding change in the collector current. In order to estimate this change in I_C due to a change in V_{CE}, we can easily extend our linearization of the BJT transfer characteristic to its output characteristic.

Consider a BJT in the forward active region, with quiescent current (using Eq. 2.1)

$$I_{C,Q} = I_S \cdot \left(e^{\frac{V_{BE,Q}}{V_T}} - 1\right) \cdot \left(1 + \frac{V_{CE,Q}}{V_A}\right) \tag{2.26}$$

Using our second linearization method, we define the *output conductance*[i], g_o, as

$$g_o = \left.\frac{\partial I_C}{\partial V_{CE}}\right|_{V_{CE}=V_{CE,Q}} \tag{2.27}$$

Thus,

[i]This term is called a conductance and not a transconductance since it relates the voltage across two terminals to the current flowing into one of the terminals.

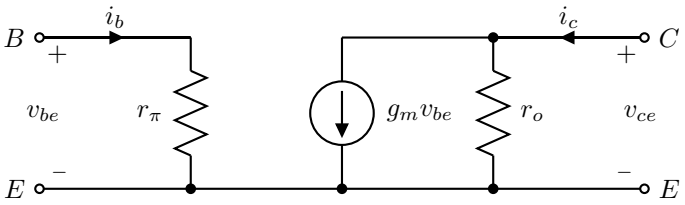


Figure 2.5: The BJT small signal equivalent circuit.

$$g_o = \frac{\partial}{\partial V_{CE}}\left(I_S \cdot \left(e^{\frac{V_{BE}}{V_T}} - 1\right) \cdot \left(1 + \frac{V_{CE}}{V_A}\right)\right)\Bigg|_{V_{CE}=V_{CE,Q}} = I_S \cdot \left(e^{\frac{V_{BE,Q}}{V_T}} - 1\right) \cdot \frac{1}{V_A} \approx \frac{I_{C,Q}}{V_A} \tag{2.28}$$

Often, it is convenient to express the output conductance of the BJT as an *output resistance*, r_o, given by

$$r_o = \frac{1}{g_o} = \frac{V_A}{I_{C,Q}} \tag{2.29}$$

Since g_o is the slope of the BJT output characteristic, we can then relate small changes in the collector-emitter voltage to the small changes in the collector current, using the linearized or small signal BJT output characteristic, given by

$$i_c = g_o \cdot v_{ce} = \frac{v_{ce}}{r_o} \tag{2.30}$$

By superposition, if we have small changes in the base-emitter voltage, and small changes in the collector-emitter voltage, we can combine Eqs. 2.17 and 2.30 to obtain the total small signal change in the collector current, resulting in

$$i_c = g_m \cdot v_{be} + \frac{v_{ce}}{r_o} \tag{2.31}$$

Lastly, if we add a small signal voltage on top of the base-emitter DC quiescent voltage, not only will there be changes in the collector current, we will also be a small signal disturbance in the base current. We can also linearize the relationship between v_{be} and i_b by extending our linearization process to the BJT input characteristic.

In the forward-active region, the quiescent base current is given by

$$I_{B,Q} = \frac{I_{C,Q}}{\beta} = \frac{I_S}{\beta} \cdot \left(e^{\frac{V_{BE,Q}}{V_T}} - 1\right) \tag{2.32}$$

We define the BJT *input conductance*, g_π, as

$$g_\pi = \frac{\partial I_B}{\partial V_{BE}}\bigg|_{V_{BE}=V_{BE,Q}} = \frac{1}{\beta} \cdot \frac{\partial I_C}{\partial V_{BE}}\bigg|_{V_{BE}=V_{BE,Q}} = \frac{g_m}{\beta} = \frac{I_{C,Q}}{\beta \cdot V_T} \tag{2.33}$$

Again, it is often convenient to represent the input conductance as an *input resistance*, r_π, expressed as

$$r_\pi = \frac{1}{g_\pi} = \frac{\beta}{g_m} = \frac{\beta \cdot V_T}{I_{C,Q}} \tag{2.34}$$

Thus, we can approximate the small signal change in the base current as a linear function of v_{be}:

$$i_b = g_\pi \cdot v_{be} = \frac{v_{be}}{r_\pi} \tag{2.35}$$

Eqs. 2.31 and 2.35 are the linearized versions of the BJT transfer, input, and output characteristics, and are collectively known as the BJT *small signal model*. These equations give us a complete picture of what happens to a BJT when we superimpose small signals on top of the DC quiescent voltages and current.

We can create a circuit that can represent the BJT small signal model, called the BJT *small signal equivalent circuit*, as shown in Fig. 2.5. The small signal equivalent circuit represents the small signal model since by writing out the KCL and KVL equations for the equivalent circuit, we will get the BJT small signal model equations. This small signal equivalent circuit becomes extremely convenient when dealing with more complicated circuits containing multiple transistors.

The MOSFET small signal equivalent circuit can be derived using the same procedure used to derive the BJT small signal equivalent circuit. For a MOSFET in the saturation region, its quiescent DC drain current, from Eq. 2.3, is

$$I_{D,Q} = k \cdot (V_{GS,Q} - V_{TH})^2 \cdot (1 + \lambda V_{DS,Q}) \tag{2.36}$$

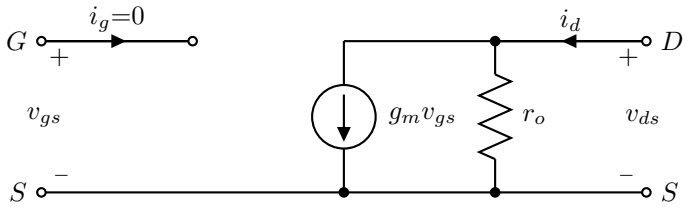


Figure 2.6: The MOSFET small signal equivalent circuit.

Thus, the MOSFET output conductance can be calculated as

$$g_o = \frac{\partial}{\partial V_{DS}} \left(k \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS}) \right) \Big|_{V_{DS}=V_{DS,Q}} = k \cdot (V_{GS} - V_{TH})^2 \cdot \lambda \approx \lambda \cdot I_{D,Q} \tag{2.37}$$

and the corresponding MOSFET output resistance is

$$r_o = \frac{1}{g_o} = \frac{1}{\lambda \cdot I_{D,Q}} \tag{2.38}$$

Since the gate is insulated from the MOSFET channel, $I_G = 0$, therefore $i_g = 0$. This means that whatever v_{gs} we apply to the gate, there will be no change in gate current since it is always zero. If we calculate the MOSFET input conductance, we would get

$$g_\pi = \frac{\partial I_G}{\partial V_{GS}} \Big|_{V_{GS}=V_{GS,Q}} = 0 = \frac{1}{r_\pi} \tag{2.39}$$

resulting in a MOSFET input resistance of

$$r_\pi \to \infty \tag{2.40}$$

Therefore we can write the MOSFET small signal model, linearizing both its transfer and output characteristic, and with $i_g = 0$, as

$$i_d = g_m \cdot v_{gs} + \frac{v_{ds}}{r_o} \tag{2.41}$$

which leads us to the MOSFET small signal equivalent circuit is shown in Fig. 2.6. Note that the form of the BJT small signal equivalent circuit reduces to that of a MOSFET when $\beta \to \infty$, resulting in $r_\pi \to \infty$ and $i_b = 0$.

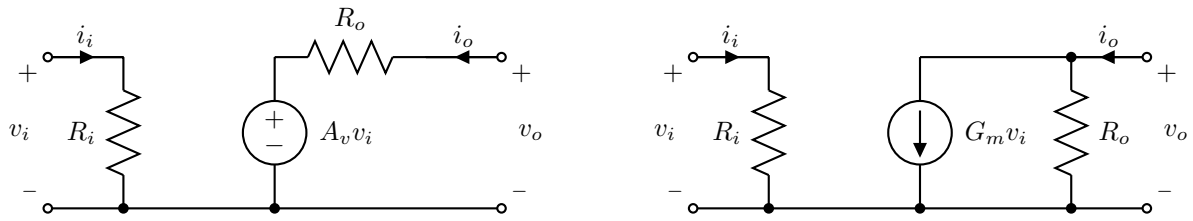
Both the BJT and MOSFET equivalent circuits are the linearized forms of the transistor's large signal characteristics. These small signal equivalent circuits (and models) have the following important characteristics:

- The small signal equivalent circuits are only valid for one operating or quiescent point. Note that the small signal parameters g_m, r_o, and r_π are dependent on the quiescent DC collector or drain current (and hence dependent on the DC voltages as well). If we change these currents, the parameter values of the small signal model (and circuit) will also change.
- These small signal circuits can only relate the "small signal" disturbances on top of the quiescent DC voltages and currents. Small signal analysis discards all the DC information once the linearization process is done. In order to compute the quiescent DC values, the large signal models have to be used.
- Since these circuits are already linear, all the linear circuit properties and analysis techniques (from EEE 31 and 33) are now applicable.

2.2.3 Two-Port Network Analysis

Since our transistor small signal models are linear, and these models have well-defined "input" and "output" ports in the BJT common-emitter and MOSFET common-source configurations, we can use one of the most powerful circuit analysis techniques: two-port network analysis. Two-port analysis allows us to reduce any linear circuit into four parameters, as long as we are only interested in the relationships among two pairs of voltages and currents. The most common two-port representations of circuits use the Z-, Y-, H-, S- and ABCD-parameters.

One of the most powerful uses of two-port network analysis is to enable circuit partitioning, for more intuitive analysis and design. In the case of EEE 51, we will use the unilateral hybrid-π two port representations, as shown in Fig. 2.7, since it will allow us to calculate the effects of adding loads to our amplifiers, such as speakers or other amplifiers. We are assuming unilateral operations for our transistors, meaning that the input voltage or current can



(a) The Thevenin model (b) The Norton model

Figure 2.7: The unilateral hybrid-π two-port network equivalent circuits.

affect the output voltage or current, but the reverse is not true. Thus, for the unilateral hybrid-π equivalent circuit, we only need three two-port parameters. Fig. 2.7 also shows the polarity conventions that we will use in EEE 51.

Fig. 2.7a shows the Thevenin version of the hybrid-π two-port equivalent circuit. It has three parameters: the input resistance, R_i, the output resistance, R_o, and the voltage gain, A_v. The Norton equivalent hybrid-π is shown in Fig. 2.7b, with a circuit transconductance, G_m, instead of the voltage gain parameter. In order to calculate the hybrid-π parameters of any linear circuit, we need to define two circuit operating conditions: the no-load condition, and the zero-input condition.

The *no-load condition* is satisfied when the two-port network does not deliver any power from its output port to a load. Thus, for the Thevenin equivalent circuit in Fig. 2.7a (a voltage output circuit), the output current, i_o should be zero (i.e. an open circuit), and for the Norton equivalent circuit in Fig. 2.7b (a current output circuit), the output voltage, v_o, should be equal to zero (i.e. a short circuit).

The *zero-input condition* is satisfied when the input to the hybrid-π circuit is zero. This means that if a voltage source, v_s is driving the input, then $v_s = 0$. If the input port is being driven by a current source, i_s, then the zero-input condition is satisfied when $i_s = 0$. With these two conditions, we can now define the unilateral hybrid-π parameters.

The input resistance, R_i, is defined as the ratio of the input voltage, v_i, to the input current, i_i, at no load conditions, thus

$$R_i = \left.\frac{v_i}{i_i}\right|_{\text{no-load}} \tag{2.42}$$

Notice that at this point, it seems that the output no-load condition does not really affect the input resistance for the circuits in Fig. 2.7. However, in more complex circuits such as feedback amplifiers, this definition becomes a very important.

Output resistance, R_o, is defined as the ratio of the output voltage, v_o, to the output current, i_o, at zero-input conditions. We can write this as

$$R_o = \left.\frac{v_o}{i_o}\right|_{\text{zero-input}} \tag{2.43}$$

The reason why we take the output impedance at zero-input conditions should be easily seen from Fig. 2.7. Zeroing out the input (either voltage or current), results in $v_i = 0$. Thus, for the Thevenin circuit, $A_v \cdot v_i = 0$, shorting out the dependent voltage source, while for the Norton equivalent, $G_m \cdot v_i = 0$, resulting in the dependent current source acting like an open circuit.

The Thevenin circuit voltage gain, A_v, is defined as the ratio of the output voltage, v_o, to the input voltage, v_i, at no-load conditions:

$$A_v = \left.\frac{v_o}{v_i}\right|_{\text{no-load}} \tag{2.44}$$

For the Thevenin equivalent at no-load conditions, $i_o = 0$, therefore, the voltage drop across the output resistance, R_o, is zero, resulting in $A_v \cdot v_i = v_o$.

The Norton circuit transconductance, G_m, is defined as the ratio of the output current, i_o, to the input voltage, v_i, also at no-load conditions:

$$G_m = \left.\frac{i_o}{v_i}\right|_{\text{no-load}} \tag{2.45}$$

At no-load conditions, $v_o = 0$, thus, the current passing through the output resistance, R_o, is zero, which results in $G_m \cdot v_i = i_o$. Since the Thevenin and Norton circuits are equivalent, we can also express the circuit transconductance as

$$G_m = -\frac{A_v}{R_o} \tag{2.46}$$

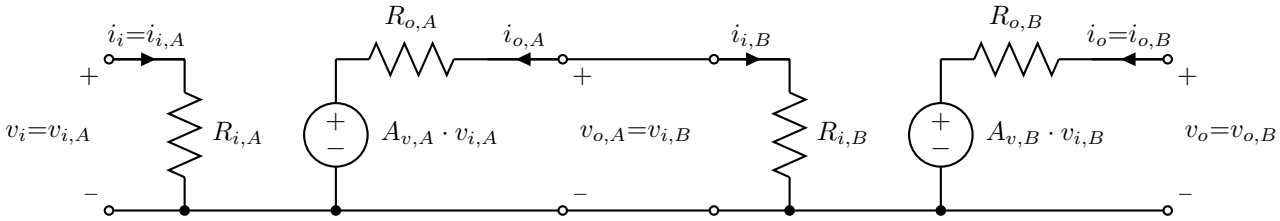


Figure 2.8: Cascading two linear circuits.

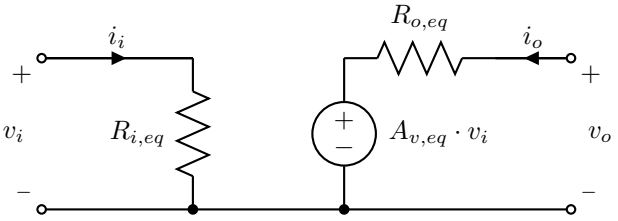


Figure 2.9: The quivalent hybrid-π circuit of the circuit in Fig. 2.8.

The negative sign is due to the polarity of the dependent current source in Fig. 2.7b.

Once we know the hybrid-π two-port equivalent circuit of two linear circuits, we can easily determine the overall behavior of the resulting circuit when these two linear circuits are cascaded. Fig. 2.8 shows two cascaded linear circuits A and B in their respective equivalent hybrid-π representations.

Using voltage division, we can compute the output voltage of circuit A, $v_{o,A}$ as

$$v_{o,A} = A_{v,A} \cdot v_i \cdot \frac{R_{i,B}}{R_{i,B} + R_{o,A}} = v_{i,B} \tag{2.47}$$

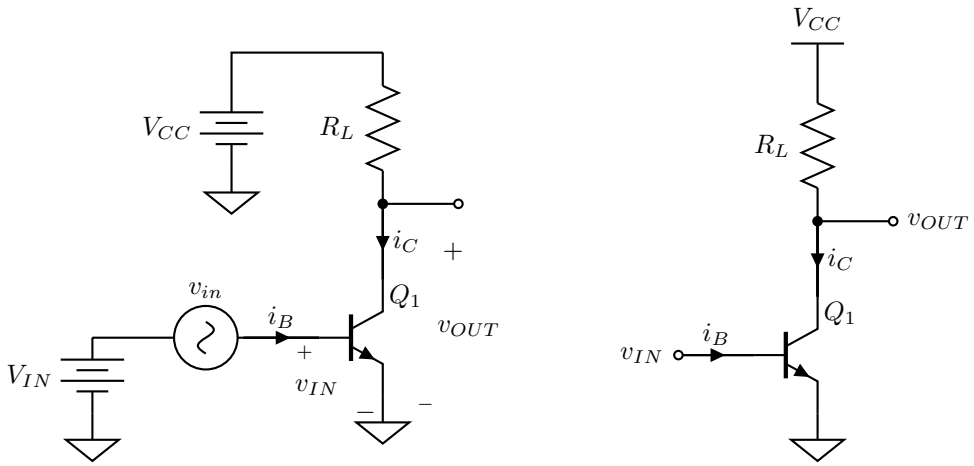
Thus, the equivalent no-load gain from v_i to v_o is

$$A_{v,eq} = \frac{v_o}{v_i} = A_{v,A} \cdot \frac{R_{i,B}}{R_{i,B} + R_{o,A}} \cdot A_{v,B} \tag{2.48}$$

Eq. 2.48 shows how circuit B loads circuit A, reducing the overall no-load voltage gain. If we used the Norton equivalent for circuit A, then we would have used current division instead of voltage division. By applying Eqs. 2.42 and 2.43, we can get the effective input resistance, $R_{i,eq} = R_{i,A}$, and output resistance, $R_{o,eq} = R_{o,B}$. Since the cascade combination of a linear circuit is also a linear circuit, we can derive the equivalent hybrid-π circuit of the circuit in Fig. 2.8, as shown in Fig. 2.9.

Now that we know how to linearize the behavior of an inherently non-linear device, such as a BJT or a MOSFET, when are inputs are small, as well as how to obtain the unilateral hybrid-π two-port quivalent circuit of any linear circuit, we can now apply these techniques to analyze the behavior of single-stage[j] transistor amplifiers.

[j] A single-stage amplifier is a transistor amplifier containing only one transistor as the amplifying element.



(a) Schematic (b) Simplified schematic

Figure 3.1: A simple BJT common-emitter amplifier.

3 Single-Stage Amplifiers

Three different two-port topologies are possible for a 3-terminal transistor. How do we know which one to use for a certain application? As we will see, each topology has its own set of advantages and disadvantages. Here, we look at the characteristics of the 3 different topologies of single-stage BJT amplifiers: (1) the common-emitter, (2) the common-base, and (3) the common-collector amplifiers, as well as their MOSFET equivalents: (1) the common-source, (2) the common-gate, and (3) the common-drain amplifiers. Single-stage amplifiers, such as these ones, are important building blocks in the design of linear electronic amplifiers.

3.1 The Common-Emitter Amplifier

Let's start with the BJT common-emitter (CE) amplifier in Fig. 3.1a. Note that to reduce the clutter of our transistor schematics, and to clearly show the signal path instead of the DC paths, we often use the simplified schematic in Fig. 3.1b. The largest DC voltage is normally referred to as the *supply voltage*, since it is usually responsible for providing the quiescent collector current, or *bias current,* to the transistor. In Fig. 3.1, V_{CC} is the supply voltage. The input voltage, v_{IN} is the sum of its quiescent DC voltage, V_{IN}, and its small signal component, v_{in}, thus

$$v_{IN} = V_{IN} + v_{in} = v_{BE} \tag{3.1}$$

The output voltage, v_{OUT}, of the amplifier is taken at the collector terminal of the transistor, and is referred to ground. It is equal to the transistor collector-emitter voltage, v_{CE}, and is also composed of a quiescent DC voltage, V_{OUT}, as well as small signal voltage, v_{out}.

In order to see how we can use our transistor to amplify signals in this configuration, we need to first get its quiescent DC operating point.

3.1.1 DC Analysis

The goal of DC analysis is to find the quiescent DC (or bias) currents and voltages of our transistors, since this will, in turn, allow us to calculate the transistor small signal parameters. These small signal parameters will then be used to calculate the two-port parameters of the common-emitter amplifier.

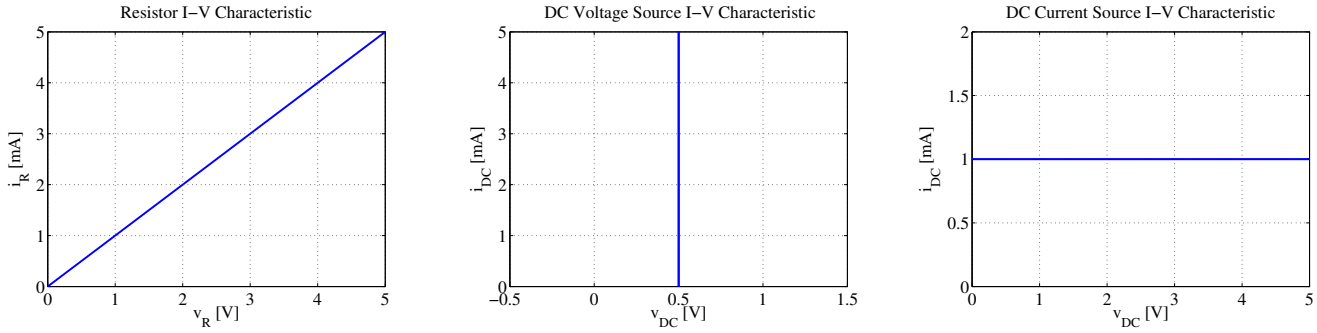
For DC analysis, we set all small signals to zero, leaving us with only the quiescent DC voltages and currents. Writing the KVL equations around the output side of the amplifier, and recognizing that $V_{BE,Q} = V_{IN}$ and $V_{CE,Q} = V_{OUT}$, we get

$$V_{CC} - I_{C,Q}R_L - V_{OUT} = 0 \tag{3.2}$$

If we assume that the transistor is operating in the forward-active region,

$$I_{C,Q} = I_S \cdot \left(e^{\frac{V_{IN}}{V_T}} - 1\right) \cdot \left(1 + \frac{V_{OUT}}{V_A}\right) \tag{3.3}$$

Thus, if we are given the transistor technology parameters I_S, and V_A, the temperature, the values of the DC sources, V_{CC} and V_{IN}, and the resistor R_L, we can use Eqs. 3.2 and 3.3 to solve for $I_{C,Q}$ and V_{OUT}.



(a) A 1 kΩ resistor (b) A 0.5 V DC voltage source (c) A 1 mA DC current source

Figure 3.2: Linear two-terminal I-V characteristics.

If V_{IN} is around 0.6 V, and V_A is large compared to the supply voltage, then we can approximate the quiescent DC collector current as

$$I_{C,Q} = I_S \cdot e^{\frac{V_{IN}}{V_T}} \tag{3.4}$$

Then we can solve for V_{OUT} as

$$V_{OUT} = V_{CC} - I_{C,Q} R_L \tag{3.5}$$

If $V_{OUT} > V_{CE,sat}$, then the transistor is indeed in the forward-active region. This is an easy check to verify our original assumption. After computing the quiescent DC collector current, and given the transistor β, we can easily get the base current using

$$I_{B,Q} = \frac{I_{C,Q}}{\beta} = \frac{I_S}{\beta} \cdot e^{\frac{V_{IN}}{V_T}} \tag{3.6}$$

3.1.2 Small Signal Analysis

From the quiescent DC collector current, we can get the transistor small signal parameters, assuming that the transistor is in the forward-active region:

$$g_m = \frac{I_{C,Q}}{V_T} \tag{3.7}$$

$$r_o = \frac{V_A}{I_{C,Q}} \tag{3.8}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{\beta \cdot V_T}{I_{C,Q}} \tag{3.9}$$

However, aside from the transistor, we have several other components in our circuit in Fig. 3.1. Let us determine the small signal equivalents of linear resistors and independent DC sources. Since these elements are two-terminal devices, we can treat them all as small signal resistances.

The current-voltage (I-V) characteristics of a linear resistor is shown in Fig. 3.2a. The small signal equivalent resistance is again defined as

$$R_{\text{small signal}} = \left(\frac{\partial i_R}{\partial v_R} \right)^{-1} = R \tag{3.10}$$

Since the slope of the I-V characteristic of a linear resistor is the same for any point, then the small signal resistance is independent of the quiescent DC voltage or current. Thus, the small signal equivalent of a linear resistor with resistance R is also a resistor with the same resistance R.

Fig. 3.2b shows the I-V characteristic of a 0.5 V DC voltage source. We note that since the voltage is constant for any current, the slope of the I-V curve is infinite, thus

$$R_{\text{small signal}} = \left(\frac{\partial i_{DC}}{\partial v_{DC}} \right)^{-1} = 0 \tag{3.11}$$

Having a small signal resistance of zero implies that for small signals, independent DC voltage sources act like short circuits. This should be intuitive, since no matter how much small signal current force into the source, there will be

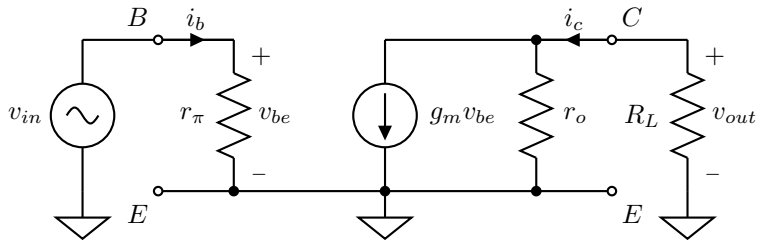


Figure 3.3: The small signal equivalent circuit of the common-emitter amplifier in Fig. 3.1a.

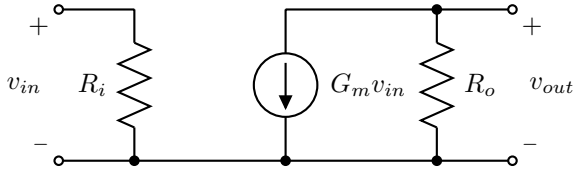


Figure 3.4: Common-emitter amplifier two-port equivalent circuit.

no small signal change in the voltage. Hence, the small signal equivalent of the DC voltage source is a short circuit since the small signal voltage is always zero.

For the independent DC current source, whose I-V characteristic is given in Fig. 3.2c, we can once again determine the equivalent small signal resistance as

$$R_{\text{small signal}} = \left(\frac{\partial i_{DC}}{\partial v_{DC}}\right)^{-1} \to \infty \tag{3.12}$$

Therefore, the small signal equivalent resistance of an independent DC current source is an open circuit. This is due to the fact that no matter what small signal voltage we force across the current source, the current will remain constant, resulting in zero small signal current change.

Using the small signal equivalents of all the components in Fig. 3.1a, the small signal equivalent circuit of the common-emitter amplifier can be obtained, as seen in Fig. 3.3. Again, it is very important to note that the small signal equivalent circuit describes the relationships only between the small voltage or current changes about the quiescent DC operating point. There is no DC (voltage or current) information in the small signal domain.

Given the small signal equivalent circuit of the common-emitter amplifier, we can now derive its equivalent two-port equivalent circuit. Using our two-port parameter definitions, the input resistance of the CE amplifier is

$$R_i = r_\pi = \frac{\beta}{g_m} = \frac{\beta \cdot V_T}{I_{C,Q}} \tag{3.13}$$

The circuit transconductance is then

$$G_m = g_m = \frac{I_{C,Q}}{V_T} \tag{3.14}$$

The output resistance can then be expressed as the parallel combination of r_o and the load resistance, R_L,

$$R_o = r_o \parallel R_L = \frac{V_A}{I_{C,Q}} \parallel R_L \tag{3.15}$$

The CE amplifier two-port equivalent circuit is shown in Fig. 3.4.

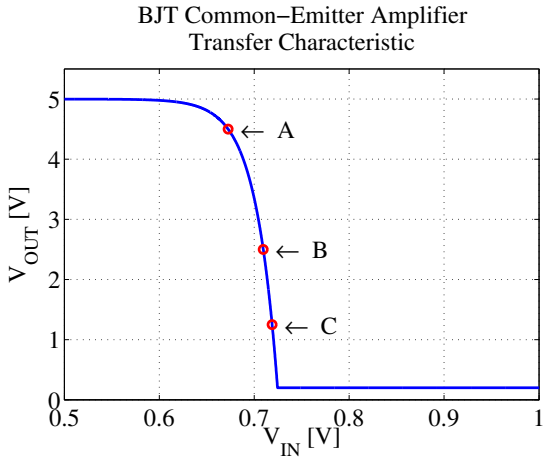
In most cases, we are interested in the small signal voltage gain. Thus,

$$A_v = \frac{v_{out}}{v_{in}} = -G_m R_o = -g_m \left(r_o \parallel R_L\right) = -g_m \cdot \frac{r_o R_L}{r_o + R_L} = -g_m r_o \cdot \frac{R_L}{r_o + R_L} \tag{3.16}$$

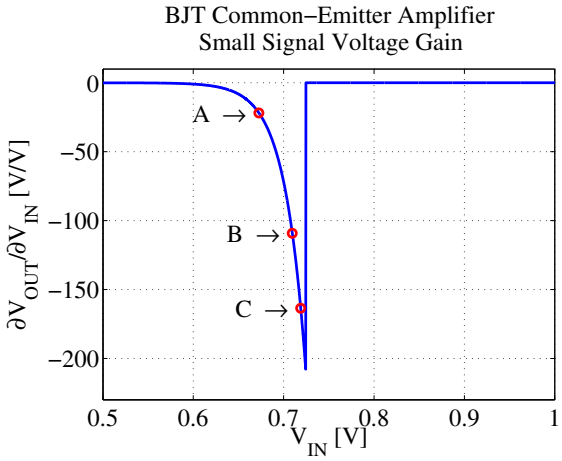
The small signal voltage gain is negative since for the CE amplifier in Fig. 3.1a, a small voltage increase at the input would result in an increase in v_{BE}, resulting in an increase in collector current. This increase in i_C results in an increase in the voltage across R_L, causing the output voltage to drop. Note that an amplifier with a negative small signal gain is called an *inverting amplifier*.

For the CE amplifier in Fig. 3.1a, if we assume that r_o is finite, the maximum small signal voltage gain can be obtained when we let $R_L \to \infty$, resulting in

$$|A_{v,\max}| = a_o = g_m r_o = -\frac{I_{C,Q}}{V_T} \cdot \frac{V_A}{I_{C,Q}} = \frac{V_A}{V_T} = \frac{q \cdot V_A}{kT} \tag{3.17}$$



(a) Large signal transfer curve



(b) Small signal voltage gain

Figure 3.5: Common-emitter characteristics for a transistor with $I_S = 2 \times 10^{-16}\,\text{A}$ and $V_A \to \infty$, using $V_{CC} = 5\,\text{V}$, and $R_L = 500\,\Omega$ at $T = 300\text{K}$.

Eq. 3.17 represents the maximum voltage gain we can get out of a single BJT, also known as the *intrinsic voltage gain*, a_o. Note that any other value of R_L would result in a voltage gain lower than a_o, and that a_o is only dependent on the transistor Early Voltage, and temperature. The intrinsic voltage gain is also a convenient metric that be used to determine if a transistor is suited for a certain circuit or task.

3.1.3 Transistor Operating Regions

Eqs. 3.13 to 3.15 clearly show that the common-emitter small signal two-port equivalent circuit is dependent on the quiescent DC operating point of the transistor. In order to understand the relationship between the DC bias point and the small signal parameters, let us look at the large signal transfer characteristic of the CE amplifier. From Eqs. 3.4 and 3.5, we can express the output DC voltage as

$$V_{OUT} = V_{CC} - R_L \cdot I_S \cdot e^{\frac{V_{IN}}{V_T}} \tag{3.18}$$

Note that Eq. 3.18 is only valid when when the transistor is in the forward active region, that is, when $V_{OUT} > V_{CE,sat}$. For $V_{IN} \approx 0$, V_{OUT} approaches V_{CC}. As V_{IN} is increased, the collector current increases, leading to a decrease in V_{OUT}. The output voltage will decrease until it reaches $V_{CE,sat}$, placing the transistor in saturation, and pinning the output voltage to approximately $V_{CE,sat}$, as we have learned in EEE 41.

The maximum collector current that can flow before the transistor enters the saturation region occurs when $V_{OUT} = V_{CE,sat}$, and can be expressed as

$$I_{C,\text{max}} = \frac{V_{CC} - V_{CE,sat}}{R_L} = I_S \cdot e^{\frac{V_{IN,sat}}{V_T}} \tag{3.19}$$

If the supply voltage is very much greater than $V_{CE,sat}$, then we can approximate Eq. 3.19 as

$$I_{C,\text{max}} \approx \frac{V_{CC}}{R_L} \tag{3.20}$$

Aside from setting the output DC voltage level, and converting the small signal current to a small signal voltage, the load resistance R_L in Fig. 3.1a also limits the maximum collector current that the transistor can draw.

Using Eq. 3.18, and the fact that $V_{OUT} = V_{CE,sat}$ when the transistor is in saturation, we can plot V_{IN} versus V_{OUT}, or the large signal transfer characteristic, of the CE amplifier in Fig. 3.1a, as shown in Fig. 3.5a.

As we expect, the small signal voltage gain is just the slope of the transfer characteristic at a particular bias point. Taking the derivative of Eq. 3.18, we get

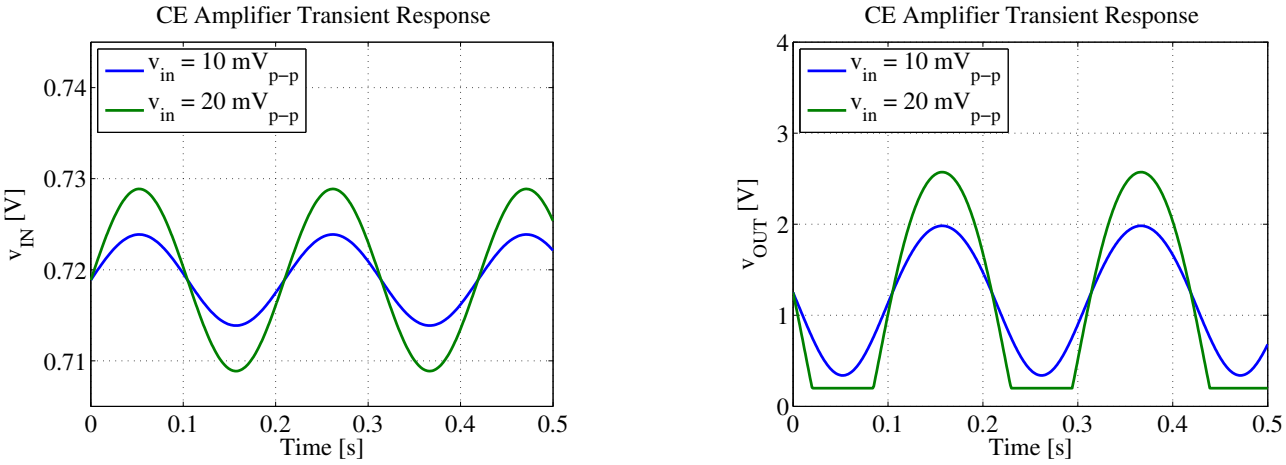
$$\frac{\partial V_{OUT}}{\partial V_{IN}} = -R_L \cdot \frac{I_S}{V_T} \cdot e^{\frac{V_{IN}}{V_T}} = -R_L \cdot \frac{I_{C,Q}}{V_T} = -g_m R_L \tag{3.21}$$

Since Eq. 3.18 assumes that $V_A \to \infty$, the resulting small signal transistor output impedance, r_o, will also approach infinity, reducing Eq. 3.16 to Eq. 3.21.

As we can see from Figs. 3.5a and 3.5b, choosing different values for the DC input voltage, V_{IN}, would result in different quiescent collector currents, leading to different quiescent output voltages and small signal gains.

Table 3.1: Biasing the common-emitter amplifier described in Fig. 3.5a.

	V_{IN} [mAV]	$I_{C,Q}$ [mA]	V_{OUT} [V]	A_v $\left[\frac{\text{V}}{\text{V}}\right]$
Point A	672.5	1	4.5	−21.7
Point B	709.5	5	2.5	−108.7
Point C	718.9	7.5	1.25	−163.0



(a) Input voltage (b) Output voltage

Figure 3.6: BJT common-emitter amplifier transient response when (a) it is biased at point C, and (b) a small signal input sinusoid is applied.

For example, choosing $V_{IN} = 709.5\,\text{mV}$, and using Eqs. 3.4 and 3.18, results in $I_{C,Q} = 5\,\text{mA}$, and $V_{OUT} = 2.5\,\text{V}$, corresponding to point B in Fig. 3.5a. Then, by using Eq. 3.21, we get $A_v = -108.7\,\frac{\text{V}}{\text{V}}$, corresponding to point B in Fig. 3.5b. Note that choosing either point A or point C in Fig. 3.5a would result in different small signal gains, as seen in Fig. 3.5b and Table 3.1.

Choosing a Bias Point: A common question in the design of linear amplifiers is "What bias point should we use?". Clearly, if we want the largest possible gain, we would bias the CE amplifier near point C in Fig. 3.5b. However, let us look at the implications of using point C as our bias point.

If we apply a sinusoidal small signal voltage, v_{in}, to the input of our CE amplifier, we would get the transient waveforms in Fig. 3.6. For $v_{in} = 10\,\text{mV}_{\text{p-p}}$, we will get an output sinusoid, $v_{out} \approx 1.6\,\text{V}_{\text{p-p}}$, as expected. However, if we increase v_{in} to $20\,\text{mV}_{\text{p-p}}$, we see that the output is distorted[a], as seen in Fig. 3.6b. The clipping of the lower part of the output sinusoid is due to the transistor's entry into its saturation region. This is due to the fact that the increase in collector current, increases the voltage across R_L, reducing the transistor's V_{CE} until it reaches $V_{CE,sat}$. Note that in the saturation region, $v_{OUT} = V_{CE,sat} \approx 0.2\,\text{V}$, independent of the input, v_{in}.

The maximum symmetric[b] peak-to-peak output voltage of an amplifier is known as its *output swing*. For the CE amplifier at bias point C, the output swing is limited by the largest negative output voltage that would keep the BJT in its forward-active region. Thus, to keep the transistor $V_{CE} > V_{CE,sat}$, we should satisfy the relation $V_{OUT} - |v_{out}| > V_{CE,sat}$ on the negative swing of v_{out}. Therefore, the output swing can be expressed as

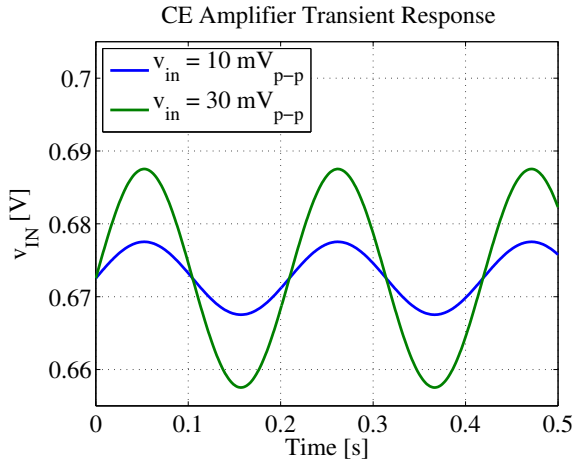
$$v_{out,\max} = 2 \cdot (V_{OUT} - V_{CE,sat}) = 2 \cdot (1.25 - 0.2)\ \text{V} = 2.1\,\text{V} \tag{3.22}$$

On the other hand, let us examine what happens when choose point A in Fig. 3.5a as our bias point. Again if we apply a sinusoidal small signal voltage, v_{in}, to the input of our CE amplifier biased at point A, we would get the transient waveforms in Fig. 3.7.

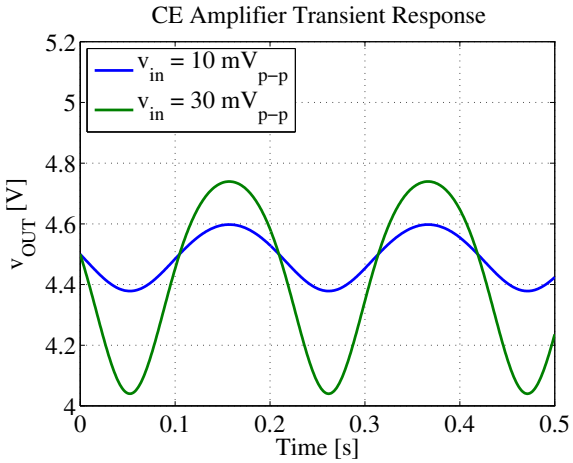
As seen in Fig. 3.7, applying $v_{in} = 10\,\text{mV}_{\text{p-p}}$ results in $v_{out} \approx 210\,\text{mV}_{\text{p-p}}$, again as expected, given that the calculated small signal gain is $-21.7\,\frac{\text{V}}{\text{V}}$. Increasing the input to $30\,\text{mV}_{\text{p-p}}$ results in an asymmetric output sinusoid, as seen in Fig. 3.7b. The negative output swing can accommodate the gain, however, the positive swing is now limited by the low-gain region in Fig. 3.5b. This is due to the fact that the quiescent DC output voltage, V_{OUT}, of point A is very close to the supply voltage, V_{CC}. Thus, for the output voltage to reach V_{CC}, the voltage across R_L has

[a] Distortion is a measure of how different a signal is from a perfect sinusoid. Strictly speaking, all semiconductor amplifiers exhibit a certain amount of distortion when a perfect sinusoid is applied at its input. However, here we mean the distortion due to the clipping or flattening of the peaks of the sinusoid.

[b] The positive swing should be equal to the negative swing about the quiescent DC point.

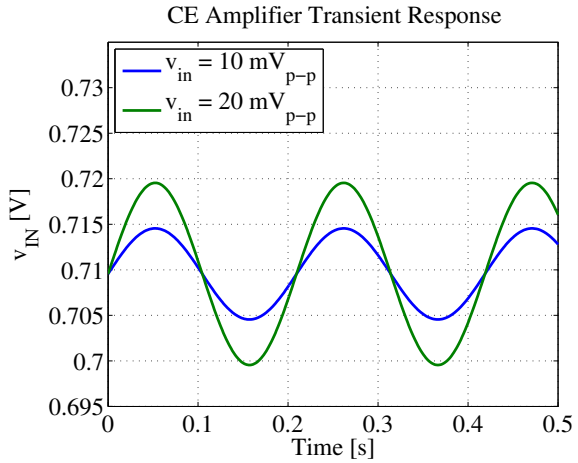


(a) Input voltage

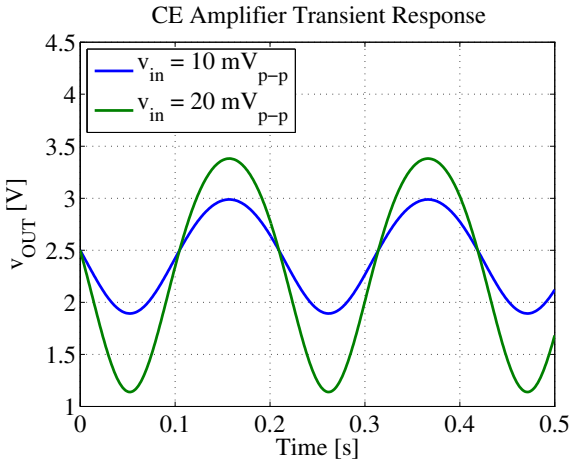


(b) Output voltage

Figure 3.7: BJT common-emitter amplifier transient response when (a) it is biased at point A, and (b) a small signal input sinusoid is applied.



(a) Input voltage



(b) Output voltage

Figure 3.8: BJT common-emitter amplifier transient response when (a) it is biased at point B, and (b) a small signal input sinusoid is applied.

to be very small, requiring a larger negative small signal input voltage. Note that for the output to reach V_{CC}, the transistor needs to be placed in its cut-off region, where the collector current is zero.

A good tradeoff between gain and output swing would be to bias the common-emitter amplifier at point B. Thus, by placing the output DC voltage at around half the supply voltage, we would get a relatively large output swing without significant loss in voltage gain. The transient response of the common-emitter amplifier biased at point B is shown in Fig. 3.8.

For a small signal input voltage of $10\,\mathrm{mV_{p-p}}$, the resulting small signal output voltage has a peak-to-peak value of around 1.1 V, consistent with our computed small signal gain of $-108.7\,\frac{\mathrm{V}}{\mathrm{V}}$ in Table 3.1. Increasing the input to $20\,\mathrm{mV_{p-p}}$ results in the output waveform in Fig. 3.8b. Note that the output exhibits less flattening during the positive cycle of the sinusoid, while clipping is avoided during the negative cycle.

It is also important to note that the DC power the amplifier needs depends on the bias point. For the common-emitter amplifier in Fig. 3.1a, we can calculate the quiescent DC power as

$$P_{DC} = V_{CC} I_{C,Q} + V_{IN} I_{B,Q} \tag{3.23}$$

As we can see in Eq. 3.23, a larger the quiescent DC collector current would result in a larger transconductance, but would also consume more power. This tradeoff between gain, output swing and power is common in designing electronic amplifiers.

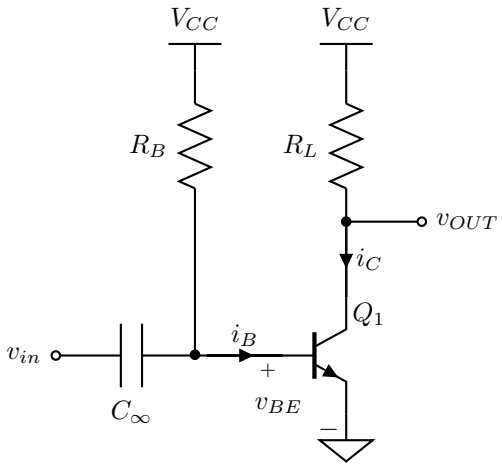


Figure 3.9: A fixed-bias common-emitter amplifier.

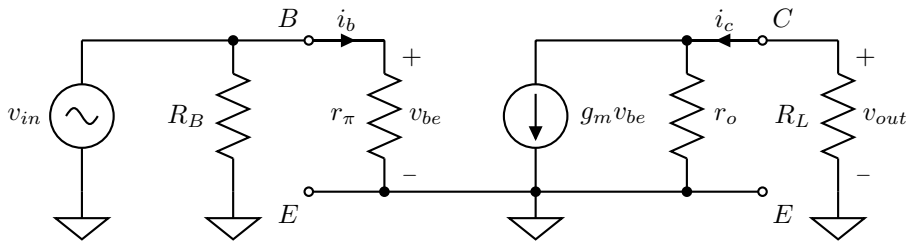


Figure 3.10: The small signal model of the fixed-bias CE amplifier in Fig. 3.9.

3.1.4 The Fixed-Bias Common-Emitter Amplifier

Biasing the common-emitter amplifier using two DC voltage sources is costly, and sometimes, depending on where the amplifier is used, using two DC voltage sources is not possible at all. Thus, an alternative to the biasing strategy used in Fig. 3.1a is to use a resistor to generate the quiescent base-emitter DC voltage, as shown in Fig. 3.9.

The input is coupled into the base of the transistor using an infinitely large capacitor, C_∞. By using C_∞, we prevent any DC current from flowing into the small signal input source, thus, preserving the DC bias point of the amplifier. Also, since the capacitor is infinitely large, any non-DC small signal v_{in} will just see a short circuit directly to the base of the transistor, and will pass through the capacitor without any attenuation.

We can calculate the bias point by writing out the KVL equation for the base loop as

$$V_{CC} - I_{B,Q}R_B - V_{BE} = 0 \tag{3.24}$$

Substituting Eq. 3.4 into Eq. 3.24, and expressing everything in terms of $I_{C,Q}$, we get

$$V_{CC} - \frac{I_{C,Q}}{\beta}R_B - V_T \ln\left(\frac{I_{C,Q}}{I_S}\right) = 0 \tag{3.25}$$

Using Eq. 3.25, we can solve for the quiescent DC collector current. However, solving a nonlinear (exponential) equation is not as easy as solving a linear one[c].

One way to quickly estimate the quiescent DC collector current is to use the approximation

$$V_{BE} \approx 0.7\,\text{V} \tag{3.26}$$

As seen in Table 3.1, the quiescent DC base-emitter voltage will be about 0.7 V, even for a relatively large range of collector currents. Thus, if we are expecting currents in the order of 1 mA to 10 mA, then using Eq. 3.26 would give a fairly good estimate of $I_{C,Q}$. Using Eqs. 3.24 and 3.26, we can calculate $I_{C,Q}$ as

$$I_{C,Q} = \beta \cdot \frac{V_{CC} - 0.7\,\text{V}}{R_B} \tag{3.27}$$

Once we know $I_{C,Q}$, we can easily get the quiescent DC operating points $I_{B,Q}$ and V_{OUT}, as well as the transistor small signal parameters g_m, r_o and r_π. The small signal equivalent circuit of the fixed-bias CE amplifier is shown in Fig. 3.10.

[c]It is common to solve these nonlinear equations by numerical, iterative, or graphical methods.

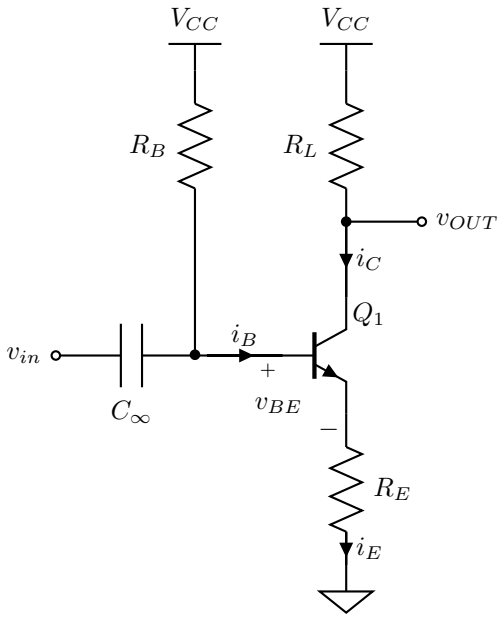


Figure 3.11: The emitter degenerated common-emitter amplifier.

Note that this small signal equivalent circuit is almost the same as the one in Fig. 3.3, except that the input resistance now becomes

$$R_i = r_\pi \parallel R_B \tag{3.28}$$

3.1.5 Emitter Degeneration

One of the assumptions we have made so far is that the transistor β is constant. However, in real transistors, due to limitations in the manufacturing process, β could vary by as much as $\pm 50\%$ from its nominal[d] value, and furthermore, β doubles for every $80\,\mathrm{C}^\circ$ rise in temperature. If we built ten copies of the fixed-bias CE amplifier in Fig. 3.9, and from Eq. 3.27, we would expect to get 10 amplifiers with small signal parameters, and output DC voltages, also varying by $\pm 50\%$.

In some cases, this variation in parameters is acceptable, but in most cases, we want circuits that we can mass produce, but can maintain tighter tolerances, say less than $\pm 1\%$, in terms of parameter variability.

One way to reduce the effect of β variation is to use emitter degenerated CE amplifiers, such as the one shown in Fig. 3.11.

To determine the quiescent DC collector current, we write out the KVL equation for the input loop

$$V_{CC} - I_{B,Q}R_B - V_{BE} - I_{E,Q}R_E = 0 \tag{3.29}$$

Thus, using Eq. 3.26 and expressing $I_{B,Q}$ and $I_{E,Q}$ in terms of $I_{C,Q}$, we get

$$V_{CC} - \frac{I_{C,Q}}{\beta}R_B - 0.7\,\mathrm{V} - I_{C,Q}\left(1 + \frac{1}{\beta}\right)R_E = 0 \tag{3.30}$$

Solving for the quiescent DC collector current, $I_{C,Q}$,

$$I_{C,Q} = \frac{V_{CC} - 0.7\,\mathrm{V}}{\frac{R_B}{\beta} + \left(1 + \frac{1}{\beta}\right)R_E} = \beta \cdot \frac{V_{CC} - 0.7\,\mathrm{V}}{R_B + (\beta + 1)\cdot R_E} \tag{3.31}$$

Note that if β is large, that is if $\beta \gg 1$, and if $\beta \cdot R_E \gg R_B$, we can express Eq. 3.31 as

$$I_{C,Q} \approx \frac{V_{CC} - 0.7\,\mathrm{V}}{R_E} \tag{3.32}$$

which is independent of β!

Another way of looking at Eq. 3.32 is when $\beta \to \infty$, $I_{B,Q} \to 0$. This leads to the voltage across R_B being reduced to zero, and hence, leads to Eq. 3.32.

[d]For example, if we have 1000 pieces of the NPN BJT 2N2222A, with $\beta = 100$ as indicated in the data sheet, and if we expect $\pm 50\%$ β variation, we would probably find some of the transistors to have β values as low as 50, or some as high as 200.

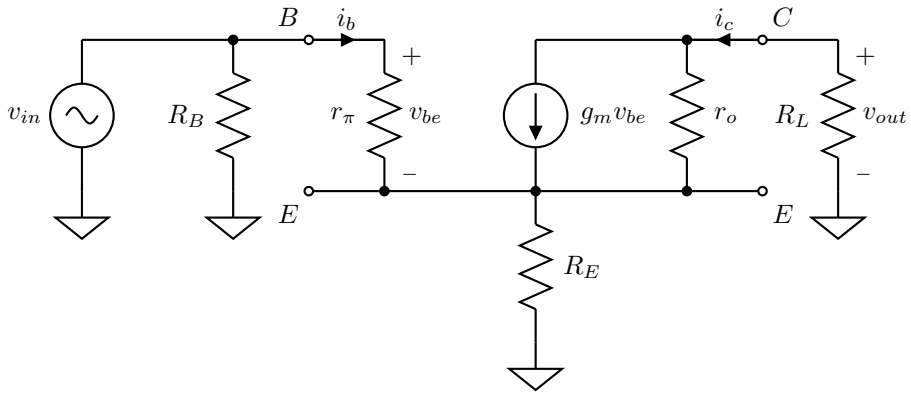


Figure 3.12: The small signal equivalent circuit of the emitter-degenerated CE amplifier in Fig. 3.11.

β Sensitivity: One way to quantify the effect of β on the quiescent DC collector current is to compute the *sensitivity* of $I_{C,Q}$ to β. Sensitivity is expressed as

$$S_\beta^{I_{C,Q}} = \frac{\partial I_{C,Q}}{\partial \beta} \tag{3.33}$$

Thus, for a circuit with a lower the sensitivity, varying β would have a smaller effect on $I_{C,Q}$.

Calculating the sensitivity of the quiescent DC collector current to the β value of the fixed-bias CE amplifier in Fig. 3.9, we would get

$$S_\beta^{I_{C,Q}} = \frac{\partial I_{C,Q}}{\partial \beta} = \frac{V_{CC} - 0.7\,\text{V}}{R_B} \tag{3.34}$$

While for the emitter-degenerated CE amplifier in Fig. 3.11, we have

$$S_\beta^{I_{C,Q}} = \frac{\partial I_{C,Q}}{\partial \beta} = \frac{V_{CC} - 0.7\,\text{V}}{R_B} \cdot \frac{1 + \frac{R_E}{R_B}}{\left(1 + (\beta + 1)\,\frac{R_E}{R_B}\right)^2} \tag{3.35}$$

Comparing Eqs. 3.34 and 3.35, we can see that as $\beta \to \infty$, the sensitivity of the emitter-degenerated CE amplifier goes to zero, while the sensitivity of the fixed-bias CE amplifier remains constant.

Notice that the quiescent DC output voltage is now

$$V_{OUT} = V_{CE} + I_{E,Q} R_E \tag{3.36}$$

Thus, if we want to set the quiescent DC output voltage to $\frac{V_{CC}}{2}$, as well as place the transistor in its forward-active region ($V_{CE} > V_{CE,sat}$), we need to make sure that

$$R_E < \frac{\frac{V_{CC}}{2} - V_{CE,sat}}{I_{C,Q}\left(1 + \frac{1}{\beta}\right)} \tag{3.37}$$

Note that Eq. 3.37 is obtained by rearranging Eq. 3.36. For example, if $V_{CC} = 5\,\text{V}$, $V_{CE,sat} = 0.2\,\text{V}$, $\beta = 100$, and $I_{C,Q} = 1\,\text{mA}$, the value of R_E should be less than $2.28\,\text{k}\Omega$, which is relatively small compared to r_o and r_π.

Once we have obtained the quiescent DC collector current, we can now determine the small signal parameters of the transistor, as well as draw the small signal equivalent circuit of the emitter-degenerated CE amplifier, as shown in Fig. 3.12.

In order to reduce the complexity of our calculations, we can first solve for the two-port Norton equivalent circuit of the transistor small signal model together with R_E, ignoring R_B and R_L for now, as shown in Fig. 3.13.

In order to get the effective transconductance of the transistor with R_E, we short the output to ground, and solve for $G'_m = \frac{i'_{out}}{v'_{in}}$, where i'_{out} is the output short-circuit current. Writing the KCL equation at the emitter node, and recognizing that $v_{be} = v'_{in} - v'_e$, we get

$$\frac{v'_e - v'_{in}}{r_\pi} + \frac{v'_e}{R_E} + \frac{v'_e}{r_o} - g_m\,(v'_{in} - v'_e) = 0 \tag{3.38}$$

Solving for v'_e, we get

$$v'_e = v'_{in} \cdot \frac{g_m + \frac{1}{r_\pi}}{g_m + \frac{1}{r_\pi} + \frac{1}{r_o} + \frac{1}{R_E}} \tag{3.39}$$

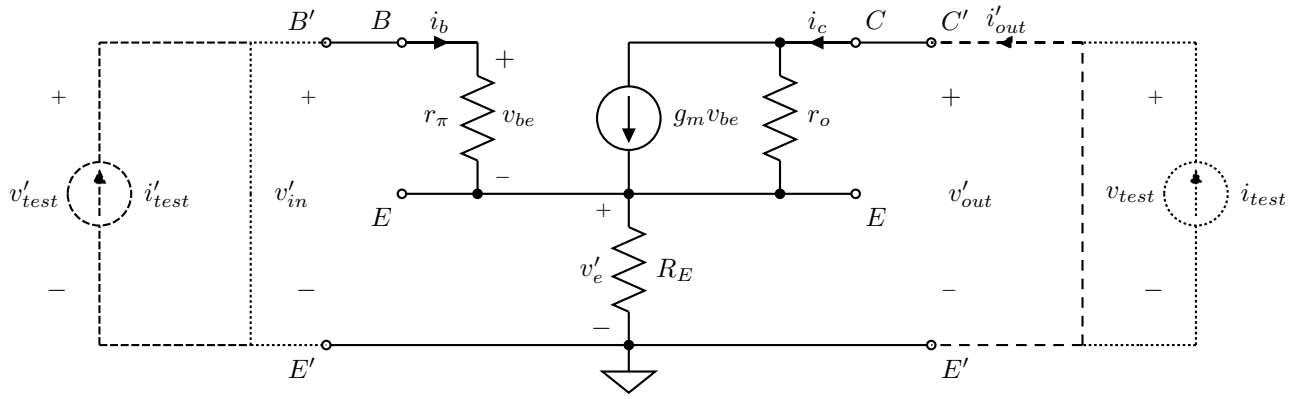


Figure 3.13: The small signal model of the emitter-degenerated NPN BJT.

The short-circuit output current is then

$$i'_{out} = g_m\left(v'_{in} - v'_e\right) - \frac{v'_e}{r_o} = v'_{in} \cdot g_m \cdot \frac{\frac{1}{R_E} - \frac{1}{r_o g_m r_\pi}}{g_m + \frac{1}{r_\pi} + \frac{1}{r_o} + \frac{1}{R_E}} \tag{3.40}$$

Thus,

$$G'_m = \frac{i'_{out}}{v'_{in}} = g_m \cdot \frac{\frac{1}{R_E} - \frac{1}{r_o g_m r_\pi}}{g_m + \frac{1}{r_\pi} + \frac{1}{r_o} + \frac{1}{R_E}} \tag{3.41}$$

Eq. 3.41 is relatively complex and does not give us much intuition regarding the effect of R_E. However, if we simplify Eq. 3.41 by assuming $g_m r_o \gg 1$, $g_m r_\pi = \beta \gg 1$, $R_E \ll r_o$, and $R_E \ll r_\pi$, we get

$$G'_m \approx g_m \cdot \frac{\frac{1}{R_E}}{g_m + \frac{1}{R_E}} = \frac{g_m}{1 + g_m R_E} < g_m \tag{3.42}$$

Since $(1 + g_m R_E) > 1$, Eq. 3.42 shows that the effective transconductance of the transistor and R_E circuit is lower than the transconductance of the transistor without R_E. Thus, we say that the transconductance is *degenerated* by the degenerating resistor, R_E.

The effective output resistance can be calculated by applying a test voltage at the output and measuring the current, when the input small signal voltage is set to zero. However, in this case, let us apply a test current source, i_{test}, at the output, and measure the resulting output voltage, v_{test}. Since the circuit is linear, we should get the same result.

Applying i_{test} at the output, and recognizing that r_π is now parallel to R_E when the input small signal voltage is set to zero, gives us

$$v'_e = i_{test} \cdot (r_\pi \parallel R_E) \tag{3.43}$$

And since $v_{be} = -v'_e$ when the input is shorted to ground, the current through the output impedance, r_o is

$$i_{r_o} = i_{test} - g_m v_{be} = i_{test} + g_m v'_e = i_{test}\left(1 + g_m\left(r_\pi \parallel R_E\right)\right) \tag{3.44}$$

Thus, the output voltage, v_{test} is equal to

$$v_{test} = i_{r_o} r_o + v'_e = i_{test}\left(r_o + g_m r_o\left(r_\pi \parallel R_E\right) + \left(r_\pi \parallel R_E\right)\right) \tag{3.45}$$

The effective output impedance of the transistor with emitter degeneration can then be expressed as

$$R'_o = \frac{v_{test}}{i_{test}} = r_o + g_m r_o\left(r_\pi \parallel R_E\right) + \left(r_\pi \parallel R_E\right) \tag{3.46}$$

Using the same set of assumptions we used for Eq. 3.42, we can simplify Eq. 3.46 as

$$R'_o \approx r_o + R_E + g_m r_o R_E \approx r_o + g_m r_o R_E = r_o\left(1 + g_m R_E\right) > r_o \tag{3.47}$$

Notice that degenerating the transistor by R_E increases its output resistance by a factor $(1 + g_m R_E)$.

Computing the effective input resistance of the emitter-degenerated transistor is similar to computing the output resistance, except that we apply the test current, i'_{test}, at the input, and measure the resulting input test voltage, v'_{test}, when the output is shorted to zero, the Norton no-load condition.

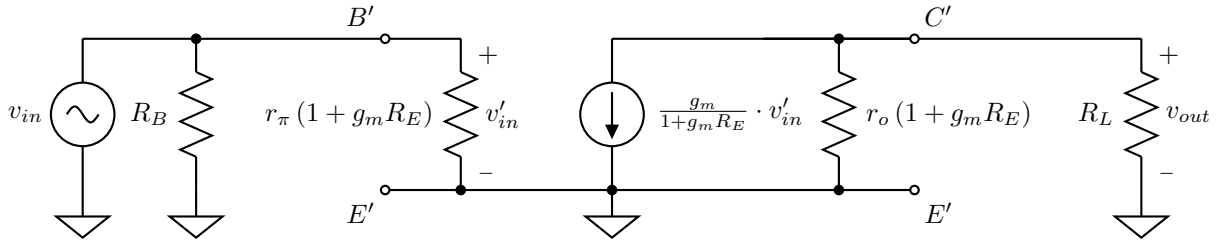


Figure 3.14: The emitter-degenerated common-emitter amplifier small signal model in Fig. 3.12 using the derived effective two-port model of the emitter-degenerated transistor.

Applying i'_{test}, and recognizing that $v_{be} = i'_{test}r_\pi$ and that R_E and r_o are connected in parallel, we can get the voltage across the parallel combination of R_E and r_o as

$$v'_e = (i'_{test} + g_m v_{be}) \cdot (R_E \parallel r_o) = i'_{test}\,(1 + g_m r_\pi) \cdot (R_E \parallel r_o) \tag{3.48}$$

Thus, we can calculate v'_{test} as

$$v'_{test} = v_{be} + v'_e = i'_{test}\,(r_\pi + (R_E \parallel r_o) + g_m r_\pi\,(R_E \parallel r_o)) \tag{3.49}$$

Therefore, the effective input resistance of the emitter-degenerated transistor is

$$R'_i = \frac{v'_{test}}{i'_{test}} = r_\pi + (R_E \parallel r_o) + g_m r_\pi\,(R_E \parallel r_o) \tag{3.50}$$

Again, using the assumptions we used for Eq. 3.42, we can simplify Eq. 3.50 as

$$R'_i \approx r_\pi + R_E + g_m r_\pi R_E \approx r_\pi + g_m r_\pi R_E = r_\pi\,(1 + g_m R_E) > r_\pi \tag{3.51}$$

Once again, note that degenerating the transistor by R_E increases its input resistance of the BJT by a factor $(1 + g_m R_E)$.

Using the small signal model of the emitter-degenerated transistor, we can now draw the two-port small signal equivalent circuit of the common-emitter amplifier with emitter degeneration, as shown in Fig. 3.14.

By inspecting Fig. 3.14, we can easily see that the effective transconductance, G_m, of the emitter degenerated CE amplifier is

$$G_m = \frac{g_m}{1 + g_m R_E} \tag{3.52}$$

and for the case when $R_L \ll r_o\,(1 + g_m R_E)$ and $R_B \ll r_\pi\,(1 + g_m R_E)$, the output and input resistances can be expressed as

$$R_o = R_L \parallel r_o\,(1 + g_m R_E) \approx R_L \tag{3.53}$$

$$R_i = R_B \parallel r_\pi\,(1 + g_m R_E) \approx R_B \tag{3.54}$$

The small signal voltage gain is then

$$A_v = -G_m R_o \approx -\frac{g_m R_L}{1 + g_m R_E} \tag{3.55}$$

Again, note that the small signal voltage gain is degraded or degenerated by R_E. It is interesting to node that if $g_m R_E \gg 1$, then the voltage gain approaches $-\frac{R_L}{R_E}$, which is independent of the transistor parameters![e]

Thus, the consequences of reducing the effect of β variations on the quiescent DC collector current include (1) reduced small signal voltage gain, (2) increased small signal input resistance, and (3) increased small signal output resistance.

[e] We will revisit this result in the feedback amplifiers section.

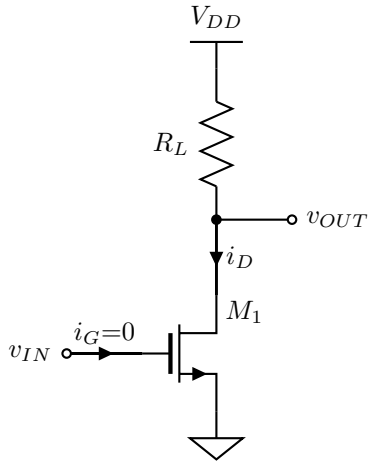


Figure 3.15: The common-source amplifier.

3.3 The Common-Source Amplifier

Similar to the common-emitter amplifier, the MOSFET common-source amplifier, shown in Fig. 3.15, utilizes the quadratic relationship between the drain current and gate-to-source voltage to provide voltage gain.

Given the input quiescent DC voltage, and recognizing that this is equal to the quiescent gate-to-source voltage, and assuming that the MOSFET is in the saturation region, we can determine the quiescent drain current, $I_{D,Q}$,

$$I_{D,Q} = k \cdot (V_{IN} - V_{TH})^2 \cdot (1 + \lambda V_{OUT}) \tag{3.57}$$

The channel length modulation parameter, λ, is usually in the order of $0.01\,\mathrm{V}^{-1}$, and for supply voltages of around $5\,\mathrm{V}$,

$$\lambda V_{OUT} \ll 1 \tag{3.58}$$

Thus Eq. 3.57 can be approximated as

$$I_{D,Q} = k \cdot (V_{IN} - V_{TH})^2 \tag{3.59}$$

The KVL equation for the output loop can be written as

$$V_{DD} - I_{D,Q} R_L - V_{OUT} = 0 \tag{3.60}$$

Plugging in Eq. 3.59 into Eq. 3.60 gives us the quiescent output DC voltage

$$V_{OUT} = V_{DD} - R_L \cdot k \cdot (V_{IN} - V_{TH})^2 \tag{3.61}$$

Recall that an important fundamental difference between BJTs and MOSFETs is the boundary between the desired operating region (forward-active for BJTs and saturation for MOSFETs) and the low V_{OUT} region (saturation for BJTs and linear or ohmic for MOSFETs). For a common-emitter amplifier, the BJT goes into saturation when $V_{CE} \leq V_{CE,sat}$. However, in a common-source amplifier, the MOSFET goes into the linear region when

$$V_{DS} \leq V_{GS} - V_{TH} \tag{3.62}$$

Again, note that this boundary between the MOSFET linear and saturation regions is dependent on the quiescent DC operating point, unlike $V_{CE,sat}$ which can be treated as a constant. In the linear or ohmic region, the MOSFET behaves like a nonlinear resistor, whose current is given by

$$I_{D,Q} = 2k \cdot \left((V_{IN} - V_{TH})\, V_{OUT} - \frac{V_{OUT}^2}{2} \right) \tag{3.63}$$

In the linear region, the relationship between $I_{D,Q}$ and V_{GS} is no longer quadratic, but is now linear, hence the name of the operating region. Thus, the transconductance, g_m, in the linear region is smaller, leading to lower voltage gain. Therefore, to prevent the MOSFET from going into the linear region, the minimum output voltage of the common-source amplifier is

$$V_{OUT,\mathrm{min}} = V_{IN} - V_{TH} \tag{3.64}$$

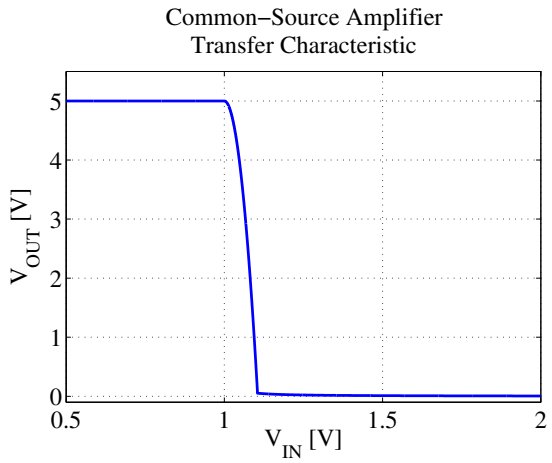


Figure 3.16: The common-source amplifier large signal transfer characteristic for $k = 90\,\frac{\text{mA}}{\text{V}^2}$, $V_{TH} = 1\,\text{V}$, $\lambda \to 0$, $V_{DD} = 5\,\text{V}$, and $R_L = 5\,\text{k}\Omega$.

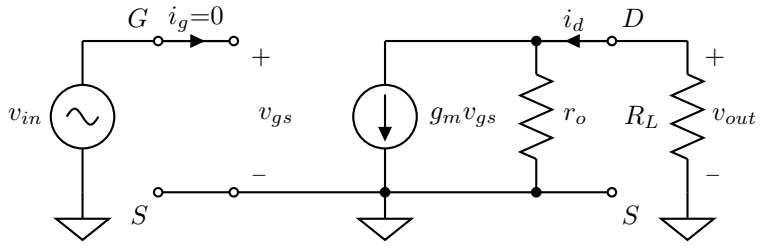


Figure 3.17: The small signal equivalent circuit of the common-source amplifier in Fig. 3.15.

Combining Eq. 3.63 into Eq. 3.60, and assuming that the output voltage is small such that the $\frac{V_{OUT}^2}{2}$ term in Eq. 3.63 is negligible, we can express the output quiescent DC voltage when the transistor is in the linear region as

$$V_{OUT} \approx \frac{V_{DD}}{1 + 2k \cdot (V_{IN} - V_{TH}) \cdot R_L} \tag{3.65}$$

Also, we can use the relationship $V_{OUT} \approx V_{DD}$ when $V_{IN} < V_{TH}$. This is due to our assumption that when the gate-to-source voltage is less than the threshold voltage, $I_{D,Q} \approx 0$. We can then use Eqs. 3.61 and 3.65 to plot the large signal common-source amplifier transfer characteristic, as shown in Fig. 3.16.

Once we have determined the quiescent DC drain current, we can now determine the small signal parameters of the MOSFET as

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{I_D = I_{D,Q}} = 2k \cdot (V_{IN} - V_{TH}) = \sqrt{4k \cdot I_{D,Q}} = \frac{2 \cdot I_{D,Q}}{V_{IN} - V_{TH}} \tag{3.66}$$

$$r_o = \left.\frac{\partial V_{DS}}{\partial I_D}\right|_{I_D = I_{D,Q}} = \frac{1}{\lambda I_{D,Q}} \tag{3.67}$$

$$r_\pi = \left.\frac{\partial V_{GS}}{\partial I_G}\right|_{I_D = I_{D,Q}} \to \infty \tag{3.68}$$

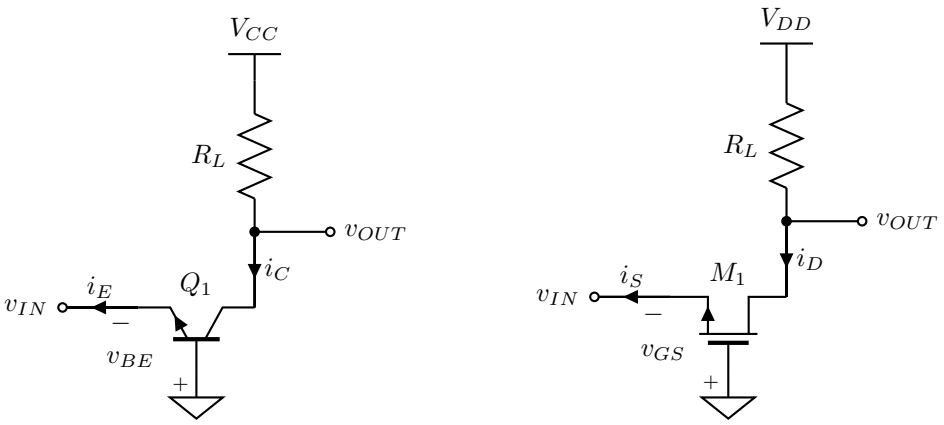
The small signal equivalent circuit of the common-source amplifier is shown in Fig. 3.17. It is interesting to note that the transconductance of a BJT is proportional to $I_{C,Q}$, while that of a MOSFET is proportional to $\sqrt{I_{D,Q}}$. Thus, for the same bias current, we can obtain a higher transconductances in BJTs.

After deriving the small signal transistor parameters, we can easily determine the hybrid-π two-port parameters. By inspection, we can see that

$$G_m = g_m = \sqrt{4k \cdot I_{D,Q}} \tag{3.69}$$

$$R_o = r_o \parallel R_L = \frac{1}{\lambda I_{D,Q}} \parallel R_L \tag{3.70}$$

$$R_i \to \infty \tag{3.71}$$



(a) The common-base amplifier (b) The common-gate amplifier

Figure 3.18

The voltage gain is then

$$A_v = -G_m R_o = -g_m \left(r_o \parallel R_L\right) \tag{3.72}$$

If $r_o \gg R_L$, the voltage gain can be approximated as

$$A_v \approx -g_m R_L = -2k \cdot R_L \cdot (V_{IN} - V_{TH}) = -R_L \sqrt{4k \cdot I_{D,Q}} \tag{3.73}$$

The intrinsic voltage gain, a_o, of a MOSFET is given as

$$a_o = -g_m r_o = -\frac{\sqrt{4k \cdot I_{D,Q}}}{\lambda I_{D,Q}} = -\frac{1}{\lambda}\sqrt{\frac{4k}{I_{D,Q}}} = -\frac{2}{\lambda\left(V_{IN} - V_{TH}\right)} \tag{3.74}$$

Note that unlike the BJT, the MOSFET intrinsic gain is dependent on its quiescent DC operating point.

Though there are fundamental differences between BJTs and MOSFETs, as soon as we obtain (or select) the quiescent DC collector or drain currents, the small signal characteristics turn out to be the same. In the case of the common-emitter and common-source amplifiers, their small signal behavior is the described by the same equivalent circuit, and only the actual parameter values (g_m, r_o, and r_π) are dependent on the transistor used.

3.4 The Common-Base and Common-Gate Amplifiers

The second single-stage amplifier topology that we will look at is the BJT common-base (CB) amplifier in Fig. 3.18a, and its MOSFET equivalent, the common-gate (CG) amplifier in Fig. 3.18b.

DC Analysis: In order to get the quiescent DC operating point of the common-base amplifier, we write out the KVL equation at the input loop, and recognizing that $v_{BE} = -v_{IN}$ and $v_{CE} = v_{OUT} - v_{IN}$, we get

$$I_{C,Q} = I_S \cdot e^{\frac{-V_{IN}}{V_T}} \cdot \left(1 + \frac{V_{CE,Q}}{V_A}\right) = I_S \cdot e^{\frac{-V_{IN}}{V_T}} \cdot \left(1 + \frac{V_{OUT} - V_{IN}}{V_A}\right) \tag{3.75}$$

If we assume that we are given the input DC voltage, V_{IN}, and that $V_A \gg V_{OUT} - V_{IN}$, we can simplify Eq. 3.75 into

$$I_{C,Q} \approx I_S \cdot e^{\frac{-V_{IN}}{V_T}} \tag{3.76}$$

Using the KVL equation at the output loop

$$V_{CC} - I_{C,Q} R_L - V_{OUT} = 0 \tag{3.77}$$

We can get quiescent DC output voltage as

$$V_{OUT} = V_{CC} - R_L \cdot I_S \cdot e^{\frac{-V_{IN}}{V_T}} \tag{3.78}$$

Note that Eq. 3.78 describes the large signal relationship between the input voltage and the output voltage, and thus, is the transfer characteristic of the common-base amplifier. We can prevent the transistor from moving into its saturation region, by making sure that

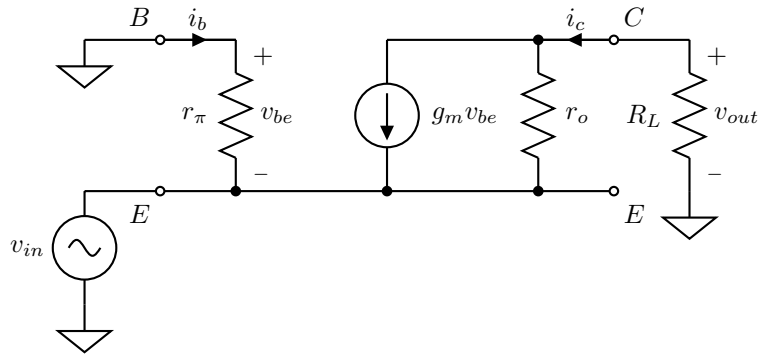


Figure 3.19: The small signal equivalent circuit of the common-base amplifier.

$$V_{CE} = V_{OUT} - V_{IN} > V_{CE,sat} \tag{3.79}$$

For the common-gate amplifier, with $v_{GS} = -v_{IN}$, and $V_{GS} = -V_{IN} > V_{TH}$, we can use the same procedure to get the quiescent DC collector current as

$$I_{D,Q} = k \cdot (-V_{IN} - V_{TH})^2 \cdot (1 + \lambda (V_{OUT} - V_{IN})) \tag{3.80}$$

and if we assume that $\lambda (V_{OUT} - V_{IN}) \ll 1$, we get

$$I_{D,Q} = k \cdot (-V_{IN} - V_{TH})^2 \tag{3.81}$$

Thus, the quiescent DC output voltage can be written as

$$V_{OUT} = V_{DD} - R_L \cdot k \cdot (-V_{IN} - V_{TH})^2 \tag{3.82}$$

Again, Eq. 3.82 is the transfer characteristic of the common-gate amplifier. To prevent the transistor from going into its linear region, we need to ensure that

$$V_{DS} = V_{OUT} - V_{IN} > -V_{IN} - V_{TH} \tag{3.83}$$

Simplifying, we get

$$V_{OUT} > -V_{TH} \tag{3.84}$$

Small Signal Behavior: As soon as we have the quiescent DC collector and drain currents, we can calculate the small signal parameters of the BJT and MOSFET. In general, Fig. 3.19 shows the small signal equivalent circuit of the common-base amplifier. Note that this is also the equivalent circuit of the common-gate amplifier. The only difference is that for the common-gate amplifier, $r_\pi \to \infty$.

To determine the effective transconductance, G_m, we short the output node of the circuit in Fig. 3.19 to ground, and calculate the output short-circuit current. Writing the KCL at the output node, and noting that $i_c = i_{out}$, $v_{be} = -v_{in}$, and $v_e = v_{in}$, we get

$$i_{out} = g_m v_{be} - \frac{v_e}{r_o} = -g_m v_{in} - \frac{v_{in}}{r_o} \tag{3.85}$$

Thus, if we assume that for the BJT,

$$|a_o| = |g_m r_o| \gg 1 \tag{3.86}$$

the effective transconductance becomes

$$G_m = \frac{i_{out}}{v_{in}} = -g_m - \frac{1}{r_o} \approx -g_m \tag{3.87}$$

This effective transconductance is slightly larger than the transconductance of the common-emitter amplifier because of the added feed-forward path from the input to the output, via r_o, leading to a larger output short-circuit current.

With the output shorted to small signal ground, we can also calculate the effective input resistance. The total current can be written as

$$i_{in} = \frac{v_{in}}{r_\pi} - i_{out} = \frac{v_{in}}{r_\pi} + g_m v_{in} + \frac{v_{in}}{r_o} \tag{3.88}$$

Table 3.2: Common-base and common-gate amplifier characteristics.

	Common-Base Amplifier	Common-Gate Amplifier
g_m	$\frac{I_{C,Q}}{V_T}$	$\sqrt{4k \cdot I_{D,Q}}$
r_o	$\frac{V_A}{I_{C,Q}}$	$\frac{1}{\lambda \cdot I_{D,Q}}$
r_π	$\frac{\beta}{g_m} = \frac{\beta \cdot V_T}{I_{C,Q}}$	∞
G_m	$-g_m = -\frac{I_{C,Q}}{V_T}$	$-g_m = -\sqrt{4k \cdot I_{D,Q}}$
R_i	$\frac{1}{g_m} = \frac{V_T}{I_{C,Q}}$	$\frac{1}{g_m} = \frac{1}{\sqrt{4k \cdot I_{D,Q}}}$
R_o	$r_o \parallel R_L = \frac{V_A}{I_{C,Q}} \parallel R_L$	$r_o \parallel R_L = \frac{1}{\lambda \cdot I_{D,Q}} \parallel R_L$
A_v	$-G_m R_o = g_m (r_o \parallel R_L) = \frac{I_{C,Q}}{V_T} \left(\frac{V_A}{I_{C,Q}} \parallel R_L \right)$	$-G_m R_o = g_m (r_o \parallel R_L) = \sqrt{4k \cdot I_{D,Q}} \left(\frac{1}{\lambda \cdot I_{D,Q}} \parallel R_L \right)$

Therefore, the small signal input resistance of the common-base amplifier is

$$R_i = \frac{v_{in}}{i_{in}} = \frac{1}{\frac{1}{r_\pi} + g_m + \frac{1}{r_o}} = r_\pi \parallel r_o \parallel \frac{1}{g_m} \tag{3.89}$$

Note that in Eq. 3.89, we treated the transistor transconductance as a resistor with value $\frac{1}{g_m}$, since the voltage that controls the dependent source is the same voltage across that dependent source. Again, using our assumption in given in Eq. 3.86, we can approximate the input resistance as

$$R_i \approx \frac{1}{g_m} \tag{3.90}$$

which is β times smaller than r_π.

The common-base output resistance can be easily found by inspection. Shorting out the input results in $v_{be} = 0$, thus zeroing out the current through the dependent source, leaving us with

$$R_o = r_o \parallel R_L \tag{3.91}$$

The common-base voltage gain is then obtained using Eqs. 3.87 and 3.91, as

$$A_v = -G_m R_o = g_m (r_o \parallel R_L) \tag{3.92}$$

It is important to note that even though the magnitude of the small signal voltage gain is the same as that of the common-emitter amplifier, the small signal voltage gain of the common-base amplifier is positive, and is thus a *non-inverting amplifier*.

The analysis is the same for a common-gate amplifier, as seen in Table 3.2. A few important things to note is that for the common-gate amplifier, even though the transistor $r_\pi \to \infty$, the input resistance of the whole amplifier is finite since the input is connected to the source and not to the gate of the MOSFET.

3.5 The Common-Collector and Common-Drain Amplifiers

The third single-stage amplifier topology is the BJT common-collector (CC) amplifier in Fig. 3.20a, and the MOSFET common-drain (CD) amplifier in Fig. 3.20b.

DC Analysis: To determine the quiescent DC operating point of the common-collector amplifier in Fig. 3.20a, we can write the KVL equation for the input loop, assuming that the transistor is in the forward-active region, as

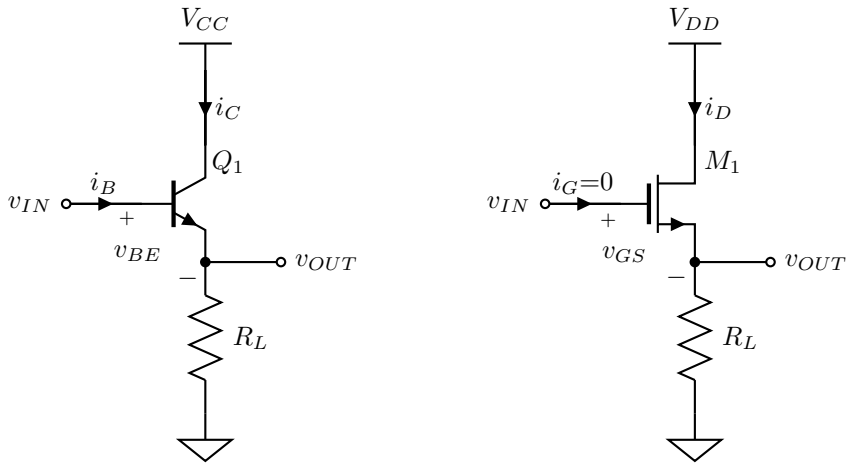
$$V_{IN} - V_{BE} - I_{E,Q} R_L = V_{IN} - V_T \ln \left(\frac{I_{C,Q}}{I_S} \right) - I_{C,Q} \left(1 + \frac{1}{\beta} \right) R_L = 0 \tag{3.93}$$

We can solve Eq. 3.93 iteratively, but for simplicity, and without losing generality, we can use the approximation that $V_{BE} = 0.7\,\text{V}$. Using this approximation, and assuming $\beta \gg 1$, the quiescent DC collector current can then be expressed as

$$I_{C,Q} = \frac{V_{IN} - 0.7\,\text{V}}{R_L \left(1 + \frac{1}{\beta} \right)} \approx \frac{V_{IN} - 0.7\,\text{V}}{R_L} \tag{3.94}$$

Note that the quiescent output DC voltage is just

$$V_{OUT} = I_{E,Q} R_L = I_{C,Q} \left(1 + \frac{1}{\beta} \right) R_L \approx I_{C,Q} R_L \tag{3.95}$$



(a) The common-collector amplifier (b) The common-drain amplifier

Figure 3.20

Combining Eqs. 3.93 and 3.95, we can express the transfer characteristic of the common-collector amplifier as

$$V_{OUT} = V_{IN} - V_{BE} = V_{IN} - 0.7\,\text{V} \tag{3.96}$$

From Eq. 3.96, we observe that the relationship between the input voltage and the output voltage is linear[a], or that the output voltage "follows" the input voltage. Thus, the common-collector amplifier is also known as an *emitter-follower* amplifier. Also, to keep the BJT is in its forward-active region, we need to ensure that

$$V_{CE} = V_{CC} - V_{OUT} > V_{CE,sat} \tag{3.97}$$

Repeating the same analysis for the common-drain amplifier in Fig. 3.20b, and with $I_{G,Q} = 0$, the KVL equation at the input loop, assuming that the MOSFET is in its saturation region and $\lambda \approx 0$, is

$$V_{IN} - V_{GS} - I_{S,Q}R_L = V_{IN} - \left(V_{TH} + \sqrt{\frac{I_{D,Q}}{k}}\right) - I_{D,Q}R_L = 0 \tag{3.98}$$

Since Eq. 3.98 is a quadratic equation, we can easily obtain the quiescent DC drain current. Also, recognizing that

$$V_{OUT} = I_{D,Q}R_L \tag{3.99}$$

the common-drain transfer characteristic can be written as

$$V_{OUT} = V_{IN} - V_{GS} = V_{IN} - \left(V_{TH} + \sqrt{\frac{I_{D,Q}}{k}}\right) \tag{3.100}$$

If there is little change in the quiescent drain current as we vary the DC input voltage, the relationship in Eq. 3.100 can be thought of as approximately linear, and that the output voltage again "follows" the input voltage. Thus, the common-drain amplifier is also known as a *source-follower* amplifier. In order to prevent the MOSFET from going into its linear region, we need to ensure that

$$V_{DS} = V_{DD} - V_{OUT} > V_{GS} - V_{TH} = V_{IN} - V_{OUT} - V_{TH} \tag{3.101}$$

or

$$V_{DD} > V_{IN} - V_{TH} \tag{3.102}$$

Small Signal Analysis: The small signal equivalent circuit of the common-collector amplifier is shown in Fig. 3.21.

To get the effective circuit transconductance, we connect the output to small signal ground, and calculate the short-circuit current. By inspection, if we connect the output to ground, then no current will flow through the resistors r_o and R_L, and recognizing that $v_{be} = v_{in}$ when $v_{out} = 0$, we get

[a]Remember that we have made a few approximations, so it is important to note that the relationship between V_{IN} and V_{OUT} is close to linear, but not exactly linear.

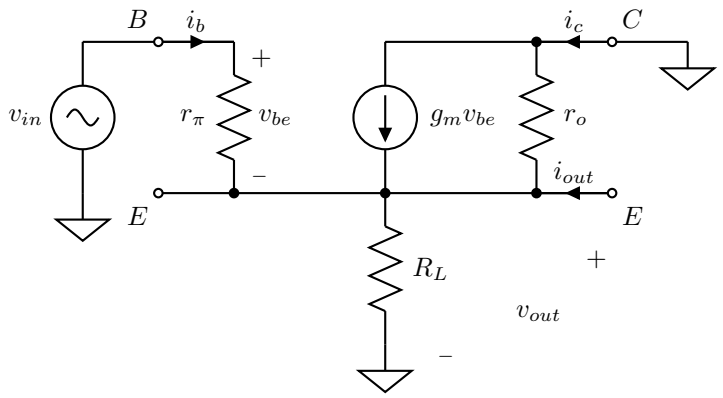


Figure 3.21: The common-collector small signal equivalent circuit.

$$i_{out} = -g_m v_{in} - \frac{v_{in}}{r_\pi} \tag{3.103}$$

The negative sign is due to the fact that the current is flowing out of the circuit, and into the short, opposite that of our convention for output current. Thus, from Eq. 3.103, and if we assume that

$$\beta = g_m r_\pi \gg 1 \tag{3.104}$$

the circuit transconductance is then

$$G_m = \frac{i_{out}}{v_{in}} = -g_m - \frac{1}{r_\pi} \approx -g_m \tag{3.105}$$

Again, by inspection, the input resistance when the output is shorted to ground, is equal to

$$R_i = r_\pi \tag{3.106}$$

To find the output resistance, the input is set to zero, and recognizing that $v_{be} = -v_{out}$, and that all the resistors are now in parallel, the output current when a test voltage source is placed at the output is

$$i_{out} = \frac{v_{out}}{R_L} + \frac{v_{out}}{r_o} + \frac{v_{out}}{r_\pi} + g_m v_{out} \tag{3.107}$$

Therefore, the output resistance is

$$R_o = \frac{v_{out}}{i_{out}} = \frac{1}{\frac{1}{R_L} + \frac{1}{r_o} + \frac{1}{r_\pi} + g_m} = R_L \parallel r_o \parallel r_\pi \parallel \frac{1}{g_m} \tag{3.108}$$

Using our assumptions in Eqs. 3.86 and 3.104, we can simplify Eq. 3.108 as

$$R_o \approx \frac{1}{g_m} \parallel R_L = \frac{R_L}{1 + g_m R_L} \tag{3.109}$$

Finally, using Eqs. 3.105 and 3.109, the small signal voltage gain of the common-collector amplifier is equal to

$$A_v = -G_m R_o = \frac{g_m R_L}{1 + g_m R_L} \tag{3.110}$$

Note that if $g_m R_L \gg 1$, then $A_v \approx 1$. This is consistent with our earlier observation that for the common-collector, the output "follows" the input.

The small signal analysis for the common-drain amplifier is exactly the same, except that for the MOSFET, $r_\pi \to \infty$.

3.6 Input Resistance Revisited

Except for the common-emitter and common-source amplifier, the input resistance is dependent on the state of the output port, and can change significantly.

Let us calculate the input resistance of the common-base and common-gate amplifiers, when the output is open-circuited. Writing the KCL equation at the output node of the circuit in Fig. 3.19, we get

$$\frac{v_{out}}{R_L} + \frac{v_{out} - v_{in}}{r_o} - g_m v_{in} = 0 \tag{3.111}$$

Table 3.3: Input resistance vs. output condition.

	$v_{out} = 0$	$i_{out} = 0$
CB/CG Amplifier	$\frac{1}{g_m}$	$\frac{1}{g_m} + \frac{R_L}{g_m r_o}$
CC/CD Amplifier	r_π	$r_\pi (1 + g_m R_L)$

Table 3.4: Summary of single-stage amplifier parameters.

	CE/CS	CB/CG	CC/CD
G_m	g_m	$-g_m$	$-g_m$
R_o	$r_o \parallel R_L$	$r_o \parallel R_L$	$\frac{1}{g_m} \parallel R_L = \frac{R_L}{1+g_m R_L}$
R_i	r_π	$\frac{1}{g_m}$	r_π
A_v	$-g_m (r_o \parallel R_L)$	$g_m (r_o \parallel R_L)$	$\frac{g_m R_L}{1+g_m R_L}$

Thus, we have

$$v_{out} = v_{in} \frac{g_m + \frac{1}{r_o}}{\frac{1}{R_L} + \frac{1}{r_o}} \approx g_m (R_L \parallel r_o) \cdot v_{in} \tag{3.112}$$

Calculating the input current,

$$i_{in} = \frac{v_{in}}{r_\pi} + \frac{v_{out}}{R_L} = \frac{v_{in}}{r_\pi} + \frac{1}{R_L} \cdot g_m \cdot \frac{R_L r_o}{R_L + r_o} v_{in} \tag{3.113}$$

Therefore, the input resistance is

$$R_i = \frac{v_{in}}{i_{in}} = \frac{1}{\frac{1}{r_\pi} + \frac{g_m r_o}{R_L + r_o}} = r_\pi \parallel \left(\frac{1}{g_m} + \frac{R_L}{g_m r_o} \right) \approx \frac{1}{g_m} + \frac{R_L}{g_m r_o} \tag{3.114}$$

As expected, Eq. 3.114 will be equal to Eq. 3.90 when $R_L = 0$. Note that the load resistance affects the input resistance of the common-base and common-gate amplifier.

This output dependent input resistance is also observed in the common-collector and common-drain amplifiers. It turns out that we have already calculated the input resistance of the circuit in Fig. 3.21 when the emitter node is open-circuited, when we calculated the input resistance of the emitter-degenerated transistor. Thus, the input resistance is

$$R_i \approx r_\pi + R_L + g_m r_\pi R_L \approx r_\pi + g_m r_\pi R_L = r_\pi (1 + g_m R_L) \tag{3.115}$$

The differences in input resistances are summarized in Table 3.3. Since the CB/CG and CC/CD amplifiers are inherently bilateral, as seen from the small signal equivalent circuits in Figs. 3.19 and 3.21, our unilateral two-port model using just three parameters (A_v, R_i and R_o) will not be enough to describe the behavior of these amplifiers for all possible output conditions.

However, for the CB/CG case, unless R_L is very large, the approximation $R_i \approx \frac{1}{g_m}$ is a good one. Note that even if $R_L = r_o$, the input resistance increases by just a factor of 2. On the other hand the input resistance of the CC/CD amplifier can change drastically, so it is important that we understand the implications of our unilateral amplifier models.

3.7 Single-Stage Amplifier Comparisons

We have looked at the small signal characteristics of the three single-stage transistor amplifier topologies, and the effective two-port parameters are summarized in Table 3.4.

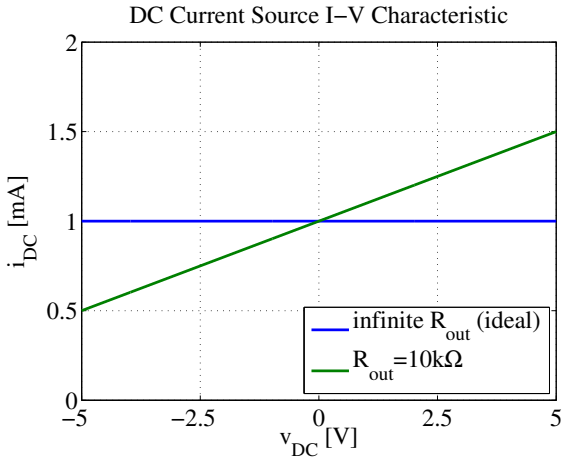
The CE/CS amplifier and the CB/CG amplifier both have relatively large voltage gains, but one is inverting, the other is non-inverting. In larger, more complex amplifiers and applications, a designer might prefer one over the other, as we will see in the succeeding topics. It is interesting to note that the output impedances of the CE/CS and CB/CG amplifiers are rather large, and can only drive resistive loads larger than their output resistance to amplify voltage signals without much loading effects.

The CC/CD amplifier, on the other hand, has a voltage gain very close to unity. However, the output resistance of these amplifiers can be made quite low, depending on the value of g_m. This is very useful in driving small resistive loads, such as audio speakers, whose impedances are typically around $8\,\Omega$.

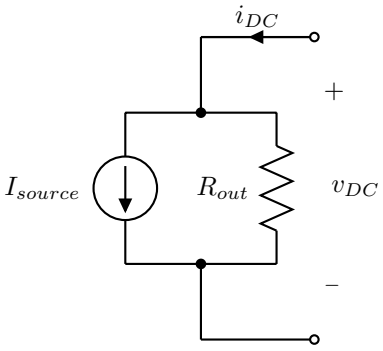
The input resistance of the CE/CS and CC/CD amplifiers, are relatively large, and in the case of MOSFET amplifiers, $R_i \to \infty$. This is desirable if the driving circuit is a voltage source with a small source resistance, since the gain degradation due to loading effects are reduced. However, if the input is a current source with a high output

impedance, it is desirable to use an amplifier with a small input resistance such as the CB/CG amplifier, again reducing the effects of loading.

As we have seen, the different single-stage amplifier topologies can provide us with a varied set of effective two-port small signal parameters. In the remainder of EEE 51, we will use these amplifiers as building blocks towards creating more useful and practical, but more complex amplifiers.



(a) I-V characteristic



(b) Circuit model

Figure 4.1: Current source characteristics.

4 Current Sources

The largest gain we can get out of a transistor is its intrinsic gain, $|a_o| = |g_m r_o|$. As we have seen previously, this intrinsic gain can be achieved if the transistor is biased by an ideal current source. In this section, we will look at how we build current sources, their characteristics, and how current source-biased amplifiers compare with their resistor-biased counterparts.

4.1 Non-Ideal Current Sources

An ideal current source maintains a constant current through its terminals, independent of the voltage applied across these terminals. However, in a real current source, the current through its terminals can vary due to an applied voltage, as seen from the I-V characteristic in Fig. 4.1a. We can model this non-ideality as the output resistance of a current source, as shown in Fig. 4.1b, where the slope of the I-V characteristic is equal to $\frac{1}{R_{out}}$.

The total current, i_{DC}, can then be expressed as

$$i_{DC} = I_{source} + \frac{v_{DC}}{R_{out}} \tag{4.1}$$

Thus, as the output resistance, R_{out}, is increased, the closer the current source is to an ideal current source.

4.1.1 Biasing Transistor Amplifiers

Let us examine the implications of using a current source, instead of a resistor, to bias the common-emitter amplifier. Recall that the small signal gain of the common-source amplifier is

$$A_v = -g_m \left(r_o \parallel R_L\right) \tag{4.2}$$

where R_L is the load resistor we use to deliver $I_{C,Q}$ from the supply voltage, V_{CC}, to the transistor. To keep the transistor in the forward active region,

$$V_{OUT} = V_{CC} - I_{C,Q} R_L > V_{CE,sat} \tag{4.3}$$

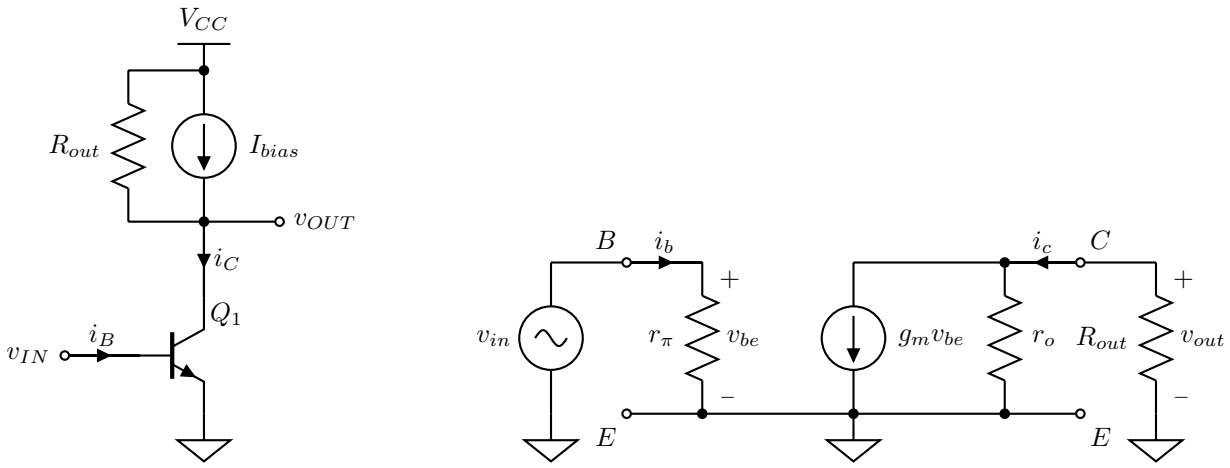
If we want a gain close to the intrinsic transistor gain, a_o, we want to make R_L as large as possible, as seen in Eq. 4.2. However, if we want to keep $I_{C,Q}$ constant[a], then from Eq. 4.3, increasing R_L will result in a smaller output voltage that can potentially drive the transistor into saturation. One way to resolve this problem is to increase the supply voltage, V_{CC}. In some cases, such as for high-power applications, the supply voltage can be increased to around 48 V or higher.

In most applications, however, we are limited to using supply voltages of around 1 V to 12 V. An alternative way to provide the quiescent DC collector current is to use a current source, as seen in Fig. 4.2a.

From the small signal equivalent circuit in Fig. 4.2b, we can see that the gain is now

$$A_v = -g_m \left(r_o \parallel R_{out}\right) \tag{4.4}$$

[a]Most amplifiers need a certain transconductance value in order to achieve a certain specification. Since the quiescent DC collector (or drain) current determines the transconductance, g_m, a specific value of $I_{C,Q}$ (or $I_{D,Q}$) is often required.



(a) Schematic (b) Small signal equivalent circuit

Figure 4.2: A common-emitter amplifier biased using a current source.

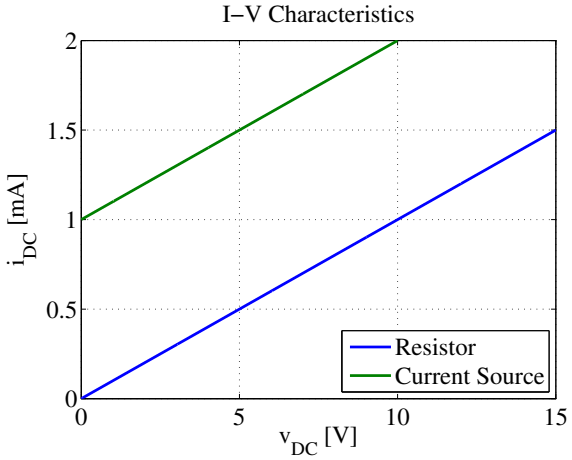


Figure 4.3: The I-V characteristics of a 10 kΩ resistor and a 1 mA current source with $R_{out} = 10\,\text{k}\Omega$.

where R_{out} is the output resistance of the current source. Again, to get the a small signal voltage gain close to a_o, we want R_{out} to be as large as possible. The quiescent DC collector current can then be expressed as

$$I_{C,Q} = I_{bias} + \frac{V_{CC} - V_{OUT}}{R_{out}} \tag{4.5}$$

Thus, as $R_{out} \to \infty$, $I_{C,Q} \to I_{bias}$. The output voltage is then equal to

$$V_{OUT} = V_{CC} - R_{out}\left(I_{C,Q} - I_{bias}\right) \tag{4.6}$$

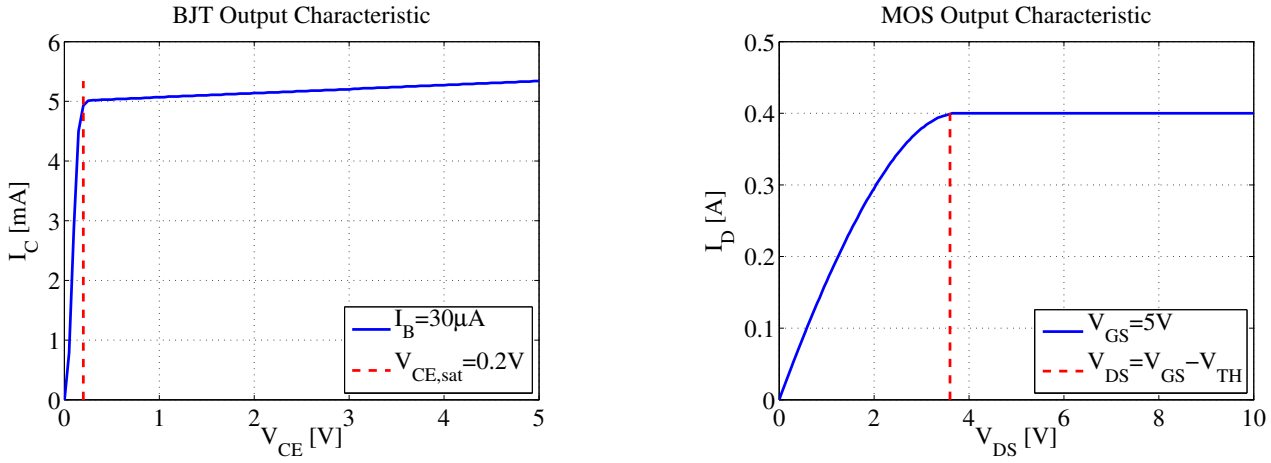
Looking Eq. 4.6, we can see that by making R_{out} large, $(I_{C,Q} - I_{bias})$ becomes smaller, removing the need for higher supply voltages. If we can manage to create a current source with $R_{out} \to \infty$, we can make $A_v \to a_o$.

Another way of looking at this is by looking at the I-V charcteristics of both the resistor and the current source, as seen in Fig. 4.3. In order to obtain a current of 1.5 mA, the current source just needs a voltage of 5 V, while the resistor needs 15 V. This is due to the fact that being linear, the resistor has to pass through the point when both the current and voltage is zero. The current source, on the other hand, is non-linear, and thus, does not have to pass through the same zero voltage and current point.

Thus, using current sources for biasing transistor amplifiers allow us to remove the relationship between the DC output voltage and the small signal voltage gain, unlike the resistor-biased amplifier, which uses R_L to control both V_{OUT} and A_v.

4.1.2 Transistor Current Sources

How do we build current sources? Let us examine the output characteristic of a typical BJT, as shown in Fig. 4.4a. In the forward-active region, the BJT output characteristic looks very much like a current source with an output resistance. Recall that the slope of the BJT output characteristic is equal to $\frac{1}{r_o}$, thus, if we think of the transistor as



(a) BJT (b) MOSFET

Figure 4.4: Transistor output characterisics.

a current source, we will have

$$I_{source} = I_C = I_S \cdot e^{\frac{V_{BE}}{V_T}} \cdot \left(1 + \frac{V_{CE}}{V_A}\right) = \beta \cdot I_B \tag{4.7}$$

and its output resistance can be expressed as

$$R_{out} = \left(\frac{\partial I_C}{\partial V_{CE}}\right)^{-1} = r_o = \frac{V_A}{I_C} \tag{4.8}$$

Note that this output resistance remains relatively large as long as the transistor is in its forward-active region. We can see from Fig. 4.4a that as soon as the transistor enters the saturation region, the slope increases, thus decreasing the output resistance. Thus, in current sources built using transistors, we can define a minimum voltage, $V_{\min}$, such that below this minimum voltage, the output resistance drops significantly. For the case of a BJT used as a current source,

$$V_{\min} = V_{CE,sat} \tag{4.9}$$

Similar to the BJT, in the saturation region, the output characteristic of a MOSFET, shown in Fig. 4.4b, looks very similar to the I-V curve of a current source. Thus, if we use a MOSFET as a current source, we get

$$I_{source} = I_D = k \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS}) \tag{4.10}$$

$$R_{out} = \left(\frac{\partial I_D}{\partial V_{GS}}\right)^{-1} = r_o = \frac{1}{\lambda \cdot I_D} \tag{4.11}$$

$$V_{\min} = V_{DSAT} = V_{GS} - V_{TH} \tag{4.12}$$

We can therefore create a simple current source out of a transistor by providing the appropriate input DC signal, that is, V_{BE} (or I_B), for a BJT, or V_{GS} for a MOSFET. Fig. 4.5 shows a simple resistive voltage divider bias that can be used to realize a BJT current source. Is this a good idea?

Let us take a closer look at the current source in Fig. 4.5. In order to get a collector current of 1 mA, and assuming $I_S = 2 \times 10^{-16}$ A, and that the output voltage is negligible compared to V_A[b] and larger than $V_{CE,sat}$, we need a base-emitter voltage of

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) = 26\,\text{mV} \cdot \ln\left(\frac{1\,\text{mA}}{2 \times 10^{-16}\,\text{A}}\right) = 0.7603\,\text{V} \tag{4.13}$$

If we increase the base-to-emitter voltage by just 10 mV (or 1.32%), and use $V_{BE} = 0.7703$ V, we would get a collector current of 1.5 mA, which is a 50% increase! Thus, we have to be able to set V_{BE} to a certain precision, which is usually hard to do.

[b] In the context of current sources, base-width modulation and channel length modulation play a big role. However, including V_A or λ in every equation results in very long and cumbersome expressions that could prevent us from obtaining an intuitive grasp of the ideas. Thus, in most cases, we will assume that $V_A \to \infty$ or $\lambda = 0$, and just point out situations when these parameters become significant.

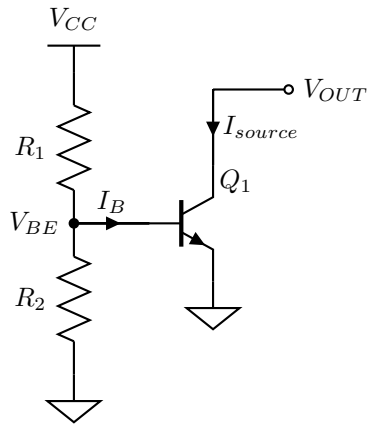


Figure 4.5: Resistive voltage divider BJT current source.

If we want a maximum current error of ±1% (or ±10 μA), the we would require that V_{BE} be within 0.7603 V ± 260 μV. This is due to the exponential relationship between V_{BE} and I_C. We can express the V_{BE} as

$$V_{BE} = I_2 R_2 = (I_1 - I_B) \cdot R_2 = \left(\frac{V_{CC} - V_{BE}}{R_1} - \frac{I_S}{\beta} \cdot e^{\frac{V_{BE}}{V_T}} \right) \cdot R_2 \tag{4.14}$$

For example, if $\beta = 200$ and $V_{CC} = 5\,\text{V}$, and if we select $R_1 = 10\,\text{k}\Omega$, then

$$R_2 = \frac{V_{BE}}{\frac{V_{CC} - V_{BE}}{R_1} - \frac{I_C}{\beta}} = 1.8146\,\text{k}\Omega \tag{4.15}$$

Solving for β, we get

$$\beta = \frac{I_S \cdot e^{\frac{V_{BE}}{V_T}}}{\frac{V_{CC}}{R_1} - V_{BE}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)} \tag{4.16}$$

Thus, if we want a maximum $\Delta V_{BE} = 260\,\mu\text{V}$, from Eq. 4.16 we can calculate the maximum and minimum β we can tolerate as

$$\beta_{\max} = \frac{I_S \cdot e^{\frac{V_{BE} + \Delta V_{BE}}{V_T}}}{\frac{V_{CC}}{R_1} - (V_{BE} + \Delta V_{BE})\left(\frac{1}{R_1} + \frac{1}{R_2}\right)} = 209 \tag{4.17}$$

$$\beta_{\min} = \frac{I_S \cdot e^{\frac{V_{BE} - \Delta V_{BE}}{V_T}}}{\frac{V_{CC}}{R_1} - (V_{BE} - \Delta V_{BE})\left(\frac{1}{R_1} + \frac{1}{R_2}\right)} = 191 \tag{4.18}$$

Note that this means the required tolerance for the transistor β is $\frac{\beta_{\max} - \beta}{\beta} = 4.52\%$. As we have mentioned before, this is very hard to obtain since typical β-variations could reach up to 50%.

For MOSFETs, the main problem turns out to be the variations in the value of the threshold voltage, V_{TH}. In typical MOSFETs, the threshold voltage could also vary by as much as 50% as well. Thus, with even perfect resistors, it is very hard to control the drain current due to the quadratic relationship between V_{TH} and I_D, as seen in Eq. 4.10.

Thus, to get a usable current source using a resistive divider, we need to (1) tightly control the the values of the supply voltage, the resistors, and the transistor β or V_{TH}, as well as (2) be able specify the values of these components to a very high degree of precision. In most cases, using very high quality components would be very costly, and most of the time, components with these specifications do not exist commercially.

4.2 The BJT Current Mirror

An alternative biasing strategy is to use another transistor to generate the required V_{BE}, instead of resistors. Consider the circuit in Fig. 4.6. Notice that since $V_{CB} = 0$, the transistor will never go into the saturation region as long as the base-emitter junction is forward-biased, since $V_{BE} = V_{CE} > V_{CE,sat}$. If we apply an input current I_o, the collector current would be

$$I_C = I_o - I_B = I_o - \frac{I_C}{\beta} \tag{4.19}$$

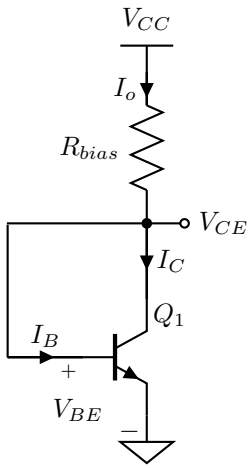


Figure 4.6: A diode-connected BJT.

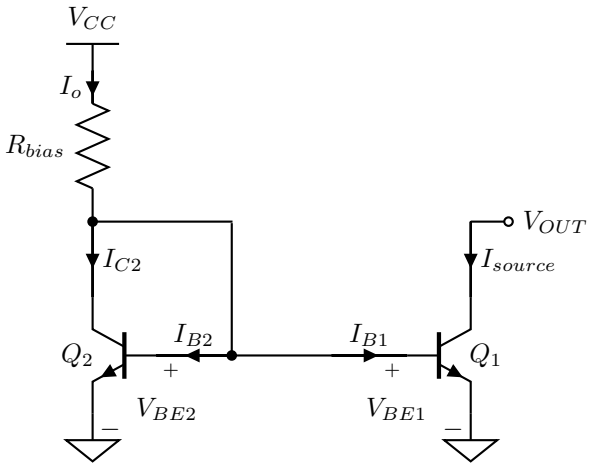


Figure 4.7: A resistor-biased BJT current mirror.

Thus, assuming $V_A \to \infty$, the base-emitter voltage can be written as

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) = V_T \ln\left(\frac{I_o}{I_S} \cdot \frac{\beta}{\beta+1}\right) \tag{4.20}$$

Since the transistor is now effectively a two-terminal device, and follows the I-V relationship similar to a diode, as given in Eq. 4.20, the transistor in Fig. 4.6 is often referred to as a *diode-connected* transistor.

Writing the KVL equation at the for the base-emitter loop, we get

$$V_{CC} - I_o R_{bias} - V_{BE} = 0 \tag{4.21}$$

Combining Eqs. 4.21 and 4.20, we get an expression for the R_{bias} needed to generate a specific V_{BE}, as given by

$$R_{bias} = \frac{V_{CC} - V_{BE}}{\left(1+\frac{1}{\beta}\right) \cdot I_S \cdot e^{\frac{V_{BE}}{V_T}} \cdot \left(1+\frac{V_{BE}}{V_A}\right)} \tag{4.22}$$

We can then use this diode connected transistor and resistor combination to generate the required V_{BE} of a transistor used as a current source, as seen in Fig. 4.7. Since $V_{BE1} = V_{BE2} = V_{BE}$, and assuming that Q_1 and Q_2 are identical transistors, giving us $\beta_1 = \beta_2 = \beta$ and $I_{S1} = I_{S2} = I_S$, we get

$$V_T \ln\left(\frac{I_{C1}}{I_{S1} \cdot \left(1+\frac{V_{CE1}}{V_A}\right)}\right) = V_T \ln\left(\frac{I_{C2}}{I_{S2} \cdot \left(1+\frac{V_{CE2}}{V_A}\right)}\right) \tag{4.23}$$

which tells us that

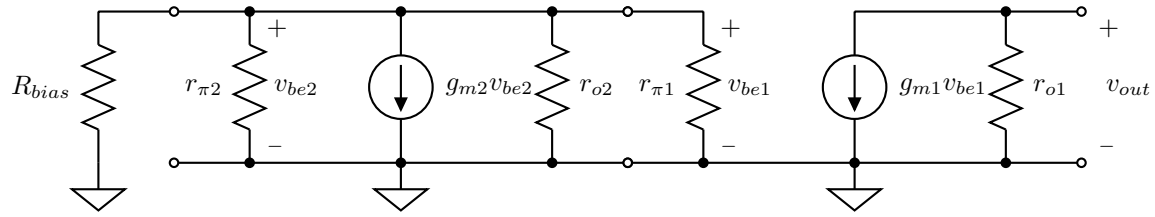


Figure 4.8: The BJT current mirror small signal equivalent circuit.

$$I_{source} = I_{C1} = I_{C2} \cdot \frac{\left(1 + \frac{V_{CE1}}{V_A}\right)}{\left(1 + \frac{V_{CE2}}{V_A}\right)} = I_{C2} \cdot \frac{V_A + V_{CE1}}{V_A + V_{CE2}} \tag{4.24}$$

We can express I_{C2} as

$$I_{C2} = I_o - I_{B1} - I_{B2} = I_o - \frac{I_{source}}{\beta} - \frac{I_{C2}}{\beta} \tag{4.25}$$

and solving for I_{C2} in terms of I_o, we get

$$I_{C2} = I_o \frac{\beta}{\beta + 1} - I_{source} \cdot \frac{1}{\beta + 1} \tag{4.26}$$

Thus, the output current of the BJT current source is

$$I_{source} = I_o \frac{\frac{\beta}{\beta+1} \cdot \frac{V_A+V_{CE1}}{V_A+V_{CE2}}}{1 + \frac{1}{\beta+1} \cdot \frac{V_A+V_{CE1}}{V_A+V_{CE2}}} = I_o \frac{\frac{\beta}{\beta+1} \cdot \frac{V_A+V_{OUT}}{V_A+V_{BE}}}{1 + \frac{1}{\beta+1} \cdot \frac{V_A+V_{OUT}}{V_A+V_{BE}}} \tag{4.27}$$

For $V_A \to \infty$, we get

$$I_{source} = I_o \frac{1}{1 + \frac{2}{\beta}} \tag{4.28}$$

and if $\beta \gg 1$ and if $V_A \to \infty$, then $I_{source} \approx I_o$. Since the output current, I_{source} is a replica of the input current, I_o, the transistor pair in Fig. 4.7 is called a *current mirror*.

There exists a mirroring error due to the fact that I_o also has to supply the base currents of the two transistors, and that any mismatch between the collector-emitter voltages of the two transistors would cause a current difference due to base-width modulation.

Assuming $V_A \to \infty$, and again, solving for β, we get

$$\beta = \frac{2}{\frac{I_o}{I_{source}} - 1} \tag{4.29}$$

Thus, to get a maximum output current variation of $\Delta I_{source} = 10\,\mu\text{A}$ for $I_{source} = 1\,\text{mA}$, resulting in an $I_o = 1.01\,\text{mA}$, we can then calculate $\beta_{\min}$ as

$$\beta_{\min} = \frac{2}{\frac{I_o}{I_{source} - \Delta I_{source}} - 1} = 99 \tag{4.30}$$

This makes the BJT current mirror very robust to β-variations since we can now tolerate a 50.5% reduction in β. Note that the higher β is, the lower the error, and as $\beta \to \infty$, $I_{source} \to I_o$, which is within our $\pm 1\%$ limit.

Using Eq. 4.27 with Eq. 4.21, and assuming that $V_A \to \infty$, the required R_{bias} needed to generate I_{source} is then

$$R_{bias} = \frac{V_{CC} - V_{BE}}{\left(1 + \frac{2}{\beta}\right) \cdot I_S \cdot e^{\frac{V_{BE}}{V_T}}} = \frac{V_{CC} - V_T \ln\left(\frac{I_{source}}{I_S}\right)}{I_{source}\left(1 + \frac{2}{\beta}\right)} \tag{4.31}$$

For the current mirror, we are using R_{bias} to generate I_o linearly, and since the conversion from I_o to V_{BE} and back again to I_{source} is effectively linear, as seen in Eq. 4.27, the required degree variation control of the resistor values is linear with the output current tolerance requirements, instead of exponential, as shown for the resistive voltage divider bias current source. This allows us to use lower quality resistors and still obtain the same output current variation.

To get the small signal output resistance of the current mirror, we set all small signal inputs to zero. Since there are no small signal inputs, we can directly obtain the small signal equivalent circuit in Fig. 4.8.

By inspection, we can see that $v_{be1} = v_{be2} = 0$, thus, the output resistance of the current mirror is

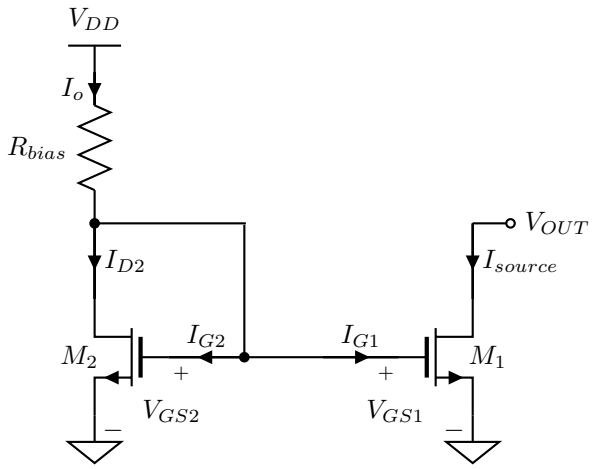


Figure 4.9: The MOSFET Current Mirror.

$$R_{out} = r_{o1} \tag{4.32}$$

The minimum output voltage of the current mirror is still

$$V_{\min} = V_{CE,sat} \tag{4.33}$$

4.3 The MOSFET Current Mirror

A MOSFET current mirror is shown in Fig. 4.9. Assuming that M_1 and M_2 are identical, and since the gate-source voltages are the same, we get

$$V_{GS1} = V_{TH} + \sqrt{\frac{I_{D1}}{k \cdot (1 + \lambda V_{DS1})}} = V_{GS2} = V_{TH} + \sqrt{\frac{I_{D2}}{k \cdot (1 + \lambda V_{DS2})}} \tag{4.34}$$

We can then compute for the output current as

$$I_{source} = I_{D1} = I_{D2} \cdot \frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}} = I_o \cdot \frac{1 + \lambda V_{OUT}}{1 + \lambda V_{GS}} \tag{4.35}$$

Note that since the gate currents are zero, the only source of error between I_o and I_{source} is the mismatch between the drain-source voltages of the two transistors due to channel length modulation. Thus, if $\lambda \to 0$, then $I_{source} \approx I_o$.

Calculating the bias resistor needed to generate I_{source}, and assuming $\lambda = 0$, we get

$$R_{bias} = \frac{V_{DD} - V_{GS}}{I_o} = \frac{V_{DD} - V_{TH} - \sqrt{\frac{I_{source}}{k}}}{I_{source}} \tag{4.36}$$

Similar to the BJT current mirror, the output resistance is still r_{o1}, and $V_{\min} = V_{GS} - V_{TH}$.

4.4 Current Mirror Loads

Now that we have a way to build current sources using current mirrors, let us use these current sources to bias our amplifiers. Consider the common-emitter amplifier biased using current mirrors shown in Fig. 4.10. In this instance, we are using PNP transistors for our current mirror and an NPN transistor for the gain stage.

Using a current source greatly simplifies the DC analysis since if we assume that I_{bias} represents some other circuit that provides an input current to the current mirror, and that $V_A \to \infty$ and $\beta \to \infty$, we then get $I_{C1,Q} = I_{bias}$. However, since in the forward-active region, Q_1 and Q_2 behave like high-impedance current sources, in order to obtain the quiescent DC output voltage, we cannot assume that the Early voltage is infinite. Thus, to compute V_{OUT}, and recognizing the fact the the collector currents of Q_1 and Q_2 are the same, we get

$$I_{C1,Q} = I_{S1} \cdot e^{\frac{V_{IN}}{V_T}} \cdot \left(1 + \frac{V_{OUT}}{V_{A1}}\right) = I_{C2,Q} = I_{S2} \cdot e^{\frac{|V_{BE2}|}{V_T}} \cdot \left(1 + \frac{|V_{CC} - V_{OUT}|}{V_{A2}}\right) \tag{4.37}$$

Ignoring the mirroring errors from Q_3 to Q_2, we can express V_{EB2} as

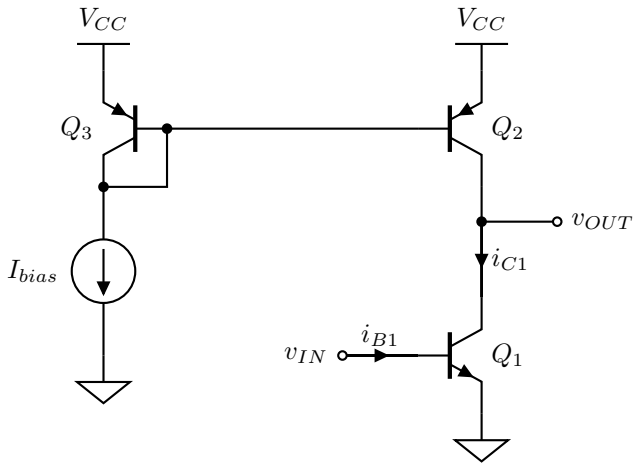


Figure 4.10: A common-emitter amplifier biased using a current mirror.

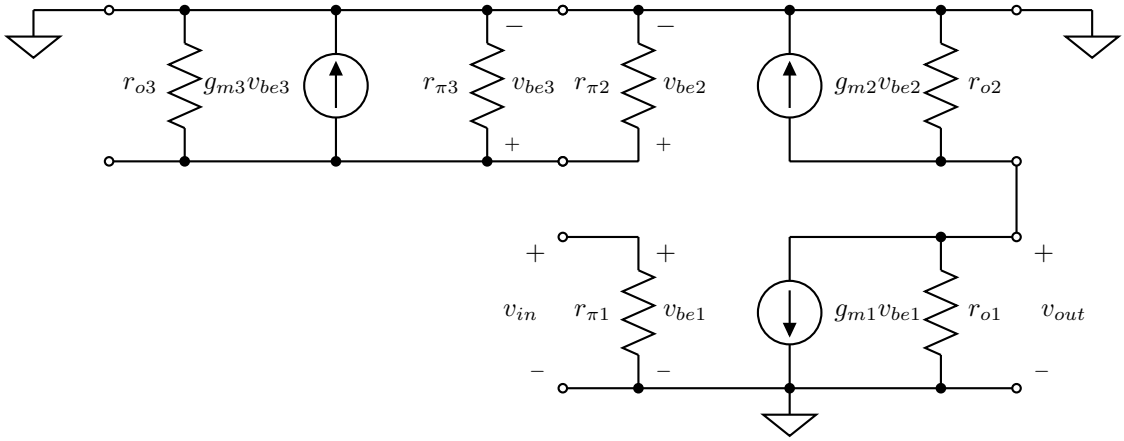


Figure 4.11: The small signal equivalent circuit of the amplifier in Fig. 4.10.

$$V_{BE2} \approx \left| V_T \ln\left(\frac{I_{bias}}{I_{S2}}\right)\right| \tag{4.38}$$

Once we know the quiescent collector currents, we can now determine the small signal parameters of each transistor. The small signal equivalent circuit of the amplifier is shown in Fig. 4.11.

Recognizing that Q_3 is a diode-connected transistor driven by an ideal current source, the resulting $V_{BE3} = V_{BE2}$ is a constant. Thus, there can be no small signal change in V_{BE3} and V_{BE2}. We can then conclude that $v_{be3} = v_{be2} = 0$. By inspection, we can see that

$$G_m = g_m \tag{4.39}$$

$$R_o = r_{o1} \parallel r_{o2} \tag{4.40}$$

$$R_i = r_{\pi1} \tag{4.41}$$

$$A_v = -g_m \cdot (r_{o1} \parallel r_{o2}) \tag{4.42}$$

Note that if $V_{A1} = V_{A2}$, then $r_{o1} = r_{o2} = r_o$, then $A_v = -\frac{g_m r_o}{2}$, which is half the intrinsic transistor gain.

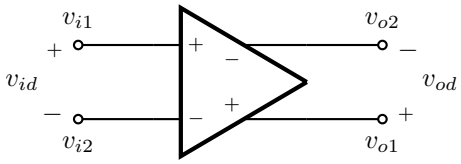


Figure 5.1: A fully-differential voltage amplifier.

5 Differential Circuits

The circuits we have covered so far have input and output small signal voltages that are referenced to (or referred to) the small signal ground. These circuits are called *single-ended circuits*. In certain cases, we want to amplify the difference between two signals. Circuits that operate on the difference between two signals are called *differential circuits*. In this section, we will look at the reasons why one would choose differential circuits over single-ended circuits, and the costs associated with using these differential circuits.

5.1 Differential Signals and Gain Definitions

Consider two voltages referred to ground, v_1 and v_2. If these two voltages are independent, then any change in v_1 will not affect v_2. We can say that v_1 and v_2 are orthogonal to each other. Thus, in order to completely describe this system of two independent voltages, we need specify both v_1 and v_2.

Just like changing coordinate axes, we can use a different set of orthogonal quantities to describe these two voltages. One such set of quantities is the the differential voltage, v_d, and the common-mode voltage, v_c, defined as

$$v_d = v_1 - v_2 \tag{5.1}$$

$$v_c = \frac{v_1 + v_2}{2} \tag{5.2}$$

Note that v_d and v_c are also orthogonal with respect to each other, since we can change the difference between v_1 and v_2[a], while maintaining their average, and vice-versa. From Eqs. 5.1 and 5.2, we can also get the inverse relationships

$$v_1 = v_c + \frac{v_d}{2} \tag{5.3}$$

$$v_2 = v_c - \frac{v_d}{2} \tag{5.4}$$

Consider a fully-differential voltage amplifier, given in Fig. 5.1. A fully-differential amplifier amplifies the differential input voltage, and produces a differential output voltage. However, since we have four quantities, we can define four distinct voltage gains.

The voltage gain between the differential input voltage to the differential output voltage is called the differential-mode gain, and is defined as

$$A_{dm} = \left.\frac{v_{od}}{v_{id}}\right|_{v_{ic}=0} = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} \tag{5.5}$$

We can also define the common-mode gain as

$$A_{cm} = \left.\frac{v_{oc}}{v_{ic}}\right|_{v_{id}=0} = \frac{\frac{1}{2}\left(v_{o1} + v_{o2}\right)}{\frac{1}{2}\left(v_{i1} + v_{i2}\right)} \tag{5.6}$$

It is also possible for an amplifier to convert the input differential voltage into a common-mode output voltage. Thus, the differential-mode to common-mode gain is

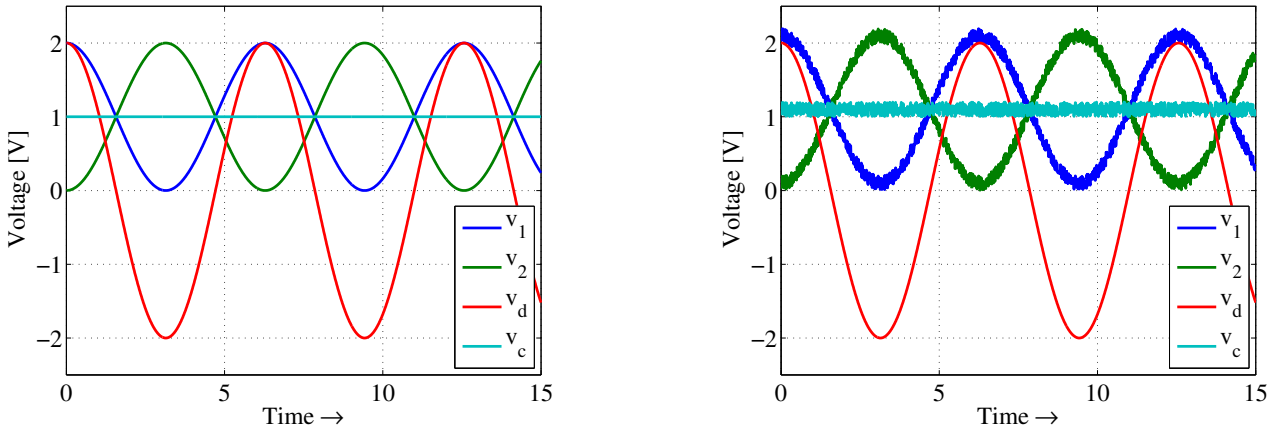
$$A_{dm-cm} = \left.\frac{v_{oc}}{v_{id}}\right|_{v_{ic}=0} \tag{5.7}$$

and the gain from the common-mode input voltage to the differential-mode output voltage is defined as

$$A_{cm-dm} = \left.\frac{v_{od}}{v_{ic}}\right|_{v_{id}=0} \tag{5.8}$$

Thus, the total differential output voltage can be expressed as

[a] In some texts, v_1 and v_2 are also referred to as v^+ and v^-, such that $v_d = v^+ - v^-$ and $v_c = \frac{1}{2}\left(v^+ + v^-\right)$.



(a) Ideal

(b) In the presence of common-mode noise

Figure 5.2: Differential vs. single-ended signals.

$$v_{od} = A_{dm} \cdot v_{id} + A_{cm-dm} \cdot v_{ic} \tag{5.9}$$

and the total common-mode output voltage is

$$v_{oc} = A_{cm} \cdot v_{ic} + A_{dm-cm} \cdot v_{id} \tag{5.10}$$

Why would we want to use differential signals (voltage or current) instead of single-ended signals? Consider the case when $v_1 = A \cdot \cos(\omega t) + B$ and $v_2 = A \cdot \cos(\omega t + 180°) + B$. We can express the differential voltage v_d as

$$v_d = v_1 - v_2 = A \cdot \cos(\omega t) + B - (-A \cdot \cos(\omega t) + B) = 2A \cdot \cos(\omega t) \tag{5.11}$$

and the common-mode voltage is

$$v_c = \frac{v_1 + v_2}{2} = \frac{A \cdot \cos(\omega t) + B + (-A \cdot \cos(\omega t) + B)}{2} = B \tag{5.12}$$

Fig. 5.2a shows the plot of v_1, v_2, v_d, and v_c for $A = 1\,\text{V}$, and $B = 1\,\text{V}$.

Now consider the case when some random noise voltage gets coupled into the two voltages, v_1 and v_2, such that

$$v_1' = v_1 + v_{noise} \tag{5.13}$$

$$v_2' = v_2 + v_{noise} \tag{5.14}$$

We can still calculate the differential and common-mode voltages as

$$v_d' = v_1' - v_2' = v_1 + v_{noise} - v_2 - v_{noise} = v_1 - v_2 = 2A\cos(\omega t) \tag{5.15}$$

$$v_c' = \frac{v_1' + v_2'}{2} = \frac{v_1 + v_{noise} + v_2 + v_{noise}}{2} = B + v_{noise} \tag{5.16}$$

Notice that as long as any noise or interference appears on both v_1 and v_2, it is not seen in the differential voltage, v_d'! All signals that are "common" to both v_1 and v_2 will appear as part of the common-mode signal, v_c', as seen in Fig. 5.2b. Thus, a differential amplifier that only amplifies the differential signal, and rejects the common-mode will be immune to this common-mode noise or interference. One metric of how well an amplifier amplifies the differential signal and at the same time rejects the common-mode signal is the *common-mode rejection ratio*, defined as

$$\text{CMRR} = \left| \frac{A_{dm}}{A_{cm}} \right| \tag{5.17}$$

Another advantage of using differential amplifiers is the inherent generation of both the inverting and non-inverting output. If an inverting amplifier is needed, one can simply re-label the output terminals of the amplifier in Fig. 5.1, such that v_{o1} becomes v_{o2} and vice versa.

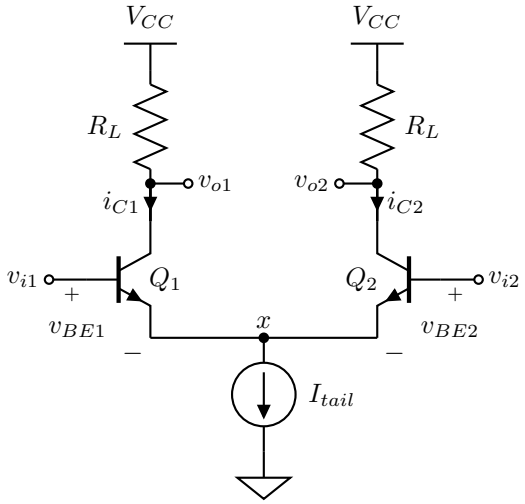


Figure 5.3: The BJT differential pair.

5.2 The BJT Differential Pair

How do we build differential circuits? One very important differential circuit building block is the BJT differential pair (or the emitter-coupled pair) with a resistor load, shown in Fig. 5.3. In order to understand how the BJT differential pair works, let us first look at its large-signal characteristics.

If we write the KVL equation around the input loop that includes the base terminals of both transistors, we get

$$V_{i1} - V_{BE1} + V_{BE2} - V_{i2} = 0 \tag{5.18}$$

Assuming that Q_1 and Q_2 are identical,

$$V_{i1} - V_{i2} = V_{id} = V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_S}\right) - V_T \ln\left(\frac{I_{C2}}{I_S}\right) = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{5.19}$$

Rearranging Eq. 5.19, we get

$$I_{C1} = I_{C2} \cdot e^{\frac{V_{id}}{V_T}} \tag{5.20}$$

Writing the KCL equation at node x,

$$I_{tail} = I_{E1} + I_{E2} = \frac{I_{C1} + I_{C2}}{\alpha} \tag{5.21}$$

Using Eqs. 5.20 and 5.21, we can get expressions for the collector currents of both transistors in terms of the input differential voltage as

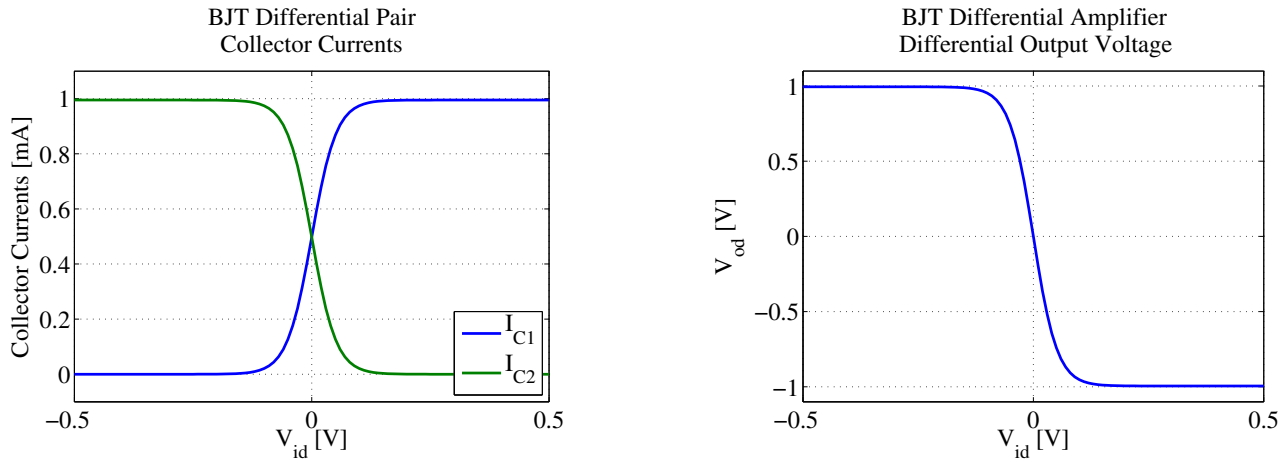
$$I_{C1} = \frac{\alpha \cdot I_{tail}}{1 + e^{-\frac{V_{id}}{V_T}}} \tag{5.22}$$

$$I_{C2} = \frac{\alpha \cdot I_{tail}}{1 + e^{+\frac{V_{id}}{V_T}}} \tag{5.23}$$

Based on Eqs. 5.22 and 5.23, the behavior of the collector currents as the input differential voltage is varied is shown in Fig. 5.4a.

When we increase the input differential voltage, V_{id}, we increase I_{C1}. But since the tail current source ensures that the sum of the two collector currents are constant, and equal to I_{tail}, any increase in I_{C1} will force I_{C2} to decrease by exactly the same amount. Also note that even if V_{i1} and V_{i2} varies, as long as they are equal, i.e. $V_{id} = 0$, both I_{C1} and I_{C2} will always be equal to $\frac{I_{tail}}{2}$.

Thus, even if the common-mode input voltage changes, for two perfectly matched transistors with an ideal tail current source, (1) the two collector currents will only be influenced by the input differential voltage, and (2) the collector currents will change in a purely differential manner, meaning that if I_{C1} increases by ΔI, or $I_{C1} = \frac{I_{tail}}{2} + \Delta I$, then $I_{C2} = \frac{I_{tail}}{2} - \Delta I$, and the common-mode current of $\frac{I_{tail}}{2}$ will not change.



(a) Collector currents

(b) Output voltage

Figure 5.4: BJT differential pair large signal characteristics for $\beta = 200$, $I_{tail} = 1\,\text{mA}$, and $R_L = 1\,\text{k}\Omega$.

5.2.1 The BJT Differential Amplifier

The collector currents are then converted to an output voltage by the two load resistors. Thus, the differential pair composed of the Q_1, Q_2 and the tail current, when loaded with R_L, can be considered a rudimentary fully differential amplifier. The output voltages are then

$$V_{o1} = V_{CC} - R_L I_{C1} \tag{5.24}$$

$$V_{o2} = V_{CC} - R_L I_{C2} \tag{5.25}$$

Solving for the differential output voltage, V_{od}, we get

$$V_{od} = V_{o1} - V_{o2} = R_L \left(I_{C2} - I_{C1}\right) \tag{5.26}$$

Combining Eqs. 5.22, 5.23, and 5.26, we get

$$V_{od} = \alpha \cdot I_{tail} \cdot R_L \left(\frac{1}{1 + e^{+\frac{V_{id}}{V_T}}} - \frac{1}{1 + e^{-\frac{V_{id}}{V_T}}} \right) = \alpha \cdot I_{tail} \cdot R_L \cdot \tanh\left(-\frac{V_{id}}{2 \cdot V_T} \right) \tag{5.27}$$

Eq. 5.27 is then the large signal differential transfer characteristic of the BJT differential amplifier since it relates the differential output voltage, V_{od}, and the differential input voltage, V_{id}, and is plotted in Fig. 5.4b.

The maximum output differential voltage we can get out of the BJT differential amplifier is equal to

$$V_{od,\max} = \alpha \cdot I_{tail} \cdot R_L \tag{5.28}$$

This is the differential output when $|V_{id}|$ is large enough such that all the tail current is flowing only on one side of the differential circuit.

5.2.2 The Common-Mode Signal Revisited

In order to simplify some of the analysis, but without loosing generality, we can assume that the input signals going into our differential amplifiers are of the form

$$v_{i1} = \frac{\hat{V}}{2} \cdot \cos\left(\omega t\right) + V_{cm} \tag{5.29}$$

$$v_{i2} = -\frac{\hat{V}}{2} \cdot \cos\left(\omega t\right) + V_{cm} \tag{5.30}$$

resulting in

$$v_{id} = v_{i1} - v_{i2} = \hat{V} \cdot \cos\left(\omega t\right) \tag{5.31}$$

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2} = V_{cm} \tag{5.32}$$

Thus, we can think of the common-mode input as a DC offset where, on top of which, we add our differential signal. Notice that v_{i1} and v_{i2} are purely differential signals since if v_{i1} increases by ΔV, v_{i2} will decrease by the same amount, relative to the common-mode voltage V_{cm}.

5.2.3 The Common-Mode Input Range

Note that Eqs. 5.19, 5.20, 5.22, 5.23, and 5.27 assume the transistor is operating in the forward-active region. In order to check the BJT operating region, we need to get the collector-emitter voltage. From Fig. 5.3, we see that

$$V_{CE1} = V_{CC} - I_{C1}R_L - V_X \tag{5.33}$$

where V_X is the voltage across the tail current source. Note that for a collector current, I_{C1}, we get

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_S}\right) \tag{5.34}$$

Therefore, we can express V_X as

$$V_X = V_{I1} - V_{BE1} \tag{5.35}$$

Thus, combining Eqs. 5.33 and 5.35, we get

$$V_{CE1} = V_{CC} - I_{C1}R_L - V_{I1} + V_T \ln\left(\frac{I_{C1}}{I_S}\right) \tag{5.36}$$

and similarly

$$V_{CE2} = V_{CC} - I_{C2}R_L - V_{I2} + V_T \ln\left(\frac{I_{C2}}{I_S}\right) \tag{5.37}$$

For the case when there is no differential input,

$$v_{i1} = V_{I1} = v_{i2} = V_{I2} = v_{ic} = V_{cm} \tag{5.38}$$

This implies that

$$I_{C1} = I_{C2} = \frac{I_{tail}}{2} \tag{5.39}$$

since the left and right side of the differential amplifier is the same, the tail current splits equally between these two sides. Thus, Eq. 5.36 becomes

$$V_{CE1} = V_{CC} - \frac{I_{tail}R_L}{2} - V_{cm} + V_T \ln\left(\frac{I_{tail}}{2 \cdot I_S}\right) > V_{CE,sat} \tag{5.40}$$

It is very important to note that as long as the transistors are in the forward-active region, the amplifier can accept a range of common-mode input voltages, and still have $I_{C1} = I_{C2} = \frac{I_{tail}}{2}$. As the common-mode input voltage is changed, the collector currents will remain the same, as enforced by the tail current source. Since the collector currents remain the same, the base-emitter voltages will also remain the same. Thus, as the common-mode input voltage increases, the voltage at node x will increase with it[b].

Using Eq. 5.40, we can then calculate the maximum common-mode input voltage as

$$V_{cm} < V_{CC} - \frac{I_{tail}R_L}{2} - V_{CE,sat} + V_T \ln\left(\frac{I_{tail}}{2 \cdot I_S}\right) = V_{cm,\max} \tag{5.41}$$

If the tail current source is not ideal and has a required minimum voltage, $V_{\min}$, then using Eq. 5.35, the minimum common-mode input voltage can then be expressed as

$$V_{cm} > V_{\min} + V_T \ln\left(\frac{I_{tail}}{2 \cdot I_S}\right) = V_{cm,\min} \tag{5.42}$$

Eqs. 5.41 and 5.42 defines the *common-mode input range* of the differential amplifier in Fig. 5.3. The common-mode input range is defined as the range of common-mode inputs that the amplifier can tolerate and still maintain proper transistor operating regions.

Unlike single-ended amplifiers and circuits, where the input DC voltages can drastically change transistor bias currents, differential amplifiers have the advantage of being able to tolerate a relatively large range of input DC voltages, while maintaining transistor bias currents.

[b] Readers will recognize that the path from v_{i1} to node x is a common-collector or emitter-follower path, and it should be no surprise that node x will try to follow v_{i1}.

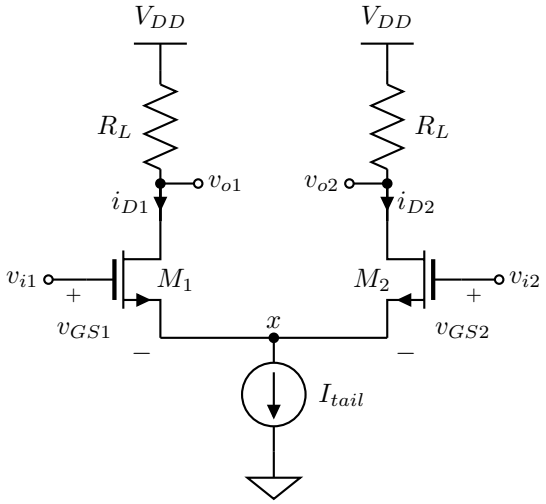


Figure 5.5: The MOSFET differential pair.

5.3 The MOSFET Differential Amplifier

We can use MOSFETs to build differential amplifier, as seen in Fig. 5.5. Once again, we can write the KVL equation for the input loop as

$$V_{i1} - V_{i2} = V_{id} = V_{GS1} - V_{GS2} \tag{5.43}$$

$$V_{id} = \left(V_{TH} + \sqrt{\frac{I_{D1}}{k}}\right) - \left(V_{TH} + \sqrt{\frac{I_{D2}}{k}}\right) = \sqrt{\frac{I_{D1}}{k}} - \sqrt{\frac{I_{D2}}{k}} \tag{5.44}$$

and again applying KCL at node x, we get

$$I_{tail} = I_{D1} + I_{D2} \tag{5.45}$$

Using Eqs. 5.44 and 5.45 to solve for the drain currents, we get

$$I_{D1} = \frac{I_{tail}}{2} + V_{id} \cdot \frac{k}{2} \cdot \sqrt{\frac{2 \cdot I_{tail}}{k} - V_{id}^2} = \frac{I_{tail}}{2} + \Delta I \tag{5.46}$$

$$I_{D2} = \frac{I_{tail}}{2} - V_{id} \cdot \frac{k}{2} \cdot \sqrt{\frac{2 \cdot I_{tail}}{k} - V_{id}^2} = \frac{I_{tail}}{2} - \Delta I \tag{5.47}$$

Note that for Eqs. 5.46 and 5.47, $I_{D1,\max} = I_{D2,\max} = I_{tail}$ and $I_{D1,\min} = I_{D2,\min} = 0$, as dictated by the tail current source. However, increasing or decreasing V_{id} in Eqs. 5.46 and 5.47 can result in currents larger than the maximum or currents below the minimum current. This means that at a certain differential input voltage, one transistor will cut-off, while the other will carry all of I_{tail}. This condition occurs when

$$\Delta I = \frac{I_{tail}}{2} = V_{id,\max} \cdot \frac{k}{2} \cdot \sqrt{\frac{2 \cdot I_{tail}}{k} - V_{id,\max}^2} \tag{5.48}$$

Solving for $V_{id,\max}$, we get

$$V_{id,\max} = \sqrt{\frac{I_{tail}}{k}} \tag{5.49}$$

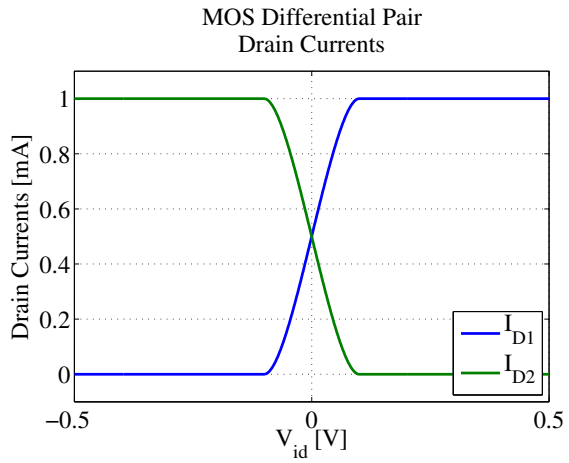
Thus, as long as $|V_{id}| \leq V_{id,\max}$, Eqs. 5.46 and 5.47 are valid. However, if the input differential voltage is outside this range, then for $V_{id} > 0$, $I_{D1} = I_{tail}$ and $I_{D2} = 0$, and for $V_{id} < 0$, $I_{D1} = 0$ and $I_{D2} = I_{tail}$, as seen in Fig. 5.6a.

The differential output voltage is then

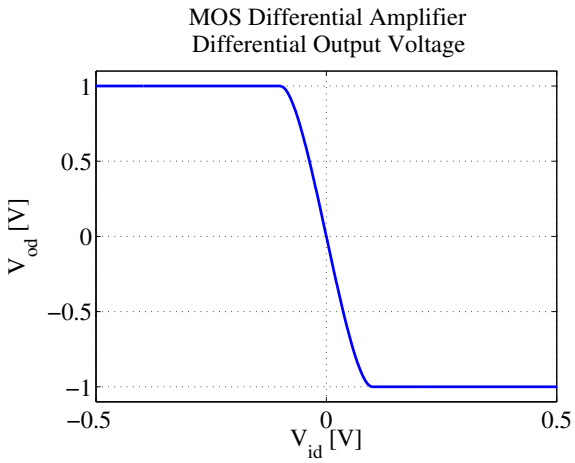
$$V_{od} = V_{o1} - V_{o2} = R_L \left(I_{D2} - I_{D1}\right) = -R_L \cdot k \cdot V_{id} \cdot \sqrt{\frac{2 \cdot I_{tail}}{k} - V_{id}^2} \tag{5.50}$$

Using Eqs. 5.49 and 5.50, we can calculate the maximum value of the differential output voltage as

$$V_{od,\max} = R_L \cdot k \cdot V_{id,\max} \cdot \sqrt{\frac{2 \cdot I_{tail}}{k} - V_{id,\max}^2} = R_L \cdot I_{tail} \tag{5.51}$$



(a) Drain currents



(b) Output voltage

Figure 5.6: MOSFET differential pair large signal characteristics with $V_{TH} = 1\,\text{V}$, $k = 100\,\frac{\text{mA}}{\text{V}^2}$, using $R_L = 1\,\text{k}\Omega$, a tail current of 1 mA, and a supply voltage of 5 V.

which is expected since the maximum differential voltage appears when all the current is already on one side of the differential pair, resulting in zero current on the other side, as seen in Fig. 5.6b.

5.3.1 Common-Mode Input Range

The drain-source voltage of transistor M_1 can be expressed as

$$V_{DS1} = V_{DD} - I_{D1}R_L - V_X \tag{5.52}$$

We can then express V_X as

$$V_X = V_{I1} - V_{GS1} \tag{5.53}$$

Thus, to prevent M_1 from going into the linear region,

$$V_{DS1} = V_{DD} - I_{D1}R_L - V_{I1} + V_{GS1} > V_{GS1} - V_{TH} \tag{5.54}$$

If we set the differential input to zero and apply only the common-mode input, $V_{I1} = V_{I2} = V_{cm}$, we get

$$V_{DD} - \frac{I_{tail}R_L}{2} - V_{cm} > -V_{TH} \tag{5.55}$$

Therefore,

$$V_{cm} < V_{DD} - \frac{I_{tail}R_L}{2} + V_{TH} = V_{cm,\max} \tag{5.56}$$

The common-mode input must also be large enough to support the minimum voltage requirement, $V_{\min}$, of the tail current source, thus

$$V_X = V_{cm} - V_{GS1} > V_{\min} \tag{5.57}$$

Thus,

$$V_{cm} > V_{\min} + V_{GS1} = V_{\min} + V_{TH} + \sqrt{\frac{I_{tail}}{2 \cdot k}} = V_{cm,\min} \tag{5.58}$$

5.4 Small Signal Analysis

After obtaining the quiescent DC currents of the simple differential amplifier, we can now determine the corresponding small signal two-port characteristics. The small signal equivalent circuit of the BJT differential amplifier in Fig. 5.3 is shown in Fig. 5.7.

Let us analyze the small signal behavior of the differential amplifier in two steps. First, we will look at the amplifier's response to purely differential signals, then we will look at the response to purely common-mode signals. Since the small signal equivalent circuit is linear, we can get the total behavior of the differential amplifier by superposition.

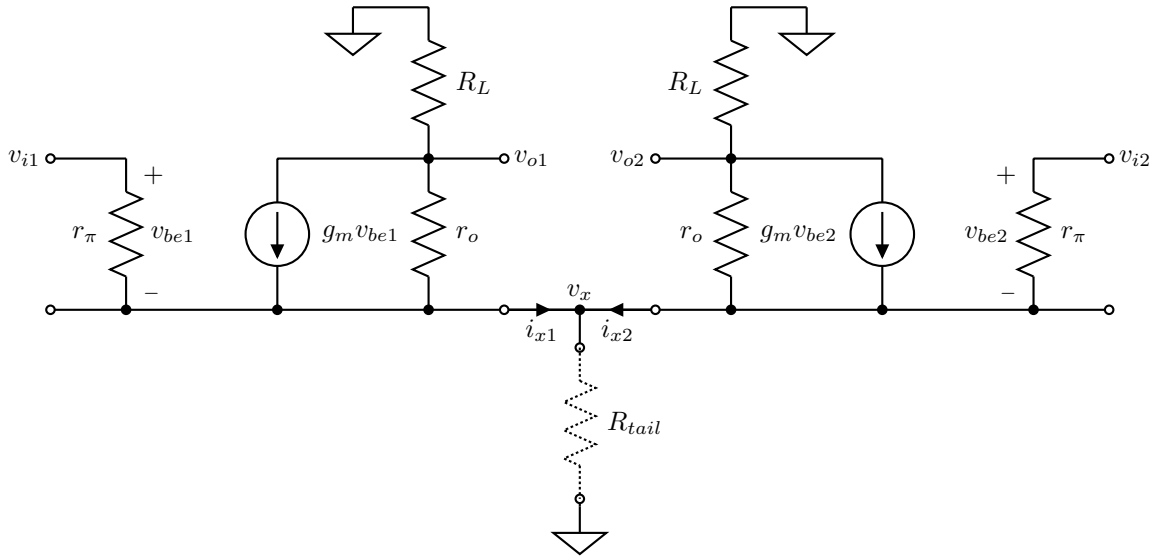


Figure 5.7: The small signal equivalent circuit of the BJT differential amplifier in Fig. 5.3.

5.4.1 The Differential Half Circuit

If we only have purely differential signals, then this means that for an input differential voltage, v_{id},

$$v_{i1} = +\frac{v_{id}}{2} \tag{5.59}$$

$$v_{i2} = -\frac{v_{id}}{2} \tag{5.60}$$

such that

$$v_{id} = v_{i1} - v_{i2} \tag{5.61}$$

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2} = 0 \tag{5.62}$$

Eqs. 5.59 and 5.60 mathematically models the fact that if the inputs are purely differential inputs, then a small change in v_{i1} would be accompanied by the same change in v_{i2} but in the opposite direction.

Writing out the KVL expression for the input loop, we get

$$v_{i1} - v_{be1} + v_{be2} - v_{i2} = \left(+\frac{v_{id}}{2}\right) - v_{be1} + v_{be2} - \left(-\frac{v_{i2}}{2}\right) = 0 \tag{5.63}$$

thus,

$$v_{id} = v_{i1} - v_{i2} = v_{be1} - v_{be2} \tag{5.64}$$

Note that v_x is the midpoint between $+\frac{v_{id}}{2}$ and $-\frac{v_{id}}{2}$. Thus, for any purely differential input, v_{id}, and if the left and right sides of the circuit are perfectly matched, then we will always get

$$v_x = 0 \tag{5.65}$$

Since v_x is always zero for purely differential inputs, then node x can be considered a *virtual ground* node. Therefore, we can redraw the small signal equivalent circuit in Fig. 5.7, and obtain the differential small signal equivalent circuit in Fig. 5.8.

By making node x a virtual ground, we have effectively decoupled the left and right sides of the differential small signal equivalent circuit. Thus, we can solve for the differential small signal two-port parameters using either the left or right side of the circuit in Fig. 5.8.

Using the left half circuit, we can calculate the differential mode gain as

$$A_{dm} = \frac{+\frac{v_{od}}{2}}{+\frac{v_{id}}{2}} = \frac{v_{od}}{v_{id}} = -g_m \cdot (r_o \parallel R_L) \tag{5.66}$$

If we apply a test voltage, $+\frac{v_{id}}{2}$, at the input, we get

$$i_{id} = \frac{+\frac{v_{id}}{2}}{r_\pi} \tag{5.67}$$

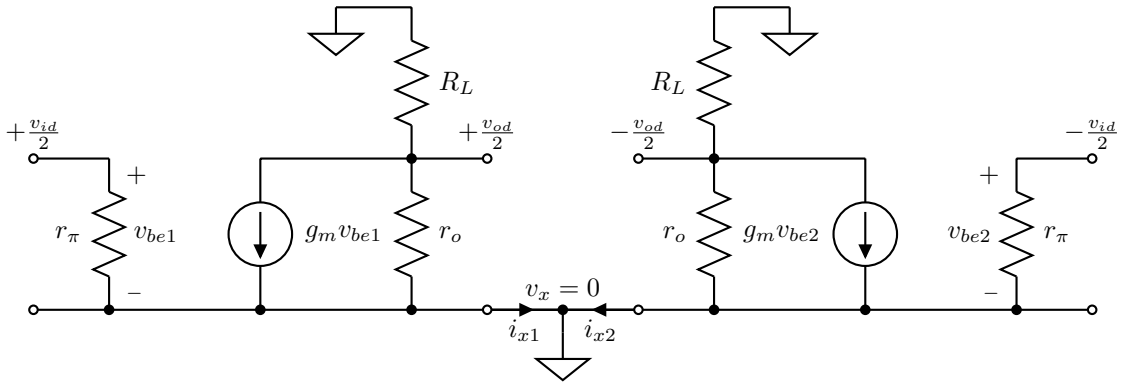


Figure 5.8: The differential small signal equivalent circuit of the amplifier in Fig. 5.3.

Thus, the input resistance can be expressed as

$$R_{id} = \frac{v_{id}}{i_{id}} = 2 \cdot r_\pi \tag{5.68}$$

Similarly, if we zero out the input, and apply a test voltage, $+\frac{v_{od}}{2}$, at the output, we get

$$i_{od} = \frac{+\frac{v_{od}}{2}}{r_o \parallel R_L} \tag{5.69}$$

The output resistance is then

$$R_{od} = \frac{v_{od}}{i_{od}} = 2 \cdot (r_o \parallel R_L) \tag{5.70}$$

We would get exactly the same expressions if we used the right half circuit of Fig. 5.8.

It is important to node that while we can consider node x as a virtual ground, no small signal current flows from node x to the small signal ground. Instead, all the current going into node x from the left half circuit is exactly the same current going out of node x into the right half circuit. Thus,

$$i_{x1} = -i_{x2} \tag{5.71}$$

This is consistent with purely differential mode inputs, since any small signal increase in voltage or current on the left side would correspond to a decrease of equal magnitude on the right side. This is true for the open circuit from node x to ground in Fig. 5.7, but it is also true even if we add any resistance to ground (e.g. if we use a tail current source with finite output resistance, R_{tail}), since $v_x = 0$.

5.4.2 The Common-Mode Half Circuit

If we only apply a purely common-mode input, v_{ic}, such that

$$v_{ic} = v_{i1} = v_{i2} \tag{5.72}$$

the differential input component will be

$$v_{id} = v_{i1} - v_{i2} = 0 \tag{5.73}$$

So if the left side of the differential amplifier is perfectly matched to the right side, then the output differential voltage will also be zero, hence

$$v_{o1} = v_{o2} = v_{oc} \tag{5.74}$$

This also means that there will be no current flowing from the left side to the right side (or vice versa) since every single node on the left side will have the same voltage as the corresponding node on the right, thus

$$i_{x1} = i_{x2} = 0 \tag{5.75}$$

Extending this idea to the whole circuit, any connection from the left side and the right side would have zero current, isolating the left side from the right. This allows us to calculate the common-mode small signal parameters using only one side of the circuit in Fig. 5.7.

To solve for the common-mode gain, we first write out the KCL equation at node x,

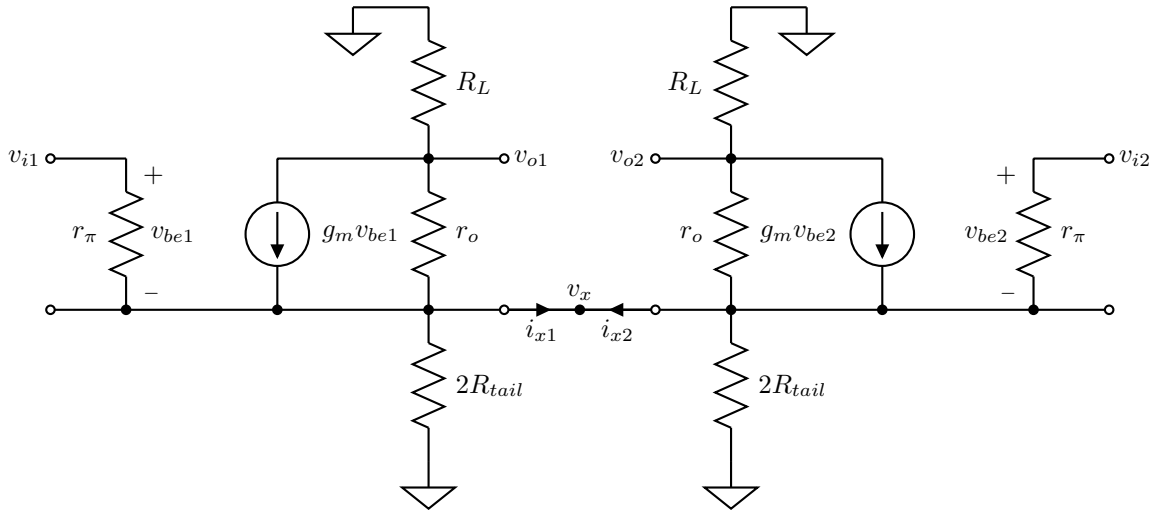


Figure 5.9: The common-mode small signal equivalent circuit of the BJT differential amplifier in Fig. 5.3.

$$\frac{v_x - v_{ic}}{r_\pi} + \frac{v_x - v_{oc}}{r_o} - g_m\left(v_{ic} - v_x\right) = 0 \tag{5.76}$$

and recognizing the that the current passing through r_π is the same current passing through R_L, we get

$$\frac{v_{oc}}{R_L} = \frac{v_{ic} - v_x}{r_\pi} \tag{5.77}$$

Using Eqs. 5.76 and 5.77, we can then express v_{oc} as

$$v_{oc} = v_{ic} \cdot \frac{R_L}{R_L + r_o + r_\pi\left(1 + g_m r_o\right)} \tag{5.78}$$

Thus, the small signal common-mode gain is

$$A_{cm} = \frac{v_{oc}}{v_{ic}} = \frac{R_L}{R_L + r_o + r_\pi\left(1 + g_m r_o\right)} \tag{5.79}$$

Assuming that$g_m r_o \gg 1$ and $r_o \gg R_L$, we get

$$A_{cm} \approx \frac{R_L}{r_\pi g_m r_o} \approx \frac{R_L}{\frac{\beta}{g_m} g_m r_o} \approx \frac{R_L}{\beta \cdot r_o} \approx 0 \tag{5.80}$$

If the tail current source is not ideal, but instead has an output resistance R_{tail}, breaks the even symmetry of the small signal model, making it hard to distinguish the left side of the circuit in Fig. 5.8 from the right side. To restore even symmetry, we can decompose R_{tail} into two parallel resistors, each with resistance value $2R_{tail}$, as shown in Fig. 5.9. Since we have even symmetry once again, and $i_{x1} = i_{x2} = 0$, then we can solve for the common-mode gain using only either the left or right half circuit.

If we take the left half circuit, and recognizing that this is exactly the same as the equivalent circuit of an emitter degenerated common-emitter amplifier, with $R_E = 2R_{tail}$, then the common-mode gain can be expressed as

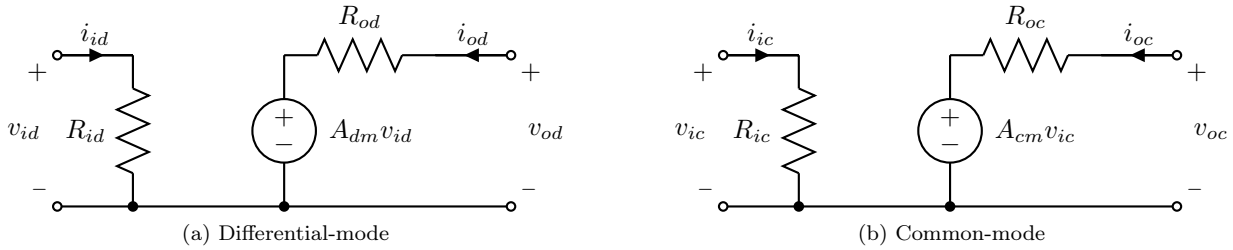
$$A_{cm} = -\frac{g_m R_L}{1 + 2 \cdot g_m R_{tail}} \tag{5.81}$$

Note that since the common-mode source has to supply the input currents of both the left and right half circuits, the common-mode input resistance is half that of the input resistance of the common-emitter amplifier with emitter degeneration. Thus,

$$R_{ic} = \frac{v_{ic}}{i_{ic,left} + i_{ic,right}} = \frac{v_{ic}}{2i_{ic}} = \frac{r_\pi\left(1 + 2 \cdot g_m R_{tail}\right)}{2} \tag{5.82}$$

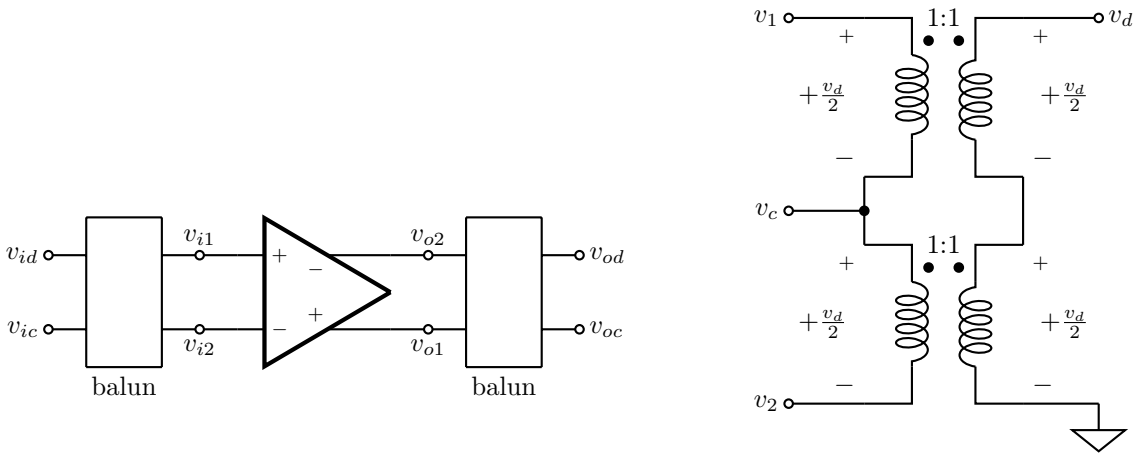
As expected, the output resistance will also be half of the emitter-degenerated amplifier output resistance since for the same output test voltage, we get twice the output current, one for each half circuit. Thus,

$$R_{oc} = \frac{v_{oc}}{i_{oc,left} + i_{oc,right}} = \frac{v_{oc}}{2i_{oc}} = \frac{r_o\left(1 + 2 \cdot g_m R_{tail}\right)}{2} \tag{5.83}$$



(a) Differential-mode (b) Common-mode

Figure 5.10: The small signal model of the BJT differential amplifier.



(a) Differential signal conversion (b) Equivalent circuit

Figure 5.11: The balun.

In summary, differential amplifiers process the differential- and common-mode signals differently. We can then think of differential amplifiers as two distinct amplifiers, one processing the differential-mode signal, and the other, manipulating the common-mode input, as shown in Fig. 5.10.

Note that the small signal analysis for MOSFET differential amplifiers is exactly the same as the analysis of its BJT counterpart. The only difference would be the expressions used to determine the transistor small signal two-port parameters, leading to $r_\pi \to \infty$.

5.5 The Balun

In many situations, it is necessary to convert single-ended signals into differential signals, and vice versa. For example, the differential component of the input could be generated separately from the common-mode DC input component, also known as an "unbalanced" pair. From the unbalanced pair, we want to generate "balanced" two wires whose difference contains the differential information, and whose average contains the common-mode information. Fig. 5.11a shows a system that uses a "balanced-unbalanced" converter, or a *balun*, to convert from the (v_d, v_c) coordinate system to the (v_1, v_2) coordinate system an vice-versa.

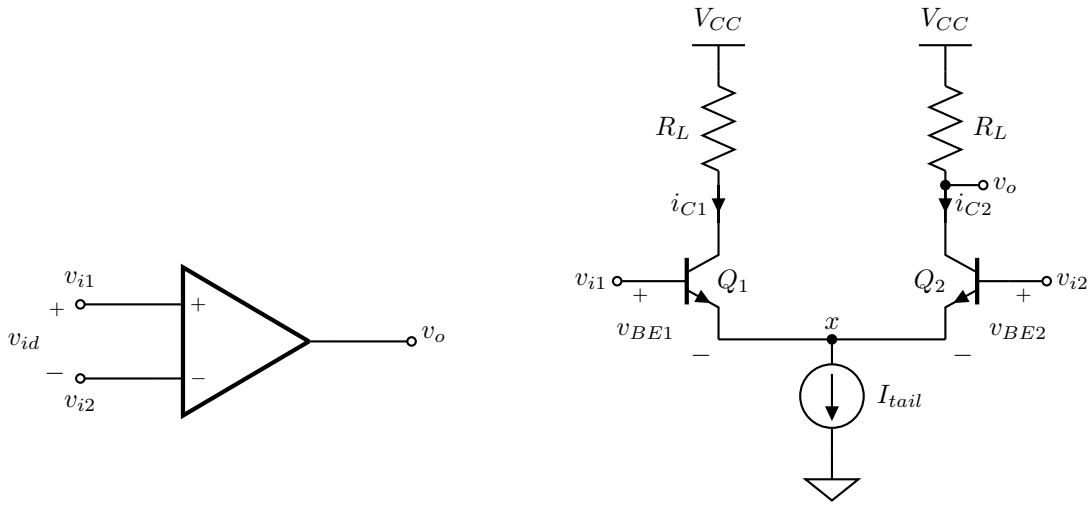
Fig. 5.11b shows a very simple balun implementation using two ideal transformers. Note that the circuit in Fig. 5.11b is bidirectional. Given v_d and v_c, it generates v_1 and v_2, realizing Eqs. 5.3 and 5.4, and if given v_1 and v_2, the balun generates v_d and v_c, as described in Eqs. 5.1 and 5.2.

5.6 Differential to Single-Ended Conversion

In some cases, the circuits driven by our amplifiers can only accept single-ended signals referred to ground. We still however, want to be able to transfer the differential output signal to the load circuit. Simply connecting one differential output to ground is normally not a good idea since the output node usually has some non-zero DC output level.

Differential input, single-ended output amplifiers, whose symbol is shown in Fig. 5.12a, are a class of amplifiers that allows us to drive single-ended loads. A relatively straightforward implementation of such an amplifier, seen in Fig. 5.12b, simply takes one side of the differential amplifier output, as the terminal used to drive the single-ended load.

Using our differential half circuit analysis, we get



(a) Symbol (b) A simple implementation

Figure 5.12: A single-ended output differential input amplifier.

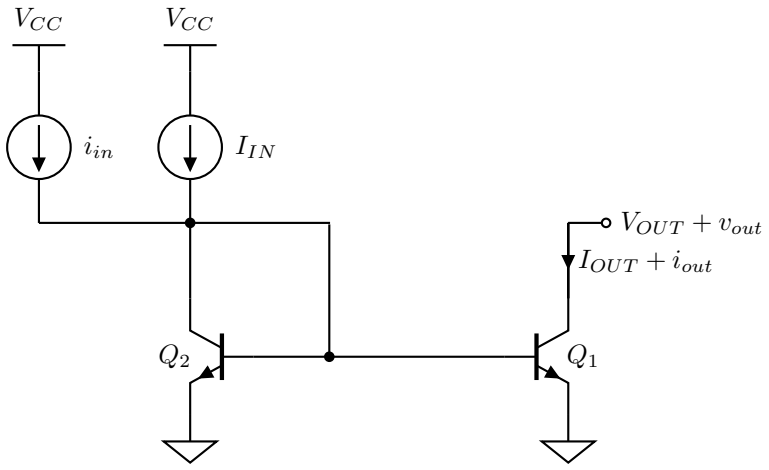


Figure 5.13: The simple BJT current mirror with small signal input current, i_{in}.

$$v_o = -g_m \left(r_o \parallel R_L\right) \cdot \left(-\frac{v_{id}}{2}\right) \tag{5.84}$$

The gain is then

$$A_v = \frac{v_o}{v_{id}} = \frac{g_m \left(r_o \parallel R_L\right)}{2} \tag{5.85}$$

As expected, the single-ended gain is only half the fully differential gain, since we are only using one half of the differential amplifier's capacity. This method of driving single-ended loads, however, is not very efficient, since we are not only getting half the gain of a common-emitter amplifier, but also comsuming twice the current for the same g_m.

An alternative way to generate a single-ended signal from a fully differential amplifier is through the use of current mirrors.

5.6.1 The Current Mirror Revisited

Before we use current mirrors for differential-to-single-ended signal conversion, we need another look at their small signal behavior. If we add a small signal current, i_{in}, on top of the DC current, I_{IN}, at the input of our current mirror, as shown in Fig. 5.13, how much of that would make it to the output?

We can easily derive the small signal equivalent circuit of the current mirror, as seen in Fig. 5.14 . Assuming $g_m r_o \gg 1$ and that β and r_o are relatively large, calculating the base-emitter voltage of both transistors, we get

$$v_{be1} = v_{be2} = i_{in} \cdot \left(\frac{1}{g_{m2}} \parallel r_{o2} \parallel r_{\pi 1} \parallel r_{\pi 2}\right) \approx \frac{i_{in}}{g_{m2}} \tag{5.86}$$

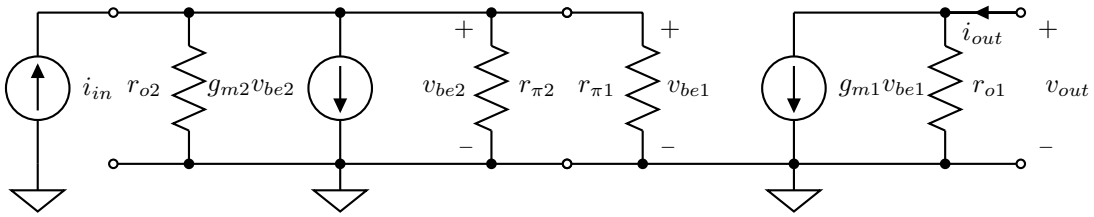


Figure 5.14: Small signal quivalent of the circuit in Fig. 5.13.

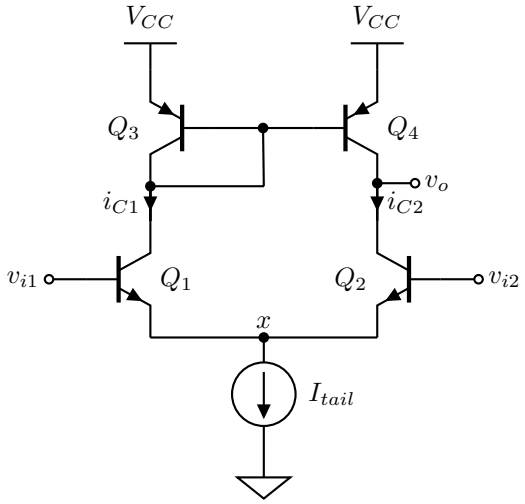


Figure 5.15: Differential to single-ended conversion using current mirrors.

Thus, if we assume that $I_{C1} \approx I_{C2}$, then the small signal output current is

$$i_{out} \approx g_{m1} v_{be1} = \frac{g_{m1}}{g_{m2}} \cdot i_{in} \approx i_{in} \tag{5.87}$$

This very simple analysis shows that the current mirror is not only a mirror for DC input currents, but is also a mirror for small signal input currents. We will use this property to make our differential-to-single-ended conversion more efficient in terms of gain.

5.6.2 Current Mirror Loads

Fig. 5.15 shows a differential amplifier, but instead of resistors, the load is a PNP current mirror, where the output, v_o, is a single-ended signal.

Since the amplifier in Fig. 5.15 no longer exhibits any symmetry, we cannot apply our half circuit analysis techniques, and we will need to perform the analysis on the whole small signal equivalent circuit, shown in Fig. 5.16.

If we once again assume that $g_m r_o \gg 1$, and that β and r_o are relatively large, we can simplify the small signal equivalent circuit in Fig. 5.16, as shown in Fig. 5.17. For purely differential inputs, node x will still be at virtual ground, and $v_{be1} = +\frac{v_{id}}{2}$ and $v_{be2} = -\frac{v_{id}}{2}$. Note that

$$v_{be3} = -g_{m1} \cdot \frac{v_{id}}{2} \cdot \frac{1}{g_{m3}} = v_{be4} \tag{5.88}$$

By shorting the output to ground, no current will pass through r_{o2} and r_{o4}, thus we can calculate the effective transconductance of the amplifier by first calculating the output short circuit current, i_o, as

$$i_o = g_{m4} \cdot v_{be4} + g_{m2} \cdot v_{be2} = -g_{m4} \cdot g_{m1} \cdot \frac{v_{id}}{2} \cdot \frac{1}{g_{m3}} - g \cdot \frac{v_{id}}{2} \tag{5.89}$$

If $g_{m1} = g_{m2} = g_m$ and $g_{m3} = g_{m4}$, we will get

$$i_o = -g_m \cdot v_{id} \tag{5.90}$$

Thus, the effective circuit transconductance is

$$G_m = -g_m \tag{5.91}$$

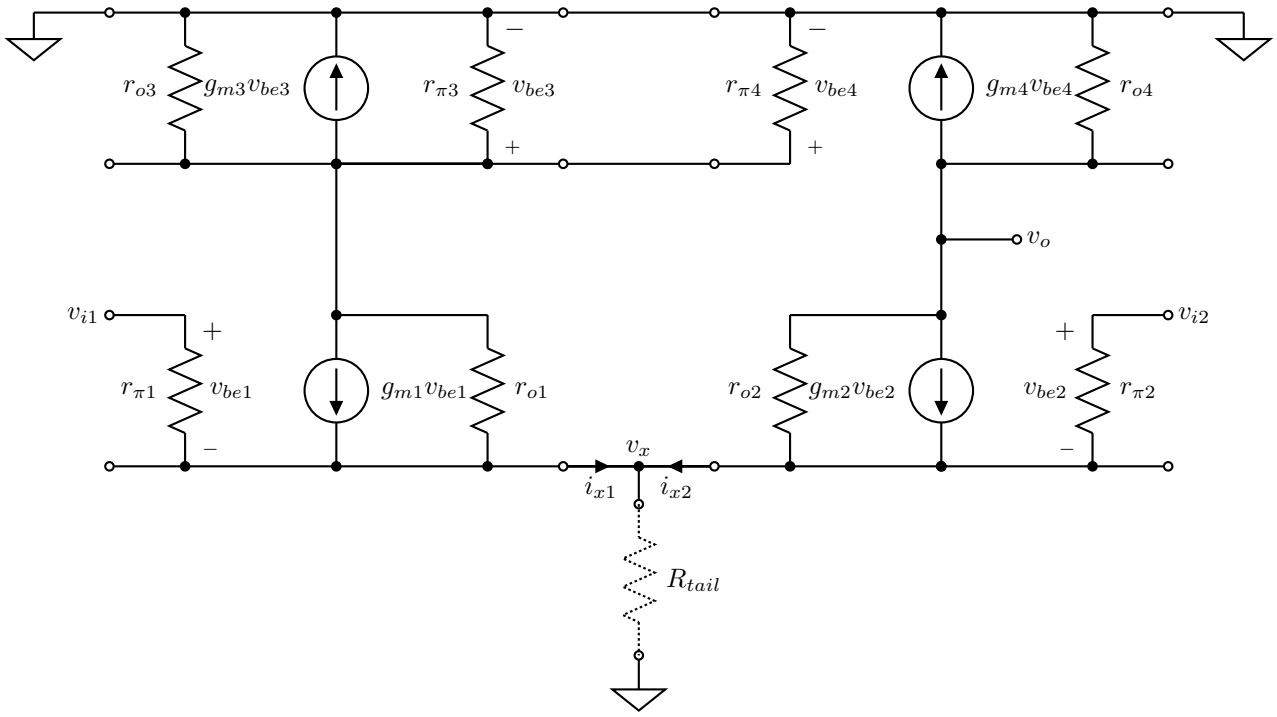


Figure 5.16: The small signal equivalent circuit of the amplifier in Fig. 5.15.

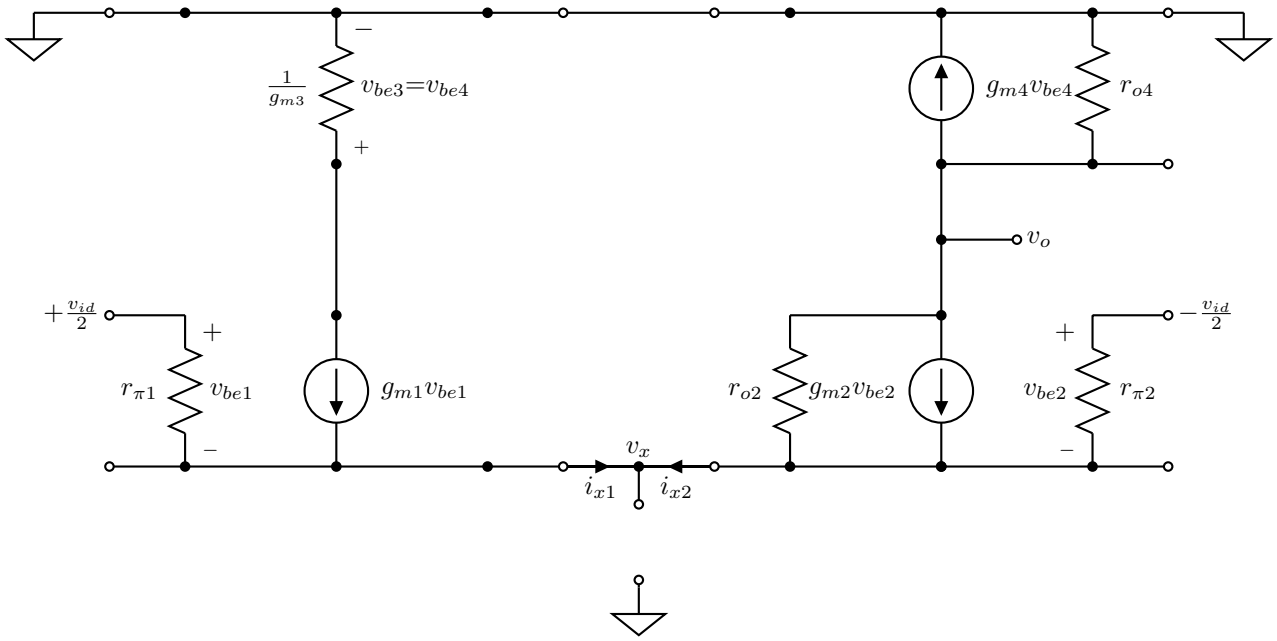


Figure 5.17: Simplified differential small signal equivalent of the circuit in Fig. 5.16.

If we zero out the input, then by inspecting the circuit in Fig. 5.17, we can see that all the dependent current sources will be turned off (zero current), thus the output resistance is

$$R_o = (r_{o2} \parallel r_{o4}) \tag{5.92}$$

The overall gain from the differential input to the single-ended output is

$$A_v = \frac{v_o}{v_{id}} = -G_m R_o = g_m (r_{o2} \parallel r_{o4}) \tag{5.93}$$

We can easily see that with the current mirror load, we will be able to achieve the same gain as the fully differential amplifier. Note that by using a current mirror as the differential amplifier load allows us to redirect the small signal current of the left half circuit to the output, where it combines constructively with the current generated by the right half circuit.

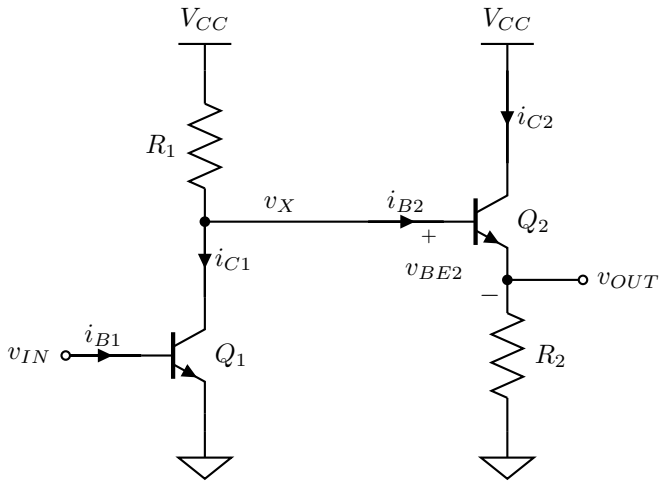


Figure 6.1: The CE-CC 2-stage amplifier.

6 Compound Amplifiers

In the single-stage and differential amplifiers we have seen so far, both the small signal characteristics, such as the voltage gain, transconductance, input and output resistances, and the large signal characteristics such as output swing, and input common-mode range, are very dependent on the amplifier topology used. In most cases, we want to "mix-and-match" these characteristics, and design an amplifier better suited for a given task.

For example, a common-emitter amplifier can have very large voltage gains, but this gain can only be realized if the output resistance is large. Thus, if we use the amplifier to drive very low resistance loads, the voltage gain is drastically reduced. But what if we want both high gain, and low output resistance? In this case, we can use several amplifiers, leveraging each others strengths, and avoiding the characteristics we do not want for a given application.

6.1 The Common-Emitter Common-Collector (CE-CC) Amplifier

One very common 2-stage amplifier topology is the common-emitter amplifier, followed by a common-collector amplifier, shown in Fig. 6.1.

In order to calculate the quiescent DC collector currents of both transistors, we write the KVL equation of the loop between the two stages as

$$V_{CC} - (I_{C1} + I_{B2}) \cdot R_1 - V_{BE2} - I_{E2}R_2 = 0 \tag{6.1}$$

Recall that

$$I_{C1} = I_{S1} \cdot e^{\frac{V_{IN}}{V_T}} \tag{6.2}$$

and

$$V_{BE2} = V_T \cdot \ln\left(\frac{I_{C2}}{I_{S2}}\right) \tag{6.3}$$

we can solve for I_{C2} using

$$V_{CC} - I_{S1} \cdot e^{\frac{V_{IN}}{V_T}} \cdot R_1 - \frac{I_{C2}}{\beta_2} \cdot R_1 - V_T \cdot \ln\left(\frac{I_{C2}}{I_{S2}}\right) - \frac{I_{C2}}{\alpha_2} \cdot R_2 = 0 \tag{6.4}$$

Note that the quiescent DC input voltage of the second stage is set by the quiescent output DC voltage of the first stage. Thus, it is important that the DC output voltage of the first stage be set to the voltage required by the second stage, as determined by the small signal specifications of the compound amplifier. If we assume that $\beta_2 \to \infty$, and $V_{BE2} \approx 0.7\,\text{V}$, then

$$I_{C2} = \frac{V_{CC} - I_{S1} \cdot e^{\frac{V_{IN}}{V_T}} \cdot R_1 - 0.7\,\text{V}}{R_2} \tag{6.5}$$

Once we have obtained the DC bias currents, we can now calculate the small signal parameters of the CE-CC amplifier by looking at the two component amplifier stages individually as shown in Fig. 6.2.

Recall that for the CE amplifier,

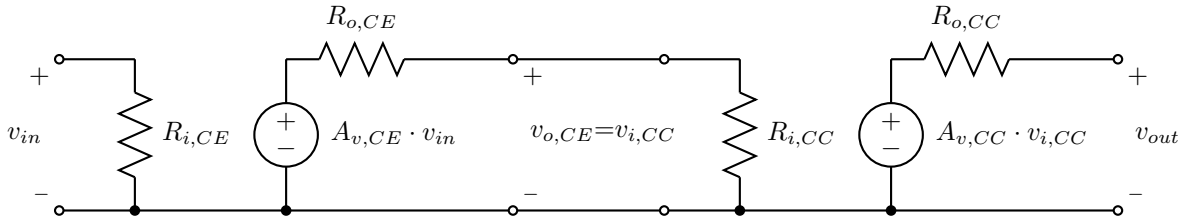


Figure 6.2: The CE-CC small signal equivalent circuit.

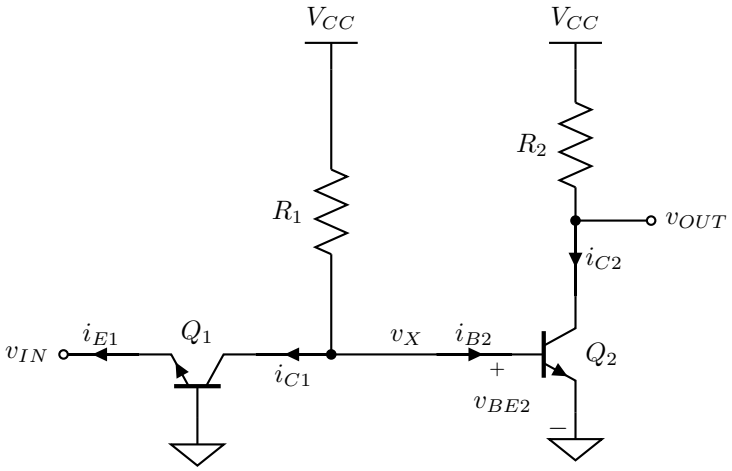


Figure 6.3: The CB-CE 2-stage amplifier.

$$A_{v,CE} = -g_{m1}\left(r_o \parallel R_1\right) \approx -g_{m1}R_1 \tag{6.6}$$

$$R_{o,CE} = \left(r_{o1} \parallel R_1\right) \approx R_1 \tag{6.7}$$

$$R_{i,CE} = r_{\pi 1} \tag{6.8}$$

and for the CC amplifier,

$$A_{v,CC} = \frac{g_{m2}R_2}{1+g_{m2}R_2} \approx 1 \tag{6.9}$$

$$R_{o,CC} = \frac{R_2}{1+g_{m2}R_2} \approx \frac{1}{g_{m2}} \tag{6.10}$$

$$R_{i,CC} = r_{\pi 2}\left(1+g_{m2}R_2\right) \tag{6.11}$$

Thus, the effective CE-CC amplifier two-port parameters are

$$A_{v,CE-CC} = A_{v,CE} \cdot \frac{R_{i,CC}}{R_{i,CC}+R_{o,CE}} \cdot A_{v,CC} = -g_{m1}R_1 \cdot \frac{r_{\pi 2}\left(1+g_{m2}R_2\right)}{r_{\pi 2}\left(1+g_{m2}R_2\right)+R_1} \approx -g_{m1}R_1 \tag{6.12}$$

$$R_{o,CE-CC} = R_{o,CC} = \frac{R_2}{1+g_{m2}R_2} \approx \frac{1}{g_{m2}} \tag{6.13}$$

$$R_{i,CE-CC} = R_{i,CE} = r_{\pi 1} \tag{6.14}$$

Notice that by cascading the two basic amplifier stages, we can create a new amplifier with approximately the same voltage gain and input resistance, but now has a significantly lower output resistance. This low output resistance is very useful in driving loads with small input resistances, such as $8\,\Omega$ speakers.

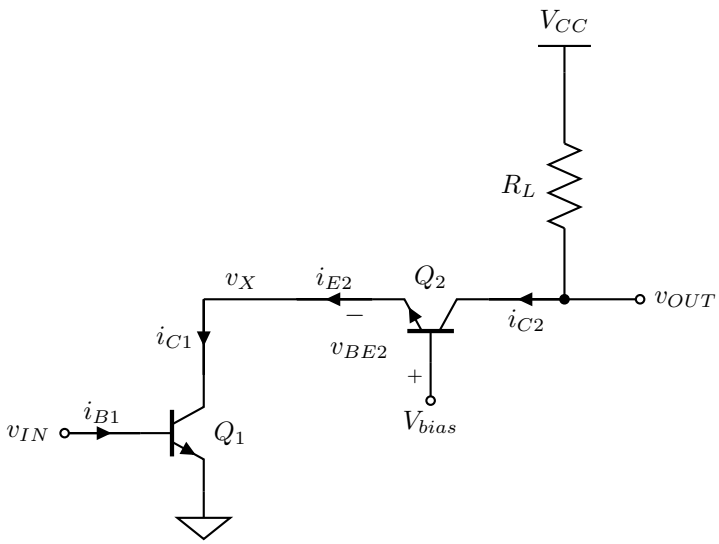


Figure 6.4: The cascode amplifier.

6.2 The Common-Base Common-Emitter (CB-CE) Amplifier

Another common topology is the common-base amplifier followed by a common-emitter amplifier, shown in Fig. 6.3.

Similar to the CE-CC amplifier, the input bias of the second stage is a function of the DC output voltage of the first stage. Writing the KVL equation around the loop in between the two stages, we get

$$V_{CC} - (I_{C1} + I_{B2}) \cdot R_1 - V_{BE2} = 0 \tag{6.15}$$

Recognizing that $V_{BE1} = -V_{IN}$, and that once again, $V_{BE2} = V_T \cdot \ln\left(\frac{I_{C2}}{I_S}\right)$, we get

$$V_{CC} - I_{S1} \cdot e^{\frac{-V_{IN}}{V_T}} \cdot R_1 - \frac{I_{C2}}{\beta_2} \cdot R_1 - V_T \cdot \ln\left(\frac{I_{C2}}{I_S}\right) \tag{6.16}$$

which we can then use to solve for I_{C2}.

Similar to the CE-CC amplifier, we can now calculate the overall gain of the CB-CE pair as

$$A_{v,CB-CE} = A_{v,CB} \cdot \frac{R_{i,CE}}{R_{i,CE} + R_{o,CB}} \cdot A_{v,CE} = g_{m1} R_1 \cdot \frac{r_{\pi 2}}{r_{\pi 2} + R_1} \cdot (-g_{m2} R_2) \approx -g_{m1} g_{m2} R_1 R_2 \tag{6.17}$$

and the input and output resistances as

$$R_i = R_{i,CB} = \frac{1}{g_{m1}} + \frac{R_1 \parallel r_{\pi 2}}{g_{m1} r_{o1}} \approx \frac{1}{g_{m1}} \tag{6.18}$$

$$R_o = R_{o,CE} = r_{o2} \parallel R_2 \approx R_2 \tag{6.19}$$

Note that the input resistance of the CB-CE pair is a function of the transconductance, and thus, the collector current of the common-base stage. This dependency of the input resistance to I_{C1} allows us to match the input resistance of the CB-CE amplifier pair to the output resistance of a driving circuit. For example, in audio applications, most microphones will have an output resistance of around 10 kΩ. Thus, one way to achieve maximum power transfer between the microphone and the amplifier is to use the common-based input stage as a matching stage, with an input resistance of 10 kΩ.

6.3 The Common-Emitter Common-Base (Cascode) Amplifier

In the previous two compound amplifiers, two separate bias currents are needed, one for each stage. One strategy used to reduce the quiescent DC power of a multi-stage amplifier is to reuse the bias current. This allows multiple transistors to use the same bias current. The most popular example of an amplifier that takes advantage of this *current reuse* strategy is the common-emitter amplifier followed by a common-base amplifier, or otherwise known as a *cascode* pair, and is shown in Fig. 6.4.

The quiescent DC collector current of Q_1 can be expressed as

$$I_{C1} = I_{S1} \cdot e^{\frac{V_{IN}}{V_T}} \tag{6.20}$$

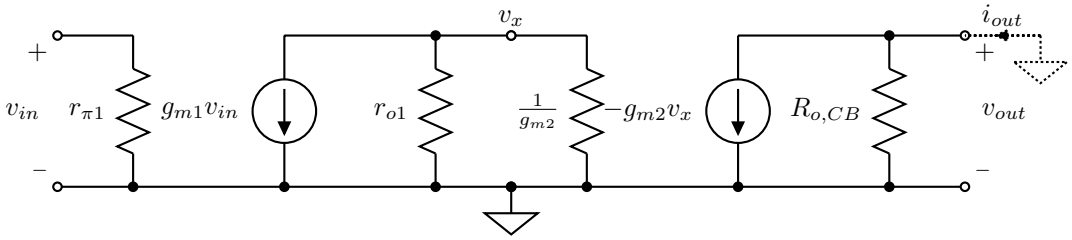


Figure 6.5: The small signal equivalent circuit of the cascode amplifier in Fig. 6.4.

Since Q_2 is in series with Q_1, then $I_{E2} = I_{C1}$, therefore

$$I_{C2} = \alpha_2 I_{E2} = \alpha_2 I_{C1} = \alpha_2 I_{S1} \cdot e^{\frac{V_{IN}}{V_T}} \tag{6.21}$$

In order to ensure that Q_1 is in the forward-active region, let us examine its collector-emitter voltage. We can express V_{CE1} as

$$V_{CE1} = V_{bias} - V_{BE2} = V_{bias} - V_T \ln\left(\frac{\alpha_2 I_{S1} \cdot e^{\frac{V_{IN}}{V_T}}}{I_{S2}}\right) = V_{bias} - V_T \ln\left(\alpha_2 \frac{I_{S1}}{I_{S2}}\right) - V_{IN} > V_{CE1,sat} \tag{6.22}$$

Thus, to ensure that Q_1 is in the forward-active region,

$$V_{bias} > V_{CE1,sat} + V_T \ln\left(\alpha_2 \frac{I_{S1}}{I_{S2}}\right) + V_{IN} \tag{6.23}$$

For Q_2, we can express V_{CE2} as

$$V_{CE2} = V_{CC} - I_{C2} R_L - V_{CE1} > V_{CE2,sat} \tag{6.24}$$

Therefore

$$V_{CC} - \alpha_2 I_{S1} \cdot e^{\frac{V_{IN}}{V_T}} \cdot R_L - V_{bias} + V_T \ln\left(\alpha_2 \frac{I_{S1}}{I_{S2}}\right) + V_{IN} > V_{CE2,sat} \tag{6.25}$$

Note that V_{CE1} and V_{CE2} can be set by (1) the DC input voltage, V_{IN}, (2) the DC bias voltage at the base of Q_2, V_{bias}, and (3) the value of the resistor, R_L.

In order to calculate the overall small signal parameters, we can draw the small signal equivalent circuit as a combination of the equivalent circuits of the CE and CB stages, as shown in Fig. 6.5.

As we have seen before, the common-base amplifier is not unilateral, i.e. its input resistance changes with load conditions. This means that its output resistance will also change if the amplifier driving the common-base amplifier has a finite output resistance[a]. Thus, we will need to solve for the overall two-port parameters in two steps: (1) first obtain the output resistance of the CB amplifier, $R_{o,CB}$, when driven by the CE amplifier, and then (2) calculate the effective transconductance, $G_{m,casc}$, of the CE-CB pair. We can then calculate the overall voltage gain from these two quantities as $A_{v,casc} = -G_{m,casc} \cdot R_{o,CB}$.

To get the output resistance of the CB stage[b], $R_{o,CB}$, let us revisit the common-base small signal model shown in Fig. 6.6, but this time, it is driven by a common-emitter amplifier, modeled as dependent voltage source, $A_{v,CE} \cdot v_{in}$, with an output resistance, $R_{o,CE}$.

Note that zeroing out the input will result in a circuit that is the same as the small signal equivalent circuit of an emitter-degenerated amplifier. Thus, we can express the output resistance of the CB stage driven by a CE stage as

$$R_{o,CB} = R_L \parallel r_{o2}\left(1 + g_{m2} R_{o,CE}\right) = R_{o,casc} \tag{6.26}$$

The overall transconductance can be obtained by shorting the output of the circuit in Fig. 6.5 to ground. Notice that this step is done independent of the output resistance of the CB amplifier since no current will flow through $R_{o,CB}$. By inspection, we can see that the effective transconductance is

$$G_{m,casc} = \frac{i_{out}}{v_{in}} = -g_{m1}\left(r_{o1} \parallel \frac{1}{g_{m2}}\right) \cdot (-g_{m2}) \approx g_{m1} \cdot \frac{g_{m2}}{g_{m2}} = g_{m1} \tag{6.27}$$

[a]The zero input condition is different since even if we zero out the driving source, we will still be left with the driving source's output resistance, and this will affect the output resistance of the common-base amplifier.

[b]Note that the output resistance of the cascode amplifier is equal to the output resistance of the CB stage, as long as it takes into account the fact that the CB stage is being driven by the CE amplifier.

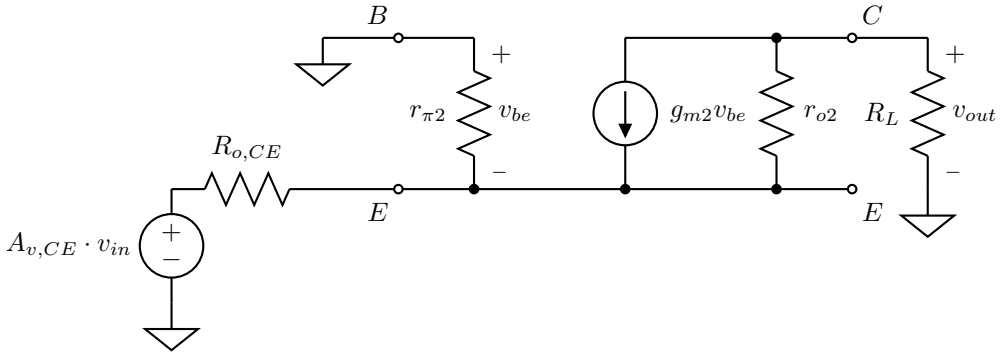
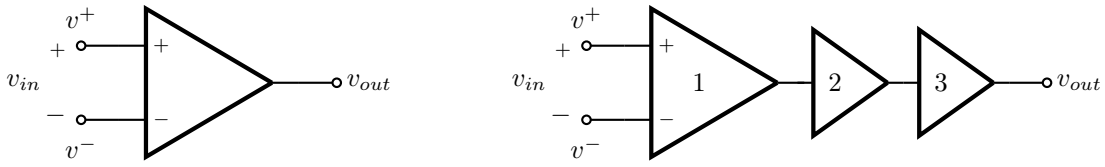


Figure 6.6: The small signal model of the CB amplifier driven by a CE amplifier.



(a) Symbol (b) Components

Figure 6.7: The operational amplifier.

Therefore, the oveall gain of the cascode amplifier is

$$A_{v,casc} = -G_{m,casc}R_{o,casc} = -g_{m1} \cdot (R_L \parallel r_{o2}\,(1 + g_{m2}R_{o,CE})) = -g_{m1} \cdot (R_L \parallel r_{o2}\,(1 + g_{m2}r_{o1})) \tag{6.28}$$

For the case when $R_L \ll r_{o2}$, then $A_{v,casc} \approx -g_{m1} \cdot R_L$. However, if we replace R_L by an ideal current source, i.e. $R_L \to \infty$, the maximum voltage gain we can get out of the cascode is

$$a_{o,casc} \approx -g_{m1}r_{o1}g_{m2}r_{o2} \approx -g_m^2 r_o^2 \tag{6.29}$$

The input resistance is equal to the input resistance of the common-emitter stage, thus

$$R_{i,casc} = r_{\pi 1} \tag{6.30}$$

One very important characteristic of the cascode amplifier is that it can achieve gains in the order of $g_m^2 r_o^2$, similar to the CB-CE amplifier, but with just one current branch. Having only one current branch can potentially lead to lower DC power consumption. However, since there are two transistors in series, the minimum output voltage is increased to support the two saturation voltages, thus reducing the output voltage swing.

6.4 The Operational Amplifier

The operational amplifier is one of the most important building blocks in modern electronic circuit design. Many larger and more complex electronic circuits such as filters, analog-to-digital converters, and motor drives, are based on the premise that we can build these operational amplifiers.

An ideal operational amplifier has (1) differential inputs, (2) single-ended outputs, (3) infinite gain, (4) infinite input resistance, and (5) zero output resistance. The symbol for an operational amplifier is shown in Fig. 6.7a.

We know we can create amplifiers with differential inputs and single-ended outputs, and we can approximate infinite input resistance amplifiers using MOSFET differential pairs, but we cannot really create infinite gain amplifiers, nor can we build zero output resistance amplifiers. However, in most cases, building amplifiers with voltage gains close to 1×10^6 is doable, as well as obtaining output resistances in the mΩ range. To build these types of circuits, we need to use several amplifier stages.

A typical operational amplifier is composed of three main blocks: (1) a differential-to-single-ended amplifier, (2) a gain stage, and (3) an output stage, as shown in Fig. 6.7b. A BJT implementation of an operational amplifier is shown in Fig. 6.8.

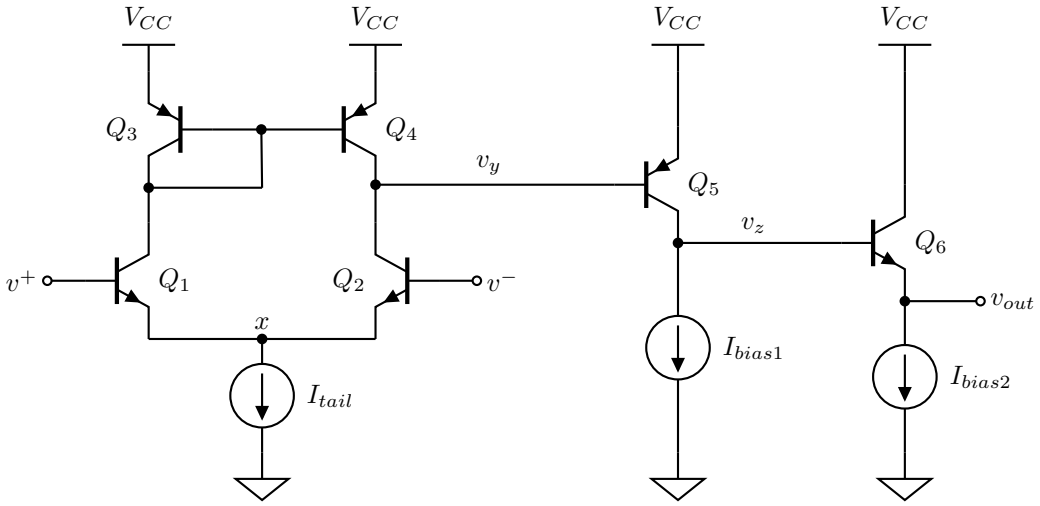


Figure 6.8: A simple BJT operational amplifier.

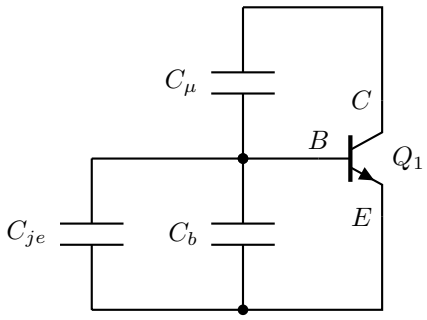


Figure 7.1: BJT parasitic capacitances.

7 Amplifier Frequency Response

In our analysis so far, we have considered only "low-frequency" small signals, or signals with frequencies such that we can ignore all frequency-dependent circuit elements such as capacitors and inductors. As we increase the frequency of the amplifier input signals, the impedances of these frequency-dependent elements can start to dominate, thus changing the amplifier's small signal behavior. In order to determine how capacitances and inductances affect our electronic circuits, we first review the sources of these parasitic[a] elements.

7.1 BJT Parasitic Capacitances

A BJT has two junctions, and each junction has a parasitic capacitance associated with it, as shown in Fig. 7.1. In the forward-active region, the forward-biased base-emitter junction capacitance is dominated by the (1) base-charging capacitance, and (2) the base-emitter junction capacitance. The reversed-bias base-collector capacitance is mostly due to the base-collector junction capacitance.

The *base-charging capacitance*, C_b, models the change in majority carriers in the base due to the change in base-emitter voltage. These majority carriers recombine with the injected minority carriers from the emitter, and the amount of minority charge injected is dependent on V_{BE}. Thus

$$C_b = \frac{\partial Q_b}{\partial V_{BE}} = g_m \tau_F \tag{7.1}$$

where τ_F is the forward base transit time, or the average time needed by a carrier to cross the transistor base region. Typically, C_b is in the hundreds of femtofarads.

The *base-emitter junction capacitance*, C_{je} represents the change in diffusion charge of the forward-biased base-emitter junction as V_{BE} is varied. Being a junction capacitance, C_{je} is nonlinear, and if we assume that the base-emitter junction is a step junction, C_{je} can be expressed as

$$C_{je} = \frac{\partial Q_{BE}}{\partial V_{BE}} = \frac{C_{je0}}{\sqrt{1 - \frac{V_{BE}}{V_{j,BE}}}} \tag{7.2}$$

where C_{je0} is the capacitance when $V_{BE} = 0$, and $V_{j,BE}$ is the built-in potential of the base-emitter junction. For $V_{BE} \approx V_{j,BE}$, $C_{je} \approx 2 \cdot C_{je0}$, and with typical values in the tens of femtofarads.

The base-collector junction capacitance, C_μ, represents the depletion capacitance of the reverse-biased collector-base junction, and for a step junction, we get

$$C_\mu = \frac{\partial Q_{CB}}{\partial V_{CB}} = \frac{C_{\mu 0}}{\sqrt{1 + \frac{V_{CB}}{V_{j,CB}}}} \tag{7.3}$$

where $C_{\mu 0}$ is the capacitance when $V_{CB} = 0$ and$V_{j,CB}$ is the built-in potential of the collector-base junction. Typically, C_μ is less than 10 fF. However due to the *Miller effect*[b], this capacitance can seem bigger to circuits driving the transistor.

Note that these small signal capacitances are dependent on the quiescent DC operating point of the transistor. Thus, the small signal equivalent circuit of the BJT, including these capacitances, is shown in Fig. 7.2, where $C_\pi = C_b + C_{je}$.

[a] These elements are called *parasitic* since they are not built on purpose, but exist only as artifacts due to (1) the fundamental structure of the device and (2) how the device is built.

[b] This is something we will discuss in detail later in this handout.

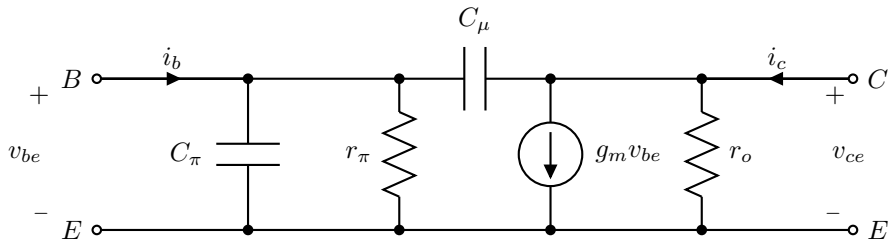


Figure 7.2: The BJT small signal equivalent circuit including the small signal capacitances.

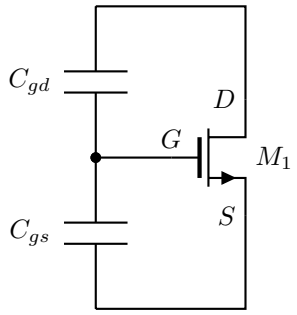


Figure 7.3: MOSFET parasitic capacitances.

7.2 MOSFET Parasitic Capacitances

In planar MOSFETs, the main parasitic capacitances are the gate-to-source capacitance, C_{gs}, and the gate-to-drain capacitace, C_{gd}.

Gate-to-drain capacitance can be considered linear, and dependent on the dimensions of the transistor...

Gate-to-source capacitance is nonlinear, MOS capacitor, but in EEE 51, the MOSFET will almost always be, by design, in the super-threshold, saturation region... thus, in most cases, we can express C_{gs} as

$$C_{gs} \approx \frac{2}{3} \cdot C_{ox} \cdot W \cdot L \tag{7.4}$$

The small signal equivalent circuit of the MOSFET, including the parasitic capacitances, is shown in Fig. 7.4.

7.3 Frequency Response of Resistor-Capacitor Circuits

Consider a simple RC circuit, shown in Fig. 7.5a. Solving for the output voltage in the Fourier domain, we get

$$v_o(\omega) = v_i(\omega) \cdot \frac{Z_C}{R + Z_C} = v_i(\omega) \cdot \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} = v_i(\omega) \cdot \frac{1}{1 + j\omega RC} = v_i(\omega) \cdot \frac{1}{1 + j\frac{\omega}{\omega_o}} = A_v \cdot v_i(\omega) \tag{7.5}$$

Thus, the voltage gain becomes

$$A_v(\omega) = \frac{v_o}{v_i}(\omega) = \frac{1}{1 + j\frac{\omega}{\omega_o}} \tag{7.6}$$

where $\omega_o = \frac{1}{RC}$.

Note that A_v is a complex number, and therefore we need two components to fully specify it. Therefore, A_v can be represented by either its real and imaginary components, $\Re(A_v)$ and $\Im(A_v)$, or its magnitude and phase, $|A_v|$ and

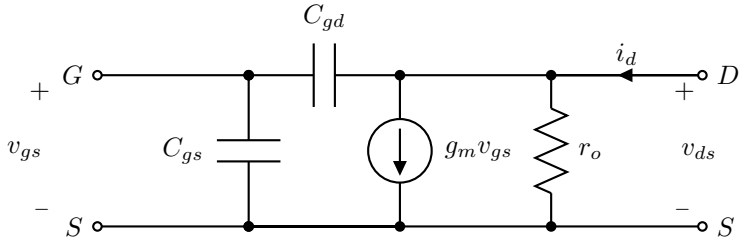
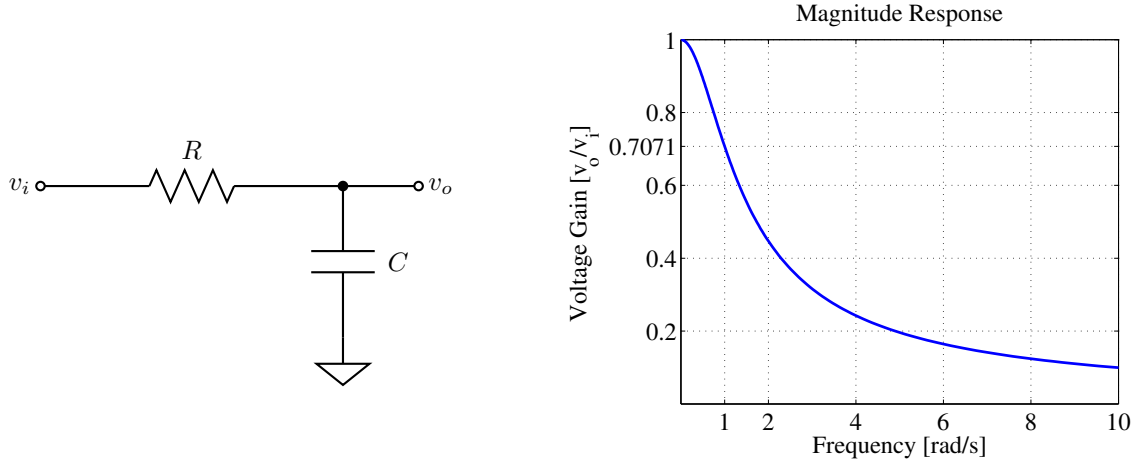


Figure 7.4: The MOSFET small signal equivalent circuit including the small signal capacitances.



(a) Schematic (b) Magnitude response

Figure 7.5: A simple RC circuit example with $R = 1\,\Omega$ and $C = 1\,\text{F}$.

$\angle A_v$, thus

$$A_v = \Re\left(A_v\right) + j \cdot \Im\left(A_v\right) = \left|A_v\right| \cdot e^{j \cdot \angle A_v} \tag{7.7}$$

where

$$\left|A_v\right| = \sqrt{A_v \cdot A_v^*} = \sqrt{\left(\Re\left(A_v\right) + j \cdot \Im\left(A_v\right)\right) \cdot \left(\Re\left(A_v\right) - j \cdot \Im\left(A_v\right)\right)} = \sqrt{\Re\left(A_v\right)^2 + \Im\left(A_v\right)^2} \tag{7.8}$$

and

$$\angle A_v = \tan^{-1} \frac{\Im\left(A_v\right)}{\Re\left(A_v\right)} \tag{7.9}$$

If we assume that the inputs are purely sinusoidal signals, then we can represent these inputs as phasors, with both magnitude and phase,

$$\left|v_o\right| \cdot e^{j \cdot \angle v_o} = \left|A_v\right| \cdot e^{j \cdot \angle A_v} \cdot \left|v_i\right| \cdot e^{j \cdot \angle v_i} = \left|A_v\right| \cdot \left|v_i\right| \cdot e^{j \cdot \left(\angle A_v + \angle v_i\right)} \tag{7.10}$$

Thus, in the time domain, for $v_i\left(t\right) = V_i \cdot \sin\left(\omega t\right)$, the general form of the output is

$$v_o\left(t\right) = V_o \cdot \sin\left(\omega t + \phi\right) \tag{7.11}$$

Therefore, in order to get the complete time domain response for a purely sinusoidal input, we need to determine V_o and ϕ. Recall that in linear circuits, the output frequency will always be the same as the input frequency.

7.3.1 Magnitude Response

The magnitude of A_v can be expressed as

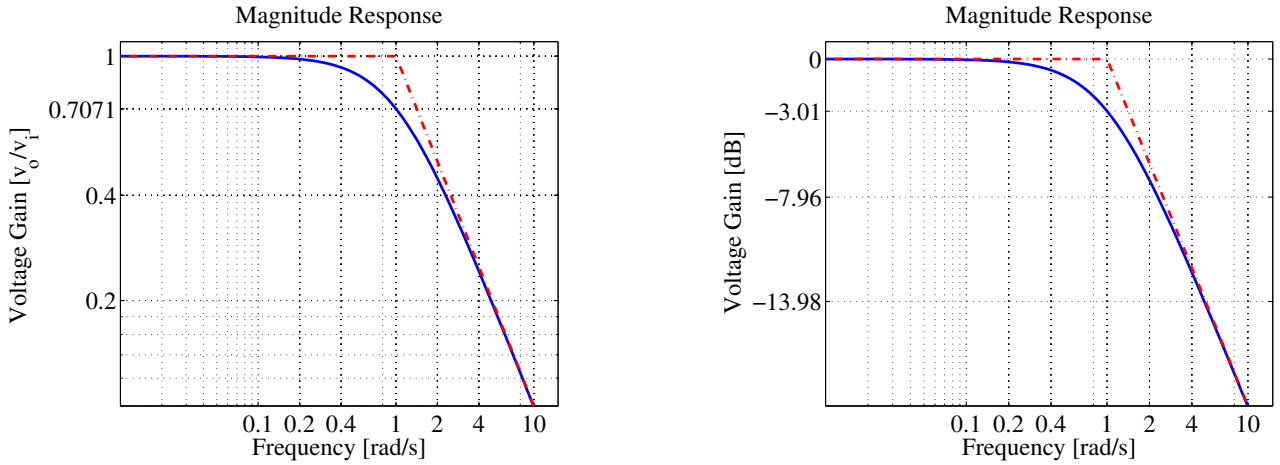
$$\left|A_v\left(\omega\right)\right| = \sqrt{A_v\left(\omega\right) \cdot A_v^*\left(\omega\right)} = \sqrt{\frac{1}{1 + j\frac{\omega}{\omega_o}} \cdot \frac{1}{1 - j\frac{\omega}{\omega_o}}} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_o}\right)^2}} \tag{7.12}$$

and is plotted in Fig. 7.5b as a function of the frequency ω.

Eq. 7.12 describes the behavior of the voltage gain when a sinusoid voltage, with frequency[c] ω, is applied at the input of the simple RC circuit in Fig. 7.5a. As expected, at DC (when $\omega = 0$), the output voltage is equal to the input voltage, since the capacitor acts like an open circuit. The voltage gain drops as the frequency of the input sinusoid increases. This is due to the decrease in the capacitor impedance, $Z_C = \frac{1}{j\omega C}$, reducing the output voltage. At very high frequencies (when $\omega \to \infty$), the capacitor starts behaving like a short circuit, or $Z_C \to 0$, thus, the output voltage also approaches zero.

The frequency ω_o represents the boundary between these two cases. When $\omega \ll \omega_o$, Eq. 7.12 becomes $\left|A_v\left(\omega\right)\right| \approx 1$. On the other hand, when $\omega \gg \omega_o$, $\left|A_v\left(\omega\right)\right| \approx \frac{\omega_o}{\omega}$. Thus, in this case, ω_o is called the *bandwidth* or *corner frequency*.

[c] In calculations, we use radians per second instead of Hertz, but in plots, the x-axis can either be in radians per second or Hertz. Note that $1\,\frac{\text{rad}}{\text{s}} = 2\pi\,\text{Hz}$.



(a) Magnitude (b) Log-magnitude

Figure 7.6: Logarithmic frequency response plots.

Below this frequency, $Z_C \gg R$, and by voltage division, the output voltage is approximately equal to the input voltage. At frequencies above ω_o, $Z_C \ll R$, resulting in an output voltage that is inversely proportional to the input frequency.

At exactly ω_o, we get

$$|A_v(\omega_o)| = \left|\frac{v_o}{v_i}(\omega_o)\right| = \frac{1}{\sqrt{2}} \tag{7.13}$$

Recall that power is proportional to the square of the voltage. Thus, if we assume that the input and output voltages are impressed on the same resistance, we can define the power gain as

$$P_v(\omega_o) = \left|\frac{v_o^2}{v_i^2}(\omega_o)\right| = \frac{1}{2} \tag{7.14}$$

Thus, ω_o is also called the *half-power point frequency*.

The magnitude response plot in Fig. 7.5b is relatively hard to interpret when looking at a broad range of (1) frequencies, ranging from a few radians per second, to billions of radians per second, and (2) gains ranging from very small fractions to millions. These are the ranges which we normally consider when designing amplifiers. Thus, the magnitude frequency response behavior is typically plotted on a *logarithmic* scale.

Redrawing Fig. 7.5b using logarithmic frequency and gain axes, we get Fig. 7.6a. Note that in a logarithmic axis, we usually measure distances in factors of 10, or in *decades*. Thus, the $10\,\frac{\text{rad}}{\text{s}}$ point is a decade above from the $1\,\frac{\text{rad}}{\text{s}}$ point, which is also a decade above from the $0.1\,\frac{\text{rad}}{\text{s}}$ point. Also notice that the $0.2\,\frac{\text{rad}}{\text{s}}$ point is also a decade below from the $2\,\frac{\text{rad}}{\text{s}}$ point. Another measure of distance in a logarithmic axis is in factors of 2, or in *octaves*. Thus, the $1\,\frac{\text{rad}}{\text{s}}$ point is an octave below the $2\,\frac{\text{rad}}{\text{s}}$ point, which is an octave below the $4\,\frac{\text{rad}}{\text{s}}$ point.

Two important characteristics of logarithmic plots... 1) exponential functions appear as straight lines, therefore easy to approximate... 2) products appear as sums... multiple poles and zeros... their behavior is additive!

Thus, for $v_i(t) = V_i \cdot \sin(\omega t)$,

$$|v_o(\omega)| = V_o = |A_v(\omega)| \cdot |v_i(\omega)| = |A_v(\omega)| \cdot V_i \tag{7.15}$$

The dB scale...

Note that

$$20 \cdot \log(|A_v(\omega_o)|) = 20 \cdot \log\left(\frac{1}{\sqrt{2}}\right) \approx -3\,\text{dB} \tag{7.16}$$

Thus, ω_o is also called the $-3\,\text{dB}$ *frequency*.

7.3.2 Phase Response

Aside from the magnitude response, phase response describes the shift in a sinusoid at the output relative to the input...

$$\angle A_v(\omega) = \tan^{-1}\frac{\Im(A_v(\omega))}{\Re(A_v(\omega))} = \tan^{-1}\left(\frac{0}{1}\right) - \tan^{-1}\left(\frac{\omega}{\omega_o}\right) = -\tan^{-1}\left(\frac{\omega}{\omega_o}\right) \tag{7.17}$$

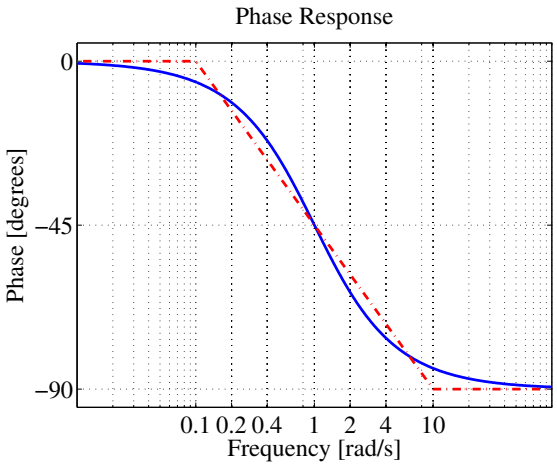


Figure 7.7: Phase response plot.

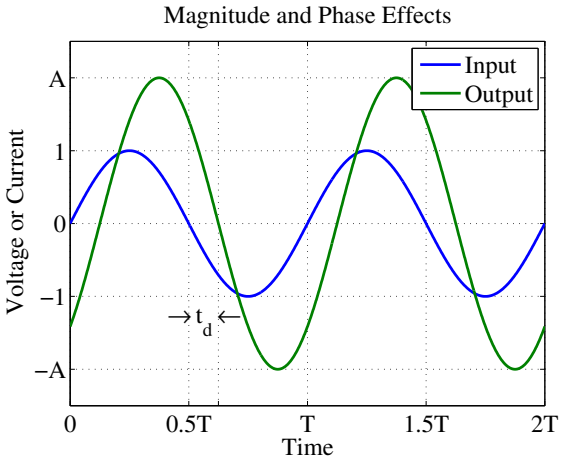


Figure 7.8: Magnitude and phase effects on an input sinusoid.

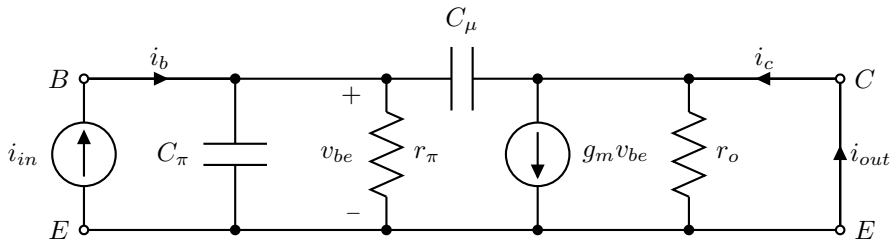


Figure 7.9: Small signal equivalent circuit for calculating f_T.

7.4 Poles and Zeros

In the Laplace domain, any transfer function, like the ratio of input and output voltages of a two-port network, can be expressed as

$$A(s) = A_0 \cdot \frac{\left(1+\frac{s}{z_1}\right)\cdot\left(1+\frac{s}{z_2}\right)\cdots\left(1+\frac{s}{z_m}\right)}{\left(1+\frac{s}{p_1}\right)\cdot\left(1+\frac{s}{p_2}\right)\cdots\left(1+\frac{s}{p_n}\right)} \tag{7.18}$$

where A_0 is the DC value, or the value of $A(s)$ when $s = 0$, and z_i and p_j are the poles and zeros of $A(s)$. Recall that z_i is a zero if $A(s = -z_i) = 0$. Similarly, p_j is a pole if $A(s = -p_j) \to \infty$.

Laplace vs. Fourier... more information in s... Fourier only takes the complex part of s...

7.4.1 Pole Frequency Response

Consider the simple RC circuit in Fig. 7.5a. Writing out the voltage gain in the Laplace domain gives us

$$A_v(s) = \frac{v_o}{v_i}(s) = \frac{1}{1 + s \cdot RC} \tag{7.19}$$

By inspection, we can see we have a real pole, $p = -\frac{1}{RC}$. In the complex s-plane, we can plot $A_v(s)$ as a surface, as shown in Fig. , where $\sigma = \Re(s)$ and $\omega = \Im(s)$, such that $s = \sigma + j\omega$.

7.4.2 Zero Frequency Response

7.5 The Transistor Transition Frequency

One metric we can use to compare the behavior of transistors as input frequency is increased, is the transistor's transition frequency, f_T. Transition frequency is defined as the frequency at which the short-circuit common-emitter or common-source current gain falls to unity.

Thus, for a BJT, using the circuit in Fig. 7.9, and noting that at very high frequencies, the impedance of the capacitors, in the Laplace domain, will be very much less than r_π, we can express v_{be} as

$$v_{be} = i_{in} \cdot \left(\frac{1}{sC_\pi} \parallel \frac{1}{sC_\mu} \parallel r_\pi\right) \approx i_{in}\left(\frac{1}{sC_\pi} \parallel \frac{1}{sC_\mu}\right) = \frac{i_{in}}{s(C_\pi + C_\mu)} \tag{7.20}$$

Also, if we assume that the output short-circuit current, i_{out} is mainly due to the transconductance, we get

$$i_{out} = g_m v_{be} = g_m \cdot \frac{i_{in}}{s(C_\pi + C_\mu)} \tag{7.21}$$

Therefore, at $s = j\omega$ and $\omega_T = 2\pi f_T$, and using the definition of the transition frquency, we get

$$\left|\frac{i_{out}}{i_{in}}\right| = 1 = \left|\frac{g_m}{j\omega_T(C_\pi + C_\mu)}\right| \tag{7.22}$$

In typical bipolar junction transistors, $C_\pi \gg C_\mu$. Thus, we get

$$\omega_T = \frac{g_m}{C_\pi + C_\mu} \approx \frac{g_m}{C_\pi} \tag{7.23}$$

For MOSFETs, the analysis is exactly the same, and we get a transition frequency equal to

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}} \approx \frac{g_m}{C_{gs}} \tag{7.24}$$

7.6 Frequency Response of Linear Amplifiers

Consider a common-emitter amplifier biased using a resistor, R_C, and driving a capacitive load, C_L, shown in Fig. ... small signal model including the BJT parasitic capacitances...

The small signal voltage gain...

7.7 Frequency Response of Differential Circuits

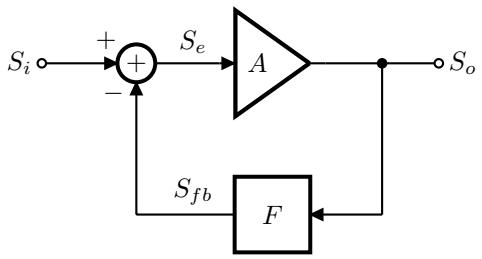


Figure 8.1: The components of a negative feedback amplifier.

8 Feedback Amplifiers

So far, we have studied the "open-loop" behavior of electronic amplifiers. This means that the amplifier output is solely determined by the amplifier input signal, independent of the state of its output. As we have seen, the small signal parameters of these open-loop amplifiers are very dependent on circuit parameters such as β, V_A, or V_{TH}, making it is very hard to get accurate and stable amplifier parameters, such as voltage gain. One way to avoid this problem is to use negative feedback techniques to create "closed-loop" amplifiers, or simply feedback amplifiers.

8.1 Feedback Basics

Consider the block diagram of a basic negative feedback amplifier, in Fig. 8.1, showing the three main components of a feedback network: (1) a forward gain, A, (2) a feedback circuit, with gain F, and (3) a mechanism that can perform subtraction. We represent the signals in Fig. 8.1 using the variable S, since in general, feedback systems and circuits can work with voltages, currents, charge, etc.

The *forward gain*, A is provided by an amplifier, amplifying the *error signal*, S_e. Thus,

$$S_o = A \cdot S_e \tag{8.1}$$

The output, S_o, is then sampled by the feedback circuit, which generates the *feedback signal*, S_{fb}, which is given by

$$S_{fb} = F \cdot S_o \tag{8.2}$$

where F is called the feedback factor. The error signal, S_e, is the difference between the input signal, S_i, and the feedback signal, S_{fb}, and can then be written as

$$S_e = S_i - S_{fb} \tag{8.3}$$

By plugging in Eqs. 8.1 and 8.2 into Eq. 8.3, we get

$$\frac{S_o}{A} = S_i - F \cdot S_o \tag{8.4}$$

We can then compute for the *closed-loop gain*, A_{CL}, as

$$A_{CL} = \frac{S_o}{S_i} = \frac{A}{1 + AF} \tag{8.5}$$

which is the familiar closed-loop gain of a feedback system. We can define the *loop gain*, T, as

$$T = AF \tag{8.6}$$

Thus, the closed-loop gain can be expressed as

$$A_{CL} = \frac{S_o}{S_i} = \frac{1}{F} \cdot \frac{AF}{1 + AF} = \frac{1}{F} \cdot \frac{T}{1 + T} = \frac{1}{F} \cdot \frac{1}{1 + \frac{1}{T}} \tag{8.7}$$

One very interesting consequence of using feedback is that if the forward gain, A, is very large, that is, if $A \to \infty$, then $T \to \infty$, thus

$$A_{CL}|_{A \to \infty} = \frac{1}{F} \tag{8.8}$$

This means that if $A \to \infty$, then closed-loop gain is only dependent on the feedback factor, F. In most applications, the feedback circuit is built using passive devices such as resistors. Therefore, we can create amplifiers whose gain is only dependent on resistor values, and not on transistor parameters!

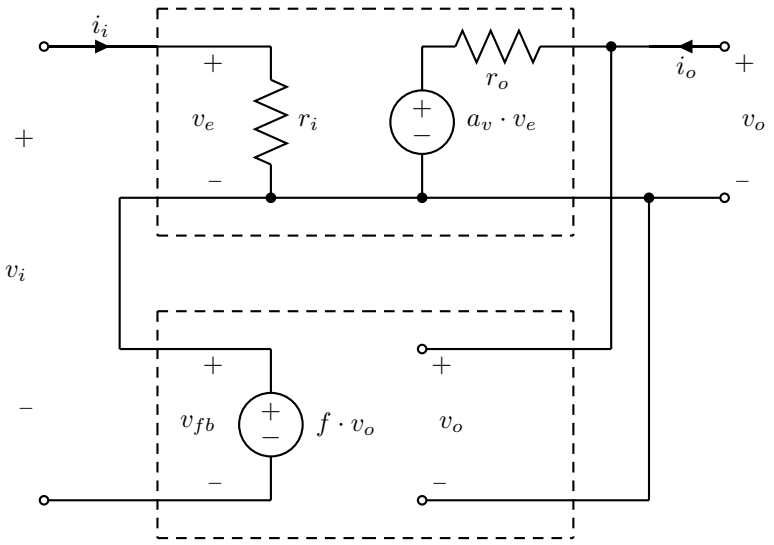


Figure 8.2: The ideal series-shunt feedback amplifier small signal equivalent circuit.

Since we cannot really build amplifiers with infinite gain, we want to quantify the effect of this finite forward gain on the closed-loop gain. For finite A, we can calculate the closed-loop gain as

$$A_{CL} = \frac{1}{F} \cdot \frac{1}{1+\frac{1}{T}} = \frac{1}{F} \cdot \left(1 - \frac{1}{T} + \frac{1}{T^2} - \frac{1}{T^3} + \ldots\right) \approx \frac{1}{F} \cdot \left(1 - \frac{1}{T}\right) = \frac{1}{F} \cdot (1-\epsilon) \tag{8.9}$$

If we have finite forward gain, our loop gain will also be finite, and the closed-loop gain will once again be dependent on the forward gain, and hence the transistor parameters. Thus, the lower the forward gain, A, the larger the closed-loop gain's deviation from $\frac{1}{F}$. This deviation from the ideal closed-loop gain is normally written as the error term ϵ. Note that as we make the forward gain, A, larger, the error term becomes smaller, and the closed-loop gain approaches $\frac{1}{F}$.

Another important result of using feedback in amplifiers is the reduced sensitivity of the closed-loop gain, A_{CL}, on the forward gain, A. Calculating the sensitivity of A_{CL} to A, we get

$$S_A^{A_{CL}} = \frac{\partial A_{CL}}{\partial A} = \frac{(1+AF) - AF}{(1+AF)^2} = \frac{1}{(1+AF)^2} = \frac{1}{(1+T)^2} \tag{8.10}$$

Thus, as we increase the forward gain, A, the closed-loop gain, A_{CL}, becomes less sensitive to variations in A.

8.2 Feedback Amplifier Topologies

In the context of feedback amplifiers, the signals, S, in Fig. 8.1, can be a voltage or a current. One way to classify feedback amplifiers is by grouping them according to what quantity is sampled at the output, and what is being compared by the subtraction mechanism.

8.2.1 The Ideal Series-Shunt Feedback Amplifier

A feedback amplifier that compares or subtracts voltages, and uses a voltage signal as input to its feedback network, is called a *series-shunt* feedback amplifier. The small signal equivalent circuit of an ideal series-shunt amplifier is shown in Fig. 8.2.

The feedback amplifier is composed of the (1) forward amplifier, with gain a_v, input resistance r_i, and output resistance r_o, and (2) the ideal feedback network, with feedback factor f. The forward gain is then

$$A_v = \frac{v_o}{v_e} = a_v \tag{8.11}$$

and the feedback factor, F, is

$$F = \frac{v_{fb}}{v_o} = \frac{f \cdot v_o}{v_o} = f \tag{8.12}$$

The loop gain, T, becomes

$$T = A_v \cdot F = a_v \cdot f \tag{8.13}$$

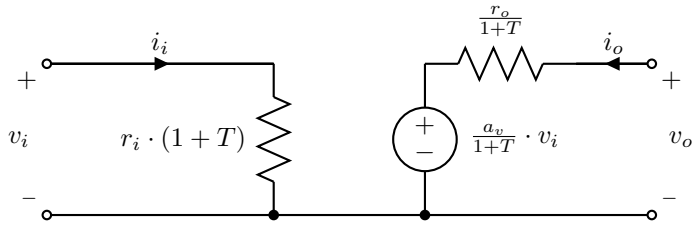


Figure 8.3: The small signal equivalent circuit of the series-shunt amplifier in Fig. 8.2.

The feedback network samples the output voltage, v_o, and the output of the feedback network, v_{fb}, is subtracted from the input voltage, v_i. Thus, the error voltage, v_e can be expressed as

$$v_e = \frac{v_o}{a_v} = v_i - v_{fb} = v_i - f \cdot v_o \tag{8.14}$$

Solving for the closed-loop gain, A_{CL}, we get

$$A_{CL} = \frac{v_o}{v_i} = \frac{a_v}{1 + a_v \cdot f} = \frac{a_v}{1+T} = \frac{1}{f} \cdot \frac{T}{1+T} \tag{8.15}$$

Note that the closed-loop gain is reduced by a factor equal to $(1+T)$ relative to the forward amplifier gain. Why would we want lower gains? In order to answer this, let us now examine the other two-port parameters of the feedback amplifier.

In order to calculate the input resistance, we set the output at no-load and apply a test voltage at the input. Since the output is a voltage, the no-load condition is an open circuit, that is, when $i_o = 0$. Thus, the input current, i_i, can be expressed as

$$i_i = \frac{v_e}{r_i} = \frac{v_i - f \cdot v_o}{r_i} = \frac{v_i - f \cdot \frac{1}{f} \cdot \frac{T}{1+T} \cdot v_i}{r_i} = \frac{v_i}{r_i \cdot (1+T)} \tag{8.16}$$

Thus, the input resistance can be calculated as

$$R_i = \frac{v_i}{i_i} = r_i \cdot (1+T) \tag{8.17}$$

Note that the input resistance of the closed-loop (feedback) amplifier is larger than the input resistance of the forward amplifier by a factor of $(1+T)$. If we assume that the closed-loop amplifier is driven by a voltage source, then a larger input resistance would reduce the voltage degradation, due to loading, at the input of the closed-loop amplifier.

Similarly, the output resistance can found by setting the input voltage source to zero, and applying a test voltage at the output. We can then express the output current, i_o, as

$$i_o = \frac{v_o - a_v \cdot v_e}{r_o} = \frac{v_o - a_v \cdot (-f \cdot v_o)}{r_o} = \frac{v_o \cdot (1 + a_v \cdot f)}{r_o} = v_o \cdot \frac{1+T}{r_o} \tag{8.18}$$

Therefore, the output resistance is

$$R_o = \frac{v_o}{i_o} = \frac{r_o}{1+T} \tag{8.19}$$

This closed-loop output resistance is smaller than the outptu resistance of the forward amplifier by a factor of $(1+T)$. Note that if the output is a voltage, then lowering the output resistance will allow the closed-loop amplifier to drive smaller resistive loads, due to less loading effects.

The small signal equivalent circuit of the closed-loop amplifier is shown in Fig. 8.3. We can now see that by using feedback, we can reduce the voltage gain of the closed-loop amplifier, but in exchange, we get better input and output resistances.

8.2.2 The Ideal Shunt-Shunt Feedback Amplifier

A feedback amplifier that compares or subtracts currents, and uses a voltage signal as input to its feedback network, is called a *shunt-shunt* feedback amplifier. The small signal equivalent circuit of an ideal shunt-shunt amplifier is shown in Fig. 8.4.

Once again, the feedback amplifier is composed of the (1) forward amplifier, with gain a_v, input resistance r_i, and output resistance r_o, and (2) the ideal feedback network, with feedback factor f. Since the input to the forward amplifier is a current, and the output is a voltage, the forward amplifier can be thought of as a *transresistance* amplifier. The forward gain is then equal to

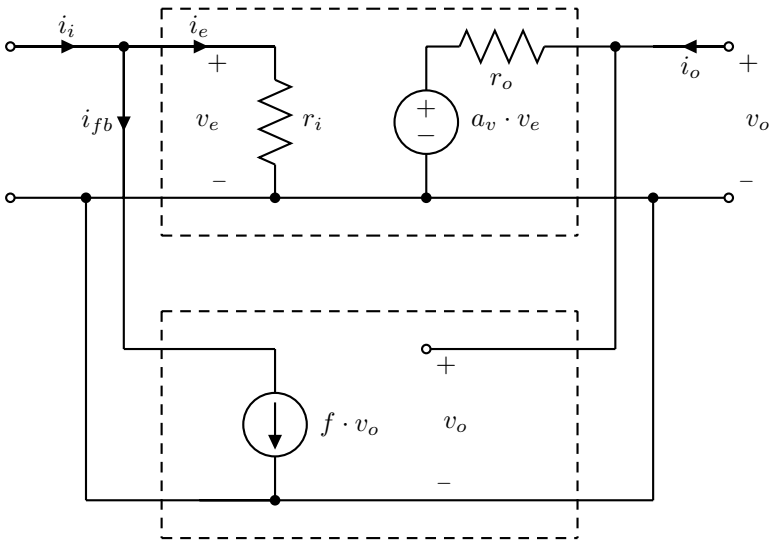


Figure 8.4: The ideal shunt-shunt feedback amplifier small signal equivalent circuit.

$$R_m = \frac{v_o}{i_e} = a_v \cdot r_i \tag{8.20}$$

and the feedback factor, F, is

$$F = \frac{i_{fb}}{v_o} = \frac{f \cdot v_o}{v_o} = f \tag{8.21}$$

The loop gain, T, can be expressed as

$$T = R_m \cdot F = a_v \cdot r_i \cdot f \tag{8.22}$$

It is very important to note that the loop gain, T, is unit-less. This a convenient way to check if your analysis is correct.

The output voltage can be expressed as

$$v_o = a_v \cdot r_i \cdot (i_i - i_{fb}) = a_v \cdot r_i \cdot (i_i - f \cdot v_o) \tag{8.23}$$

Thus, the closed-loop gain is

$$R_{CL} = \frac{v_o}{i_i} = \frac{a_v \cdot r_i}{1 + a_v \cdot r_i \cdot f} = \frac{R_m}{1+T} = \frac{1}{f} \cdot \frac{T}{1+T} \tag{8.24}$$

Once again, we see that the forward gain is reduced by a factor of $(1 + T)$ when the forward amplifier is placed in feedback.

The closed-loop input resistance can be found by applying an input current and calculating the input voltage. The output current is set to zero (an open circuit) to satisfy the no-load condition. The input voltage is then

$$v_i = i_e \cdot r_i = (i_i - f \cdot v_o) \cdot r_i = \left(i_i - f \cdot \frac{a_v \cdot r_i}{1+T} \cdot i_i \right) \cdot r_i \tag{8.25}$$

Thus, the closed-loop input resistance can be expressed as

$$R_i = \frac{r_i}{1+T} \tag{8.26}$$

Note that the input resistance is now smaller than the open-loop input resistance by a factor of $(1 + T)$. For current-input amplifiers, this is a big improvement since it reduces the degradation due to loading when being driven by a current source with finite output resistance.

The closed-loop output resistance can be found using the procedure applies to the series-shunt amplifier. However, since the input is a current, zero-input means an open-circuited input. Applying a test voltage, v_o, at the output results in an output current equal to

$$i_o = \frac{v_o - a_v \cdot v_e}{r_o} = \frac{v_o - a_v \cdot r_i \cdot (-f \cdot v_o)}{r_o} = v_o \frac{1+T}{r_o} \tag{8.27}$$

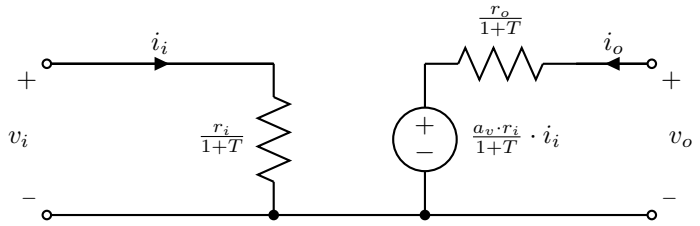


Figure 8.5: The small signal equivalent circuit of the shunt-shunt amplifier in Fig. 8.4.

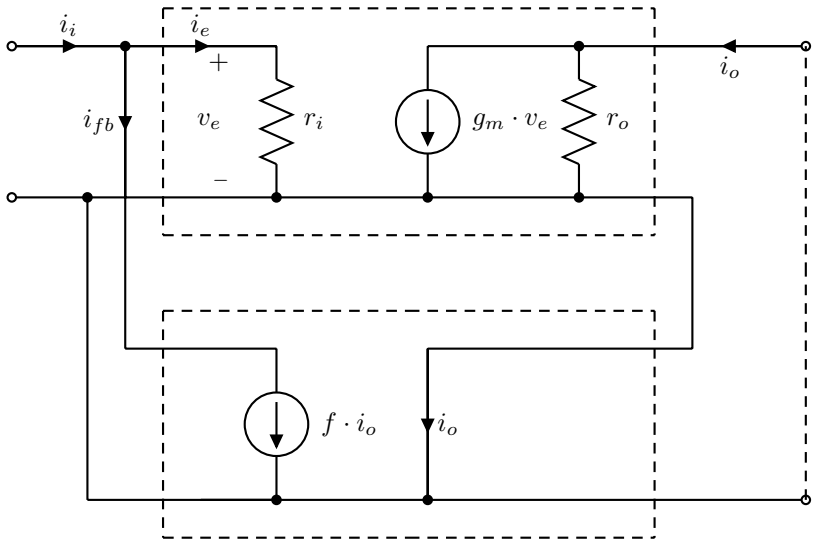


Figure 8.6: The ideal shunt-series feedback amplifier small signal equivalent circuit.

Hence, the output resistance of the closed-loop amplifier is equal to

$$R_o = \frac{r_o}{1+T} \tag{8.28}$$

Again, we see that feedback reduces the output resistance of a voltage-output amplifier, resulting in less degradation when driving resistive loads. The small signal equivalent circuit of the closed-loop amplifier is shown in Fig. 8.5.

8.2.3 The Ideal Shunt-Series Feedback Amplifier

A feedback amplifier that compares or subtracts currents, and samples an output current, which is then used as input to its feedback network, is called a *shunt-series* feedback amplifier. The small signal equivalent circuit of an ideal shunt-shunt amplifier is shown in Fig. 8.6

The forward current gain, A_i, is equal to

$$A_i = \frac{i_o}{i_e} = g_m \cdot r_i \tag{8.29}$$

and the feedback factor is

$$F = \frac{i_{fb}}{i_o} = \frac{f \cdot i_o}{i_o} = f \tag{8.30}$$

Therefore the loop gain, T, can be expressed as

$$T = A_i \cdot F = g_m \cdot r_i \cdot f \tag{8.31}$$

The output current can be expressed as

$$i_o = g_m \cdot r_i \cdot (i_i - f \cdot i_o) \tag{8.32}$$

leading to a closed-loop current gain that is equal to

$$A_{CL} = \frac{i_o}{i_i} = \frac{g_m \cdot r_i}{1 + g_m \cdot r_i \cdot f} = \frac{A_i}{1+T} = \frac{1}{f} \cdot \frac{T}{1+T} \tag{8.33}$$

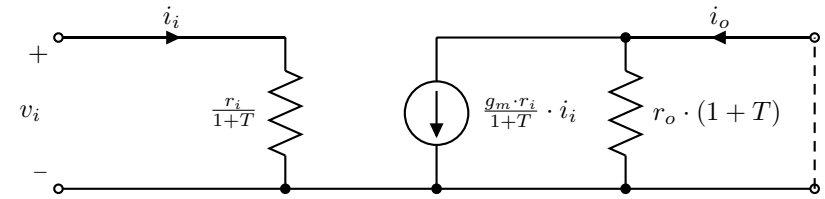


Figure 8.7: The small signal equivalent circuit of the shunt-series amplifier in Fig. 8.6.

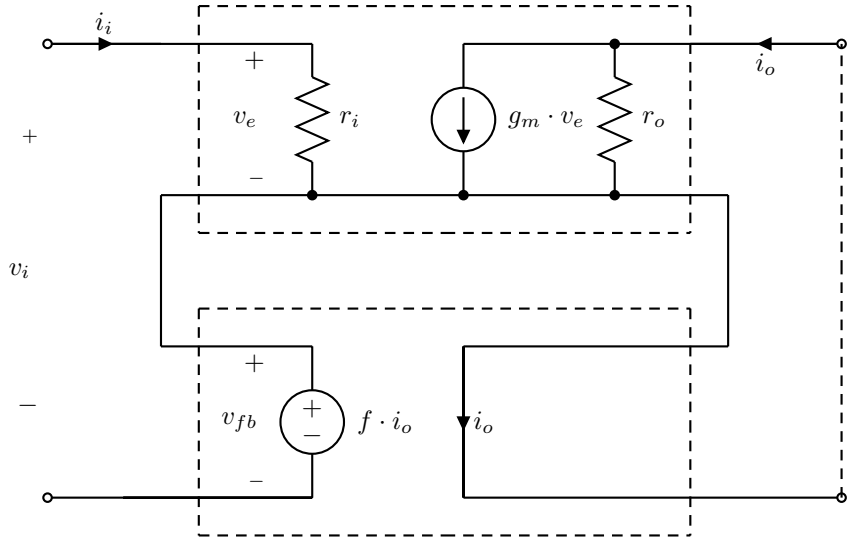


Figure 8.8: The ideal series-series feedback amplifier small signal equivalent circuit.

Once again, we see that the forward gain is reduced by a factor of $(1+T)$ when the forward amplifier is placed in feedback.

The closed-loop input resistance can be found by applying an input current, i_i, and calculating the input voltage, v_i. The output voltage is set to zero, the no-load condition of the current output amplifier. The output voltage is then equal to

$$v_i = i_e \cdot r_i = (i_i - f \cdot i_o) \cdot r_i = \left(i_i - f \cdot \frac{g_m \cdot r_i}{1+T}\right) \cdot r_i = i_i \cdot \frac{r_i}{1+T} \tag{8.34}$$

Thus, the closed-loop input resistance can be expressed as

$$R_i = \frac{r_i}{1+T} \tag{8.35}$$

Note that the input resistance is reduced by a factor of $(1+T)$, again, an improvement for current-input amplifiers.

8.2.4 The Ideal Series-Series Feedback Amplifier

A feedback amplifier that compares or subtracts voltages, and samples an output current, which is then used as input to its feedback network, is called a *series-series* feedback amplifier. The small signal equivalent circuit of an ideal shunt-shunt amplifier is shown in Fig. 8.8

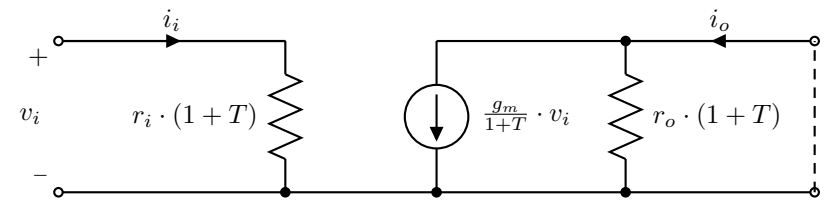


Figure 8.9: The small signal equivalent circuit of the series-series amplifier in Fig. 8.8.

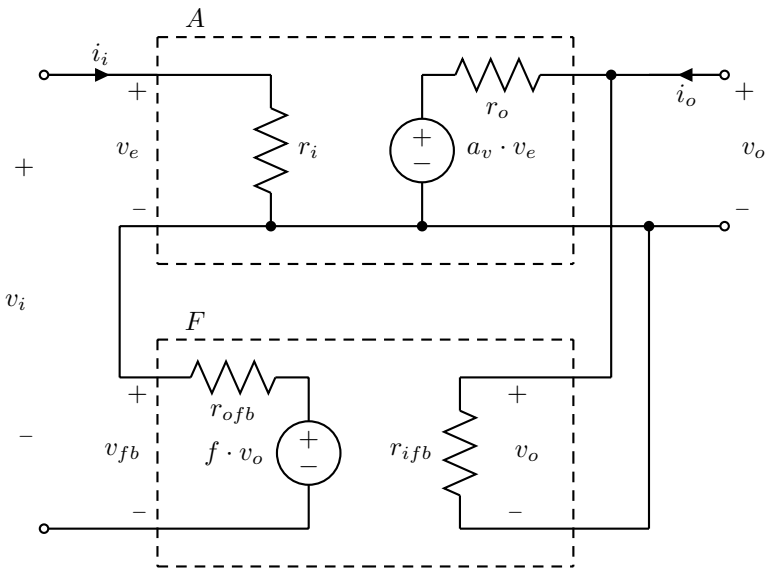


Figure 8.10: The series-shunt feedback amplifier small signal equivalent circuit with a non-ideal feedback network.

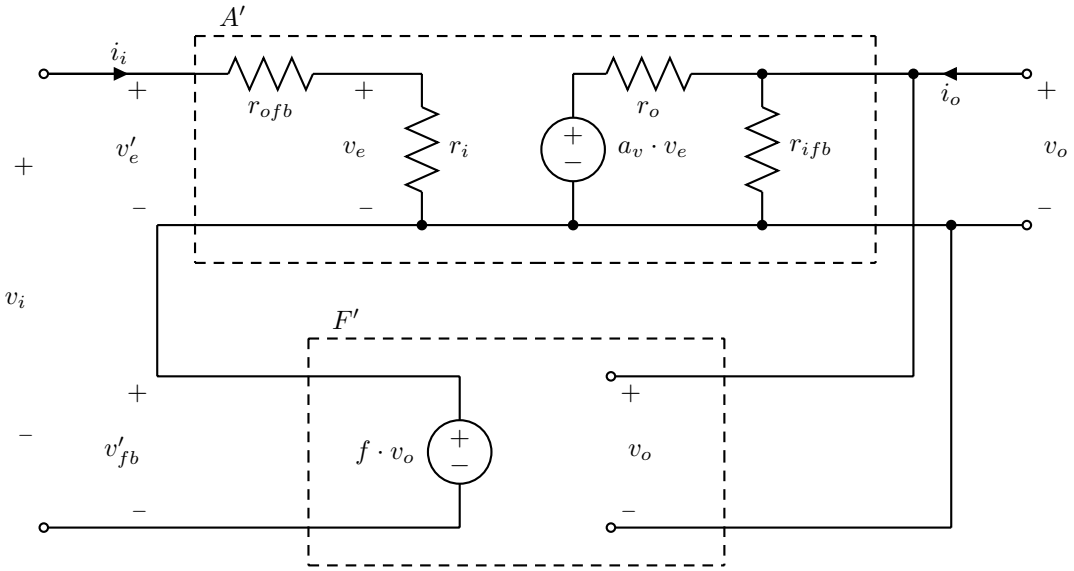


Figure 8.11: The redrawn series-shunt feedback amplifier small signal equivalent circuit that returns the feedback network back into an ideal feedback network.

8.3 Feedback Network Loading

8.4 Feedback Amplifier Frequency Response

8.5 Stability

8.6 Compensation