EEE 51 Assignment 3

2nd Semester SY 2018-2019
Due: 5pm Tuesday, February 19, 2019 (Rm. 220)

Instructions: Write legibly. Show all solutions and state all assumptions. Write your full name, student number, and section at the upper-right corner of each page. Start each problem on a new sheet of paper. Box or encircle your final answer.

Answer sheets should be color coded according to your lecture section. The color scheme is as follows:

THQ – yellow
THU – white
WFX – pink

1. **Single Stage Amplifier with Diode connected Load**

   Given that $V_{DD} = 5V$, $k_n = 6mA/V^2$, $k_p = 0.5mA/V^2$, $V_{th_n} = 0.7V$, $V_{th_p} = -0.5V$, $\lambda_n = 0.1V^{-1}$, $\lambda_p = 0.05V^{-1}$, and both FETs in saturation, answer the questions below.

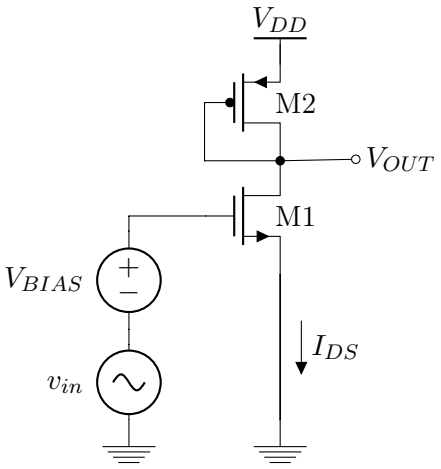


Figure 1: Amplifier with diode connected load

   (a) What is the amplifier configuration? *(1 pt.)*

   (b) Solve for I_{DS} and V_{BIAS} given that $V_{OUT} = 2.5V$ *(2 pts.)*

   (c) Solve for the small signal parameters then draw the small-signal equivalent circuit. Properly label all components and their values as well as terminal names. DO NOT assume that $|\lambda V_{DS}| << 1$ for both transistors in this part (use partial differentiation to get the small signal parameters). *(3 pts.)*

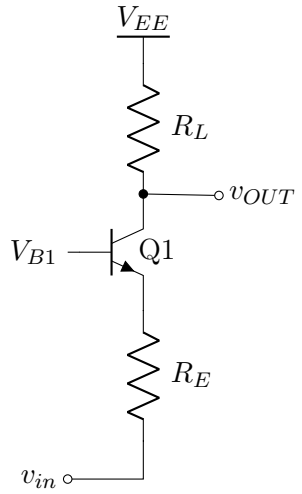
   (d) Get the expression for R_o then solve for its value. *(2 pts.)*

   (e) Get the expression for G_m then solve for its value. *(1 pt.)*

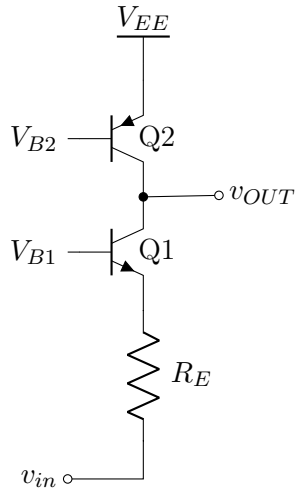
   (f) Solve for the value of the small signal voltage gain, $\frac{v_{out}}{v_{in}}$ *(1 pt.)*

2. **Single Stage Amplifier with Current Source Load**

For Figure 2, Assume that $Q1$ and $Q2$ are biased to operate in Forward Active Region @ $T = 300K$ but only $Q1$ has an early voltage that approaches infinity ($V_{A_{Q1}} \longrightarrow \infty$).



(a) Single Stage Amplifier with Load Resistor R_L



(b) Single Stage Amplifier with $Q2$

Figure 2

(a) Refer to Figure 2a for the items below.

i. Give the type of amplifier configuration for Figure 2a. *(1 pt.)*

ii. Draw the *simplified* small signal equivalent circuit and label all transistors terminals, small signal parameters and external resistors. *(2 pts.)*

iii. Derive the *simplified* expression for voltage gain $A_{v1} = \frac{v_{out}}{v_{in}}$ in terms of small signal parameters, R_E and R_L. You can assume that ($r_\pi >> \frac{1}{g_m}$) so that ($r_\pi || \frac{1}{g_m}$) $\approx \frac{1}{g_m}$. *(2 pts.)*

(b) Suppose that I_{DC} was replaced by $Q2$ which is shown in Figure 2b, refer to this figure for the items below.

i. Is the amplifier configuration type changed when R_L was replaced with $Q2$? Why or Why not? (Limit your answer into two sentences). *(1 pt.)*

ii. Draw the *simplified* small signal equivalent circuit and label all transistors terminals, small signal parameters and external resistors. *(3 pts.)*

iii. Derive the *simplified* expression for voltage gain $A_{v2} = \frac{v_{out}}{v_{in}}$ in terms of small signal parameters and R_E. You can also assume that ($r_\pi >> \frac{1}{g_m}$). *(2 pts.)*

(c) Lets say that the $\beta's$ for both transistors ($Q1$ for both figures and $Q2$) are high enough for the base currents (I_{B1} and I_{B2}) to be negligible with respect to the collector currents I_{C1} and I_{C2}. Now, for Figures 2a and 2b and given that $V_{EE} = 8V$, $V_{OUT} = 3V$, $R_E = 80\Omega$ with a voltage drop of

$V_{R_E} = 1.6V$, $Q2$ early voltage $V_{A_{Q2}} = 100V$, and still holding the assumption for $Q1$ early voltage to be $V_{A_{Q1}} \longrightarrow \infty$, Calculate the following:

i. Values for the derived A_{v1} and A_{v2}. (Limit your answer up to two decimal places) *(3 pts.)*

ii. The percentage increase/decrease of the two gains above relative to A_{v2}. What can you conclude about this? *(1 pt.)*

TOTAL: 25 points.