EEE 51 Assignment 5 Solution

2nd Semester SY 2017-2018
Due: 5pm Tuesday, March. 6, 2018 (Rm. 220)

Instructions: Write legibly. Show all solutions and state all assumptions. Write your full name, student number, and section at the upper-right corner of each page. Start each problem on a new sheet of paper. Box or encircle your final answer.

Starting from this homework onwards, answer sheets should be colored according to your lecture section. The color scheme is as follows:

THQ – yellow
THR – blue
THU – white
THX – green
WFX – pink

1. **BJT Differential Amplifier.** Given the BJT differential circuit shown in Figure 1. Assume that the two transistors are identical, and they are biased such that $I_{C1} = I_{C2} = \frac{I_{tail}}{2}$. Assume that V_A approachesAnswer the following questions using the concepts discussed in class and in the notes.

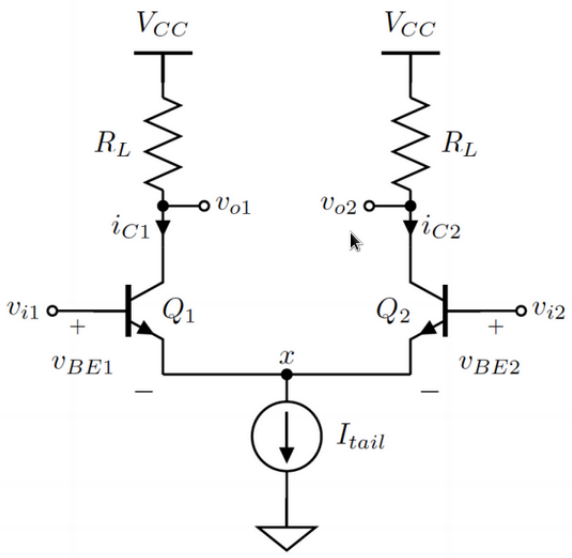

Figure 1: BJT Differential Amplifier.

(a) Determine the behavior(increase or decrease or no change) of I_{C1}, I_{C2}, V_{O1} and V_{O2} for the following changes in DC input bias voltages. [4 pts]

Table 1: Behavior of collector currents and output voltages with respect to changes in input voltage.

	I_{C1}	I_{C2}	V_{O1}	V_{O2}
$\uparrow V_{I1}, \downarrow V_{I2}$	$\uparrow$	$\downarrow$	$\downarrow$	$\uparrow$
$\downarrow V_{I1}, \uparrow V_{I2}$	$\downarrow$	$\uparrow$	$\uparrow$	$\downarrow$
$\uparrow V_{I1}, \uparrow V_{I2}$	no change	no change	no change	no change
$\downarrow V_{I1}, \downarrow V_{I2}$	no change	no change	no change	no change

(b) What is the difference between A_{cm} and A_{dm}. What is the effect of having a very high common mode gain? How does it affect the output of the differential amplifier? What would be its effect on the noise rejection of the differential amplifier? [3 pts]

Common Mode gain is the gain on the identical signal components that are common to both the + and - inputs of the differential amplifier. This includes in-phase components of the two input, and random noise voltages coupled into the two inputs of the amplifier.

Differential Mode Gain is the gain on the difference of the two input signals on the differential amplifier. These input signals are the signals that we want to amplify in a differential amplifier.

In a differential amplifier, we want to amplify the differential input voltage. This means that all other kinds of inputs are considered as unwanted. This includes the common-mode signals. Which means that we want to attenuate common mode signals in order to reduce its effect on the differential signals. If the common mode gain is high, there will be significant distortion to the output of the differential amplifier. Also, since random noise that is coupled to both inputs of the differential amplifier is considered as common-mode signals, these noise will be amplified as well.

(c) During fabrication, the transistors Q_1 and Q_2 were fabricated such that the two transistors are mismatched (i.e. the transistors are not identical). What would be the effect of this mismatch on the behavior of the differential amplifier? What would be its effect on the output of the differential amplifier assuming that the two transistors are biased at the same voltage? Explain these effects. [3 pts]

One of the most significant effects of the transistor mismatch in differential amplifiers is the output offset voltage. If transistors are mismatched, this means that the parameter I_S and V_A of the transistors are not equal. Therefore, having the same input bias voltage (V_{BE}) on both inputs will result in different currents in the two branches. If the resistors are equal in value, then the DC output differential voltage will not be equal to zero since the voltage drops across the two resistors are not equal. Due to this, there will be an output offset. In order to make the offset voltage of the differential amplifier zero, then the two transistors must be biased differently resulting in a required input offset voltage. Also, since BJTs are considered as current-controlled current source, then the input bias currents (I_B) to the two transistors also have an offset.

2. **MOSFET Differential Pair.** Consider the circuit shown below. For this problem, assume that $\lambda = 0$ for both M1 and M2.

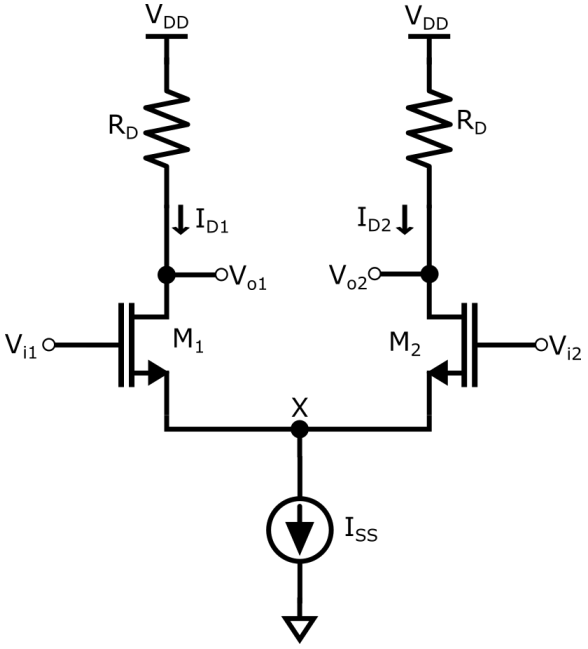

Figure 2: MOSFET Differential Pair

(a) **Derive** an expression for $I_{D1} - I_{D2}$ as a function of the differential input voltage, $V_{id} = V_{i1} - V_{i2}$. Assume that M1 and M2 are symmetric and saturated. [3 pts]
Note: While expressions for I_{D1} and I_{D2} are already on the lecture slides, this is an exercise on being able to derive such equations. You can start by identifying the voltage at node X in terms of V_{i1} and V_{i2}.

Since the voltage in node X is equal to $V_{i1} - V_{GS1}$ and $V_{i2} - V_{GS2}$, we can say that,

$$V_{i1} - V_{i2} = V_{GS1} - V_{GS2} \tag{1}$$

Also since it is assumed that both transistors are saturated and that $\lambda = 0$, we can rewrite the drain current equation of the MOSFET into,

$$(V_{GS} - V_{th})^2 = \frac{I_D}{k} \tag{2}$$

$$V_{GS} = \sqrt{\frac{I_D}{k}} + V_{th} \tag{3}$$

Since M1 and M2 are matched ($V_{th1} = V_{th2}$), it then follows that,

$$V_{i1} - V_{i2} = \left(\sqrt{\frac{I_{D1}}{k}} + V_{th1}\right) - \left(\sqrt{\frac{I_{D2}}{k}} + V_{th2}\right) = \sqrt{\frac{I_{D1}}{k}} - \sqrt{\frac{I_{D2}}{k}} \tag{4}$$

Squaring both sides and noting that $I_{D1} + I_{D2} = I_{SS}$,

$$(V_{i1} - V_{i2})^2 = \frac{I_{D1}}{k} + \frac{I_{D2}}{k} - 2\sqrt{\frac{I_{D1}I_{D2}}{k^2}} = \frac{I_{SS}}{k} - \frac{2}{k}\sqrt{I_{D1}I_{D2}} \tag{5}$$

Re-arranging Eq. (5) above,

$$k(V_{i1} - V_{i2})^2 - I_{SS} = -2\sqrt{I_{D1}I_{D2}} \tag{6}$$

Squaring both sides again,

$$k^2(V_{i1} - V_{i2})^4 - 2k(V_{i1} - V_{i2})^2 I_{SS} + I_{SS}^2 = 4I_{D1}I_{D2} \tag{7}$$

Note that,

$$4I_{D1}I_{D2} = (I_{D1} + I_{D2})^2 - (I_{D1} - I_{D2})^2 = I_{SS}^2 - (I_{D1} - I_{D2})^2 \tag{8}$$

Combining Eqs. (7) and (8),

$$(I_{D1} - I_{D2})^2 = -k^2(V_{i1} - V_{i2})^4 + 2k(V_{i1} - V_{i2})^2 I_{SS} \tag{9}$$

And then taking the square root,

$$I_{D1} - I_{D2} = \sqrt{k^2(V_{i1} - V_{i2})^2 \left[\frac{2}{k}I_{SS} - (V_{i1} - V_{i2})^2\right]} = k(V_{i1} - V_{i2})\sqrt{\frac{2I_{SS}}{k} - (V_{i1} - V_{i2})^2} \tag{10}$$

$$\boxed{I_{D1} - I_{D2} = k(V_{i1} - V_{i2})\sqrt{\frac{2I_{SS}}{k} - (V_{i1} - V_{i2})^2}}$$

[1 pt] will be given for using the drain current equation to express V_{GS} as shown in Eq. (3). [1 pt] will be given for squaring the expression $V_{i1} - V_{i2}$ and arriving at Eq. (5) or (6). [1 pt] will be given for squaring again and arriving at Eq. (10).

(b) Determine the slope of the characteristic equation (the equivalent G_m) you get from (a). [2 pts]

The slope or the equivalent G_m can be obtained by taking the partial derivative of your answer in (a) with respect to $V_{id} = V_{i1} - V_{i2}$. We denote $I_{D1} - I_{D2}$ as ΔI_D.

Recall from your Math 53, $D[a(x)b(x)] = a(x)D[b(x)] + D[a(x)]b(x)$

$$\frac{\partial \Delta I_D}{\partial V_{id}} = \frac{\partial}{\partial V_{id}}\left[kV_{id}\left(\frac{2I_{SS}}{k} - V_{id}^2\right)^{\frac{1}{2}}\right] = kV_{id}\frac{1}{2}\left(\frac{2I_{SS}}{k} - V_{id}^2\right)^{-\frac{1}{2}}(-2V_{id}) + k\left(\frac{2I_{SS}}{k} - V_{id}^2\right)^{\frac{1}{2}} \tag{11}$$

$$\frac{\partial \Delta I_D}{\partial V_{id}} = \frac{-kV_{id}^2}{\sqrt{\frac{2I_{SS}}{k} - V_{id}^2}} + \frac{2I_{SS} - kV_{id}^2}{\sqrt{\frac{2I_{SS}}{k} - V_{id}^2}} = \frac{2I_{SS} - 2kV_{id}^2}{\sqrt{\frac{2I_{SS}}{k} - V_{id}^2}} \tag{12}$$

$$G_m = \frac{\partial \Delta I_D}{\partial V_{id}} = \frac{2I_{SS} - 2kV_{id}^2}{\sqrt{\frac{2I_{SS}}{k} - V_{id}^2}}$$

[0.5 pts] will be given for the final answer while [1.5 pts] will be given for the complete solution.

(c) For this question onwards, use $I_{SS} = 1mA$ and $k = 2.5mA/V^2$. At equilibrium, determine the gate overdrive voltage, $V_{GS} - V_{th}$, of both transistors. [1 pt]

This can be solved from the drain current equation of the MOSFET at saturation,

$$V_{GS} - V_{th} = \sqrt{\frac{I_D}{k}} = \sqrt{\frac{\frac{I_{SS}}{2}}{k}} = \sqrt{\frac{0.5mA}{2.5mA}V^2} = 0.4472V \tag{13}$$

$$V_{GS} - V_{th} = 0.4472V \text{ [1 pt]}$$

(d) What are the drain currents of M1 and M2 if $V_{id} = 50mV$? [1 pt]

From Eq. (10),

$$I_{D1} - I_{D2} = (2.5m\frac{A}{V^2})(50mV)\sqrt{\frac{2(1mA)}{2.5m\frac{A}{V^2}} - (50mV)^2} = 111.6\mu A \tag{14}$$

$$I_{D1} = \frac{I_{SS} + 111.6\mu A}{2} = 555.8\mu A \text{ [0.5 pts]}$$
$$I_{D2} = \frac{I_{SS} - 111.6\mu A}{2} = 444.2\mu A \text{ [0.5 pts]}$$

(e) What is the equivalent G_m if $V_{id} = 50mV$? [1 pt]

Using Eq. (12),

$$G_m = \frac{2I_{SS} - 2kV_{id}^2}{\sqrt{\frac{2I_{SS}}{k} - V_{id}^2}} = \frac{2(1mA) - 2(2.5m\frac{A}{V^2})(50mV)^2}{\sqrt{\frac{2(1mA)}{2.5m\frac{A}{V^2}} - (50mV)^2}} = 2.226mS \tag{15}$$

$$G_m = 2.226mS \text{ [0.5 pts]}$$

(f) For what value of V_{id} does G_m drop by 10% from equilibrium? By 90%? [2 pts]

At equilibrium ($V_{id} = 0$), $G_m = 2.236mS$. Thus we need to solve V_{id} for $G_{m,10\%drop} = 2.012mS$ and $G_{m,90\%drop} = 0.2236mS$. Now re-writing Eq. (12) to express V_{id}^2 in terms of G_m:

$$G_m\sqrt{\frac{2I_{SS}}{k} - V_{id}^2} = 2I_{SS} - 2kV_{id}^2 \tag{16}$$

Squaring both sides,

$$\left(G_m\sqrt{\frac{2I_{SS}}{k} - V_{id}^2}\right)^2 = (2I_{SS} - 2kV_{id}^2)^2 \tag{17}$$

$$\frac{2I_{SS}G_m^2}{k} - G_m^2V_{id}^2 = 4I_{SS}^2 - 8kI_{SS}V_{id}^2 + 4k^2V_{id}^4 \tag{18}$$

$$4k^2V_{id}^4 + (G_m^2 - 8kI_{SS})V_{id}^2 + \left(4I_{SS}^2 - \frac{2I_{SS}G_m^2}{k}\right) \tag{19}$$

Solving for V_{id}^2,

$$V_{id}^2 = \frac{-(G_m^2 - 8kI_{SS}) \pm \sqrt{(G_m^2 - 8kI_{SS})^2 - 4(4k^2)\left(4I_{SS}^2 - \frac{2I_{SS}G_m^2}{k}\right)}}{2(4k^2)} \tag{20}$$

$$V_{id}^2 = \frac{8kI_{SS} - G_m^2 \pm \sqrt{(G_m^2 - 8kI_{SS})^2 - 64k^2I_{SS}^2 + 32kI_{SS}G_m^2}}{8k^2} \tag{21}$$

Using Eq. (21) and using $G_{m,10\%drop} = 2.012mS$, we get two possible values for V_{id}^2.

We get $V_{id}^2 = 0.5861V \rightarrow |V_{id}| = 0.7656V$ and $V_{id}^2 = 0.05196V \rightarrow |V_{id}| = 0.2279V$. To determine which one is the correct value, substitute these values back into Eq. (12).

For $V_{id}^2 = 0.5861V$, $G_m = -2.012mS$, while for $V_{id}^2 = 0.05196V$, $G_m = 2.012mS$. Hence we take the smaller value.

For 10% drop in G_m, $\lvert V_{id}\rvert = 0.2279V$ [1 pt]

Again, using Eq. (21) and using $G_{m,90\%drop} = 0.2236mS$, we also get two possible values for V_{id}^2.

We get $V_{id}^2 = 0.4273V \rightarrow |V_{id}| = 0.6537V$ and $V_{id}^2 = 0.3707V \rightarrow |V_{id}| = 0.6088V$. To determine which one is the correct value, substitute these values back into Eq. (12).

For $V_{id}^2 = 0.4273V$, $G_m = -0.2236mS$, while for $V_{id}^2 = 0.3707V$, $G_m = 0.2236mS$. Hence we take the smaller value.

For 90% drop in G_m, $\lvert V_{id}\rvert = 0.6088V$ [1 pt]

3. **MOSFET Differential Amplifier with Active Load**. Dahyun wants to attend a concert with Sana, but she finds out that the venue's speakers are broken, so she decides to build her own amplifier. She designs the amplifier shown in Figure 3 with the following parameters: $k_n = 10\frac{mA}{V^2}$, $k_p = 8\frac{mA}{V^2}$, $V_{TH,n} = 0.3V$, $V_{TH,p} = -0.5V$, $\lambda_n = 0$, and $\lambda_p = 0.05V^{-1}$. $V_{DD} = 12V$, $V_P = 8.2V$, and $I_{tail} = 200mA$. The non-ideal current source has a finite resistance $R_{tail} = 1000\Omega$ and has a $V_{min} = 1V$. Similar transistors are perfectly matched (i.e. M_1 and M_2 are matched; M_3 and M_4 are matched). Dahyun needs to extract the amplifier's specifications, so now she asks for your help.

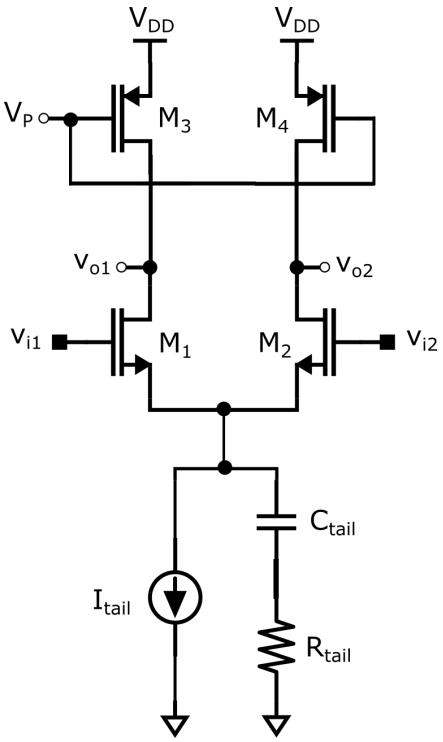

Figure 3: MOSFET Differential Amplifier with Active Load

(a) What is the common mode input range (ICMR) of the amplifier? [2 pts]

The solution to this question is similar to the one in Handout 5. Let node x be the node that connects the sources of the two NMOS and I_{tail} and C_{tail} so that the voltage across the current source is V_X. The drain-to-source voltage of M_1 is:

$$V_{DS1} = V_{DD} - V_{SD3} - V_X \tag{22}$$

and V_X can be expressed as:

$$V_X = V_{I1} - V_{GS1} \tag{23}$$

To ensure that M_1 is in saturation,

$$V_{DS1} > V_{GS1} - V_{TH,n} \tag{24}$$

$$V_{DD} - V_{SD3} - V_{I1} + V_{GS1} > V_{GS1} - V_{TH,n} \tag{25}$$

$$V_{DD} - V_{SD3} - V_{cm} > -V_{TH,n} \tag{26}$$

If there is no differential input applied to the circuit, V_I becomes V_{cm}. C_{tail} then becomes an open circuit, so the drain currents of the transistors $I_D = \frac{I_{tail}}{2} = 100mA$. Then for the PMOS transistors,

$$V_{SD3} = \frac{\frac{I_D}{k_p(V_{SG3}-|V_{TH,p}|)^2} - 1}{\lambda_p} = 4.4141V \tag{27}$$

Checking for the region of operation of the PMOS transistors:

$$V_{SD3,sat} = V_{SG3} - |V_{TH,p}| = 12 - 8.2 - 0.6 = 3.2V \tag{28}$$

We can see that $V_{SD3} > V_{SD3,sat}$, so the PMOS transistors are in saturation. Now, substituting (27) into (25), we get

$$V_{DD} - V_{SD3} + V_{TH,n} > V_{cm} = V_{cm,max} \tag{29}$$

$$V_{cm,max} = V_{DD} - V_{SD3} + V_{TH,n} > V_{cm} \tag{30}$$

$$V_{cm,max} = 12 - 4.4141 + 0.3 \tag{31}$$

$$V_{cm,max} = 7.8859V \text{ [1 pt]}$$

The minimum value of V_{cm} is determined by the V_{min} of the current source I_{tail}.

$$V_X = V_{cm} - V_{GS1} > V_{min} \tag{32}$$

$$V_{cm,min} = V_{GS1} + V_{min} \tag{33}$$

$$V_{cm,min} = V_{TH,n} + \sqrt{\frac{I_{tail}}{2k_n}} + V_{min} = 0.3 + \sqrt{\frac{200mA}{2(10\frac{mA}{V^2})}} + 1 \tag{34}$$

$$V_{cm,min} = 4.4623V \text{ [1 pt]}$$

(b) Solve for A_{dm}. Be sure to include the small signal circuit and label everything accordingly. [4 pts]

First, get the small signal parameters of the transistors.

$$g_{m1} = g_{m2} = \sqrt{4k_n I_D} = \sqrt{4(10\tfrac{mA}{V^2})(100mA)} = 63.2455mS \text{ [0.25 pt]}$$
$$g_{m3} = g_{m4} = \sqrt{4k_p(1+\lambda_p V_{SD3})I_D} = \sqrt{4(8\tfrac{mA}{V^2})[1+(0.05)(1.6263)](100mA)} = 58.8235mS \text{ [0.25 pt]}$$
$$r_{o1} = r_{o2} = \frac{1}{\lambda_n I_D} = \frac{1}{(0)(100mA)} \to \infty \text{ [0.25 pt]}$$
$$r_{o3} = r_{o4} = \frac{1}{\lambda_p I_D} = \frac{1}{(0.05V^{-1})(100mA)} = 200\Omega \text{ [0.25 pt]}$$

Next, since the circuit is symmetric about node x, we can analyze the small signal behavior by getting the differential mode half circuit. Now let us consider the left side of the differential pair. Remember that in the differential mode, node x can be considered as a virtual ground. The corresponding half circuit is shown in Figure 4.

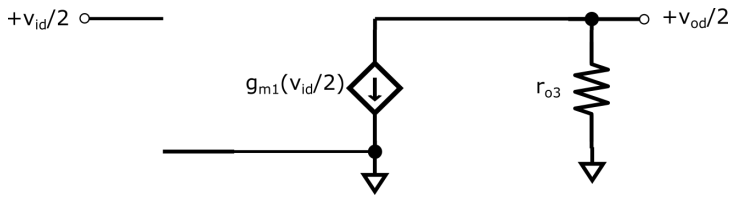

Figure 4: Differential Mode Small Signal Half Circuit Equivalent

2 pts shall be credited to the correct small signal half circuit.

The small signal half circuit is the same as that of a single transistor with load equivalent to the r_o of the PMOS. The differential mode gain is then

$$A_{dm} = -g_{m1}r_{o3} = -(63.2455mS)(200\Omega) = -12.6491 \text{ [1 pt]}$$

(c) Solve for A_{cm}. Be sure to include the small signal circuit and label everything accordingly. [3 pts]

Because we are dealing with small signals in this analysis, we can ignore the tail current. The common mode small signal circuit is then:

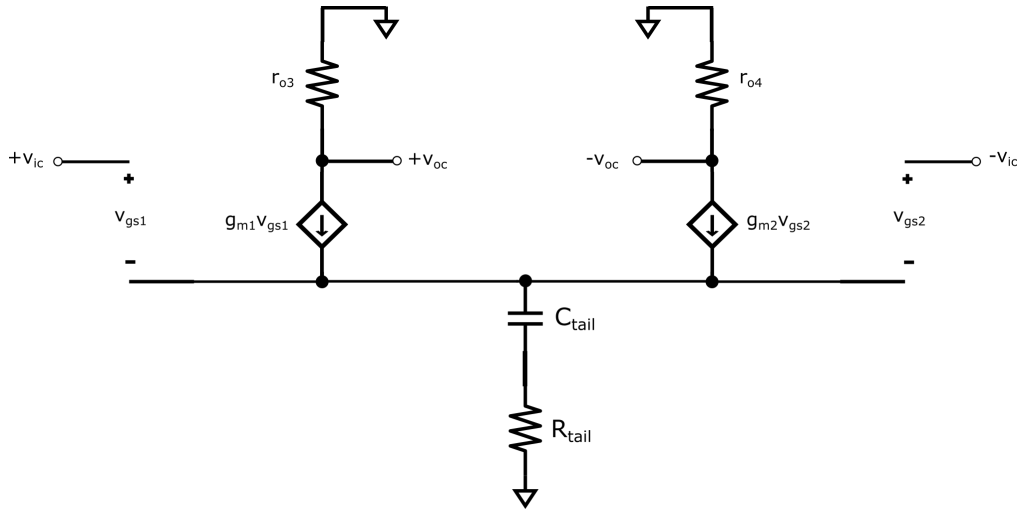

Figure 5: Common Mode Small Signal Circuit

We can reduce the small signal circuit further into its half circuit equivalent. Since C_{tail} is infinitely large, it becomes an open circuit and the common mode half circuit equivalent is:

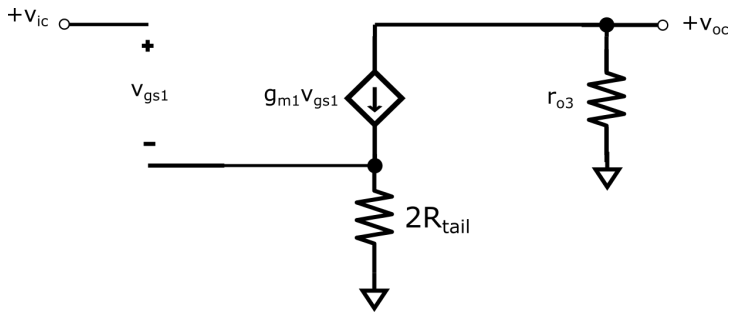

Figure 6: Common Mode Half Circuit Small Signal Equivalent

2 pts shall be given to the correct half circuit.

Notice that the circuit in Figure 6 is similar to that of a source degenerated amplifier with source resistance equal to $2R_{tail}$. The common mode gain, $A_{cm} = \frac{v_{oc}}{v_{ic}}$ can be computed as follows:

$$v_{ic} = v_{gs1} + g_{m1}v_{gs1}(2R_{tail}) \tag{35}$$

$$v_{gs1} = \frac{v_{ic}}{1 + 2g_{m1}R_{tail}} \tag{36}$$

$$v_{oc} = -g_{m1}v_{gs1}r_{o3} = -v_{ic}\frac{g_{m1}r_{o3}}{1 + 2g_{m1}R_{tail}} \tag{37}$$

$$A_{cm} = -\frac{g_{m1}r_{o3}}{1 + 2g_{m1}R_{tail}} = -\frac{(63.2455mS)(200\Omega)}{1 + 2(63.2455mS)(1000\Omega)} \tag{38}$$

$A_{cm} = -0.0992$ [1 pt]

(d) The concert will be able to push through if the common mode rejection ratio (CMRR) of the amplifier is greater than 100. Will Dahyun be able to take Sana to the concert? [1 pt]

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{12.6491}{0.0992}\right| \tag{39}$$

$CMRR = 127.4911$
Yes, Dahyun will be able to take Sana to the concert. [1 pt]

TOTAL: 30 points.