EEE 51 Assignment 5

2nd Semester SY 2018-2019
Due: 5pm Tuesday, March 12, 2019 (Rm. 220)

Instructions: Write legibly. Show all solutions and state all assumptions. Write your full name, student number, and section at the upper-right corner of each page. Start each problem on a new sheet of paper. Box or encircle your final answer.

Answer sheets should be color coded according to your lecture section. The color scheme is as follows:

THQ – yellow
THU – white
WFX – pink

1. **Simpe BJT Differential Pair**

   Shown in Figure 1 is a BJT differential pair with resistor load. Assume that the BJTs operate in the forward active region, $V_A \to \infty$. Answer the following.

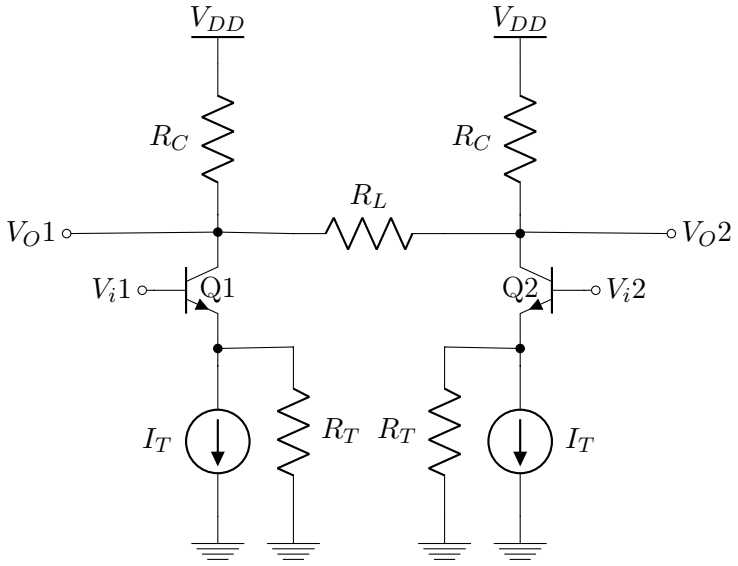

Figure 1: BJT differential pair

   (a) Explain the difference between differential mode gain, A_{dm} and common mode gain, A_{cm} and their relation to Common Mode Rejection Ratio (CMRR). Do we want a high or low CMRR? Explain. (2pts)

   (b) Why is it important that the components in the branches be matched? How does it affect the analysis of the differential pair? (2pts)

   (c) Draw the differential mode half circuit and find the differential mode gain, A_{dm} in terms of small signal parameters and circuit components. (2pts)

   (d) Draw the common mode half circuit and find the common mode gain, A_{cm} in terms of small signal parameters and circuit components. (2pts)

   (e) How does R_T affect the amplifier's performance? (2pts)

2. **Differential Pair with Resistive Bias and Resistive Load.**

The differential pair shown in Figure 2 is supplied by $V_{DD} = -V_{SS} = 1\,\text{V}$. The process technology used have the following: $V_{TH,P} = 400\,\text{mV}$, $V_{TH,N} = 550\,\text{mV}$, $\lambda_P = 0.001\,\text{V}^{-1}$, and $\lambda_N = 0.01\,\text{V}^{-1}$. Each transistor have been characterized and found out that: $k_1 = k_2 = 4.082\,\mu\text{A/V}^2$, $k_3 = k_4 = 12.5\,\mu\text{A/V}^2$, $k_5 = 400\,\mu\text{A/V}^2$, $k_6 = 4\,\mu\text{A/V}^2$, and $k_7 = 250\,\text{nA/V}^2$, where k is defined as $k = \frac{\mu C_{ox}}{2}\frac{W}{L}$. The pair is used with input DC voltage of 0 V on both sides ($V_I^+ = V_I^- = 0\,\text{V}$).

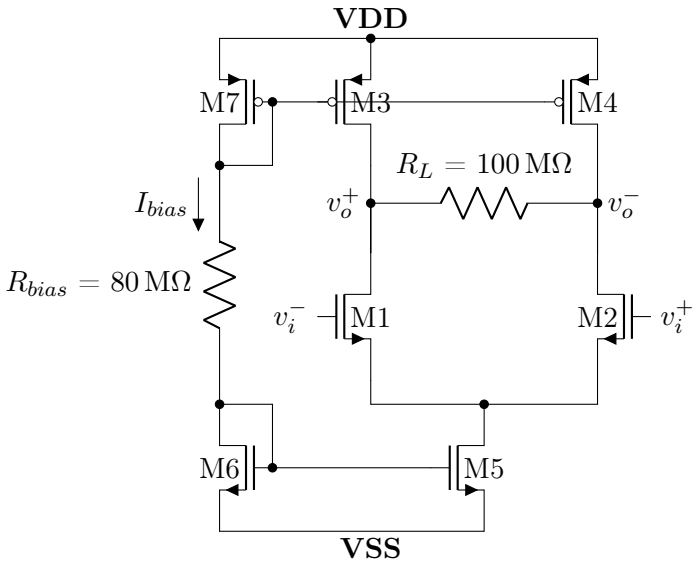

Figure 2: Differential Pair with Resistive Bias

Answer the following questions. Ignore channel length modulation. Unless otherwise stated, always round off your answers to the nearest whole number of the appropriate magnitude.

(a) Find the biasing values for the transistors to complete the table below. Round off your answers to the nearest millivolt. (3 pts)

Transistor	V_{SG} or V_{GS} (mV)
M1 & M2	
M3, M4, & M7	
M5 & M6	

(b) Draw the small-signal differential mode half circuit with corresponding labels and values, and identify the differential gain. (2 pts)

(c) Draw the small-signal common mode half circuit with corresponding labels and values, and identify the common mode gain. (2 pts)

(d) What is the value of the CMRR? Round down the answer to the greatest integer less than or equal to the actual answer. If the bias circuit (M6, M7, and R_{bias}) is fixed, as well as the dimensions of M1 to M4, what adjustment should be made to either R_L or M5 to increase the CMRR? (2 pts)

(e) What is the maximum differential input voltage swing? (1 pt)

3. **BJT Differential Amplifier <3.** You finally found the person of your dreams in your EEE 52 class, so want to impress him/her with your skills through your design project. Luckily, your instructor simplified your design project: all you have to do is amplify a 2 mV peak-to-peak 1 KHz sinusoid into a 400 mV peak-to-peak 1 KHz sinusoid using a differential amplifier with resistive load as shown in fig. 3. Let's define $v_{out} = v_o^+ - v_o^-$, and $V_{DD} = 9V$. You may assume $V_A \to \infty$, $\beta = 200$, $V_{BE,on} = 0.7V$, $V_T = 26mV$, and $V_{CE,sat} = 0.2V$, and that all transistors are identical.

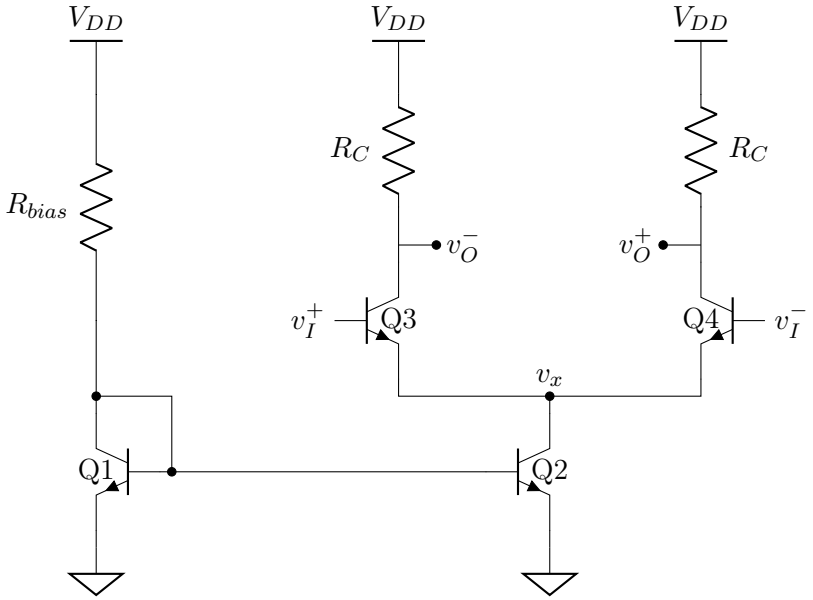

Figure 3: Differential Pair with Resistive Load

You want to ensure that the amplifier works within the target range of input and output voltages. So you check the DC biasing conditions first:

(a) What is the minimum DC bias for the input voltages V_I^+ and V_I^- such that all transistors are biased at Forward active? (0.5 pt.)

(b) Is there a maximum DC bias for the input voltages V_I^+ and V_I^- to ensure correct operation of the amplifier? If yes, what is it? (0.5 pt.)

(c) Your instructor required everyone to design the amplifier to have a total of 2 mA current draw from V_{DD}, both the differential amplifier and the current reference. How much current should flow through Q3 and Q4 each? (0.5 pt.)

Small-signal analysis:

(d) How much differential-mode gain A_{DM}, will you need? (0.5 pt)

(e) Calculate the required R_C to meet the necessary small-signal differential-mode gain, A_{DM}. (1 pt.)

(f) Calculate the DC biasing V_O^- and V_O^+ for the calculated R_C. (1 pt)

(g) Calculate the common-mode gain, A_{CM}. (1 pt)

Do or Die! Assume you biased $V_I^+ = V_I^- = 2V$. It's the demo day, and everything was well until...

(h) All the AC sources in the lab suddenly malfunctioned! Each sinusoidal source voltage is increased by 2 Volts DC. Will your amplifier still work? Should you (A) suddenly turn off all the sources to save yourself from shame; or (B) leave everything on, and impress both the person of your dreams, and your instructor? Prove by presenting/calculating whichever parameter/s must be considered. (Hint: You'll need to look at at least 1 DC biasing parameter, and 1 differential amplifier parameter) (2 pts)

(i) All the AC sources suddenly got fixed and now give the correct DC biasing. However, your instructor was disappointed / impressed. So he/she disconnected and changed the AC sources:

$$\begin{aligned} v_i^- &= -1sin(2\pi ft)mV \\ v_i^+ &= 0.01 + 1sin(2\pi ft)mV \\ f &= 1KHz \end{aligned}$$

He/she then asks you in front of everyone what would happen to the output when the AC source is connected. It's your chance to shine! Write the mathematical expression for the small-signal differential output voltage, v_{od}. (2 pt)

(j) Calculate the small-signal common-mode output voltage, v_{oc} for the problem in (i). (1 pt)

TOTAL: 30 points.