EEE 51 Assignment 3 Solution

2nd Semester SY 2017-2018
Due: 5pm Tuesday, Feb. 20, 2018 (Rm. 220)

Instructions: Write legibly. Show all solutions and state all assumptions. Write your full name, student number, and section at the upper-right corner of each page. Start each problem on a new sheet of paper. Box or encircle your final answer.

Starting from this homework onwards, answer sheets should be colored according to your lecture section. The color scheme is as follows:

THQ – yellow
THR – blue
THU – white
THX – green
WFX – pink

1. **Darlington Emitter Follower.** Tzuyu receives an invite to Jihyo's birthday party, but shown in the invitation are the NPN Darlington emitter follower in Figure 1, as well as their parameters. $V_{IN} = 16.4V$, $\beta_1 = \beta_2 = \beta = 200$, $I_{S1} = 8.12fA$, $I_{S2} = 10.15fA$, and $V_A \to \infty$ for both transistors. To attend the party, guests must send a four-letter reply that can be decoded by analyzing the circuit. Round your answers to three decimal places.

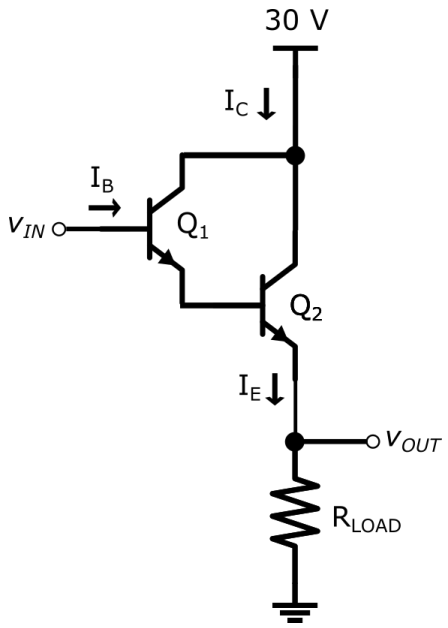

Figure 1: Darlington Emitter Follower

(a) Express β_{eff} in terms of β. What is the advantage of using a Darlington pair over a single transistor? [2 pts]

First, express the effective currents of the Darlington pair in terms of the individual currents of each transistor.

$$I_C = I_{C1} + I_{C2} \tag{1}$$

$$I_B = I_{B1} \tag{2}$$

$$I_E = I_{E2} \tag{3}$$

In (1), replace the individual I_C's in terms of β, so we get:

$$I_C = \beta I_{B1} + \beta I_{B2} \tag{4}$$

Substituting (2) in (4), we have another form of the equation.

$$I_C = \beta I_B + \beta I_{B2} \tag{5}$$

Looking at the configuration, we can see that I_{E1} and I_{B2} are equal. So we can express this base current of $Q2$ in terms of the base and collector currents of $Q1$. We can simplify this further so that I_{B2} can be expressed in terms of I_B.

$$I_{B2} = I_{E1} = I_{C1} + I_B = \beta_1 I_B + I_B = (\beta_1 + 1) I_B \tag{6}$$

Revisiting (5) we can use (6) to obtain another expression for the equation.

$$I_C = \beta_1 I_B + \beta_2(\beta_1 + 1) I_B = (\beta_1 + \beta_2\beta_1 + \beta_2) I_B \tag{7}$$

Since β_1 and β_2 are equal,

$$I_C = (2\beta + \beta^2) I_B \tag{8}$$

$\beta_{eff} = \frac{I_C}{I_B} = 2\beta + \beta^2$ [1 pt]
It can be seen in (8) that using a Darlington pair increases the DC current gain. This means that a smaller base current is required for high collector currents. This high current gain also implies a higher input impedance compared to using a single transistor. [1 pt]

In deriving β_{eff}, other solutions will be accepted as long as the analysis and final answer are correct.

(b) Solve for the DC value V_{LOAD}. [1 pt]

To solve for V_{LOAD}, the current through R_{LOAD} must first be solved. To do this, we can apply KVL through the loop from V_{IN} to V_{LOAD} as follows:

$$V_{IN} = V_{BE1} + V_{BE2} + I_{LOAD} R_{LOAD} \tag{9}$$

We can express the V_{BE} of both transistors through I_{LOAD}, so that (9) can be expressed as:

$$V_{IN} = kTln\left(\frac{I_{LOAD}}{I_{S1}}\frac{\beta}{\beta+1}\right) + kTln\left(\frac{I_{LOAD}}{I_{S2}}\frac{\beta}{(\beta+1)^2}\right) + I_{LOAD} R_{LOAD} \tag{10}$$

All other parameters are known, so I_{LOAD} can be calculated from (10). Rounding off to three decimal places, we get I_{LOAD} and V_{LOAD} to be:

$I_{LOAD} = 5.069mA$ [0.5 pt]
$V_{LOAD} = I_{LOAD} R_{LOAD} = (5.069mA)(2985\Omega) = 15.132V$ [0.5 pt]

(c) Solve for $I_{C,tot}$. [2 pts]

$$I_{C2} = I_{E2}\frac{\beta}{\beta+1} = I_{LOAD}\frac{\beta}{\beta+1} = 5.044mA \tag{11}$$

$$I_{C1} = I_{LOAD}\frac{\beta}{(\beta+1)^2} = 25.093\mu A \tag{12}$$

$I_{C2} = 5.044mA$ [0.5 pt] $I_{C1} = 25.093\mu A$ [0.5 pt] $I_{C,tot} = I_{C1} + I_{C2} = 5.044mA + 25.093\mu A = 5.069mA$ [1 pt]

(d) Solve for A_v. Include and make sure to box the simplified version of your small signal circuit. Label everything accordingly. [4 pts]

The small signal parameters of each transistor can be solved using the quiescent currents of Q1 and Q2. Recall the following equations:

$$g_m = \frac{I_{C,Q}}{V_T} \tag{13}$$

$$r_o = \frac{V_A}{I_{C,Q}} \tag{14}$$

$$r_\pi = \frac{\beta V_T}{I_{C,Q}} \tag{15}$$

Since $V_A \to \infty$ for both transistors, $r_o \to \infty$ for both transistors as well. We already have the I_C's from (11) and (12), therefore the values of the small signal parameters are:

$g_{m1} = 965.115\mu S$ [0.25 pt]
$g_{m2} = 194mS$ [0.25 pt]
$r_{\pi 1} = 207,229.108\Omega$ [0.25 pt]
$r_{\pi 2} = 1,030.928\Omega$ [0.25 pt]

The equivalent small-signal model of the Darlington emitter follower is shown in Figure 2.

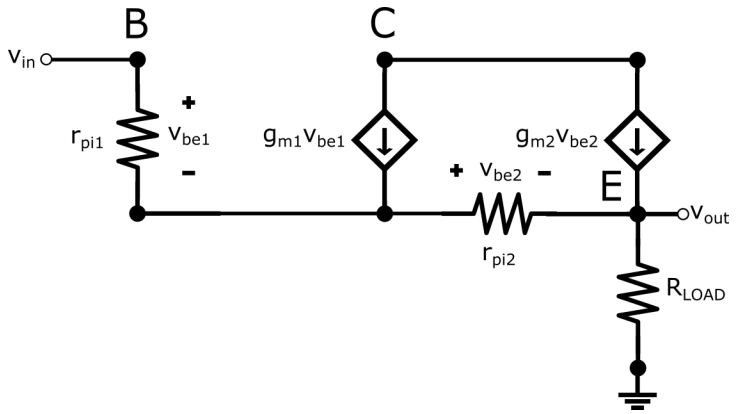

Figure 2: Darlington Emitter Follower Small Signal Model

1 pt shall be credited to the correct small signal circuit.

To get A_v, G_m and R_o must first be solved.

$$G_m = \left.\frac{i_o}{v_i}\right|_{no-load} \tag{16}$$

$$i_o + g_{m2} v_{be2} + \frac{v_{be2}}{r_{\pi 2}} = 0 \tag{17}$$

$$i_o = -v_{be2}\left(g_{m2} + \frac{1}{r_{\pi 2}}\right) \tag{18}$$

$$g_{m1}v_{be1} + \frac{v_{be1}}{r_{\pi 1}} = \frac{v_{be2}}{r_{\pi 2}} \tag{19}$$

$$v_{be1}\left(g_{m1} + \frac{1}{r_{\pi 1}}\right) = v_{be2}\left(\frac{1}{r_{\pi 2}}\right) \tag{20}$$

$$v_i = v_{be1} + v_{be2} = v_{be2}\left[\frac{1}{r_{\pi 2}(g_{m1} + \frac{1}{r_{\pi 1}})}\right] \tag{21}$$

$$v_i = v_{be2}\left(1 + \frac{1}{r_{\pi 2}g_{m1} + \frac{r_{\pi 2}}{r_{\pi 1}}}\right) \tag{22}$$

$$\frac{i_o}{v_i} = -\left(\frac{g_{m2} + \frac{1}{r_{\pi 2}}}{1 + \frac{1}{r_{\pi 2}g_{m1} + \frac{r_{\pi 2}}{r_{\pi 1}}}}\right) \tag{23}$$

$$G_m = -97.482mS \text{ [0.5 pt]}$$

$$R_o = \left.\frac{v_o}{i_o}\right|_{zero-input} \tag{24}$$

$$i_o + \frac{v_{be2}}{r_{\pi 2}} + g_{m2}v_{be2} = 0 \tag{25}$$

$$i_o = -v_{be2}\left(g_{m2} + \frac{1}{r_{\pi 2}}\right) \tag{26}$$

$$\frac{v_{be1}}{r_{\pi 1}} + g_{m1}v_{be1} = \frac{v_{be2}}{r_{\pi 2}} \tag{27}$$

$$v_{be1} = v_{be2}\left(\frac{\frac{1}{r_{\pi 2}}}{\frac{1}{r_{\pi 1}} + g_{m1}}\right) \tag{28}$$

$$v_o = -(v_{be1} + v_{be2}) \tag{29}$$

$$v_o = -\left[v_{be2}\left(\frac{1}{\frac{r_{\pi 2}}{r_{\pi 1}} + r_{\pi 2}g_{m1}}\right) + v_{be2}\right] = -v_{be2}\left(1 + \frac{1}{\frac{r_{\pi 2}}{r_{\pi 1}} + r_{\pi 2}g_{m1}}\right) \tag{30}$$

$$\frac{v_o}{i_o} = \frac{1 + \frac{1}{\frac{r_{\pi 2}}{r_{\pi 1}} + r_{\pi 2}g_{m1}}}{g_{m2} + \frac{1}{r_{\pi 2}}} \tag{31}$$

$$R_o = 10.258\Omega \text{ [0.5 pt]}$$

$$A_v = -G_mR_o = -(-97.482mS)(10.258\Omega) \tag{32}$$

$$A_v = 0.999970356 \approx 1 \text{ [1 pt]}$$

(e) If the input to the circuit is $26mV$ peak-to-peak, what is the amplitude of the output in mV?

Since the voltage gain is 1, then $V_{out,pp} = V_{in,pp}$. So for the given input voltage, the output amplitude should be

$$V_{out,amp} = 13mV \text{ [1 pt]}$$

(f) The four-letter reply corresponds to the answers in (b) to (e). The numbers can be translated to the order of the letters in the English alphabet. (e.g. $A = 1$, $B = 2$, $C = 3$, etc.) For answers greater than 26, just add 26 to the original code, i.e. $A = 27$, $B = 28$, $C = 29$. What should be Tzuyu's reply to Jihyo? [0 pt, this is just for fun :)]

$V_{LOAD} = 15.132V \rightarrow 15 \rightarrow O$
$I_{C,tot} = 5.069mA \rightarrow 5 \rightarrow E$
$A_v = 1 \rightarrow A$
$V_{out,amp} = 13mV \rightarrow 13 \rightarrow M$

The code is $OEAM$. [0 pt]

2. **MOSFET CS Amplifier with current source load**. Given the circuit below and provided the following parameters: $V_{DD} = 3V$, $k_n = 7mA/V^2$, $k_p = 0.48mA/V^2$, $V_{th,n} = 0.6V$, $V_{th,p} = -0.5V$, $\lambda_n = 0.1V^{-1}$, $\lambda_p = 0.05V^{-1}$ and $I_{DS1} = I_{SD2} = 0.5mA$ when both M1 and M2 are in saturation, solve for the following.

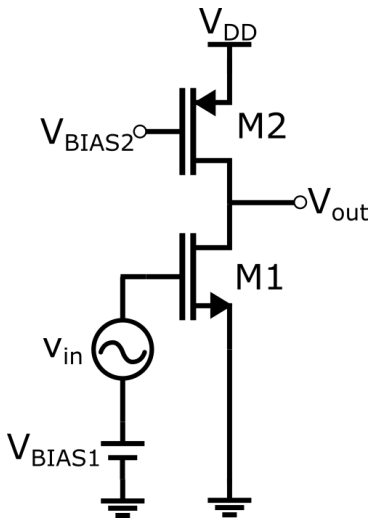

Figure 3: CS amplifier with current source load

(a) **Simple DC Biasing.** What would be the needed values of V_{BIAS1} and V_{BIAS2} if we want to bias the circuit such that $V_{OUT} = 1.5V$? [1 pt]

For a $V_{OUT} = 1.5V$ and keeping $I_{DS1} = I_{SD2} = 0.5mA$, we can solve for the bias voltages, V_{BIAS1} and V_{BIAS2} by writing the current equations for M1 and M2 at saturation.

For M1,

$$I_{DS1} = k_n(V_{GS1} - V_{th,n})^2(1 + \lambda V_{DS1}) \tag{33}$$

And for M2,

$$I_{SD2} = k_p(V_{SG2} - |V_{th,p}|)^2(1 + \lambda V_{SD2}) \tag{34}$$

Solving for V_{BIAS1} using the equation for M1 and noting that $V_{GS1} = V_{BIAS1}$ and $V_{DS1} = V_{OUT}$,

$$0.5mA = 7m\frac{A}{V^2}(V_{BIAS1} - 0.6)^2(1 + (0.1)(1.5)) \tag{35}$$

$V_{BIAS1} = 0.849V$ [0.5 pts]

Doing the same for M2 and noting that $V_{SG2} = V_{DD} - V_{BIAS2}$ and $V_{SD2} = V_{DD} - V_{OUT}$,

$$0.5mA = 0.48m\frac{A}{V^2}(3 - V_{BIAS2} - |-0.5|)^2(1 + (0.05)(1.5)) \tag{36}$$

$V_{BIAS2} = 1.516V$ [0.5 pts]

(b) Draw the complete small-signal model of the circuit. Label the transistor terminals, the small-signal parameters of both transistors (r_π, r_o, g_m) and their values. You can assume that $\lambda_n V_{DS} << 1$ and $\lambda_p V_{SD} << 1$ for this part. [3 pts]

In computing the values of the small signal parameters, the following were used:

$$r_{o,n} = \frac{1}{\lambda I_{DS}} \quad r_{o,p} = \frac{1}{\lambda I_{SD}} \tag{37}$$

For the g_m's of M1 and M2, since we assumed that $\lambda_n V_{DS} << 1$ and $\lambda_p V_{SD} << 1$, we can use the following set of equations,

$$g_{m,n} = \sqrt{4k_n I_{DS}} \quad g_{m,p} = \sqrt{4k_p I_{SD}} \tag{38}$$

Lastly, since for MOS transistors, $I_G = 0$, then $r_{\pi,n} = r_{\pi,p} = \infty$.

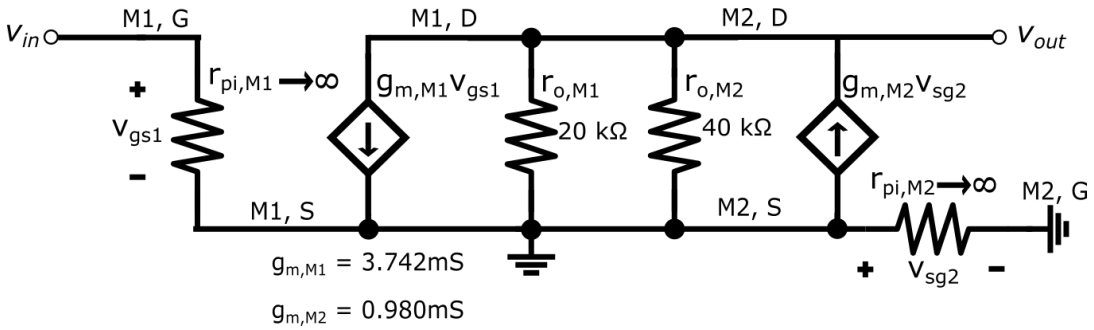

Figure 4: **Complete** small-signal model with parameter values

Scoring for this part would be: **[2 pts]** for the **complete** small-signal model. If the drawing is still correct but is **simplified** or there are missing labels and/or components (like resistors that would otherwise be not present in the simplified drawing since they are "open" or infinite) **[1 pt]** will be given. As for the parameter values (r_π, r_o, g_m), **[1 pt]** will be given for the correct values. All values must be correct otherwise no point will be given.

(c) Find the expression for the small-signal gain, $\frac{v_{out}}{v_{in}}$. [2 pts]

Simplifying the small-signal model, we get the following figure below:

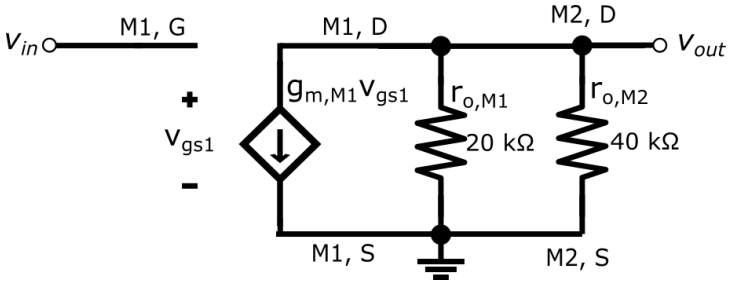

Figure 5: Simplified small-signal model

For simplicity, we denote $g_{m,M1}$, $r_{o,M1}$ and $r_{o,M2}$ as g_{m1}, r_{o1} and r_{o2} respectively. By applying KCL at the output node, we get the following:

$$-g_{m1}v_{gs1} = \frac{v_{out}}{r_{o1}} + \frac{v_{out}}{r_{o2}} \tag{39}$$

$$-g_{m1}v_{gs1} = v_{out}\left(\frac{1}{r_{o1}} + \frac{1}{r_{o2}}\right) = v_{out}\left(\frac{r_{o1}+r_{o2}}{r_{o1}r_{o2}}\right) \tag{40}$$

Also,

$$v_{gs1} = v_{g1} - v_{s1} = v_{in} \tag{41}$$

If we substitute this into the KCL equation,

$$-g_{m1}v_{in} = v_{out}\left(\frac{r_{o1}+r_{o2}}{r_{o1}r_{o2}}\right) \tag{42}$$

Small-signal gain, $\frac{v_{out}}{v_{in}} = -\frac{g_{m1}r_{o1}r_{o2}}{r_{o1}+r_{o2}} = -g_{m1}(r_{o1}//r_{o2})$ [2 pts]

(d) Solve for the actual value of the small-signal gain. [1 pt]

We just substitute the values for the small-signal parameters we previously solved into the gain equation.

$A_v = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}r_{o1}r_{o2}}{r_{o1}+r_{o2}} = -\frac{(3.742mS)(20k\Omega)(40k\Omega)}{60k\Omega} = -49.893$ [1 pt]

(e) Calculate the minimum and maximum output voltage, $V_{OUT,min}$ and $V_{OUT,max}$, possible while keeping both M1 and M2 in saturation. [2 pts]

To determine the minimum and maximum output voltage, we should check the operation of transistors M1 and M2 when they are individually at the boundary of saturation and linear mode of operation.

If we assume that M1 is on the edge of the saturation and linear region of operation, then we can say that:

$$V_{GS1} - V_{th,n} = V_{DS1} = V_{OUT} \tag{43}$$

We can then write the current equation of M1,

$$I_{DS1} = k_n(V_{GS1} - V_{th,n})^2(1 + \lambda_n V_{DS1}) = k_n V_{DS1}^2(1 + \lambda_n V_{DS1}) \tag{44}$$

Replacing V_{DS1} with V_{OUT} and rewriting the equation:

$$k_n\lambda_n V_{OUT}^3 + k_n V_{OUT}^2 - I_{DS1} = 0 \tag{45}$$

With every other variables given, the equation above is a cubic function of V_{OUT} with three possible roots, $V_{OUT} = -9.993V$, $V_{OUT} = 0.264V$ and $V_{OUT} = -0.271V$. Of the three, the only possible value of the output voltage that could still manage to keep M1 saturated is:

$V_{OUT,min} = 0.264V$ [1 pt]

On the other hand, if we assume that M2 is on the edge of saturation and linear region of operation, then we can say that:

$$V_{SG2} - |V_{th,p}| = V_{SD2} \tag{46}$$

We can then write the current equation of M2,

$$I_{SD2} = k_p(V_{SG2} - |V_{th,p}|)^2(1 + \lambda_p V_{SD2}) = k_p V_{SD2}^2(1 + \lambda_p V_{SD2}) \tag{47}$$

Rewriting the equation:

$$k_p\lambda_p V_{SD2}^3 + k_p V_{SD2}^2 - I_{SD2} = 0 \tag{48}$$

With every other variables given, the equation above is a cubic function of V_{SD2} with three possible roots, $V_{SD2} = -19.948V$, $V_{SD2} = 0.996V$ and $V_{SD2} = -1.048V$. Of the three, the only possible value of V_{SD2} that still manages to keep M2 saturated is $V_{SD2} = 0.996V$.

$$V_{OUT,max} = V_{DD} - V_{SD2} = 3 - 0.996 = 2.004V \text{ [1 pt]}$$

(f) Assuming that M1 and M2 are biased properly, what is the maximum peak to peak input voltage, $v_{in,p-p}$ you can use and still keep both M1 and M2 in saturation? [1 pt]

In the previous problem, the maximum possible output swing that still keeps both transistors in saturation was solved. And since it is assumed that M1 and M2 are biased properly, we can determine the maximum peak to peak input voltage we can use by simply dividing the output swing we solved earlier by the gain of the circuit.

$$v_{in,p-p} = \frac{V_{OUT,max} - V_{OUT,min}}{|A_v|} = \frac{2.004 - 0.264}{49.893} \tag{49}$$

$$V_{in,p-p} = 34.875mV_{p-p} \text{ [1 pt]}$$

3. **Introduction to Current Mirrors**. In reality, we do not have ideal current sources. So we use circuits that behave approximately like current sources such as current mirrors. The circuit diagram of a current mirror is shown in Figure 6. By varying the value of resistor R_1, the current and the bias voltage (V_{GS_1}) of transistor M_1 can be varied. Since the gates of M_1 and M_2 are connected, the gate voltages of the two transistors are equal. Therefore, by changing the resistance of R_1, we can control the gate voltage of M_2 which controls the drain current of M_2. This operation makes the current mirror behave like a variable current source.
Given that $V_{DD} = 12V$, $k_p = k_n = \frac{1\,\text{mA}}{V^2}$, $V_{TH,n} = 3V$, $V_{TH,p} = -2.5V$, $\lambda_n = 0.1V^{-1}$, $\lambda_p = 0.05V^{-1}$.

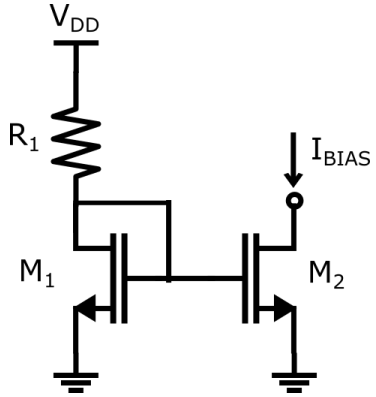

Figure 6: Current Mirror Circuit Diagram

(a) If the value of R_1 is $1\,\text{k}\Omega$, what is the gate-source voltage of transistor M_2?
Assuming that transistor M_1 is in saturation, and assuming no channel length modulation for the calculation of bias currents,

$$I_{DS,1} = k_n(V_{GS,1} - V_{TH,n})^2 \tag{50}$$

Since $I_{DS,1} = I_{R_1}$, and $I_{R_1} = \frac{V_{DD} - V_{GS,1}}{R_1}$,

$$\frac{V_{DD} - V_{GS,1}}{R_1} = k_n(V_{GS,1} - V_{TH,n})^2 \tag{51}$$

By substituting the given values,

$$\frac{12 - V_{GS,1}}{1000} = 0.001(V_{GS,1} - 3)^2 \tag{52}$$

$$V_{GS,1} = 5.541V \tag{53}$$

Check if M_1 is indeed in saturation:

$$V_{DS,1} > V_{GS,1} - V_{TH,n} \tag{54}$$

$$V_{DS,1} = V_{GS,1} \tag{55}$$

$$5.541 > 5.541 - 2 = 2.541 \tag{56}$$

M_1 is in saturation.

$V_{GS,1} = 5.541V$ [1 pt]

(b) What is the value of I_{BIAS}, assuming that M_2 is in saturation?
Since the gates of M_1 and M_2 are connected, $V_{GS,1} = V_{GS,2}$. Therefore, the drain current of M2 is given by (assuming no channel length modulation):

$$I_{BIAS} = I_{DS,2} = k(V_{GS,2} - V_{TH,n})^2 = 0.001(5.541 - 3)^2 \tag{57}$$

$I_{BIAS} = 6.456mA$ [1 pt]

(c) Draw the small-signal model of the current mirror. Label all transistor terminals and all small-signal parameters. [2 pts]

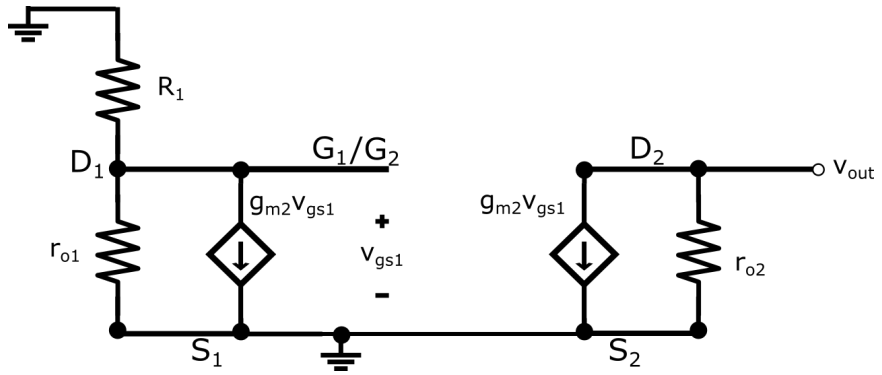

Figure 7: Complete small signal model of the current mirror.

Since we know that there are no small signal in the current mirror (purely DC), we can reduce v_{gs} to 0 and this will eliminate all the dependent current sources. Due to this, we can simplify the small signal model to:

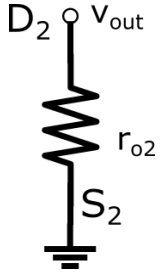

Figure 8: Simplified small signal model of the current mirror.

Calculating for the values of the small signal parameters,

$$r_{o1} = r_{o2} = \frac{1}{\lambda_n I_{DS,2}} = \frac{1}{\lambda_n I_{BIAS}} = \frac{1}{(0.1)(6.456mA)} = 1548.95\,\Omega \text{ [1 pt]}$$

$$g_{m1} = g_{m2} = \sqrt{4k_n I_{DS}} = \sqrt{4(0.001)(0.006456)} = 5.08\,\text{mS} \text{ [1 pt]}$$

(d) What is the small-signal output resistance, r_o, of the current mirror?

$$r_o = \frac{1}{\lambda_n I_{DS,2}} = \frac{1}{\lambda_n I_{BIAS}} = \frac{1}{(0.1)(6.456mA)} = 1548.95\,\Omega \text{ [1 pt]}$$

(e) A PMOS common-source amplifier with current mirror biasing is shown in Figure 11. If we use the I_{BIAS} in (b), draw the small signal model of the amplifier. Label all transistor terminals and small-signal parameters with your calculated values. [3 pts]

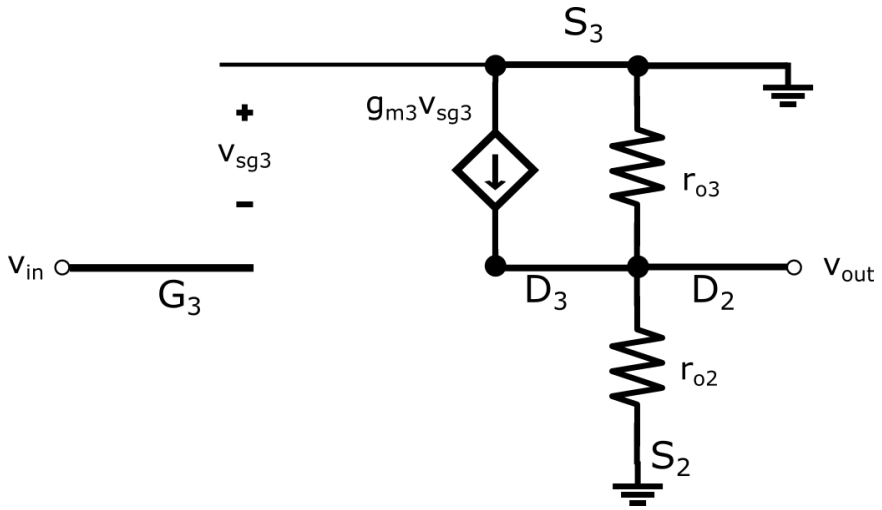

Figure 9: Small signal model of NMOS current mirror-loaded PMOS CS amplifier.

$$r_{o3} = \frac{1}{\lambda_p I_{DS,2}} = \frac{1}{\lambda_p I_{BIAS}} = \frac{1}{(0.05)(6.456mA)} = 3097.89\,\Omega \text{ [1 pt]}$$

$$g_{m3} = \sqrt{4k_p I_{DS}} = \sqrt{4(0.001)(0.006456)} = 5.08\,\text{mS} \text{ [1 pt]}$$

(f) What is the small-signal gain, A_V, of the CS amplifier?

$$R_o = r_{o2} || r_{o3} = 3097.82 || 1548.95 = 1032.63\,\Omega \tag{58}$$

$$A_V = -G_m R_o = -g_{m,3} R_o = (5.0814mS)(1032.63\Omega) = -5.247 \text{ [1 pt]}$$

(g) What is the maximum output swing of the common emitter amplifier such that the transistor remains in saturation?

The output swing is determined by the maximum and minimum output voltages such that transistors M_1 and M_2 remains in saturation.

For transistor M_2, the gate source voltage is constant. Therefore, it is easy to determine what output voltage would keep transistor M_2 in saturation.

$$V_{out} = V_{DS,2} \geq V_{GS,2} - V_{TH,n} \tag{59}$$

$$V_{DS,2} = V_{GS,2} - V_{TH,n} = 5.541 - 3 = 2.541V \tag{60}$$

For M_3, the source-gate voltage, V_{SG}, at the specific bias current is 5.041 V. So in order to keep the transistor in saturation,

$$V_{SD,3} \geq V_{SG,3} - |V_{TH,p}| \tag{61}$$

$$V_{SD,3} = V_{GS,3} - |V_{TH,p}| = 5.041 - 2.5 = 2.541V \tag{62}$$

$$V_{out} = V_{DD} - V_{SD,3} = 12 - 2.541 = 9.459V \tag{63}$$

$2.541V < V_{out} < 9.459V$ [1 pt]

(h) Plot V_{IN} vs. V_{OUT} of the common-source amplifier. [2 pts]

In fig. 10, the vertical axis is V_{out}, and the horizontal axis is V_{in}. We know that M_2 is always on since $V_{gs,2}$ is always greater V_{TH}. So, in order to APPROXIMATE the voltage transfer characteristic of the CS amplifier, we must characterize the behavior of M_3. When the input voltage is very low (I), the PMOS transistor is fully turned on, therefore it approximately serves as a short circuit to V_{DD}. At very high voltages (II), the PMOS transistor will turn off since $V_{sg,3} < |V_{th,3}|$. Since M_2 is turned on, it will serve as a path to ground. Effectively pulling the output node to ground. At middle voltages, both transistors will be in saturation, and this is where we want our amplifier to operate. The slope of the line will give us the gain of the amplifier. It has be emphasized that this graph is just an approximation. In order accurately construct the voltage transfer curve, we have to determine the operating points of the transistors where they will have equal currents while also considering channel length modulation.

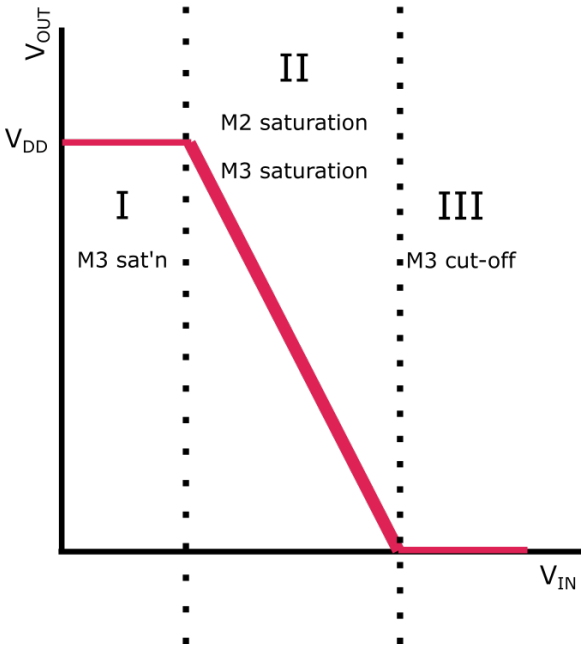

Figure 10: Approximate voltage transfer curve of CS amplifier.

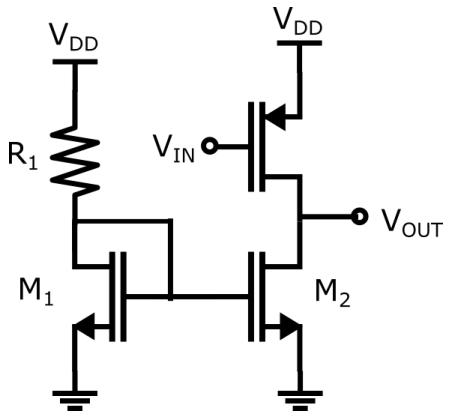

Figure 11: Common Source amplifier with current mirror biasing

TOTAL: 32/32 points.