EEE 51 Assignment 10

2nd Semester SY 2017-2018
Due: 5pm Thursday, May 17, 2018 (Rm. 220)

Instructions: Write legibly. Show all solutions and state all assumptions. Write your full name, student number, and section at the upper-right corner of each page. Start each problem on a new sheet of paper. Box or encircle your final answer.

Answer sheets should be color coded according to your lecture section. The color scheme is as follows:

THQ – yellow
THR – blue
THU – white
THX – green
WFX – pink

1. **BJT common-collector amplifier.** Given the amplifier below with $I_{C,Q1} = 50mA$, $V_A = 200V$, $\beta = 150$, $V_{CC} = 5V$, $R_E = R_S = 100\Omega$, and $C_1 = 10pF$, solve for the following:

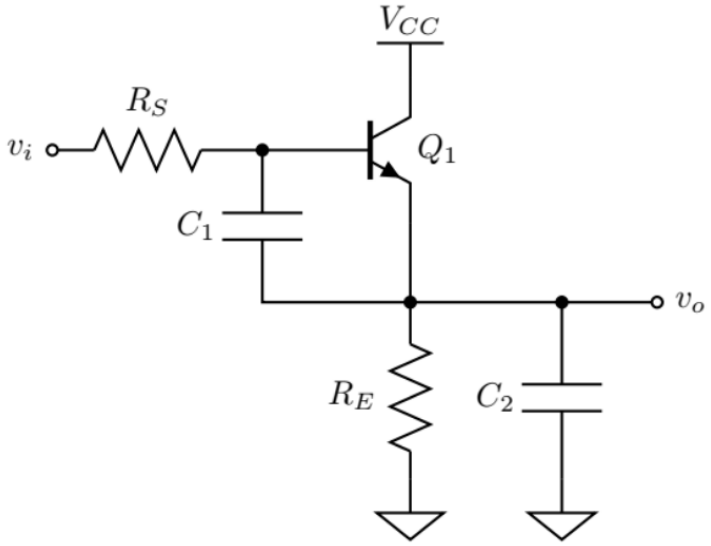

Figure 1

   (a) Draw the small-signal model and redraw the circuit for feedback. Find the feedback factor F. [2 pts]
   (b) Find the value of C_2 such that the phase margin is 60°. [2 pts]
   (c) Find the value of C_2 such that the phase margin is 45°. [2 pts]
   (d) For a phase margin of 45°, find the loop gain $T(s)$ and closed loop gain $A_{CL}(s) = \frac{v_o}{v_i}$. What are the values of T_0 and A_{v0}? [2 pts]
   (e) Plot the magnitude and phase response of the circuit as a function of frequency. [2 pts]

2. **Unity-Gain Feedback.** In order to design a larger, multi-stage amplifier, the common BJT to be used for the stages is placed under a simple test to characterize some performance basics.

   The single NPN Q_1 under test is placed in common-emitter (as seen in Figure 2a) and is loaded at the input and output with capacitors C_i and C_L to simulate expected loading in between stages. The common-emitter is constructed with an ideal current source to bias it. Unity-gain feedback is achieved by using an ideal summing amplifier, which also takes care of the quiescent input current to match the bias created by the

ideal current source. This setup is as shown in Figure 2b. For all intents and purposes there is no other output load than the load capacitor C_L and the input should be treated as ideal, trusting in this summing amplifier and not loading this system any further.

Q_1 has known and finite values of V_A, V_T at the operating temperature, as well as β. The bias current I_C can be set and is chosen to be some starting value that ensures that Q_1 is in forward-active.

For the following questions, express all values asked for in terms of I_C, V_A, V_T, β, and C_i. You may assume that parasitic capacitances are negligible for this setup when calculating for the values asked for.

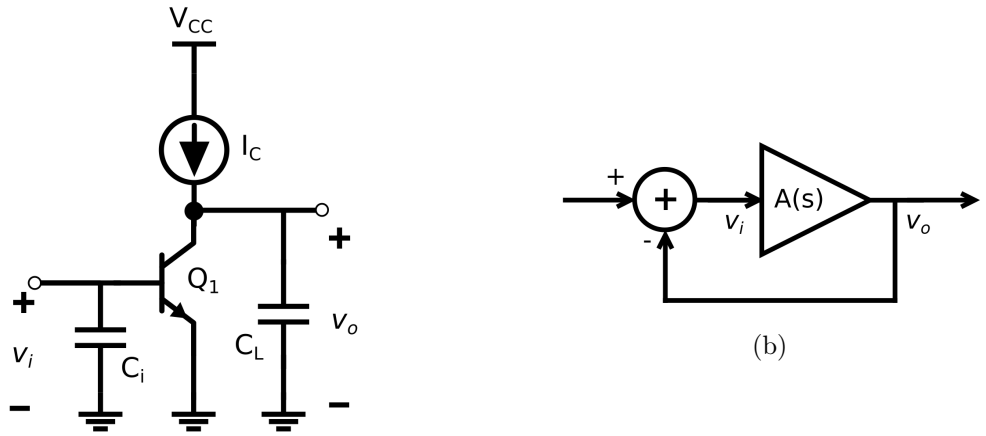

Figure 2: Common-emitter amplifier in unity-gain feedback.

(a) What is the gain of the amplifier at DC? [1 pt]

(b) This amplifier is intended to be loaded such that the phase margin is at 90°. C_i is already at the minimum and cannot be changed; C_L is already at the same capacitance as C_i but can be increased. What should the value of C_L be in order to meet this phase margin? Assume that the output pole created by C_L should have a frequency smaller than the input pole. [2 pts]

(c) The bandwidth is determined by the location of the first pole with the smallest frequency, in order to approximate the -3 dB point. What is the bandwidth? [1 pt]

(d) In this setup, what is the trade-off between the gain-bandwidth product and power consumption? [2 pts]

(e) Since C_L is now at the proper value for a 90° phase margin to be achieved for some bias point generated by I_C, if I_C had to be changed later on, how would the phase margin change? [1 pt]

(f) In constructing a multi-stage amplifier in a manner similar to this, would it make sense to follow this setup such that poles nearer to the output have a lower pole frequency than the ones at the input? Or is the opposite true, or does it not matter? Explain. [2 pts]

(g) Suppose the concept of a multi-stage amplifier now upsets you, and you attempt instead to construct a Cascode amplifier in an attempt to bypass the problem of having loading between stages. What are the trade-offs, frequency response-wise, in doing so? [1 pt]

3. Given the circuit with the parameters below, solve for the following:

$V_{DD} = 5V$, I_{M8}=5pA , $k_{1,2} = 2.5\frac{pA}{V^2}$, $k_{3,4} = 3.75\frac{pA}{V^2}$, $k_{5,6,7,9} = 2.5\frac{nA}{V^2}$, $k_8 = 5\frac{pA}{V^2}$, $\lambda = 0.01V^{-1}$, $C_L = 5 * 10^{-21}F$, $C_{L2} = 500 * 10^{-24}F$, and $|V_{TH_{n|p}}| = 1V$

Assume that the compensating capacitances have no effect on the analysis of the first stage and is purely for the 2nd stage and that $C_M >> C_{L2}$

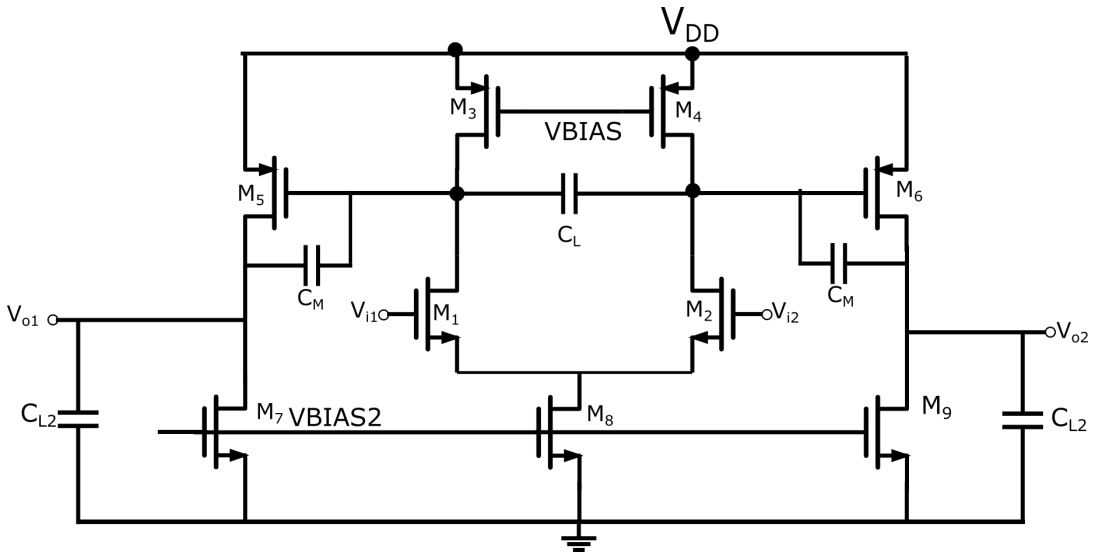

Figure 3

(a) Plot the magnitude and phase response of the amplifier. When $C_M = 0$ [2.5 pts]

(b) Solve for the poles, zero and $A_{total}(s)$ equations.[2.5 pts]

(c) Compute the necessary C_M to achieve a 45° phase margin at the w_p of the first stage. [2.5 pts].

(d) Plot the new magnitude and phase response. [2.5 pts]

TOTAL: 30 points.