EEE 51: Second Semester 2017 - 2018

Lecture 3

Two-Port Networks

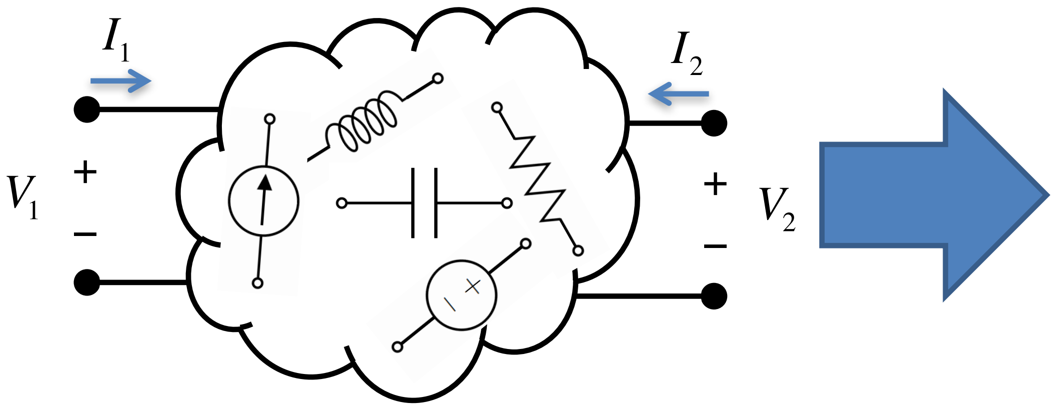
Single-Stage Amplifiers

Today

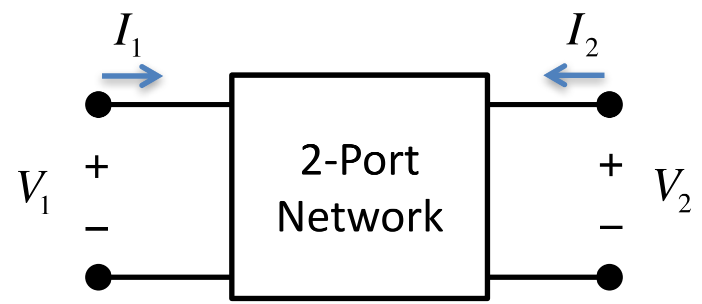
- Two-Port Networks
- Single-Stage Amplifiers

Two-Port Network Reduction

- Can reduce any linear circuit into 4 parameters



Linear → R, L, C, dependent sources



Given 2 terminal parameters (V or I), we can get the other 2 (V or I)

How convenient are these representations for EEE 51?

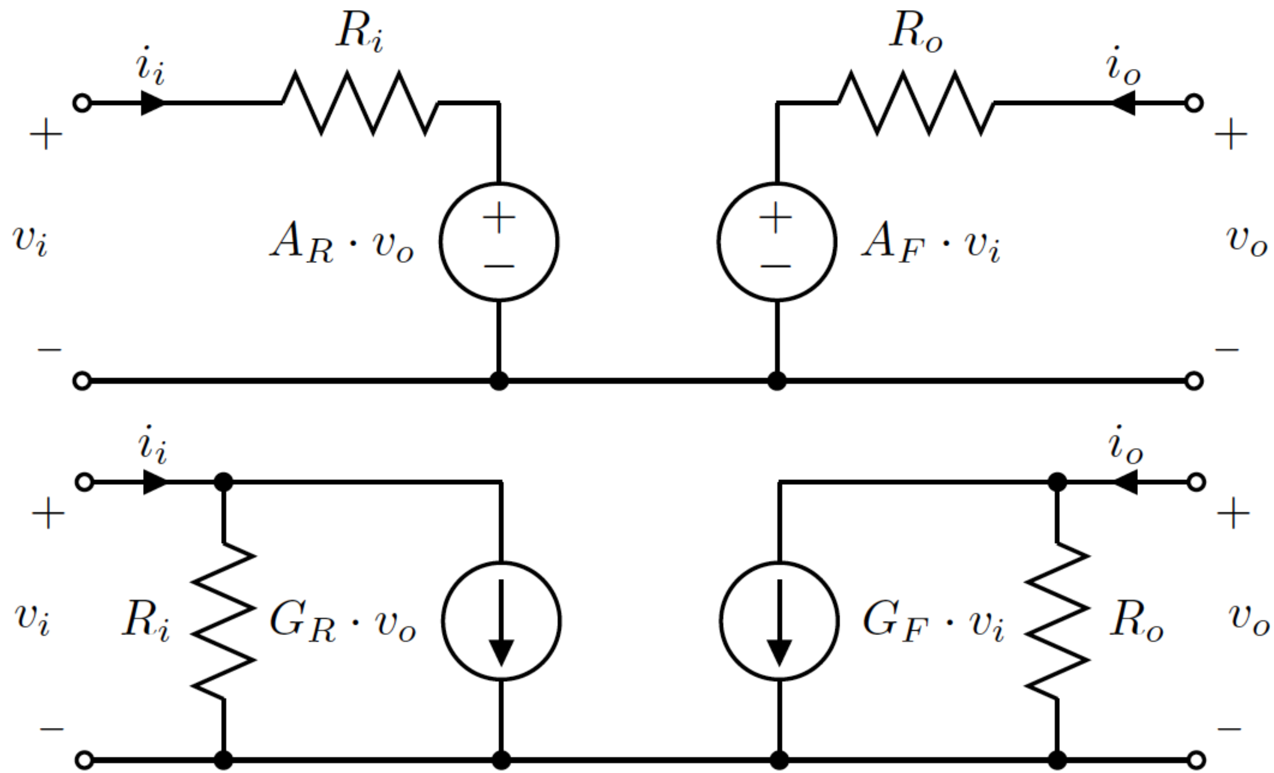
$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

The Bilateral Hybrid-π Two-Port Network

Thevenin equivalent:

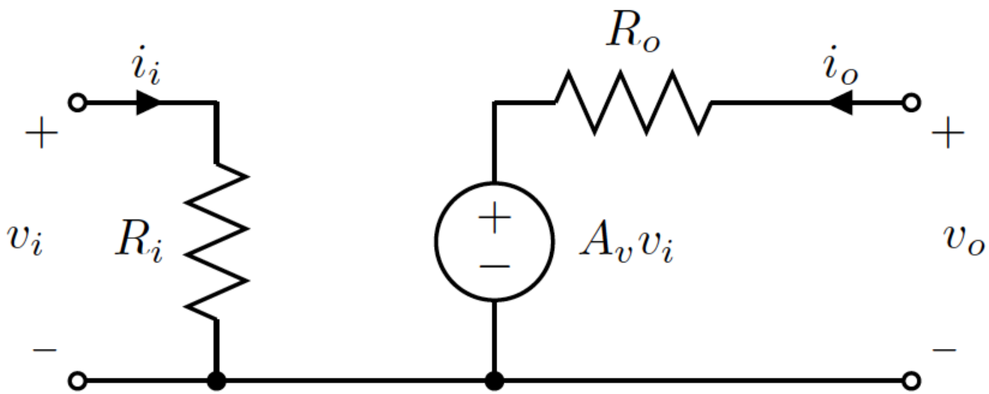
Norton equivalent:



Unilateral equivalents?

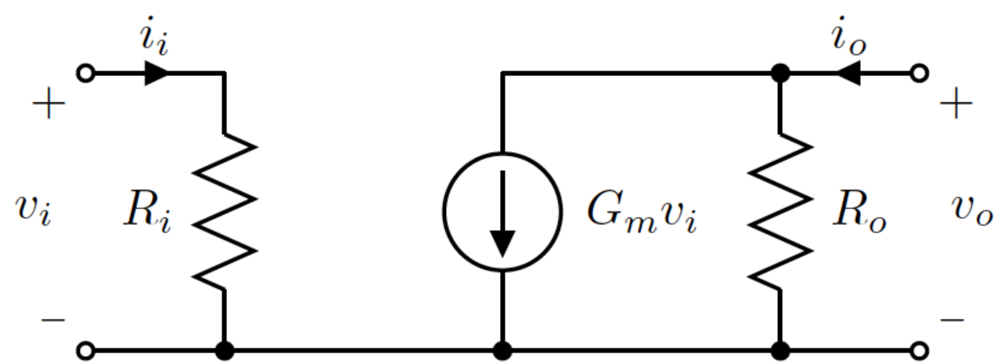
The Unilateral Hybrid-π Two-Port Network

- Requires only 3 parameters



The Thevenin Equivalent
(R_i, A_v, R_o)

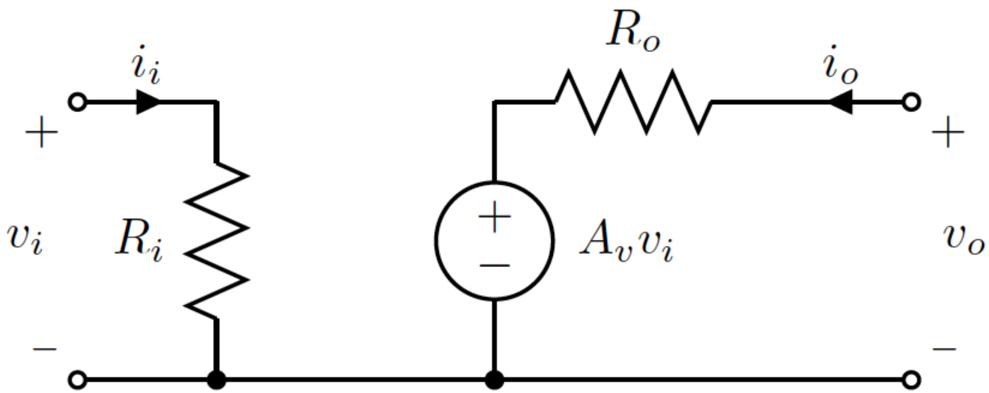
The Norton Equivalent
(R_i, G_m, R_o)



Looks very familiar…

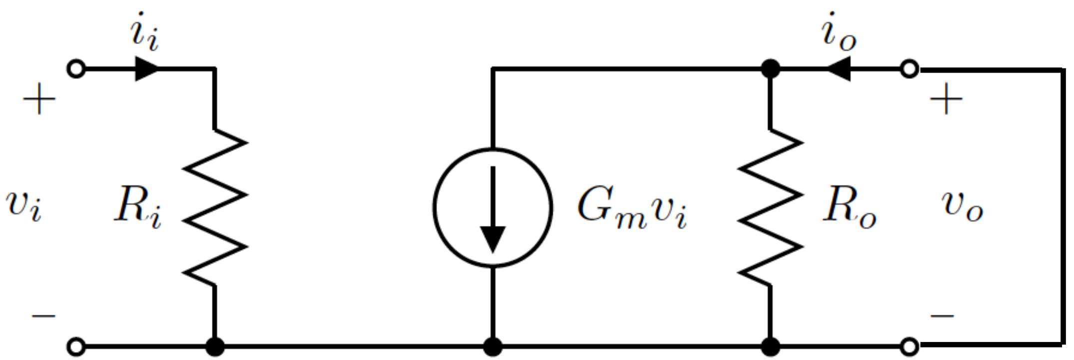
Operating Conditions (1)

- **No-Load → No power draw at the output**



Open circuit

$i_o = 0$

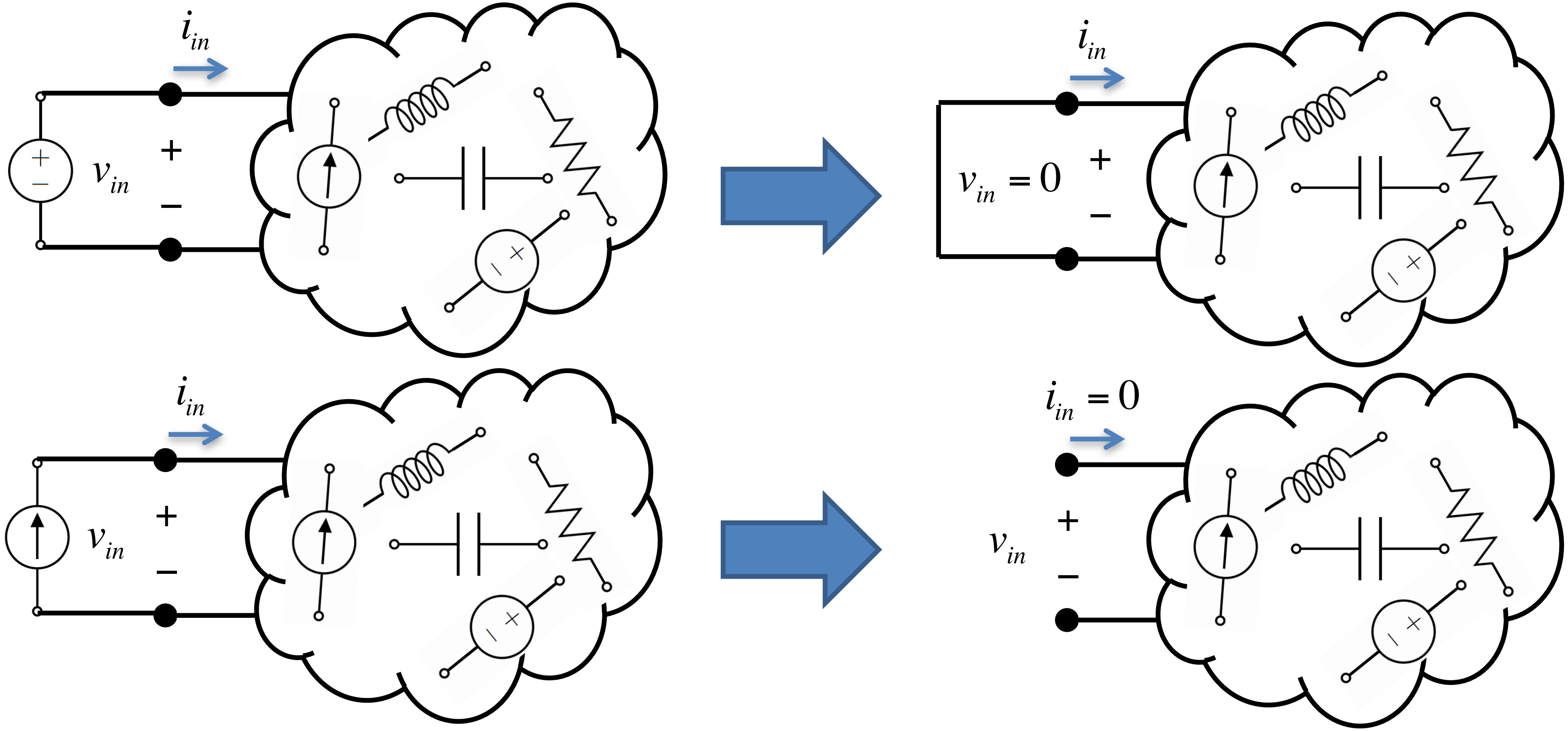


Short circuit

$v_o = 0$

Operating Conditions (2)

- **Zero-Input** → No excitation at the input

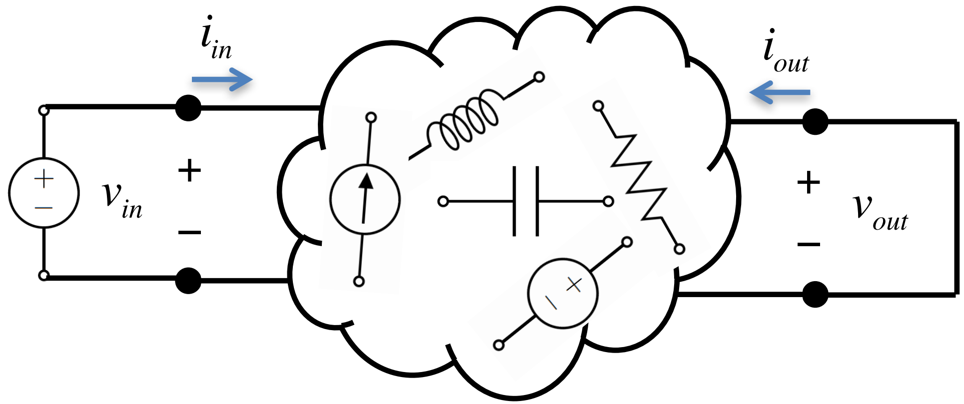


Solving for the Hybrid-π Parameters (1)

- Circuit Transconductance

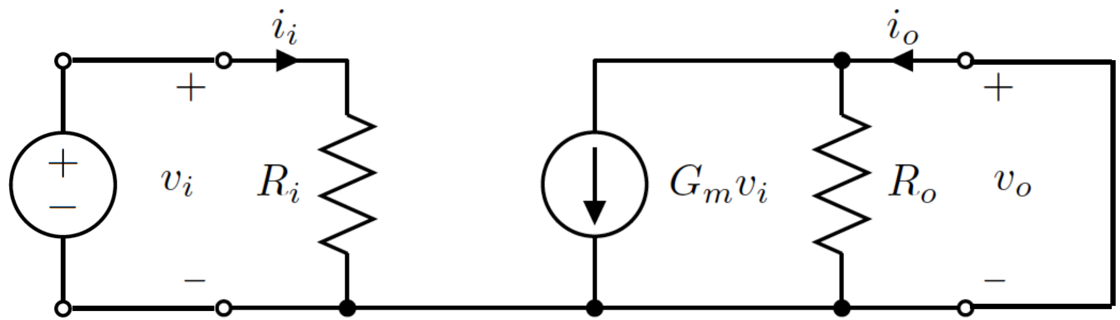
Solving for G_m:

$$G_m = \left.\frac{i_{out}}{v_{in}}\right|_{\text{no-load}}$$



No-load

$v_{out} = 0$

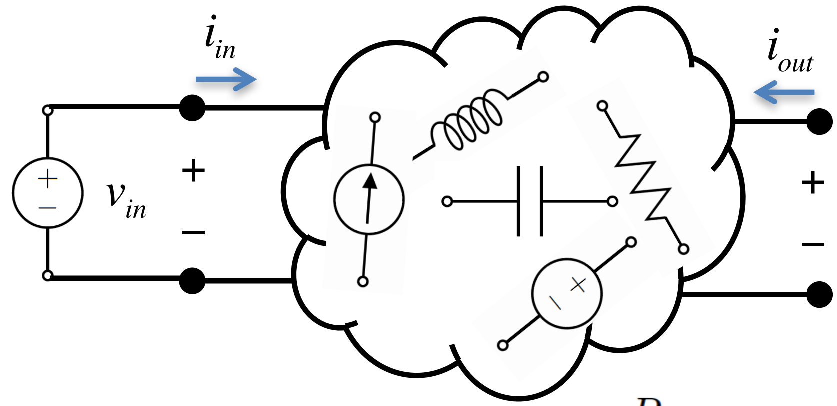


Solving for the Hybrid-π Parameters (2)

- Circuit Voltage Gain

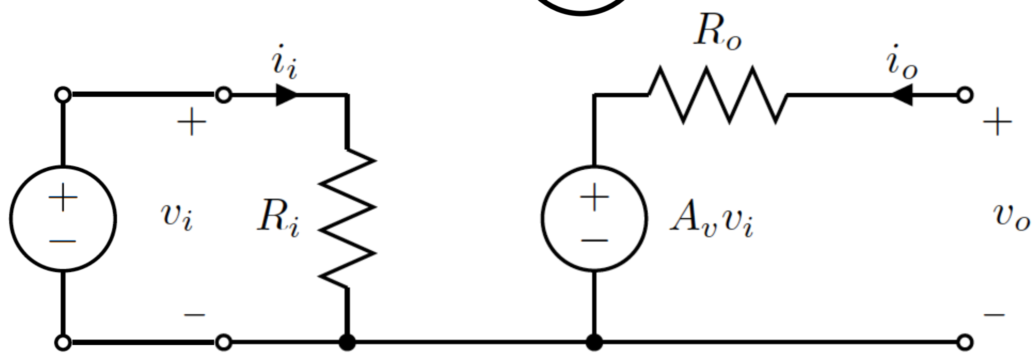
Solving for A_v:

$$A_v = \left.\frac{v_{out}}{v_{in}}\right|_{\text{no-load}}$$



No-load

$i_{out} = 0$



Solving for the Hybrid-π Parameters (3)

- Circuit Output Resistance

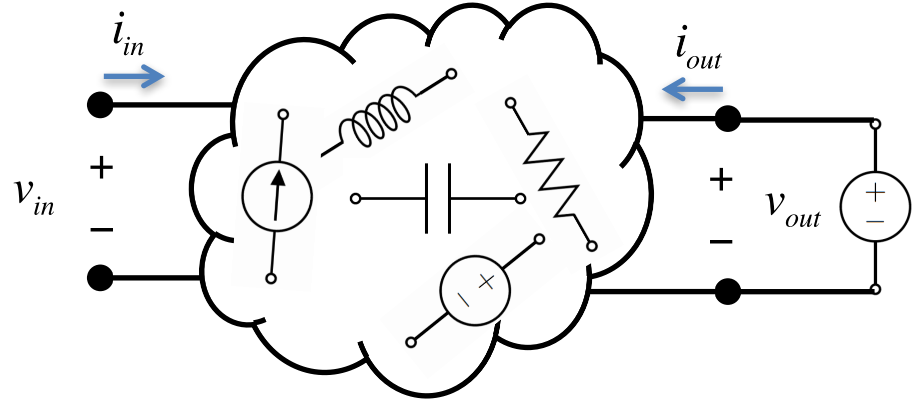
Solving for R_o:

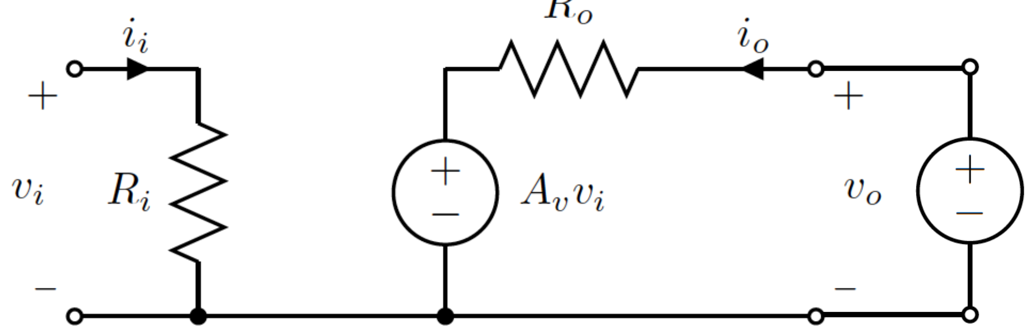
$$R_o = \left.\frac{v_{out}}{i_{out}}\right|_{\text{zero-input}}$$

Zero-input

$i_{in} = 0$ or

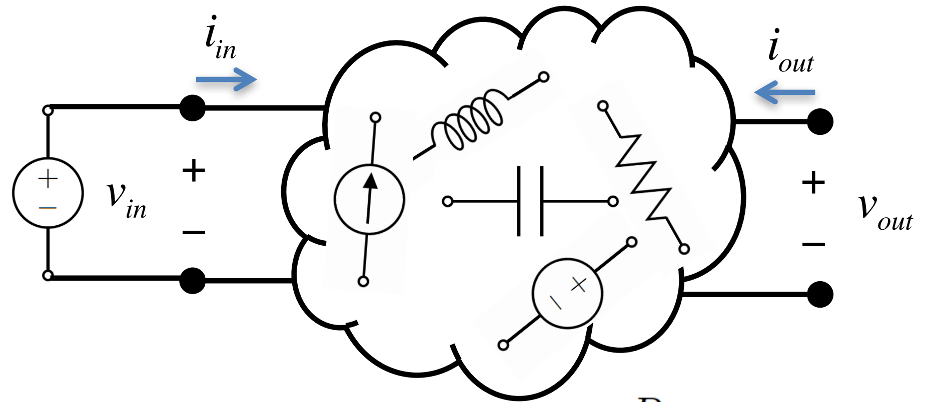
$v_{in} = 0$





Solving for the Hybrid-π Parameters (4)

- Circuit Input Resistance

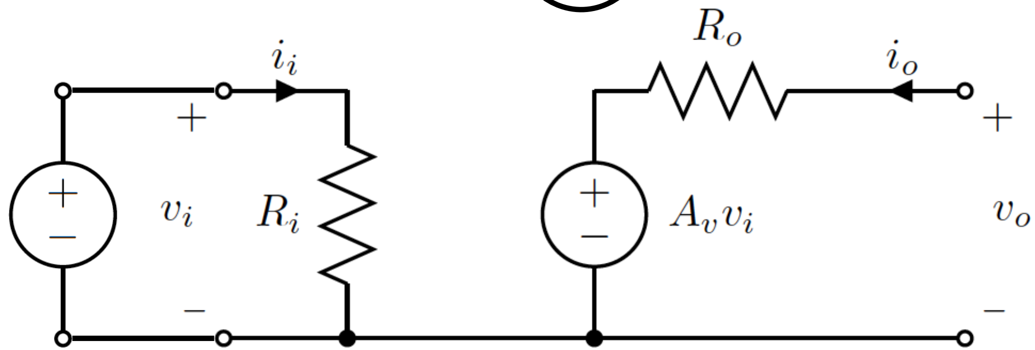


No-load

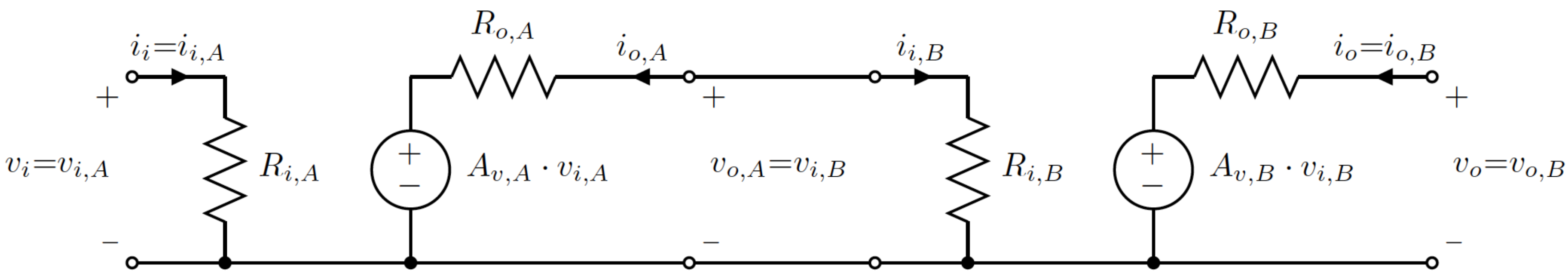
$i_{out} = 0$

Solving for R_i:

$$R_i = \left. \frac{v_{in}}{i_{in}} \right|_{\text{no-load}}$$

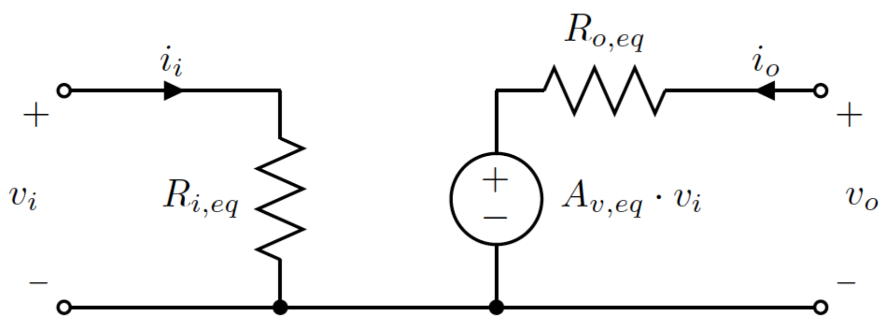


Cascading Two-Port Networks



Circuit A

Circuit B



$$A_{v,eq} = A_{v,A} \cdot \frac{R_{i,B}}{R_{i,B} + R_{o,A}} \cdot A_{v,B}$$

$$R_{i,eq} = R_{i,A}$$

$$R_{o,eq} = R_{o,B}$$

Equivalent 2-Port Circuit taking into account **loading effects**

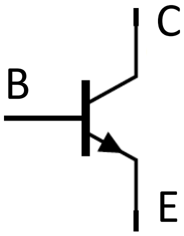
So Far…

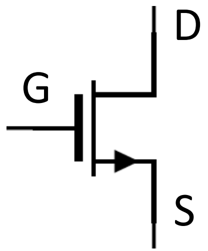
- We can analyze small signals separately from large signals

- We can use 2-port networks to reduce/combine small signal circuits

- Let’s look at the small signal behavior of our basic electronic circuit building blocks:
  - Single-stage amplifiers

Choices:



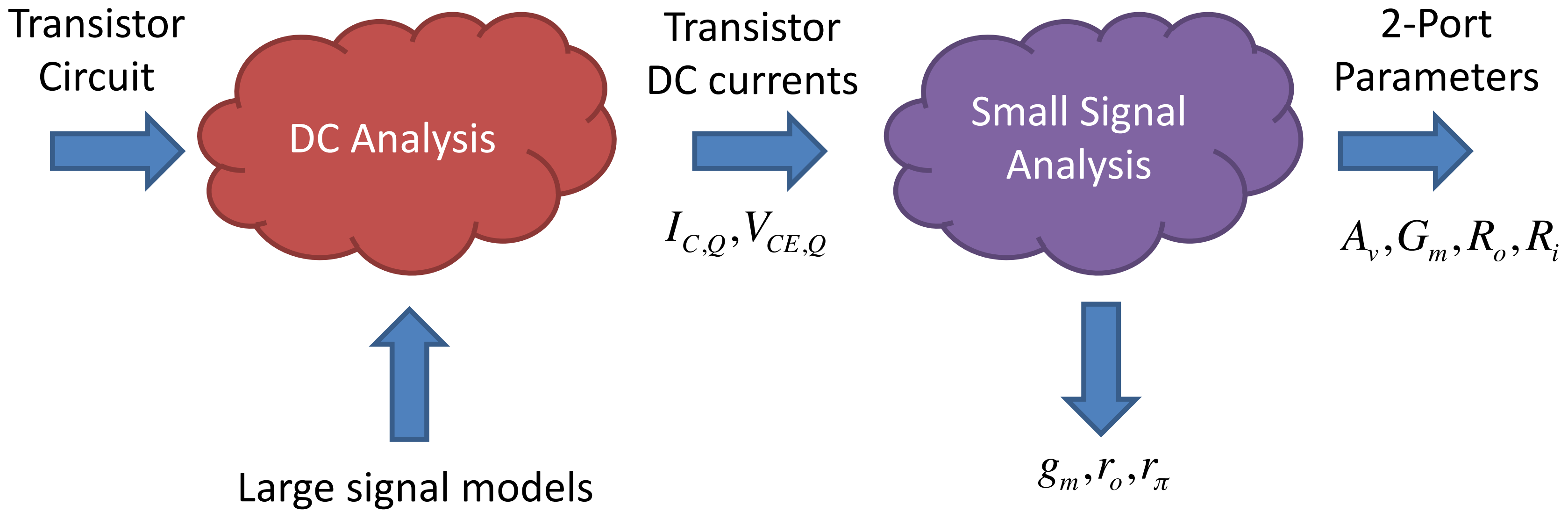


Where do we put in the input?

Where do we get the output?

Where do we start?

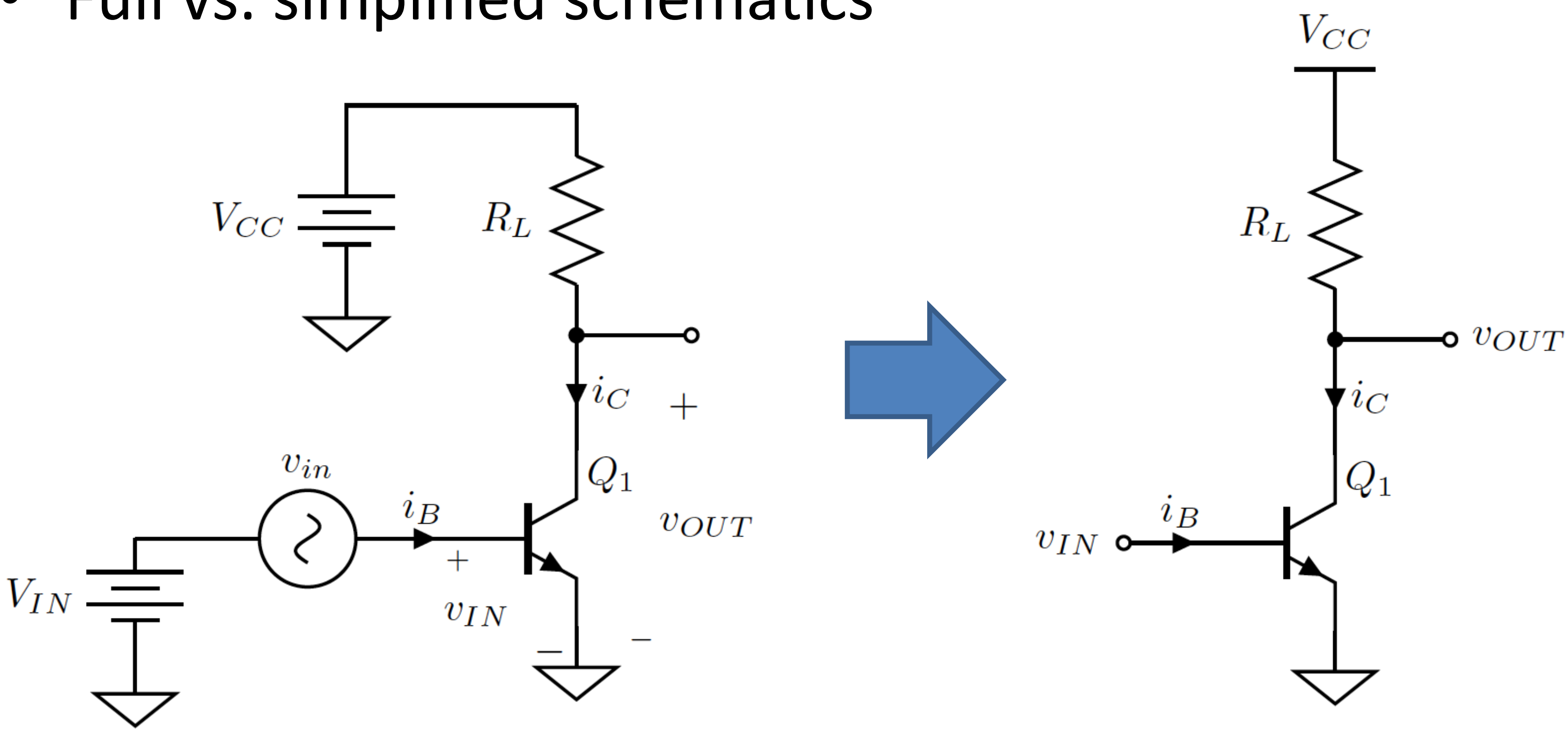
Transistor Amplifier Analysis



$$I_C = I_S\left(e^{\frac{V_{BE}}{V_T}} - 1\right)\left(1 + \frac{V_{CE}}{V_A}\right)$$

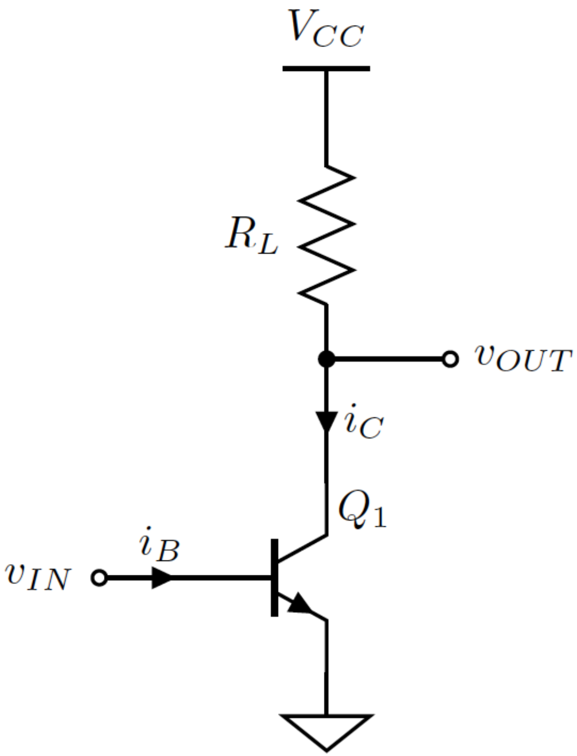
The Basic Common-Emitter (CE) Amplifier

- Full vs. simplified schematics



Common-Emitter DC Analysis

- Objective: Determine $I_{C,Q}$



KVL equations → 2 equations, 2 unknowns (assumptions?)

$$V_{CC} - I_{C,Q}R_L - V_{CE,Q} = 0$$

$$I_{C,Q} = I_S\left(e^{\frac{V_{IN}}{V_T}} - 1\right)\left(1 + \frac{V_{CE,Q}}{V_A}\right)$$

In most cases, we will deal with: $V_{OUT} = V_{CE,Q} << V_A$

Thus,

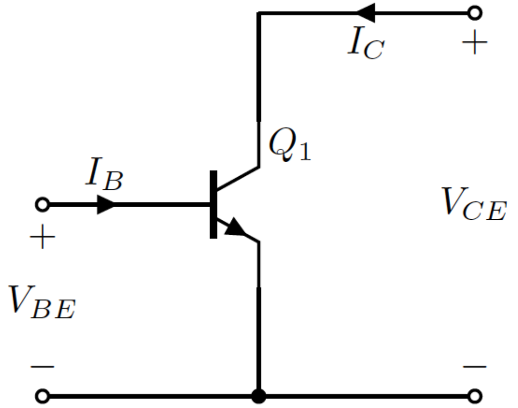
$$I_{C,Q} = I_S\left(e^{\frac{V_{IN}}{V_T}} - 1\right)$$

$$V_{OUT} = V_{CC} - I_{C,Q}R_L$$

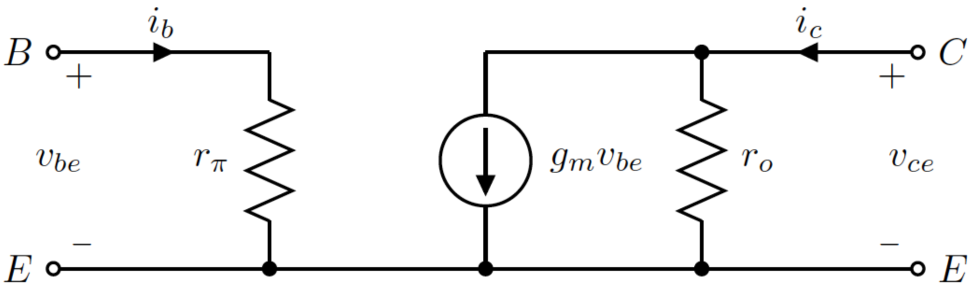
$$= V_{CC} - R_L I_S\left(e^{\frac{V_{IN}}{V_T}} - 1\right)$$

Common-Emitter Amplifier Small Signal Analysis

- Given $I_{C,Q}$:



$$r_\pi = \frac{\beta \cdot V_T}{I_{C,Q}} \qquad g_m = \frac{I_{C,Q}}{V_T} \qquad r_o = \frac{V_A}{I_{C,Q}}$$

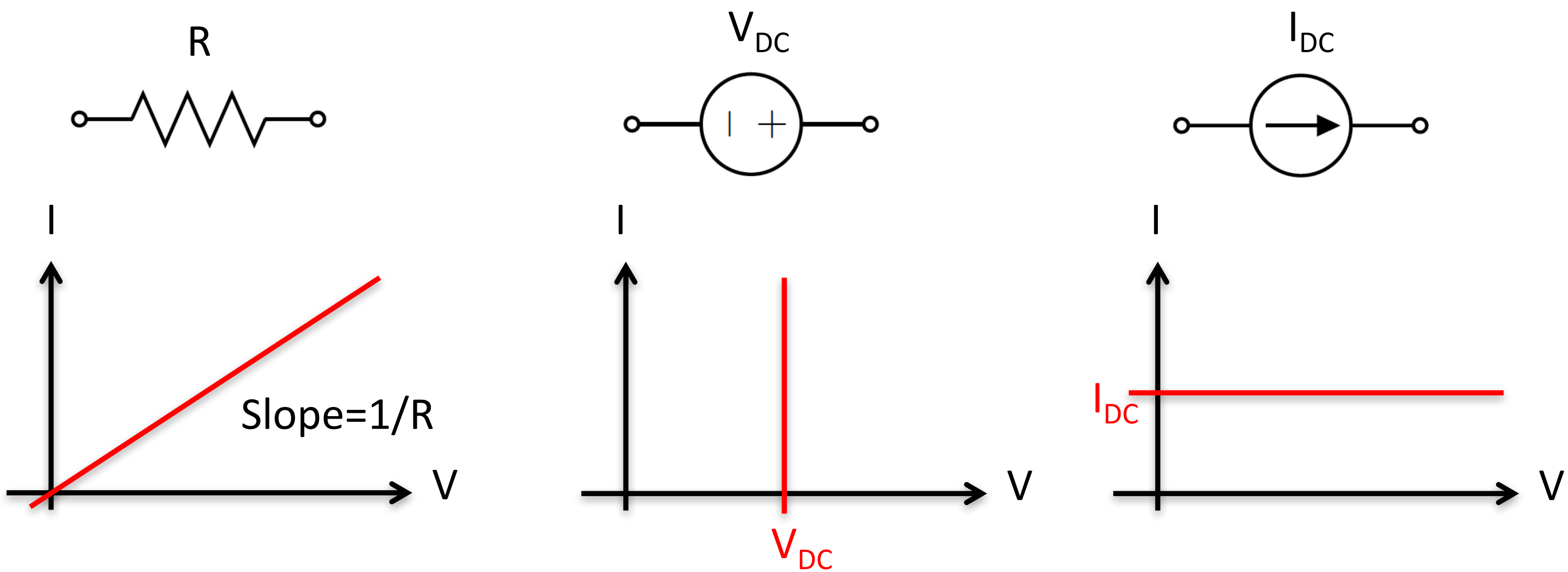


What about the other circuit elements?

- Resistors
- Independent voltage/current sources

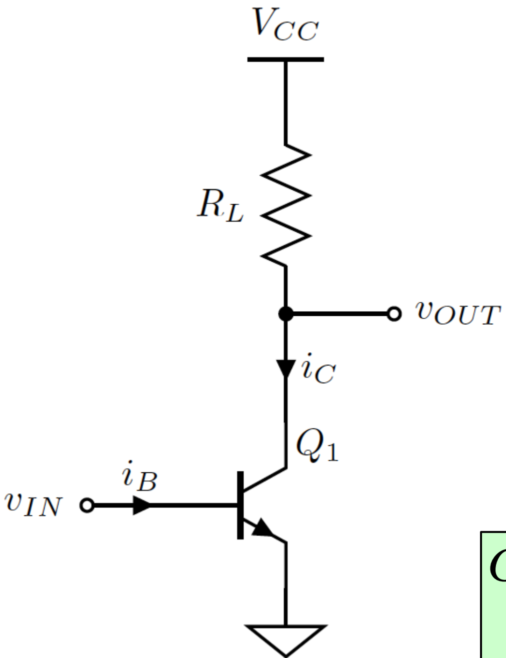
Linear Two-Terminal Devices

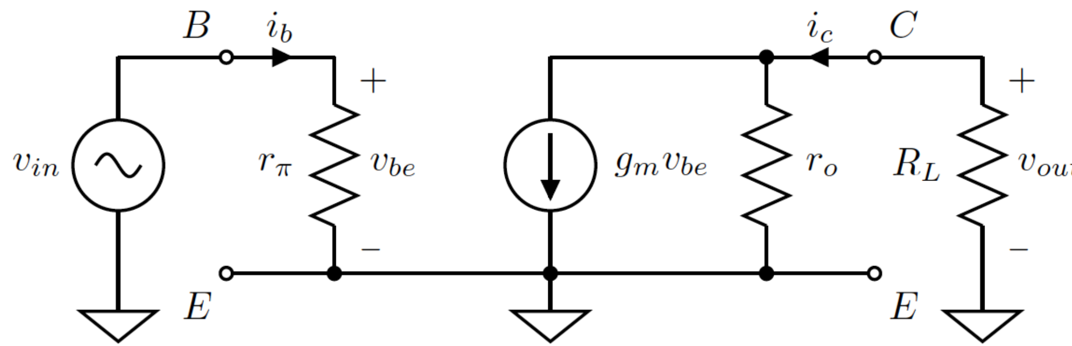
- Small signal conductance / resistance: $R_{\text{small signal}} = \dfrac{\partial V}{\partial I}$

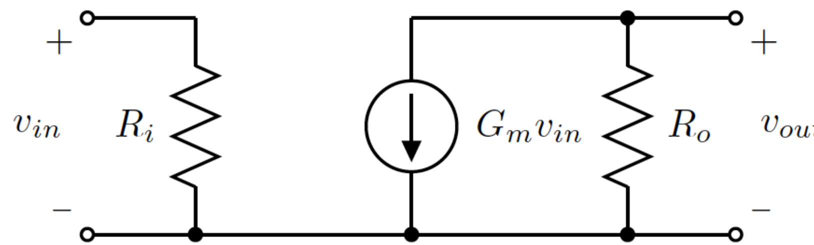


$R_{\text{small signal}} = R$ $\qquad$ $R_{\text{small signal}} = 0$ $\qquad$ $R_{\text{small signal}} \to \infty$

CE Amplifier Small Signal Equivalent Circuit





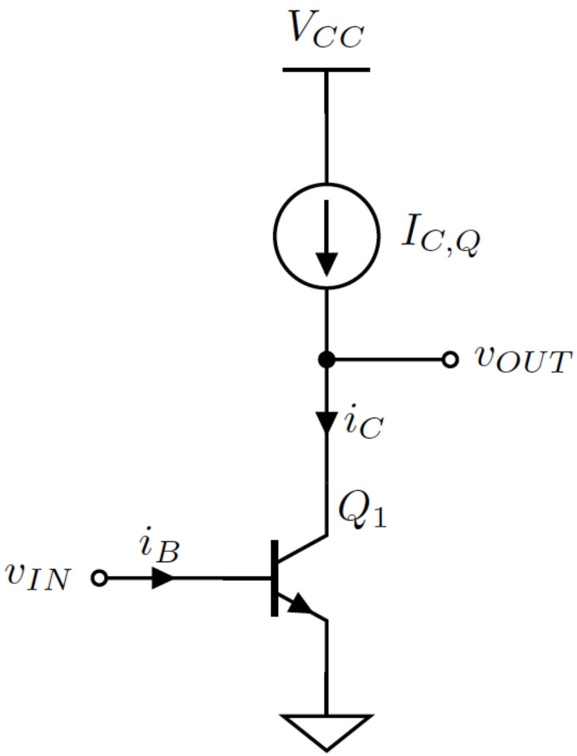


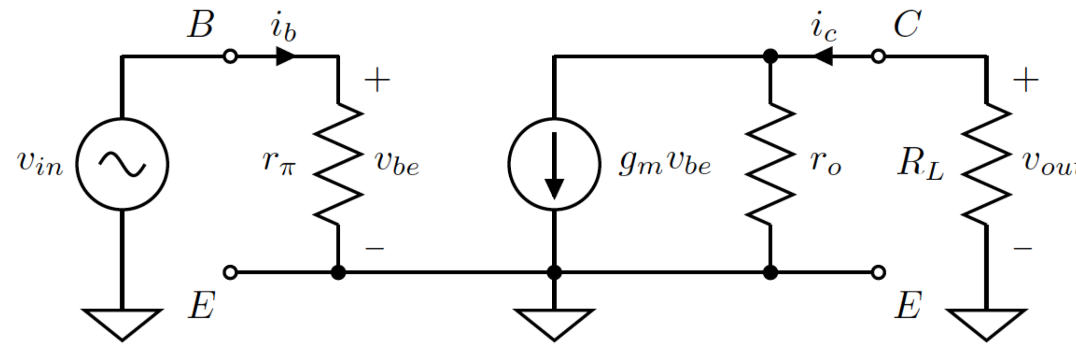
"inverting amplifier"

$$
\begin{aligned}
G_m &= g_m \\
R_i &= r_\pi \\
R_o &= r_o \parallel R_L \\
A_v &= -G_m R_o \\
&= -g_m \left(r_o \parallel R_L \right)
\end{aligned}
$$

Define: Intrinsic Transistor Gain (a_o)

- Ideal bias circuit:





$$G_m = g_m$$
$$R_i = r_\pi$$
$$R_o = r_o$$
$$A_v = -G_m R_o = -g_m r_o = a_o$$

$R_L \rightarrow \infty$

Why?

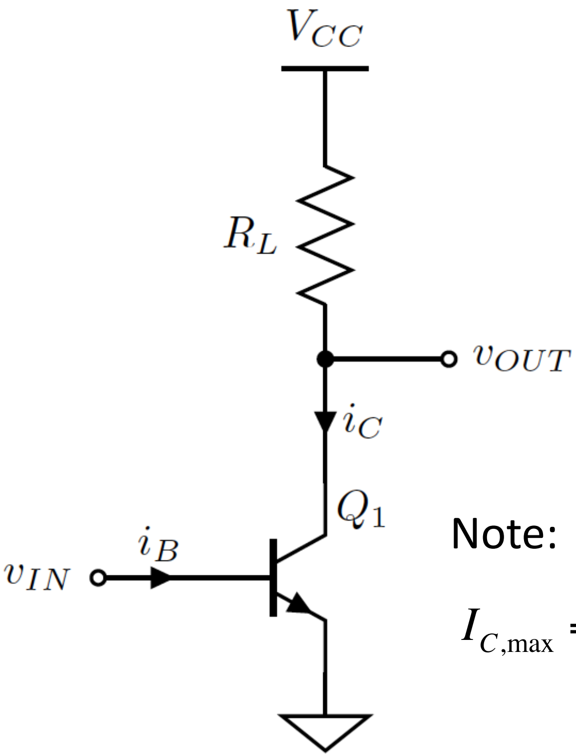
a_o → largest voltage gain out of a single transistor

$$a_o = -g_m r_o = -\frac{I_{C,Q}}{V_T} \cdot \frac{V_A}{I_{C,Q}} = -\frac{V_A}{V_T} = -\frac{q \cdot V_A}{kT}$$

How do we interpret voltage gain?

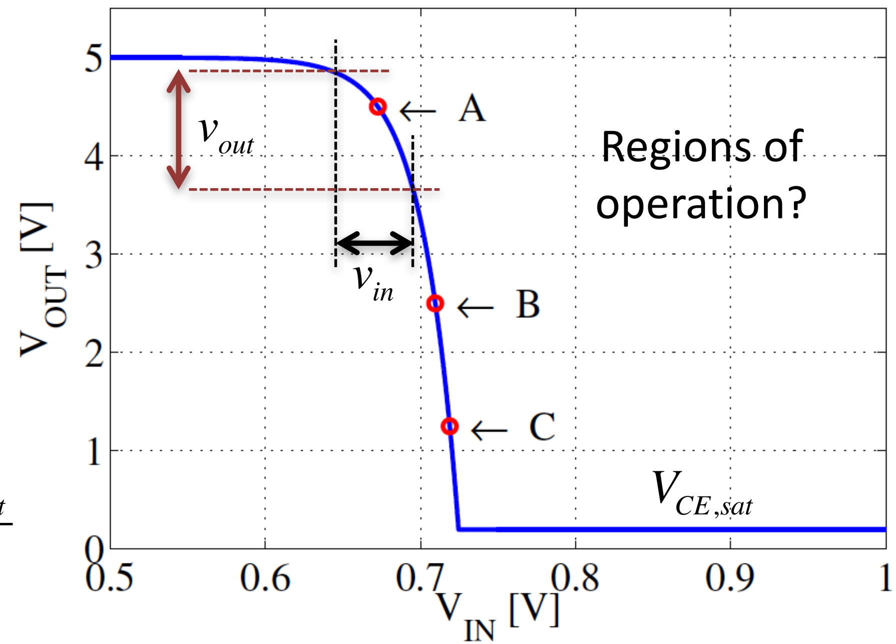
- Large signal transfer characteristic:

$$V_{OUT} = V_{CC} - R_L \cdot I_S \cdot e^{\frac{V_{IN}}{V_T}}$$



Note:

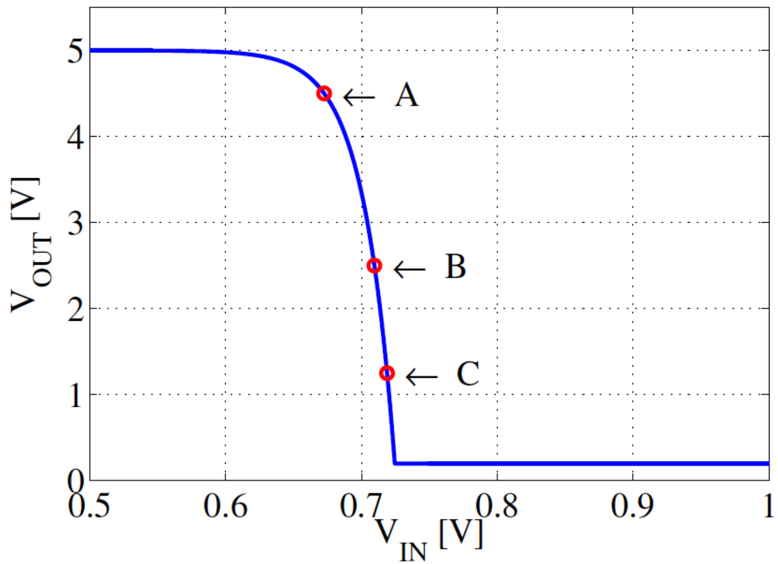
$$I_{C,\max} = \frac{V_{CC} - V_{CE,sat}}{R_L}$$



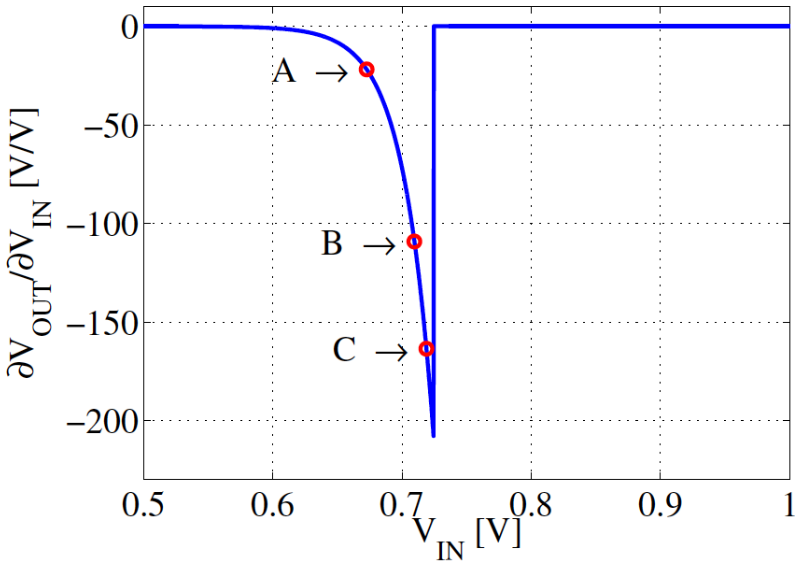
Small Signal Voltage Gain

$$V_{OUT} = V_{CC} - R_L \cdot I_S \cdot e^{\frac{V_{IN}}{V_T}}$$

$$A_v = \frac{\partial V_{OUT}}{\partial V_{IN}} = -R_L \frac{I_S \cdot e^{\frac{V_{IN}}{V_T}}}{V_T} = -R_L \frac{I_{C,Q}}{V_T}$$



$$A_v = \frac{\partial V_{OUT}}{\partial V_{IN}}$$



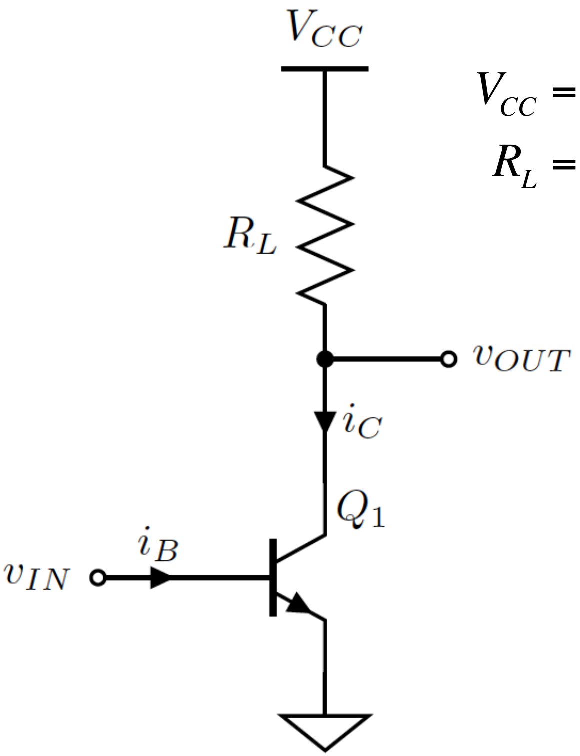
Assumptions?

- $V_A \rightarrow \infty$

Compare to $A_v = -g_m \left(r_o \parallel R_L\right)$

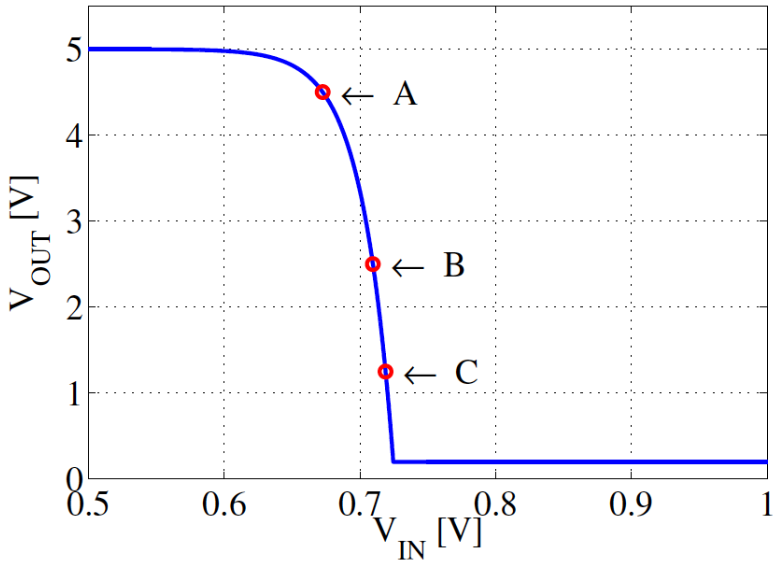
Choosing the Bias Point?

- Largest gain? → Point C



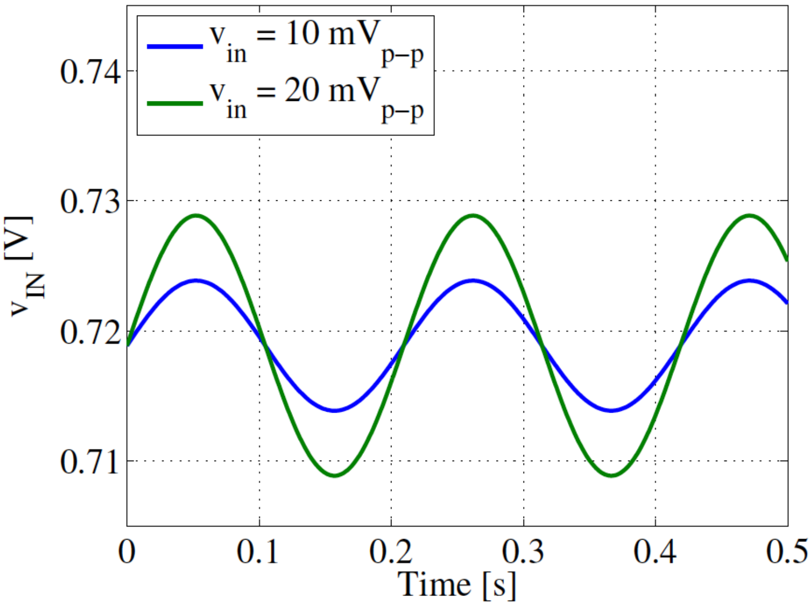
$V_{CC} = 5\text{V}$

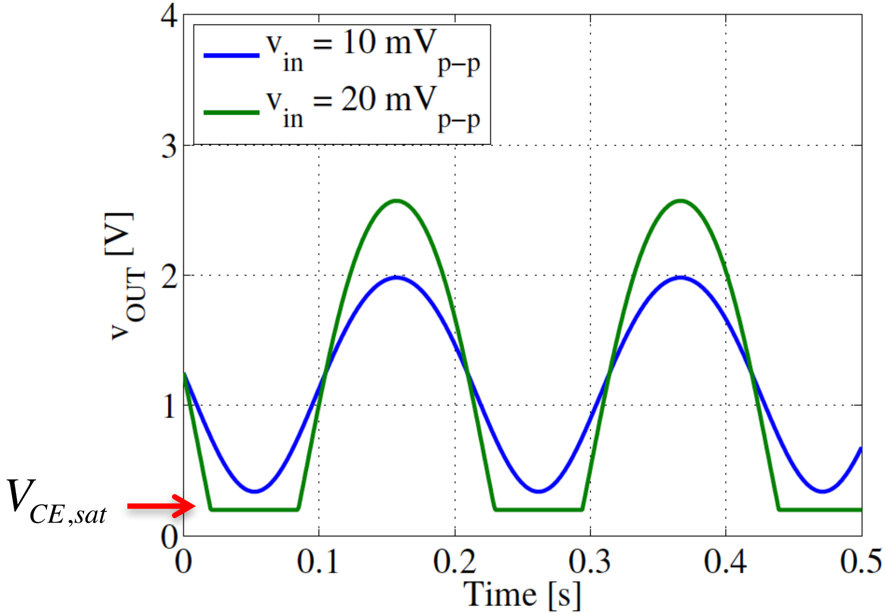
$R_L = 500\Omega$



	V_{IN} [mAV]	$I_{C,Q}$ [mA]	V_{OUT} [V]	A_v $[\frac{V}{V}]$
Point A	672.5	1	4.5	−21.7
Point B	709.5	5	2.5	−108.7
Point C	718.9	7.5	1.25	−163.0

Transient Response at Point C: Output Swing





$V_{CC} = 5\text{V}$

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	V_{IN} [mAV]	$I_{C,Q}$ [mA]	V_{OUT} [V]	A_v $[\frac{\text{V}}{\text{V}}]$
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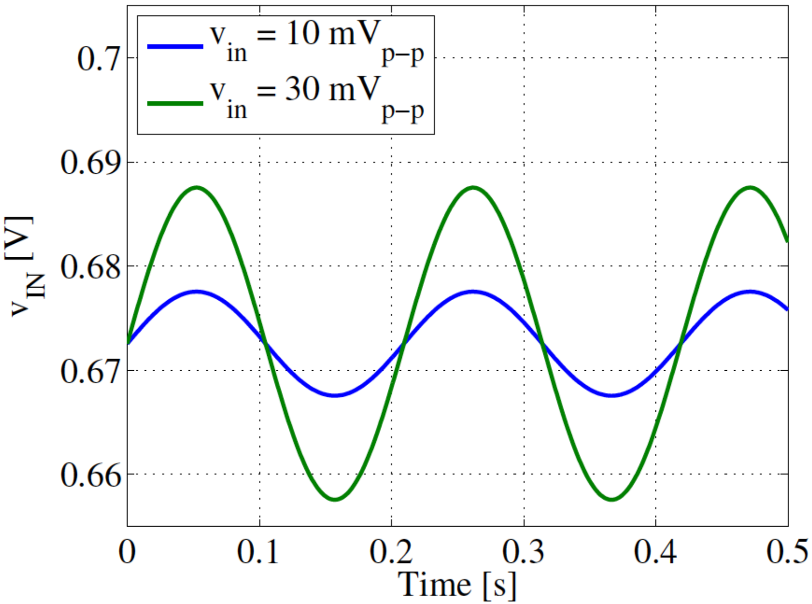
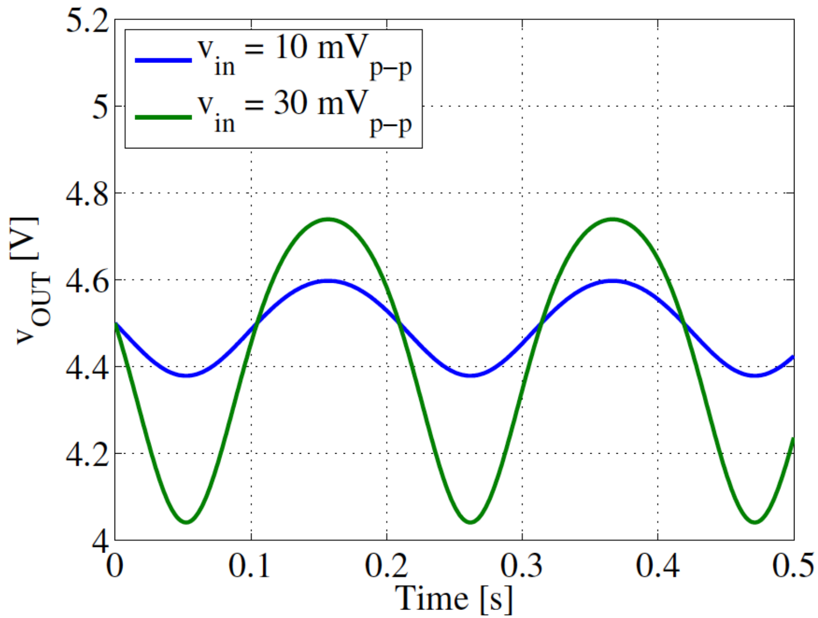
Point C	$\boxed{718.9}$	7.5	$\boxed{1.25}$	−163.0

Transient Response at Point A: Output Swing





$V_{CC} = 5\text{V}$

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	V_{IN} [mAV]	$I_{C,Q}$ [mA]	V_{OUT} [V]	A_v $[\frac{\text{V}}{\text{V}}]$
Point A	672.5	1	4.5	-21.7
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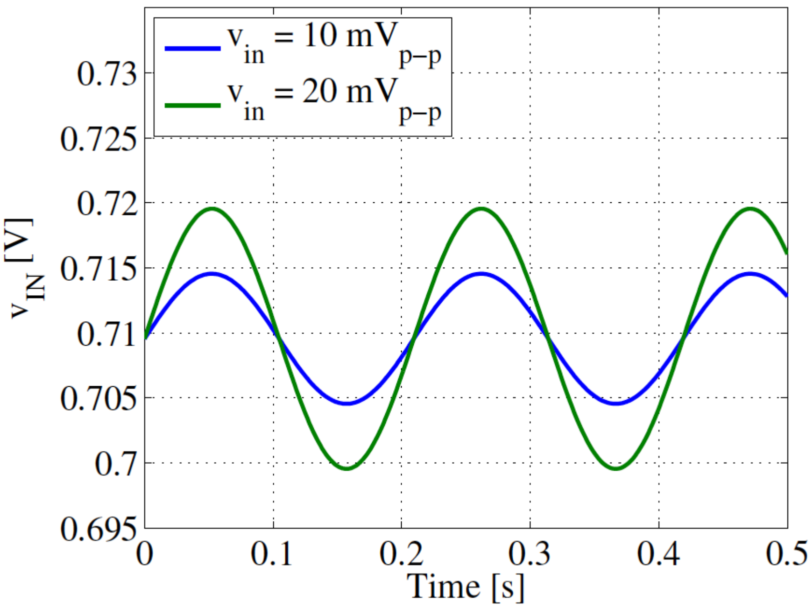
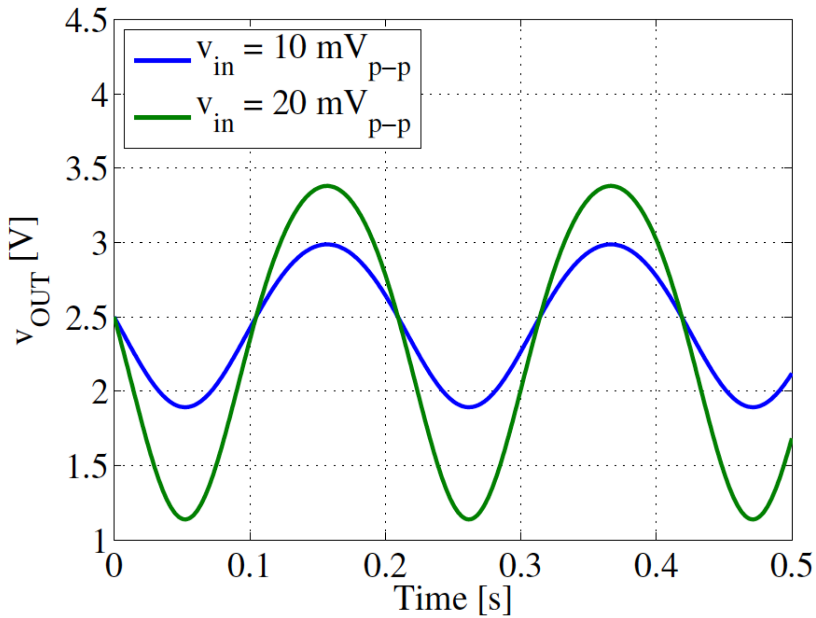
Point C	718.9	7.5	1.25	-163.0

Transient Response at Point B: Output Swing





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Point A	672.5	1	4.5	−21.7
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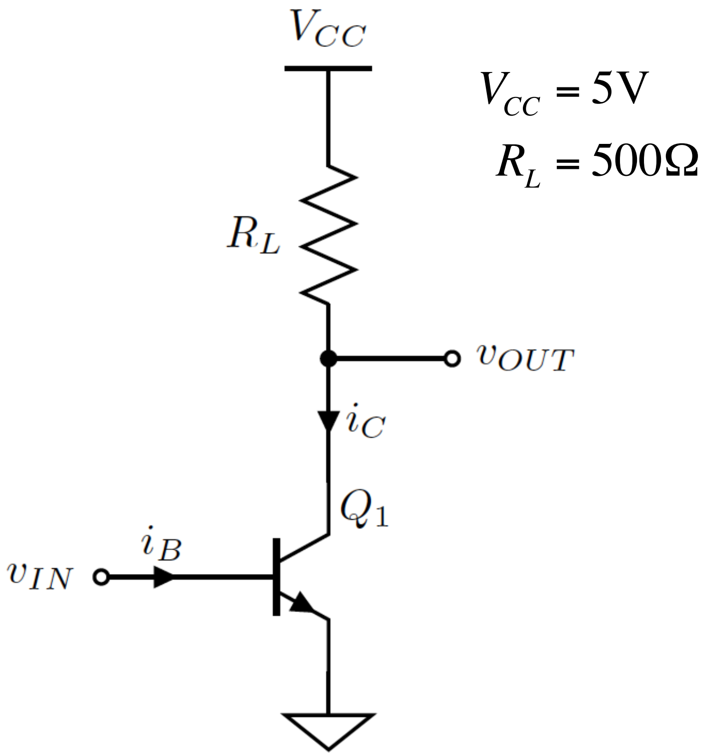
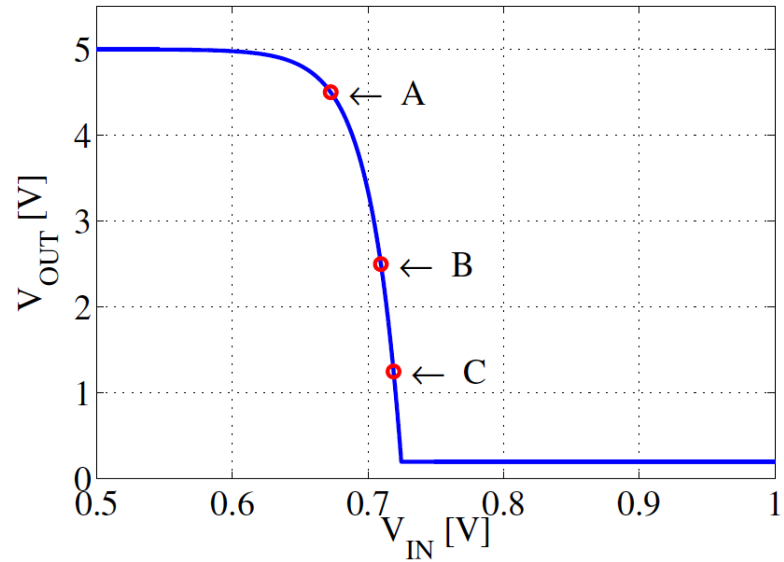
Choosing the Bias Point → Swing vs. Distortion

- Depends on what you need





	V_{IN} [mAV]	$I_{C,Q}$ [mA]	V_{OUT} [V]	A_v $\left[\frac{\text{V}}{\text{V}}\right]$
Point A	672.5	1	4.5	-21.7
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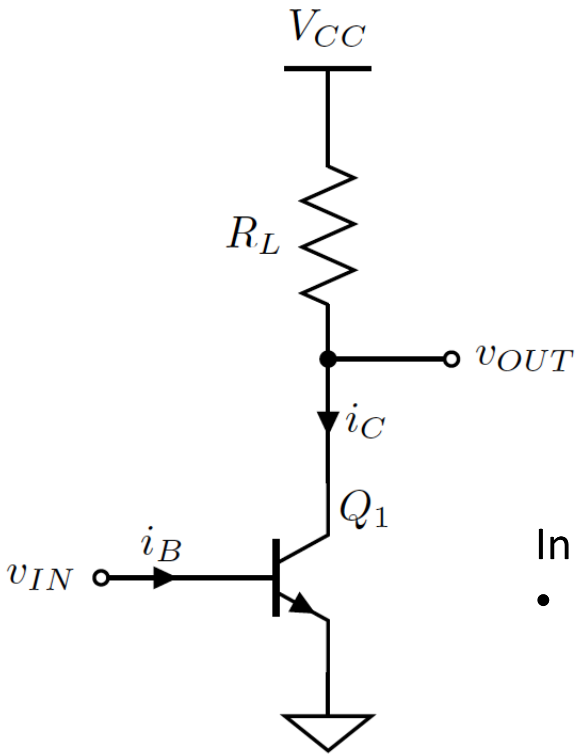
Quiescent DC Power

- Amplification requires power input



$$
\begin{aligned}
P_{DC} &= V_{CC} I_{C,Q} + V_{IN} I_{B,Q} \\
&= V_{CC} I_{C,Q} + V_{IN} \frac{I_{C,Q}}{\beta} \\
&= I_{C,Q} \left(V_{CC} + \frac{V_{IN}}{\beta} \right)
\end{aligned}
$$

In general:

- Higher gain → larger $I_{C,Q}$ → higher DC power consumption

Next Meeting

- Single-Stage Amplifiers
  - Common-Emitter Biasing
  - Common-Source Amplifier
  - Common-Base / Common-Gate Amplifier
  - Common-Collector / Common-Drain Amplifier