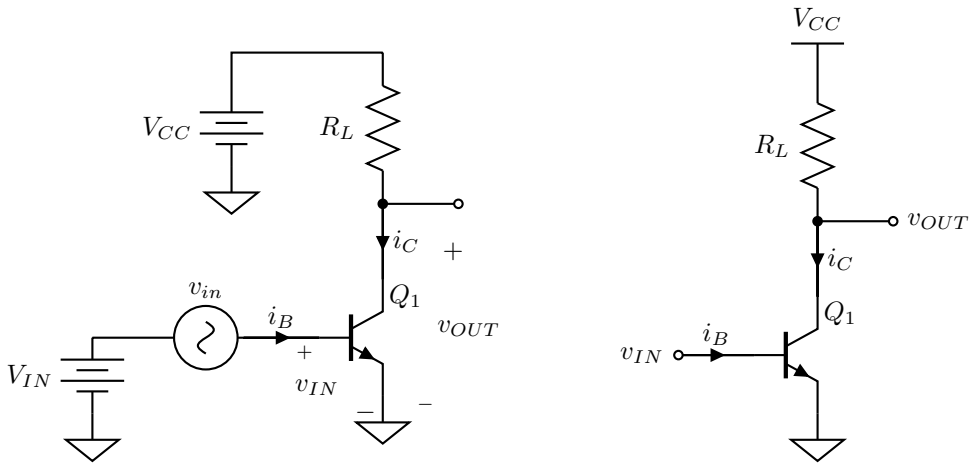


(a) Schematic (b) Simplified schematic

Figure 3.1: A simple BJT common-emitter amplifier.

3 Single-Stage Amplifiers

Three different two-port topologies are possible for a 3-terminal transistor. How do we know which one to use for a certain application? As we will see, each topology has its own set of advantages and disadvantages. Here, we look at the characteristics of the 3 different topologies of single-stage BJT amplifiers: (1) the common-emitter, (2) the common-base, and (3) the common-collector amplifiers, as well as their MOSFET equivalents: (1) the common-source, (2) the common-gate, and (3) the common-drain amplifiers. Single-stage amplifiers, such as these ones, are important building blocks in the design of linear electronic amplifiers.

3.1 The Common-Emitter Amplifier

Let's start with the BJT common-emitter (CE) amplifier in Fig. 3.1a. Note that to reduce the clutter of our transistor schematics, and to clearly show the signal path instead of the DC paths, we often use the simplified schematic in Fig. 3.1b. The largest DC voltage is normally referred to as the *supply voltage*, since it is usually responsible for providing the quiescent collector current, or *bias current,* to the transistor. In Fig. 3.1, V_{CC} is the supply voltage. The input voltage, v_{IN} is the sum of its quiescent DC voltage, V_{IN}, and its small signal component, v_{in}, thus

$$v_{IN} = V_{IN} + v_{in} = v_{BE} \tag{3.1}$$

The output voltage, v_{OUT}, of the amplifier is taken at the collector terminal of the transistor, and is referred to ground. It is equal to the transistor collector-emitter voltage, v_{CE}, and is also composed of a quiescent DC voltage, V_{OUT}, as well as small signal voltage, v_{out}.

In order to see how we can use our transistor to amplify signals in this configuration, we need to first get its quiescent DC operating point.

3.1.1 DC Analysis

The goal of DC analysis is to find the quiescent DC (or bias) currents and voltages of our transistors, since this will, in turn, allow us to calculate the transistor small signal parameters. These small signal parameters will then be used to calculate the two-port parameters of the common-emitter amplifier.

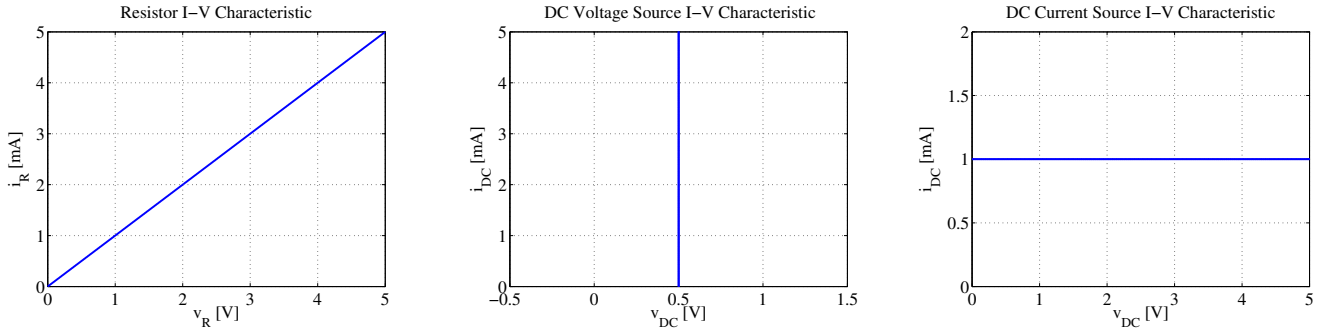
For DC analysis, we set all small signals to zero, leaving us with only the quiescent DC voltages and currents. Writing the KVL equations around the output side of the amplifier, and recognizing that $V_{BE,Q} = V_{IN}$ and $V_{CE,Q} = V_{OUT}$, we get

$$V_{CC} - I_{C,Q}R_L - V_{OUT} = 0 \tag{3.2}$$

If we assume that the transistor is operating in the forward-active region,

$$I_{C,Q} = I_S \cdot \left(e^{\frac{V_{IN}}{V_T}} - 1\right) \cdot \left(1 + \frac{V_{OUT}}{V_A}\right) \tag{3.3}$$

Thus, if we are given the transistor technology parameters I_S, and V_A, the temperature, the values of the DC sources, V_{CC} and V_{IN}, and the resistor R_L, we can use Eqs. 3.2 and 3.3 to solve for $I_{C,Q}$ and V_{OUT}.



(a) A 1 kΩ resistor (b) A 0.5 V DC voltage source (c) A 1 mA DC current source

Figure 3.2: Linear two-terminal I-V characteristics.

If V_{IN} is around 0.6 V, and V_A is large compared to the supply voltage, then we can approximate the quiescent DC collector current as

$$I_{C,Q} = I_S \cdot e^{\frac{V_{IN}}{V_T}} \tag{3.4}$$

Then we can solve for V_{OUT} as

$$V_{OUT} = V_{CC} - I_{C,Q} R_L \tag{3.5}$$

If $V_{OUT} > V_{CE,sat}$, then the transistor is indeed in the forward-active region. This is an easy check to verify our original assumption. After computing the quiescent DC collector current, and given the transistor β, we can easily get the base current using

$$I_{B,Q} = \frac{I_{C,Q}}{\beta} = \frac{I_S}{\beta} \cdot e^{\frac{V_{IN}}{V_T}} \tag{3.6}$$

3.1.2 Small Signal Analysis

From the quiescent DC collector current, we can get the transistor small signal parameters, assuming that the transistor is in the forward-active region:

$$g_m = \frac{I_{C,Q}}{V_T} \tag{3.7}$$

$$r_o = \frac{V_A}{I_{C,Q}} \tag{3.8}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{\beta \cdot V_T}{I_{C,Q}} \tag{3.9}$$

However, aside from the transistor, we have several other components in our circuit in Fig. 3.1. Let us determine the small signal equivalents of linear resistors and independent DC sources. Since these elements are two-terminal devices, we can treat them all as small signal resistances.

The current-voltage (I-V) characteristics of a linear resistor is shown in Fig. 3.2a. The small signal equivalent resistance is again defined as

$$R_{\text{small signal}} = \left(\frac{\partial i_R}{\partial v_R} \right)^{-1} = R \tag{3.10}$$

Since the slope of the I-V characteristic of a linear resistor is the same for any point, then the small signal resistance is independent of the quiescent DC voltage or current. Thus, the small signal equivalent of a linear resistor with resistance R is also a resistor with the same resistance R.

Fig. 3.2b shows the I-V characteristic of a 0.5 V DC voltage source. We note that since the voltage is constant for any current, the slope of the I-V curve is infinite, thus

$$R_{\text{small signal}} = \left(\frac{\partial i_{DC}}{\partial v_{DC}} \right)^{-1} = 0 \tag{3.11}$$

Having a small signal resistance of zero implies that for small signals, independent DC voltage sources act like short circuits. This should be intuitive, since no matter how much small signal current force into the source, there will be

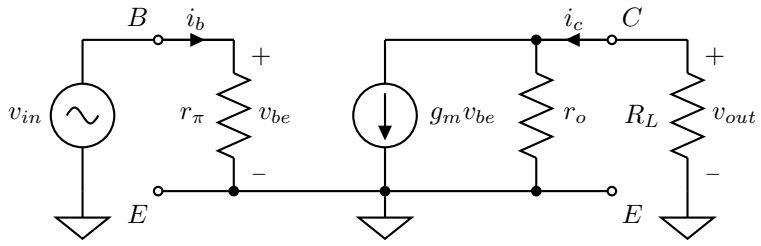


Figure 3.3: The small signal equivalent circuit of the common-emitter amplifier in Fig. 3.1a.

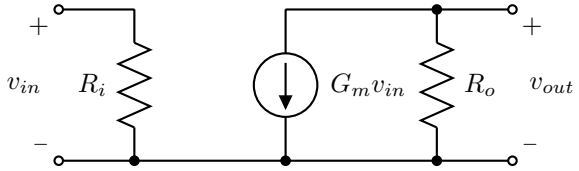


Figure 3.4: Common-emitter amplifier two-port equivalent circuit.

no small signal change in the voltage. Hence, the small signal equivalent of the DC voltage source is a short circuit since the small signal voltage is always zero.

For the independent DC current source, whose I-V characteristic is given in Fig. 3.2c, we can once again determine the equivalent small signal resistance as

$$R_{\text{small signal}} = \left(\frac{\partial i_{DC}}{\partial v_{DC}}\right)^{-1} \to \infty \tag{3.12}$$

Therefore, the small signal equivalent resistance of an independent DC current source is an open circuit. This is due to the fact that no matter what small signal voltage we force across the current source, the current will remain constant, resulting in zero small signal current change.

Using the small signal equivalents of all the components in Fig. 3.1a, the small signal equivalent circuit of the common-emitter amplifier can be obtained, as seen in Fig. 3.3. Again, it is very important to note that the small signal equivalent circuit describes the relationships only between the small voltage or current changes about the quiescent DC operating point. There is no DC (voltage or current) information in the small signal domain.

Given the small signal equivalent circuit of the common-emitter amplifier, we can now derive its equivalent two-port equivalent circuit. Using our two-port parameter definitions, the input resistance of the CE amplifier is

$$R_i = r_\pi = \frac{\beta}{g_m} = \frac{\beta \cdot V_T}{I_{C,Q}} \tag{3.13}$$

The circuit transconductance is then

$$G_m = g_m = \frac{I_{C,Q}}{V_T} \tag{3.14}$$

The output resistance can then be expressed as the parallel combination of r_o and the load resistance, R_L,

$$R_o = r_o \parallel R_L = \frac{V_A}{I_{C,Q}} \parallel R_L \tag{3.15}$$

The CE amplifier two-port equivalent circuit is shown in Fig. 3.4.

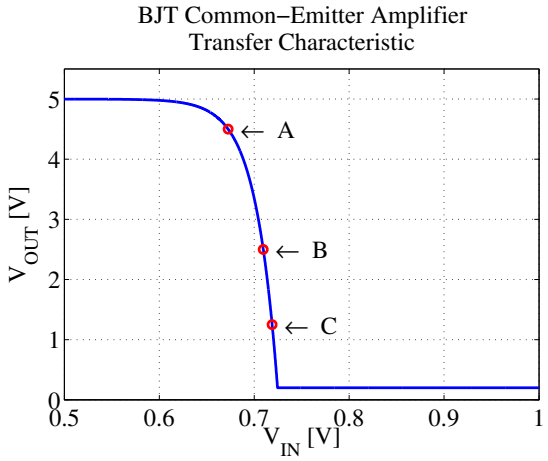
In most cases, we are interested in the small signal voltage gain. Thus,

$$A_v = \frac{v_{out}}{v_{in}} = -G_m R_o = -g_m \left(r_o \parallel R_L\right) = -g_m \cdot \frac{r_o R_L}{r_o + R_L} = -g_m r_o \cdot \frac{R_L}{r_o + R_L} \tag{3.16}$$

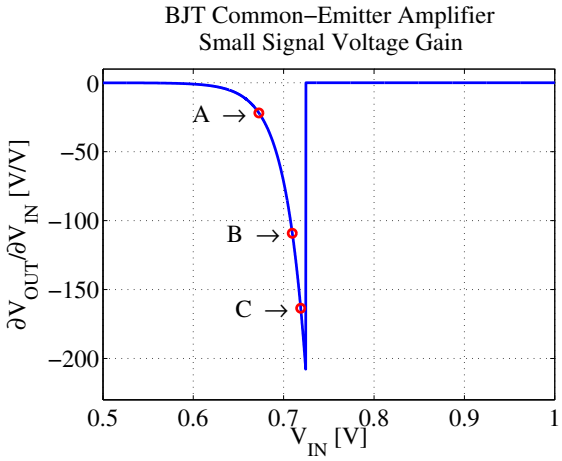
The small signal voltage gain is negative since for the CE amplifier in Fig. 3.1a, a small voltage increase at the input would result in an increase in v_{BE}, resulting in an increase in collector current. This increase in i_C results in an increase in the voltage across R_L, causing the output voltage to drop. Note that an amplifier with a negative small signal gain is called an *inverting amplifier*.

For the CE amplifier in Fig. 3.1a, if we assume that r_o is finite, the maximum small signal voltage gain can be obtained when we let $R_L \to \infty$, resulting in

$$|A_{v,\max}| = a_o = g_m r_o = -\frac{I_{C,Q}}{V_T} \cdot \frac{V_A}{I_{C,Q}} = \frac{V_A}{V_T} = \frac{q \cdot V_A}{kT} \tag{3.17}$$



(a) Large signal transfer curve



(b) Small signal voltage gain

Figure 3.5: Common-emitter characteristics for a transistor with $I_S = 2 \times 10^{-16}\,\text{A}$ and $V_A \to \infty$, using $V_{CC} = 5\,\text{V}$, and $R_L = 500\,\Omega$ at $T = 300\text{K}$.

Eq. 3.17 represents the maximum voltage gain we can get out of a single BJT, also known as the *intrinsic voltage gain*, a_o. Note that any other value of R_L would result in a voltage gain lower than a_o, and that a_o is only dependent on the transistor Early Voltage, and temperature. The intrinsic voltage gain is also a convenient metric that be used to determine if a transistor is suited for a certain circuit or task.

3.1.3 Transistor Operating Regions

Eqs. 3.13 to 3.15 clearly show that the common-emitter small signal two-port equivalent circuit is dependent on the quiescent DC operating point of the transistor. In order to understand the relationship between the DC bias point and the small signal parameters, let us look at the large signal transfer characteristic of the CE amplifier. From Eqs. 3.4 and 3.5, we can express the output DC voltage as

$$V_{OUT} = V_{CC} - R_L \cdot I_S \cdot e^{\frac{V_{IN}}{V_T}} \tag{3.18}$$

Note that Eq. 3.18 is only valid when when the transistor is in the forward active region, that is, when $V_{OUT} > V_{CE,sat}$. For $V_{IN} \approx 0$, V_{OUT} approaches V_{CC}. As V_{IN} is increased, the collector current increases, leading to a decrease in V_{OUT}. The output voltage will decrease until it reaches $V_{CE,sat}$, placing the transistor in saturation, and pinning the output voltage to approximately $V_{CE,sat}$, as we have learned in EEE 41.

The maximum collector current that can flow before the transistor enters the saturation region occurs when $V_{OUT} = V_{CE,sat}$, and can be expressed as

$$I_{C,\text{max}} = \frac{V_{CC} - V_{CE,sat}}{R_L} = I_S \cdot e^{\frac{V_{IN,sat}}{V_T}} \tag{3.19}$$

If the supply voltage is very much greater than $V_{CE,sat}$, then we can approximate Eq. 3.19 as

$$I_{C,\text{max}} \approx \frac{V_{CC}}{R_L} \tag{3.20}$$

Aside from setting the output DC voltage level, and converting the small signal current to a small signal voltage, the load resistance R_L in Fig. 3.1a also limits the maximum collector current that the transistor can draw.

Using Eq. 3.18, and the fact that $V_{OUT} = V_{CE,sat}$ when the transistor is in saturation, we can plot V_{IN} versus V_{OUT}, or the large signal transfer characteristic, of the CE amplifier in Fig. 3.1a, as shown in Fig. 3.5a.

As we expect, the small signal voltage gain is just the slope of the transfer characteristic at a particular bias point. Taking the derivative of Eq. 3.18, we get

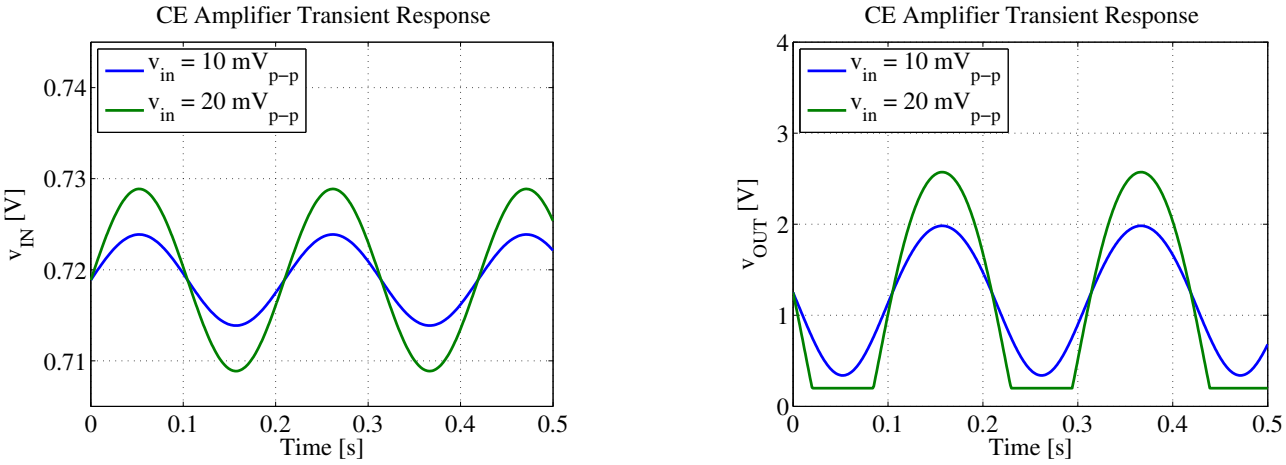
$$\frac{\partial V_{OUT}}{\partial V_{IN}} = -R_L \cdot \frac{I_S}{V_T} \cdot e^{\frac{V_{IN}}{V_T}} = -R_L \cdot \frac{I_{C,Q}}{V_T} = -g_m R_L \tag{3.21}$$

Since Eq. 3.18 assumes that $V_A \to \infty$, the resulting small signal transistor output impedance, r_o, will also approach infinity, reducing Eq. 3.16 to Eq. 3.21.

As we can see from Figs. 3.5a and 3.5b, choosing different values for the DC input voltage, V_{IN}, would result in different quiescent collector currents, leading to different quiescent output voltages and small signal gains.

Table 3.1: Biasing the common-emitter amplifier described in Fig. 3.5a.

	V_{IN} [mAV]	$I_{C,Q}$ [mA]	V_{OUT} [V]	A_v $\left[\frac{\text{V}}{\text{V}}\right]$
Point A	672.5	1	4.5	−21.7
Point B	709.5	5	2.5	−108.7
Point C	718.9	7.5	1.25	−163.0



(a) Input voltage (b) Output voltage

Figure 3.6: BJT common-emitter amplifier transient response when (a) it is biased at point C, and (b) a small signal input sinusoid is applied.

For example, choosing $V_{IN} = 709.5\,\text{mV}$, and using Eqs. 3.4 and 3.18, results in $I_{C,Q} = 5\,\text{mA}$, and $V_{OUT} = 2.5\,\text{V}$, corresponding to point B in Fig. 3.5a. Then, by using Eq. 3.21, we get $A_v = -108.7\,\frac{\text{V}}{\text{V}}$, corresponding to point B in Fig. 3.5b. Note that choosing either point A or point C in Fig. 3.5a would result in different small signal gains, as seen in Fig. 3.5b and Table 3.1.

Choosing a Bias Point: A common question in the design of linear amplifiers is "What bias point should we use?". Clearly, if we want the largest possible gain, we would bias the CE amplifier near point C in Fig. 3.5b. However, let us look at the implications of using point C as our bias point.

If we apply a sinusoidal small signal voltage, v_{in}, to the input of our CE amplifier, we would get the transient waveforms in Fig. 3.6. For $v_{in} = 10\,\text{mV}_{\text{p-p}}$, we will get an output sinusoid, $v_{out} \approx 1.6\,\text{V}_{\text{p-p}}$, as expected. However, if we increase v_{in} to $20\,\text{mV}_{\text{p-p}}$, we see that the output is distorted[a], as seen in Fig. 3.6b. The clipping of the lower part of the output sinusoid is due to the transistor's entry into its saturation region. This is due to the fact that the increase in collector current, increases the voltage across R_L, reducing the transistor's V_{CE} until it reaches $V_{CE,sat}$. Note that in the saturation region, $v_{OUT} = V_{CE,sat} \approx 0.2\,\text{V}$, independent of the input, v_{in}.

The maximum symmetric[b] peak-to-peak output voltage of an amplifier is known as its *output swing*. For the CE amplifier at bias point C, the output swing is limited by the largest negative output voltage that would keep the BJT in its forward-active region. Thus, to keep the transistor $V_{CE} > V_{CE,sat}$, we should satisfy the relation $V_{OUT} - |v_{out}| > V_{CE,sat}$ on the negative swing of v_{out}. Therefore, the output swing can be expressed as

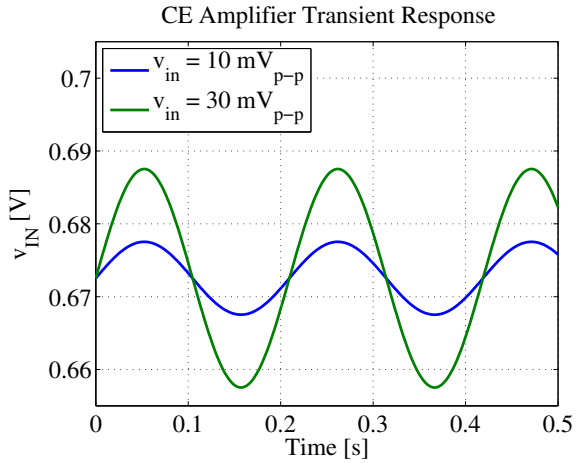
$$v_{out,\max} = 2 \cdot (V_{OUT} - V_{CE,sat}) = 2 \cdot (1.25 - 0.2)\ \text{V} = 2.1\,\text{V} \tag{3.22}$$

On the other hand, let us examine what happens when choose point A in Fig. 3.5a as our bias point. Again if we apply a sinusoidal small signal voltage, v_{in}, to the input of our CE amplifier biased at point A, we would get the transient waveforms in Fig. 3.7.

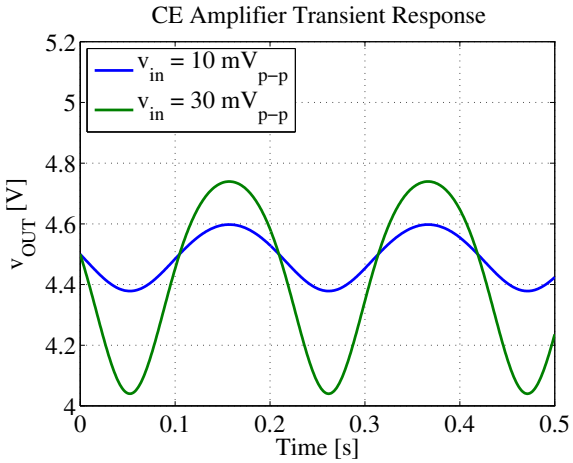
As seen in Fig. 3.7, applying $v_{in} = 10\,\text{mV}_{\text{p-p}}$ results in $v_{out} \approx 210\,\text{mV}_{\text{p-p}}$, again as expected, given that the calculated small signal gain is $-21.7\,\frac{\text{V}}{\text{V}}$. Increasing the input to $30\,\text{mV}_{\text{p-p}}$ results in an asymmetric output sinusoid, as seen in Fig. 3.7b. The negative output swing can accommodate the gain, however, the positive swing is now limited by the low-gain region in Fig. 3.5b. This is due to the fact that the quiescent DC output voltage, V_{OUT}, of point A is very close to the supply voltage, V_{CC}. Thus, for the output voltage to reach V_{CC}, the voltage across R_L has

[a] Distortion is a measure of how different a signal is from a perfect sinusoid. Strictly speaking, all semiconductor amplifiers exhibit a certain amount of distortion when a perfect sinusoid is applied at its input. However, here we mean the distortion due to the clipping or flattening of the peaks of the sinusoid.

[b] The positive swing should be equal to the negative swing about the quiescent DC point.

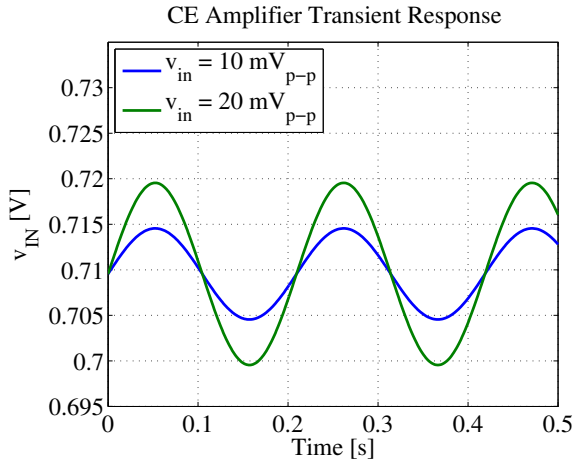


(a) Input voltage

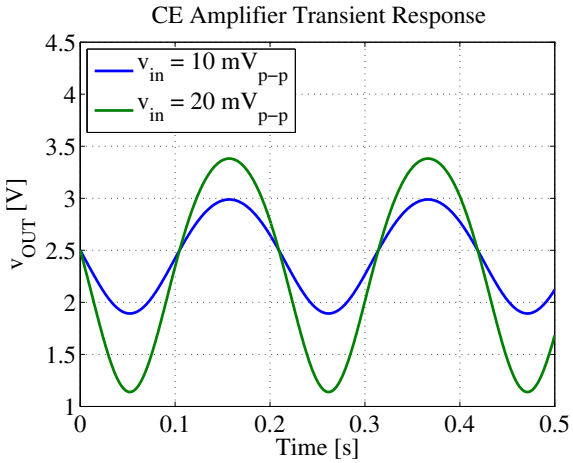


(b) Output voltage

Figure 3.7: BJT common-emitter amplifier transient response when (a) it is biased at point A, and (b) a small signal input sinusoid is applied.



(a) Input voltage



(b) Output voltage

Figure 3.8: BJT common-emitter amplifier transient response when (a) it is biased at point B, and (b) a small signal input sinusoid is applied.

to be very small, requiring a larger negative small signal input voltage. Note that for the output to reach V_{CC}, the transistor needs to be placed in its cut-off region, where the collector current is zero.

A good tradeoff between gain and output swing would be to bias the common-emitter amplifier at point B. Thus, by placing the output DC voltage at around half the supply voltage, we would get a relatively large output swing without significant loss in voltage gain. The transient response of the common-emitter amplifier biased at point B is shown in Fig. 3.8.

For a small signal input voltage of $10\,\mathrm{mV_{p-p}}$, the resulting small signal output voltage has a peak-to-peak value of around 1.1 V, consistent with our computed small signal gain of $-108.7\,\frac{\mathrm{V}}{\mathrm{V}}$ in Table 3.1. Increasing the input to $20\,\mathrm{mV_{p-p}}$ results in the output waveform in Fig. 3.8b. Note that the output exhibits less flattening during the positive cycle of the sinusoid, while clipping is avoided during the negative cycle.

It is also important to note that the DC power the amplifier needs depends on the bias point. For the common-emitter amplifier in Fig. 3.1a, we can calculate the quiescent DC power as

$$P_{DC} = V_{CC} I_{C,Q} + V_{IN} I_{B,Q} \tag{3.23}$$

As we can see in Eq. 3.23, a larger the quiescent DC collector current would result in a larger transconductance, but would also consume more power. This tradeoff between gain, output swing and power is common in designing electronic amplifiers.

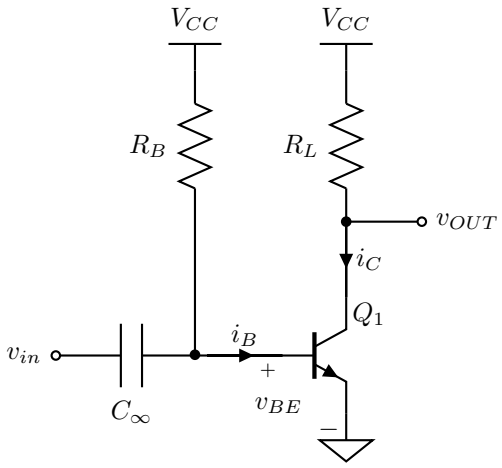


Figure 3.9: A fixed-bias common-emitter amplifier.

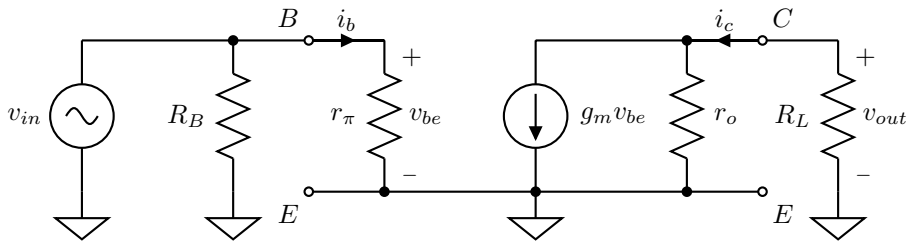


Figure 3.10: The small signal model of the fixed-bias CE amplifier in Fig. 3.9.

3.1.4 The Fixed-Bias Common-Emitter Amplifier

Biasing the common-emitter amplifier using two DC voltage sources is costly, and sometimes, depending on where the amplifier is used, using two DC voltage sources is not possible at all. Thus, an alternative to the biasing strategy used in Fig. 3.1a is to use a resistor to generate the quiescent base-emitter DC voltage, as shown in Fig. 3.9.

The input is coupled into the base of the transistor using an infinitely large capacitor, C_∞. By using C_∞, we prevent any DC current from flowing into the small signal input source, thus, preserving the DC bias point of the amplifier. Also, since the capacitor is infinitely large, any non-DC small signal v_{in} will just see a short circuit directly to the base of the transistor, and will pass through the capacitor without any attenuation.

We can calculate the bias point by writing out the KVL equation for the base loop as

$$V_{CC} - I_{B,Q}R_B - V_{BE} = 0 \tag{3.24}$$

Substituting Eq. 3.4 into Eq. 3.24, and expressing everything in terms of $I_{C,Q}$, we get

$$V_{CC} - \frac{I_{C,Q}}{\beta}R_B - V_T \ln\left(\frac{I_{C,Q}}{I_S}\right) = 0 \tag{3.25}$$

Using Eq. 3.25, we can solve for the quiescent DC collector current. However, solving a nonlinear (exponential) equation is not as easy as solving a linear one[c].

One way to quickly estimate the quiescent DC collector current is to use the approximation

$$V_{BE} \approx 0.7\,\text{V} \tag{3.26}$$

As seen in Table 3.1, the quiescent DC base-emitter voltage will be about 0.7 V, even for a relatively large range of collector currents. Thus, if we are expecting currents in the order of 1 mA to 10 mA, then using Eq. 3.26 would give a fairly good estimate of $I_{C,Q}$. Using Eqs. 3.24 and 3.26, we can calculate $I_{C,Q}$ as

$$I_{C,Q} = \beta \cdot \frac{V_{CC} - 0.7\,\text{V}}{R_B} \tag{3.27}$$

Once we know $I_{C,Q}$, we can easily get the quiescent DC operating points $I_{B,Q}$ and V_{OUT}, as well as the transistor small signal parameters g_m, r_o and r_π. The small signal equivalent circuit of the fixed-bias CE amplifier is shown in Fig. 3.10.

[c]It is common to solve these nonlinear equations by numerical, iterative, or graphical methods.

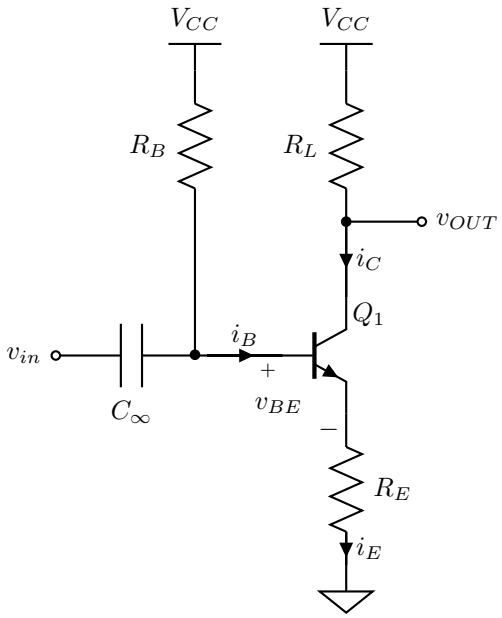


Figure 3.11: The emitter degenerated common-emitter amplifier.

Note that this small signal equivalent circuit is almost the same as the one in Fig. 3.3, except that the input resistance now becomes

$$R_i = r_\pi \parallel R_B \tag{3.28}$$

3.1.5 Emitter Degeneration

One of the assumptions we have made so far is that the transistor β is constant. However, in real transistors, due to limitations in the manufacturing process, β could vary by as much as $\pm 50\%$ from its nominal[d] value, and furthermore, β doubles for every $80\,\mathrm{C}^\circ$ rise in temperature. If we built ten copies of the fixed-bias CE amplifier in Fig. 3.9, and from Eq. 3.27, we would expect to get 10 amplifiers with small signal parameters, and output DC voltages, also varying by $\pm 50\%$.

In some cases, this variation in parameters is acceptable, but in most cases, we want circuits that we can mass produce, but can maintain tighter tolerances, say less than $\pm 1\%$, in terms of parameter variability.

One way to reduce the effect of β variation is to use emitter degenerated CE amplifiers, such as the one shown in Fig. 3.11.

To determine the quiescent DC collector current, we write out the KVL equation for the input loop

$$V_{CC} - I_{B,Q}R_B - V_{BE} - I_{E,Q}R_E = 0 \tag{3.29}$$

Thus, using Eq. 3.26 and expressing $I_{B,Q}$ and $I_{E,Q}$ in terms of $I_{C,Q}$, we get

$$V_{CC} - \frac{I_{C,Q}}{\beta}R_B - 0.7\,\mathrm{V} - I_{C,Q}\left(1 + \frac{1}{\beta}\right)R_E = 0 \tag{3.30}$$

Solving for the quiescent DC collector current, $I_{C,Q}$,

$$I_{C,Q} = \frac{V_{CC} - 0.7\,\mathrm{V}}{\frac{R_B}{\beta} + \left(1 + \frac{1}{\beta}\right)R_E} = \beta \cdot \frac{V_{CC} - 0.7\,\mathrm{V}}{R_B + (\beta + 1)\cdot R_E} \tag{3.31}$$

Note that if β is large, that is if $\beta \gg 1$, and if $\beta \cdot R_E \gg R_B$, we can express Eq. 3.31 as

$$I_{C,Q} \approx \frac{V_{CC} - 0.7\,\mathrm{V}}{R_E} \tag{3.32}$$

which is independent of β!

Another way of looking at Eq. 3.32 is when $\beta \to \infty$, $I_{B,Q} \to 0$. This leads to the voltage across R_B being reduced to zero, and hence, leads to Eq. 3.32.

[d]For example, if we have 1000 pieces of the NPN BJT 2N2222A, with $\beta = 100$ as indicated in the data sheet, and if we expect $\pm 50\%$ β variation, we would probably find some of the transistors to have β values as low as 50, or some as high as 200.

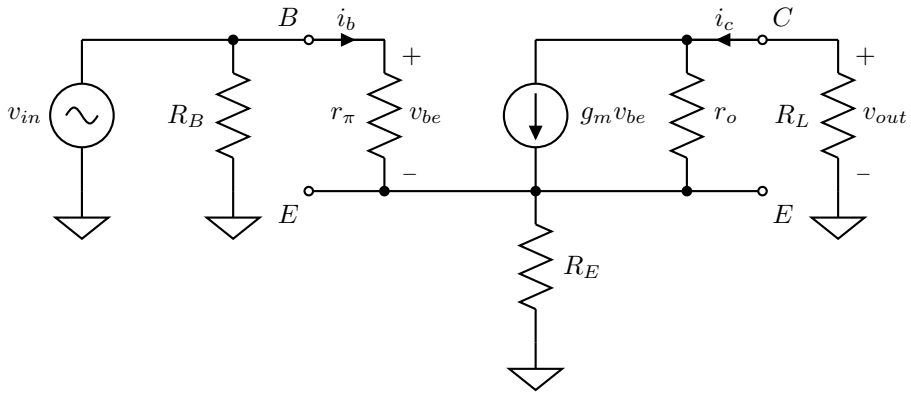


Figure 3.12: The small signal equivalent circuit of the emitter-degenerated CE amplifier in Fig. 3.11.

β Sensitivity: One way to quantify the effect of β on the quiescent DC collector current is to compute the *sensitivity* of $I_{C,Q}$ to β. Sensitivity is expressed as

$$S_\beta^{I_{C,Q}} = \frac{\partial I_{C,Q}}{\partial \beta} \tag{3.33}$$

Thus, for a circuit with a lower the sensitivity, varying β would have a smaller effect on $I_{C,Q}$.

Calculating the sensitivity of the quiescent DC collector current to the β value of the fixed-bias CE amplifier in Fig. 3.9, we would get

$$S_\beta^{I_{C,Q}} = \frac{\partial I_{C,Q}}{\partial \beta} = \frac{V_{CC} - 0.7\,\text{V}}{R_B} \tag{3.34}$$

While for the emitter-degenerated CE amplifier in Fig. 3.11, we have

$$S_\beta^{I_{C,Q}} = \frac{\partial I_{C,Q}}{\partial \beta} = \frac{V_{CC} - 0.7\,\text{V}}{R_B} \cdot \frac{1 + \frac{R_E}{R_B}}{\left(1 + (\beta + 1)\,\frac{R_E}{R_B}\right)^2} \tag{3.35}$$

Comparing Eqs. 3.34 and 3.35, we can see that as $\beta \to \infty$, the sensitivity of the emitter-degenerated CE amplifier goes to zero, while the sensitivity of the fixed-bias CE amplifier remains constant.

Notice that the quiescent DC output voltage is now

$$V_{OUT} = V_{CE} + I_{E,Q} R_E \tag{3.36}$$

Thus, if we want to set the quiescent DC output voltage to $\frac{V_{CC}}{2}$, as well as place the transistor in its forward-active region ($V_{CE} > V_{CE,sat}$), we need to make sure that

$$R_E < \frac{\frac{V_{CC}}{2} - V_{CE,sat}}{I_{C,Q}\left(1 + \frac{1}{\beta}\right)} \tag{3.37}$$

Note that Eq. 3.37 is obtained by rearranging Eq. 3.36. For example, if $V_{CC} = 5\,\text{V}$, $V_{CE,sat} = 0.2\,\text{V}$, $\beta = 100$, and $I_{C,Q} = 1\,\text{mA}$, the value of R_E should be less than $2.28\,\text{k}\Omega$, which is relatively small compared to r_o and r_π.

Once we have obtained the quiescent DC collector current, we can now determine the small signal parameters of the transistor, as well as draw the small signal equivalent circuit of the emitter-degenerated CE amplifier, as shown in Fig. 3.12.

In order to reduce the complexity of our calculations, we can first solve for the two-port Norton equivalent circuit of the transistor small signal model together with R_E, ignoring R_B and R_L for now, as shown in Fig. 3.13.

In order to get the effective transconductance of the transistor with R_E, we short the output to ground, and solve for $G'_m = \frac{i'_{out}}{v'_{in}}$, where i'_{out} is the output short-circuit current. Writing the KCL equation at the emitter node, and recognizing that $v_{be} = v'_{in} - v'_e$, we get

$$\frac{v'_e - v'_{in}}{r_\pi} + \frac{v'_e}{R_E} + \frac{v'_e}{r_o} - g_m\,(v'_{in} - v'_e) = 0 \tag{3.38}$$

Solving for v'_e, we get

$$v'_e = v'_{in} \cdot \frac{g_m + \frac{1}{r_\pi}}{g_m + \frac{1}{r_\pi} + \frac{1}{r_o} + \frac{1}{R_E}} \tag{3.39}$$

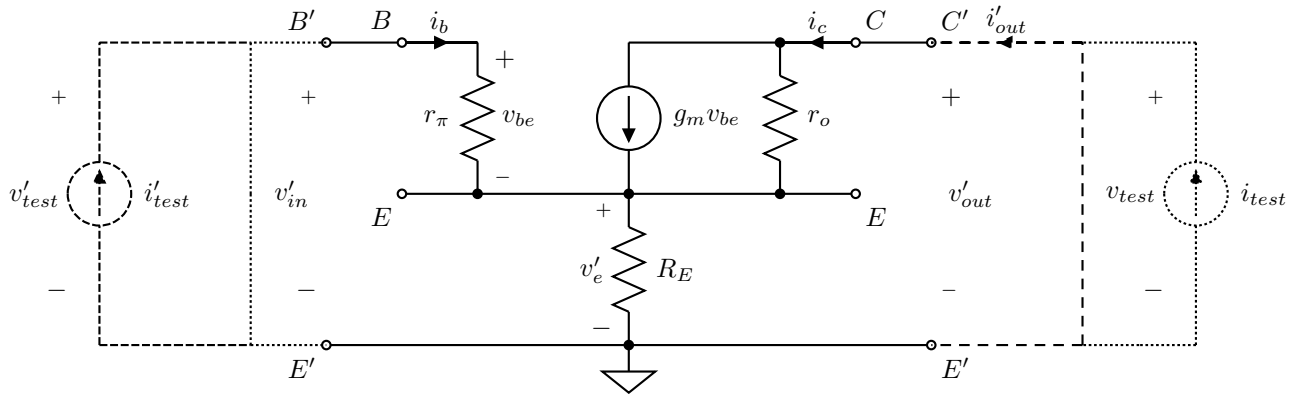


Figure 3.13: The small signal model of the emitter-degenerated NPN BJT.

The short-circuit output current is then

$$i'_{out} = g_m\left(v'_{in} - v'_e\right) - \frac{v'_e}{r_o} = v'_{in} \cdot g_m \cdot \frac{\frac{1}{R_E} - \frac{1}{r_o g_m r_\pi}}{g_m + \frac{1}{r_\pi} + \frac{1}{r_o} + \frac{1}{R_E}} \tag{3.40}$$

Thus,

$$G'_m = \frac{i'_{out}}{v'_{in}} = g_m \cdot \frac{\frac{1}{R_E} - \frac{1}{r_o g_m r_\pi}}{g_m + \frac{1}{r_\pi} + \frac{1}{r_o} + \frac{1}{R_E}} \tag{3.41}$$

Eq. 3.41 is relatively complex and does not give us much intuition regarding the effect of R_E. However, if we simplify Eq. 3.41 by assuming $g_m r_o \gg 1$, $g_m r_\pi = \beta \gg 1$, $R_E \ll r_o$, and $R_E \ll r_\pi$, we get

$$G'_m \approx g_m \cdot \frac{\frac{1}{R_E}}{g_m + \frac{1}{R_E}} = \frac{g_m}{1 + g_m R_E} < g_m \tag{3.42}$$

Since $(1 + g_m R_E) > 1$, Eq. 3.42 shows that the effective transconductance of the transistor and R_E circuit is lower than the transconductance of the transistor without R_E. Thus, we say that the transconductance is *degenerated* by the degenerating resistor, R_E.

The effective output resistance can be calculated by applying a test voltage at the output and measuring the current, when the input small signal voltage is set to zero. However, in this case, let us apply a test current source, i_{test}, at the output, and measure the resulting output voltage, v_{test}. Since the circuit is linear, we should get the same result.

Applying i_{test} at the output, and recognizing that r_π is now parallel to R_E when the input small signal voltage is set to zero, gives us

$$v'_e = i_{test} \cdot (r_\pi \parallel R_E) \tag{3.43}$$

And since $v_{be} = -v'_e$ when the input is shorted to ground, the current through the output impedance, r_o is

$$i_{r_o} = i_{test} - g_m v_{be} = i_{test} + g_m v'_e = i_{test}\left(1 + g_m\left(r_\pi \parallel R_E\right)\right) \tag{3.44}$$

Thus, the output voltage, v_{test} is equal to

$$v_{test} = i_{r_o} r_o + v'_e = i_{test}\left(r_o + g_m r_o\left(r_\pi \parallel R_E\right) + \left(r_\pi \parallel R_E\right)\right) \tag{3.45}$$

The effective output impedance of the transistor with emitter degeneration can then be expressed as

$$R'_o = \frac{v_{test}}{i_{test}} = r_o + g_m r_o\left(r_\pi \parallel R_E\right) + \left(r_\pi \parallel R_E\right) \tag{3.46}$$

Using the same set of assumptions we used for Eq. 3.42, we can simplify Eq. 3.46 as

$$R'_o \approx r_o + R_E + g_m r_o R_E \approx r_o + g_m r_o R_E = r_o\left(1 + g_m R_E\right) > r_o \tag{3.47}$$

Notice that degenerating the transistor by R_E increases its output resistance by a factor $(1 + g_m R_E)$.

Computing the effective input resistance of the emitter-degenerated transistor is similar to computing the output resistance, except that we apply the test current, i'_{test}, at the input, and measure the resulting input test voltage, v'_{test}, when the output is shorted to zero, the Norton no-load condition.

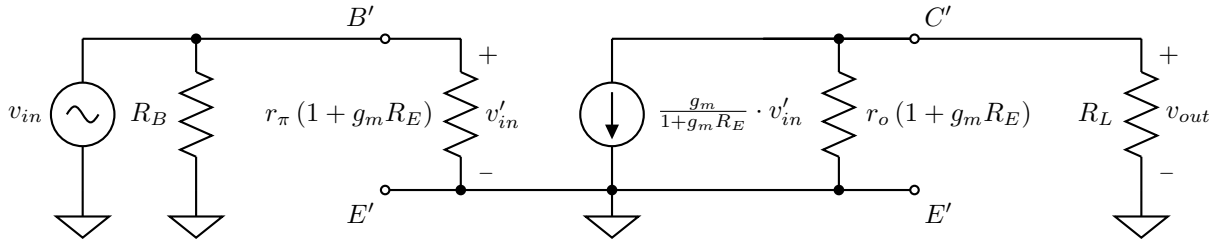


Figure 3.14: The emitter-degenerated common-emitter amplifier small signal model in Fig. 3.12 using the derived effective two-port model of the emitter-degenerated transistor.

Applying i'_{test}, and recognizing that $v_{be} = i'_{test}r_\pi$ and that R_E and r_o are connected in parallel, we can get the voltage across the parallel combination of R_E and r_o as

$$v'_e = (i'_{test} + g_m v_{be}) \cdot (R_E \parallel r_o) = i'_{test}\,(1 + g_m r_\pi) \cdot (R_E \parallel r_o) \tag{3.48}$$

Thus, we can calculate v'_{test} as

$$v'_{test} = v_{be} + v'_e = i'_{test}\,(r_\pi + (R_E \parallel r_o) + g_m r_\pi\,(R_E \parallel r_o)) \tag{3.49}$$

Therefore, the effective input resistance of the emitter-degenerated transistor is

$$R'_i = \frac{v'_{test}}{i'_{test}} = r_\pi + (R_E \parallel r_o) + g_m r_\pi\,(R_E \parallel r_o) \tag{3.50}$$

Again, using the assumptions we used for Eq. 3.42, we can simplify Eq. 3.50 as

$$R'_i \approx r_\pi + R_E + g_m r_\pi R_E \approx r_\pi + g_m r_\pi R_E = r_\pi\,(1 + g_m R_E) > r_\pi \tag{3.51}$$

Once again, note that degenerating the transistor by R_E increases its input resistance of the BJT by a factor $(1 + g_m R_E)$.

Using the small signal model of the emitter-degenerated transistor, we can now draw the two-port small signal equivalent circuit of the common-emitter amplifier with emitter degeneration, as shown in Fig. 3.14.

By inspecting Fig. 3.14, we can easily see that the effective transconductance, G_m, of the emitter degenerated CE amplifier is

$$G_m = \frac{g_m}{1 + g_m R_E} \tag{3.52}$$

and for the case when $R_L \ll r_o\,(1 + g_m R_E)$ and $R_B \ll r_\pi\,(1 + g_m R_E)$, the output and input resistances can be expressed as

$$R_o = R_L \parallel r_o\,(1 + g_m R_E) \approx R_L \tag{3.53}$$

$$R_i = R_B \parallel r_\pi\,(1 + g_m R_E) \approx R_B \tag{3.54}$$

The small signal voltage gain is then

$$A_v = -G_m R_o \approx -\frac{g_m R_L}{1 + g_m R_E} \tag{3.55}$$

Again, note that the small signal voltage gain is degraded or degenerated by R_E. It is interesting to node that if $g_m R_E \gg 1$, then the voltage gain approaches $-\frac{R_L}{R_E}$, which is independent of the transistor parameters![e]

Thus, the consequences of reducing the effect of β variations on the quiescent DC collector current include (1) reduced small signal voltage gain, (2) increased small signal input resistance, and (3) increased small signal output resistance.

[e] We will revisit this result in the feedback amplifiers section.