EEE 51 Assignment 6 Solution

2nd Semester SY 2017-2018

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1. **MOSFET Differential CS Amplifier.** Given the following:

   $V_{DD} = 5V$, I_R=$50uA$, $k_{1,2,7,8} = 2k_6 = 100\frac{uA}{V^2}$, $k_{3,4} = 2k_5 = 75\frac{uA}{V^2}$ $\lambda = 0.02V^{-1}$, and $V_{TH_{n|p}} = 1V$:

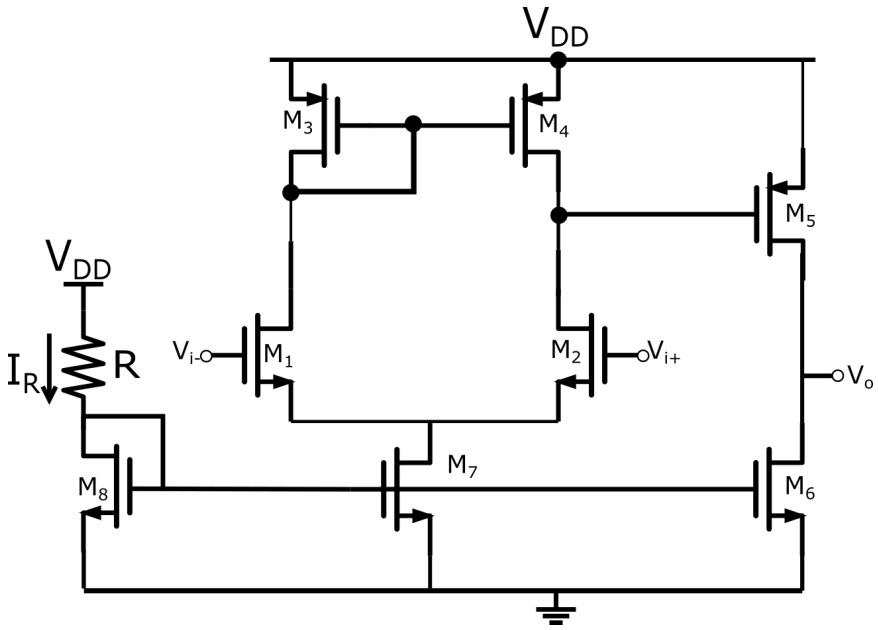

Figure 1: Differential-CS amplifier

(a) Complete the table and ignore channel length modulation effect and assuming all transistors in saturation. [7 pts]

$I_R = I_{D,M8}$ and since M8, M7 and M6 are current mirrors we assume that they have the same V_{GS}. Manipulating I_D equation with equal $V_{GS} and V_{TH}$.

$$I_R = I_{D,M8} = \frac{k_8}{k_7} I_{D,M7} = \frac{k_8}{k_6} I_{D,M6} \tag{1}$$

$I_{D,M8} = 50\mu A$, $I_{D,M7} = 50\mu A$, $I_{D,M6} = 25\mu A$.

The differential amplifier currents are as follows:

$$I_{D,M1} = I_{D,M2} = I_{D,M3} = I_{D,M4} = \frac{I_{D,M7}}{2} \tag{2}$$

$I_{D,M1} = I_{D,M2} = I_{D,M3} = I_{D,M4} == 25\mu A$

The CS amplifier current is the same as its current mirror current. $I_{D,M5} = I_{D,M6} = 25\mu A$.

Using the equation $V_{GS} = V_{TH} + \sqrt[2]{\frac{I_D}{k}}$ to get the V_{GS} of all transistors.

$|V_{GS,M8,M7,M6}| = 1.707V$

$|V_{GS,M5}| = 1.816V$

$|V_{GS,M4,M3}| = 1.577V$

$|V_{GS,M2,M1}| = 1.5V$

The g_m can be computed using $g_m = 2k(|V_{GS}| - |V_{TH}|)$.

$|g_{m,M8,M7}| = 141.421\mu S$

$|g_{m,M6}| = 70.711\mu S$

$|g_{m,M5}| = 61.237\mu S$

$|g_{m,M4,M3}| = 86.603\mu S$
$|g_{m,M2,M1}| = 100\mu S$
The output resistance r_o is computed using $r_o = \frac{1}{\lambda I_D}$
$|r_{o,M8,M7}| = 1M\Omega$
$|r_{o,M6,M5,M4,M3,M2,M1}| = 2M\Omega$

Parameter	M1	M2	M3	M4	M5	M6	M7	M8
ID(A)	25.0E-6	25.0E-6	25.0E-6	25.0E-6	25.0E-6	25.0E-6	50.0E-6	50.0E-6
|Vgs|(V)	1.500E+0	1.500E+0	1.577E+0	1.577E+0	1.816E+0	1.707E+0	1.707E+0	1.707E+0
gm(S)	100.000E-6	100.000E-6	86.603E-6	86.603E-6	61.237E-6	70.711E-6	141.421E-6	141.421E-6
ro(ohms)	2.0E+6	2.0E+6	2.0E+6	2.0E+6	2.0E+6	2.0E+6	1.0E+6	1.0E+6

Figure 2: Parameter table

(b) Solve for the gain of the 1st and 2nd stage as well as the overall gain of the amplifier. [3 pts]
The gain for the 1st stage which is the differential amplifier stage is:

$$A_{V1} = -g_{m,M2}(r_{o,M2}||r_{o,M4}) = -100 \tag{3}$$

The gain for the 2nd stage which is the common source stage is:

$$A_{V2} = -g_{m,M5}(r_{o,M5}||r_{o,M6}) = -61.24 \tag{4}$$

The overall voltage gain is:

$$A_V = A_{V1} * A_{V2} = 6124 \tag{5}$$

2. **BJT Cascode Amplifier with Cascode Load**. A Cascode amplifier is designed as shown in Figure 3. Bias voltages have been provided to it, and the input is fed through a DC block in order to maintain proper biasing. All transistors are confirmed to be biased properly to forward active. The load is a Cascode current mirror designed to provide an output resistance similar to the amplifier's.

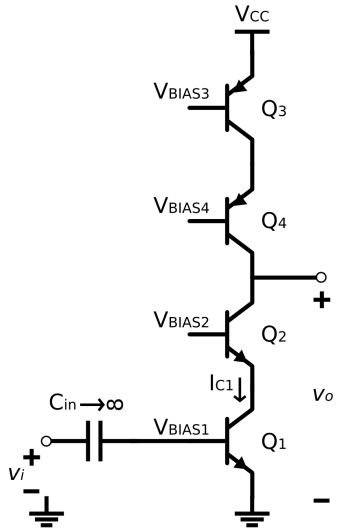

Figure 3: Cascode Amplifier

(a) Draw the small-signal equivalent circuit. Determine the total output resistance R_o, transconductance G_m and gain A_v of the whole amplifier as a function of the small-signal parameters (g_{m1}, r_{o1}, $r_{\pi 1}$, g_{m2}, etc.). [6 pts]

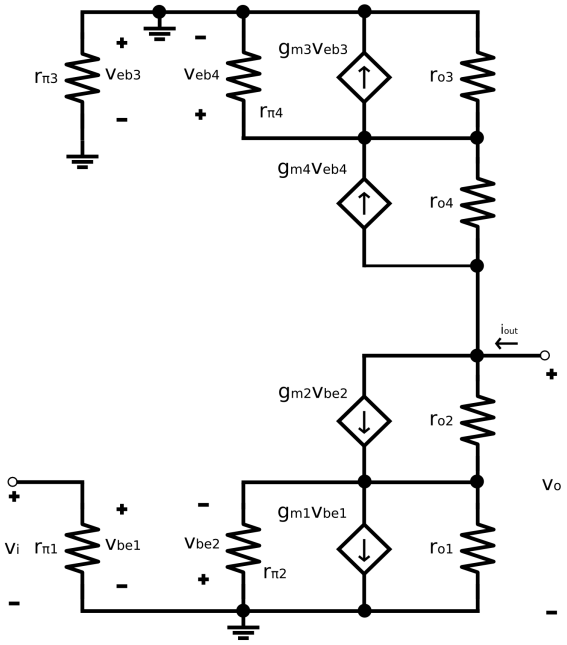

Figure 4: Small-signal equivalent

[2 pts]

The small-signal equivalent is shown as in Figure 4. The bias voltages are effectively shorted to ground. By inspection, the circuit can be analyzed by halving it, and calculating separately the transconductance (G_m) and output resistance of the amplifier (R_{12}) without the mirror, and the output resistance of the mirror (R_{34}). This is assumed such that

$$R_o = R_{12}||R_{34} \tag{6}$$

The circuit to be analyzed then becomes

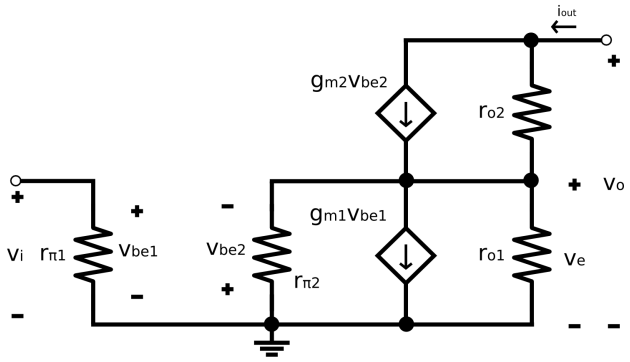

Figure 5: Small-signal equivalent of the amplifier without mirror

Figure 5 is enough to solve for G_m, as the current mirror does not contribute due to it not being on the path from input to output in any way. Start with looking for the small-signal output current.

$$i_{out} = \frac{v_o - v_e}{r_{o2}} + g_{m2}v_e \tag{7}$$

We need v_e, so using a supermesh

$$v_e = (i_{out} - g_{m1} v_i)\,(r_{o1} || r_{\pi 2}) \tag{8}$$

for G_m the output voltage is zeroed, so Equation (7) is rewritten as

$$i_{out} = -v_e \left(\frac{1}{r_{o2}} + g_{m2}\right) \tag{9}$$

$$i_{out} = g_{m1} v_i \left(\frac{1}{r_{o2}} + g_{m2}\right)(r_{o1} || r_{\pi 2}) - i_{out} \left(\frac{1}{r_{o2}} + g_{m2}\right)(r_{o1} || r_{\pi 2}) \tag{10}$$

Bringing the i_{out} terms together,

$$i_{out} \left(1 + \left(\frac{1}{r_{o2}} + g_{m2}\right)(r_{o1} || r_{\pi 2})\right) = g_{m1} v_i \left(\frac{1}{r_{o2}} + g_{m2}\right)(r_{o1} || r_{\pi 2}) \tag{11}$$

$$i_{out} \left(\frac{1}{r_{o1} || r_{\pi 2}} + \frac{1}{r_{o2}} + g_{m2}\right)(r_{o1} || r_{\pi 2}) = g_{m1} v_i \left(\frac{1}{r_{o2}} + g_{m2}\right)(r_{o1} || r_{\pi 2}) \tag{12}$$

$$i_{out} \left(\frac{1}{r_{o1} || r_{\pi 2}} + \frac{1}{r_{o2}} + g_{m2}\right) = g_{m1} v_i \left(\frac{1}{r_{o2}} + g_{m2}\right) \tag{13}$$

Now G_m can be seen as

$$G_m = \frac{i_{out}}{v_i} = g_{m1} \frac{\frac{1}{r_{o2}} + g_{m2}}{\frac{1}{r_{o1} || r_{\pi 2}} + \frac{1}{r_{o2}} + g_{m2}} \tag{14}$$

Or, in order to see this factor a little more clearly,

$$G_m = g_{m1} \frac{r_{o1} || r_{\pi 2} || r_{o2} || \frac{1}{g_{m2}}}{r_{o2} || \frac{1}{g_{m2}}} \tag{15}$$

This is itself a little unwieldy, but would suffice as an answer. However, looking ahead it can be seen that we are allowed to choose the biasing later on by means of manipulating I_{C1} and so all the bias currents at once. We can then make the assumption that we could choose to bias this amplifier "normally" such that the usual assumption that the $\frac{1}{g_m}$ term would be much smaller than r_o or r_π terms. Therefore, we can simplify this result to

$G_m = g_{m1}$ [1 pt]

Since we have broken the circuit down, instead of R_o, solve first for R_{12}, the output resistance of the amplifier. By inspection, this would lead to an expression that would be usable for R_{34}, the output resistance of the mirror.

Going back to Equation (7), it still holds. However, since v_i is zero for output resistance,

$$v_e = i_{out}\,(r_{o1} || r_{\pi 2}) \tag{16}$$

$$i_{out} = \frac{v_o}{r_{o2}} - \frac{v_e}{r_{o2}} + g_{m2} v_e \tag{17}$$

$$i_{out} = \frac{v_o}{r_{o2}} - v_e \left(g_{m2} - \frac{1}{r_{o2}}\right) \tag{18}$$

$$i_{out} = \frac{v_o}{r_{o2}} - i_{out}\,(r_{o1} || r_{\pi 2}) \left(g_{m2} - \frac{1}{r_{o2}}\right) \tag{19}$$

Bringing the i_{out} terms together,

$$i_{out}\left(1+(r_{o1}||r_{\pi 2})\left(g_{m2}-\frac{1}{r_{o2}}\right)\right)=\frac{v_o}{r_{o2}} \tag{20}$$

$$i_{out}\left(r_{o1}||r_{\pi 2}\right)\left(\frac{1}{r_{o1}||r_{\pi 2}}+g_{m2}-\frac{1}{r_{o2}}\right)=\frac{v_o}{r_{o2}} \tag{21}$$

The output resistance is then

$$R_{12}=\frac{v_o}{i_{out}}=\left(r_{o1}||r_{\pi 2}\right)\frac{\frac{1}{r_{o1}||r_{\pi 2}}+g_{m2}-\frac{1}{r_{o2}}}{\frac{1}{r_{o2}}} \tag{22}$$

$$R_{12}=\left(r_{o1}||r_{\pi 2}\right)\frac{r_{o2}}{r_{o1}||r_{\pi 2}||\frac{1}{g_{m2}}||-r_{o2}} \tag{23}$$

Again, making the assumption that $\frac{1}{g_m}$ terms dominate in a parallel resistance,

$$R_{12}=\left(r_{o1}||r_{\pi 2}\right)g_{m2}r_{o2} \tag{24}$$

Similarly, the output resistance of the current mirror must then be

$$R_{34}=\left(r_{o3}||r_{\pi 4}\right)g_{m4}r_{o4} \tag{25}$$

$$R_o=\left(\left(r_{o1}||r_{\pi 2}\right)g_{m2}r_{o2}\right)||\left(\left(r_{o3}||r_{\pi 4}\right)g_{m4}r_{o4}\right)\text{ [2 pts]}$$

The gain is then $-G_mR_o$ or

$$A_v=-g_m\left(\left(\left(r_{o1}||r_{\pi 2}\right)g_{m2}r_{o2}\right)||\left(\left(r_{o3}||r_{\pi 4}\right)g_{m4}r_{o4}\right)\right)\text{ [1 pt]}$$

(b) Convert the small-signal parameters such that G_m, R_o and A_v are then a function of the quiescent collector current of Q_1, I_{C1}. For both NPN and PNP transistors, $V_A = 200\,\text{V}$, $\beta = 200$, and let $V_T = 26\,\text{mV}$. [3 pts]

Since α is very close to 1 (Since β is 200 then it's an error of about half a percent), we can use it as if $I_C \approx I_E$ for all transistors. This then assumes that I_C is exactly the same for all transistors.

This problem could be done with the actual value of α but that would still match $I_{C1} = -I_{C3}$ and $I_{C2} = -I_{C4}$, with these pairs being only slightly off.

This simplifies the output resistance and gain as

$$R_o=\left(r_o||r_\pi\right)\frac{a_o}{2} \tag{26}$$

$$A_v=g_m\left(r_o||r_\pi\right)\frac{a_o}{2} \tag{27}$$

The useful thing about expressing this in terms of intrinsic gain is that it is not at all dependent on the bias current. $a_o=\frac{V_A}{V_T}$ so long as it's biased in forward active.

G_m is the simplest to convert.

$$G_m=\frac{I_{C1}}{V_T}\text{ [1 pt]}$$

R_o contains a parallel resistance, which needs to be evaluated further.

$$R_o = \frac{\frac{V_A}{I_{C1}} \times \frac{\beta V_T}{I_{C1}}}{\frac{V_A + \beta V_T}{I_{C1}}} \frac{V_A}{2V_T} \tag{28}$$

$$R_o = \frac{V_A \times \beta V_T}{I_{C1}\left(V_A + \beta V_T\right)} \frac{V_A}{2V_T} \tag{29}$$

Since we have values of V_A, β, and V_T, we can show that βV_T is about 40 times less than V_A, and so V_A dominates.

$$R_o = \frac{V_A \times \beta V_T}{I_{C1} V_A} \frac{V_A}{2V_T} \tag{30}$$

$R_o = \frac{\beta}{2} \frac{V_A}{I_{C1}}$ [1 pt]

Which is a nice expression as that is also $\frac{\beta}{2} r_o$. Combining these two, the gain would be

$$A_v = \frac{I_{C1}}{V_T} \frac{\beta}{2} \frac{V_A}{I_{C1}} \tag{31}$$

$A_v = \frac{\beta}{2} \frac{V_A}{V_T}$ [1 pt]

Which is $\frac{\beta}{2} a_o$. Note that, if β had been infinite, the parallel resistance would instead allow the βV_T term to instead cancel in the output resistance, and the total gain would be in its most ideal form, $\frac{{a_o}^2}{2}$. It is because of this loading effect between the two stages is why this is not the case for a non-ideal, finite β, even a pretty large one such as $\beta = 200$.

The other thing to note is that while G_m and R_o are affected by the bias current, A_v is not. This reflects the same relationship for a single-stage CE with an ideal current source load, that a_o is independent of bias current and that only the ratio of g_m to r_o is affected.

(c) Given that the gain and output characteristics of the amplifier have been shown in relationship to the bias current, as a design problem how would you determine what to set the bias current as, based on what possible and reasonable parameters or specifications? [1 pt]

The first important thing to take note in choosing this bias current is that it should be within a reasonable range where all transistors can maintain being in forward active, as well as that r_o and r_π are large enough to be much greater than $\frac{1}{g_m}$, in order to satisfy a condition placed earlier in making assumptions for both G_m and R_o.

It has been shown that gain is almost wholly independent of bias current, and so the gain cannot be optimized much by choosing a specific bias current. However, since this amplifier may be loaded further, one method to choose is to set R_o such that any future loading effect is minimized. This implies a high I_{C1} in order to have a large G_m and small R_o, allowing the gain while loaded to still be close to $\frac{\beta}{2} a_o$. However, this also poses the problem of increasing total quiescent power. The power consumption is equivalent to $V_{CC} I_{C1}$ across the main branch of the amplifier (without any loading), and so increasing the bias current also increases power consumption. Another option, assuming that the load intended for this amplifier is very large, is to minimize I_{C1}, assuming that loading effects to not degrade the gain by too much.

Because no such load has been specified, either answer would be acceptable given that the proper assumptions on the load are stated. [1 pt]

3. **Multistage Amplifier**. For the given figure below, you are given the following assumptions: $\beta \gg 1$ and $|V_{BE}| = 0.7V$. The input and output DC quiescent voltages are set to 0.

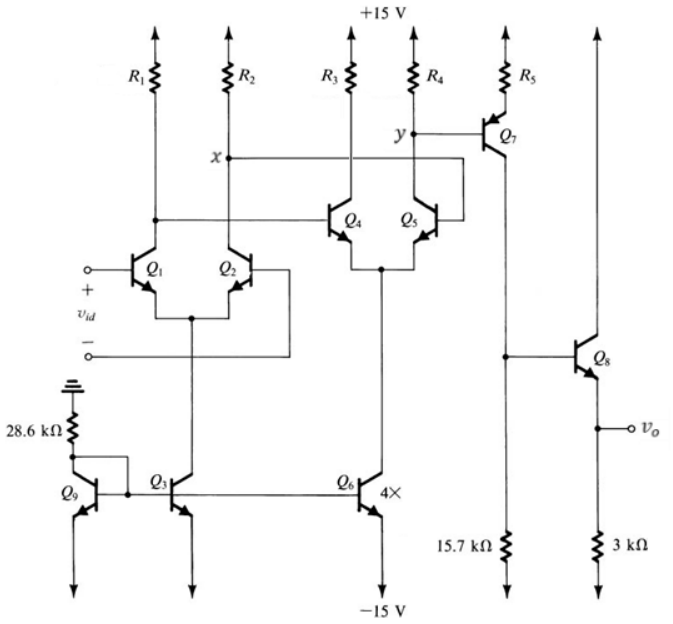

Figure 6: Multistage Amplifier

(a) Determine all the DC collector currents of each transistor. [2 pts]

Starting with the current mirror Q9-Q3, applying KCL yields,

$$I_{C9} = \frac{0 - 0.7 - (-15)}{28.6k\Omega} = 500\mu A = I_{C3} \tag{32}$$

For the current mirror Q9-Q6, the collector current on Q6 is 4 times (4X) the collector current on Q9. Therefore, $I_{C6} = 2mA$.

For the differential pairs Q1-Q2 and Q4-Q5, we can assume that $I_{C1} = I_{C2} = \frac{I_{C3}}{2}$ and $I_{C4} = I_{C5} = \frac{I_{C6}}{2}$. This gives us,

$$I_{C1} = I_{C2} = 250\mu A \tag{33}$$

$$I_{C4} = I_{C5} = 1mA \tag{34}$$

For the emitter-degenerated CE stage Q7, we can solve for I_{C7} (equal to $I_{15.7k\Omega}$) by applying KVL from V_O to $-15V$. This yields,

$$V_o = -V_{BE,8} + (I_{C7})(15.7k\Omega) + (-15V) \tag{35}$$

Rearranging the equation, we get,

$$I_{C7} = \frac{V_o + V_{BE,8} + 15V}{15.7k\Omega} = \frac{0 + 0.7V + 15V}{15.7k\Omega} = 1mA \tag{36}$$

For the last stage, applying KVL gives us,

$$I_{C8} = \frac{V_o - (-15V)}{3k\Omega} = \frac{0 + 15V}{3k\Omega} = 5mA \tag{37}$$

$$I_{C1} = I_{C2} = 250\mu A,\ I_{C3} = I_{C9} = 500\mu A,\ I_{C4} = I_{C5} = 1mA,\ I_{C6} = 2mA,\ I_{C7} = 1mA,\ I_{C8} = 5mA$$

(b) Given V_x= 6 V and V_y= 7.5 V, what are the values of resistors R_1 to R_5? [2 pts]

Given the collector currents were already obtained from (a), solving for the resistances is straightforward.

$$R_2 = R_1 = \frac{V_{DD} - V_x}{I_{C2}} = \frac{15V - 6V}{250\mu A} = 36k\Omega \tag{38}$$

$$R_4 = R_3 = \frac{V_{DD} - V_y}{I_{C4}} = \frac{15V - 7.5V}{1mA} = 7.5k\Omega \tag{39}$$

$$R_5 = \frac{V_{DD} + V_{BE,7} - V_y}{I_C7} = \frac{15V + (-0.7V) - 7.5V}{1mA} = 6.8k\Omega \tag{40}$$

$$R_1 = R_2 = 36k\Omega,\ R_3 = R_4 = 7.5k\Omega,\ R_5 = 6.8k\Omega$$

(c) Assuming ideal current sources, find the circuit gain A_v with loading in-between stages. Write your *complete* solution. [6 pts]

With loading in-between stages, we arrive at this expression for the overall gain:

$$A_v = A_{v1}\frac{R_{i2}}{R_{i2} + R_{o1}} A_{v2}\left(\frac{1}{2}\right)\frac{R_{i3}}{R_{i3} + \frac{R_{o2}}{2}} A_{v3}\frac{R_{i4}}{R_{i4} + R_{o3}} A_{v4} \tag{41}$$

The equation only considers half of A_{v2} and R_{o2} since the next stage only draws from half of the differential circuit in the 2nd stage. For the small-signal output resistance, given the assumption that there is no early effect, $V_A \gg 1$ and thus $r_o = \frac{V_A}{I_{C,Q}}$ is very large.

For the input differential stage 1 (Q1 and Q2),

$$R_{o1} = 2(r_{o1} \parallel R_1) \approx 2R_1 = \underline{72k\Omega} \tag{42}$$

$$A_{v1} = -g_{m1}(r_{o1} \parallel R_1) \approx -\frac{I_{C1}}{V_T}(R_1) = \underline{-346.15} \tag{43}$$

For the input differential stage 2 (Q4 and Q5) (note that $\beta = 200 \gg 1$),

$$R_{i2} = r_{\pi 4} + r_{\pi 5} = 2r_{\pi 4} = 2\left(\frac{\beta V_T}{I_{C4}}\right) = \underline{10.40k\Omega} \tag{44}$$

$$R_{o2} = 2(r_{o4} \parallel R_3) \approx 2R_3 = \underline{15k\Omega} \tag{45}$$

$$A_{v2} = -g_{m4}(r_{o4} \parallel R_3) \approx -\frac{I_{C4}}{V_T}(R_3) = \underline{-288.46} \tag{46}$$

For the 3rd stage (emitter-degenerated CE amplifier) on Q7,

$$R_{i3} = R_B \parallel r_{\pi 7}(1 + g_{m7}R_5) \approx r_{\pi 7} g_{m7} R_5 = \beta R_5 = \underline{1.36M\Omega} \tag{47}$$

$$R_{o3} \approx \underline{15.70k\Omega} \tag{48}$$

$$A_{v3} = \frac{-g_{m7}(15.7k\Omega)}{1 + g_{m7}(R_5)} = \underline{-2.32} \tag{49}$$

For 4th stage (emitter follower) on Q8,

$$R_{i4} = r_{\pi 8} = \frac{\beta V_T}{I_{C8}} = \underline{1.04k\Omega} \tag{50}$$

$$A_{v4} = \frac{g_{m8}(3k\Omega)}{1 + g_{m8}(3k\Omega)} \approx 0.99 = \underline{1} \tag{51}$$

The overall circuit gain A_v is therefore equal to,

$$A_v = (-346.15)\frac{10.40k\Omega}{10.40k\Omega + 72k\Omega}(-288.46)\left(\frac{1}{2}\right)\frac{1.36M\Omega}{1.36M\Omega + \frac{15k\Omega}{2}}(-2.32)\frac{1.04k\Omega}{1.04k\Omega + 15.70k\Omega}(1) = -903.24 \tag{52}$$

$$\boxed{A_v = -903.24}$$