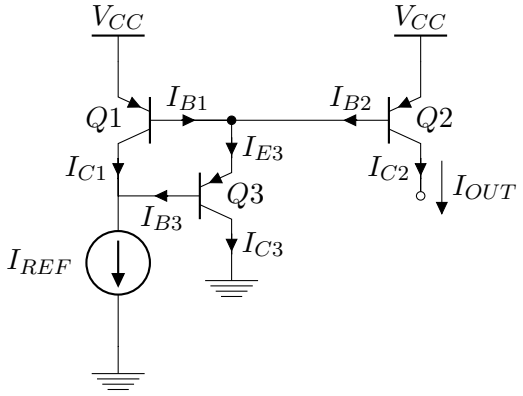
1. **Current Mirrors**

(a) From Figure 1, define first the necessary current flows in the circuit.



Since the BJTs are matched, they have the same $I_S = I_{S1} = I_{S2} = I_{S3}$ and $\beta = \beta_1 = \beta_2 = \beta_3$

$$\begin{aligned} V_{EB1} &= V_{EB2} \\ V_T \cdot ln\left(\frac{I_{C1}}{I_S}\right) &= V_T \cdot ln\left(\frac{I_{C2}}{I_S}\right) \\ I_{C1} &= I_{C2} = I_{OUT} \end{aligned}$$

KCL @ the Base node of $Q1$ and $Q2$:

$$\begin{aligned} I_{B1} + I_{B2} &= I_{E3} \\ I_{B1} + I_{B2} &= I_{B3} + I_{C3} \\ \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta} &= \frac{I_{C3}}{\beta}(\beta + 1) \\ I_{OUT}\left(\frac{2}{\beta}\right) &= \frac{I_{C3}}{\beta}(\beta + 1) \end{aligned}$$

KCL@ the collector node of $Q1$ and base node of $Q3$:

$$\begin{aligned} I_{REF} &= I_{C1} + I_{B3} \\ I_{REF} &= I_{OUT} + \frac{I_{C3}}{\beta} \end{aligned}$$

Combining the two KCL equations:

$$\begin{aligned} I_{REF} &= I_{OUT} + I_{OUT}\left(\frac{2}{\beta(\beta+1)}\right) \\ I_{REF} &= I_{OUT}\left(1 + \frac{2}{\beta(\beta+1)}\right) \\ \boxed{I_{OUT} &= I_{REF}\left(\frac{1}{1 + \frac{2}{\beta(\beta+1)}}\right)} \end{aligned}$$

(b) The expression of a simple current mirror has only a factor of β but from the derived expression, it has a β^2 factor so this configuration is better for mirroring currents with lesser errors.

(c) $Q3$ supplies the currents I_{B1} and I_{B2} without drawing much current from the current source I_{REF} if β is large enough so that $I_{OUT} \approx I_{REF}$.

From Figure 2, start from the $M6$ KVL branch and we see that $I_{SD6} = I_2$:

$$V_{DD} - V_{SG6} - I_2R_2 = 0$$
$$V_{DD} - \left(\sqrt{\frac{I_2}{k_p}} + |V_{THp}|\right) - I_2R_2 = 0$$
$$R_2 = \frac{V_{DD} - \left(\sqrt{\frac{I_2}{k_p}} + |V_{THp}|\right)}{I_2}$$
$$R_2 = \frac{2.5V - \left(\sqrt{\frac{50\mu A}{200\mu A/V^2}} + |-0.45V|\right)}{50\mu A}$$
$$R_2 = \frac{2.5V - (0.5V + 0.45V)}{50\mu A}$$
$$\boxed{R_2 = 31k\Omega}$$

We already know that $V_{SG6} = 0.95V$ and it forces the V_{SG5} of $M5$ to be equal to V_{SG6} implying that $I_{SD5} = I_{SD6}$. We can also imply that $I_{DS4} = I_{DS2} = I_{SD5} = 50\mu A$ because it lies in a single branch. We can now solve for the V_{GS} of $M4$ and $M2$:

$$V_{GS4} = \sqrt{\frac{I_{DS4}}{kn}} + V_{THn}$$
$$= \sqrt{\frac{50\mu A}{312.5\mu A/V^2}} + 0.4V$$
$$V_{GS4} = 0.8V = V_{GS2}$$

V_{GS2} forces the V_{GS} of $M1$ so $V_{GS1} = V_{GS2}$. Therefore the current $I_{DS1} = I_{DS2}$. Since there is an assumption that $M1$ operates at minimum V_{DS} to still remain in saturation, it is exactly the value of $(V_{GS1} - V_{THn})$.

$$V_{DS1_{min}} = V_{GS1} - V_{THn}$$
$$= 0.8V - 0.4V$$
$$V_{DS1_{min}} = 0.4V$$

$M1$, $M3$, and R_1 lies in one branch so the current $I_{DS3} = I_{DS1} = I_{R_1} = I_{OUT}$. This implies that $\boxed{I_{OUT} = 50\mu A}$. We can solve for V_{GS3}:

$$V_{GS3} = \sqrt{\frac{I_{OUT}}{k_n}} + V_{THn}$$
$$= \sqrt{\frac{50\mu A}{312.5\mu A}} + 0.4V$$
$$V_{GS3} = 0.8V$$

KVL @ the inner loop of $M2$, $M4$, $M3$, and R_1:

$$V_{GS2} + V_{GS4} = V_{GS3} + V_{R_1} + V_{DS1_{min}}$$
$$1.6V = 0.8V + V_{R_1} + 0.4V$$
$$V_{R_1} = 0.4V = \frac{I_{OUT}}{R_1}$$
$$R_1 = \frac{V_{R_1}}{I_{OUT}} = \frac{0.4V}{50\mu A}$$
$$\boxed{R_1 = 8k\Omega}$$

2. **More Current Mirrors**

(a) First we note that $I_{DS4} = I_{DS1} = 20\mu A$. Looking at M1 first,

$$I_{D1} = k_{M1}(V_{GS1} - V_{th})^2$$

$$V_{GS1} = \sqrt{\frac{I_{D1}}{k_{M1}}} + V_{th} = 0.25 + 0.6 = 0.85V$$

Since the source terminals of M1 and M2 are shorted to ground, we can say that $V_{G1} = V_{G2} = 0.85V$. Also note that $I_O = I_{DS3} = I_{DS2}$. From here we can use the MOS current characteristic equation for M2 to solve for I_O.

$$I_O = I_{DS2} = k_{M2}(V_{GS2} - V_{th})^2 = 3.2m\frac{A}{V^2}(0.85V - 0.6V)^2 = 200\mu A$$

$I_O = 200\mu A$ (1 pt)

(b) Since the gate voltage of M2 has already been solved in the previous item, we need only to find the gate voltage of M3. Looking at M4 and since M4 and M1 have the same characteristics, M4's gate to source voltage is also the same $V_{GS4} = 0.85V$.

$$V_{GS4} = V_{G4} - V_{S4} = 0.85V$$

$$V_{G4} = 0.85 + V_{S4}$$

Where $V_{S4} = V_{D1} = V_{G1} = 0.85V$. Thus,

$$V_{G4} = 0.85 + V_{G1} = 0.85 + 0.85 = 1.7V = V_{G3}$$

$V_{G2} = 0.85V$ (0.5 pts) $V_{G3} = 1.7V$ (0.5 pts)

(c) The values of the small-signal parameters are as follows:

$$g_{m3} = g_{m2} = 2k_{M2}(V_{GS2} - V_{th}) = 1.6mS$$

$$g_{m4} = g_{m1} = 2k_{M1}(V_{GS1} - V_{th}) = 0.16mS$$

$$r_{o4} = r_{o1} = \frac{1}{\lambda I_{D1}} = 500k\Omega$$

$$r_{o3} = r_{o2} = \frac{1}{\lambda I_{D2}} = 50k\Omega$$

The small-signal equivalent of the circuit is shown in Fig. 6 below.

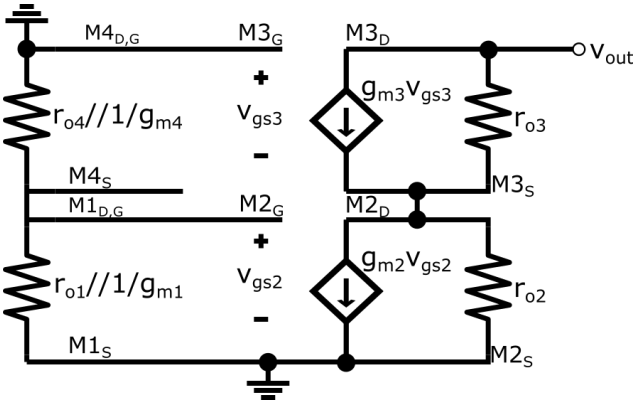


Figure 6: Cascoded MOS current mirror small-signal equivalent circuit

(d) By applying a test voltage and measuring the resulting current, we can determine the output resistance of the circuit as follows.

$$R_O = \frac{V_{test}}{I_{test}} = \frac{1}{I_{test}}$$

Looking at Fig. 6, the path from the drain of M4 to the source of M1 is tied to ground on both sides, thus we can say that the current thru that path is 0. With that we can also say that, $v_{gs2} = 0$ since there is no voltage drop across the parallel combination of r_{o1} and $\frac{1}{g_{m1}}$. We can then simplify the circuit as shown in Fig. 7 below.

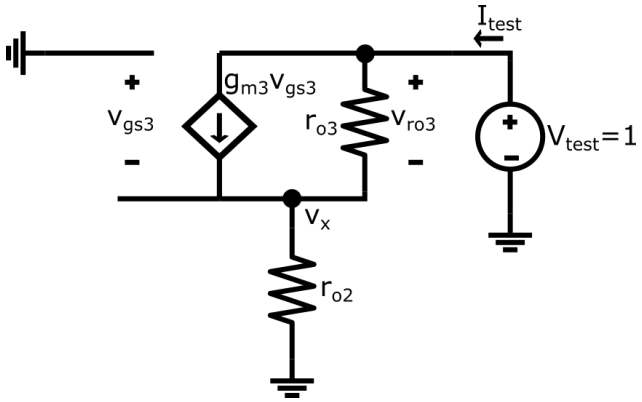


Figure 7: Simplified small-signal equivalent of Fig. 6

From Fig. 7,

$$v_x = -v_{gs3} = I_{test} r_{o2}$$

$$v_{gs3} = -I_{test} r_{o2}$$

Doing KCL at the output node,

$$I_{test} = g_{m3} v_{gs3} + \frac{v_{ro3}}{r_{o3}} = g_{m3} v_{gs3} + \frac{1 + v_{gs3}}{r_{o3}}$$

where,

$$v_{ro3} = V_{test} - v_x = 1 + v_{gs3}$$

Substitute $-I_{test} r_{o2}$ for v_{gs3},

$$I_{test} = -I_{test} g_{m3} r_{o2} + \frac{1}{r_{o3}} - I_{test} \frac{r_{o2}}{r_{o3}}$$

$$I_{test} \left(1 + r_{o2} \left(g_{m3} + \frac{1}{r_{o3}}\right)\right) = \frac{1}{r_{o3}}$$

$$I_{test} = \frac{\frac{1}{r_{o3}}}{1 + r_{o2} \left(g_{m3} + \frac{1}{r_{o3}}\right)}$$

$$R_O = \frac{V_{test}}{I_{test}} = \frac{1}{\frac{\frac{1}{r_{o3}}}{1 + r_{o2}\left(g_{m3} + \frac{1}{r_{o3}}\right)}} = \frac{1 + r_{o2}\left(g_{m3} + \frac{1}{r_{o3}}\right)}{\frac{1}{r_{o3}}} = r_{o3} + g_{m3} r_{o2} r_{o3} + r_{o2}$$

$R_O = 4.1M\Omega$ (0.5 pts). (1.5 pts) will be given for the solution.

(e) Since "Early effect" or channel length modulation effects can be ignored, all the transistors have $r_o \to \infty$ and by applying a test voltage at node V_3 and getting the resulting current, we can determine the resistance seen at V_3. From Fig. 8.

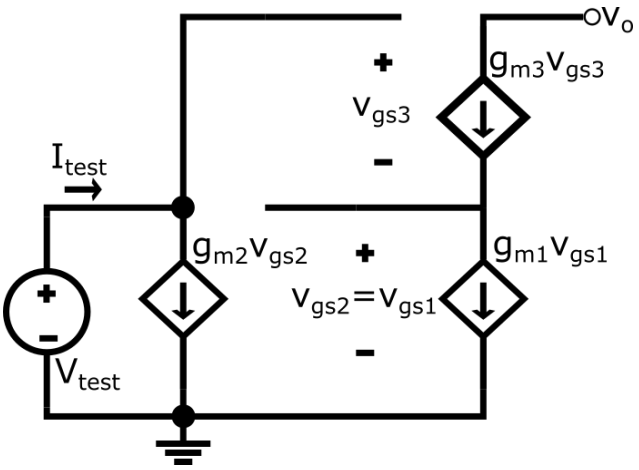


Figure 8: Small-signal equivalent of the Wilson current mirror

$$I_{test} = g_{m2} v_{gs2}$$

$$v_{gs3} = V_{test} - v_{gs2} \rightarrow V_{test} = v_{gs3} + v_{gs2}$$

Also, since all the transistors are identical we can say that $v_{gs3} = v_{gs2}$

$$R_I = \frac{V_{test}}{I_{test}} = \frac{v_{gs3} + v_{gs2}}{g_{m2} v_{gs2}} = \frac{2 v_{gs2}}{g_{m2} v_{gs2}} = \frac{2}{g_{m2}}$$

$R_I = \frac{2}{g_{m2}} \Omega$ (0.5 pts). (1.5 pts) will be given for the solution.

(f) If β is considered to be high then we can say that $I_O = I_{REF} = 10\mu A$ and that for $I_O = I_{REF}$, the base-emitter voltages of the transistors must also be the same ($V_{BE1} = V_{BE2} = V_{BE3}$). From the given V_{BE} at a specified output current and ignoring Early effect,

$$1mA = I_s e^{\frac{0.8}{V_T}}$$

Also,

$$I_{REF} = 10\mu A = I_s e^{\frac{V_{BE}}{V_T}}$$

Dividing the two,

$$\frac{I_{REF}}{1m} = \frac{I_s e^{\frac{V_{BE}}{V_T}}}{I_s e^{\frac{0.8}{V_T}}} = e^{\frac{V_{BE} - 0.8}{V_T}}$$

$$\ln\left(\frac{I_{REF}}{1m}\right) = \frac{V_{BE} - 0.8}{V_T}$$

$$V_{BE} = V_T \ln\left(\frac{I_{REF}}{1m}\right) + 0.8 = 0.6803V$$

Doing KVL on the loop from R going through the BE-junctions of Q3, Q1 and Q2,

$$I_O R = -V_{BE3} + V_{BE1} + V_{BE2}$$

$$R = \frac{V_{BE}}{I_O} = \frac{0.6803V}{10\mu A} = 68.03k\Omega$$

$R = 68.03k\Omega$ (0.5 pts). (1.5 pts) will be given for the solution.