EEE 51 Assignment 6 Answer Key

2nd Semester SY 2018-2019
Due: 5pm Tuesday, March 19, 2019 (Rm. 220)

Instructions: Write legibly. Show all solutions and state all assumptions. Write your full name, student number, and section at the upper-right corner of each page. Start each problem on a new sheet of paper. Box or encircle your final answer.

Answer sheets should be color coded according to your lecture section. The color scheme is as follows:

THQ – yellow
THU – white
WFX – pink

1. **Single-Ended Operational Amplifier.**

   A single-ended operational amplifier was created with a topology slightly similar to the LF35 op amp which is shown in Figure 1. You are tasked to verify the approximate characteristics of the design at $T = 300\,\text{K}$. The MOSFETs have $k = \frac{\mu C_{ox}}{2}\frac{W}{L} = 250\,\mu\text{A/V}^2$ and $\lambda = 0.001\,\text{V}^{-1}$. The BJTs have the following: $\beta = 100$ and $V_A = 50\,\text{V}$. Assume that the current sources and diodes are ideal ($V_{min} = 0\,\text{V}$ and $\text{R} \to \infty$ for the current sources; and $V_f = 0.7\,\text{V}$, $\text{R}_{\text{ON}} = 0\,\Omega$, and $\text{R}_{\text{OFF}} \to \infty$ for the diodes) and that the transistors are in their necessary operating regions (saturation for MOSFETs and forward active for BJTs). **Show your complete solution and round off to the required value to merit a maximum of full points**.

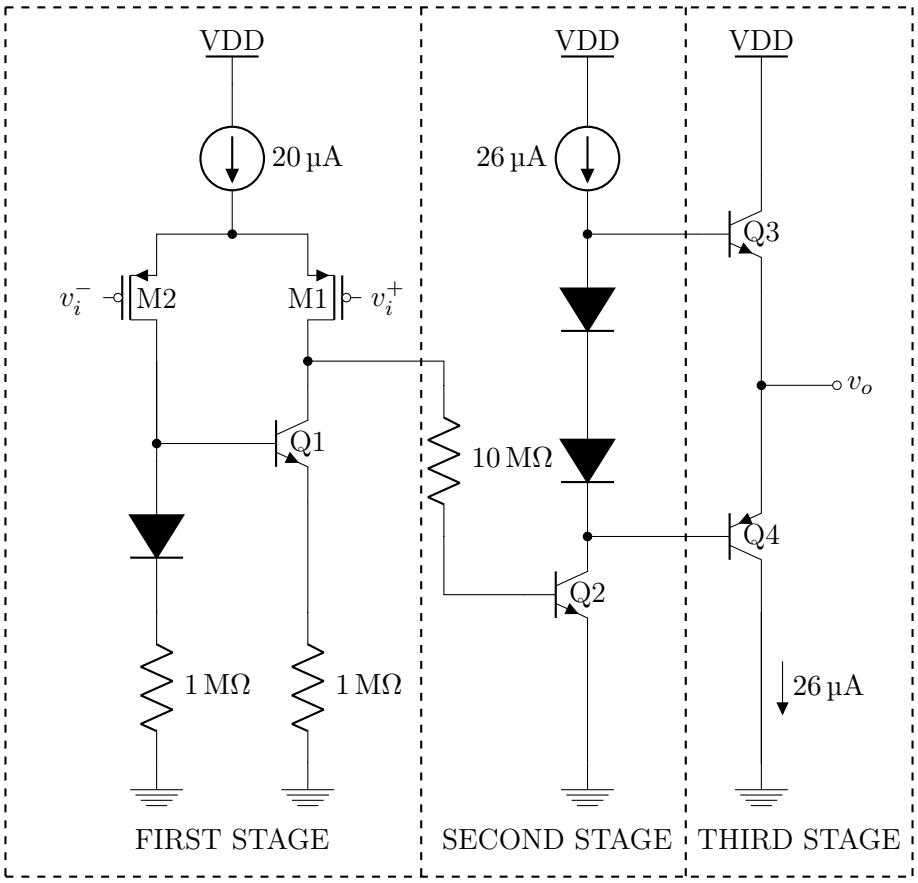


Figure 1: The Single-Ended Operational Amplifier

(a) What should be the value (rounded to the nearest ten thousands) of the load resistance to get maximum power? (2 pts)

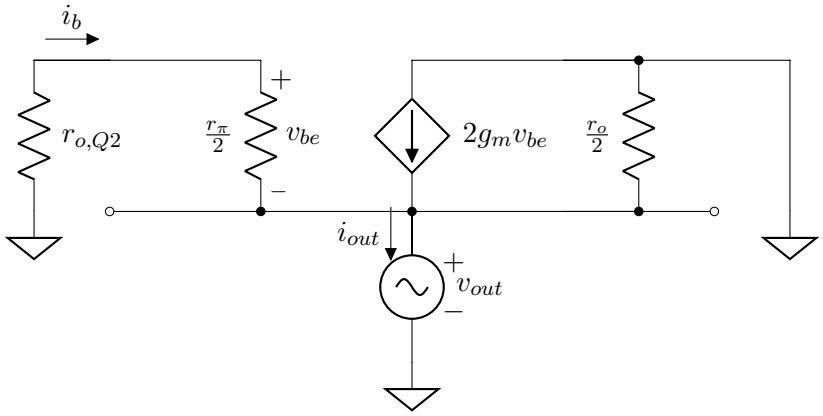
- To get maximum power, the load resistance R_{load} must be the same as the output resistance of the amplifier R_O, which is also the output resistance of the third stage (Class AB amplifier).
- The last stage is just two parallel transistors in common collector configuration.
- The output resistance of Q_2 is common to both transistors. The output resistance of a common collector with a series base resistance of $2r_{o,Q2}$ (seen from the emitter) is approximately:

$$\begin{aligned} R_e &\approx \frac{1}{g_m} + \frac{2r_{o,Q2}}{\beta+1} \\ &\approx \frac{V_T}{I_{C3}} + \frac{2\frac{V_A}{I_{C2}}}{\beta+1} \\ &\approx \frac{26m}{26u} + \frac{2\frac{50}{26u}}{100+1} \\ &\approx 40\,\text{k}\Omega \end{aligned}$$

- Since they are in parallel...

$$\boxed{R_{load} \approx R_O \approx 20\,\text{k}\Omega}$$

- The problem may also be solved by drawing the equivalent small-signal model



$$\begin{aligned} i_{out} &= \frac{v_{out}}{\frac{r_\pi}{2}+r_{o,Q2}} + 2g_m v_{out}\frac{\frac{r_\pi}{2}}{\frac{r_\pi}{2}+r_{o,Q2}} + \frac{v_{out}}{\frac{r_o}{2}} \\ &= 2v_{out}\left(\frac{1}{r_\pi+2r_{o,Q2}} + \frac{g_m r_\pi}{r_\pi+2r_{o,Q2}} + \frac{1}{r_o}\right) \\ R_O = \frac{v_{out}}{i_{out}} &= \frac{1}{2\left(\frac{1}{r_\pi+2r_{o,Q2}} + \frac{g_m r_\pi}{r_\pi+2r_{o,Q2}} + \frac{1}{r_o}\right)} \\ &= \frac{(r_\pi+2r_{o,Q2})\,r_o}{2\,(r_o+g_m r_\pi r_o+r_\pi+2r_{o,Q2})} \\ &= \frac{(r_\pi+2r_o)\,r_o}{2\,(\beta r_o+r_\pi+3r_o)} \\ &= \frac{((100k)+2\,(1.923M))\,(1.923M)}{2\,((100)\,(1.923M)+(100k)+3\,(1.923M))} \\ &\approx 19\,146.420\,\Omega \\ &\approx \boxed{20\,\text{k}\Omega} \end{aligned}$$

(b) Find the value of the following rounded to the nearest whole number:

i. Gain of the first stage with respect to v_i^+ (ie: $A_{v1} = \frac{v_{o1}^-}{v_i^+}$) (2 pts)

- The first stage is just a common source amplifier.
- Note that Q_1 is in a common emitter with resistor degeneration configuration.

$$\begin{aligned} A_{v1} &= -g_{m1}\left(r_{o,M1}||R_{O,Q1}||R_{IN,Q2}\right) \\ &= -\sqrt{4kI_D}\left[\frac{1}{\lambda I_D}||\left(1+\frac{I_{C1}}{V_T}\left(1M\right)\right)\frac{V_A}{I_{C1}}||\left(10M+\frac{\beta V_T}{I_{C2}}\right)\right] \\ &= -100u\left(9130042.395\right) \\ &\approx -913.004 \\ &\approx \boxed{-913} \end{aligned}$$

ii. Gain of the second stage (2 pts)

- The second stage is a common emitter amplifier.
- The diodes are ideal. Assuming they are forward-biased, we can replace them by 2 DC sources of 0.7 V each. Since we are analyzing in small-signal, these sources are shorted.
- Find the input resistance of the third stage first
- Q_3 has a load resistance equal to the output resistance of Q_4. Q_4 has a load resistance equal to the output resistance of Q_3. Each of them therefore have an input resistance of:

$$R_{IN,3} = R_{IN,4} = r_\pi + (\beta+1)\frac{1}{g_m}$$

- The base of Q_3 and Q_4 are in parallel therefore:

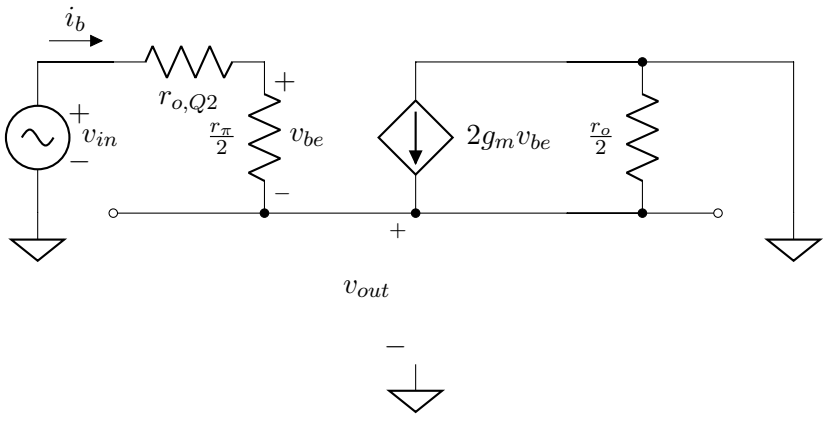
$$R_{IN} = \frac{r_\pi + \frac{\beta+1}{g_m}}{2}$$

- Thus, the gain is:

$$\begin{aligned} A_{v2} &= -g_{m2}\left(r_{o,Q2}||R_{IN}\right) \\ &= -1m\left(1.923M||100.5k\right) \\ &= -1m\left(95.509k\right) \\ &\approx -95.509 \\ &\approx \boxed{-96} \end{aligned}$$

iii. Gain of the third stage (2 pts)

- We use the following small-signal model to solve for the gain:



- Perform KCL at the output node:

$$\begin{aligned}
\frac{v_{in}-v_{out}}{\frac{r_\pi}{2}+r_{o,Q3}}+2g_m\left(v_{in}-v_{out}\right)\frac{r_\pi}{r_\pi+r_{o,Q2}}-\frac{v_{out}}{\frac{r_o}{2}}&=0\\
2v_{in}\left(\frac{1}{r_\pi+2r_{o,Q2}}+\frac{g_m r\pi}{r_\pi+2r_{o,Q2}}\right)&=2v_{out}\left(\frac{1}{r_\pi+2r_{o,Q2}}+\frac{g_m r\pi}{r_\pi+2r_{o,Q2}}+\frac{1}{r_o}\right)\\
v_{in}\left(\frac{1+g_m r_\pi}{r_\pi+2r_{o,Q2}}\right)&=v_{out}\left(\frac{r_o+g_m r_\pi r_o+r_\pi}{\left(r_\pi+2r_{o,Q2}\right)r_o}\right)\\
v_{in}\left(\frac{1+\beta}{r_\pi+2r_{o,Q2}}\right)&=v_{out}\left(\frac{r_o+\beta r_o+r_\pi+2r_{o,Q2}}{\left(r_\pi+2r_{o,Q2}\right)r_o}\right)\\
A_{v3}=\frac{v_{out}}{v_{in}}&=\frac{\left(\beta+1\right)r_o}{r_o+\beta r_o+r_\pi+2r_{o,Q2}}\\
&=\frac{101\left(1.923M\right)}{100\left(1.923M\right)+100k+3\left(1.923M\right)}\\
&\approx 0.980\\
&=\boxed{1}
\end{aligned}$$

(c) Give the value of the differential gain ($\frac{v_o}{v_{id}}$) approximate to the nearest ten thousands. (2 pts)

- We don't multiply the answers from (b) immediately. Note that at (b.i), we only solved for $\frac{v_{o1}^-}{v_i^+}$. Assuming that $v_{id}=v_i^+-v_i^-=2v_i^+$, then:

$$\begin{aligned}
A_{v1,single}&=\frac{A_{v1}}{2}\\
&\approx -456.502
\end{aligned}$$

- The gain of the amplifier is thus:

$$\begin{aligned}
A_v&=A_{v1,single}A_{v2}A_{v3}\\
&=\left(-456.502\right)\left(-95.509\right)\left(0.980\right)\\
&\approx 42731.757\\
&\approx \boxed{\text{43000 (or 43k)}}\text{ to }\boxed{\text{44000 (or 44k)}}
\end{aligned}$$

- Subscribe2PewDiePie

2. **Simple Two-stage Operational Amplifier.** Consider the circuit shown in Fig. 2. Given the following: $V_{DD} = 3V$, $I_{REF} = 1mA$, $k_p = 6.25mA/V^2$, $k_n = 19.75mA/V^2$, $V_{th,n} = 0.7V$, $|V_{th,p}| = 0.8V$.

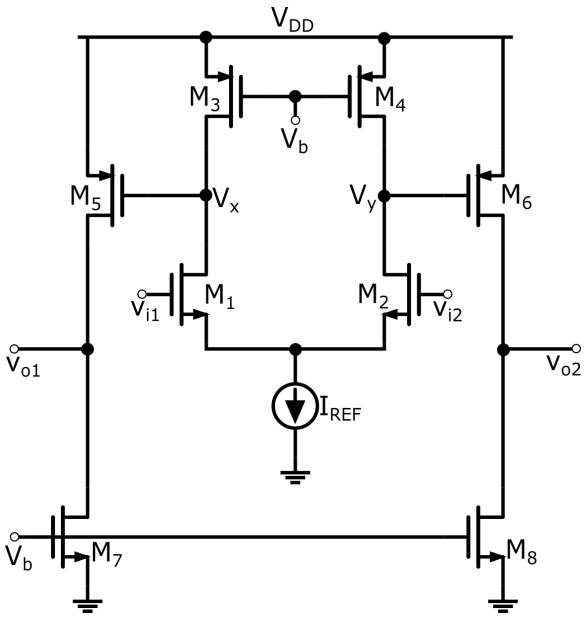


Figure 2: 2-stage Operational Amplifier Circuit

(a) What is the CM voltage level needed at the drains of M_3 and M_4 so that the current through the M_5-M_7 and M_6-M_8 is $1mA$? [2 pts]

$$I_{SD5,6} = k_p(V_{SG5,6} - |V_{th,p}|)^2 = 1mA$$

$$V_{SG5,6} = \sqrt{\frac{I_{SD5,6}}{k_p}} + |V_{th,p}| = 1.2V$$

$$V_{x,y} = V_{DD} - V_{SG5,6} = 3 - 1.2 = 1.8V$$

$V_{x,y} = 1.8V$ (1 pt). (1 pt) will be given for the solution.

(b) Keeping the values obtained in (a), what is the maximum input CM level? [2 pts]

With the given drain voltages of M_3 and M_4 (and consequently M_1 and M_2 respectively), the maximum input CM level is found by keeping M_1 and M_2 to operate in the saturation region, and at the boundary between saturation and linear regions of operation, we have the following relation,

$$V_{DS} = V_{GS} - V_{th}$$

Rearranging the above equation,

$$V_{GS1,2} = V_{i1,i2} - V_{S1,2} = V_{DS1,2} + V_{th,n} = V_{x,y} - V_{S1,2} + V_{th,n}$$

Which leaves us with,

$$V_{i1,i2max} = V_{x,y} + V_{th,n} = 1.8V + 0.7V = 2.5V$$

This makes sense since having a $V_{in} > 2.5V$, would result to a $V_{GS} - V_{th}$ value, which is usually called the overdrive voltage, that is greater than the drain-source voltage which means that the transistors M_1 and M_2 would operate in the linear region if $V_{x,y}$ is kept at $1.8V$.

$V_{i1,i2max} = 2.5V$ (1 pt). (1 pt) will be given for the solution.

(c) For all transistors, evaluate the following:

i. The drain-to-source currents, I_{DS}. [0.5 pts]
Still keeping the values obtained from (a), the drain-to-source current of M_5 and M_6 is $-1mA$ while it is $1mA$ for M_7 and M_8. Transistor pairs M_3-M_4 and M_1-M_2 are identical having the same k and V_{th}, thus the drain-to-source current of M_3 and M_4 is $-\frac{1}{2}I_{REF} = -0.5mA$ while it is $0.5mA$ for M_1 and M_2.

ii. The gate-to-source voltages, $|V_{GS}|$. [1 pt]
The gate-to-source voltage for M_5 and M_6 have been solved already. Using the same equation as before would allow us to solve for the gate-to-source voltage of the other transistors as follows:

$$V_{SG} = \sqrt{\frac{I_{SD}}{k_p}} + |V_{th,p}|$$

$$V_{GS} = \sqrt{\frac{I_{DS}}{k_n}} + V_{th,n}$$

For PMOS and NMOS devices respectively. For M_1 and M_2,

$$V_{GS} = \sqrt{\frac{0.5mA}{19.75mA/V^2}} + 0.7 = 0.86V$$

For M_3 and M_4,

$$V_{SG} = \sqrt{\frac{0.5mA}{6.25mA/V^2}} + 0.8 = 1.08V$$

For M_7 and M_8,

$$V_{GS} = \sqrt{\frac{1mA}{19.75mA/V^2}} + 0.7 = 0.925V$$

iii. g_m. [1 pts]

The following is used to compute for the g_m of the transistors: $\sqrt{4k_nI_{DS}}$ and $\sqrt{4k_pI_{SD}}$ for NMOS and PMOS respectively. For M_1 and M_2,

$$g_m = \sqrt{4(19.75mA/V^2)(0.5mA)} = 6.285mS$$

For M_3 and M_4,

$$g_m = \sqrt{4(6.25mA/V^2)(0.5mA)} = 3.535mS$$

For M_5 and M_6,

$$g_m = \sqrt{4(6.25mA/V^2)(1mA)} = 5mS$$

For M_7 and M_8,

$$g_m = \sqrt{4(19.75mA/V^2)(1mA)} = 8.888mS$$

iv. r_o. Use $\lambda_n = 0.1V^{-1}$ and $\lambda_p = 0.2V^{-1}$. [0.5 pt]

The following is used to compute for the r_o: $\frac{1}{\lambda_n I_{DS}}$ or $\frac{1}{\lambda_p I_{SD}}$ for NMOS and PMOS respectively. The values are computed using these formulas and is indicated in the table below.

Parameter	M1	M2	M3	M4	M5	M6	M7	M8
I_{DS} (mA)	0.5	0.5	-0.5	-0.5	-1	-1	1	1
$\|V_{GS}\|$ (V)	0.86	0.86	1.08	1.08	1.2	1.2	0.925	0.925
g_m (mS)	6.285	6.285	3.535	3.535	5	5	8.888	8.888
r_o (kΩ)	20	20	10	10	5	5	10	10

Checking for this part will be all or nothing per row.

(d) Calculate the overall voltage gain of the circuit. [2 pts]

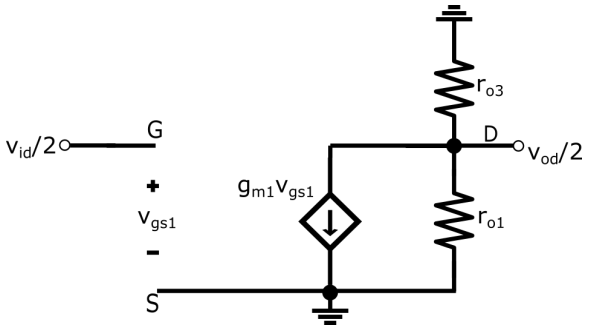


Figure 3: 1st-stage Small Signal Half Circuit Model

Refer to Fig. 3 for the half-circuit of the 1st stage (which is composed of transistors M_1-M_4), solving for the gain,

$$\frac{v_{od}}{2} = -g_{m1}v_{gs1}(r_{o1}//r_{o3}) = -g_{m1}\frac{v_{id}}{2}(r_{o1}//r_{o3})$$

$$A_{v,1} = \frac{\frac{v_{od}}{2}}{\frac{v_{id}}{2}} = \frac{v_{od}}{v_{id}} = -g_{m1}(r_{o1}//r_{o3}) = -41.9$$

For the 2nd stage, refer to Fig. 4 below.

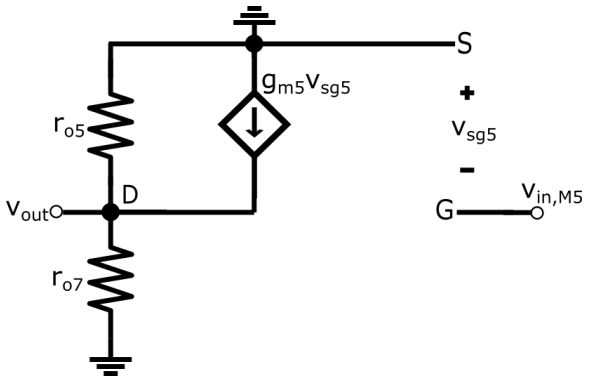


Figure 4: 2nd-stage Small Signal Model

$$v_{out} = g_{m5}v_{sg5}(r_{o5}//r_{o7}) = g_{m5}(-v_{in,M5})(r_{o5}//r_{o7})$$

$$A_{v,2} = \frac{v_{out}}{v_{in,M5}} = -g_{m5}(r_{o5}//r_{o7}) = -16.67$$

The overall gain is simply the product of the gains of the first and second stage.

$A_{v,total} = A_{v,1}A_{v,2} = 698.3$ (0.5 pts). (1.5 pts) will be given for the solution.

(e) What is the maximum output swing? [1 pt]

The output swing is determined by keeping the transistors in the 2nd stage (M_5-M_7 and M_6-M_8) in saturation. The upper limit is found by keeping M_5/M_6 in saturation:

$$V_{o,max} = V_{DD} - |V_{OD5}| = 3 - (1.2 - 0.8) = 2.6V$$

Where $|V_{OD5}| = V_{GS5} - |V_{th,p}|$ denotes the overdrive voltage of M_5. The lower limit on the other hand is found by keeping M_7/M_8 in saturation:

$$V_{o,min} = V_{OD,7} + V_{SS} = (0.925 - 0.7) + 0 = 0.225V$$

The single-ended output swing is then $2.6 - 0.225 = 2.375V$ but since the circuit is configured to have a differential output then,

$V_{o,swing} = 2 * 2.375 = 4.75V$ (0.5 pts). (0.5 pts) will be given for the solution.

TOTAL: 20 points.