# EEE 51 Assignment 1 Solution

2nd Semester SY 2017-2018
Due: 5pm Tuesday, Jan. 30, 2018 (Rm. 220)

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*Instructions:* Write legibly. Show all solutions and state all assumptions. Write your full name, student number, and section at the upper-right corner of each page. Start each problem on a new sheet of paper. Box or encircle your final answer.

1. **BJT DC Biasing 1.** Consider the circuit shown below. Provided that $V_{CC} = 5V$, $V_{IN} = 3V$ $R_{B1} = 200k\Omega$, $R_{C1} = 2k\Omega$, $R_{C2} = 200\Omega$, $\beta_{Q1} = 100$, $\beta_{Q2} = 50$, $V_{BE1,on} = V_{BE2,on} = 0.7V$ and $V_{CE1,sat} = V_{CE2,sat} = 0.2V$ determine the following:

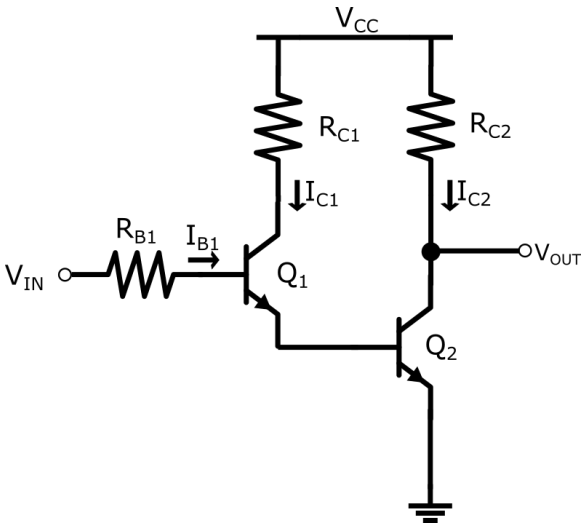


Figure 1: BJT Darlington Pair

(a) $I_{B1}$, $I_{C1}$ and $V_{CE1}$. State all necessary assumptions. [3 pts]

First, assume that transistors Q1 and Q2 are ON and Q1 is operating in the forward-active region. $I_{B1}$ can be computed by doing KVL from $V_{IN}$ to ground through the base-emitter junctions of Q1 and Q2.

$$V_{IN} = I_{B1}R_{B1} + V_{BE1,on} + V_{BE2,on} \tag{1}$$

Re-writing (1),

$$I_{B1} = \frac{V_{IN} - V_{BE1,on} - V_{BE2,on}}{R_{B1}} = \frac{3 - 1.4}{200k} = 8\mu A \tag{2}$$

| $I_{B1} = 8\mu A$ [1 pt] |
|---|

Since Q1 is assumed to be in the forward-active region,

$$I_{C1} = \beta_{Q1}I_{B1} = 100 * 8\mu A = 800\mu A \tag{3}$$

To compute for $V_{CE1}$, we write the KVL equation from $V_{CC}$ to ground through Q1 and Q2.

$$V_{CC} = I_{C1}R_{C1} + V_{CE1} + V_{BE2,on} \tag{4}$$

Re-writing (4),

$$V_{CE} = V_{CC} - I_{C1}R_{C1} - V_{BE2,on} = 5 - (2k)(800\mu) - 0.7 = 2.7V \tag{5}$$

Since $I_{B1} > 0$ and $V_{CE1} > V_{CE1,sat}$ our assumption that Q1 is in forward-active is correct [1 pt]
As such, $I_{C1} = 800\mu A$ [0.5 pts] and $V_{CE1} = 2.7V$ [0.5 pts]

(b) $I_{C2}$ and $V_{OUT}$. State all necessary assumptions. [2 pts]

Let us assume this time instead that Q2 is operating in the saturation region. To prove that Q2 is indeed in saturation, the following must be satisfied:

- $I_{B2} > 0$, $I_{C2} > 0$ and
- $I_{C2} < \beta_{Q2} I_{B2}$

From Fig. 1, we can say that $I_{B2} = I_{E1} = (\beta_{Q1} + 1) I_{B1} = 808\mu A > 0$. As for $I_{C2}$, it can be determined by writing the KVL equation from $V_{CC}$ to ground through Q2.

$$I_{C2} = \frac{V_{CC} - V_{CE2,sat}}{R_{C2}} = \frac{5 - 0.2}{200} = 24mA \tag{6}$$

$$I_{C2} = 24mA < 40.4mA = \beta_{Q2} I_{B2} \tag{7}$$

Since $I_{B2} < 0$, $I_{C2} < 0$ and $I_{C2} < \beta_{Q2} I_{B2}$ our assumption that Q2 is in saturation is correct [1 pt]
As such, $I_{C2} = 24mA$ [0.5 pts] and $V_{OUT} = V_{CE2,sat} = 0.2V$ [0.5 pts]

Conversely, one can begin this question by assuming that Q2 is operating in the forward-active region. Doing so, one would eventually find $I_{C2} = \beta_{Q2} I_{B2} = 40.4mA$ and $V_{OUT} = V_{CC} - R_{C2} I_{C2} = -3.08V$ which is obviously less than $V_{CE2,sat}$ thus making the assumption that Q2 is in forward-active to be incorrect.

(c) Suppose we want to achieve a $V_{OUT}$ of at least $1V$ by changing $R_{B1}$. Determine the minimum value of $R_{B1}$ needed to get the desired $V_{OUT}$. Again, state all necessary assumptions. [2 pts]

Previously, we've found that Q2 is actually operating in the saturation region, for the output voltage to be 1V, this time, Q2 must operate in the forward-active region. With that in mind, we express $V_{OUT}$ by writing the KVL equation from $V_{CC}$ to ground through Q2.

$$V_{OUT} = V_{CC} - R_{C2} I_{C2} \tag{8}$$

Also,

$$I_{C2} = \beta_{Q2} I_{B2} = \beta_{Q2} I_{E1} = \beta_{Q2} (\beta_{Q1} + 1) I_{B1} \tag{9}$$

And,

$$I_{B1} = \frac{V_{IN} - V_{BE1,on} - V_{BE2,on}}{R_{B1}} \tag{10}$$

Combining (10) and (9) into (8),

$$V_{OUT} = V_{CC} - R_{C2} \beta_{Q2} (\beta_{Q1} + 1) \frac{V_{IN} - V_{BE1,on} - V_{BE2,on}}{R_{B1}} \tag{11}$$

$$V_{OUT} = 5 - (200)(50)(101) \frac{3 - 0.7 - 0.7}{R_{B1}} = 1V \tag{12}$$

Solving for $R_{B1}$,

$R_{B1,min} = 404k\Omega$ [1 pt]
Also, since $I_{B2} = \frac{I_{C2}}{\beta_{Q2}} = 400\mu A > 0$ and $V_{CE2} = V_{OUT} > V_{CE2,sat}$, Q2 is indeed in forward-active [1 pt]

2. **BJT DC Biasing 2**. To understand her EEE 51 class better, Mina plans to implement the circuit in Figure 2. $V_{CC} = 12V$, $R_1 = 1k\Omega$, $R_2 = 500\Omega$, $R_3 = 129k\Omega$, and $R_4 = 1k\Omega$. For transistor $Q_1$, $V_A \to \infty$ and $\beta = 150$. For both $Q_1$ and $Q_2$, $|V_{BE,on}| = 0.7V$ and $|V_{CE,sat}| = 0.2V$. In this circuit, the current through resistor $R_1$ should be $5mA$, and the voltage across $R_4$ should be $10V$. Round your answers up to four decimal places.

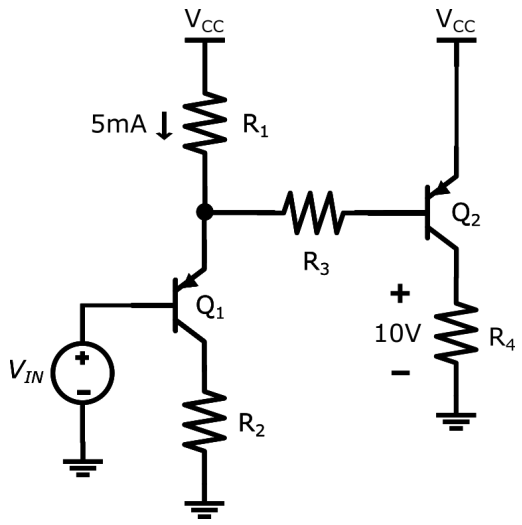


Figure 2: Mina's Circuit

(a) What is the value of $V_{IN}$? [2 pts]

Assume first that $Q_1$ is operating in the forward active region. We can use KVL around the loop that includes $V_{CC}$, $R_1$, $V_{EB1}$ and $V_{IN}$ to solve for $V_{IN}$.

$$V_1 = I_1 R_1 = (5mA)(1k\Omega) = 5V \tag{13}$$

$$V_{EB1} = 0.7V \tag{14}$$

$$V_{IN} = V_{CC} - R_1 I_1 - V_{EB1} = 12 - 5 - 0.7 = 6.3V \tag{15}$$

Check if $Q_1$ is indeed in the forward active region by solving for the value of $V_{EC1}$. To do this, we must first solve for $I_{C2}$ using the equation for a PNP BJT:

$$I_E = I_B + I_C = \frac{I_C}{\beta} + I_C \tag{16}$$

Both $I_{E1}$ and $I_{C1}$ are still unknown, but $I_{E1}$ can be computed using KCL:

$$I_{E1} = I_1 + I_3 \tag{17}$$

To get $I_3$, the voltage drop across $R_3$ must be known. Since $V_{EC2} = 2V > V_{EC,sat} = 0.2V$, we can assume that $V_{EB2} = 0.7V$. $I_3$ can now be computed using:

$$I_3 = \frac{V_{B2} - V_{E1}}{R_1} = \frac{11.3 - 7}{129k\Omega} = 33.3333\mu A \tag{18}$$

Using equations (15), (16), and (17), we can compute the value of $I_{C1}$.

$$I_{C1} = 5mA = I_2 \tag{19}$$

Now, $V_{EC1}$ can be computed using KVL.

$$V_{CC} - I_1 R_1 - V_{EC1} - I_2 R_2 = 0 \tag{20}$$

$$V_{EC1} = 4.5V \tag{21}$$

This means that $Q_1$ is in the forward the active region. [1 pt]

Our assumption of the operating region of $Q_1$ is correct, so our computed value for $V_{IN}$ is also correct.

$V_{IN} = 6.3V$ [1 pt]

(b) Since all components but $Q_2$ are available at the lab, Mina asks her friends for help to build the circuit. Momo, Jennie, and Irene each offer her a box that contains a BC556A, BC556B, and BC557C respectively. (Datasheet: *https://www.mouser.com/ds/2/302/nxp_bc556_57-1188849.pdf*) To make the circuit operate with the given requirements, which of her friends should Mina choose and why? You can assume that $V_A \to \infty$ for $Q_2$. (Hint: $h_{FE}$ is the same as $\beta$.) [2 pts]

Mina needs a transistor that will be able to provide the base and collector currents of $Q_2$. In the previous question, we have already solved for $I_{B2}$, which is equal to $I_3$. We can also solve for $I_{C2}$ since the voltage across $R_4$ is known. After this, we can compute the value of $\beta$ required for $Q_2$.

$$I_4 = I_{C2} = \frac{V_4}{R_4} = \frac{10V}{1k\Omega} = 10mA \tag{22}$$

$$\beta_2 = \frac{I_{C2}}{I_{B2}} = \frac{10mA}{33.3333\mu A} = 300 \tag{23}$$

$\beta_2 = 300$ [1 pt]
Using the datasheet, it can be seen that for a collector current of 10mA, the $\beta$ provided by the BC556B is 300, which is what Mina needs. Therefore, Mina should choose Jennie. [1 pt]

(c) Mina disconnects $R_3$ from $Q_1$ and decides to test only the left side of the circuit. She replaces $R_1$ with a 2kΩ resistor and $R_2$ with a 1.25kΩ resistor, and she biases $Q_1$ with a voltage of 4V. What is the voltage that Mina expects to measure across $R_2$? [2 pts]

Since the bias voltage for $Q_1$ changed, the transistor currents will also change. To get $I_E$, assume first that $Q_1$ is in the forward active region.

$$V_E = V_{EB} + V_{IN} = 0.7 + 4 = 4.7V \tag{24}$$

$$I_1 = I_E = \frac{V_{CC} - V_E}{R_1} = \frac{12 - 4.7}{2k\Omega} = 3.65mA \tag{25}$$

To get the voltage across $R_2$, we must first solve for $I_C$.

$$I_2 = I_C = (\frac{\beta}{1+\beta})I_E = (\frac{150}{1+150})(3.65mA) = 3.6258mA \tag{26}$$

$$V_2 = I_C R_2 = (3.6258mA)(1.25k\Omega) = 4.5323V \tag{27}$$

Check if the assumption is correct by solving for $V_{EC}$ through KVL:

$$V_{EC} = V_{CC} - I_E R_1 - I_C R_2 = 12 - (3.65mA)(2k\Omega) - (3.6258mA)(1.25k\Omega) = 0.1677V < V_{EC,sat} = 0.2V \tag{28}$$

$V_{EC} = 0.1677V < V_{EC,sat} = 0.2V$ [1 pt]

which means that $Q_1$ is in saturation, and $V_{EC} = 0.2V$. The correct $V_2$ can now be solved using KVL.

$$V_2 = V_{CC} - I_E R_1 - V_{EC} = 12 - (3.65mA)(2k\Omega) - 0.2 = 4.5V \tag{29}$$

| $V_2 = 4.5V$ [1 pt] |
|---|

3. **MOSFET DC Biasing**. In the circuit shown in Figure 3, the current across the load resistance $R_L$ is 1 mA. Given that $R_L = 4k\Omega$, $R_3 = 1600\Omega$, and $V_{DD} = 12V$. For both transistors, $|V_{TH}| = 3V$, k = $1000\,\mu A/V^2$ and $\lambda = 0$. Assume that there is no body effect.

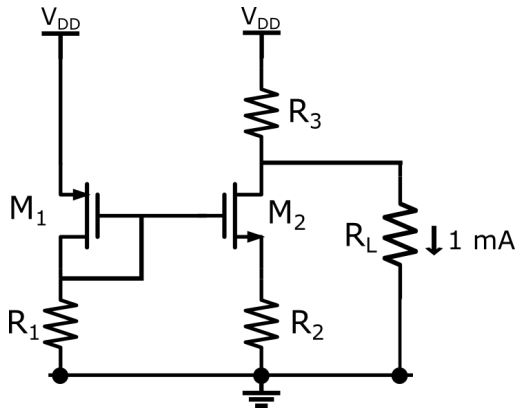


Figure 3: MOSFET Circuit

(a) What is the drain current of transistor M2? [2 pts]

Since we already know the current flowing through the load resistor and the value of its resistance, we can find the voltage $R_L$.

$$V_L = I_L R_L = (1\,\text{mA})(4\,\text{k}\Omega) = 4\,\text{V} \tag{30}$$

By KVL at the load side, we can find the voltage across $R_3$.

$$V_{R_3} = V_{DD} - V_L = 12\,\text{V} - 4\,\text{V} = 8\,\text{V} \tag{31}$$

Therefore the current flowing through $R_3$ is

$$I_{R_3} = \frac{V_{R_3}}{R_3} = \frac{8\,\text{V}}{1600\,\Omega} = 5\,\text{mA} \tag{32}$$

By KCL at the drain node of M2,

$$I_{D_2} = I_{R_3} - I_L = 5\,\text{mA} - 1\,\text{mA} \tag{33}$$

| $I_{D_2} = 4\,\text{mA}$ [2 pt] |
|---|

(b) What is the maximum resistance of resistor R2 such that M2 remains in the saturation region? State all necessary assumptions. [3 pts]

The two conditions for saturation are:

$$V_{GS} > V_{TH} \tag{34}$$

$$V_{DS} > V_{GS} - V_{TH} \tag{35}$$

Also, the drain current equation for MOSFET devices at saturation is

$$I_D = k(V_{GS} - V_{TH})^2 \tag{36}$$

Due to condition for saturation shown in equation 35, there is a lower limit for the drain-source voltage ($V_{DS}$) for a given current. Since the load voltage is constant, and it is equal to the sum of the drain-source voltage of M2 and of voltage drop across $R_2$, there is an upper limit to the possible resistance of $R_2$.

The minimum value of $V_{DS}$ to remain in saturation is:

$$V_{DS_2} = V_{GS_2} - V_{TH} \tag{37}$$

Using the answer in (a) and k = $1000\,\mu A/V^2$, we can get the value of $V_{GS_2}$ using equation 36.

$$V_{GS_2} = \sqrt{\frac{I_{D_2}}{k}} + V_{TH} = 5\,\text{V} \tag{38}$$

| $V_{GS_2} = 5\,\text{V}$ [2 pt] |
|---|

Therefore, $V_{DS} = 2\,\text{V}$. By KVL,

$$V_{R_2} = V_L - V_{DS} = 2\,\text{V} \tag{39}$$

$R_2$ can be obtained by using $V_{R_2}$ and $I_{D_2}$

$$R_2 = \frac{V_{R_2}}{I_{D_2}} = 500\,\Omega \tag{40}$$

| $R_2 = 500\,\Omega$ [1 pt] |
|---|

(c) What must be the resistance of R1 in order to supply the correct voltage to the gate of M2? Use the values from your calculations in (b). [2 pts]

First, we must take note that M1 is a PMOS transistor.

From the previous problem, we know that $V_{DS_2} = 2V$ and $V_{R_2} = 2V$. From this, we can solve for the gate voltage of M2, $V_G$.

$$V_G = V_{GS_2} + V_{R_2} = 5V + 2V = 7V \tag{41}$$

Therefore, the gate-source of M1 is given by

$$V_{GS_1} = V_G - V_{DD} = 7V - 12V = -5V \tag{42}$$

Since M1 is diode connected, we know that $V_{GS_1} = V_{DS_1}$. Therefore, $|V_{DS_1}|$ is always greater than $|V_{GS_1}| - |V_{TH}|$ which means that it is in the saturation region. Also, the drain current is equal to the current across resistor $R_1$. Using equation 36,

$$I_{R_1} = \frac{V_{DD} - V_{GS_1}}{R_1} = I_{DS_1} = k(|V_{GS_1}| - |V_{TH}|)^2 \tag{43}$$

$$R_1 = \frac{V_{DD} - |V_{GS_1}|}{k(|V_{GS_1}| - |V_{TH}|)^2} = 1750\,\Omega \tag{44}$$

| $R_1 = 1750\,\Omega$ [2 pt] |
|---|

TOTAL: 20 points.