



# **EEE 51: Second Semester 2017 – 2018**

## **Lecture 25**

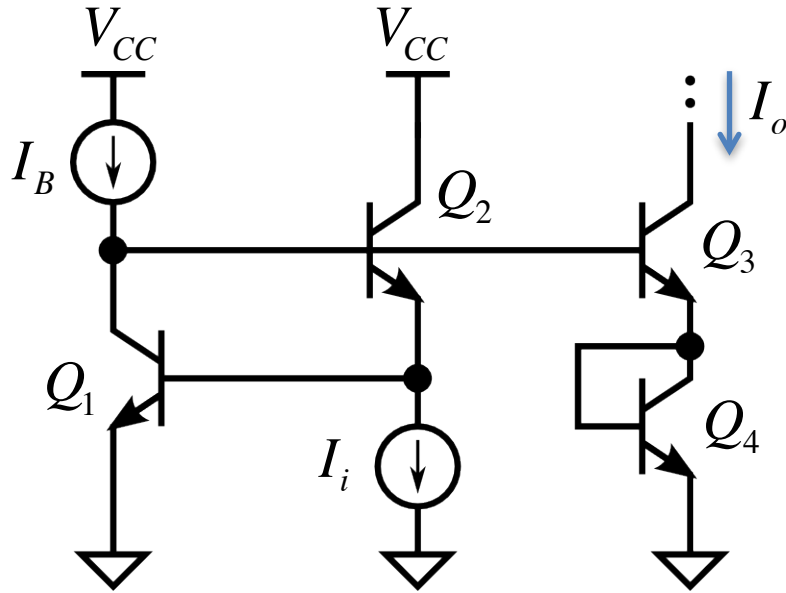
# Analog Computation and Course Summary

# Analog Computation Circuits

- Translinear Circuits
  - Nonlinear Function Synthesis
- Addition
- Subtraction



# The Square-Root Circuit



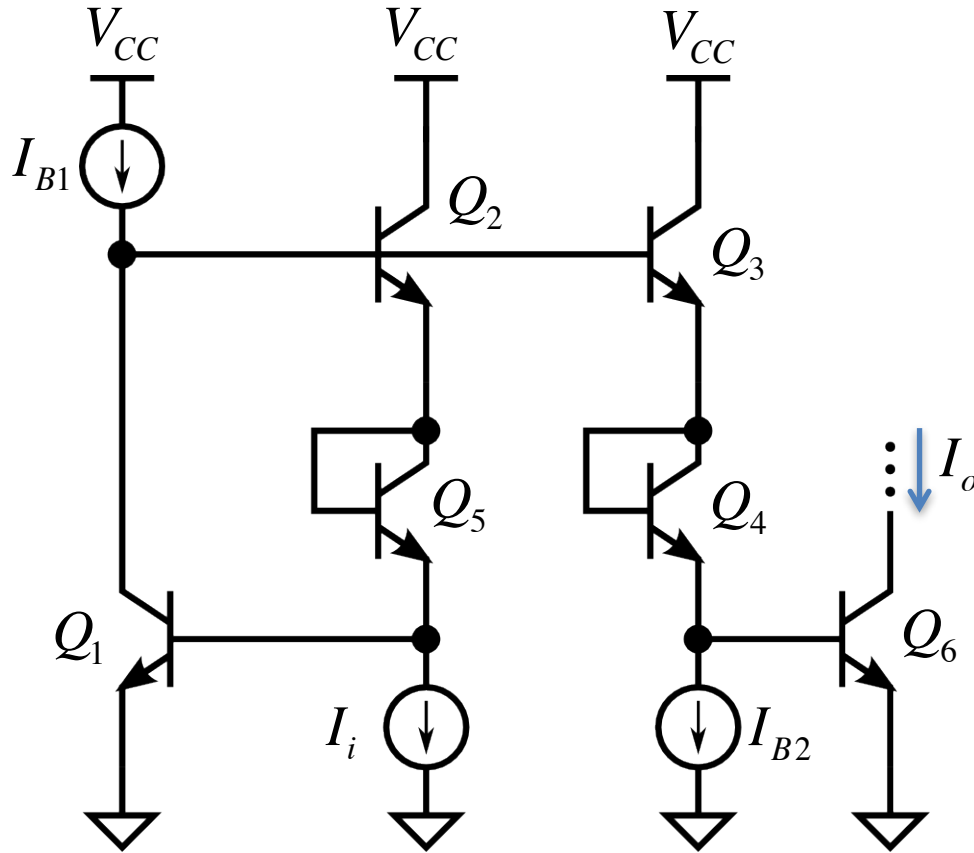
$$V_{BE1} + V_{BE2} - V_{BE3} - V_{BE4} = 0$$

$$V_T \ln\left(\frac{I_B}{I_{S1}}\right) + V_T \ln\left(\frac{I_i}{I_{S2}}\right) - V_T \ln\left(\frac{I_o}{I_{S3}}\right) - V_T \ln\left(\frac{I_o}{I_{S4}}\right) = 0$$

$$\ln\left(\frac{I_B}{I_{S1}} \frac{I_i}{I_{S2}}\right) = \ln\left(\frac{I_o}{I_{S3}} \frac{I_o}{I_{S4}}\right)$$

$$I_o = \sqrt{I_i} \sqrt{I_B} \sqrt{\frac{I_{S3}}{I_{S1}} \frac{I_{S4}}{I_{S2}}}$$

# The Square-Law Circuit



$$V_{BE1} + V_{BE5} + V_{BE2} = V_{BE3} + V_{BE4} + V_{BE6}$$

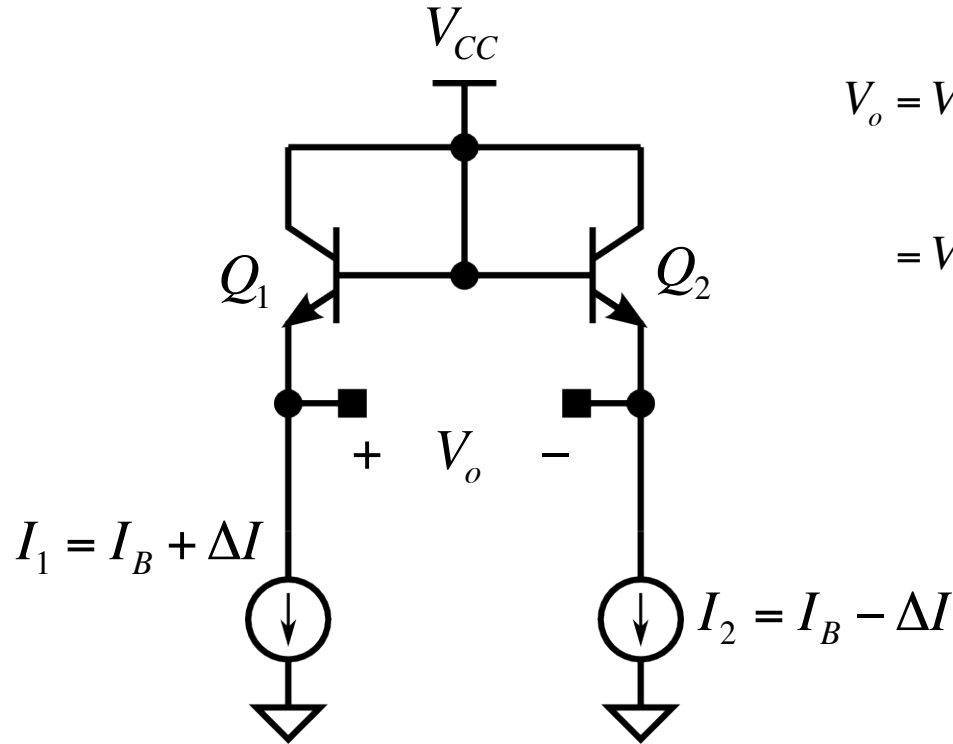
$$V_{BE} = V_T \ln \left( \frac{I_C}{I_{S1}} \right)$$

$$\ln \left( \frac{I_{B1}}{I_{S1}} \frac{I_i}{I_{S5}} \frac{I_i}{I_{S2}} \right) = \ln \left( \frac{I_{B2}}{I_{S3}} \frac{I_{B2}}{I_{S4}} \frac{I_o}{I_{S6}} \right)$$

$$I_o = I_i^2 \frac{I_{B1}}{I_{B2}^2} \frac{I_{S3}}{I_{S1}} \frac{I_{S4}}{I_{S5}} \frac{I_{S6}}{I_{S2}}$$



# The $\tanh^{-1}$ Circuit

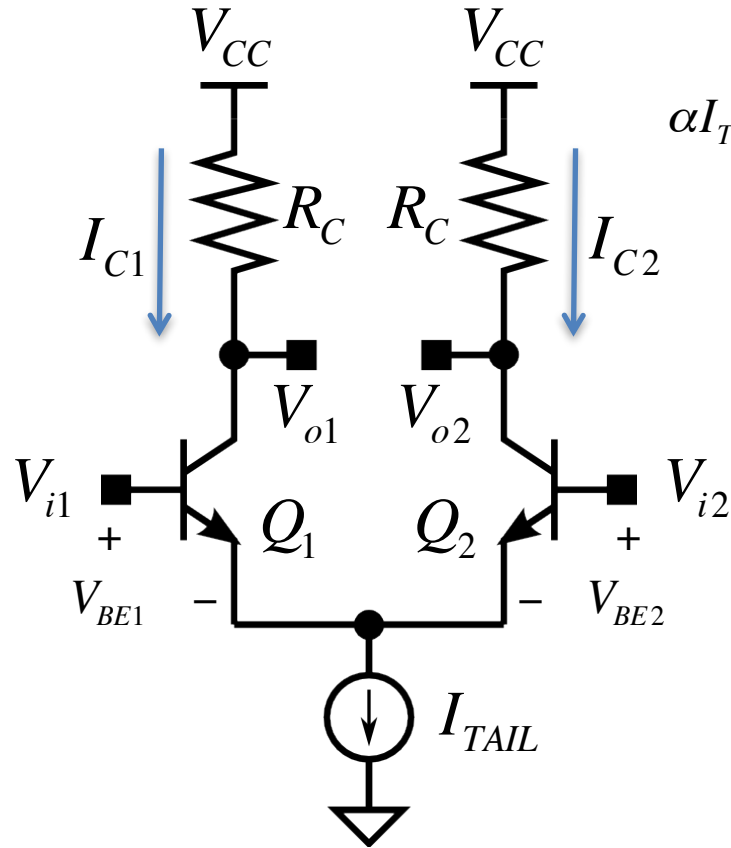


$$\begin{aligned} V_o &= V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_B + \Delta I}{I_S}\right) - V_T \ln\left(\frac{I_B - \Delta I}{I_S}\right) \\ &= V_T \ln\left(\frac{I_B + \Delta I}{I_B - \Delta I}\right) \end{aligned}$$

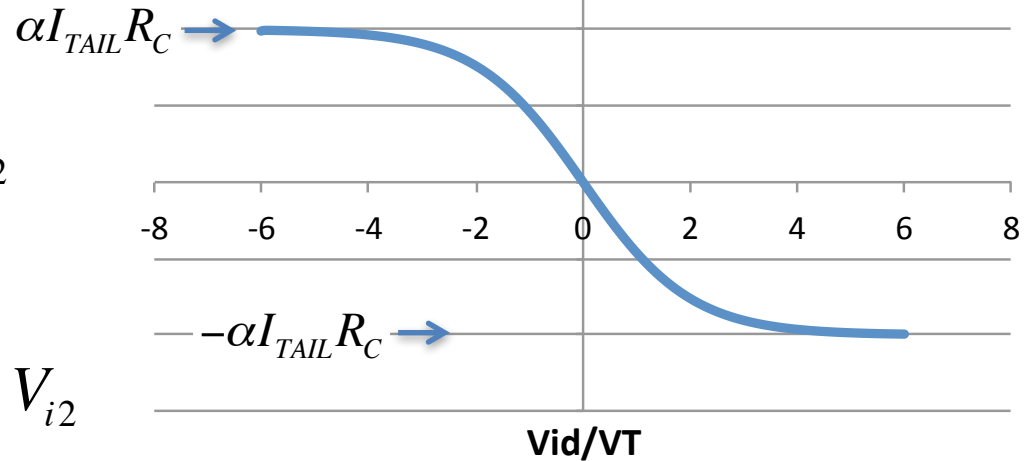
$$\text{Note: } \tanh^{-1} x = \frac{1}{2} \ln\left(\frac{1+x}{1-x}\right)$$

$$V_o = 2V_T \tanh^{-1}\left(\frac{\Delta I}{I_B}\right)$$

# Linearization



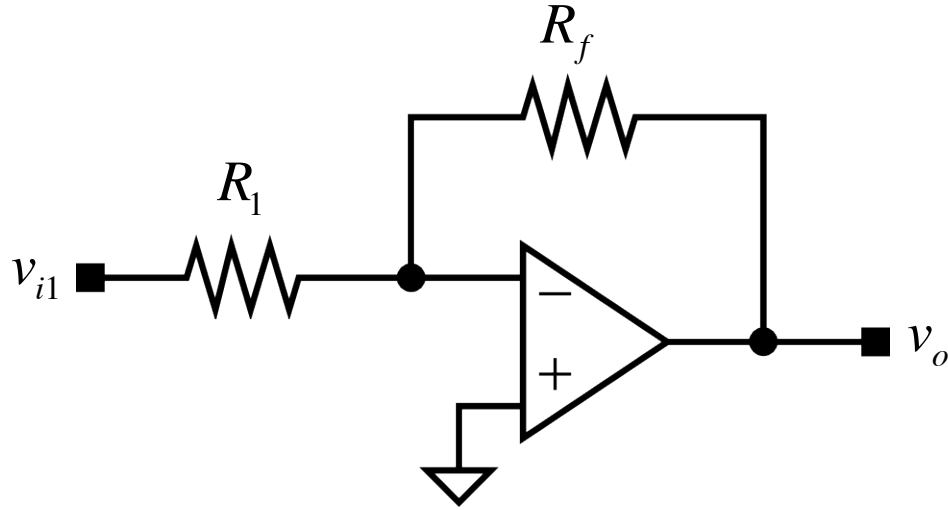
$$V_{od} = V_{o1} - V_{o2}$$



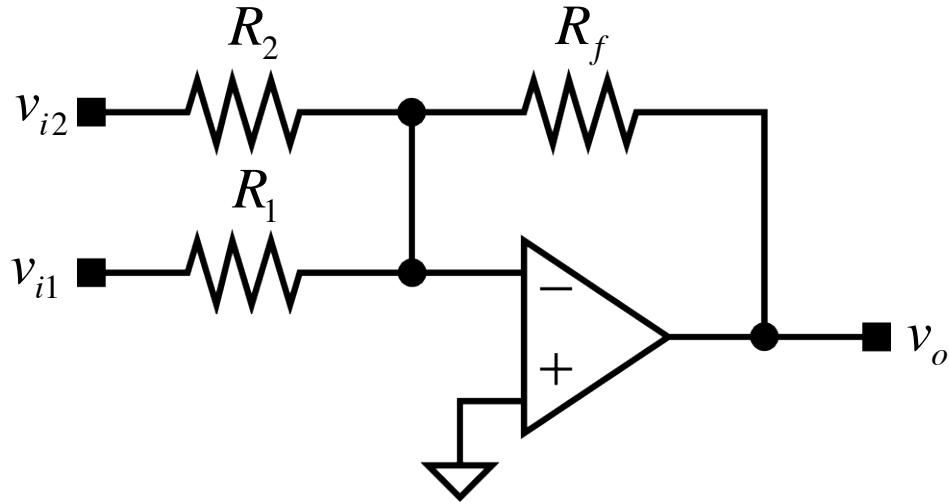
$$V_{od} = \alpha I_{TAIL} R_C \tanh\left(-\frac{V_{id}}{2V_T}\right)$$

Can this function be made linear?

# Analog Addition



# Analog Addition





# Subtraction





# COURSE SUMMARY

# EEE 51 – Linear Transistor Amplifiers

- Transistor Models
  - Large signal  $\rightarrow$  Biasing
  - Small signal  $\rightarrow$  Linearization  $\rightarrow$  2-port equivalents
- Basic Amplifiers
  - Single-stage amplifiers
  - Current mirrors
  - Differential amplifiers
- Cascaded Amplifiers
  - Operational amplifiers



# EEE 51 – Linear Transistor Amplifiers

- Frequency Response
  - Capacitances (and inductances)
  - Poles, zeros, Bode plots (magnitude/phase)
- Feedback
  - Basic topologies, loop gain, closed-loop gain
  - Advantages → input/output impedances, bandwidth, linearity
  - Cost → Stability



# EEE 51 – Linear Transistor Amplifiers

- Stability
  - Positive feedback vs. negative feedback
  - Metrics → phase margin, gain margin
  - Effect of the loop gain
- Oscillators
  - Barkhausen's Criteria
  - Phase-shift model, generalized (LC) model, negative resistance
  - Crystal oscillators
- Translinear Circuits
  - Analog computation → examples: square-root, square-law,  $\tanh^{-1}$
  - Addition, subtraction, etc.



# Example: AM Receiver

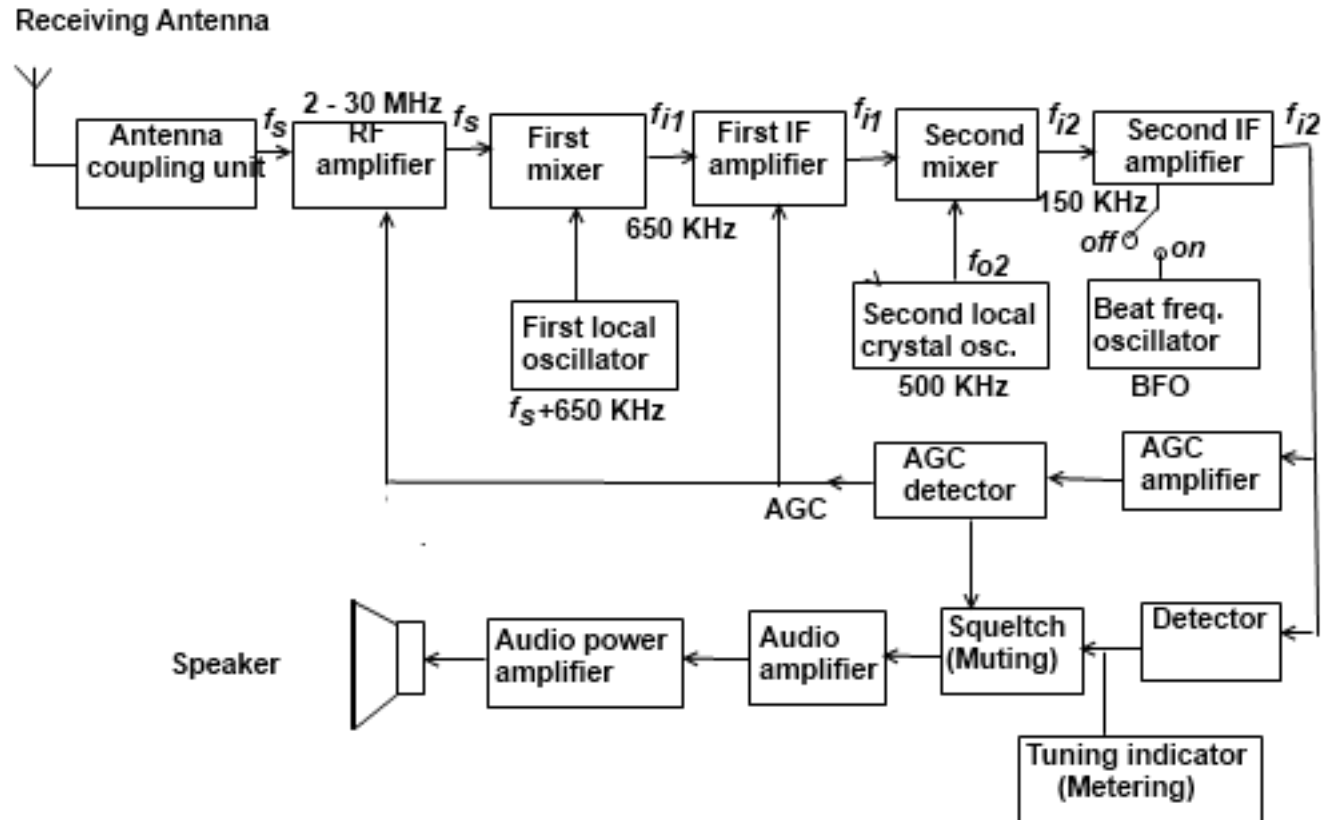
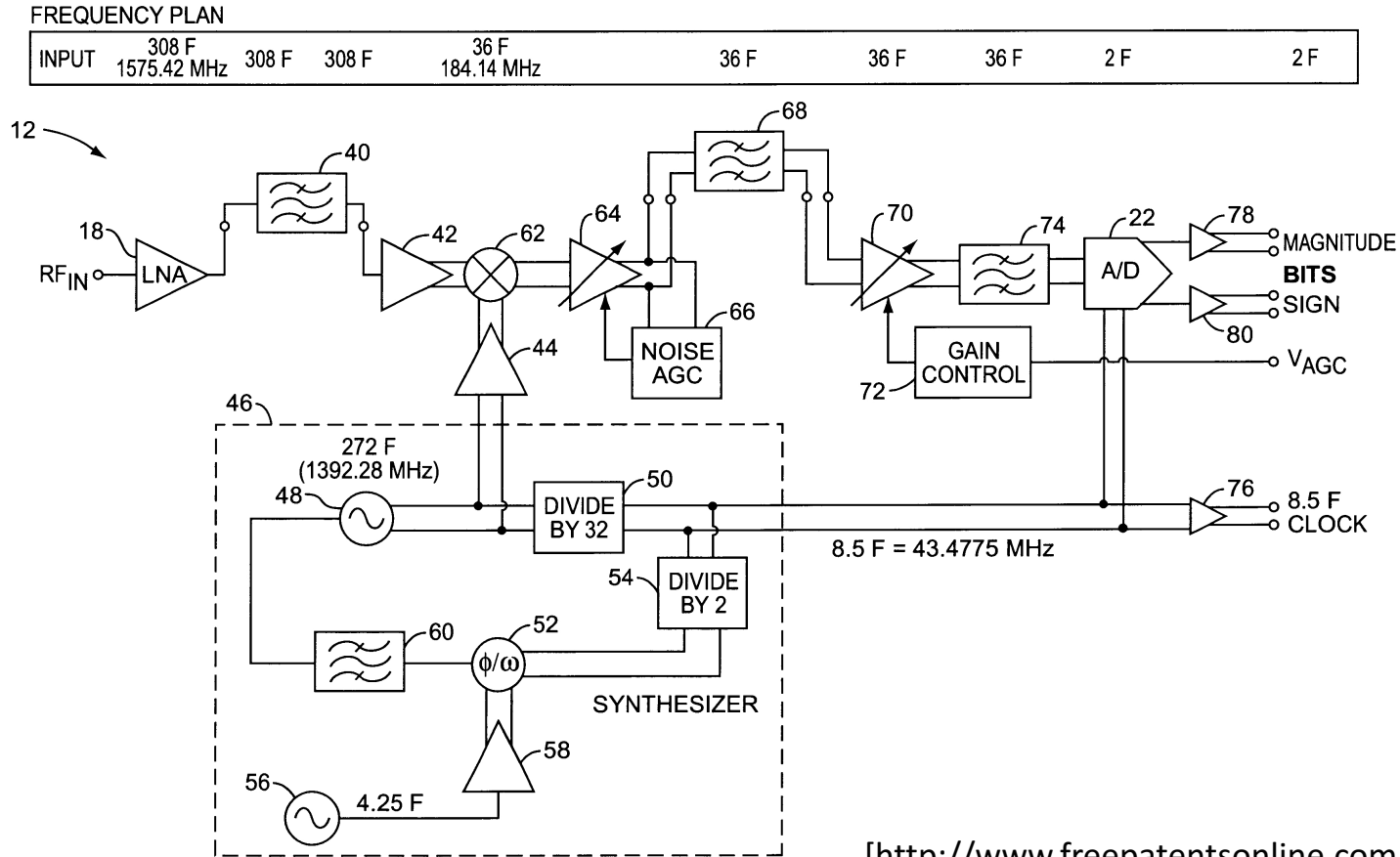


Figure (a): Block Diagram of a Typical AM Communication Receiver

[[www.daenotes.com](http://www.daenotes.com)]



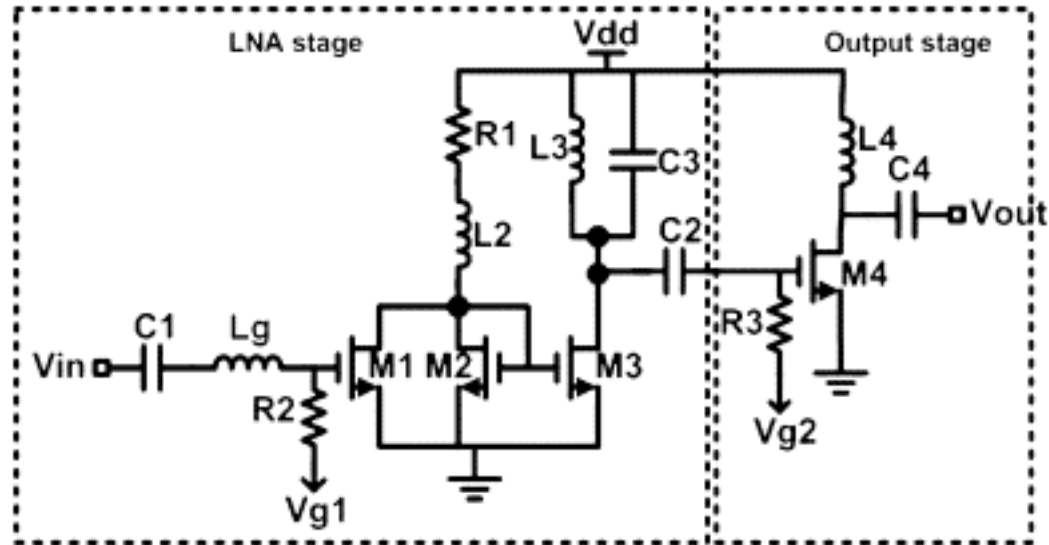
# Example: GPS Receiver



[<http://www.freepatentsonline.com/6670914.html>]



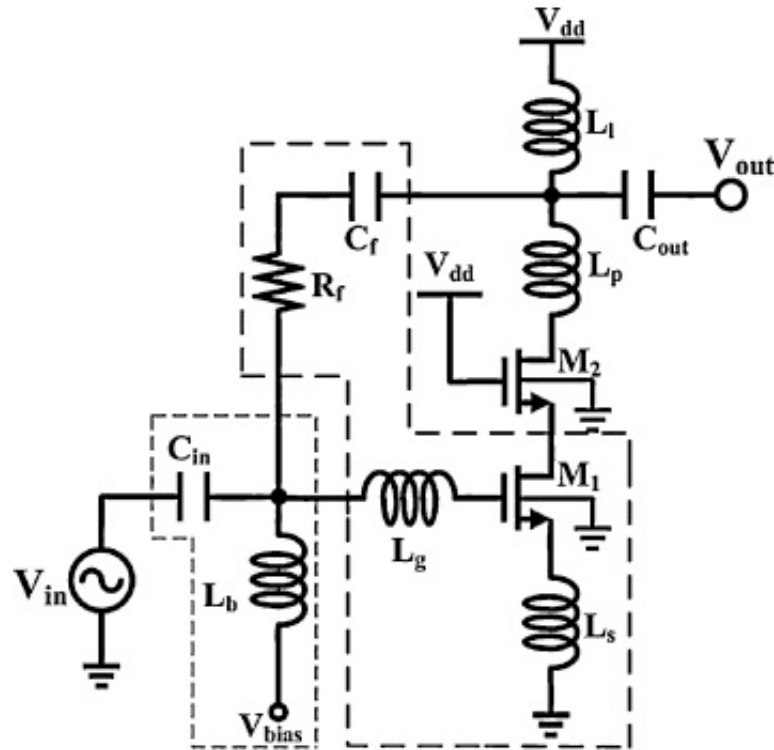
# Example: 1V 12.8 GHz Low Noise Amplifier



[[www.sciencedirect.com](http://www.sciencedirect.com)]

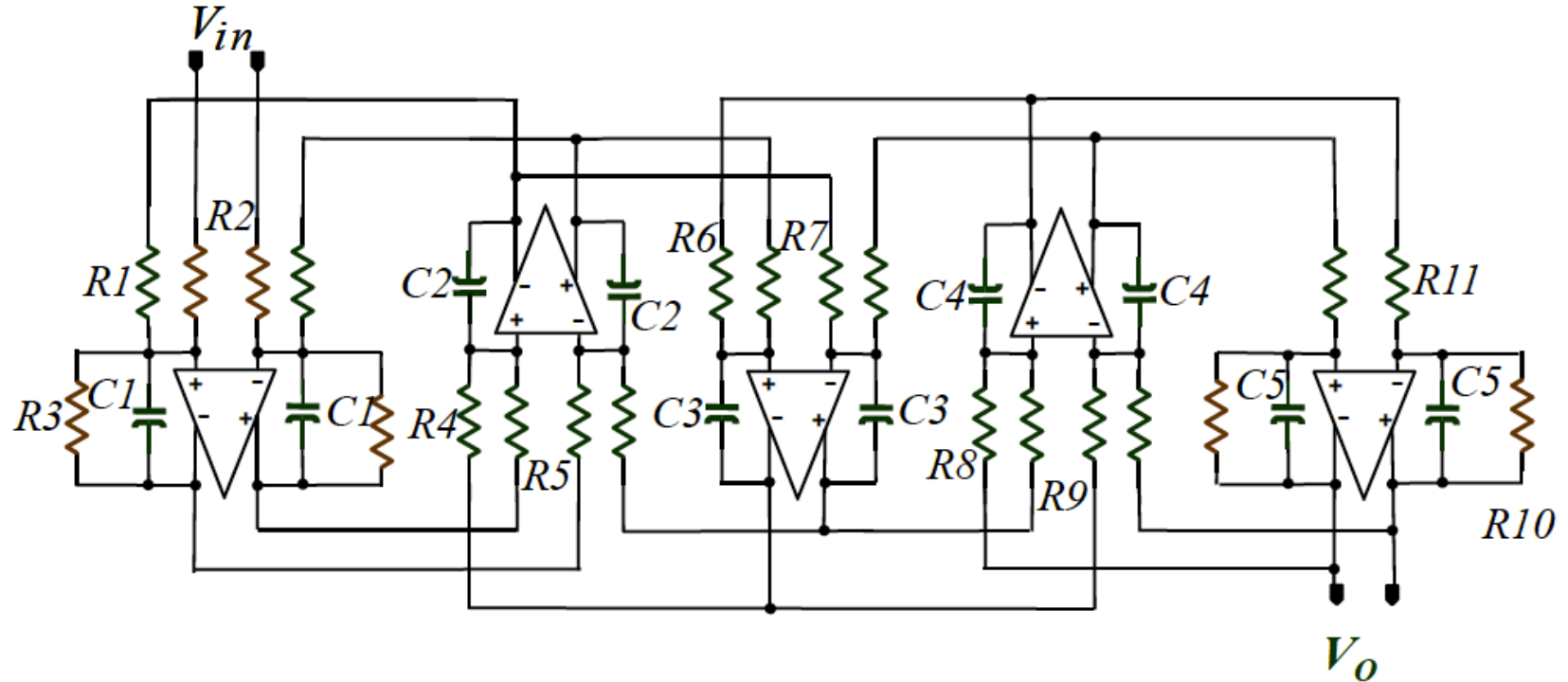


# Example: 1.8V 3.1 – 10.6 GHz LNA

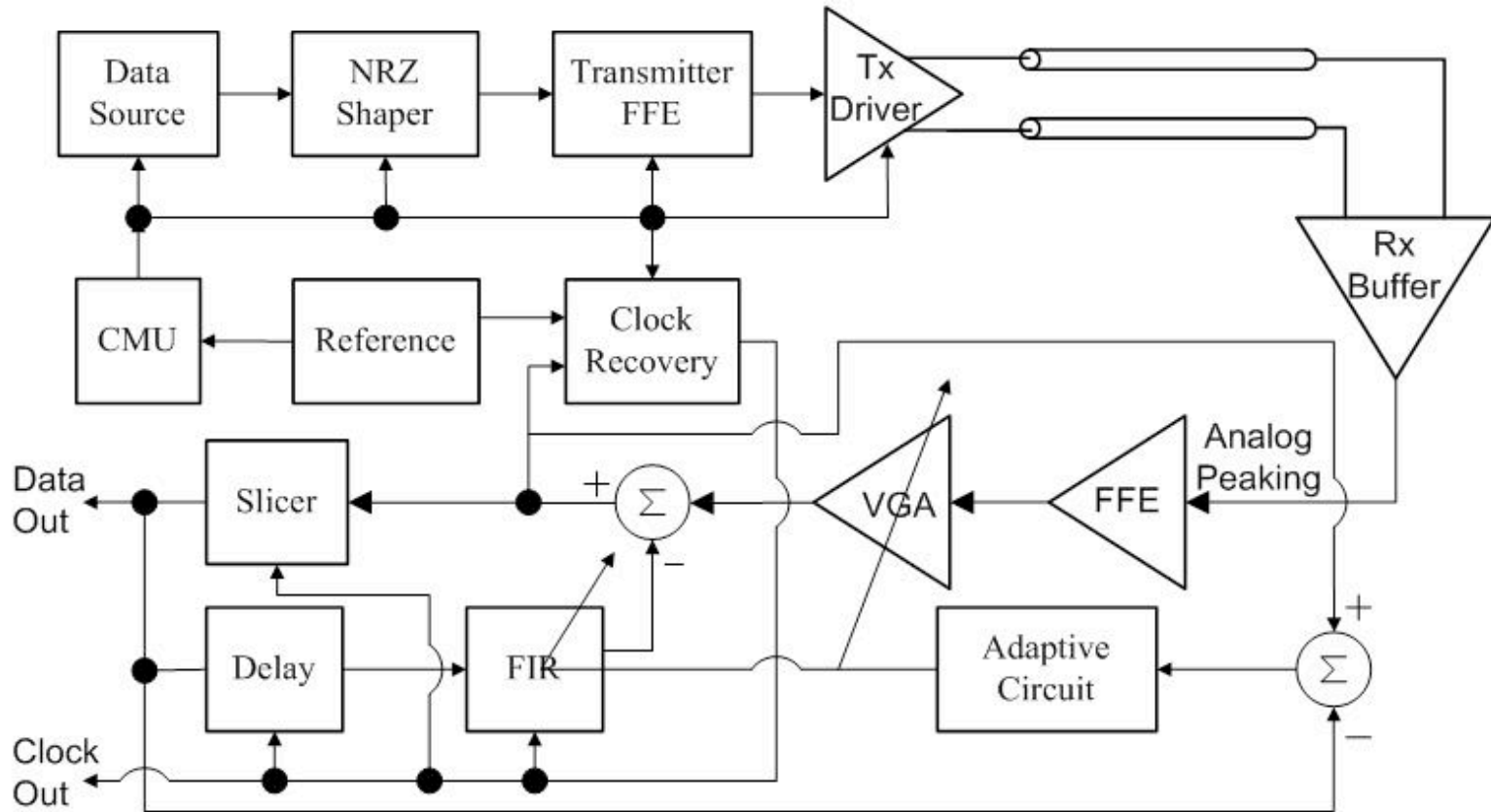


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# Example: Integrator-Based Active Filter



# Example: High-Speed Wired Communications



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# End of EEE 51!

- Final Exam:
  - Thursday May 24, 2018
  - 1 – 4 pm
  - Bring: pen, calculator

