EEE 51 Assignment 5 Answer Key

2nd Semester SY 2018-2019
Due: 5pm Tuesday, March 12, 2019 (Rm. 220)

Instructions: Write legibly. Show all solutions and state all assumptions. Write your full name, student number, and section at the upper-right corner of each page. Start each problem on a new sheet of paper. Box or encircle your final answer.

Answer sheets should be color coded according to your lecture section. The color scheme is as follows:

THQ – yellow
THU – white
WFX – pink

1. **Simple BJT Differential Pair**

   Shown in Figure 1 is a BJT differential pair with resistor load. Assume that the BJTs operate in the forward active region, $V_A \to \infty$. Answer the following.

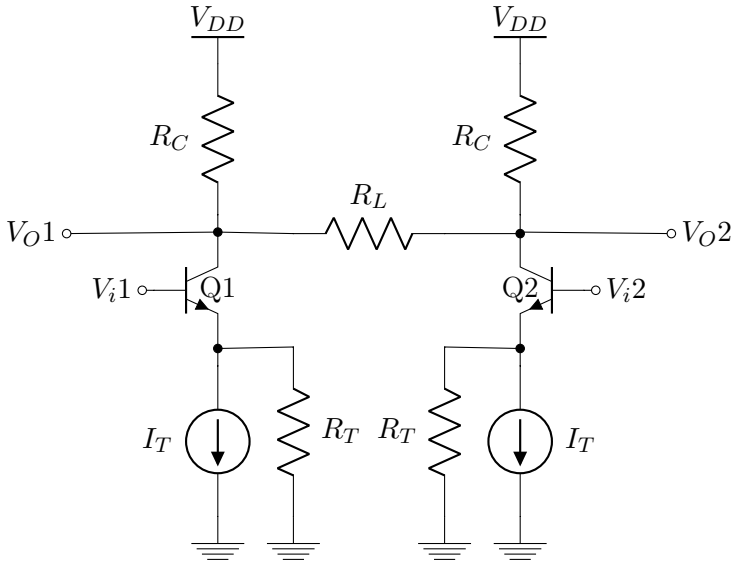


Figure 1: BJT differential pair

   (a) Explain the difference between differential mode gain, A_{dm} and common mode gain, A_{cm} and their relation to Common Mode Rejection Ratio (CMRR). Do we want a high or low CMRR? Explain. (2pts)

   - The differential gain is the gain at the output for a given differential input, $\frac{V_{od}}{V_{id}}$. On the other hand, common mode gain is the gain at the output for a given input common to both Q1 and Q2, $\frac{V_{oc}}{V_{ic}}$. For a good differential amplifier, a high differential gain and a low common mode gain is desired to suppress signals common to both input nodes while amplifying the desired signal. Thus, a high CMRR is wanted for a differential amplifier.

   (b) Why is it important that the components in the branches be matched? How does it affect the analysis of the differential pair? (2pts)

   - It is important to match the branches to have symmetry. Additionally, the symmetry allows us to simplify the solution by allowing us to use half circuit analysis for both the differential mode and common mode.

(c) Draw the differential mode half circuit and find the differential mode gain, A_{dm} in terms of small signal parameters and circuit components. (2pts)

- The differential mode half circuit is shown in Figure 2. The half circuit is an emitter degenerated BJT. For ease of computations, we may assume $\beta >> 1$. The differential mode gain is

$$\boxed{A_{dm} = -\frac{g_m(R_C || \frac{R_L}{2})}{1 + g_m R_T}}$$

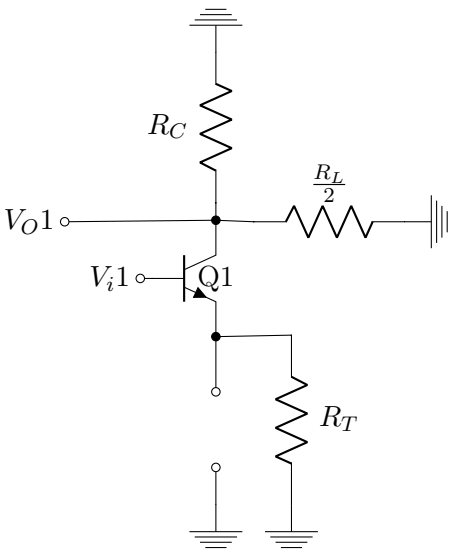


Figure 2: Differential mode half circuit

(d) Draw the common mode half circuit and find the common mode gain, A_{cm} in terms of small signal parameters and circuit components. (2pts)

- The common mode half circuit is shown in Figure 3. The half circuit is an emitter degenerated BJT with $\frac{R_L}{2}$ open. For ease of computations, we may assume $\beta >> 1$. The common mode gain is

$$\boxed{A_{cm} = -\frac{g_m R_C}{1 + g_m R_T}}$$

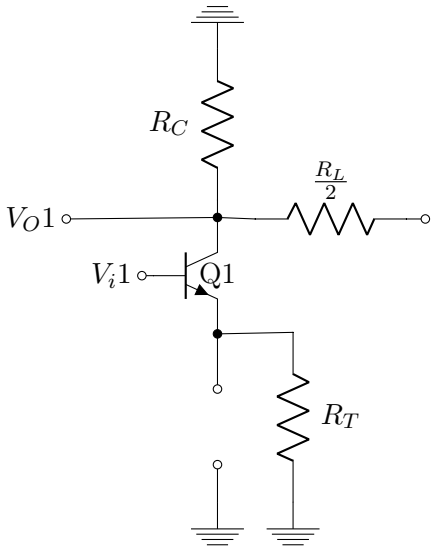


Figure 3: Common mode half circuit

(e) How does R_T affect the amplifier's performance? (2pts)

- The resistance, R_T acts as a emitter degenerate resistor. Thus, it lowers the gain of the differential mode (unwanted) for linearity. However, it also lowers the gain of the common mode (desired). Additionally, in computing the CMRR, the denominator terms cancel out.

2. **Differential Pair with Resistive Bias and Resistive Load.**

The differential pair shown in Figure 4 is supplied by $V_{DD} = -V_{SS} = 1\,\text{V}$. The process technology used have the following: $V_{TH,P} = 400\,\text{mV}$, $V_{TH,N} = 550\,\text{mV}$, $\lambda_P = 0.001\,\text{V}^{-1}$, and $\lambda_N = 0.01\,\text{V}^{-1}$. Each transistor have been characterized and found out that: $k_1 = k_2 = 4.082\,\mu\text{A/V}^2$, $k_3 = k_4 = 12.5\,\mu\text{A/V}^2$, $k_5 = 400\,\mu\text{A/V}^2$, $k_6 = 4\,\mu\text{A/V}^2$, and $k_7 = 250\,\text{nA/V}^2$, where k is defined as $k = \frac{\mu C_{ox}}{2}\frac{W}{L}$. The pair is used with input DC voltage of 0 V on both sides ($V_I^+ = V_I^- = 0\,\text{V}$).

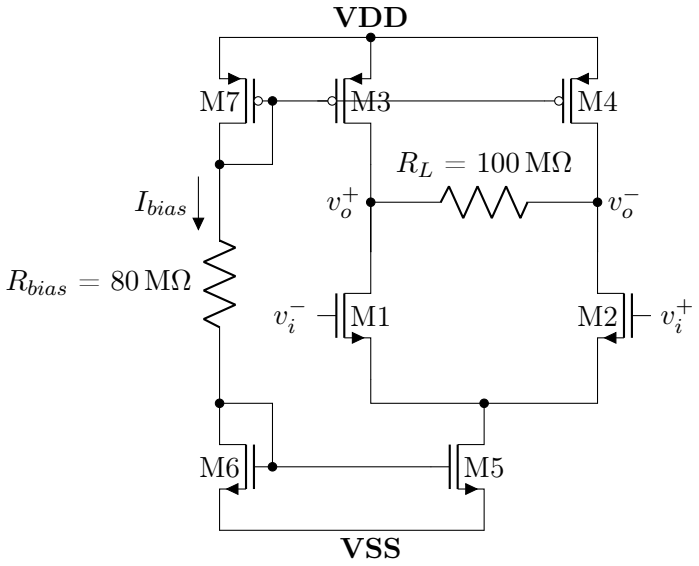


Figure 4: Differential Pair with Resistive Bias

Answer the following questions. Ignore channel length modulation. Unless otherwise stated, always round off your answers to the nearest whole number of the appropriate magnitude.

(a) Find the biasing values for the transistors to complete the table below. Round off your answers to the nearest millivolt. (3 pts)

Transistor	V_{SG} or V_{GS} (mV)
M1 & M2	900 mV
M3, M4, & M7	600 mV
M5 & M6	600 mV

- Assume that all transistors are in saturation. We perform KVL in the bias circuit to find V_{GS6} and V_{SG7}:

$$V_{DD} - V_{SD7} - I_{bias}R_{bias} - V_{DS6} - V_{SS} = 0$$

Also note that M6 and M7 are diode-connected transistors:

$$V_{DS6} = V_{GS6}$$
$$V_{SD7} = V_{SG7}$$

Since there is only one current going through M6 and M7, we can find the relationship between V_{GS6} and V_{SG7}:

$$\begin{aligned} I_{bias} &= I_{SD7} = I_{DS6} \\ &= k_6 \left(V_{GS6} - V_{TH,N}\right)^2 \\ &= k_7 \left(V_{SG7} - V_{TH,P}\right)^2 \\ k_6 \left(V_{GS6} - V_{TH,N}\right)^2 &= k_7 \left(V_{SG7} - V_{TH,P}\right)^2 \\ V_{GS6} &= \left[\sqrt{\frac{k_7}{k6}} \left(V_{SG7} - V_{TH,P}\right)\right] + V_{TH,N} \end{aligned}$$

Thus,

$$\begin{aligned} V_{DD} - V_{SD7} - I_{bias} R_{bias} - V_{DS6} - V_{SS} &= 0 \\ V_{DD} - V_{SD7} - \left[k_7 \left(V_{SG7} - V_{TH,P}\right)^2\right] R_{bias} + \left[\sqrt{\frac{k_7}{k6}} \left(V_{SG7} - V_{TH,P}\right)\right] + V_{TH,N} - V_{SS} &= 0 \\ 1 - V_{SD7} - \left[250n \left(V_{SG7} - 0.4\right)^2\right] (80M) + \left[\sqrt{\frac{250n}{4\mu}} \left(V_{SG7} - 0.4\right)\right] + 0.55 - -1 &= 0 \\ 20 V_{SG}^2 - 14.75 V_{SG7} + 1.65 &= 0 \end{aligned}$$

Solving the quadratic equation will yield:

$$\begin{aligned} V_{SG7,1} &= 0.1375 \\ V_{SG7,2} &= 0.6 \end{aligned}$$

Since M7 is in saturation, then:

$$\boxed{V_{SG7} = 600\,\text{mV}}$$
$$\boxed{V_{GS6} = 600\,\text{mV}}$$

From the schematic, it is obvious that:

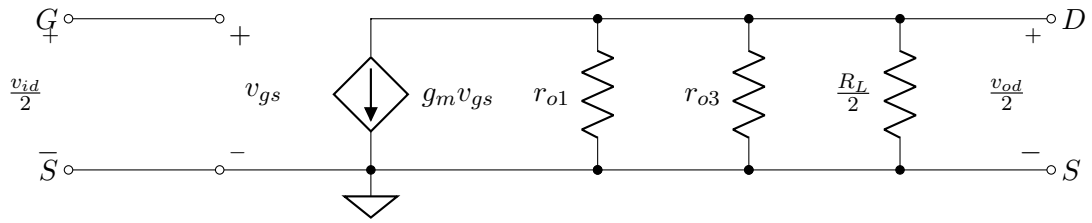
$$\begin{aligned} V_{SG7} = V_{SG3} &= V_{SG4} \\ V_{GS6} &= V_{GS5} \end{aligned}$$

- To find V_{GS1} and V_{GS2}, we need to know the drain current first:

$$\begin{aligned} I_{DS1} &= I_{SD3} \\ &= k_3 \left(V_{SG3} - V_{TH,P}\right)^2 \\ &= 12.5\mu \left(0.6 - 0.4\right)^2 \\ &= 500\,\text{nA} \\ 500\,\text{nA} &= k_1 \left(V_{GS1} - V_{TH,N}\right)^2 \\ &= 4.082\mu \left(V_{GS1} - 0.55\right)^2 \\ V_{GS1} &\approx 899.984\,25\,\text{mV} \\ &\approx \boxed{900\,\text{mV}} \end{aligned}$$

Assuming that M1 and M2 are matched, as well as M3 and M4, then $V_{GS1} = V_{GS2}$.

(b) Draw the small-signal differential mode half circuit with corresponding labels and values, and identify the differential gain. (2 pts)



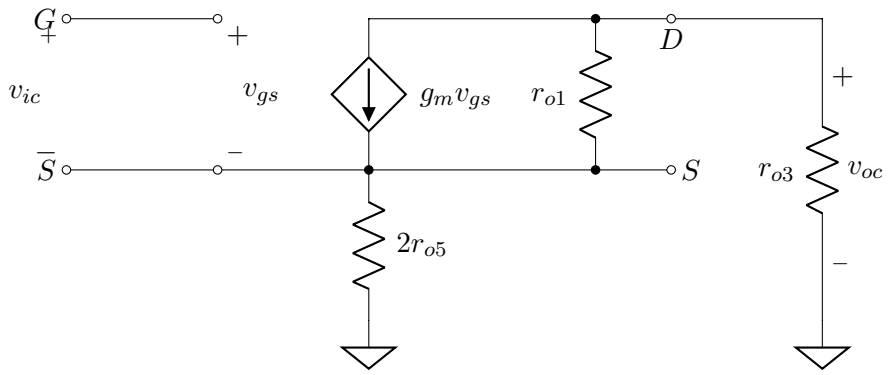
- Since $I_{DS1} = 500\,\text{nA}$:

$$\begin{aligned}
g_{m1} &= \sqrt{4k_1 I_{DS1}} \\
&= \sqrt{4\,(4.082\mu)\,(500n)} \\
&\approx 2.857\,27\,\mu\text{S} \\
g_{m1} &\approx 3\,\mu\text{S} \\
r_{o1} &= \frac{1}{\lambda_N I_{DS1}} \\
&= \frac{1}{(0.01)\,(500n)} \\
r_{o1} &= 200\,\text{M}\Omega \\
r_{o3} &= \frac{1}{\lambda_P I_{DS1}} \\
&= \frac{1}{(0.001)\,(500n)} \\
r_{o3} &= 2\,\text{G}\Omega
\end{aligned}$$

- The differential mode half circuit is just a common source configuration, thus:

$$\begin{aligned}
A_{dm} &= -G_M R_O \\
&= -g_{m1}\left(r_{o1}||r_{o3}||\frac{R_L}{2}\right) \\
&= -\,(2.85727\mu)\left(200M||2G||\frac{100M}{2}\right) \\
&= -\,(2.85727\mu)\,(39.215686M) \\
&\approx -112.04986 \\
&\approx \boxed{-117 \text{ to } -112}
\end{aligned}$$

(c) Draw the small-signal common mode half circuit with corresponding labels and values, and identify the common mode gain. (2 pts)



- Each half of the pair have 500 nA of drain current, so $I_{DS5} = 1\,\mu\text{A}$:

$$\begin{aligned}
r_{o5} &= \frac{1}{\lambda_N I_{DS5}} \\
&= \frac{1}{(0.01)\,(1\mu)} \\
r_{o5} &= 100\,\text{M}\Omega \\
r_{o1} &= 200\,\text{M}\Omega \\
r_{o3} &= 2\,\text{G}\Omega \\
g_{m1} &\approx 3\,\mu\text{S}
\end{aligned}$$

- The common mode half circuit is just a common source with source degeneration resistor:

$$\begin{aligned}
G_M &= \frac{g_{m1}}{1 + 2g_{m1}r_{o5}} \\
&= \frac{2.85727\mu}{1 + 2\,(2.85727\mu)\,(100M)} \\
&\approx 4.991\,27\,\text{nS} \\
G_M &\approx 5\,\text{nS} \\
R_O &= (1 + 2g_{m1}r_{o5})\,r_{o1}||r_{o3} \\
&= (1 + 2\,(2.85727\mu)\,(100M))\,(200M)\,||2G \\
&\approx 1.965\,66\,\text{G}\Omega \\
R_O &\approx 2\,\text{G}\Omega \\
A_{cm} &= -G_M R_O \\
&\approx -\,(4.99127n)\,(1.96566G) \\
&\approx -9.81114 \\
&\approx \boxed{-10}
\end{aligned}$$

(d) What is the value of the CMRR? Round down the answer to the greatest integer less than or equal to the actual answer. If the bias circuit (M6, M7, and R_{bias}) is fixed, as well as the dimensions of M1 to M4, what adjustment should be made to either R_L or M5 to increase the CMRR? (2 pts)

$$\begin{aligned}\text{CMRR} &= \frac{|A_{dm}|}{|A_{cm}|} \\ &\approx \frac{|112.04986|}{|9.81114|} \\ &\approx 11.42067 \\ &\approx \boxed{11}\end{aligned}$$

- The answer to the second question will be obvious if we write first the expression for the CMRR:

$$\begin{aligned}\text{CMRR} &= \frac{|A_{dm}|}{|A_{cm}|} \\ &= \frac{g_{m1}\left(r_{o1}||r_{o3}||\frac{R_L}{2}\right)}{\left(\frac{g_{m1}}{1+2g_{m1}r_{o5}}\right)\left[\left(1+2g_{m1}r_{o5}\right)r_{o1}||r_{o3}\right]} \\ &= \frac{\left[\left(1+2g_{m1}r_{o5}\right)r_{o1}+r_{o3}\right]R_L}{r_{o1}R_L+r_{o3}R_L+2r_{o1}r_{o3}}\end{aligned}$$

Increasing R_L will increase A_{dm}, increasing the CMRR. As for M5, we can change its dimensions such that the DC biasing will be unchanged but its output resistance r_{o5} will increase. Assuming $r_{o5} \to \infty$, the effective G_M will drop to 0, thus $A_{cm} = 0$, and CMRR $\to \infty$. Therefore, to increase CMRR, we need to $\boxed{\textbf{INCREASE } R_L \textbf{ and/or } r_{o5}}$.

(e) What is the maximum differential input voltage swing? (1 pt)

- To determine the maximum input swing, we need to find the maximum output swing first. The maximum output swing is limited by the saturation of the transistors.
- The upper part of the swing is limited by the saturation condition of M3 and M4 assuming that they are matched:

$$\begin{aligned}V_{SD3,sat} &= V_{SG3} - V_{TH,P} \\ &= 0.6 - 0.4 \\ &= 0.2\,\text{V} \\ v_{o,max} &= V_{DD} - V_{SD3,sat} \\ &= 1 - 0.2 \\ v_{o,max} &= 0.8\,\text{V}\end{aligned}$$

- The lower part of the swing is limited by the saturation conditions of M1 and M5, with the assumption that M1 and M2 are matched.

$$
\begin{aligned}
V_{DS5,sat} &= V_{GS5} - V_{TH,N} \\
&= 0.6 - 0.55 \\
&= 0.05\,\text{V} \\
V_{DS1,sat} &= V_{GS1} - V_{TH,N} \\
&= V_{G1} - V_{S1} - V_{TH,N} \\
&= V_{G1} - V_{D5} - V_{TH,N} \\
&= V_{G1} - (V_{DS5,sat} + V_{SS}) - V_{TH,N} \\
&= 0 - (0.05 + -1) - 0.55 \\
&= 0.4\,\text{V} \\
v_{o,min} &= V_{DS5,sat} + V_{DS1,sat} + V_{SS} \\
&= 0.05 + 0.4 + -1 \\
v_{o,min} &= -0.55\,\text{V}
\end{aligned}
$$

- The maximum output swing is:

$$
\begin{aligned}
v_{o,max} - v_{o,min} &= 0.8 - -0.55 \\
v_{o,max,swing} &= 1.35\,\text{V}
\end{aligned}
$$

We divide this by the differential gain to get the maximum differential input swing:

$$
\begin{aligned}
v_{i,max,swing} &= \frac{v_{o,max,swing}}{|A_{dm}|} \\
&\approx \frac{1.35}{112.04986} \\
&\approx 0.012\,05\,\text{V} \\
&\approx \boxed{12\,\text{mV}}
\end{aligned}
$$

3. **BJT Differential Amplifier <3.** You finally found the person of your dreams in your EEE 52 class, so want to impress him/her with your skills through your design project. Luckily, your instructor simplified your design project: all you have to do is amplify a 2 mV peak-to-peak 1 KHz sinusoid into a 400 mV peak-to-peak 1 KHz sinusoid using a differential amplifier with resistive load as shown in fig. 5. Let's define $v_{out} = v_o^+ - v_o^-$, and $V_{DD} = 9V$. You may assume $V_A \to \infty$, $\beta = 200$, $V_{BE,on} = 0.7V$, $V_T = 26mV$, and $V_{CE,sat} = 0.2V$, and that all transistors are identical.

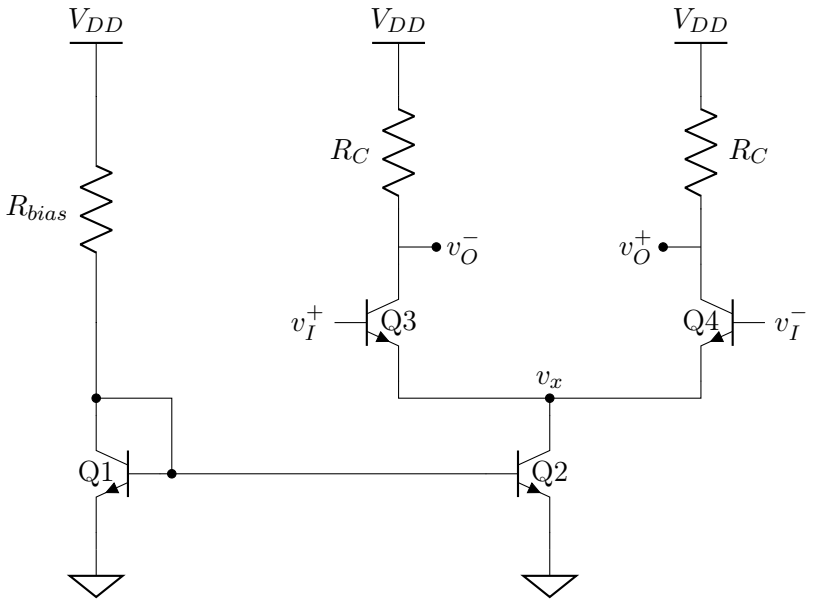


Figure 5: Differential Pair with Resistive Load

You want to ensure that the amplifier works within the target range of input and output voltages. So you check the DC biasing conditions first:

SOLUTION NOTES:

i. Let V_{CEx} be the V_{CE} across Qx, and V_{BEx} be the V_{BE} across Qx.

ii. DC biasing parameters such as, but not limited to $[V_I^+$ and $V_I^-]$, $[V_O^+$ and $V_O^-]$ should have the same value. You should be able to solve them using just one equation per pair of variables, but they will be solved separately here to show each possible solution.

(a) What is the minimum DC bias for the input voltages V_I^+ and V_I^- such that all transistors are biased at Forward active? (0.5 pt.)

$$V_{I,min}^+ = V_{CE2,min} + V_{BE3,min}$$
$$V_{I,min}^- = V_{CE2,min} + V_{BE4,min}$$

where:

$$V_{CE2,min} = V_{CE,sat} = 0.2V$$
$$V_{BE4,min} = V_{BE,on} = 0.7V$$

Thus,

$$V_{I,min}^+ = 0.2V + 0.7V = 0.9V$$
$$V_{I,min}^- = 0.2V + 0.7V = 0.9V$$

$$\boxed{V_{I,min}^+ = V_{I,min}^- = 0.9V} \text{ (0.5 pt)}$$

(b) Is there a maximum DC bias for the input voltages V_I^+ and V_I^- to ensure correct operation of the amplifier? If yes, what is it? (0.5 pt.)

The maximum values for V_O^+ and V_O^- would be limited by the upper voltage swing of the output. A 400-mV peak-to-peak sinusoid would have an amplitude of 200 mV. Thus, V_O^+ and V_O^- should each be able to swing 200 mV – 100 mV above, and 100 mV below the bias. This means that:

$$V_{O,max}^+ = V_{DD} - 0.1V = 9V - 0.1V = 8.9V$$
$$V_{O,max}^- = V_{DD} - 0.1V = 9V - 0.1V = 8.9V$$

Increasing the DC bias for V_I^+ and V_I^- would lead to:
(1) higher current, which often leads to lower biasing at V_O^+ and V_O^-, and
(2) higher voltage biasing at V_X, leading to a smaller available swing at V_O^+ and V_O^-.
We'd typically have to compare each of these two cases, but since we don't have a value for R_C yet, we'll just check the biasing limited by V_X.

$$V_{O,max}^+ = V_{X,max} + V_{CE4,min}$$
$$V_{O,max}^- = V_{X,max} + V_{CE3,min}$$

where:

$$V_{X,max} = V_{I,max}^+ - V_{BE3,on}$$
$$= V_{I,max}^- - V_{BE4,on}$$

$$V_{O,max}^+ = V_{I,max}^- - V_{BE4,on} + V_{CE4,sat}$$
$$V_{O,max}^- = V_{I,max}^+ - V_{BE3,on} + V_{CE3,sat}$$

Thus,

$$V_{I,max}^- = V_{O,max}^+ + V_{BE4,on} - V_{CE4,sat} = 8.9V + 0.7V - 0.2V = 9.4V$$
$$V_{I,max}^+ = V_{O,max}^+ + V_{BE3,on} - V_{CE3,sat} = 8.9V + 0.7V - 0.2V = 9.4V$$

$$\boxed{V_{I,max}^+ = V_{I,max}^- = 9.4V} \text{ (0.5 pt)}$$

(c) Your instructor required everyone to design the amplifier to have a total of 2 mA current draw from V_{DD}, both the differential amplifier and the current reference. How much current should flow through Q3 and Q4 each? (0.5 pt.)

Since $\beta = 200$, any assumption involving $I_E = I_C$ with bear just $1 - \frac{\beta}{\beta+1} \approx 0.5\%$ approximation error, so for the rest of calculations, we'll assume $I_E \approx I_C$.

The total current is:

$$I_{VDD} = 2mA = I_{C1} + I_{C3} + I_{C4}$$
$$\text{where: } I_{C3} = I_{C4}$$
$$\text{and } I_{C1} \approx I_{C2} = I_{C3} + I_{C4} = 2I_{C3} = 2I_{C4}$$
$$I_{VDD} = 2mA = 4I_{C3} = 4I_{C4}$$

$$\boxed{I_{C3} = I_{C4} = 0.5mA} \text{ (0.5 pt)}$$

Small-signal analysis:

Note: We must first check if for the given input, the small-signal model will always hold true. $\frac{v_{be,max}}{V_T} = \frac{1mV amplitude}{26mV} = 0.0385 << 1$. Therefore, we can use the small-signal model we know. :)

(d) How much differential-mode gain A_{DM}, will you need? (0.5 pt)
Note the polarity of the output voltage. When v_i^+ increases, v_o^+ also increases, and vice versa. This means that the way the output voltages are tapped (see Figure 5, and the output voltage is defined ($v_{out} = v_o^+ - v_o^-$) introduce a non-inverting gain rather than the usual inverting gain of common emitter amplifiers. You can invert the sign of v_{out} by simply switching v_o^+ and v_o^-. This is one of the useful features of differential amplifiers, easy voltage inversion.

$$\begin{aligned} A_{DM} &= \frac{v_{out,dm}}{v_{in,dm}} \\ &= \frac{400mV_{p-p}}{2mV_{p-p}} \\ &= 200V/V \end{aligned}$$

$$\boxed{A_{DM} = 200V/V} \text{ (0.5 pt)}$$

(e) Calculate the required R_C to meet the necessary small-signal differential-mode gain, A_{DM}. (1 pt.)

$$\begin{aligned} A_{DM} &= -g_m R_C \\ \text{where } g_m &= \frac{I_C}{V_T} = \frac{0.5mA}{26mV} = 19.23mS \\ \text{Thus, } R_C &= \frac{A_{DM}}{g_m} \\ &= \frac{200}{19.23mS} = 10.4K\Omega \end{aligned}$$

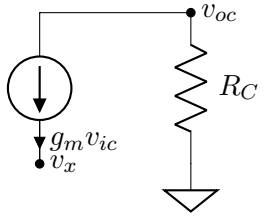
$$\boxed{R_C = 10.4K\Omega} \text{ (1 pt)}$$

(f) Calculate the DC biasing V_O^- and V_O^+ for the calculated R_C. (1 pt)

$$\begin{aligned} V_O^+ &= V_{DD} - I_{C4}R_C = 9V - (0.5mA)(10.4K\Omega) = 3.8V \\ V_O^- &= V_{DD} - I_{C3}R_C = 9V - (0.5mA)(10.4K\Omega) = 3.8V \end{aligned}$$

$$\boxed{V_O^+ = V_O^- = 3.8V} \text{ (1 pt)}$$

(g) Calculate the common-mode gain, A_{CM}. (1 pt)
The common-mode half-circuit will look like:



Note that v_x is virtually unconnected due to the infinite output impedance of the tail transistor Q2. Thus, by applying KCL at node V_{oc}, we get:

$$0 + \frac{v_{oc}}{R_C} = 0 - - > v_{oc} = 0$$

$$\boxed{A_{CM} = \frac{v_{oc}}{v_{ic}} = 0} \text{ (1 pt)}$$

Do or Die! Assume you biased $V_I^+ = V_I^- = 2V$. It's the demo day, and everything was well until...

(h) All the AC sources in the lab suddenly malfunctioned! Each sinusoidal source voltage is increased by 2 Volts DC. Will your amplifier still work? Should you (A) suddenly turn off all the sources to save yourself from shame; or (B) leave everything on, and impress both the person of your dreams, and your instructor? Prove by presenting/calculating whichever parameter/s must be considered. (Hint: You'll need to look at at least 1 DC biasing parameter, and 1 differential amplifier parameter) (2 pts)

First, we check the DC biasing conditions. We need to verify if I_{C3} or I_{C4} changed. If each sinusoidal source is increased by 2 Volts DC, $V_I^+ = V_I^- = 2V + 2V = 4V$. For this input biasing, the BJTs are biased in forward active mode. Since $V_A \to \infty$, any change to v_x doesn't change I_{C2} which means that neither I_{C3} nor I_{C4} changes. Thus, the output voltage biasing does not change:

$$\boxed{V_O^+ = V_O^- = 3.8V}$$

We then check if any of the small-signal parameters have been affected by the input change. Since neither I_{C3} nor I_{C4} changed, the small-signal parameters stay the same:

$$\boxed{A_{DM} = 200V/V} \quad \boxed{A_{CM} = 0V/V}$$

Thus the output differential voltage should remain the same, provided that none of the transistors saturate for the expected output range (3.6 V to 4 V). We check through the input biasing:

$$\begin{aligned} V_{O,min,allowed}^+ &= V_I^- - V_{BE4,on} + V_{CE4,sat} \\ &= 4V - 0.7V + 0.2V \\ &= 3.5V \\ V_{O,min,allowed}^- &= V_I^+ - V_{BE3,on} + V_{CE3,sat} \\ &= 4V - 0.7V + 0.2V \\ &= 3.5V \end{aligned}$$

$$\boxed{V_{O,min,allowed}^+ = V_{O,min,allowed}^- = 3.5V}$$

If you realized that the DC biasing can still accommodate the 400 mVp-p output sinusoid, and that the small-signal parameters didn't change, you'd know $\boxed{\text{not to turn off all voltage sources.}}$ You'd impress everyone with your fast thinking!

(i) All the AC sources suddenly got fixed and now give the correct DC biasing. However, your instructor was disappointed / impressed. So he/she disconnected and changed the AC sources:

$$\begin{aligned} v_i^- &= -1sin(2\pi ft)mV \\ v_i^+ &= 0.01 + 1sin(2\pi ft)mV \\ f &= 1KHz \end{aligned}$$

He/she then asks you in front of everyone what would happen to the output when the AC source is connected. It's your chance to shine! Write the mathematical expression for the small-signal differential output voltage, v_{od}. (2 pt)

$$\begin{aligned} v_{id} &= v_i^+ - v_i^- \\ &= (0.01 + 1sin(2\pi ft)mV) - (-1sin(2\pi ft)mV) \\ &= 0.01 + 2sin(2\pi ft)mV \\ v_{od} &= A_{DM} v_{id} \\ &= (200)(0.01 + 2sin(2\pi ft)mV) \\ &= 2 + 400sin(2\pi ft)mV \end{aligned}$$

$\boxed{v_{od} = 2 + 400sin(2\pi ft)mV}$ (2 pts)

(j) Calculate the small-signal common-mode output voltage, v_{oc} for the problem in (i). (1 pt)

$$\begin{aligned} v_{ic} &= \frac{v_i^+ + v_i^-}{2} \\ &= \frac{(0.01 + 1sin(2\pi ft)mV) + (-1sin(2\pi ft)mV)}{2} \\ &= 0.005mV \\ v_{oc} &= A_{CM} v_{ic} \\ &= (0)(0.005mV) \\ &= 0 \end{aligned}$$

Therefore, any common-mode voltage you apply on the inputs of this amplifier gets rejected. You just need to figure out if the input voltage is still within the limits we calculated in parts (a) and (b). Hopefully, you figured this out before all the mayhem happened and managed to impress both your instructor and the person of your dreams. :)

$$\boxed{v_{oc} = 0} \text{ (1 pt)}$$

TOTAL: 30 points.