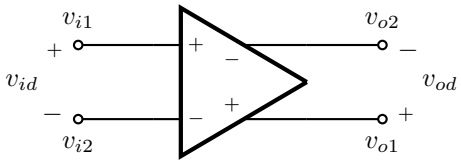


Figure 5.1: A fully-differential voltage amplifier.

5 Differential Circuits

The circuits we have covered so far have input and output small signal voltages that are referenced to (or referred to) the small signal ground. These circuits are called *single-ended circuits*. In certain cases, we want to amplify the difference between two signals. Circuits that operate on the difference between two signals are called *differential circuits*. In this section, we will look at the reasons why one would choose differential circuits over single-ended circuits, and the costs associated with using these differential circuits.

5.1 Differential Signals and Gain Definitions

Consider two voltages referred to ground, v_1 and v_2. If these two voltages are independent, then any change in v_1 will not affect v_2. We can say that v_1 and v_2 are orthogonal to each other. Thus, in order to completely describe this system of two independent voltages, we need specify both v_1 and v_2.

Just like changing coordinate axes, we can use a different set of orthogonal quantities to describe these two voltages. One such set of quantities is the the differential voltage, v_d, and the common-mode voltage, v_c, defined as

$$v_d = v_1 - v_2 \tag{5.1}$$

$$v_c = \frac{v_1 + v_2}{2} \tag{5.2}$$

Note that v_d and v_c are also orthogonal with respect to each other, since we can change the difference between v_1 and v_2[a], while maintaining their average, and vice-versa. From Eqs. 5.1 and 5.2, we can also get the inverse relationships

$$v_1 = v_c + \frac{v_d}{2} \tag{5.3}$$

$$v_2 = v_c - \frac{v_d}{2} \tag{5.4}$$

Consider a fully-differential voltage amplifier, given in Fig. 5.1. A fully-differential amplifier amplifies the differential input voltage, and produces a differential output voltage. However, since we have four quantities, we can define four distinct voltage gains.

The voltage gain between the differential input voltage to the differential output voltage is called the differential-mode gain, and is defined as

$$A_{dm} = \left.\frac{v_{od}}{v_{id}}\right|_{v_{ic}=0} = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} \tag{5.5}$$

We can also define the common-mode gain as

$$A_{cm} = \left.\frac{v_{oc}}{v_{ic}}\right|_{v_{id}=0} = \frac{\frac{1}{2}\left(v_{o1} + v_{o2}\right)}{\frac{1}{2}\left(v_{i1} + v_{i2}\right)} \tag{5.6}$$

It is also possible for an amplifier to convert the input differential voltage into a common-mode output voltage. Thus, the differential-mode to common-mode gain is

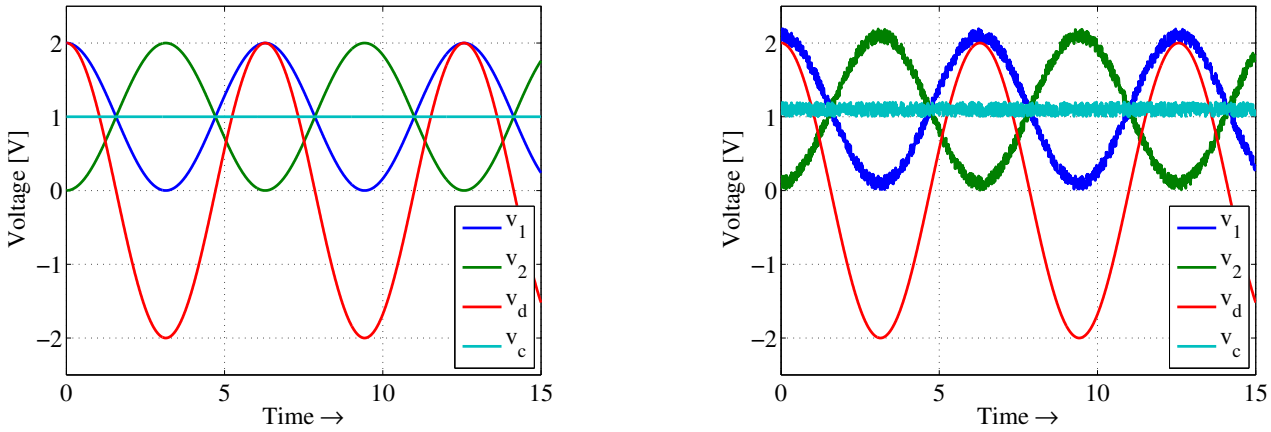
$$A_{dm-cm} = \left.\frac{v_{oc}}{v_{id}}\right|_{v_{ic}=0} \tag{5.7}$$

and the gain from the common-mode input voltage to the differential-mode output voltage is defined as

$$A_{cm-dm} = \left.\frac{v_{od}}{v_{ic}}\right|_{v_{id}=0} \tag{5.8}$$

Thus, the total differential output voltage can be expressed as

[a] In some texts, v_1 and v_2 are also referred to as v^+ and v^-, such that $v_d = v^+ - v^-$ and $v_c = \frac{1}{2}\left(v^+ + v^-\right)$.



(a) Ideal

(b) In the presence of common-mode noise

Figure 5.2: Differential vs. single-ended signals.

$$v_{od} = A_{dm} \cdot v_{id} + A_{cm-dm} \cdot v_{ic} \tag{5.9}$$

and the total common-mode output voltage is

$$v_{oc} = A_{cm} \cdot v_{ic} + A_{dm-cm} \cdot v_{id} \tag{5.10}$$

Why would we want to use differential signals (voltage or current) instead of single-ended signals? Consider the case when $v_1 = A \cdot \cos(\omega t) + B$ and $v_2 = A \cdot \cos(\omega t + 180°) + B$. We can express the differential voltage v_d as

$$v_d = v_1 - v_2 = A \cdot \cos(\omega t) + B - (-A \cdot \cos(\omega t) + B) = 2A \cdot \cos(\omega t) \tag{5.11}$$

and the common-mode voltage is

$$v_c = \frac{v_1 + v_2}{2} = \frac{A \cdot \cos(\omega t) + B + (-A \cdot \cos(\omega t) + B)}{2} = B \tag{5.12}$$

Fig. 5.2a shows the plot of v_1, v_2, v_d, and v_c for $A = 1\,\text{V}$, and $B = 1\,\text{V}$.

Now consider the case when some random noise voltage gets coupled into the two voltages, v_1 and v_2, such that

$$v_1' = v_1 + v_{noise} \tag{5.13}$$

$$v_2' = v_2 + v_{noise} \tag{5.14}$$

We can still calculate the differential and common-mode voltages as

$$v_d' = v_1' - v_2' = v_1 + v_{noise} - v_2 - v_{noise} = v_1 - v_2 = 2A\cos(\omega t) \tag{5.15}$$

$$v_c' = \frac{v_1' + v_2'}{2} = \frac{v_1 + v_{noise} + v_2 + v_{noise}}{2} = B + v_{noise} \tag{5.16}$$

Notice that as long as any noise or interference appears on both v_1 and v_2, it is not seen in the differential voltage, v_d'! All signals that are "common" to both v_1 and v_2 will appear as part of the common-mode signal, v_c', as seen in Fig. 5.2b. Thus, a differential amplifier that only amplifies the differential signal, and rejects the common-mode will be immune to this common-mode noise or interference. One metric of how well an amplifier amplifies the differential signal and at the same time rejects the common-mode signal is the *common-mode rejection ratio*, defined as

$$\text{CMRR} = \left| \frac{A_{dm}}{A_{cm}} \right| \tag{5.17}$$

Another advantage of using differential amplifiers is the inherent generation of both the inverting and non-inverting output. If an inverting amplifier is needed, one can simply re-label the output terminals of the amplifier in Fig. 5.1, such that v_{o1} becomes v_{o2} and vice versa.

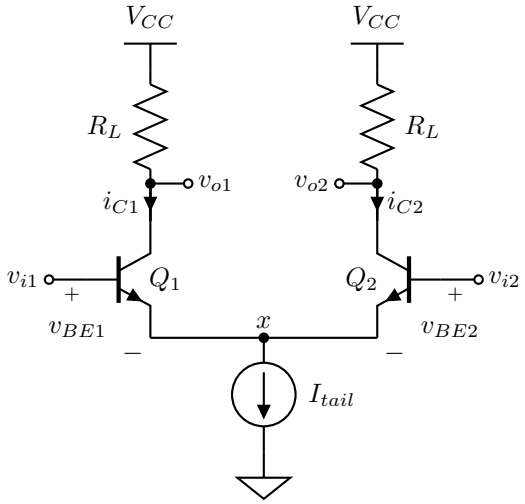


Figure 5.3: The BJT differential pair.

5.2 The BJT Differential Pair

How do we build differential circuits? One very important differential circuit building block is the BJT differential pair (or the emitter-coupled pair) with a resistor load, shown in Fig. 5.3. In order to understand how the BJT differential pair works, let us first look at its large-signal characteristics.

If we write the KVL equation around the input loop that includes the base terminals of both transistors, we get

$$V_{i1} - V_{BE1} + V_{BE2} - V_{i2} = 0 \tag{5.18}$$

Assuming that Q_1 and Q_2 are identical,

$$V_{i1} - V_{i2} = V_{id} = V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_S}\right) - V_T \ln\left(\frac{I_{C2}}{I_S}\right) = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{5.19}$$

Rearranging Eq. 5.19, we get

$$I_{C1} = I_{C2} \cdot e^{\frac{V_{id}}{V_T}} \tag{5.20}$$

Writing the KCL equation at node x,

$$I_{tail} = I_{E1} + I_{E2} = \frac{I_{C1} + I_{C2}}{\alpha} \tag{5.21}$$

Using Eqs. 5.20 and 5.21, we can get expressions for the collector currents of both transistors in terms of the input differential voltage as

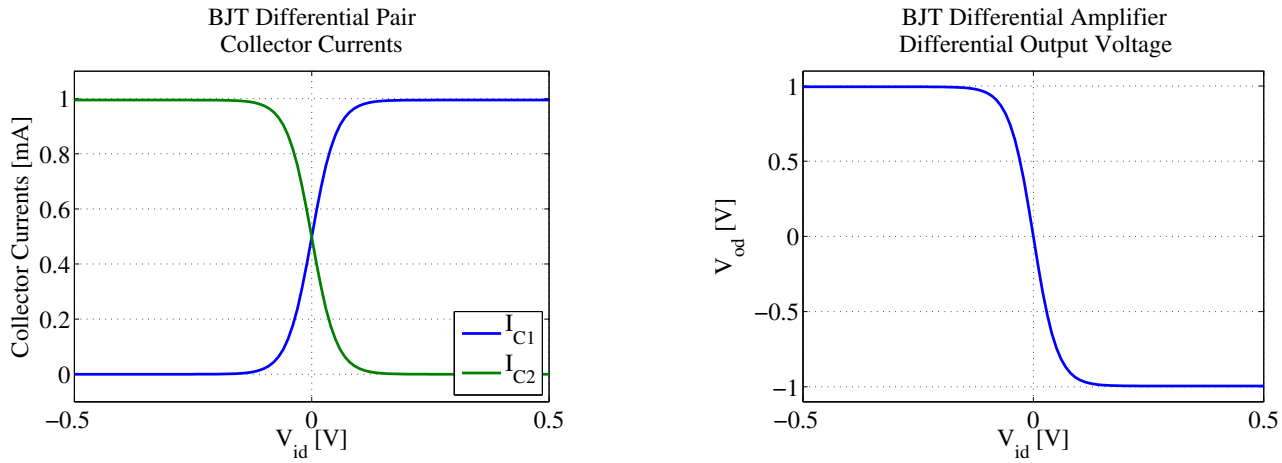
$$I_{C1} = \frac{\alpha \cdot I_{tail}}{1 + e^{-\frac{V_{id}}{V_T}}} \tag{5.22}$$

$$I_{C2} = \frac{\alpha \cdot I_{tail}}{1 + e^{+\frac{V_{id}}{V_T}}} \tag{5.23}$$

Based on Eqs. 5.22 and 5.23, the behavior of the collector currents as the input differential voltage is varied is shown in Fig. 5.4a.

When we increase the input differential voltage, V_{id}, we increase I_{C1}. But since the tail current source ensures that the sum of the two collector currents are constant, and equal to I_{tail}, any increase in I_{C1} will force I_{C2} to decrease by exactly the same amount. Also note that even if V_{i1} and V_{i2} varies, as long as they are equal, i.e. $V_{id} = 0$, both I_{C1} and I_{C2} will always be equal to $\frac{I_{tail}}{2}$.

Thus, even if the common-mode input voltage changes, for two perfectly matched transistors with an ideal tail current source, (1) the two collector currents will only be influenced by the input differential voltage, and (2) the collector currents will change in a purely differential manner, meaning that if I_{C1} increases by ΔI, or $I_{C1} = \frac{I_{tail}}{2} + \Delta I$, then $I_{C2} = \frac{I_{tail}}{2} - \Delta I$, and the common-mode current of $\frac{I_{tail}}{2}$ will not change.



(a) Collector currents

(b) Output voltage

Figure 5.4: BJT differential pair large signal characteristics for $\beta = 200$, $I_{tail} = 1\,\text{mA}$, and $R_L = 1\,\text{k}\Omega$.

5.2.1 The BJT Differential Amplifier

The collector currents are then converted to an output voltage by the two load resistors. Thus, the differential pair composed of the Q_1, Q_2 and the tail current, when loaded with R_L, can be considered a rudimentary fully differential amplifier. The output voltages are then

$$V_{o1} = V_{CC} - R_L I_{C1} \tag{5.24}$$

$$V_{o2} = V_{CC} - R_L I_{C2} \tag{5.25}$$

Solving for the differential output voltage, V_{od}, we get

$$V_{od} = V_{o1} - V_{o2} = R_L \left(I_{C2} - I_{C1}\right) \tag{5.26}$$

Combining Eqs. 5.22, 5.23, and 5.26, we get

$$V_{od} = \alpha \cdot I_{tail} \cdot R_L \left(\frac{1}{1 + e^{+\frac{V_{id}}{V_T}}} - \frac{1}{1 + e^{-\frac{V_{id}}{V_T}}} \right) = \alpha \cdot I_{tail} \cdot R_L \cdot \tanh\left(-\frac{V_{id}}{2 \cdot V_T} \right) \tag{5.27}$$

Eq. 5.27 is then the large signal differential transfer characteristic of the BJT differential amplifier since it relates the differential output voltage, V_{od}, and the differential input voltage, V_{id}, and is plotted in Fig. 5.4b.

The maximum output differential voltage we can get out of the BJT differential amplifier is equal to

$$V_{od,\max} = \alpha \cdot I_{tail} \cdot R_L \tag{5.28}$$

This is the differential output when $|V_{id}|$ is large enough such that all the tail current is flowing only on one side of the differential circuit.

5.2.2 The Common-Mode Signal Revisited

In order to simplify some of the analysis, but without loosing generality, we can assume that the input signals going into our differential amplifiers are of the form

$$v_{i1} = \frac{\hat{V}}{2} \cdot \cos\left(\omega t\right) + V_{cm} \tag{5.29}$$

$$v_{i2} = -\frac{\hat{V}}{2} \cdot \cos\left(\omega t\right) + V_{cm} \tag{5.30}$$

resulting in

$$v_{id} = v_{i1} - v_{i2} = \hat{V} \cdot \cos\left(\omega t\right) \tag{5.31}$$

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2} = V_{cm} \tag{5.32}$$

Thus, we can think of the common-mode input as a DC offset where, on top of which, we add our differential signal. Notice that v_{i1} and v_{i2} are purely differential signals since if v_{i1} increases by ΔV, v_{i2} will decrease by the same amount, relative to the common-mode voltage V_{cm}.

5.2.3 The Common-Mode Input Range

Note that Eqs. 5.19, 5.20, 5.22, 5.23, and 5.27 assume the transistor is operating in the forward-active region. In order to check the BJT operating region, we need to get the collector-emitter voltage. From Fig. 5.3, we see that

$$V_{CE1} = V_{CC} - I_{C1}R_L - V_X \tag{5.33}$$

where V_X is the voltage across the tail current source. Note that for a collector current, I_{C1}, we get

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_S}\right) \tag{5.34}$$

Therefore, we can express V_X as

$$V_X = V_{I1} - V_{BE1} \tag{5.35}$$

Thus, combining Eqs. 5.33 and 5.35, we get

$$V_{CE1} = V_{CC} - I_{C1}R_L - V_{I1} + V_T \ln\left(\frac{I_{C1}}{I_S}\right) \tag{5.36}$$

and similarly

$$V_{CE2} = V_{CC} - I_{C2}R_L - V_{I2} + V_T \ln\left(\frac{I_{C2}}{I_S}\right) \tag{5.37}$$

For the case when there is no differential input,

$$v_{i1} = V_{I1} = v_{i2} = V_{I2} = v_{ic} = V_{cm} \tag{5.38}$$

This implies that

$$I_{C1} = I_{C2} = \frac{I_{tail}}{2} \tag{5.39}$$

since the left and right side of the differential amplifier is the same, the tail current splits equally between these two sides. Thus, Eq. 5.36 becomes

$$V_{CE1} = V_{CC} - \frac{I_{tail}R_L}{2} - V_{cm} + V_T \ln\left(\frac{I_{tail}}{2 \cdot I_S}\right) > V_{CE,sat} \tag{5.40}$$

It is very important to note that as long as the transistors are in the forward-active region, the amplifier can accept a range of common-mode input voltages, and still have $I_{C1} = I_{C2} = \frac{I_{tail}}{2}$. As the common-mode input voltage is changed, the collector currents will remain the same, as enforced by the tail current source. Since the collector currents remain the same, the base-emitter voltages will also remain the same. Thus, as the common-mode input voltage increases, the voltage at node x will increase with it[b].

Using Eq. 5.40, we can then calculate the maximum common-mode input voltage as

$$V_{cm} < V_{CC} - \frac{I_{tail}R_L}{2} - V_{CE,sat} + V_T \ln\left(\frac{I_{tail}}{2 \cdot I_S}\right) = V_{cm,\max} \tag{5.41}$$

If the tail current source is not ideal and has a required minimum voltage, $V_{\min}$, then using Eq. 5.35, the minimum common-mode input voltage can then be expressed as

$$V_{cm} > V_{\min} + V_T \ln\left(\frac{I_{tail}}{2 \cdot I_S}\right) = V_{cm,\min} \tag{5.42}$$

Eqs. 5.41 and 5.42 defines the *common-mode input range* of the differential amplifier in Fig. 5.3. The common-mode input range is defined as the range of common-mode inputs that the amplifier can tolerate and still maintain proper transistor operating regions.

Unlike single-ended amplifiers and circuits, where the input DC voltages can drastically change transistor bias currents, differential amplifiers have the advantage of being able to tolerate a relatively large range of input DC voltages, while maintaining transistor bias currents.

[b] Readers will recognize that the path from v_{i1} to node x is a common-collector or emitter-follower path, and it should be no surprise that node x will try to follow v_{i1}.

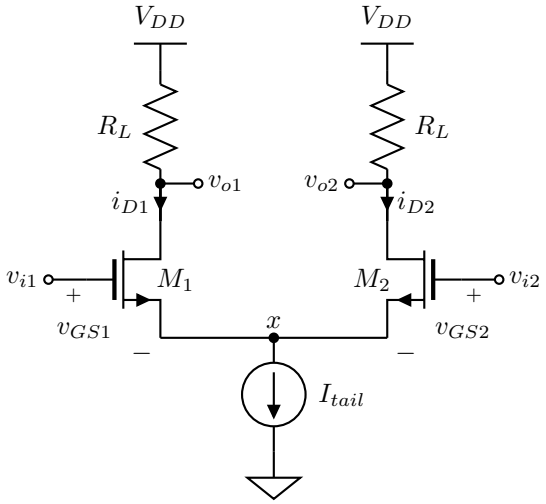


Figure 5.5: The MOSFET differential pair.

5.3 The MOSFET Differential Amplifier

We can use MOSFETs to build differential amplifier, as seen in Fig. 5.5. Once again, we can write the KVL equation for the input loop as

$$V_{i1} - V_{i2} = V_{id} = V_{GS1} - V_{GS2} \tag{5.43}$$

$$V_{id} = \left(V_{TH} + \sqrt{\frac{I_{D1}}{k}}\right) - \left(V_{TH} + \sqrt{\frac{I_{D2}}{k}}\right) = \sqrt{\frac{I_{D1}}{k}} - \sqrt{\frac{I_{D2}}{k}} \tag{5.44}$$

and again applying KCL at node x, we get

$$I_{tail} = I_{D1} + I_{D2} \tag{5.45}$$

Using Eqs. 5.44 and 5.45 to solve for the drain currents, we get

$$I_{D1} = \frac{I_{tail}}{2} + V_{id} \cdot \frac{k}{2} \cdot \sqrt{\frac{2 \cdot I_{tail}}{k} - V_{id}^2} = \frac{I_{tail}}{2} + \Delta I \tag{5.46}$$

$$I_{D2} = \frac{I_{tail}}{2} - V_{id} \cdot \frac{k}{2} \cdot \sqrt{\frac{2 \cdot I_{tail}}{k} - V_{id}^2} = \frac{I_{tail}}{2} - \Delta I \tag{5.47}$$

Note that for Eqs. 5.46 and 5.47, $I_{D1,\max} = I_{D2,\max} = I_{tail}$ and $I_{D1,\min} = I_{D2,\min} = 0$, as dictated by the tail current source. However, increasing or decreasing V_{id} in Eqs. 5.46 and 5.47 can result in currents larger than the maximum or currents below the minimum current. This means that at a certain differential input voltage, one transistor will cut-off, while the other will carry all of I_{tail}. This condition occurs when

$$\Delta I = \frac{I_{tail}}{2} = V_{id,\max} \cdot \frac{k}{2} \cdot \sqrt{\frac{2 \cdot I_{tail}}{k} - V_{id,\max}^2} \tag{5.48}$$

Solving for $V_{id,\max}$, we get

$$V_{id,\max} = \sqrt{\frac{I_{tail}}{k}} \tag{5.49}$$

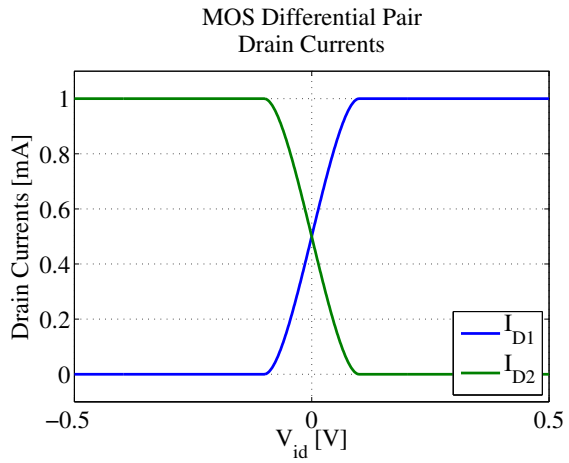
Thus, as long as $|V_{id}| \leq V_{id,\max}$, Eqs. 5.46 and 5.47 are valid. However, if the input differential voltage is outside this range, then for $V_{id} > 0$, $I_{D1} = I_{tail}$ and $I_{D2} = 0$, and for $V_{id} < 0$, $I_{D1} = 0$ and $I_{D2} = I_{tail}$, as seen in Fig. 5.6a.

The differential output voltage is then

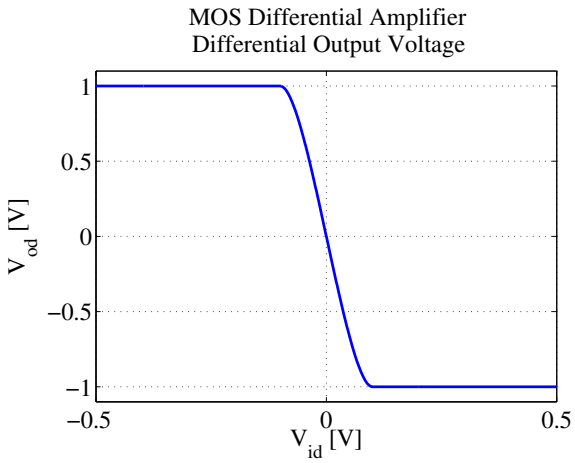
$$V_{od} = V_{o1} - V_{o2} = R_L \left(I_{D2} - I_{D1}\right) = -R_L \cdot k \cdot V_{id} \cdot \sqrt{\frac{2 \cdot I_{tail}}{k} - V_{id}^2} \tag{5.50}$$

Using Eqs. 5.49 and 5.50, we can calculate the maximum value of the differential output voltage as

$$V_{od,\max} = R_L \cdot k \cdot V_{id,\max} \cdot \sqrt{\frac{2 \cdot I_{tail}}{k} - V_{id,\max}^2} = R_L \cdot I_{tail} \tag{5.51}$$



(a) Drain currents



(b) Output voltage

Figure 5.6: MOSFET differential pair large signal characteristics with $V_{TH} = 1\,\text{V}$, $k = 100\,\frac{\text{mA}}{\text{V}^2}$, using $R_L = 1\,\text{k}\Omega$, a tail current of 1 mA, and a supply voltage of 5 V.

which is expected since the maximum differential voltage appears when all the current is already on one side of the differential pair, resulting in zero current on the other side, as seen in Fig. 5.6b.

5.3.1 Common-Mode Input Range

The drain-source voltage of transistor M_1 can be expressed as

$$V_{DS1} = V_{DD} - I_{D1}R_L - V_X \tag{5.52}$$

We can then express V_X as

$$V_X = V_{I1} - V_{GS1} \tag{5.53}$$

Thus, to prevent M_1 from going into the linear region,

$$V_{DS1} = V_{DD} - I_{D1}R_L - V_{I1} + V_{GS1} > V_{GS1} - V_{TH} \tag{5.54}$$

If we set the differential input to zero and apply only the common-mode input, $V_{I1} = V_{I2} = V_{cm}$, we get

$$V_{DD} - \frac{I_{tail}R_L}{2} - V_{cm} > -V_{TH} \tag{5.55}$$

Therefore,

$$V_{cm} < V_{DD} - \frac{I_{tail}R_L}{2} + V_{TH} = V_{cm,\max} \tag{5.56}$$

The common-mode input must also be large enough to support the minimum voltage requirement, $V_{\min}$, of the tail current source, thus

$$V_X = V_{cm} - V_{GS1} > V_{\min} \tag{5.57}$$

Thus,

$$V_{cm} > V_{\min} + V_{GS1} = V_{\min} + V_{TH} + \sqrt{\frac{I_{tail}}{2 \cdot k}} = V_{cm,\min} \tag{5.58}$$

5.4 Small Signal Analysis

After obtaining the quiescent DC currents of the simple differential amplifier, we can now determine the corresponding small signal two-port characteristics. The small signal equivalent circuit of the BJT differential amplifier in Fig. 5.3 is shown in Fig. 5.7.

Let us analyze the small signal behavior of the differential amplifier in two steps. First, we will look at the amplifier's response to purely differential signals, then we will look at the response to purely common-mode signals. Since the small signal equivalent circuit is linear, we can get the total behavior of the differential amplifier by superposition.

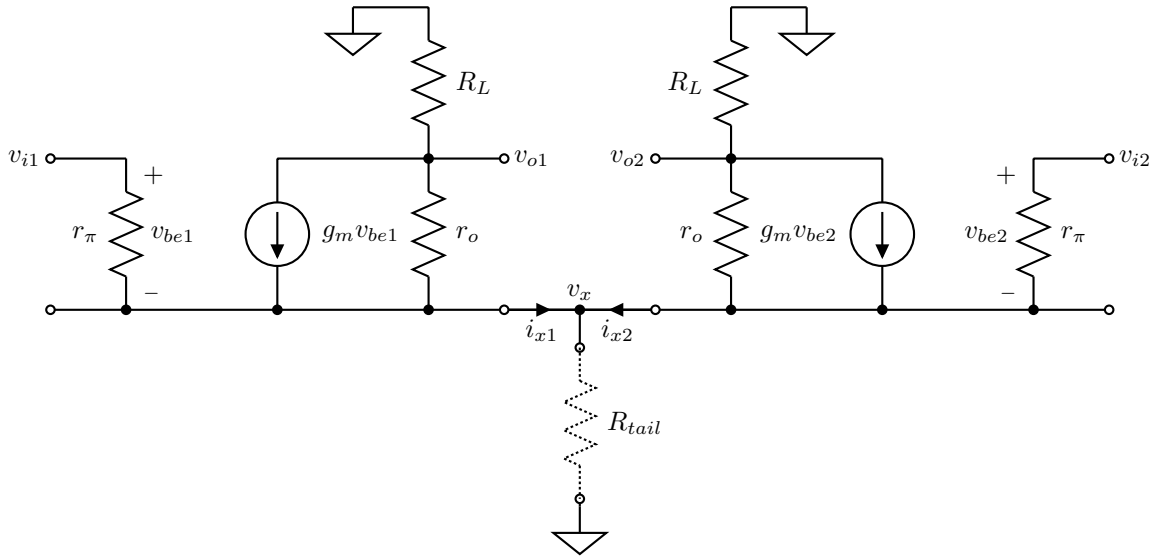


Figure 5.7: The small signal equivalent circuit of the BJT differential amplifier in Fig. 5.3.

5.4.1 The Differential Half Circuit

If we only have purely differential signals, then this means that for an input differential voltage, v_{id},

$$v_{i1} = +\frac{v_{id}}{2} \tag{5.59}$$

$$v_{i2} = -\frac{v_{id}}{2} \tag{5.60}$$

such that

$$v_{id} = v_{i1} - v_{i2} \tag{5.61}$$

$$v_{ic} = \frac{v_{i1} + v_{i2}}{2} = 0 \tag{5.62}$$

Eqs. 5.59 and 5.60 mathematically models the fact that if the inputs are purely differential inputs, then a small change in v_{i1} would be accompanied by the same change in v_{i2} but in the opposite direction.

Writing out the KVL expression for the input loop, we get

$$v_{i1} - v_{be1} + v_{be2} - v_{i2} = \left(+\frac{v_{id}}{2}\right) - v_{be1} + v_{be2} - \left(-\frac{v_{i2}}{2}\right) = 0 \tag{5.63}$$

thus,

$$v_{id} = v_{i1} - v_{i2} = v_{be1} - v_{be2} \tag{5.64}$$

Note that v_x is the midpoint between $+\frac{v_{id}}{2}$ and $-\frac{v_{id}}{2}$. Thus, for any purely differential input, v_{id}, and if the left and right sides of the circuit are perfectly matched, then we will always get

$$v_x = 0 \tag{5.65}$$

Since v_x is always zero for purely differential inputs, then node x can be considered a *virtual ground* node. Therefore, we can redraw the small signal equivalent circuit in Fig. 5.7, and obtain the differential small signal equivalent circuit in Fig. 5.8.

By making node x a virtual ground, we have effectively decoupled the left and right sides of the differential small signal equivalent circuit. Thus, we can solve for the differential small signal two-port parameters using either the left or right side of the circuit in Fig. 5.8.

Using the left half circuit, we can calculate the differential mode gain as

$$A_{dm} = \frac{+\frac{v_{od}}{2}}{+\frac{v_{id}}{2}} = \frac{v_{od}}{v_{id}} = -g_m \cdot (r_o \parallel R_L) \tag{5.66}$$

If we apply a test voltage, $+\frac{v_{id}}{2}$, at the input, we get

$$i_{id} = \frac{+\frac{v_{id}}{2}}{r_\pi} \tag{5.67}$$

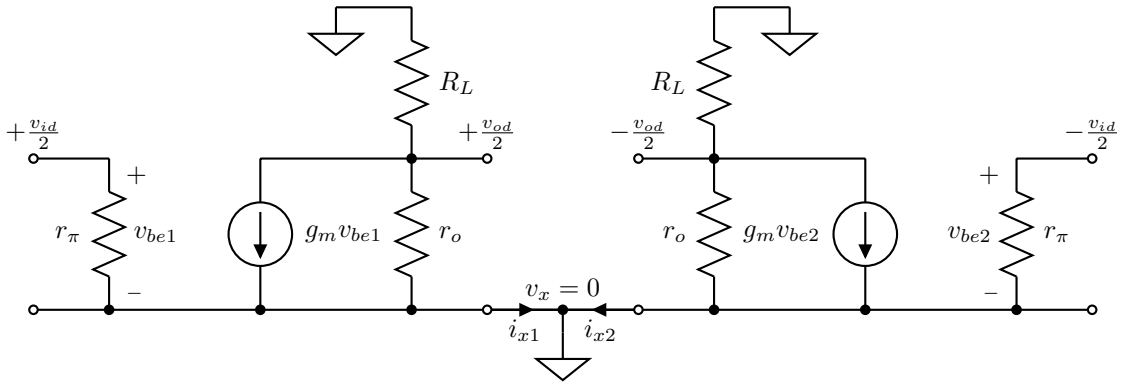


Figure 5.8: The differential small signal equivalent circuit of the amplifier in Fig. 5.3.

Thus, the input resistance can be expressed as

$$R_{id} = \frac{v_{id}}{i_{id}} = 2 \cdot r_\pi \tag{5.68}$$

Similarly, if we zero out the input, and apply a test voltage, $+\frac{v_{od}}{2}$, at the output, we get

$$i_{od} = \frac{+\frac{v_{od}}{2}}{r_o \parallel R_L} \tag{5.69}$$

The output resistance is then

$$R_{od} = \frac{v_{od}}{i_{od}} = 2 \cdot (r_o \parallel R_L) \tag{5.70}$$

We would get exactly the same expressions if we used the right half circuit of Fig. 5.8.

It is important to node that while we can consider node x as a virtual ground, no small signal current flows from node x to the small signal ground. Instead, all the current going into node x from the left half circuit is exactly the same current going out of node x into the right half circuit. Thus,

$$i_{x1} = -i_{x2} \tag{5.71}$$

This is consistent with purely differential mode inputs, since any small signal increase in voltage or current on the left side would correspond to a decrease of equal magnitude on the right side. This is true for the open circuit from node x to ground in Fig. 5.7, but it is also true even if we add any resistance to ground (e.g. if we use a tail current source with finite output resistance, R_{tail}), since $v_x = 0$.

5.4.2 The Common-Mode Half Circuit

If we only apply a purely common-mode input, v_{ic}, such that

$$v_{ic} = v_{i1} = v_{i2} \tag{5.72}$$

the differential input component will be

$$v_{id} = v_{i1} - v_{i2} = 0 \tag{5.73}$$

So if the left side of the differential amplifier is perfectly matched to the right side, then the output differential voltage will also be zero, hence

$$v_{o1} = v_{o2} = v_{oc} \tag{5.74}$$

This also means that there will be no current flowing from the left side to the right side (or vice versa) since every single node on the left side will have the same voltage as the corresponding node on the right, thus

$$i_{x1} = i_{x2} = 0 \tag{5.75}$$

Extending this idea to the whole circuit, any connection from the left side and the right side would have zero current, isolating the left side from the right. This allows us to calculate the common-mode small signal parameters using only one side of the circuit in Fig. 5.7.

To solve for the common-mode gain, we first write out the KCL equation at node x,

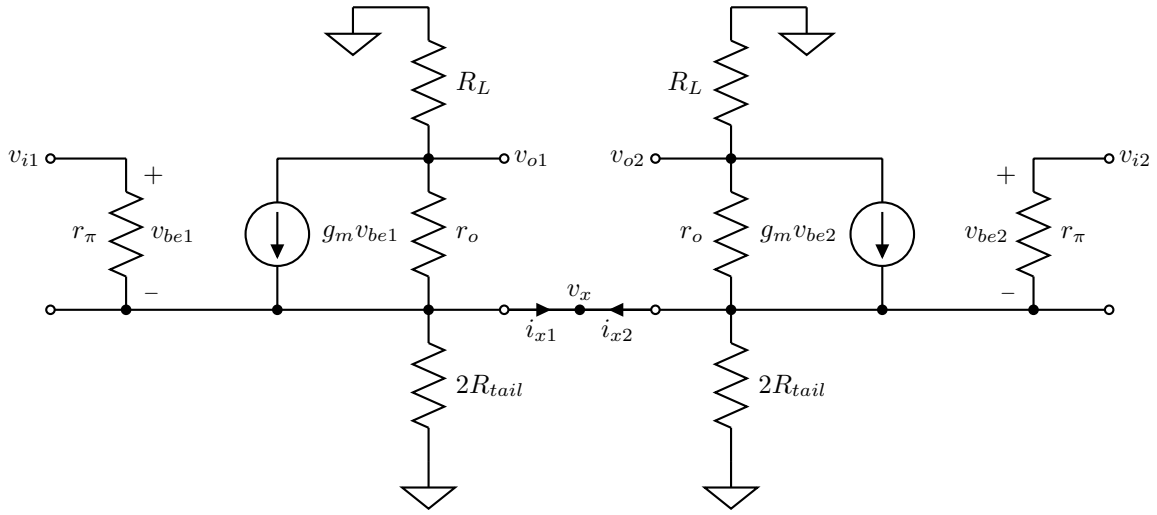


Figure 5.9: The common-mode small signal equivalent circuit of the BJT differential amplifier in Fig. 5.3.

$$\frac{v_x - v_{ic}}{r_\pi} + \frac{v_x - v_{oc}}{r_o} - g_m\left(v_{ic} - v_x\right) = 0 \tag{5.76}$$

and recognizing the that the current passing through r_π is the same current passing through R_L, we get

$$\frac{v_{oc}}{R_L} = \frac{v_{ic} - v_x}{r_\pi} \tag{5.77}$$

Using Eqs. 5.76 and 5.77, we can then express v_{oc} as

$$v_{oc} = v_{ic} \cdot \frac{R_L}{R_L + r_o + r_\pi\left(1 + g_m r_o\right)} \tag{5.78}$$

Thus, the small signal common-mode gain is

$$A_{cm} = \frac{v_{oc}}{v_{ic}} = \frac{R_L}{R_L + r_o + r_\pi\left(1 + g_m r_o\right)} \tag{5.79}$$

Assuming that$g_m r_o \gg 1$ and $r_o \gg R_L$, we get

$$A_{cm} \approx \frac{R_L}{r_\pi g_m r_o} \approx \frac{R_L}{\frac{\beta}{g_m} g_m r_o} \approx \frac{R_L}{\beta \cdot r_o} \approx 0 \tag{5.80}$$

If the tail current source is not ideal, but instead has an output resistance R_{tail}, breaks the even symmetry of the small signal model, making it hard to distinguish the left side of the circuit in Fig. 5.8 from the right side. To restore even symmetry, we can decompose R_{tail} into two parallel resistors, each with resistance value $2R_{tail}$, as shown in Fig. 5.9. Since we have even symmetry once again, and $i_{x1} = i_{x2} = 0$, then we can solve for the common-mode gain using only either the left or right half circuit.

If we take the left half circuit, and recognizing that this is exactly the same as the equivalent circuit of an emitter degenerated common-emitter amplifier, with $R_E = 2R_{tail}$, then the common-mode gain can be expressed as

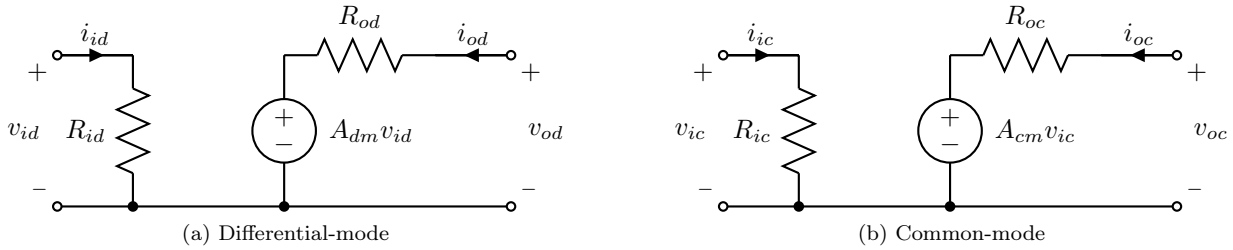
$$A_{cm} = -\frac{g_m R_L}{1 + 2 \cdot g_m R_{tail}} \tag{5.81}$$

Note that since the common-mode source has to supply the input currents of both the left and right half circuits, the common-mode input resistance is half that of the input resistance of the common-emitter amplifier with emitter degeneration. Thus,

$$R_{ic} = \frac{v_{ic}}{i_{ic,left} + i_{ic,right}} = \frac{v_{ic}}{2i_{ic}} = \frac{r_\pi\left(1 + 2 \cdot g_m R_{tail}\right)}{2} \tag{5.82}$$

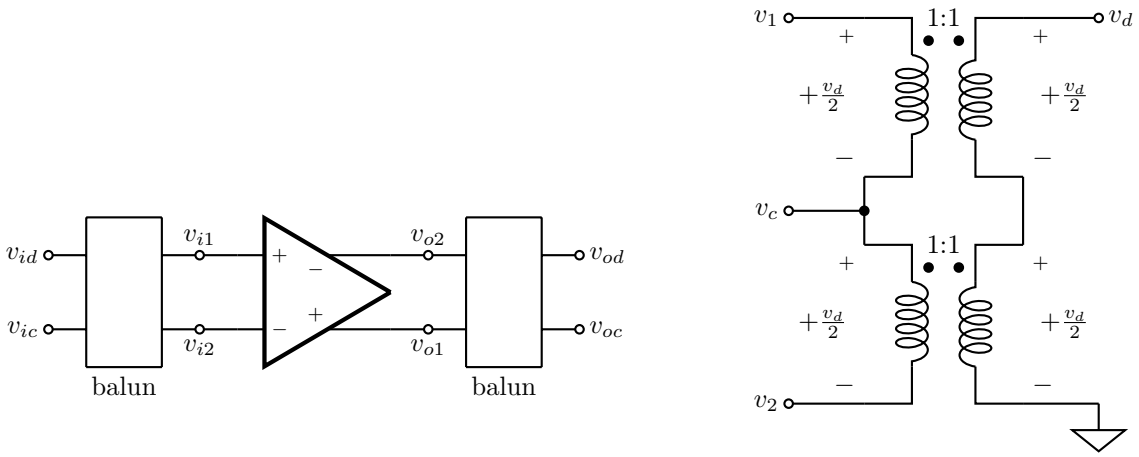
As expected, the output resistance will also be half of the emitter-degenerated amplifier output resistance since for the same output test voltage, we get twice the output current, one for each half circuit. Thus,

$$R_{oc} = \frac{v_{oc}}{i_{oc,left} + i_{oc,right}} = \frac{v_{oc}}{2i_{oc}} = \frac{r_o\left(1 + 2 \cdot g_m R_{tail}\right)}{2} \tag{5.83}$$



(a) Differential-mode (b) Common-mode

Figure 5.10: The small signal model of the BJT differential amplifier.



(a) Differential signal conversion (b) Equivalent circuit

Figure 5.11: The balun.

In summary, differential amplifiers process the differential- and common-mode signals differently. We can then think of differential amplifiers as two distinct amplifiers, one processing the differential-mode signal, and the other, manipulating the common-mode input, as shown in Fig. 5.10.

Note that the small signal analysis for MOSFET differential amplifiers is exactly the same as the analysis of its BJT counterpart. The only difference would be the expressions used to determine the transistor small signal two-port parameters, leading to $r_\pi \to \infty$.

5.5 The Balun

In many situations, it is necessary to convert single-ended signals into differential signals, and vice versa. For example, the differential component of the input could be generated separately from the common-mode DC input component, also known as an "unbalanced" pair. From the unbalanced pair, we want to generate "balanced" two wires whose difference contains the differential information, and whose average contains the common-mode information. Fig. 5.11a shows a system that uses a "balanced-unbalanced" converter, or a *balun*, to convert from the (v_d, v_c) coordinate system to the (v_1, v_2) coordinate system an vice-versa.

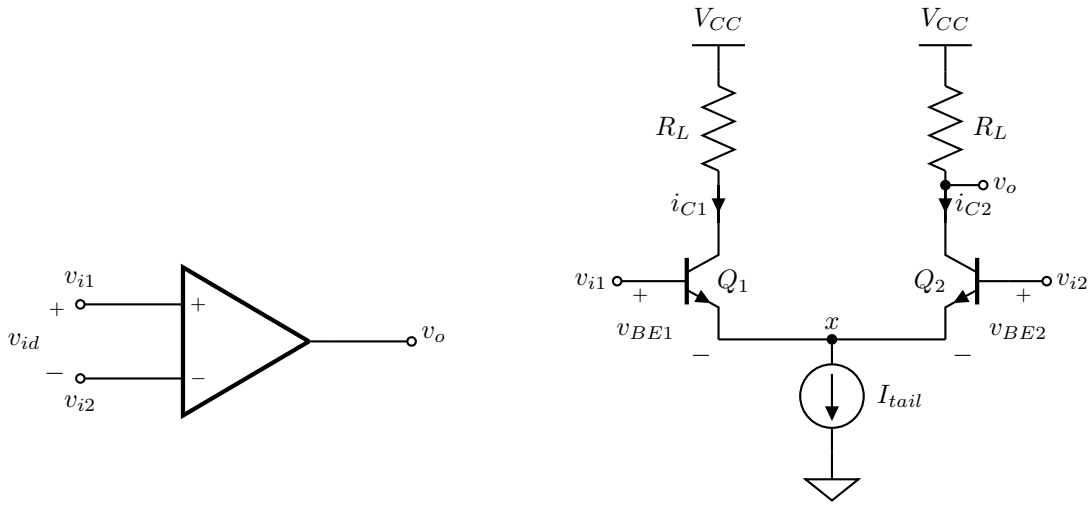
Fig. 5.11b shows a very simple balun implementation using two ideal transformers. Note that the circuit in Fig. 5.11b is bidirectional. Given v_d and v_c, it generates v_1 and v_2, realizing Eqs. 5.3 and 5.4, and if given v_1 and v_2, the balun generates v_d and v_c, as described in Eqs. 5.1 and 5.2.

5.6 Differential to Single-Ended Conversion

In some cases, the circuits driven by our amplifiers can only accept single-ended signals referred to ground. We still however, want to be able to transfer the differential output signal to the load circuit. Simply connecting one differential output to ground is normally not a good idea since the output node usually has some non-zero DC output level.

Differential input, single-ended output amplifiers, whose symbol is shown in Fig. 5.12a, are a class of amplifiers that allows us to drive single-ended loads. A relatively straightforward implementation of such an amplifier, seen in Fig. 5.12b, simply takes one side of the differential amplifier output, as the terminal used to drive the single-ended load.

Using our differential half circuit analysis, we get



(a) Symbol (b) A simple implementation

Figure 5.12: A single-ended output differential input amplifier.

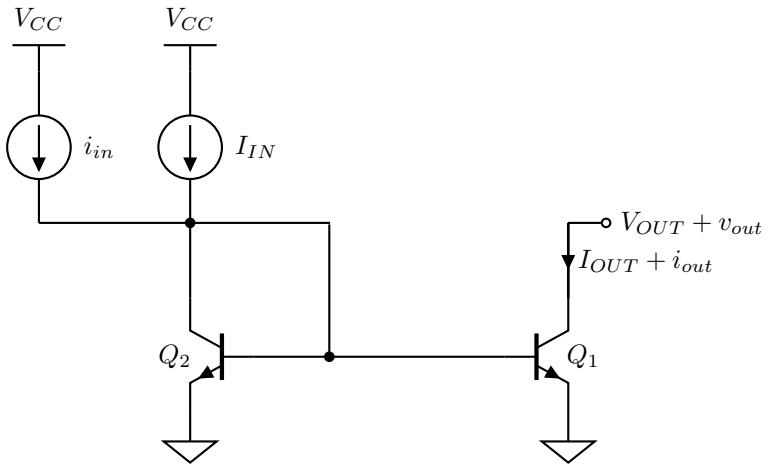


Figure 5.13: The simple BJT current mirror with small signal input current, i_{in}.

$$v_o = -g_m \left(r_o \parallel R_L\right) \cdot \left(-\frac{v_{id}}{2}\right) \tag{5.84}$$

The gain is then

$$A_v = \frac{v_o}{v_{id}} = \frac{g_m \left(r_o \parallel R_L\right)}{2} \tag{5.85}$$

As expected, the single-ended gain is only half the fully differential gain, since we are only using one half of the differential amplifier's capacity. This method of driving single-ended loads, however, is not very efficient, since we are not only getting half the gain of a common-emitter amplifier, but also comsuming twice the current for the same g_m.

An alternative way to generate a single-ended signal from a fully differential amplifier is through the use of current mirrors.

5.6.1 The Current Mirror Revisited

Before we use current mirrors for differential-to-single-ended signal conversion, we need another look at their small signal behavior. If we add a small signal current, i_{in}, on top of the DC current, I_{IN}, at the input of our current mirror, as shown in Fig. 5.13, how much of that would make it to the output?

We can easily derive the small signal equivalent circuit of the current mirror, as seen in Fig. 5.14 . Assuming $g_m r_o \gg 1$ and that β and r_o are relatively large, calculating the base-emitter voltage of both transistors, we get

$$v_{be1} = v_{be2} = i_{in} \cdot \left(\frac{1}{g_{m2}} \parallel r_{o2} \parallel r_{\pi 1} \parallel r_{\pi 2}\right) \approx \frac{i_{in}}{g_{m2}} \tag{5.86}$$

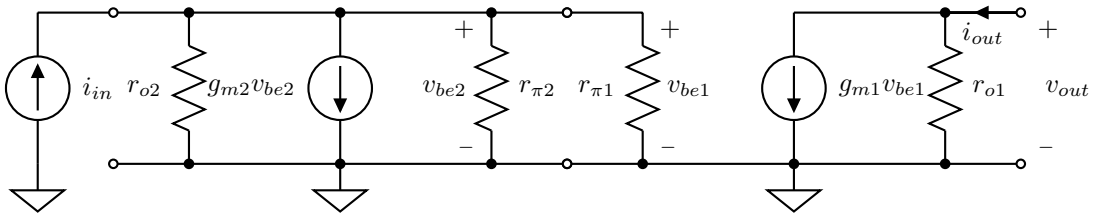


Figure 5.14: Small signal quivalent of the circuit in Fig. 5.13.

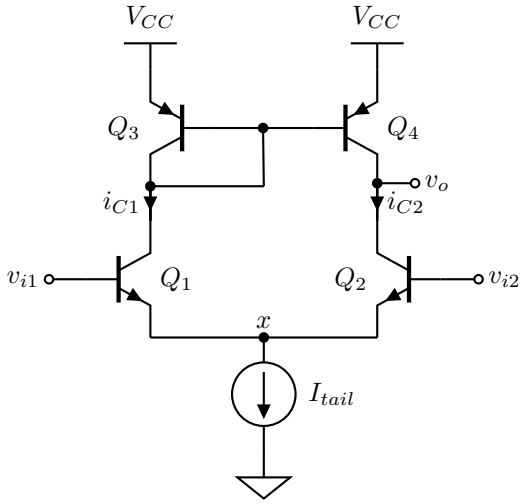


Figure 5.15: Differential to single-ended conversion using current mirrors.

Thus, if we assume that $I_{C1} \approx I_{C2}$, then the small signal output current is

$$i_{out} \approx g_{m1} v_{be1} = \frac{g_{m1}}{g_{m2}} \cdot i_{in} \approx i_{in} \tag{5.87}$$

This very simple analysis shows that the current mirror is not only a mirror for DC input currents, but is also a mirror for small signal input currents. We will use this property to make our differential-to-single-ended conversion more efficient in terms of gain.

5.6.2 Current Mirror Loads

Fig. 5.15 shows a differential amplifier, but instead of resistors, the load is a PNP current mirror, where the output, v_o, is a single-ended signal.

Since the amplifier in Fig. 5.15 no longer exhibits any symmetry, we cannot apply our half circuit analysis techniques, and we will need to perform the analysis on the whole small signal equivalent circuit, shown in Fig. 5.16.

If we once again assume that $g_m r_o \gg 1$, and that β and r_o are relatively large, we can simplify the small signal equivalent circuit in Fig. 5.16, as shown in Fig. 5.17. For purely differential inputs, node x will still be at virtual ground, and $v_{be1} = +\frac{v_{id}}{2}$ and $v_{be2} = -\frac{v_{id}}{2}$. Note that

$$v_{be3} = -g_{m1} \cdot \frac{v_{id}}{2} \cdot \frac{1}{g_{m3}} = v_{be4} \tag{5.88}$$

By shorting the output to ground, no current will pass through r_{o2} and r_{o4}, thus we can calculate the effective transconductance of the amplifier by first calculating the output short circuit current, i_o, as

$$i_o = g_{m4} \cdot v_{be4} + g_{m2} \cdot v_{be2} = -g_{m4} \cdot g_{m1} \cdot \frac{v_{id}}{2} \cdot \frac{1}{g_{m3}} - g \cdot \frac{v_{id}}{2} \tag{5.89}$$

If $g_{m1} = g_{m2} = g_m$ and $g_{m3} = g_{m4}$, we will get

$$i_o = -g_m \cdot v_{id} \tag{5.90}$$

Thus, the effective circuit transconductance is

$$G_m = -g_m \tag{5.91}$$

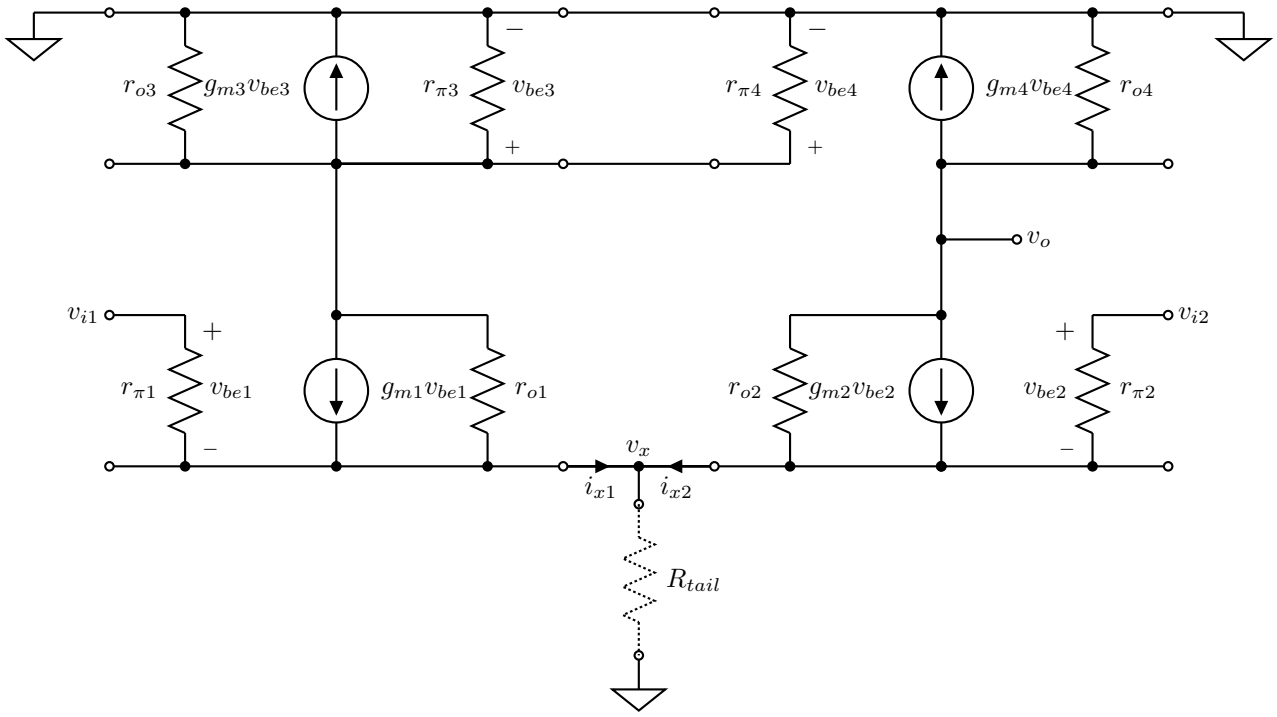


Figure 5.16: The small signal equivalent circuit of the amplifier in Fig. 5.15.

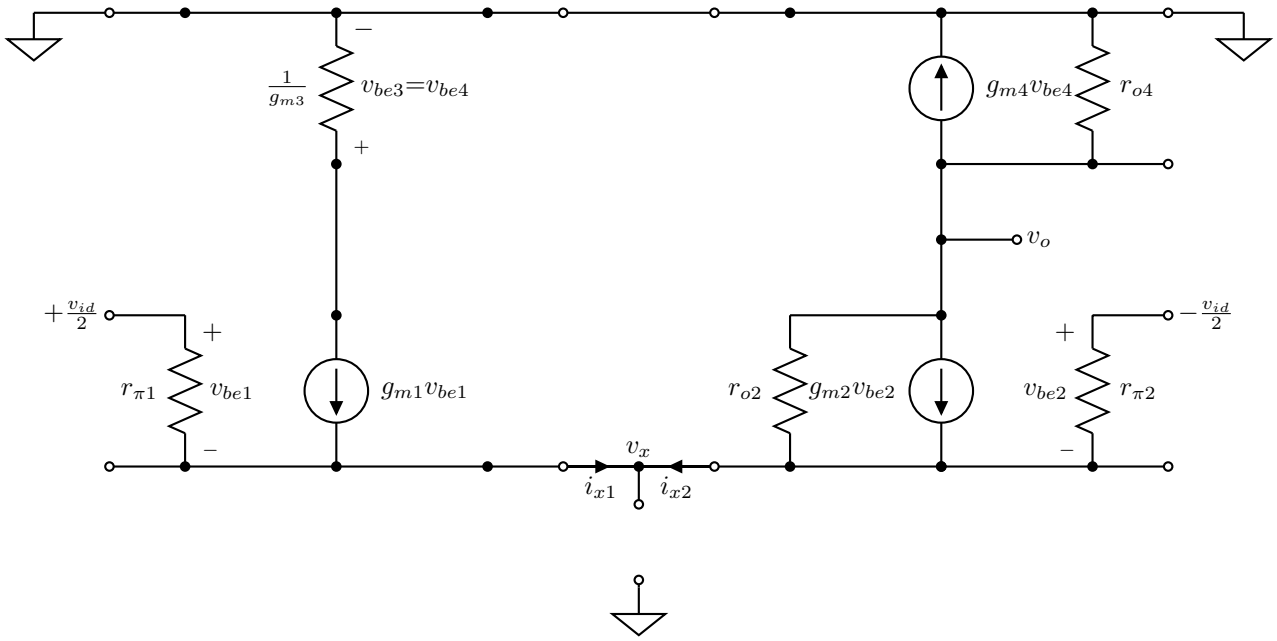


Figure 5.17: Simplified differential small signal equivalent of the circuit in Fig. 5.16.

If we zero out the input, then by inspecting the circuit in Fig. 5.17, we can see that all the dependent current sources will be turned off (zero current), thus the output resistance is

$$R_o = (r_{o2} \parallel r_{o4}) \tag{5.92}$$

The overall gain from the differential input to the single-ended output is

$$A_v = \frac{v_o}{v_{id}} = -G_m R_o = g_m (r_{o2} \parallel r_{o4}) \tag{5.93}$$

We can easily see that with the current mirror load, we will be able to achieve the same gain as the fully differential amplifier. Note that by using a current mirror as the differential amplifier load allows us to redirect the small signal current of the left half circuit to the output, where it combines constructively with the current generated by the right half circuit.