
STM32
CubeMX

1. Description

1.1. Project

Project Name	2020_RW_controller
Board Name	NUCLEO-F303K8
Generated with:	STM32CubeMX 6.1.2
Date	03/01/2021

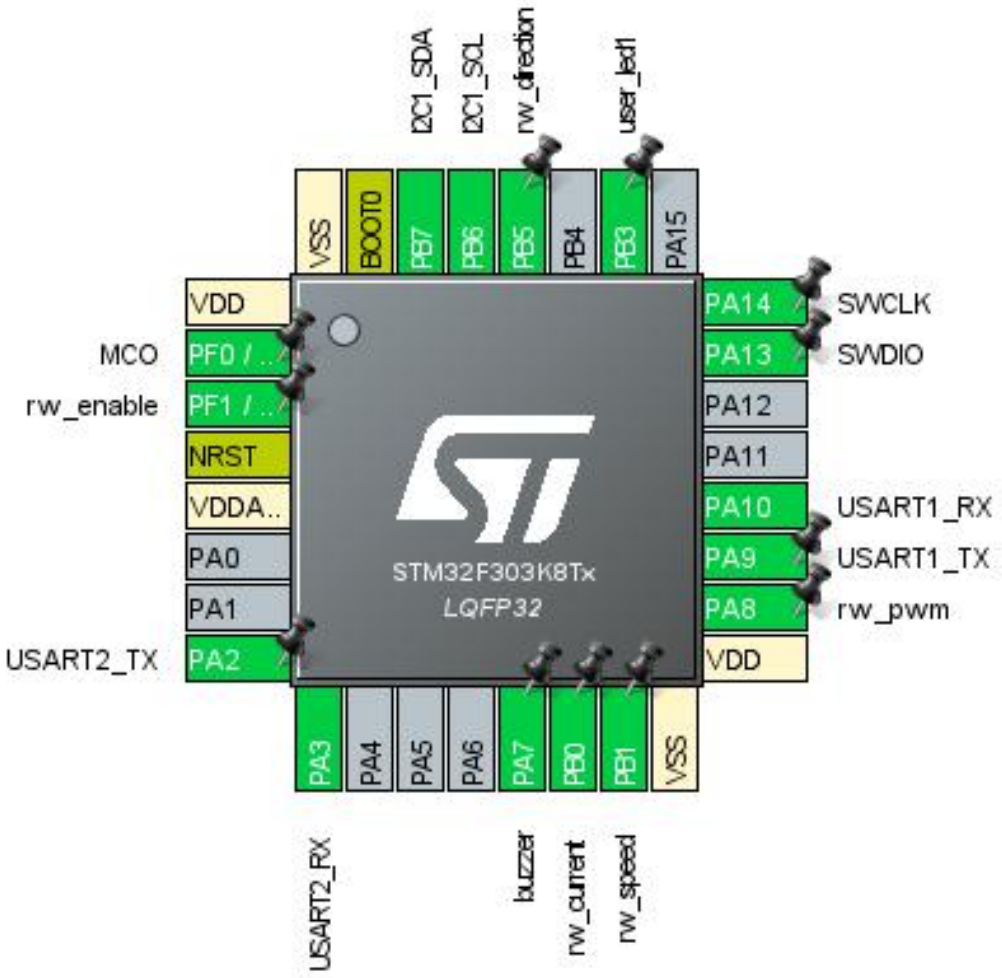
1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303K8Tx
MCU Package	LQFP32
MCU Pin number	32

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

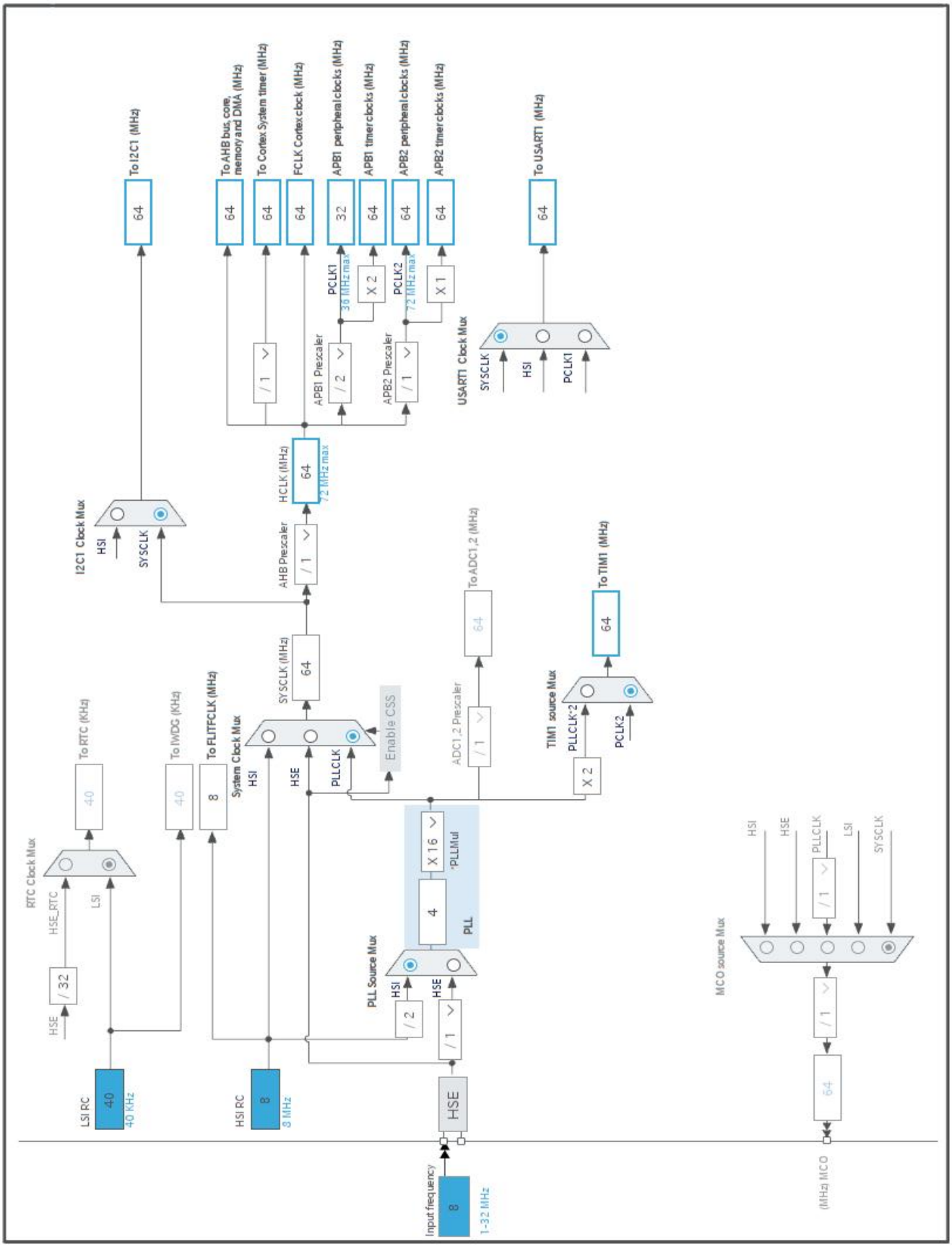


3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0 / OSC_IN	I/O	RCC_OSC_IN	MCO
3	PF1 / OSC_OUT *	I/O	GPIO_Output	rw_enable
4	NRST	Reset		
5	VDDA/VREF+	Power		
8	PA2	I/O	USART2_TX	
9	PA3	I/O	USART2_RX	
13	PA7 *	I/O	GPIO_Output	buzzer
14	PB0	I/O	ADC1_IN11	rw_current
15	PB1	I/O	ADC1_IN12	rw_speed
16	VSS	Power		
17	VDD	Power		
18	PA8	I/O	TIM1_CH1	rw_pwm
19	PA9	I/O	USART1_TX	
20	PA10	I/O	USART1_RX	
23	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
24	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
26	PB3 *	I/O	GPIO_Output	user_led1
28	PB5 *	I/O	GPIO_Output	rw_direction
29	PB6	I/O	I2C1_SCL	
30	PB7	I/O	I2C1_SDA	
31	BOOT0	Boot		
32	VSS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	2020_RW_controller
Project Folder	/home/jack/STM32CubeIDE/workspace_1.4.0/2020_RW_controller
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_USART2_UART_Init	USART2
5	MX_ADC1_Init	ADC1
6	MX_I2C1_Init	I2C1
7	MX_TIM1_Init	TIM1
8	MX_USART1_UART_Init	USART1
9	MX_TIM2_Init	TIM2
10	MX_TIM17_Init	TIM17
11	MX_TIM3_Init	TIM3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303K8Tx
Datasheet	DS9866_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

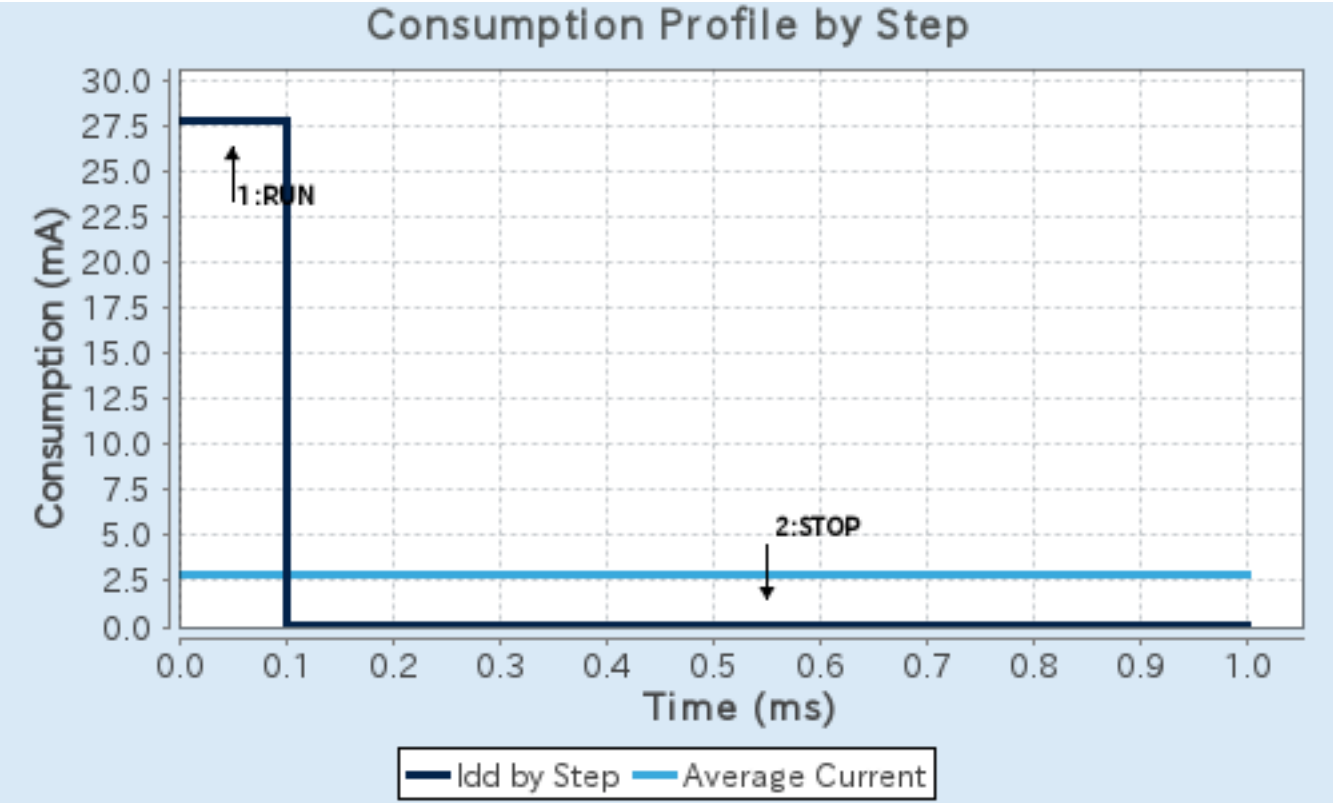
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	RAM	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSEBYP PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27.84 mA	9.55 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	98.99	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.79 mA
Battery Life	1 month, 20 days, 5 hours	Average DMIPS	90.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
30.0
27.5
25.0
22.5
20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN11: IN11 Single-ended

mode: IN12

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
SequencerNbRanks	1
Rank	1
Channel	Channel 11
Sampling Time	**181.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 12 ***
Sampling Time	**181.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00602173 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.3. RCC

High Speed Clock (HSE): BYPASS Clock Source

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100

LSE Startup Timout Value (ms)	5000

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**64-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.6. TIM2

Clock Source : Internal Clock

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1280000-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.7. TIM3

Clock Source : Internal Clock

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**64-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.8. TIM17

mode: Activated

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**64-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000-1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

7.9. USART1

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.10. USART2

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PB0	ADC1_IN11	Analog mode	No pull up pull down	n/a	rw_current
	PB1	ADC1_IN12	Analog mode	No pull up pull down	n/a	rw_speed
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull up	**High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull up	**High ***	
RCC	PF0 / OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull up pull down	Low	rw_pwm
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PA3	USART2_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
GPIO	PF1 / OSC_OUT	GPIO_Output	Output Push Pull	No pull up pull down	Low	rw_enable
	PA7	GPIO_Output	Output Push Pull	No pull up pull down	Low	buzzer
	PB3	GPIO_Output	Output Push Pull	No pull up pull down	Low	user_led1
	PB5	GPIO_Output	Output Push Pull	No pull up pull down	Low	rw_direction

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	**Word ***

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
TIM2 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
USART1 global interrupt / USART1 wake-up interrupt through EXT line 25	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger and commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
I2C1 event global interrupt / I2C1 wake-up interrupt through EXT line 23	unused		
I2C1 error interrupt	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXT line 26	unused		
Floating point unit interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false

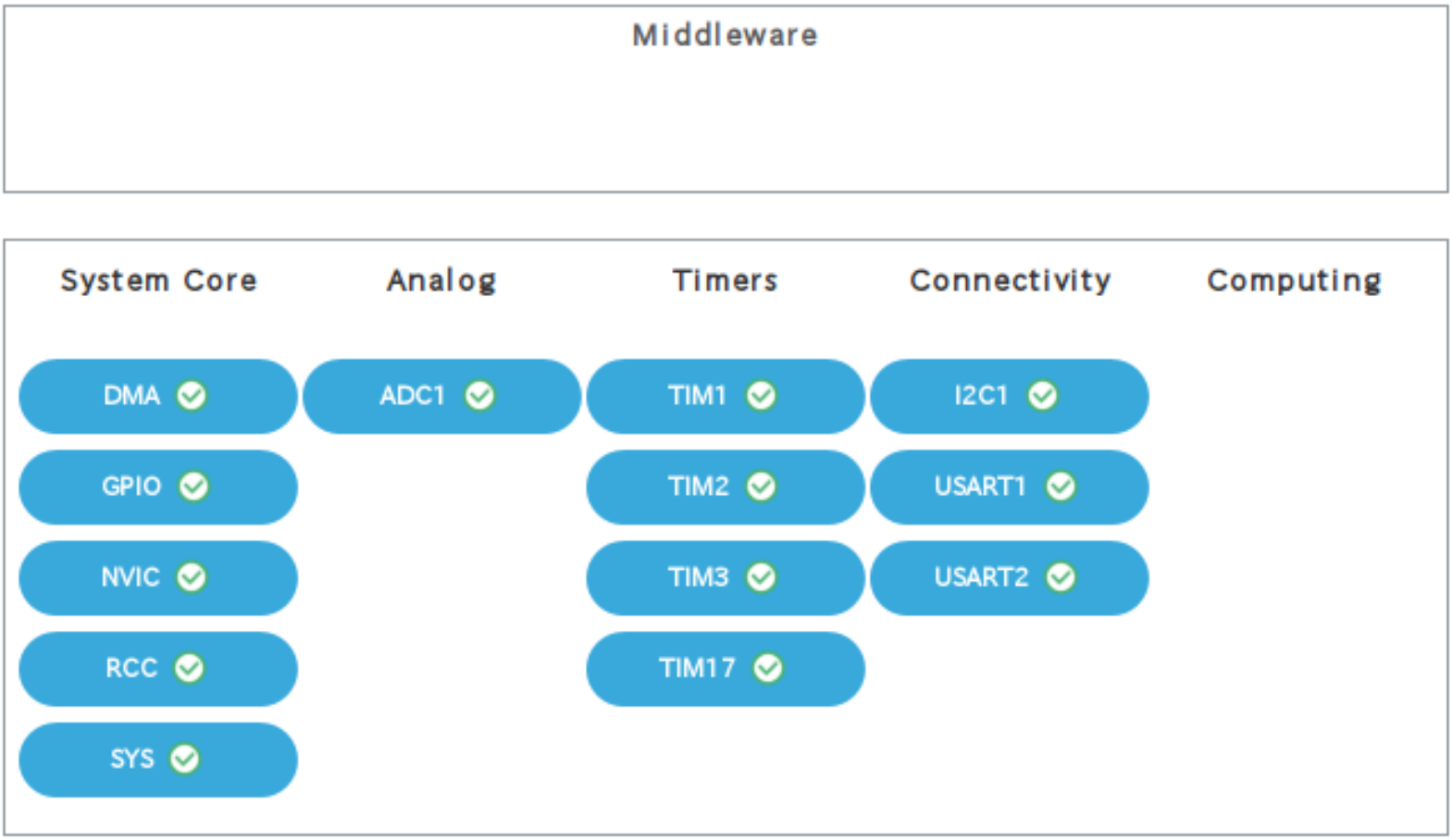
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
TIM2 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
USART1 global interrupt / USART1 wake-up interrupt through EXT line 25	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00092070.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00043574.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00109011.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00083249.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00157785.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note	http://www.st.com/resource/en/application_note/DM00210617.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00260340.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00269146.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00445657.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00607955.pdf
Application note	http://www.st.com/resource/en/application_note/DM00442720.pdf