Jieming Yin

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OBJECTIVE: Hardware/Software Engineering, Spring 2015

EDUCATION

Ph.D in Computer Science

University of Minnesota, Twin Cities, Sep. 2009–Dec. 2014 (expected)
Thesis Research: *Energy Efficient Heterogeneous Multi-core Systems*

B.Eng. in Electrical Engineering

Harbin Institute of Technology, China, July 2008
Thesis: *Point-to-point Scalar Operand Networks for Clustered Superscalar Processor*

EXPERIENCE

Summer Intern **May. 2013–Aug. 2013**

Qualcomm, Multimedia Architecture Team (San Diego, CA)

- Bring up a heterogeneous system simulation platform containing CPU and GPU with shared memory space.
- Enable ARM and OpenCL support for running GPU applications on the simulation platform.
- Evaluate SVM efficiency and on-chip communication traffic caused by data transfer and coherence messages.

Academic Simulator Development

gem5-gpu: A heterogeneous CPU-GPU simulation infrastructure (https://gem5-gpu.cs.wisc.edu/wiki/**)**

- Contribute to support ARMv7 32-bit ISA.

Research Assistant in University of Minnesota, Twin Cities **Sep. 2009–present**

Memory Consistency for Heterogeneous Multicore Systems:

- Implement coherence protocols and memory consistency models in a heterogeneous simulation platform.
- Evaluate different coherence protocols and consistency models for CPU and GPU.
- Optimize on-chip communication efficiency.

Co-design of Computation and Communication for High-throughput Data-parallel Accelerators:

- Propose GPU thread scheduling mechanism, maximizing computation resource utilization.
- Propose on-chip communication strategy, maximizing DRAM bank-level parallelism and row-access locality.
- Energy and performance analysis for the proposed system.

Energy Efficient Time-Division Multiplexed (TDM) Hybrid-Switched NoC:

- Build a heterogeneous simulation platform that contains both CPU and GPU; as well as design a hybrid-switched network that supports both packet switching and TDM-based circuit switching.
- Perform energy and performance analysis for the proposed hybrid-switched NoC.
- RTL implementation of the proposed NoC.

Integrated Layout and Architectural Design for Multicore Platforms:

- Develop customized on-chip interconnection architectures that provide benefits for building high-performance and energy efficient multicore systems.
- Performance modeling and evaluation for the proposed architecture.

Parallelization of Single-Threaded Programs Using Speculative Slicing

- Design and evaluate slicing algorithms that can be implemented in multicore systems.
- Propose compiler algorithms that generate program dependent graphs and collects program runtime profile.
- Speculatively parallelize single thread programs using slicing algorithms based on dependent graph.

PUBLICATION

Conference Paper:

[1] **Jieming Yin**, Pingqiang Zhou, Sachin S. Sapatnekar, Antonia Zhai. *Energy-Efficient Time-Division Multiplexed Hybrid-Switched NoC for Heterogeneous Multicore Systems*. 28th IEEE International Parallel & Distributed Processing Symposium (IPDPS), Phoenix, USA, May 2014.

[2] **Jieming Yin**, Pingqiang Zhou, Anup P. Holey, Sachin S. Sapatnekar, Antonia Zhai. *Energy-Efficient Non-Minimal Path On-chip Interconnection Network for Heterogeneous Multicore Systems*. The International Symposium on Low Power Electronics and Design (ISLPED), Redondo Beach, USA, Aug. 2012.

[3] Pingqiang Zhou, **Jieming Yin**, Antonia Zhai, Sachin S. Sapatnekar. *NoC Frequency Scaling with Flexible-Pipeline Routers*. The International Symposium on Low Power Electronics and Design (ISLPED), Fukuoka, Japan, Aug. 2011.

[4] Bing Yang, Zhigang Mao, **Jieming Yin**, Xiao Chen. *A Point-to-Point Inter-Cluster Communication Network in Clustered Superscalar Processor*. IEEE The 9th International Conference on Solid-State and Integrated-Circuit Technology. Beijing, China, Oct. 2008.

Other Publication:

[1] (**Techical Report**) Pingqiang Zhou, **Jieming Yin**, Antonia Zhai, and Sachin S. Sapatnekar. *NoC Design and Performance Optimization*. SRC TECHCON, 2011.

[2] (**Poster**) *Energy-Efficient NoC Design for CMP System*. 15th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2010). Pittsburgh, PA, March, 2010.

COURSES TAKEN

Advanced Computer Architecture, Parallel Computer Organization, Operating Systems, Advanced Compiler Techniques, Advanced Algorithms and Data Structures, VLSI Design Lab

COMPUTER SKILLS

Programming Languages	C/C++ and SystemC; CUDA, OpenCL; Perl, Python; VerilogHDL; and assembly languages for x86, ARM, and SPARC.
Operating Systems	LINUX, UNIX, and Windows.
Tools	GEM5, Simics/GEMS, gpgpu-sim, and SimpleScalar Simulator; Cacti, McPAT, Wattch and Orion Power model; Pin Tools; Matlab, ModelSim.

VISA STATUS

F1 student visa