

# Jieming Yin

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## EDUCATION

### Ph.D in Computer Science

University of Minnesota, Twin Cities, 2009 – 2015

Thesis: *Time-Division-Multiplexing Based Hybrid-Switched NoC for Heterogeneous Multicore Systems*

Courses: Advanced Computer Architecture, Parallel Computer Organization, Operating Systems, Advanced Compiler Techniques, VLSI Design Labs, Advanced Algorithms and Data Structures

### B.Eng. in Electrical Engineering

Harbin Institute of Technology, China, 2004 - 2008

Thesis: *Point-to-point Scalar Operand Networks for Clustered Superscalar Processor*

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## COMPUTER SKILLS

Programming Languages	C/C++ and SystemC; CUDA, OpenCL; Perl, Python; VerilogHDL; and assembly languages for x86, and ARM.
Operating Systems	LINUX, UNIX, and Windows.
Tools/Simulators	gem5, gpgpu-sim, and SimpleScalar Simulator; Cacti, McPAT, Wattch and Orion Power model; Pin Tools; R, Matlab; ModelSim; SQL.

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## EXPERIENCE

### *Postdoc Researcher*

**Mar. 2015–Dec. 2016**

#### **AMD Research (Bellevue, WA)**

- SoC component integration: performance modeling and evaluation for in-package communication networks and memory networks; evaluate design trade-offs for various topologies and routing algorithms.
- Design novel communication architecture that guarantees quality-of-service.
- Build tools to visualize communication patterns and identify network bottlenecks.
- Optimize coherence protocols for exascale heterogeneous processor that contains both CPUs and GPUs.
- Port proxy-apps to the simulation infrastructure.

### *Summer Intern*

**May. 2013–Aug. 2013**

#### **Qualcomm, Multimedia Architecture Team (San Diego, CA)**

- Bring up a heterogeneous simulation platform containing CPU and GPU with shared memory space (SVM).
- Enable ARM and OpenCL support for running GPU applications on the simulation platform.
- Evaluate SVM efficiency and on-chip communication traffic caused by data transfer and coherence messages.

### *Academic Simulator Development*

**gem5-gpu: A heterogeneous CPU-GPU simulation infrastructure** (<https://gem5-gpu.cs.wisc.edu/wiki/>)

- Contribute to support ARMv7 32-bit ISA.

**Memory Consistency for Heterogeneous Multicore Systems:**

- Implement coherence protocols and memory consistency models in a heterogeneous simulation platform.
- Evaluate different coherence protocols and consistency models; optimize on-chip communication efficiency.

**Co-design of Computation and Communication for High-throughput Data-parallel Accelerators:**

- Propose GPU thread scheduling mechanism, maximizing computation resource utilization.
- Co-design on-chip interconnection network with processors, taking advantage of different traffic patterns.

**Energy Efficient Time-Division Multiplexed (TDM) Hybrid-Switched NoC:**

- Build a heterogeneous simulation platform that contains both CPU and GPU; as well as design a hybrid-switched network that supports both packet switching and TDM-based circuit switching.
- Perform energy and performance analysis for the proposed hybrid-switched NoC.
- RTL implementation of the proposed NoC.

**Integrated Layout and Architectural Design for Multicore Platforms:**

- Develop customized on-chip interconnection architectures that provide benefits for building high-performance and energy efficient multicore systems.
- Performance modeling and evaluation for the proposed architecture.

**Parallelization of Single-Threaded Programs Using Speculative Slicing**

- Design and evaluate program slicing algorithms that can be implemented in multicore systems.
- Propose compiler algorithms that generate program dependent graphs and collect program runtime profile.
- Speculatively parallelize single thread programs using slicing algorithms based on dependent graph.

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**PUBLICATION****Conference Paper:**

- [1] **Jieming Yin**, Onur Kayiran, Matthew Poremba, Natalie Enright Jerger, Gabriel H. Loh. *Efficient Synthetic Traffic Models for Large, Complex SoCs*. 22nd International Symposium on High Performance Computer Architecture (HPCA), Barcelona, Spain, March 2016.
- [2] **Jieming Yin**, Pingqiang Zhou, Sachin S. Sapatnekar, Antonia Zhai. *Energy-Efficient Time-Division Multiplexed Hybrid-Switched NoC for Heterogeneous Multicore Systems*. 28th IEEE International Parallel & Distributed Processing Symposium (IPDPS), Phoenix, USA, May 2014.
- [3] **Jieming Yin**, Pingqiang Zhou, Anup P. Holey, Sachin S. Sapatnekar, Antonia Zhai. *Energy-Efficient Non-Minimal Path On-chip Interconnection Network for Heterogeneous Multicore Systems*. The International Symposium on Low Power Electronics and Design (ISLPED), Redondo Beach, USA, Aug. 2012.
- [4] Pingqiang Zhou, **Jieming Yin**, Antonia Zhai, Sachin S. Sapatnekar. *NoC Frequency Scaling with Flexible-Pipeline Routers*. The International Symposium on Low Power Electronics and Design (ISLPED), Fukuoka, Japan, Aug. 2011.
- [5] Bing Yang, Zhigang Mao, **Jieming Yin**, Xiao Chen. *A Point-to-Point Inter-Cluster Communication Network in Clustered Superscalar Processor*. IEEE The 9th International Conference on Solid-State and Integrated-Circuit Technology. Beijing, China, Oct. 2008.

**Other Publication:**

- [1] **(Technical Report)** Pingqiang Zhou, **Jieming Yin**, Antonia Zhai, and Sachin S. Sapatnekar. *NoC Design and Performance Optimization*. SRC TECHCON, 2011.
- [2] **(Poster)** *Energy-Efficient NoC Design for CMP System*. 15<sup>th</sup> International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2010). Pittsburgh, PA, March, 2010.