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Energy Efficient NoC Design for CMP Systems

Pingqiang Zhou **Jieming Yin (Poster Presenter)** **Antonia Zhai** **Sachin S. Sapatnekar**

{zhoux205, sachin}@umn.edu {jyin, zhai}@cs.umn.edu

University of Minnesota, Twin Cities

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Background:

⇨ On-chip interconnection network must satisfy power constrains

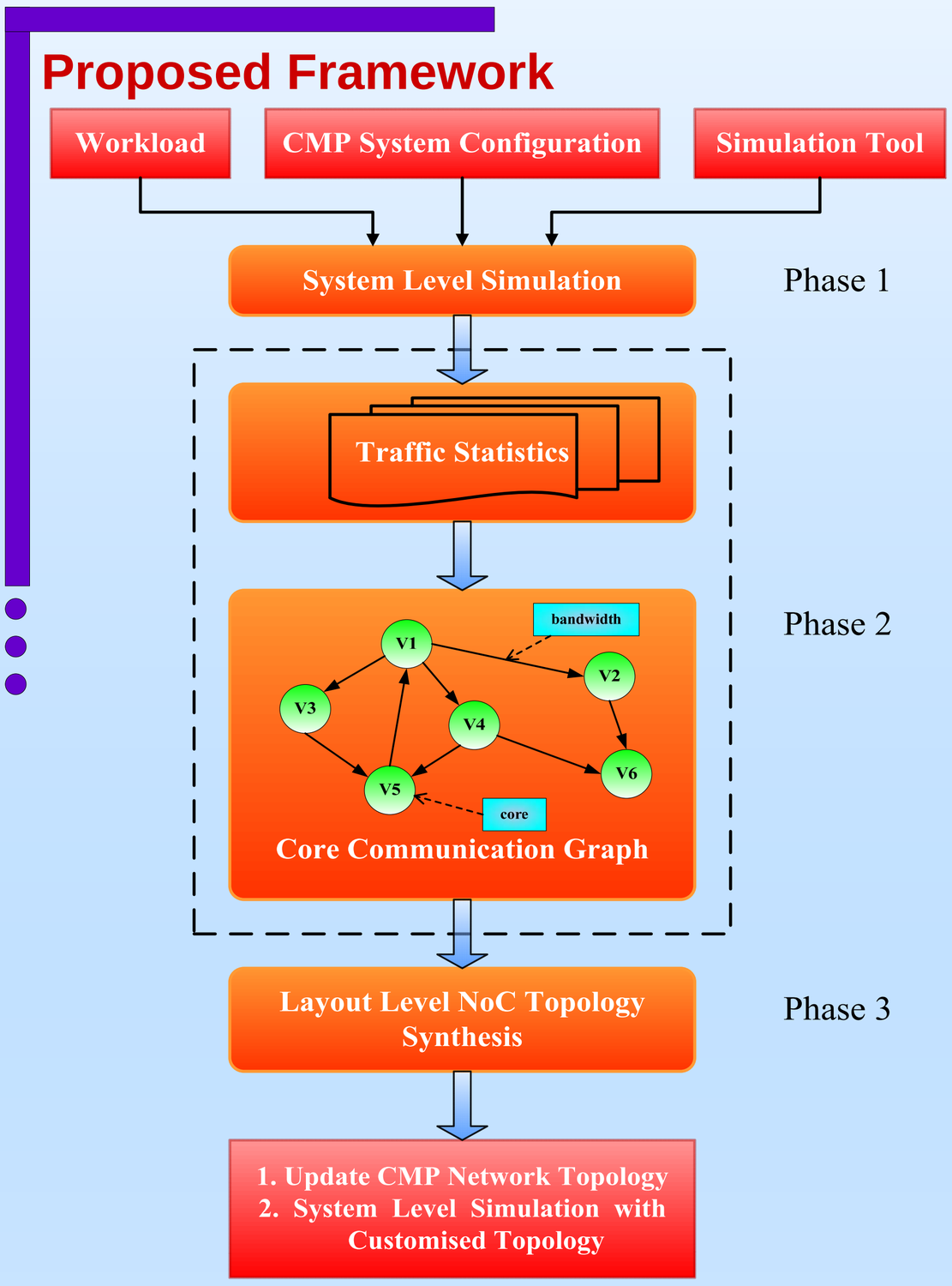
⇨ Router power

Number of ports & buffer size

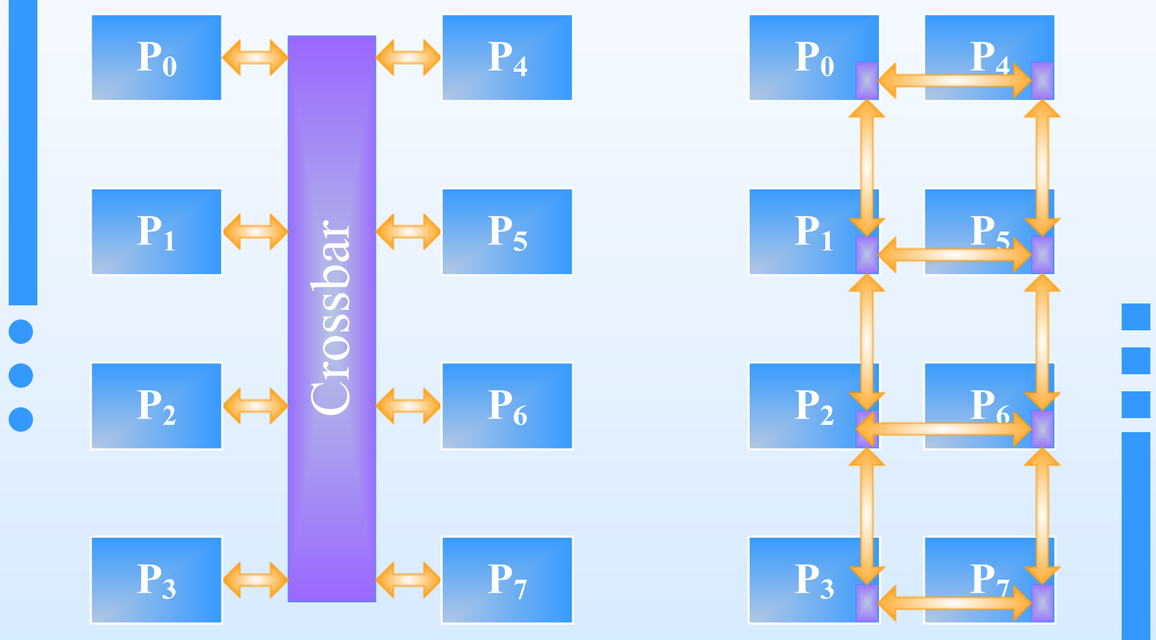
⇨ Link power

Average transmission hops & wire length

Proposed Framework



Traditional Approach



Crossbar

- Area consumption
- Energy inefficiency

Mesh

- More transmission hops

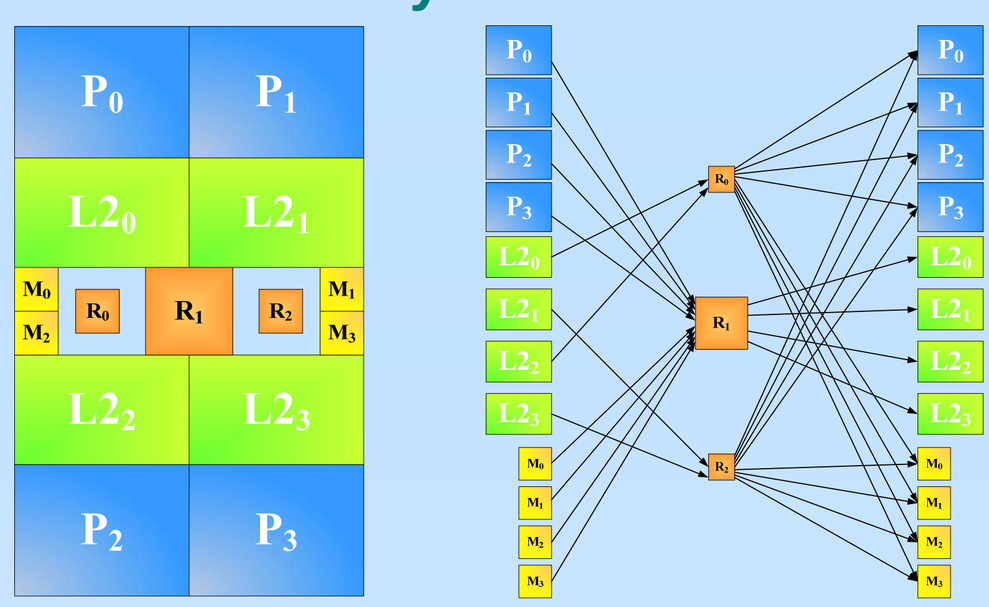
Hybrid:

⇨ Heterogeneous routers

Smaller switches compare to crossbar

Fewer hop count compare to mesh

Customized Layout

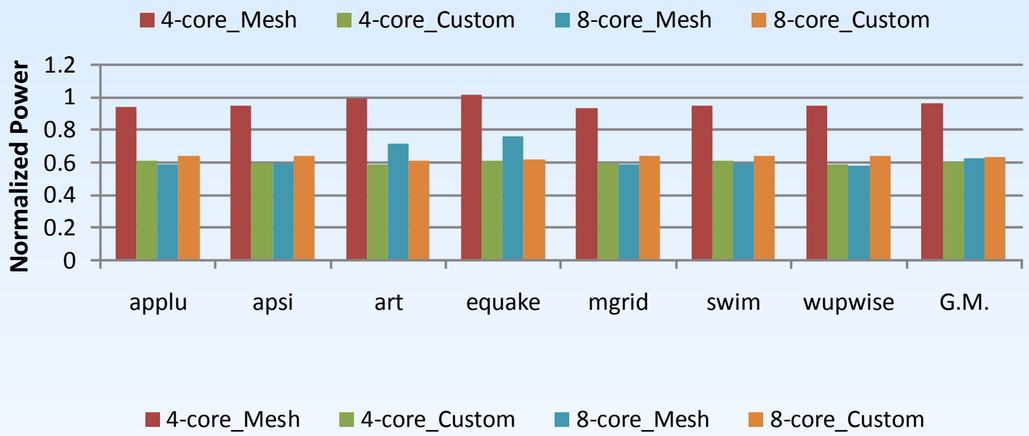


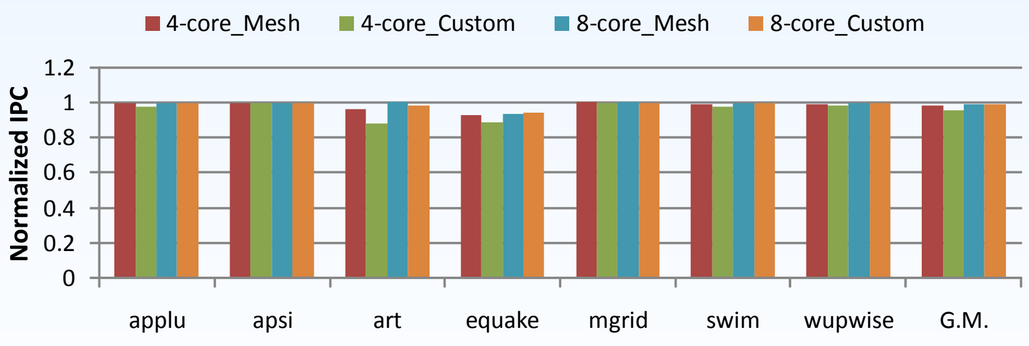
Experimental Results

⇨ Design trade-offs compare to crossbar

+ Power consumption decrease significantly (40%)

- IPC decrease slightly (5%)





⇨ Customized network is more energy efficient in most cases

⇨ For 4-core CMP system, a 32% average reduction in ED^2P

⇨ For 8-core CMP system, a 34% average reduction in ED^2P

⇨ Improved energy efficiency of on-chip interconnection network with heterogeneous routers

⇨ Also work for 16-core system