# Jie Yang

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## PERSONAL SUMMARY

Highly motivated, reliable and capable person with profound interdisciplinary research experience of integrated circuit, digital design, image processing and computer vision. Possess vast subject knowledge, confidence, communication skills and interest to educate others in a very friendly and comprehensive manners. Currently looking for a suitable academic position to attest my teaching skills and broaden my experience further.

## EDUCATION

Ph.D. Microelectronics, University of Chinese Academy of Sciences, Beijing, 2015
Dissertation: *Design of Vision Chip Based On Hierarchical Heterogeneous Parallel Processing Architecture*
Supervisor: Prof. Nanjian Wu
Committee: Zhihua Wang (chair), Jie Chen, Yuepeng Yan, Haigang Yang,Huaxiang Lu

B.S. Electronic Science and Technology, Tianjin University, 2010

## ACADEMIC APPOINTMENTS

2015– University of Calgary, Calgary
Postdoctoral Scholar, Integrated Intelligent Sensing Lab, Schulich School of Engineering
Supervisor: Prof. Orly Yadid-Pecht, ***FIEEE, FSPIE, FAIMBE***

## RESEARCH/TEACHING INTERESTS

Very large scale integrated (VLSI) circuit design

Computer vision, Machine Learning

VLSI architecture for computer vision and machine learning

## INTERNATIONAL PATENTS

2018 O. Yadid-Pecht, **J. Yang**, "NEURAL NETWORK TRAINED SYSTEM FOR PRODUCING LOW DYNAMIC RANGE IMAGES FROM WIDE DYNAMIC RANGE IMAGES." *Provisional patent filled September, 2018.*

2017 O. Yadid-Pecht, **J. Yang**, U. Shahnovich, and A. Horé, "METHOD OF PRESENTING WIDE DYNAMIC RANGE IMAGES AND A SYSTEM EMPLOYING SAME." *PCT/CA2017/050842, Filed July 11, 2017.*

## PUBLICATIONS

### Peer-Reviewed Journal Articles

2018 **J. Yang**, U. Shahnovich, and O. Yadid-Pecht, "Mantissa-exponent based Tone Mapping for Wide Dynamic Range Image Sensors," accepted at *IEEE Transactions on Circuits and System II: Express Briefs*.

2018 **J. Yang**, A. Horé and O. Yadid-Pecht, "Local tone mapping algorithm and hardware implementation," *Electronics Letters*, vol. 54, no. 9, pp. 560-562, 5 May 2018.

2018 **J. Yang**, Y. Yang, Z. Chen, L. Liu, J. Liu, and N. Wu, "A Heterogeneous Parallel Processor for High-Speed Vision Chip," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 28, no. 3, pp. 746-758, March 2018.

2014 **J. Yang**, C. Shi, L. Liu, J. Liu, and N. Wu, "Pixel-parallel feature detection on vision chip," *Electronics Letters*, vol. 50, no. 24, pp. 1839-1841, 20 December 2014.

2014 **J. Yang**, C. Shi, L. Liu, and N. Wu, "Heterogeneous vision chip and LBP-based algorithm for high-speed tracking," *Electronics Letters*, vol. 50, no. 6, pp. 438-439, 13 March 2014.

2017 Y. Yang, **J. Yang**, L. Liu, and N. Wu, "High-Speed Target Tracking System Based on a Hierarchical Parallel Vision Processor and Gray-Level LBP Algorithm," *IEEE Transactions on Systems, Man, and Cybernetics: Systems*, vol. 47, no. 6, pp. 950-964, June 2017.

2017 V. Nshunguyimfura, **J. Yang**, L. Liu, and N. Wu, "Property-driven functional verification technique for high-speed vision system-on-chip processor," *Japanese Journal of Applied Physics*, vol. 56, no. 4s, pp. 4CF15, March 2017.

2016 Y. Yang, **J. Yang**, Z. Zhang, L. Liu, and N. Wu, "High-speed visual target tracking with mixed rotation invariant description and skipping searching," *Science China Information Sciences*, vol. 60, no. 6, Dec. 2016.

2016 Z. Chen, **J. Yang**, C. Shi, Q. Qin, L. Liu, and N. Wu, "High speed vision processor with reconfigurable processing element array based on full-custom distributed memory," *Japanese Journal of Applied Physics*, vol. 55, no. 4S, pp. 04EF08, 16 March 2016

2016 Y. Yang, **J. Yang**, Z. Zhang, L. Liu, and N. Wu, "High-speed visual tracking with mixed rotation invariant description," *Electronics Letters*, vol. 52, no. 7, pp. 511-513, 31 March 2016

2014 C. Shi, **J. Yang**, Y. Han, Z. Cao, Q. Qin, L. Liu, N. Wu, and Z. Wang, "A 1000 fps Vision Chip Based on a Dynamically Reconfigurable Hybrid Architecture Comprising a PE Array Processor and Self-Organizing Map Neu-ral Network," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 9, pp. 2067-2082, Sept. 2014.

2014 C. Shi, **J. Yang**, N. Wu, and Z. Wang, "A high speed multi-level-parallel array processor for vision chips," *Science China Information Sciences*, vol. 57, no. 6, pp. 1-12, Jun. 2014.

2017 Z. Liu, L. Liu, **J. Yang**, and N. Wu, "A CMOS fully integrated 860-GHz terahertz sensor," *IEEE Transactions on Terahertz Science and Technology*, vol. 7, no. 4, pp. 455-465, July. 2017.

2014 C. Shi, Z. Chen, **J. Yang**, N. Wu, and Z. Wang, "A compact PE memory for vision chips," *Journal of Semiconductors*, vol. 35, no. 9, pp. 095002, 2014.

**Journal Article Manuscripts Under Review**

2018 **J. Yang**, U. Shahnovich, and O. Yadid-Pecht, "Wide Dynamic Range Image Tone Mapping Based on Multi-scale His-togram Synthesis," Major reversion and resubmit at *IEEE Transactions on Image Processing*.

2018 **J. Yang**, C. Shi, J. Liu, and N. Wu, "Implementing Pixel-parallel Image Processing On 1D PE Array," Revise and resubmit at *IEEE Transactions on Circuits and System II: Express Briefs*.

2018 Z. Zhang, H. Li, Q. Luo, **J. Yang**, W. Zhu, L. Liu, J. Liu, and N. Wu, "High-Speed Ship Detection System Based on Local-Feature-and-CNN Algorithm and Hierarchical Parallel Vision Processor," Under review at *IEEE Transactions on Circuits and System II: Express Briefs*.

**Peer-Reviewed Conference Proceedings**

2018 **J. Yang**, D. McDonald, U. Shahnovich, and O. Yadid-Pecht, "Mobile GPU implementation of wide dynamic range image compression based on multi-scale histogram synthesis," Electronics Imaging 2018. Burlingame, California

2017 **J. Yang**, A. Horè, U. Shahnovich and O. Yadid-Pecht, "Multi-Scale histogram tone mapping algorithm for display of wide dynamic range images," International Workshop on Computational Advances in Multi-Sensor Adaptive Processing, Curacao, Curacao

2017 **J. Yang**, A. Horé, U. Shahnovich, K. Lai, S. N. Yanushkevich and O. Yadid-Pecht, "Multi-Scale histogram tone mapping algorithm enables better object detection in wide dynamic range images," IEEE International Conference on Advanced Video and Signal Based Surveillance, Lecce, Italy 2017

2013 **J. Yang**, C. Shi, Z. Cao, Y. Han, L. Liu and N. Wu, "Smart image sensing system," IEEE International Conference on Sensors, Balti-more, MD, 2013

2017 H. Zheng **J. Yang**, and J. Chen "A performance evaluation method for infrared tracker," International Conference on Image and Vision Computing, Christchurch, New Zealand 2017.

2015 Z. Zhang, **J. Yang**, H. Li, L. Liu, J. Liu, and N. Wu, "High-speed object detection based on a hierarchical parallel vision chip ," IEEE 11th International Conference on ASIC, Chengdu, China 2015

2014 C. Shi, **J. Yang**, Y. Han, Z. Cao, Q. Qin, L. Liu, N. Wu and Z. Wang, "A 1000fps vision chip based on a dynamically reconfigurable hybrid architecture comprising a PE array and self-organizing map neural net-work," IEEE International Solid-State Circuits Conference Digest of Technical Papers, San Fran-cisco, CA, 2014, pp. 128-129.

2013 Z. Chen, **J. Yang**, C. Shi, and N. Wu, "A novel architecture of local memory for programmable SIMD vision chip," IEEE 10th International Conference on ASIC ,Shenzhen, China 2013

2015 Z. Liu, L. Liu, **J. Yang**, and N. Wu, "A fully-integrated 860-GHz CMOS terahertz sensor," IEEE Asian Solid-State Circuits Conference, Xiamen, China 2015

2015 H. Li, Z. Zhang, **J. Yang**, L. Liu, and N. Wu, "A novel vision chip architecture for image recognition based on convolutional neural network," IEEE 11th International Conference

on ASIC, Chengdu, China 2015

**Manuscripts in Preparation**

2018 **J. Yang**, M. Lin, D. McDonald, U. Shahnovich, and Orly Yadid-Pecht, "Mobile-end Implementation of Integral Image and Integral Histogram based Tone Mapping," Target: *IEEE Transactions on Industrial Informatics*, Fall 2018.

2018 **J. Yang**, H. Li, Z. Zhang, L. Liu and N. Wu, "Hierarchical Heterogeneous Processor for Vision Chip," Target: *IEEE Transactions on Circuits and Systems for Video Technology* , Fall 2018.

2018 **J. Yang**, M. Lin, U. Shahnovich and Orly Yadid-Pecht, "Deep Laplacian Decomposition for High Dynamic Range Tone mapping" Target: *Conference on Computer Vision and Pattern Recognition 2019*, Fall 2018.

## TEACHING EXPERIENCE

**University of Calgary**

Integrated Micro and Nanotechnology Sensory System (fall '17)

Integrated Micro and Nanotechnology Sensory System (fall '16)

## PEER REVIEWER

*Israel Science Foundation*

*IEEE Transactions on Circuits and Systems for Video Technology*

*International Journal of Remote Sensing*

*International Journal of Innovative Computing and Applications*

*Future Generation Computer Systems*

*The Second International Conference on Physics, Mathematics and Statistics*

## WORK STYLE

Passionate for challenges and innovation

Quick learner for new knowledge and skills, adaptable to new environments

Independent and optimistic personality

Excellent team-worker and team-builder

## REFERENCES

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