A Fully-Integrated 860-GHz CMOS Terahertz Sensor

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***Abstract*—This paper proposes a fully-integrated 860-GHz terahertz wave sensor. The sensor integrates a terahertz detector and readout circuit in 180-nm standard CMOS process. The readout circuit consists of a low-noise instrumentation amplifier and a high-resolution ΔΣ-ADC. Transmissive imaging without source modulation (no lock-in technique required) is realized using the sensor. The detector consists of a novel on-chip grounded patch antenna, a source-feeding NMOS field effect transistor and matching networks. A quarter-wavelength microstrip transmission line is designed to connect the gate of the NMOS transistor to eliminate the influence of bonding wire and pad. The measured maximum voltage responsivity (R_v) and minimum noise equivalent power (NEP) of the detector at 860 GHz are 3.3 kV/W and 106 pW/Hz$^{1/2}$, respectively. The measured readout circuit noise is 2.03 μVrms.**

Keywords—CMOS; terahertz imaging; continuous wave; terahertz sensor; terahertz detector; readout circuit

I. INTRODUCTION

Considerable attention has been attracted to the terahertz frequency range (0.3-3THz) in recent years. Because terahertz radiation can penetrate different kinds of materials such as plastic, wood or paper sheets, terahertz wave imaging can be widely applied into a lot of potential applications areas. The lack of low-cost and intensively integrated detector was once a major obstacle to build low-cost, small volume and video rate terahertz imaging systems. Because of the advantages of low cost, high yield and easy integration, CMOS technology is becoming an alternative to other technologies. Terahertz detector using FET is based on plasma wave theory proposed by Dyakonov and Shur [1] which allows detection of terahertz radiations far beyond the FET devices characteristic frequency (f_T). The first silicon FET detector was demonstrated by Knap et al [2]. Then CMOS based multi-pixel terahertz detector array with an integrated silicon lens was reported by Hadi and Sherry et al. in 2011 [3]. The array can sense radiation with frequency ranging from 0.6 to 1 THz. Detector can also be implemented by dedicate designed Schottky-Diode under CMOS process. An implementation under 130-nm digital CMOS has been reported which operated well under illumination of 280 GHz [4]. But, most of CMOS terahertz sensors today have to use lock-in measurement techniques through raster scanning to acquire images. In 2012, a 1k-pixel terahertz video camera chip was presented [5], which can capture terahertz video-frames without lock-in measurement techniques. However, it did not integrate on-chip ADC. In the future a fully integrated terahertz image sensor would be a very wise approach to realize video-rate terahertz cameras.

This paper proposes a fully-integrated CMOS terahertz sensor in 180 nm standard CMOS process. The sensor consists of a terahertz detector, a low-noise instrumentation amplifier and a high-resolution ΔΣ-ADC, which can realize raster scanning image with continuous-wave illumination. A novel on-chip grounded patch antenna is designed to couple a source-feeding NMOS via a matching network. To eliminate the influence of pad and bonding wire, a quarter-wavelength microstrip transmission line is proposed.

II. SENSOR ARCHITECTURE

The block diagram of the terahertz sensor is shown in Fig. 1. The sensor integrates a terahertz detector, a low-noise instrumentation amplifier and a high-resolution ΔΣ-ADC. The detector consists of a novel on-chip grounded patch antenna, a source-feeding NMOS field effect transistor and matching networks MN and TL. The terahertz radiation wave is received by the grounded patch antenna and then coupled to the source terminal of the NMOS transistor. The matching network MN is designed to improve power transfer efficiency between antenna and NMOS transistor. The matching network TL is an open quarter-wavelength microstrip transmission line. It is used to eliminate the influence of bonding wire and pad on the input impedance of the NMOS transistor. The detector outputs a dc voltage signal that is proportional to the detected terahertz radiation power [6]. The rectifying dc voltage signal is amplified by an instrumentation amplifier. Finally, the ADC converts the amplifier's output signal into digital signal. The switch at the detector's output is a reserved interface used to isolate the influence of the readout circuit when measuring the performance of the detector.

Due to low terahertz source power, the output signal of the detector is also weak and hence a high-resolution and low-noise readout circuit is required. Since the detector

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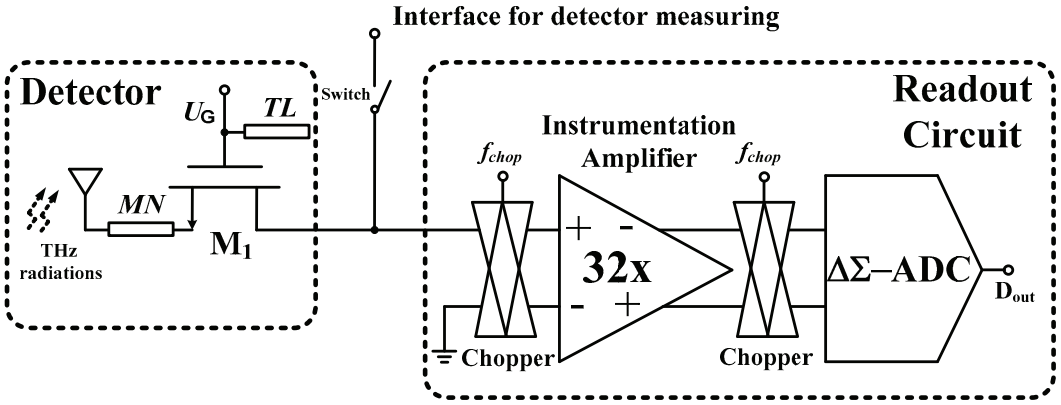

Fig. 1. Block diagram of the proposed terahertz sensor

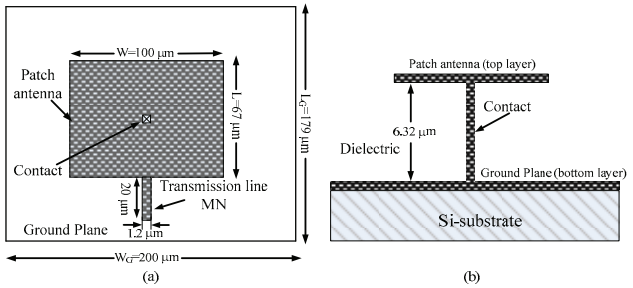

Fig. 2. Structure of grounded patch antenna

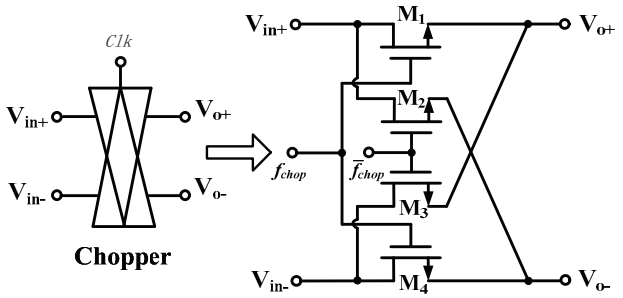

Fig. 3. Schematic of the chopper

outputs a dc voltage signal, the *1/f* noise of the readout circuit must be reduced. The instrumentation amplifier utilizes chopping technique to reduce offset and *1/f* noise of the amplifier. The ΔΣ-ADC is selected because of its multiple advantages such as low noise, high accuracy, matching-free property and low requirements for operational amplifier. The design of the block circuits is described in the following sections.

III. Detector Design

The proposed source-driven detector consists of an NMOS field effect transistor with non-biased channel as rectifying element, an integrated on-chip grounded patch antenna, a matching network MN and an open quarter-wavelength microstrip transmission line TL. The NMOS transistor has a gate length of 0.18 μm and a gate width of 0.24 μm, which is the minimum size of the process.

A. Grounded Patch Antenna

The structure of the grounded patch antenna is shown in Fig. 2. The patch has a length of 67 μm and a width of 100 μm. It is formed by the top metal layer in the process and the bottom metal layer is utilized to form ground plane. The thickness of dielectric insulator between patch and ground plane is 6.32 μm. A contact connecting the top metal and bottom metal at the center of the antenna is designed to provide a dc ground to the source of the NMOS. The contact does not degrade the electromagnetic performance of the antenna since the center of antenna is zero-field intensity (H-plane). Compared to [3], this structure doesn't require an extra source bias through the antenna, thus reducing system-level complexity for future array implementation. The simulated antenna directivity is 5.3 dBi at 860 GHz. The effective area A_{eff} of the antenna is 0.0329 mm^2, which can be calculated as [7]

$$A_{eff} = D\lambda^2 / 4\pi \quad (1)$$

where D is directivity of the antenna and λ is electromagnetic wave length.

B. Matching Networks

To improve the power transfer efficiency, we add a microstrip transmission line MN between antenna and NMOS transistor as the matching network, as shown in Fig. 1. The transmission line has a length of 20 μm and a width of 1.2 μm. It is implemented in the top metal layer and the bottom metal layer is utilized to form ground plane.

Since the gate of NMOS should be biased to a constant potential, conventional design employs off-chip biasing which connects to the gate directly through the bonding wire. Considering the influence of the parasitic capacitance and inductance of pad and bondwire on the input impedance of the NMOS transistor, we propose an open quarter-wavelength microstrip transmission line connected to the gate of the NMOS, as shown in Fig. 1, which forms a ground point for terahertz radiation and has no impact on gate dc bias. The quarter-wavelength microstrip transmission line has a length of 29 μm and a width of 1.2 μm. It is also implemented in the top metal layer and the bottom metal layer serves as the ground plane.

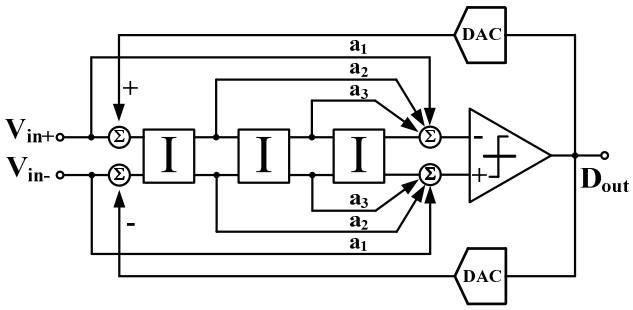

Fig. 4. Block diagram of the ΔΣ-ADC

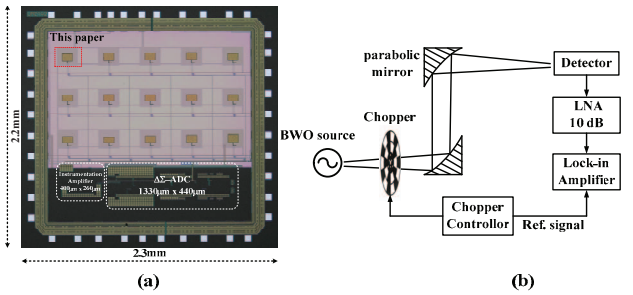

Fig. 5. (a) Chip microphotograph and (b) Measurement setup for characterizing the detector

IV. Readout Circuit

The readout circuit consists of a low-noise instrumentation amplifier and a high-resolution ΔΣ-ADC.

A. Instrumentation Amplifier

The instrumentation amplifier is a two-stage differential amplifier with chopper to reduce offset and *1/f* noise. One input of the amplifier is connected to the detector output and the other is grounded. Fig. 3 shows the schematic of the chopper which driven by a 125 kHz clock, f_{chop}. The simulated closed-loop gain of the instrumentation amplifier is 32.

B. Delta-Sigma ADC

The block diagram of the ΔΣ-ADC is shown in Fig. 4. It uses a third-order CIFF modulator structure [8]. The modulator output is captured by an external FPGA in which a digital decimation filter is implemented. Each integrator incorporates a two-stage cascode configuration operational amplifier of 120-dB dc gain. The first stage utilizes chopping technique to reduce offset and *1/f* noise. The sampling capacitor, sampling rate and oversampling rate of the ΔΣ-ADC are 4 pF, 500 kHz and 8192, respectively.

V. Measurement Results

Fig. 5 (a) shows the die photo of the 860 GHz CMOS terahertz sensors with various sizes of detectors for testing. The proposed detector is at the upper left, which has the best performance. The areas of the instrumentation amplifier and ΔΣ-ADC are 400 μm × 260 μm and 1330 μm × 440 μm, respectively.

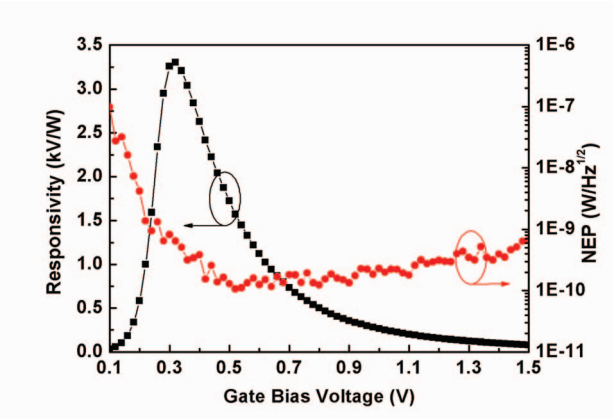

Fig. 6. Measured R_v and NEP as a function of gate bias voltage

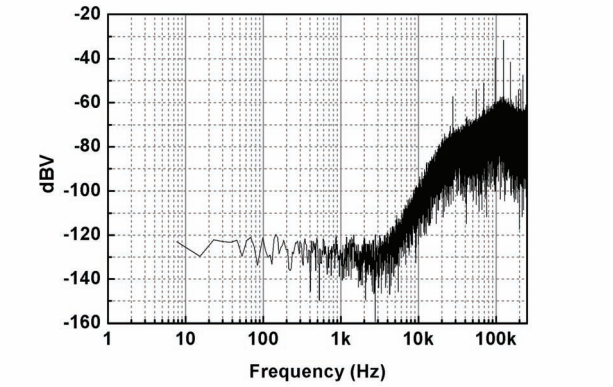

Fig. 7. Noise power spectral density of the readout circuit

The detector of the sensor is characterized by means of lock-in techniques. Fig. 5 (b) illustrates the measurement setup. The measured voltage responsivity versus gate bias voltage at 860 GHz is shown in Fig. 6. The peak responsivity is 3.3 kV/W when the gate bias voltage is 0.32 V. The measured noise equivalent power (NEP) under different gate-bias conditions at 177-Hz modulation frequency is also plotted in Fig. 6. The minimum NEP is 106 pW/Hz$^{1/2}$ when the gate bias voltage is 0.52 V. The gain of external amplifier is excluded from the test results.

Fig. 7 shows the measured noise power spectral density of the readout circuit. When the oversampling rate is 8192, the readout circuit noise is 2.03 μVrms.

Imaging at terahertz in most recent published works [3, 4, 9-11] is done by means of lock-in techniques which needs source modulation. This paper, however, demonstrates the raster-scanned image with continuous-wave illumination. Fig. 8 shows the block diagram of the terahertz imaging system used for transmission mode imaging. The ΔΣ-ADC oversampling rate is 8192. Fig. 9 shows a raster scanned image at 860 GHz of different tree leaves. The image clearly reflects the internal structure of the leaves. The performance comparison between this work and the published terahertz sensors is presented in Table I.

VI. CONCLUSIONS

A fully-integrated 860-GHz terahertz sensor which was implemented in 180-nm standard CMOS process has been presented. The sensor integrates a terahertz detector, a low-noise instrumentation amplifier and a high-resolution ΔΣ-ADC. It is designed to achieve terahertz image with continuous-wave illumination. The detector consists of a novel on-chip grounded patch antenna and an NMOS field effect transistor. A matching network is designed to improve power transfer efficiency. A quarter-wavelength microstrip transmission line is proposed to connect the gate of the NMOS to eliminate influence of pad and bonding wire. The detector achieves a voltage responsivity of 3.3 kV/W and an NEP of 106 pW/Hz$^{1/2}$ at 860 GHz under room temperature. The measured readout circuit noise is 2.03 μVrms. The terahertz sensor can successfully retrieve raster-scanned image with continuous-wave illumination. It indicates that the proposed sensor can be further used in multi-pixel array for terahertz imaging.

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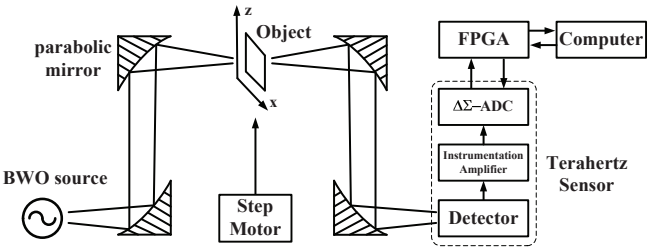

Fig. 8. Block diagram of the terahertz imaging system

Fig. 9. Measured image of leaves

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TABLE I. PERFORMANCE COMPARISON BETWEEN THE CMOS TERAHERTZ SENSORS

Technology	Freq. [THz]	Max R_v [V/W]	Min NEP [pW/Hz$^{1/2}$]	Image acquisition mode	Ref.
180 nm CMOS	0.86	3.3k	106	Integtated ADC	This work
65 nm CMOS	0.86	[1]140k	[1]100	External ADC	[5]
65 nm CMOS	1	800	66	Lock-in tecniques	[3]
65 nm SOI	0.65	1.1k	50	Lock-in tecniques	[9]
130 nm CMOS (SBD)	0.28	0.25k	33	Lock-in tecniques	[4]
180 nm CMOS	0.332	[2]632k	-	Lock-in tecniques	[10]
250nm CMOS	0.65	[3]80k	[3]300	Lock-in tecniques	[11]

[1]with integrated amplifier of 5 dB gain and si lens

[2]with integrated amplifier of 27 dB close-loop gain

[3]with integrated amplifier of 43 dB open-loop gain