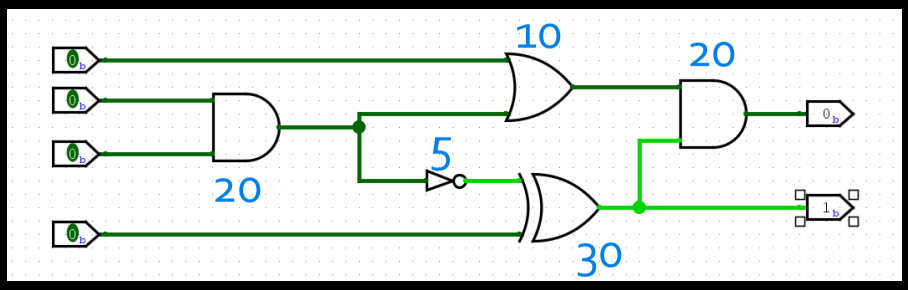
Week 5 Review

Max propagation delay

- This is the longest possible delay for a circuit.
- Slowest path from any input to any output.
  - In terms of total propagation delay, not path length or number of components on it.



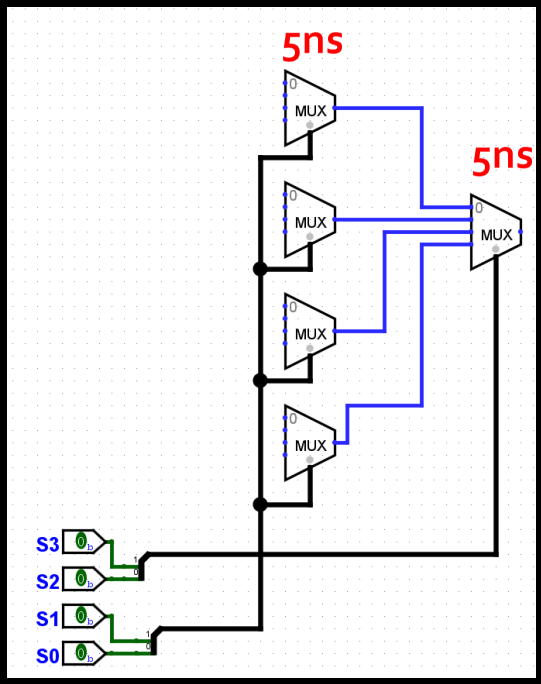
30

75

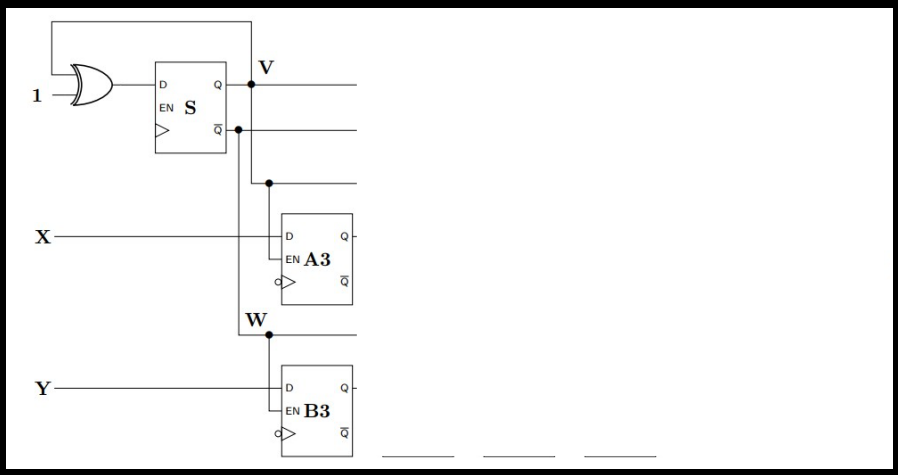
55

Practice Question 1

- Build a 16-to-1 mux from 4-to-1 muxes that have a maximum propagation delay of 5 nanoseconds
- It must finish within one clock cycle.
- What is the minimum safest clock cycle for our circuit?
- → 10ns

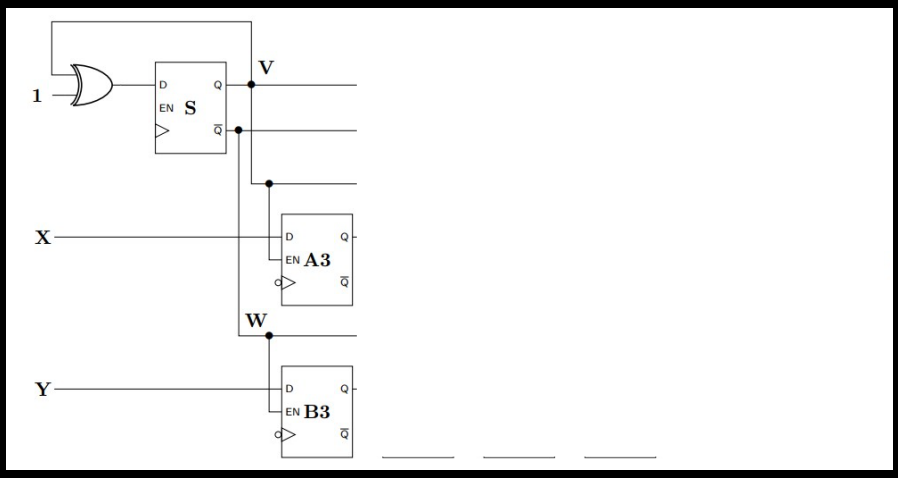


Practice Question 2



- The flip-flop S is triggered on the _____ edge of the clock, while the flip-flops A3, B3 are triggered on the _____ edge of the clock

Practice Question 2

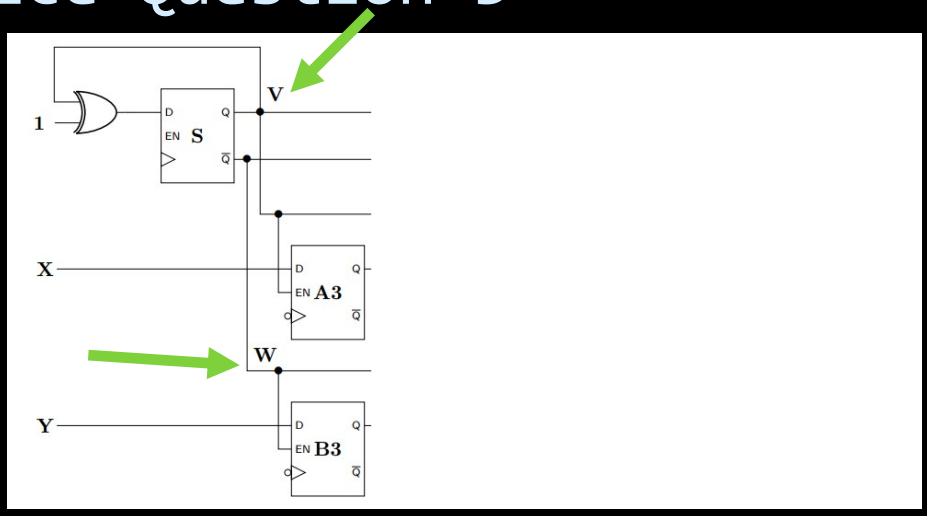


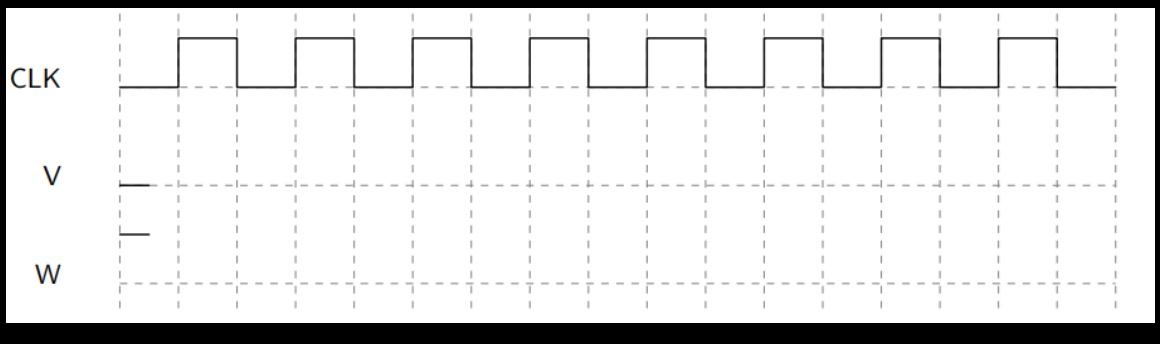
- The flip-flop S is triggered on the _rising_ edge of the clock, while the flip-flops A3, B3 are triggered on the _falling_ edge of the clock

Practice Question 3

Draw V and W given CLK.

Assume S is zero at the beginning.





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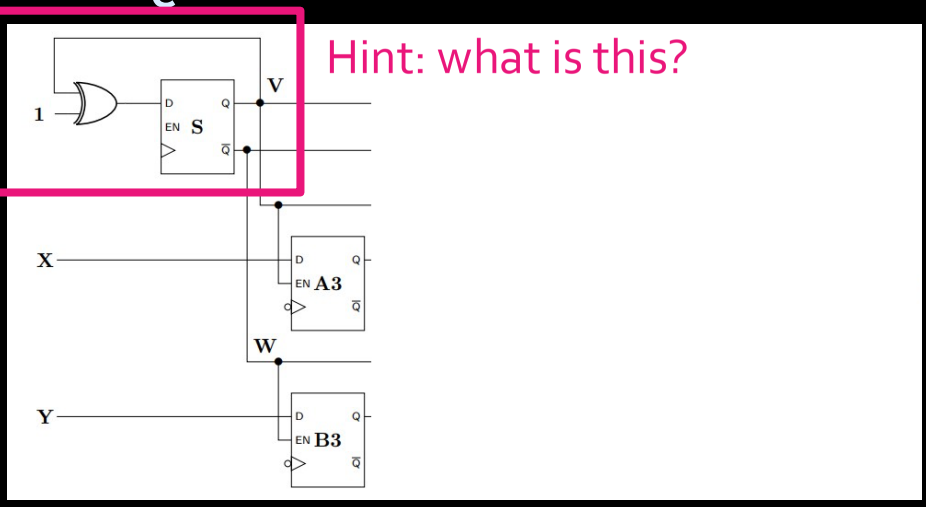
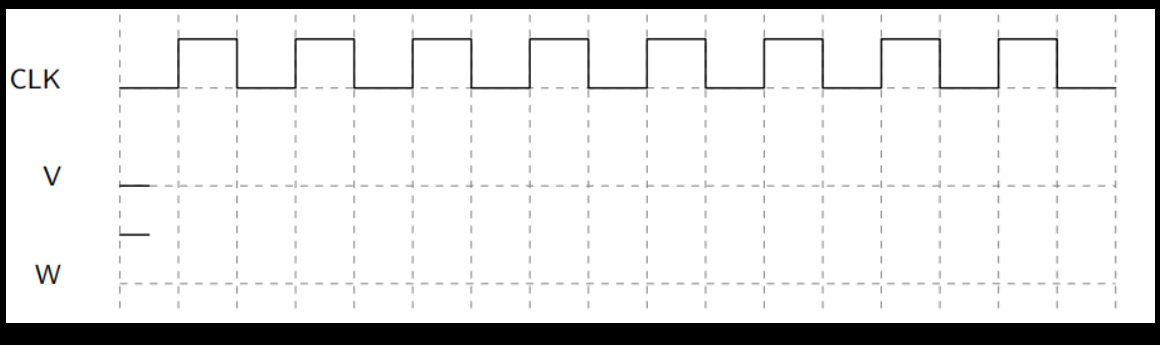


Hint: what is this?



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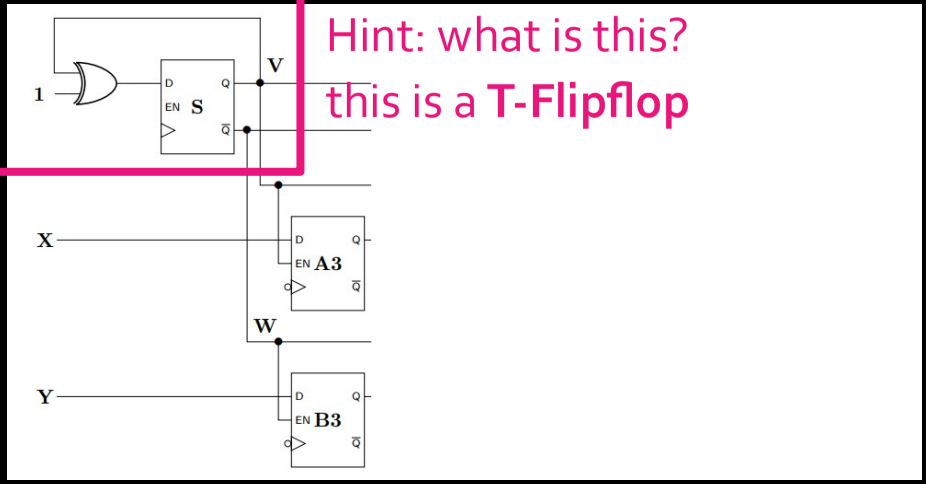
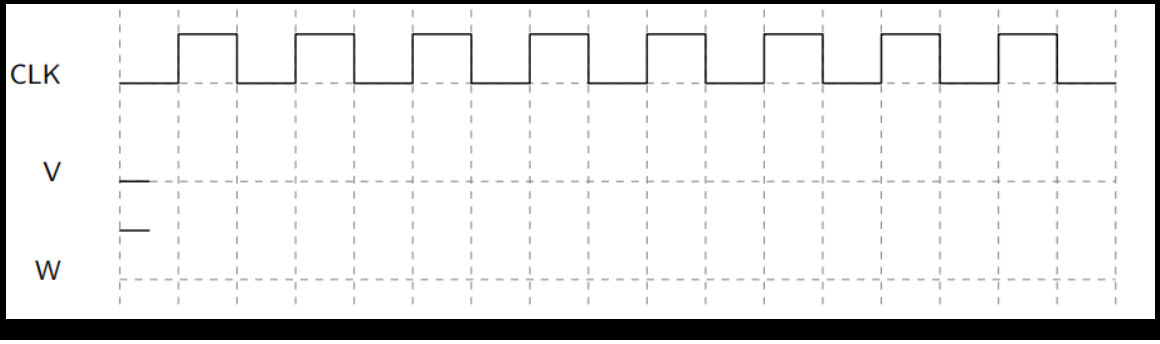


Hint: what is this?

this is a **T-Flipflop**



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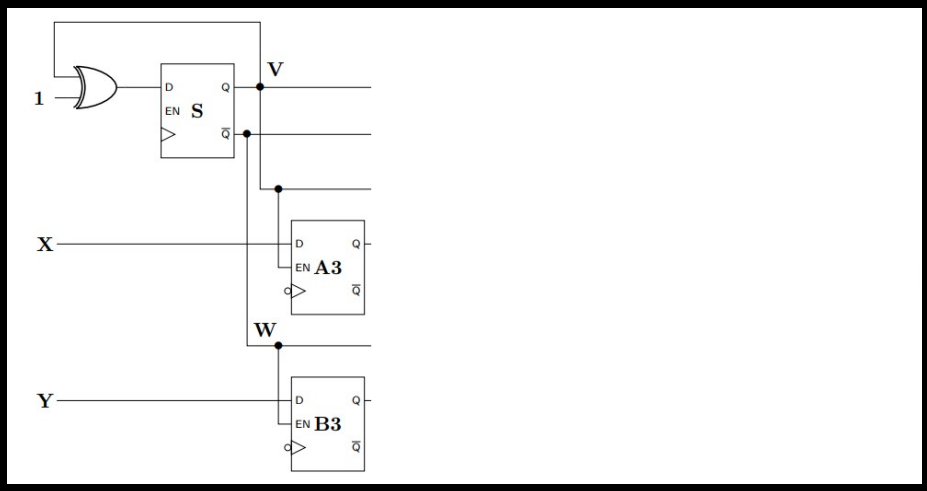
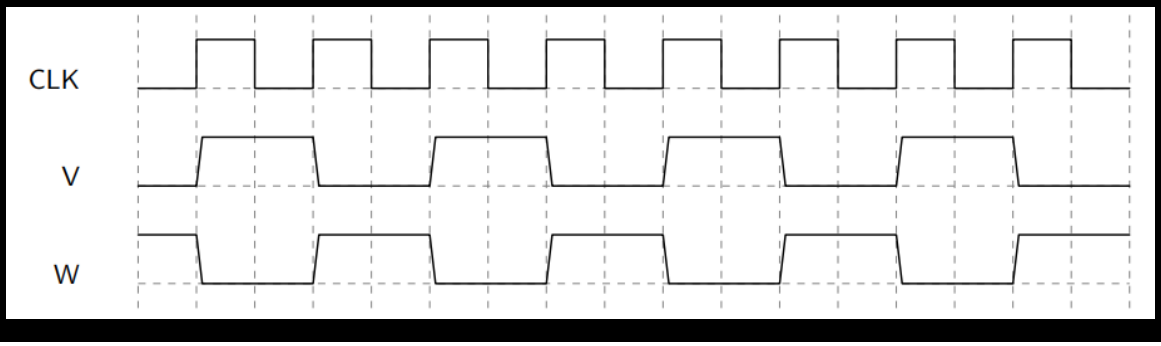
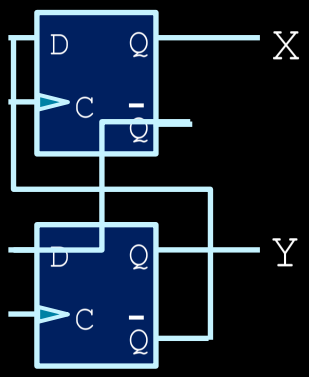




Practice Question 4

- Assuming the Q output of both flip-flops starts as low (X=0 Y=0).
- What will the values of X and Y be over the next few clock cycles?
  - (These are positive edge- triggered)



X

Y

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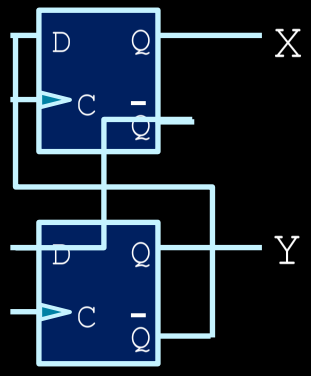
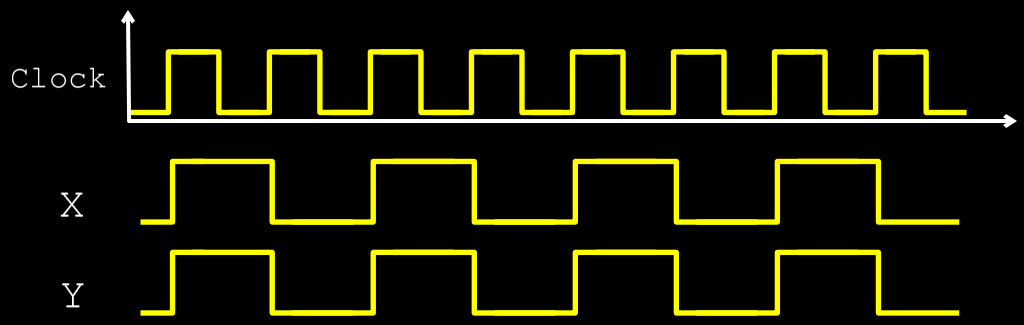
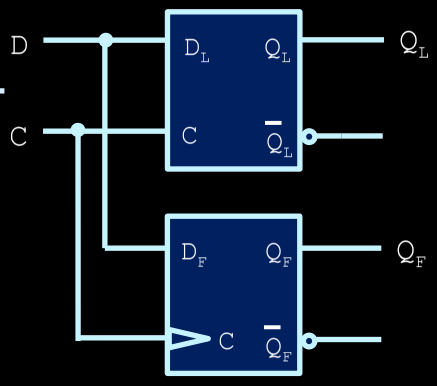
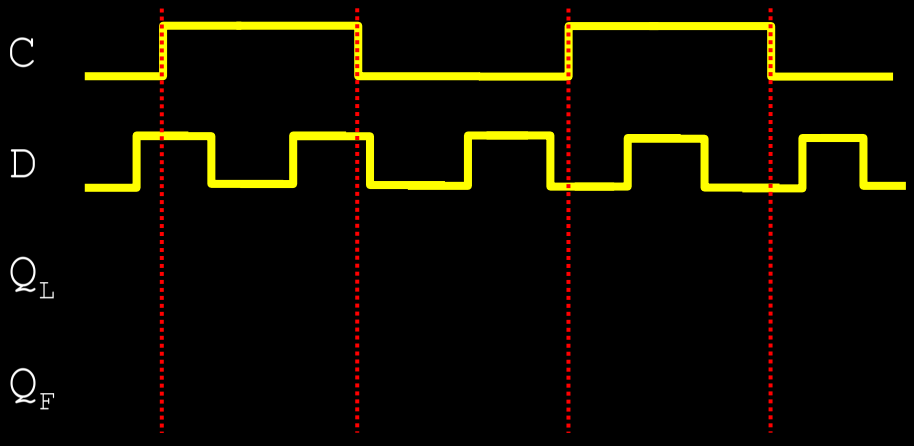




Practice Question 4

- Given the circuit on the right and the input waveform below, what will the outputs be on Q_L and Q_F?
  - Initial state for both is zero





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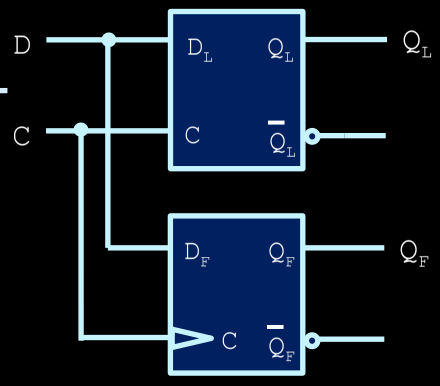

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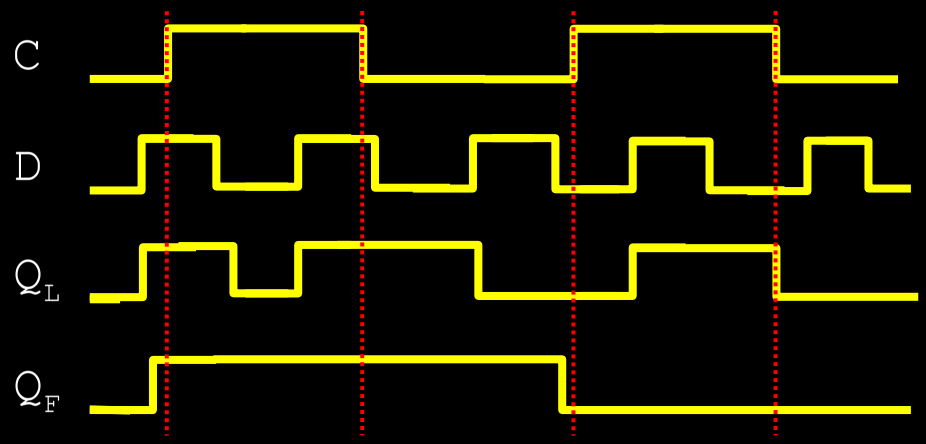
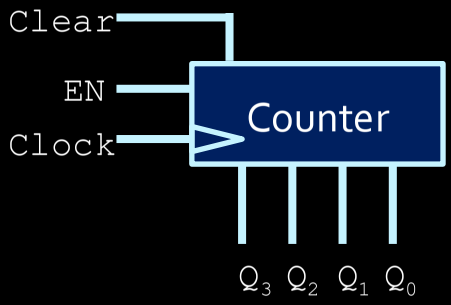


Question 5

- You have this counter:



- How do you make a signal Y that goes high after exactly 10 clock cycles?

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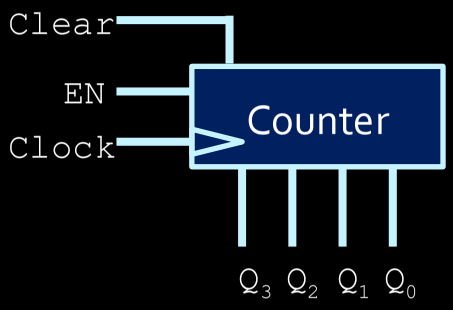

- How do you make a signal Y that goes high after exactly 10 clock cycles?
  - $Y = Q_3\overline{Q_2}Q_1\overline{Q_0}$

Question 6

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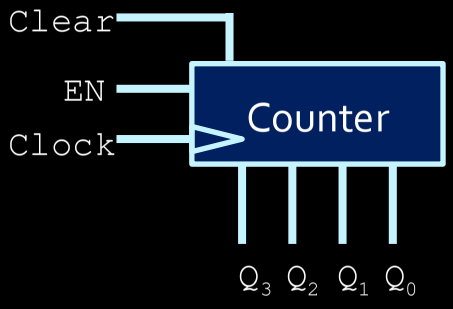

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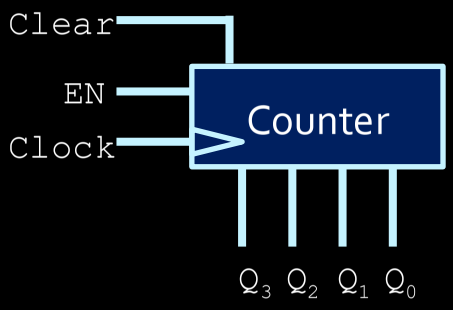

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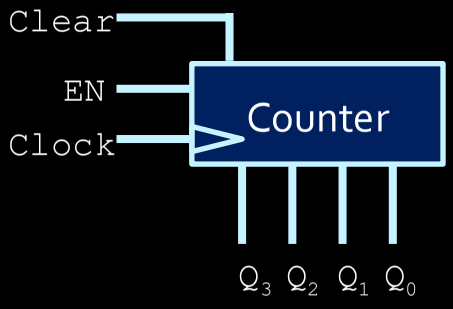

- How do you make a signal Y that goes high every 10 clock cycles?
  - $Y = Q_3\overline{Q_2}Q_1\overline{Q_0}$ ← is this good enough?
  - No! This Y goes high every 16 cycles!

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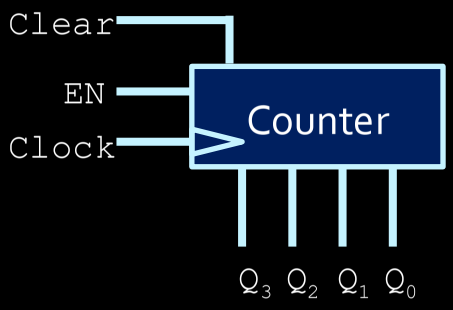

- How do you make a signal Y that goes high every 10 clock cycles?
  - $Y = Q_3\overline{Q_2}Q_1\overline{Q_0}$
  - Clear = Y ← set to zero after reaching 10!