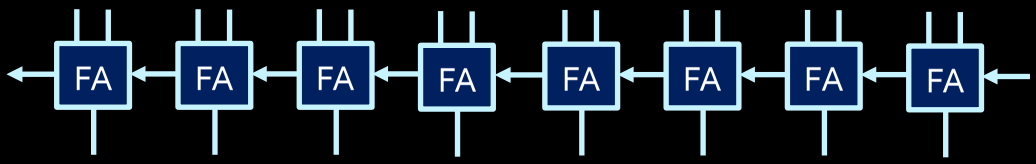
WEEK 4 REVIEW

Question #1

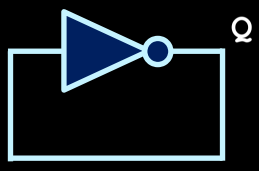
- Can we subtract numbers using only ripple carry adders?



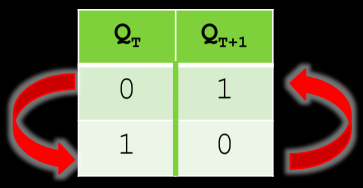
- No! we need additional gates
  - Two's complement is NOT(Y) +1
  - C_{in} gives us +1, but we still need to compute NOT(Y)

Question #2

- Is this circuit stable or does it oscillate?



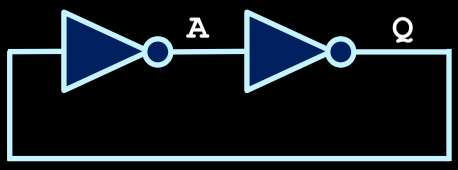
- It oscillates!



Q_T	Q_{T+1}
0	1
1	0

Question #3

- Is this circuit stable or does it oscillate?

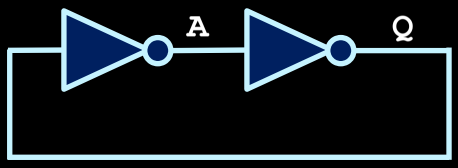


Q_T	A_T
0	1
1	0

A_T	Q_{T+1}
1	0
0	1

Question #3

- Is this circuit stable or does it oscillate?

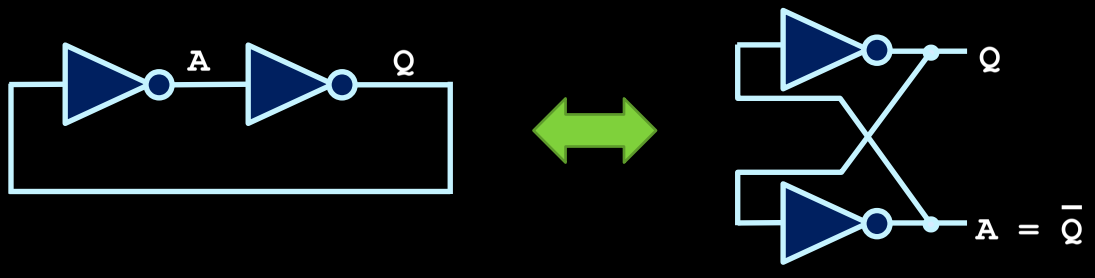


- It is stable!
  - Q=0 remains 0
  - Q=1 remains 1

Q_T	A_T
0	1
1	0

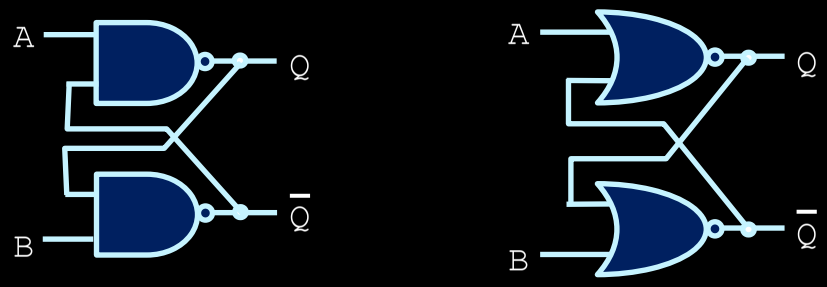
A_T	Q_{T+1}
1	0
0	1

Rearrange the circuit…



Latches

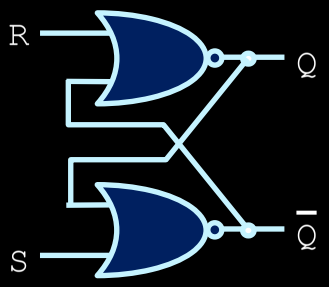
- We overcome oscillations by combining multiple NAND or NOR gates.



- These circuits are called latches.

Question #4

- Complete the truth table
  - Don't-care inputs allowed.
- And name the 4 possible S,R input combinations



S	R	Q_T	$\overline{Q}_T$	Q_{T+1}	$\overline{Q}_{T+1}$

← Hold

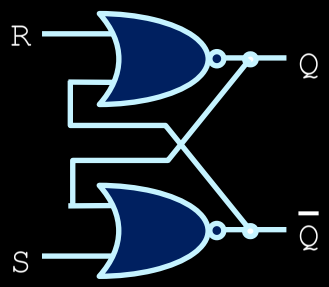
← Reset

← Set

← Forbidden

Question #4

- Complete the truth table
  - Don't-care inputs allowed.
- And name the 4 possible S,R input combinations

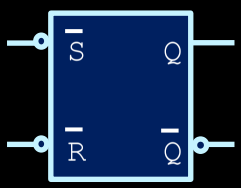


S	R	Q_T	$\overline{Q}_T$	Q_{T+1}	$\overline{Q}_{T+1}$	
0	0	0	1	0	1	← Hold
0	0	1	0	1	0	
0	1	X	X	0	1	← Reset
1	0	X	X	1	0	← Set
1	1	X	X	0	0	← Forbidden

Summary: S'R' and SR latches

$\overline{S}\overline{R}$-latch

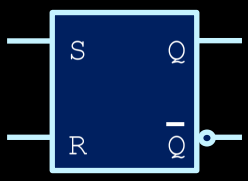
$\overline{S}$	$\overline{R}$	Q_T	$\overline{Q}_T$	Q_{T+1}	$\overline{Q}_{T+1}$	
0	0	X	X	1	1	Forbidden state
0	1	X	X	1	0	Set Q to 1
1	0	X	X	0	1	Reset Q to 0
1	1	0	1	0	1	Maintain Q
1	1	1	0	1	0	



"set" and "reset" cannot be both true!

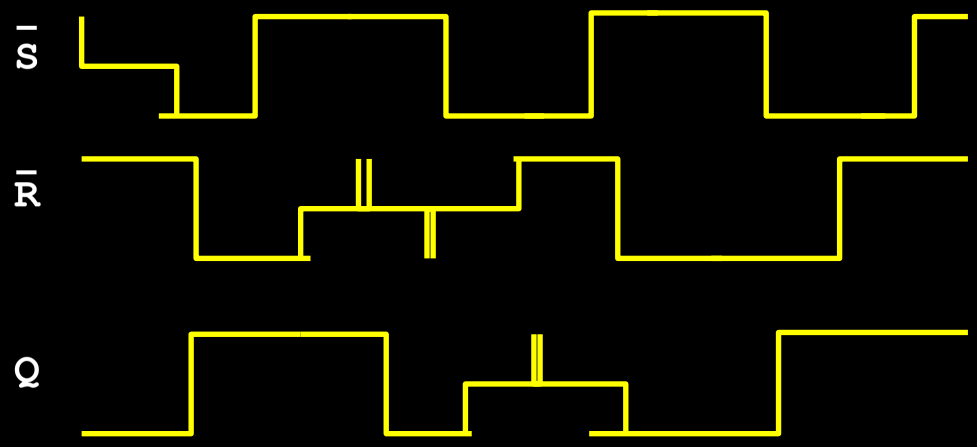
SR-latch

S	R	Q_T	$\overline{Q}_T$	Q_{T+1}	$\overline{Q}_{T+1}$	
0	0	0	1	0	1	Maintain Q
0	0	1	0	1	0	
0	1	X	X	0	1	Reset Q to 0
1	0	X	X	1	0	Set Q to 1
1	1	X	X	0	0	Forbidden state



Question #5

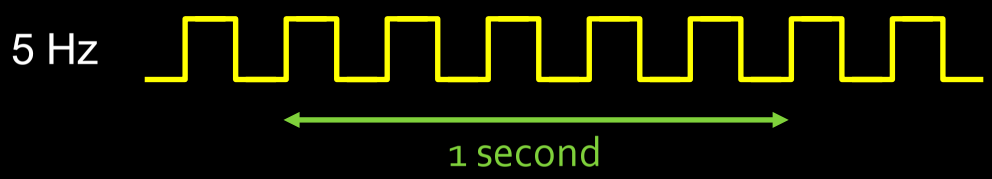
- Given the input waveforms, sketch the output Q of an $\bar{S}\bar{R}$ latch. Assume Q was zero initially.



Clocks

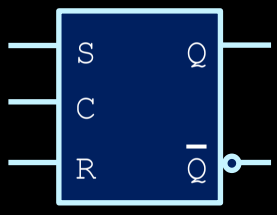
- A periodic signal that gives timing for our circuit

- Frequency = the number of pulses occur per second.



Clocked/Gated latches

- Add a new input C that acts like a "gate" over the inputs:
- If C=0 the latch ignores input
  - Maintains state.
- If C=1 the latch is "active"
  - Responds to input



Question #6

- What are the output values from Q and $\overline{Q}$ given the following inputs on S, R and C?

Time

S	R	C	Q	$\overline{Q}$
			?	?
0	0	1		
1	0	1		
1	0	0		
0	0	0		
0	1	0		
0	1	1		

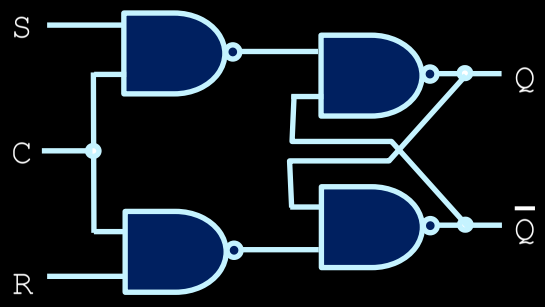
Question #6

- What are the output values from Q and $\overline{Q}$ given the following inputs on S, R and C?

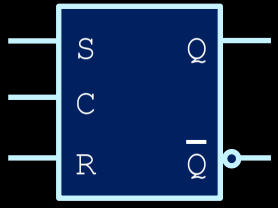
Time

S	R	C	Q	$\overline{Q}$
			?	?
0	0	1	?	?
1	0	1	1	0
1	0	0	1	0
0	0	0	1	0
0	1	0	1	0
0	1	1	0	1

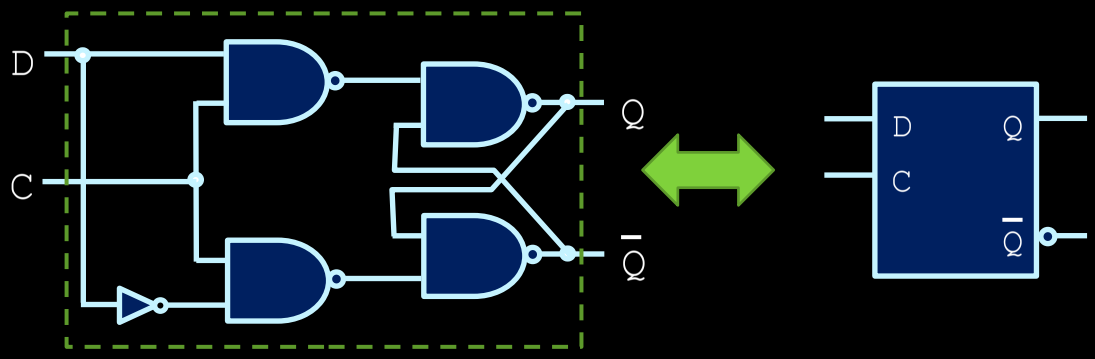
Clocked SR latch behaviour



C	S	R	Q_{T+1}	Result
0	X	X	Q_T	hold
1	0	0	Q_T	hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	?	undefined



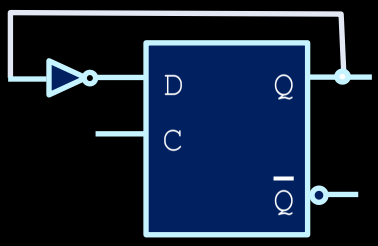
D latch

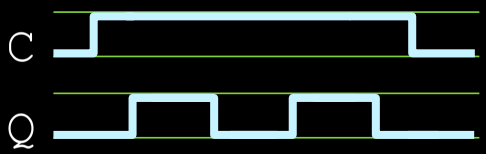


- This design is good!
  - Easy to store a bit: just set D to what you want to store.
  - Can maintain state as long as C is low
  - No weird forbidden inputs.

D latch is transparent

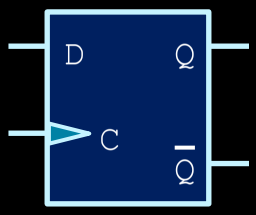
- Any changes to its inputs are visible to the output when control signal (Clock) is 1.
  - Output keeps toggling back and forth.
- We want output to change exactly once per cycle.



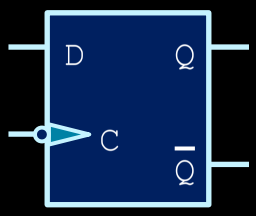


Flip-flops

- Positive edge: triggered on rising edge of the clock

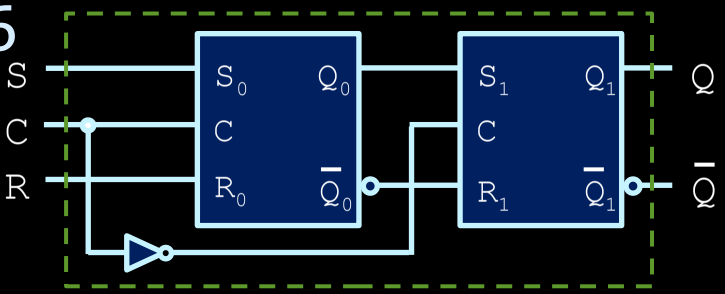


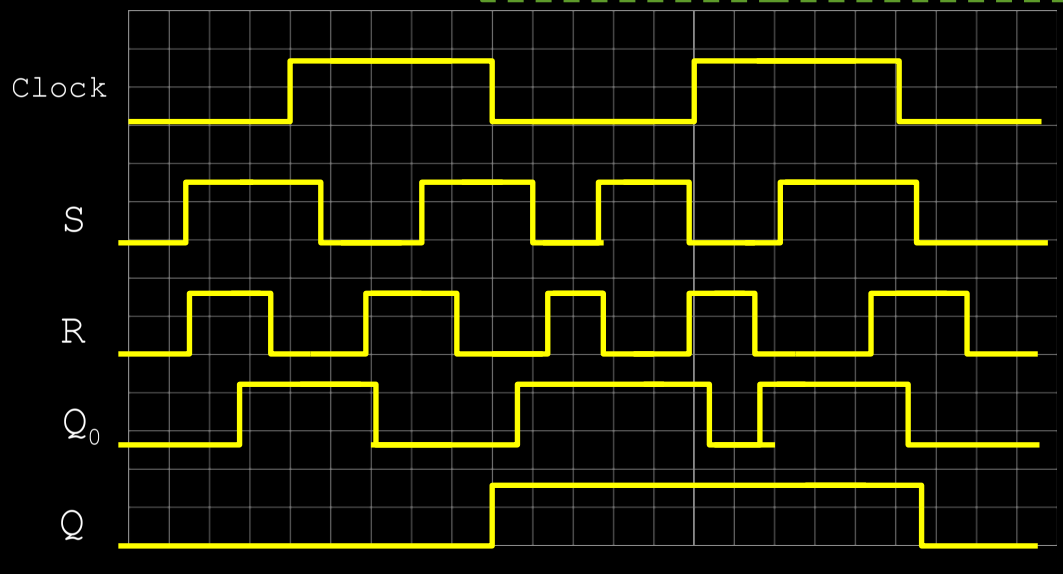
- Negative edge: triggered on falling edge of the clock



Question #6

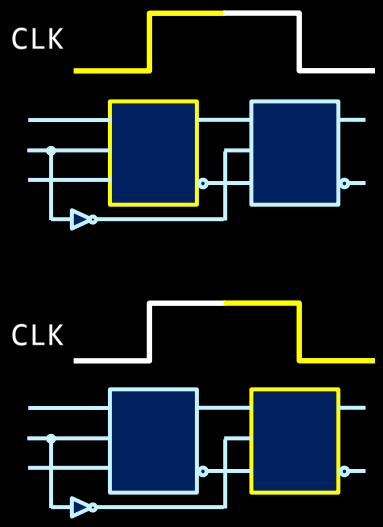
- Assuming all inputs start low, complete the timing diagram





Flip-flops

- For input to propagate to output, it takes each of the latches to be active once.
- First latch changes on "flip".
- Output can only change upon "flop", which is basically the falling edge of the clock signal
- At most one change per clock cycle

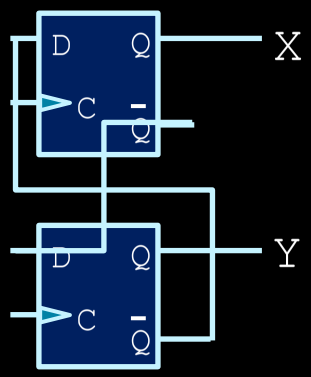


Flip-flops

- We have:
  - D flip-flops (most common type!)
  - SR flip-flops
  - T flip-flops (for "toggle")
  - JK flip-flops

Question #8

- Assuming the Q output of both flip-flops starts as low (X=0 Y=0).
- What will the values of X and Y be over the next few clock cycles?
  - (These are positive edge- triggered)



X

Y

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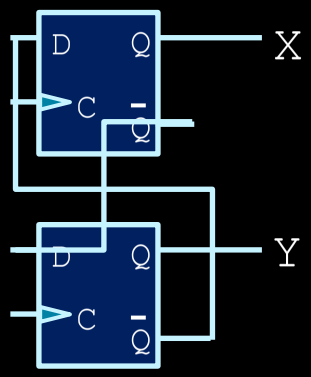
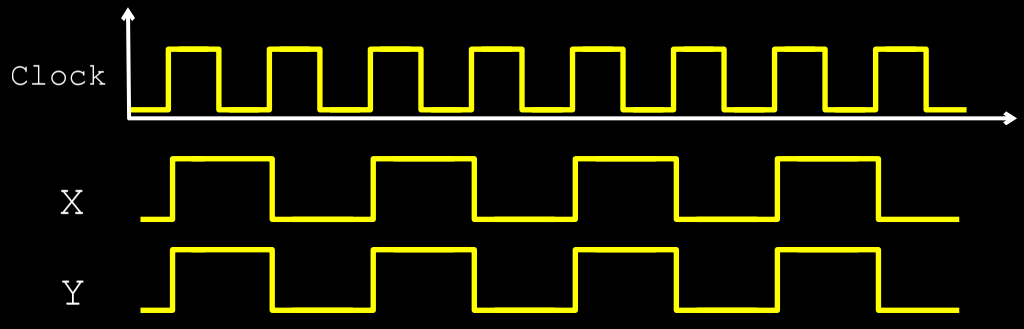
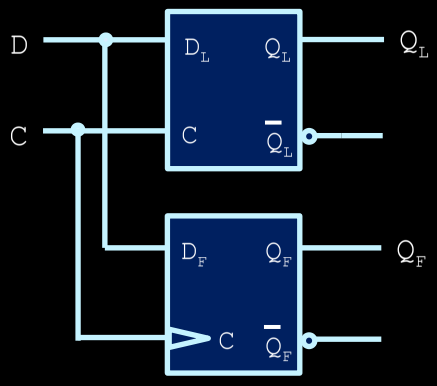
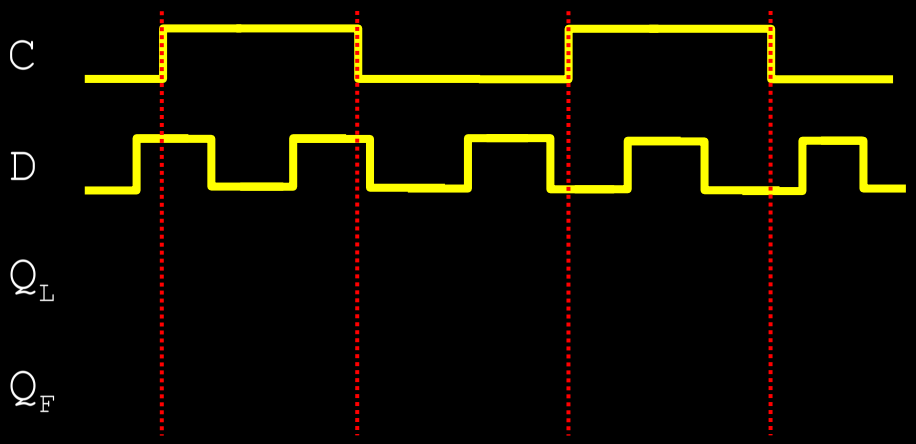




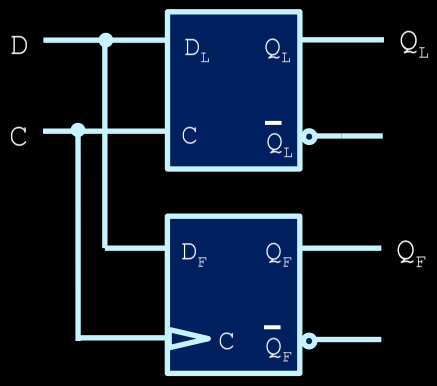
Question #9



- Given the circuit on the right and the input waveform below, what will the outputs be on Q_L and Q_F?
  - Initial state for both is zero



Question #9



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