Implement of Many-Core System Homework 5

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Introduction

With high-level synthesis tool (Cadence® Stratus™), we can quickly design and verify RTL implementation from abstract IEEE 1666 synthesizable SystemC®, C, or C++ models. In this homework, given the synthesizable example codes for sobel filter and script files for synthesis, we need to build a synthesizable RTL of Gaussian filter and also modify those script files for new system.

Implementation details

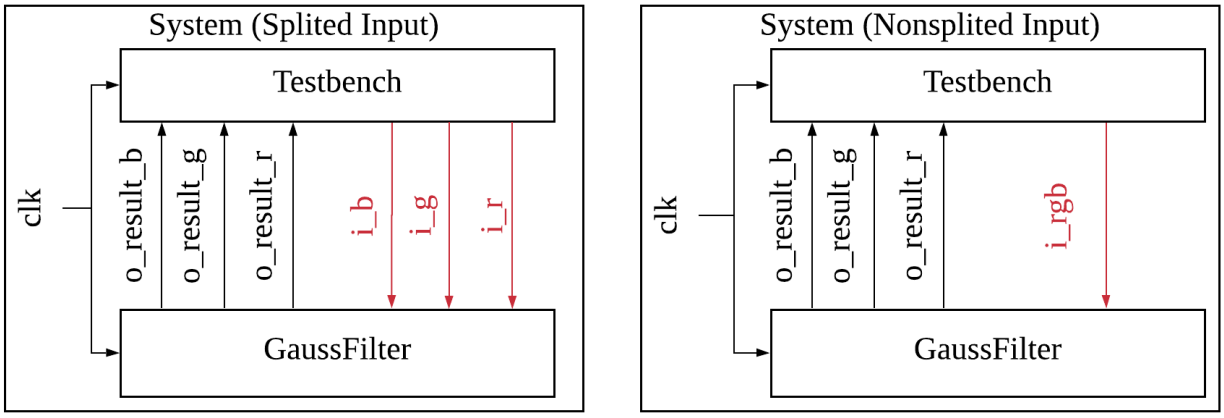
1. Gaussian blur filter is an image filter in digital signal processing. In this homework, we will implement a 3x3 Gaussian blur filter. The kernel is defined as shown below:

$$\text{kernel} = \begin{bmatrix} 1, & 2, & 1 \\ 2, & 4, & 2, \\ 1, & 2, & 1 \end{bmatrix}$$

After 2-D convolution with the original image (lena_std_short.bmp), Gaussian blur process finishes. Also, the 2-D convolution is defined as shown below: since there are three values (r, g, b) in one pixel, the convolution will be done on each value one by one.

$$\text{result}[m,n] = \sum_{j}\sum_{i} \text{original}[i,j] \cdot \text{filter}[m-i, n-j], \qquad 0 \le m,n,i,j \le 2$$

2. Architecture of the whole system.

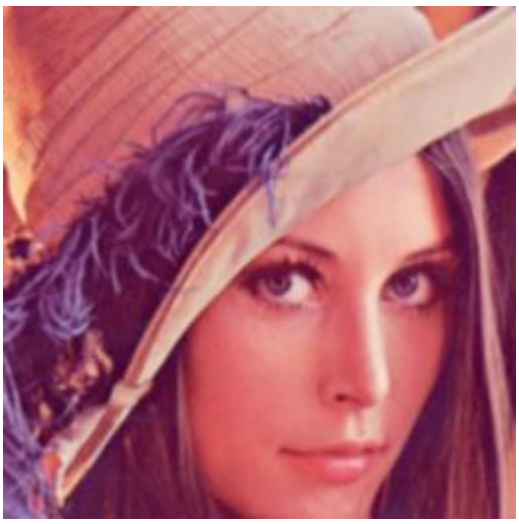


The system with splited input features is shown on the left-hand side, and the system with nonsplited input features is shown on the right-hand side. They both contain Testbench and GaussFilter modules. Also, between two modules, both systems use splited output channels for R, G, B pixels. However, for input channels, the right system combine three input pixels into one channel.

In Testbench module, the input pixels for GaussFilter module are given sequentially one by one. After processing 2D convolution to one pixel, Testbench will receive a result (1 pixel) from GaussFilter and put them into .bmp format. In GaussFilter module, 2D convolution will be done for each channel, For each pixel, after receiving 3x3 input pixels for R, G, B channels, it will put the result pixel into output FIFO and then send into Testbench module. After receiving the result pixel, the Testbench module will then send the next 9 pixels serially to GaussFilter. The process will be repeated till 256 pixels are be processed.

Results

1. Use lena_std_short.bmp for verifying the functionality of Gaussian filter:

Before Gaussian blur	After Gaussian blur
	

Since functions in both systems are the same, we only show the result of one system.

2. Simulation time between different kinds of input featured and different synthesis constraints:

Splited input features - B	Nonsplited input features - B
Info: /OSCI/SystemC: Simulation stopped by user. Total run time = 26214390 ns Simulated time == 26214450 ns	Info: /OSCI/SystemC: Simulation stopped by user. Total run time = 14417910 ns Simulated time == 14417970 ns
Splited input features - BASIC	**Nonsplited input features - BASIC**
Info: /OSCI/SystemC: Simulation stopped by user. Simulation stopped via $stop(1) at time 45219895100 PS + 0 ./bdw_work/sims/top_V_BASIC.v:75 #100 $stop; ncsim> quit Total run time = 45219830 ns	Info: /OSCI/SystemC: Simulation stopped by user. Simulation stopped via $stop(1) at time 28180535100 PS + 0 ./bdw_work/sims/top_V_BASIC.v:69 #100 $stop; ncsim> quit Total run time = 28180470 ns
Splited input features - DPA	**Nonsplited input features - DPA**
Info: /OSCI/SystemC: Simulation stopped by user. Simulation stopped via $stop(1) at time 45219895100 PS + 0 ./bdw_work/sims/top_V_DPA.v:75 #100 $stop; ncsim> quit Total run time = 45219830 ns	Info: /OSCI/SystemC: Simulation stopped by user. Simulation stopped via $stop(1) at time 28180535100 PS + 0 ./bdw_work/sims/top_V_DPA.v:69 #100 $stop; ncsim> quit Total run time = 28180470 ns

The total run time of system with splited input features is 1.6 times the run time of system with nonsplited input features.

3. Synthesis reports between different kinds of input featured and different synthesis constraints:

	Splited input features			Nonsplited input features		
	Seq.	Comb.	Total	Seq.	Comb.	Total
BASIC	2443.9	11094.1	13538.0	2463.1	11121.8	13584.9
DPA	2398.8	9675.6	12074.4	**2410.4**	**10923.4**	**13333.9**

The synthesis reports from stratus_hls.log and stratus_ide (RTL_Summary) are inside the Appendix 1. and Appendix 2. part.

Discussion

From the area result table, we can find that the DPA synthesis constraint will not only reduce the combinational area, but also sequential area. Though area of system with nonsplited input features is slightly bigger than area of system with splited input features, its total run time reduces almost 50%. As a result, system with nonsplited input features is a better design. The main reason why system with nonsplited input features outperforms another can be found in synthesis reports. In the reports of system with nonsplited input features, there are a smaller number of registers, and multiplexers. Besides, the number of adders, dividers and logic gates are all the same.

Conclusion

In this lab, we implement a real function and synthesize it into gate-level module. Also, we change different kinds of implementation and synthesis constraints to get familiar with high-level synthesis tool.

Appendix1.

Splited input features - BASIC

Allocation Report for all threads:

Resource	Count	Area/Instance Seq(#FF)	Comb	BB	Total Area
GaussFilter_Div_32Ux32U_8U_4	1	799.6(108)	6966.4		7766.0
GaussFilter_Mul_32Sx8U_32S_4	2		1239.8		2479.5
mux_32bx2i1c	4		86.9		347.7
GaussFilter_Add_32Ux32U_32U_4	1		269.8		269.8
mux_32bx3i0c	2		101.7		203.4
mux_32bx2i0c	2		99.3		198.7
mux_32bx4i0c	1		136.6		136.6
mux_8bx2i0c	4		24.8		99.3
GaussFilter_N_Mux_32_2_0_4	1		43.8		43.8
GaussFilter_Add_4Ux2U_4U_4	2		15.0		30.1
mux_4bx2i0c	2		12.4		24.8
GaussFilter_OrReduction_8U_1U_4	3		5.1		15.4
GaussFilter_Xor_1Ux1U_1U_1	3		4.4		13.3
GaussFilter_Not_1U_1U_1	3		4.1		12.3
GaussFilter_gen_busy_r_4	3		4.1		12.3
GaussFilter_Add_2Ux1U_2U_4	2		6.2		12.3
mux_1bx2i2c	5		2.3		11.6
GaussFilter_Mul_2Ux2U_4U_4	1		11.3		11.3
mux_2bx3i3c	2		5.4		10.9
mux_2bx2i1c	2		5.4		10.9
mux_4bx2i1c	1		10.9		10.9
GaussFilter_LessThan_2Ux2U_1U_4	2		5.1		10.3
mux_1bx7i1c	1		9.5		9.5
mux_2bx4i4c	1		7.3		7.3
GaussFilter_N_Muxb_1_2_1_4	3		2.4		7.2
GaussFilter_And_1Ux1U_1U_4	5		1.4		6.8
GaussFilter_Or_1Ux1U_1U_4	3		1.4		4.1
mux_1bx2i0c	1		3.1		3.1
GaussFilter_ROM_9X32_mask	1			?	?
registers	34				
Reg bits by type:					
EN SS SC AS AC					
0 0 1 0 0	6	5.5(1)	1.4		
0 1 0 0 0	3	5.5(1)	1.4		
1 0 0 0 0	194	7.5(1)	0.0		
1 0 1 0 0	15	7.5(1)	1.4		
1 1 0 0 0	3	7.5(1)	1.4		
all register bits	221	7.4(1)	0.2		1681.3
estimated cntrl	1		87.5		87.5
Total Area		2443.9(329)	11094.1	0.0	13538.0

Nonsplited input features - BASIC

Allocation Report for all threads:

Resource	Count	Area/Instance Seq(#FF)	Comb	BB	Total Area
GaussFilter_Div_32Ux32U_8U_4	1	799.6(108)	6966.4		7766.0
GaussFilter_Mul_32Sx8U_32S_4	2		1239.8		2479.5
GaussFilter_Add_32Ux32U_32U_4	2		269.8		539.7
mux_32bx2i1c	4		86.9		347.7
mux_32bx3i0c	2		101.7		203.4
mux_32bx2i0c	2		99.3		198.7
GaussFilter_N_Mux_32_2_0_4	1		43.8		43.8
GaussFilter_Add_4Ux2U_4U_4	2		15.0		30.1
mux_8bx2i0c	1		24.8		24.8
GaussFilter_Mul_2Ux2U_4U_4	2		11.3		22.6
mux_2bx2i1c	3		5.4		16.3
GaussFilter_OrReduction_8U_1U_4	3		5.1		15.4
mux_4bx3i0c	1		14.5		14.5
GaussFilter_Xor_1Ux1U_1U_1	3		4.4		13.3
mux_4bx2i0c	1		12.4		12.4
GaussFilter_Not_1U_1U_1	3		4.1		12.3
GaussFilter_Add_2Ux1U_2U_4	2		6.2		12.3
mux_2bx3i3c	2		5.4		10.9
mux_4bx2i1c	1		10.9		10.9
GaussFilter_LessThan_2Ux2U_1U_4	2		5.1		10.3
mux_1bx2i2c	4		2.3		9.3
GaussFilter_And_1Ux1U_1U_4	5		1.4		6.8
mux_1bx5i1c	1		6.6		6.6
GaussFilter_Or_1Ux1U_1U_4	3		1.4		4.1
GaussFilter_gen_busy_r_4	1		4.1		4.1
GaussFilter_N_Muxb_1_2_1_4	1		2.4		2.4
GaussFilter_ROM_9X32_mask	1			?	?
registers	28				
Reg bits by type:					
EN SS SC AS AC					
0 0 1 0 0	6	5.5(1)	1.4		
0 1 0 0 0	1	5.5(1)	1.4		
1 0 0 0 0	201	7.5(1)	0.0		
1 0 1 0 0	14	7.5(1)	1.4		
1 1 0 0 0	1	7.5(1)	1.4		
all register bits	223	7.5(1)	0.1		1693.6
estimated cntrl	1		73.1		73.1
Total Area		2463.1(331)	11121.8	0.0	13584.9

Splited input features - DPA	Nonsplited input features – DPA

Allocation Report for all threads:

Resource	Count	Area/Instance Seq(#FF)	Area/Instance Comb	Area/Instance BB	Total Area
GaussFilter_Div_32Ux32U_8U_4	1	799.6(108)	6966.4		7766.0
GaussFilter_Add2Mul2s32u8s32_4	1		1377.9		1377.9
mux_32bx2i1c	4		86.9		347.7
GaussFilter_Add_32Ux32U_32U_4	1		269.8		269.8
mux_32bx3i0c	2		101.7		203.4
mux_32bx2i0c	1		99.3		99.3
mux_8bx2i0c	3		24.8		74.5
GaussFilter_N_Mux_32_2_19_4	1		43.8		43.8
mux_8bx3i0c	1		27.0		27.0
GaussFilter_Add2u2Mul2i3u2_4	1		17.8		17.8
GaussFilter_OrReduction_8U_1U_4	3		5.1		15.4
GaussFilter_Xor_1Ux1U_1U_1	3		4.4		13.3
GaussFilter_Not_1U_1U_1	3		4.1		12.3
GaussFilter_gen_busy_r_4	3		4.1		12.3
mux_2bx3i3c	2		5.4		10.9
mux_2bx2i1c	2		5.4		10.9
mux_4bx2i1c	1		10.9		10.9
mux_1bx7i1c	1		9.5		9.5
mux_1bx2i2c	4		2.3		9.3
GaussFilter_N_Muxb_1_2_13_4	3		2.4		7.2
GaussFilter_And_1Ux1U_1U_4	5		1.4		6.8
GaussFilter_Add2i1u2_4	2		3.4		6.8
mux_2bx2i0c	1		6.2		6.2
GaussFilter_Or_1Ux1U_1U_4	3		1.4		4.1
mux_1bx2i0c	1		3.1		3.1
GaussFilter_Lti3u2_4	2		1.0		2.1
GaussFilter_ROM_9X32_mask	1			?	?
registers	31				
Reg bits by type:					
EN SS SC AS AC					
0 0 1 0 0	6	5.5(1)	1.4		
0 1 0 0 0	3	5.5(1)	1.4		
1 0 0 0 0	191	7.5(1)	0.0		
1 0 1 0 0	12	7.5(1)	1.4		
1 1 0 0 0	3	7.5(1)	1.4		
all register bits	215	7.4(1)	0.2		1632.0
estimated cntrl	1		74.0		74.0
Total Area		2398.8(323)	9675.6	0.0	12074.4

Allocation Report for all threads:

Resource	Count	Area/Instance Seq(#FF)	Area/Instance Comb	Area/Instance BB	Total Area
GaussFilter_Div_32Ux32U_8U_4	1	799.6(108)	6966.4		7766.0
GaussFilter_Add2Mul2s32u8s32_4	2		1377.9		2755.8
mux_32bx2i1c	4		86.9		347.7
GaussFilter_Add_32Ux32U_32U_4	1		269.8		269.8
mux_32bx2i0c	2		99.3		198.7
mux_32bx3i0c	1		101.7		101.7
GaussFilter_N_Mux_32_2_19_4	1		43.8		43.8
mux_8bx2i0c	1		24.8		24.8
GaussFilter_Add2u2Mul2i3u2_4	1		17.8		17.8
GaussFilter_OrReduction_8U_1U_4	3		5.1		15.4
GaussFilter_Xor_1Ux1U_1U_1	3		4.4		13.3
GaussFilter_Not_1U_1U_1	3		4.1		12.3
mux_2bx2i1c	2		5.4		10.9
mux_4bx2i1c	1		10.9		10.9
GaussFilter_And_1Ux1U_1U_4	5		1.4		6.8
GaussFilter_Add2i1u2_4	2		3.4		6.8
mux_1bx5i1c	1		6.6		6.6
mux_2bx2i0c	1		6.2		6.2
mux_2bx3i3c	1		5.4		5.4
mux_1bx2i2c	2		2.3		4.7
GaussFilter_Or_1Ux1U_1U_4	3		1.4		4.1
GaussFilter_gen_busy_r_4	1		4.1		4.1
GaussFilter_N_Muxb_1_2_13_4	1		2.4		2.4
GaussFilter_Lti3u2_4	2		1.0		2.1
GaussFilter_ROM_9X32_mask	1			?	?
registers	24				
Reg bits by type:					
EN SS SC AS AC					
0 0 1 0 0	6	5.5(1)	1.4		
0 1 0 0 0	1	5.5(1)	1.4		
1 0 0 0 0	198	7.5(1)	0.0		
1 0 1 0 0	10	7.5(1)	1.4		
1 1 0 0 0	1	7.5(1)	1.4		
all register bits	216	7.5(1)	0.1		1635.4
estimated cntrl	1		60.2		60.2
Total Area		2410.4(324)	10923.4	0.0	13333.9

Appendix2. (Memory Area are all 0)

Splited input features - BASIC	Nonsplited input features - BASIC

Area Metrics

Combinational Area:	11,094
Resource Comb. Area:	9,844
Mux Comb. Area:	1,126
Other Comb. Area:	124
Sequential Area:	2,444
Black Box Area:	0
Total Bound Operations:	105
Total Area:	**13,538**

Timing Metrics

Time Units:	ns
Clock Period:	10.00
Cycle Slack:	0.00
Path Delay Limit:	unset
Target Delay:	10.00
Worst Slack:	**0.04**

Resource Metrics

Number of Instances:	31
Widest Input or Output:	32
Number of Pipelined Instances:	1
Bound Operations:	38
Total Resource Area:	**10,644**

Mux Metrics

Number of Instances:	32
Widest Input or Output:	32
Largest Fanin:	7
Implicit Mux Area:	1,075
Explicit Mux Area:	51
Muxed Operations:	37
Total Mux Area:	**1,126**

Register Metrics

Register Count:	34
Register Bits:	221
Bound Register Operations:	65
Total Register Area:	**1,681**

Area Metrics

Combinational Area:	11,122
Resource Comb. Area:	10,117
Mux Comb. Area:	902
Other Comb. Area:	103
Sequential Area:	2,463
Black Box Area:	0
Total Bound Operations:	81
Total Area:	**13,585**

Timing Metrics

Time Units:	ns
Clock Period:	10.00
Cycle Slack:	0.00
Path Delay Limit:	unset
Target Delay:	10.00
Worst Slack:	**0.04**

Resource Metrics

Number of Instances:	31
Widest Input or Output:	32
Number of Pipelined Instances:	1
Bound Operations:	36
Total Resource Area:	**10,916**

Mux Metrics

Number of Instances:	24
Widest Input or Output:	32
Largest Fanin:	5
Implicit Mux Area:	856
Explicit Mux Area:	46
Muxed Operations:	13
Total Mux Area:	**902**

Register Metrics

Register Count:	28
Register Bits:	223
Bound Register Operations:	43
Total Register Area:	**1,694**

Splited input features - DPA	Nonsplited input features – DPA

Area Metrics

Combinational Area:	9,676
Resource Comb. Area:	8,705
Mux Comb. Area:	864
Other Comb. Area:	107
Sequential Area:	2,399
Black Box Area:	0
Total Bound Operations:	97
Total Area:	**12,074**

Timing Metrics

Time Units:	ns
Clock Period:	10.00
Cycle Slack:	0.00
Path Delay Limit:	unset
Target Delay:	10.00
Worst Slack:	**0.04**

Resource Metrics

Number of Instances:	28
Widest Input or Output:	32
Number of Pipelined Instances:	1
Bound Operations:	33
Total Resource Area:	**9,505**

Mux Metrics

Number of Instances:	27
Widest Input or Output:	32
Largest Fanin:	7
Implicit Mux Area:	813
Explicit Mux Area:	51
Muxed Operations:	37
Total Mux Area:	**864**

Register Metrics

Register Count:	31
Register Bits:	215
Bound Register Operations:	62
Total Register Area:	**1,632**

Area Metrics

Combinational Area:	10,923
Resource Comb. Area:	10,075
Mux Comb. Area:	764
Other Comb. Area:	85
Sequential Area:	2,410
Black Box Area:	0
Total Bound Operations:	74
Total Area:	**13,334**

Timing Metrics

Time Units:	ns
Clock Period:	10.00
Cycle Slack:	0.00
Path Delay Limit:	unset
Target Delay:	10.00
Worst Slack:	**0.04**

Resource Metrics

Number of Instances:	27
Widest Input or Output:	32
Number of Pipelined Instances:	1
Bound Operations:	31
Total Resource Area:	**10,874**

Mux Metrics

Number of Instances:	18
Widest Input or Output:	32
Largest Fanin:	5
Implicit Mux Area:	718
Explicit Mux Area:	46
Muxed Operations:	13
Total Mux Area:	**764**

Register Metrics

Register Count:	24
Register Bits:	216
Bound Register Operations:	41
Total Register Area:	**1,635**