Advance Data Sheet

B50282

Octal QSGMII Copper Gigabit Ethernet Transceiver

GENERAL DESCRIPTION

The Broadcom® B50282 is a fully integrated octal gigabit transceiver with support for Energy Efficient Ethernet (EEE) and Synchronous Ethernet (SyncE).

The MDI twisted-pair transceiver consists of eight triple-speed 10/100/1000BASE-T Ethernet transceivers.

When in Copper mode, the PHY performs all of the physical layer functions for 10BASE-T, 100BASE-TX, and 1000BASE-T on standard Category 5 UTP cable.

The B50282 is designed to be compliant with the QSGMII industry standards.

The B50282 is based on the proven digital-signal processor technology of Broadcom, combining digital adaptive equalizers, ADCs, phase locked loops, line drivers, encoders, decoders, echo cancelers, crosstalk cancelers, and all other required support circuitry integrated into a single, monolithic CMOS chip.

Designed for reliable operation over worst-case Category 5 cable plants, the B50282 automatically negotiates with any transceiver on the opposite end of the wire to agree on an operating speed. The PHY can also evaluate the condition of the twisted-pair wiring to ensure that the wiring can support operation at Gigabit speeds, and detect and correct most common wiring problems. The device continually monitors both the wiring and the opposing transceiver and alerts the system if it detects potential problems with reliable operation.

APPLICATIONS

- High-density Gigabit Ethernet switches and routers.

FEATURES

- QSGMII interface
- Support for IEEE 802.3-compliant copper line interfaces:
  - 1000BASE-T
  - 100BASE-TX
  - 10BASE-T
- Integrated twisted-pair termination resistors
- IEEE 802.3az-compliant (Energy Efficient Ethernet)
  - Support for native EEE MACs
  - Support for legacy non-EEE MACs using AutogrEEEn® mode
- Ethernet@WireSpeed™
- Cable plant diagnostics that detect cable plant impairments
- Sync_E support
  - Two recovered clocks
  - Two recovered clock lock outputs
- Jumbo frame support for 16 KB packets
- 3.3V digital I/O
- Support for only two power supplies (1.0V and 3.3V)
- Line-side and switch-side loopbacks
- Dual MDIO support for reduced latency
- Programmable LEDs
- Robust Cable ESD (CESD) tolerance
- Low EMI emissions
- IEEE 1149.1 and 1149.6 (ACJTAG) boundary scan
- Package: 17 mm x 17 mm 256-ball FBGA

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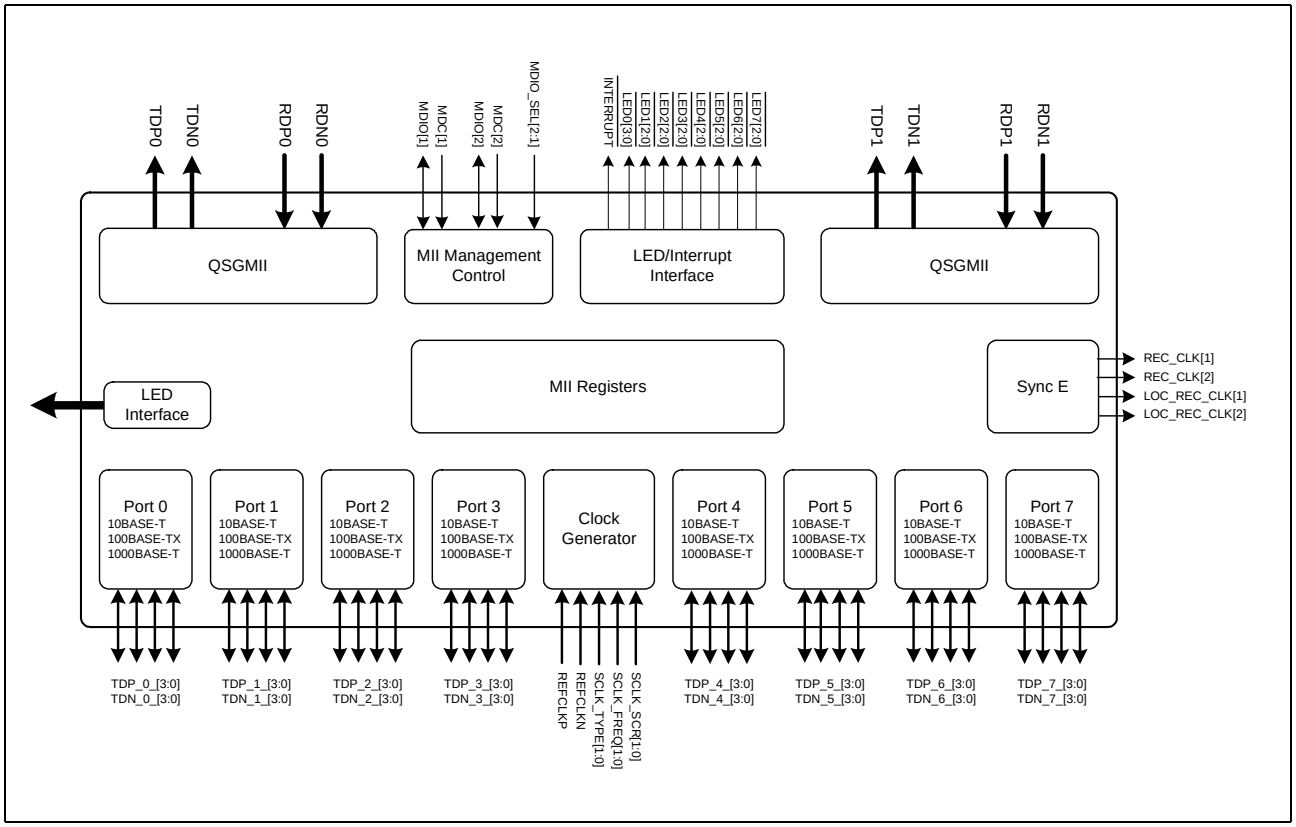
Figure 1: Functional Block Diagram



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Revision History

Change Description	*Customer Impact*	*Action Items*
Revision: B50282-DS04-R **Date:** 05/06/14 **Note:** Page numbers referred to are valid only for this revision of the document.		
Updated:		
• "Cleanup PLL Considerations" on page 26 changed < to ≤.	–	–
• Table 17: "Ball Descriptions," on page 57 changed ball description for LOCK_REC_CLK[1:0] from Copper PLL Reference Clock Lock to PLL Reference Clock Lock.	–	–
• "Per Port QSGMII/SGMII Packet Loopback" on page 130 changed Write RDB_Register, offset 0x021, bit[0] = 1'b'1 (1000BASE-T register space selected.) to Write RDB_Register, offset 0x021, bit[0] = 1'b'0 (1000BASE-T register space selected.)	–	–
Added:		
Revision: B50282-DS03-R **Date:** 09/10/13 **Note:** Page numbers referred to are valid only for this revision of the document.		
Updated:		
• Table 71: "Ordering Information," on page 159.	–	–
Added:		
• Table 53: "I/O Operating at OVDD = 2.5V," on page 147.	–	–
Revision: B50282-DS02-R **Date:** 05/20/13 **Note:** Page numbers referred to are valid only for this revision of the document.		
Updated:		
• Removed LLPD from "AutogrEEEn Flow" on page 28.	–	–
• QSGMII description in "QSGMII: Quad Serial Gigabit Media Independent Interface" on page 38.	–	–
• QSGMII description in Table 6: "QSGMII Interface Balls," on page 39.	–	–
• "Wire Map and Pair Skew Correction" on page 43.	–	–
• Fiber, SGMII, QSGMII, and TRST descriptions in Table 27: "Ball Descriptions," on page 84.	–	–
• Added new ESR row in Table 37: "Typical Crystal Parameters," on page 123.	–	–
• Added Force link for 10/100Mb/s in "Per Port QSGMII/SGMII Packet loopback" on page 133.	–	–
• Figure 41: "REFCLK Input Timing Single-Ended Mode," on page 138.	–	–
• Figure 42: "REFCLK Input Timing Differential Mode," on page 139.	–	–
• Table 55: "QSGMII to Copper Current Consumption," on page 146.	–	–
• Output differential voltage and definition of Load Type 2 in Table 68: "QSGMII Transmitter," on page 150.	–	–
• Definition of Load Type 2 in Table 70: "QSGMII Receiver," on page 152.	–	–

Change Description	*Customer Impact*	*Action Items*
Added:		
Revision: B50282-DS01-R **Date:** 10/23/12 **Note:** Page numbers referred to are valid only for this revision of the document.		
Updated:		
• Global change from MDI MII to MDIO MII.	–	–
• Global change from Differential Clock to CML Differential Clock.	–	–
• TBD to 1 ns in Table 34: “REFCLK Input Timing,” on page 100 and Table 35: “REFCLKP/N Clock Input Timing,” on page 101.	–	–
• MDIO output delay from 15 ns to 50 ns in for OVDDMDIO = 1.2V Table 36: “Management Interface Timing,” on page 102.	–	–
• Changed min. and max. TCK to TDO Delay from 5.0 ns to 4.5 ns and 15 ns to 20 ns in Table 37: “JTAG Timing,” on page 102.	–	–
• Changed vil from 0.8V to 0.7V and voh from OVDD-0.4V to OVDD - 0.45V in Table 46: “JTAG: OVDDJTAG Operating at 2.5V,” on page 107.	–	–
• Reference clock input voltage swing differential from 1600 to 2000 in Table 49: “CML Differential Reference Clock,” on page 108.	–	–
• Differential Input Impedance from 80 to 90 and from 120 to 130 in Table 49: “CML Differential Reference Clock,” on page 108.	–	–
• Reference clock input voltage swing differential from 500 to 600 in Table 49: “CML Differential Reference Clock,” on page 108.	–	–
• C0 to C1 in Table 57: “Ordering Information,” on page 116.	C0 silicon is no longer supported.	Order C1 silicon.
Added:		
• Added register writes for QSGMII LPI enable in “Native EEE Flow” on page 18.	–	–
• Added PU to MDIO I/O type and PD to MDC I/O type in Table 18: “Ball Descriptions,” on page 63.	–	–
• Added REFCLKP/REFCLKN have an internal 100Ω differential impedance in “CML Differential Mode” on page 84.	–	–
Revision: B50282-DS00-R **Date:** 05/04/12 **Note**: Page numbers referred to are valid only for this revision of the document.		
Initial release.	–	–

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About This Document

Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® B50282. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

Acronyms and abbreviations in this document are also defined in Appendix A: “Acronyms and Abbreviations,” on page 100.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

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In addition, Broadcom provides other product support through its Downloads and Support site (http://www.broadcom.com/support/).

Section 1: Introduction

Overview

This document provides the following information on the B50282 PHY:

Section 2: Functional Description

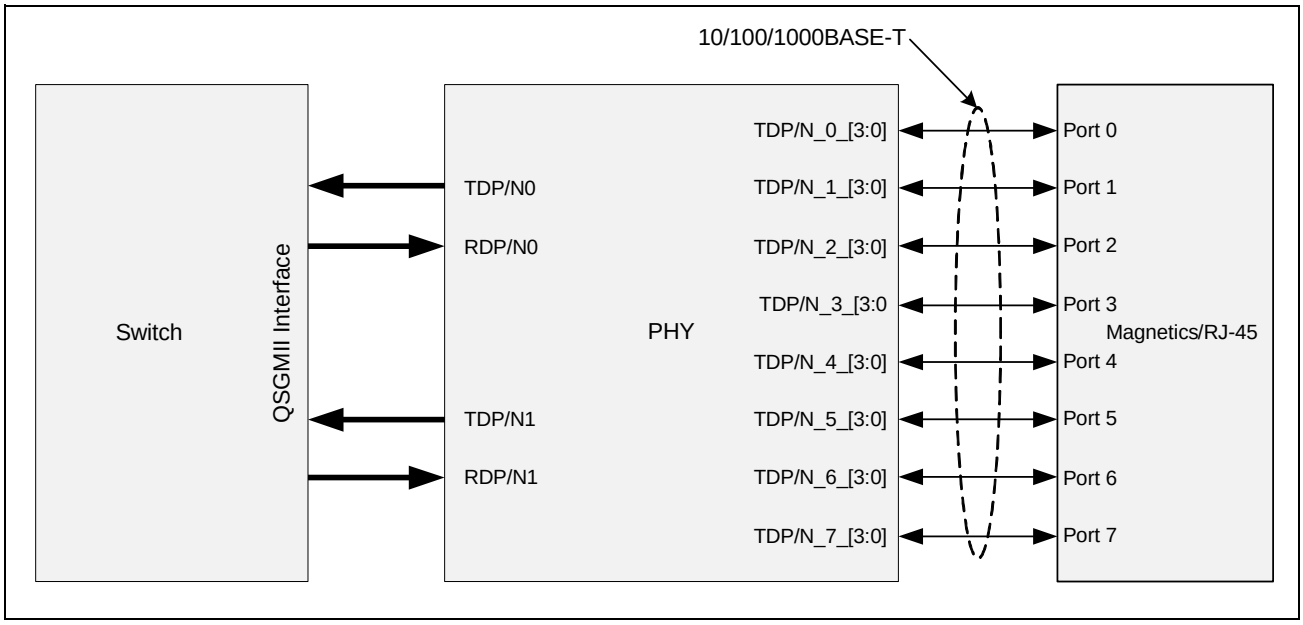
Overview

The Broadcom B50282 is an Octal Gigabit Ethernet transceiver. See Table 1 for a summary of supported interfaces and features.

Table 1: Auto-Negotiation Register

Switch Interface	*MDI Interface*	*Protocol for MDI*	*Additional Features*
QSGMII	Copper	• 1000BASE-T • 100BASE-TX • 10BASE-T	• Energy Efficient Ethernet (EEE): IEEE 802.3az-compliant • AutogrEEEn • Synchronous Ethernet See Figure 3: “Key Features,” on page 15.

Figure 2: QSGMII-to-Copper Block Diagram



Section 3: Key Features

Overview

This section describes the key features of the B50282.

- Energy Efficient Ethernet—IEEE 802.3az-compliant
- AutogrEEEn
- Synchronous Ethernet

Energy Efficient Ethernet

The B50282 contains support for EEE. Energy Efficient Ethernet is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in low-power idle (LPI) mode, which when enabled supports quiet times during low link utilization allowing both sides of a link to disable portions of each PHY's operating circuitry and save power.

The B50282 offers the following two basic modes of operation:

- Native EEE mode—For switches that support LPI signaling across the QSGMII interface.
- AutogrEEEn mode—For legacy switches that do not support LPI signaling across the QSGMII interface.

When in either Native or AutogrEEEn mode, the PHY supports the following:

- Support for 100BASE-TX (auto-negotiation must be enabled).
- Support for 1000BASE-T (auto-negotiation must be enabled).
- Link status does not change.
- Frames are not dropped or corrupted.
- The transition time to and from the lower power levels is transparent to upper layer protocols and applications.

In addition to the standard EEE operation, the B50282 supports the following enhancements to the EEE functions:

- Native mode enhancements
  - QSGMII Auto-Negotiation Link Partner Register includes new EEE Capability bit (bit[9] = 1'b1: LPI Capability).
- AutogrEEEn mode enhancements
  - Fixed latency
  - Variable latency

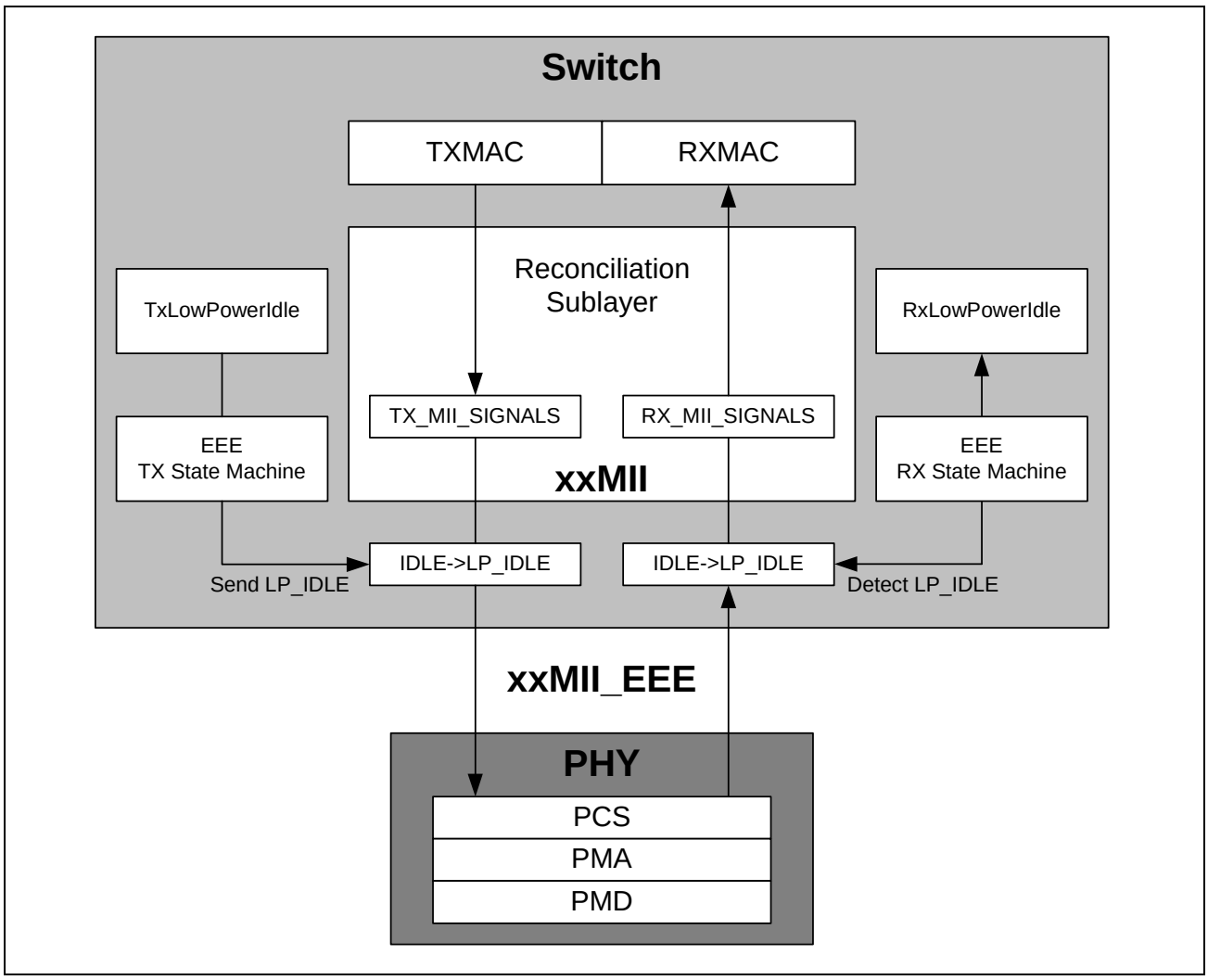
Native EEE Mode

Native EEE mode is used for switches that support IEEE 802.3az LPI-code group signaling through the QSGMII interfaces. Figure 3 shows LPI support in the switch.

The switch also has to be aware that the medium is not immediately available when in LPI mode. This means the switch needs to be able to do the following:

- Hold off data transmission when the link is in LPI mode.
- Account for wake-up time when transitioning from LPI to the active state when it wants to initiate data transmission.
- Optionally, support the IEEE 802.3AB protocol (LLDP). This is used by devices to negotiate additional wake-up times.

Figure 3: Native EEE Mode (Switch-Supported EEE LPI)



Native EEE Flow

The following steps are required to enable Native EEE mode on a per port basis.

1. Enable Native EEE mode.

   Write Clause 45, DEVAD 0x7, address 0x803D, bits[15:14] = 2'b11 (default setting).

2. Enable QSGMII LPI.
   a. Write 0xC000 to QSGMII[0]Register: BAR = 0x8330, REGAD = 0x1E, AER = 0x0000
   b. Write 0xC000 to SGMII[1] Register: BAR = 0x8330, REGAD = 0x1E, AER = 0x0004

3. Advertise normal auto-negotiation capabilities.
   a. Write Register 0x04 with 10BASE-T and 100BASE-TX abilities.
   b. Write Register 0x09 with 1000BASE-T abilities.

4. Advertise EEE auto-negotiation capabilities.
   a. Write Clause 45 DEVAD 0x7, address 0x3C, bit[1] = 1'b1 (advertise 100BASE-TX EEE ability).
   b. Write Clause 45 DEVAD 0x7, address 0x3C, bit[2] = 1'b1 (advertise 1000BASE-T EEE ability).

5. Initiate auto-negotiation.

   Write Register 0x0, bit[12] = 1'b1 (restart auto-negotiation).

   Local and remote PHY auto-negotiate speed, duplex, remote fault, pause, master/slave, next page and EEE abilities. The link is established (10BASE-T, 100BASE-TX or 1000BASE-T).

   The switch looks at the EEE_RESOLUTION_STATUS Register, Clause 45 DEVAD 0x7, address 0x803E, bits[2:1] to determine what EEE speeds are supported. Bit[2] = 1'b1: Both local device and link partner advertise EEE 1000BASE-T capability. Bit[1] = 1'b1: Local and link partner advertise EEE 100BASE-TX mode.

6. Read EEE 1000BASE-T resolution.

   Clause 45, DEVAD 0x7, address 0x803E, bit[2] = 1'b1 (EEE_1000T_Resolution).

7. Read EEE 100BASE-TX resolution.

   Clause 45, DEVAD 0x7, address 0x803E, bit[1] = 1'b1 (EEE_100TX_Resolution).

If both the local and remote PHYs support EEE, they can optionally negotiate longer system wake-up times (T_{w_sys}) through LLPD. The default settings below are used if LLPD is not used.

- T_{w_sys} default for 100BASE-TX = 30 µs
- T_{w_sys} default for 1000BASE-T = 16.5 µs

The switch determines when the B50282 transmits LPI signals on the MDI. The B50282 transmits LPI signals when the B50282 receives the newly defined code groups from the switch as specified in IEEE 802.3az.

- If a 100BASE-TX link is established, the B50282 can start sending LPI.
- If a 1000BASE-T link is established, the B50282 only enters LPI mode after it transmits LP_Sleep and receives LP_Sleep from the remote PHY.

The B50282 communicates and coordinates the LPI transition across the MDI. See “MDI LPI Operation” on page 21. The B50282 keeps the link-related parameters current during refresh. The switch determines when the B50282 stops sending LPI signals on the MDI and transitions to normal mode.

The B50282 stops transmitting LPI signals when the B50282 receives normal IPGs from the switch to stop transmitting LPI signals. After the Tw_PHY time, the switch may send normal data.

Note: The user is not allowed to send normal data to terminate an LPI request.

LPI Mode Status

To determine when the PHY is receiving LPI from the switch, read PCS_STATUS_1 register.

- Clause 45, DEVAD 0x3, address 0x1, bit[9] = 1’b1 (transmit PCS is currently receiving LPI).
- Clause 45, DEVAD 0x3, address 0x1, bit[8] = 1’b1 (receive PCS is currently receiving LPI).

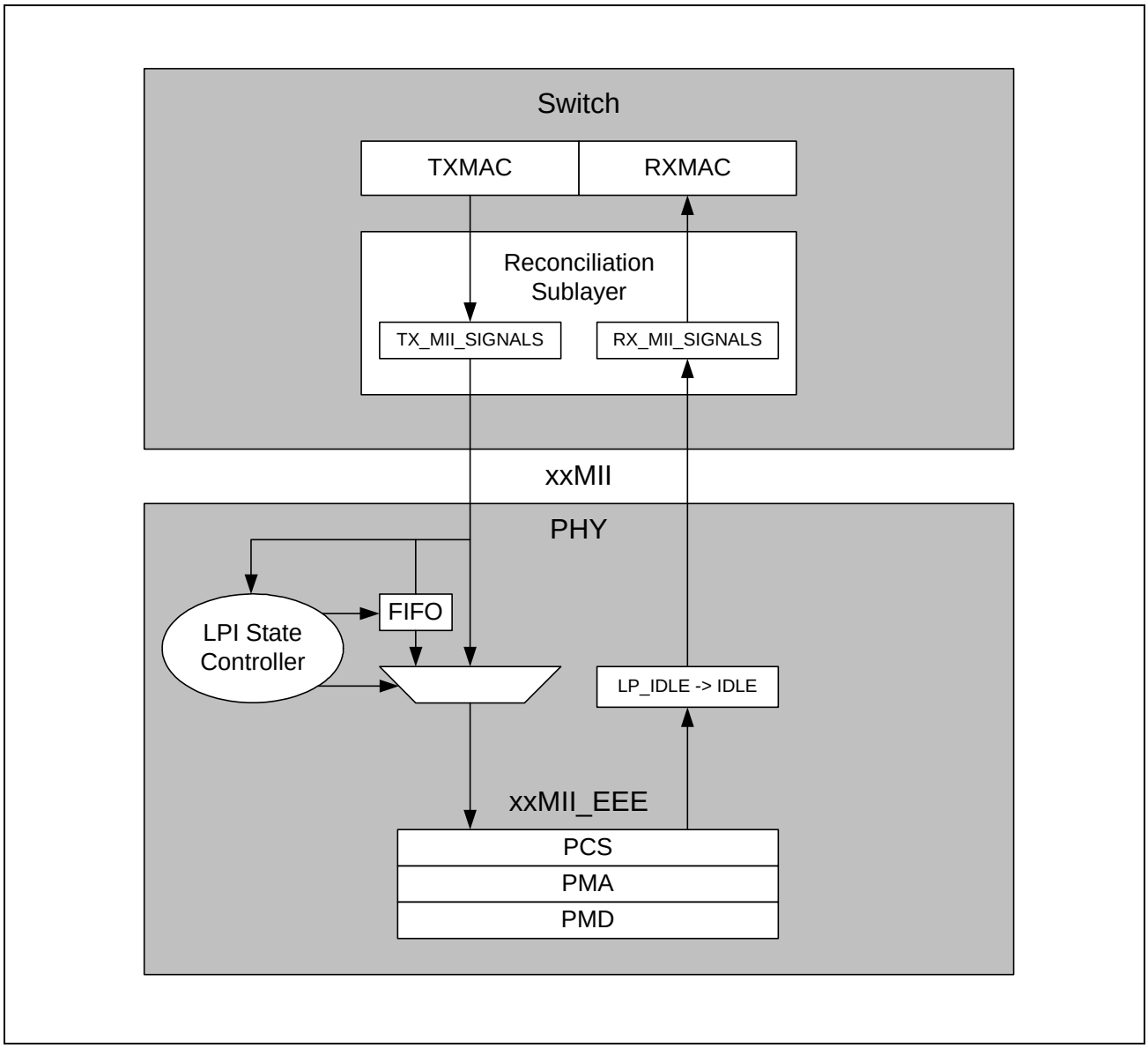
AutogrEEEn Mode

AutogrEEEn mode is used for legacy switches that do not support IEEE 802.3az LPI-code group signaling through the QSGMII interfaces. Figure 4 on page 19 shows LPI support in the PHY. AutogrEEEn mode transmits the same LPI signals on the MDI as Native EEE mode, making it compatible with PHYs that support either Native EEE or AutogrEEEn mode.

AutogrEEEn mode has the following benefits:

- The switch does not need to be aware that the PHY is transmitting LPIs.
- The switch assumes that the media is always available to it.
- Legacy switches can connect to either EEE-enabled link partners or non-EEE-enabled link partners.

Figure 4: AutogrEEEn Mode (PHY Supported EEE LPI)



AutogrEEEn Flow

The following are the steps needed to enable AutogrEEEn mode on a per port basis. AutogrEEEn mode is disabled by default.

1. Enable EEE mode.

   Write Clause 45, DEVAD 0x7, address 0x803D, bits[15:14] = 2'b11 (default setting).

2. Advertise EEE auto-negotiation capabilities.
   a. Write Clause 45, DEVAD 0x7, address 0x3C, bit[1] = 1'b1 (100BASE-TX EEE ability).
   b. Write Clause 45, DEVAD 0x7, address 0x3C, bit[2] = 1'b1 (1000BASE-T EEE ability).

3. Advertise normal auto-negotiation capabilities.
   a. Write Register 0x04 with 10BASE-T and 100BASE-TX abilities.
   b. Write Register 0x09 with 1000BASE-T abilities.
4. Enable optional variable/fixed latency modes (see “Variable/Fixed Latency Modes” on page 22).
   - RDB_Register, offset 0x800, bit[2] = 1’b1 (enable variable latency mode)

     or
   - RDB_Register, offset 0x800, bit[2] = 1’b0 (enable fixed latency mode)
5. Initiate auto-negotiation by writing register 0x00, bit[9] = 1’b1 (restart Auto_Negotiation).
   a. Local and remote PHY auto-negotiate speed, duplex, remote fault, pause, master/slave, next page, and EEE abilities.
   b. The link is established (10BASE-T, 100BASE-TX, or 1000BASE-T).
   c. The switch looks at the EEE_RESOLUTION_STATUS Register, Clause 45 DEVAD 0x7, address 0x803E, bits[2:1] to determine what EEE speeds are supported. Bit[2] = 1’b1: Both local device and link partner advertise EEE 1000BASE-T capability. Bit[1] = 1’b1: Local and link partner advertise EEE 100BASE-TX mode.
6. Read EEE 1000BASE-T resolution.

   Read Clause 45, DEVAD 0x7, address 0x803E, bit[2] = 1’b1 (EEE_1000T_Resolution).
7. Read EEE 100BASE-TX resolution.

   Read Clause 45, DEVAD 0x7, address 0x803E, bit[1] = 1’b1 (EEE_100TX_Resolution:).
8. Enable AutogrEEEn on port by port basis:
   a. Port 0: Write RDB_Register, offset 0x8000, bit[0] = 1’b1
   b. Port 1: Write RDB_Register, offset 0x8002, bit[0] = 1’b1
   c. Port 2: Write RDB_Register, offset 0x8004, bit[0] = 1’b1
   d. Port 3: Write RDB_Register, offset 0x8006, bit[0] = 1’b1
   e. Port 4: Write RDB_Register, offset 0x8008, bit[0] = 1’b1
   f. Port 5: Write RDB_Register, offset 0x800A, bit[0] = 1’b1
   g. Port 6: Write RDB_Register, offset 0x800C, bit[0] = 1’b1
   h. Port 7: Write RDB_Register, offset 0x800E, bit[0] = 1’b1

The B50282 transmits LPI signals on the MDI, when the number of consecutive idle symbols is equal to the EEE_Idle threshold.

- If a 100BASE-TX link is established, the B50282 can start sending LPI.
- If a 1000BASE-T link is established, the B50282 will only enter LPI mode after it transmits LP_Sleep and receives LP_Sleep from the remote PHY.

The B50282 communicates and coordinates the LPI transition across the MDI (see “MDI LPI Operation” on page 21). The B50282 keeps the link related parameters up to date through refresh. The B50282 will stop sending LPI signals on the MDI and transition to normal mode when a transmit data is received from the switch.

QSGMII Auto-Negotiation

The QSGMII auto-negotiation register, in addition to the link, duplex, and speed bits, now contains a EEE-capable bit (bit[9]) indicating if the remote device is EEE-capable (as shown in Table 2).

Table 2: Auto-Negotiation Register

Bit	Name	Description
15	Copper link	1'b1 = Link up. 1'b0 = Link down.
14	Reserved	Reserve for auto-negotiation acknowledge as specified in IEEE 802.3z.
13	Reserved	Reserved for future use.
12	Copper duplex	1'b1 = Full-duplex mode. 1'b0 = Half-duplex mode.
11:10	Copper speed	2'b11 = Reserved. 2'b10 = 1000BASE-T. 2'b01 = 100BASE-TX. 2'b00 = 10BASE-T.
9	EEE-capable	1'b1 = Remote device is Energy Efficient Ethernet capable. 1'b0 = Remote device is not Energy Efficient Ethernet capable.
8:1	Reserved	Write as 1'b0. Reserved for future use.
0	QSGMII selector	Write as 1'b1.

MDI LPI Operation

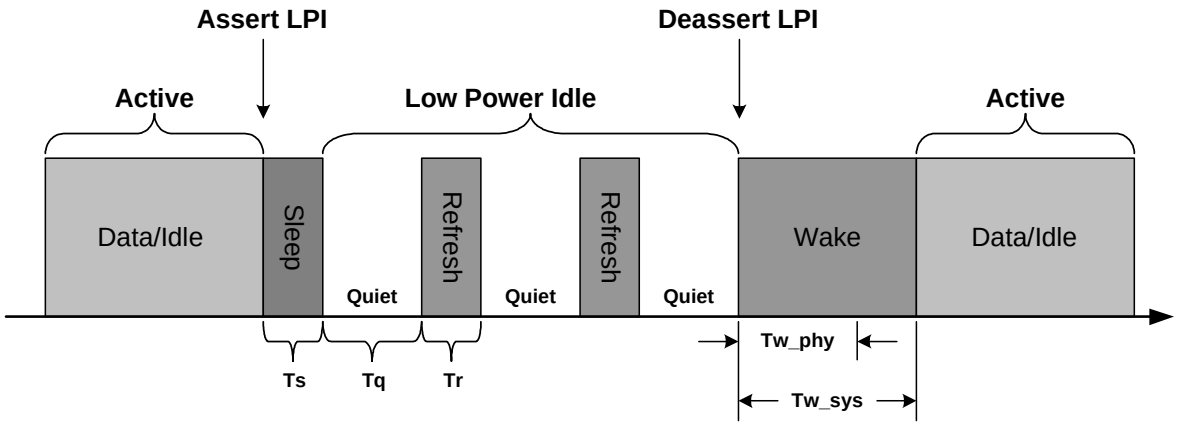
In 100BASE-TX mode, the local PHY transmits a special LP_Sleep signal to communicate to the link partner that the local system is entering LPI mode. In 1000BASE-T mode, the transmit function of the local PHY enters a quiet mode only after the local PHY transmits LP_Sleep and receives LP_Sleep from the remote PHY. If the remote PHY does not signal LPI, then neither PHY can go quiet. The LPI requests are still passed from one end to the other end of the link, since other system energy savings may be achieved even if the PHY link does not go quiet.

The following three states are visible above the EEE PHY when in Native EEE mode. These states are also shown in Figure 5 on page 22. For AutogrEEEn mode, these states are handled by the B50282.

- Active—Transmission of data and normal idle.
- Low Power Idle—Transmission LPI.
- Hold—Transition state between LPI and active.

During LPI mode, only two states are visible; sleep and quiet. For times in each state and value, refer to IEEE 802.3az Clause 24 table 24-2 for 100BASE-TX and Clause 40.12.5 for 1000BASE-T.

Figure 5: AutogrEEEn Mode (PHY Supported EEE LPI)



- Tw_sys >= Tw_phy
- Wait a minimum of Tw_sys before sending data.

Variable/Fixed Latency Modes

When in AutogrEEEn mode, the B50282 can support either variable or fixed latency modes. When operating in variable latency mode:

- Non-IDLE characters are written into the FIFO.
- The FIFO drains as the IDLEs accumulate in the traffic profile.
- The FIFO is bypassed once it is empty.

When operating in fixed latency mode (RDB_Register, offset 0x800, bit[2] = 1'b0), IDLE characters are stuffed in the FIFO to maintain a constant latency value in the data stream.

Synchronous Ethernet

The B50282 has the provision to output a clock, recovered from the copper MDI link partner, allowing point-to-point synchronization of the clock frequency. The recovered clock output, if it is fed back into the B50282 REFCLKP/REFCLKN input, must be fed into a jitter-attenuating cleanup PLL to attenuate accumulated jitter and provide a clean reference.

The recovered clock is 25 MHz when the B50282 is linked in 1000BASE-T slave and 100BASE-TX mode. When in 1000BASE-T mode, to output the recovered clock from the link partner, the B50282 must auto-negotiate to Slave mode. If the B50282 auto-negotiates to master mode, the B50282 will recover its own clock, not the clock of the link partner. 10BASE-T is Manchester encoded and the clock phase information is only transmitted when a packet is being transmitted, so 10BASE-T cannot not be used for Synchronous Ethernet applications.

The B50282 provides two recovered clocks (REC_CLK[1] and REC_CLK[2]) and two PLL lock indicators (LOC_REC_CLK[1] and LOC_REC_CLK[2]) for Synchronous Ethernet applications. The recovered clocks will be based on either the B50282's reference clock or the recovered clock from one of the B50282's ports. Table 3 on page 24 shows the source from which the recovered clocks are derived. The recovered clock output must be fed into a jitter attenuating cleanup PLL to attenuate accumulated jitter and provide a clean reference. The recovered clock is 25 MHz when the device is linked in 1000BASE-T Slave and 100BASE-TX modes. For additional information, see *Synchronizing Broadcom PHYs for Point-to-Point Synchronous Ethernet Applications* (SYNCE-AN10x-R).

Caution! When Synchronous Ethernet is enabled, EEE and AutogrEEEn mode must be disabled on the port used for the REC_CLK[1] and or REC_CLK[2].

Caution! 1000BASE-T master mode recovers its own clock and should not be used for Synchronous Ethernet applications.

Caution! 10BASE-T is Manchester encoded and the clock phase information is only transmitted when a packet is being transmitted, therefore 10BASE-T should not be used for Synchronous Ethernet applications.

Table 3: Recovered Clock Source and Speed Based on Link Status

Mode	*Recovered Clock Source*	*Recovered Clock Speed*
1000BASE-T (slave, link up)	Recovered clock from line-side data	25 MHz
1000BASE-T (master, link up)	B50282 reference clock	25 MHz
1000BASE-T (master or slave, link-down) • RDB_Register, offset 0x83C, bit[8] = 1'b0.	B50282 reference clock	25 MHz
1000BASE-T (master or slave, link-down) • RDB_Register, offset 0x83C, bit[8] = 1'b1.	Driven low	N/A
100BASE-TX (link up)	Recovered clock from line-side data	25 MHz
100BASE-TX (link-down) • RDB_Register, offset 0x83C, bit[8] = 1'b0.	B50282 reference clock	25 MHz
100BASE-TX (link-down) • RDB_Register, offset 0x83C, bit[8] = 1'b1.	Driven low	N/A
10BASE-T (link up)	B50282 reference clock	25 MHz
10BASE-T (link-down) • RDB_Register, offset 0x83C, bit[8] = 1'b0.	B50282 reference clock	25 MHz
10BASE-T (link-down) • RDB_Register, offset 0x83C, bit[8] = 1'b1.	Driven low	N/A

REC_CLK[1] and REC_CLK[2]

REC_CLK[1] and REC_CLK[2] are disabled by default. The port that the recovered clocks are derived from can be selected by writes to the SYNCE_RECOVERY_CLOCK Register. The port that REC_CLK[1] is derived from is set by bits[2:0] and the port that REC_CLK[2] is derived from is set by bits[6:4] See Table 4 on page 25. The B50282 also supports Sync_E Auto Clock Disable mode and Sync_E Auto Switching mode.

Table 4: Recovered Clock Port Selection

REC_CLK[1]		*REC_CLK[2]*	
Port #	***RDB_Register, Offset 0x83C, Bits[2:0]***	***Port #***	***RDB_Register, Offset 0x83C, Bits[6:4]***
Port 0	0x0	Port 0	0x0
Port 1	0x1	Port 1	0x1
Port 2	0x2	Port 2	0x2
Port 3	0x3	Port 3	0x3
Port 4	0x4	Port 4	0x4
Port 5	0x5	Port 5	0x5
Port 6	0x6	Port 6	0x6
Port 7	0x7	Port 7	0x7

REC_CLK[1] and REC_CLK[2]

By default, the REC_CLK[1] and REF_CLK[2] outputs are disabled.

- Enable REC_CLK[1]: REC_CLK1_DISABLE bit (RDB_Register, offset 0x83C, bit[3] = 1’b0).
- Disable REC_CLK[1]: REC_CLK1_DISABLE bit (RDB_Register, offset 0x83C, bit[3] = 1’b1).
- Enable REC_CLK[2]: REC_CLK2_DISABLE bit (RDB_Register, offset 0x83C, bit[7] = 1’b0).
- Disable REC_CLK[2]: REC_CLK2_DISABLE bit (RDB_Register, offset 0x83C, bit[7] = 1’b1).

Sync_ E Auto-Clock Disable Mode

Sync_E Auto-Clock Disable mode programs the REC_CLK[1] and REC_CLK[2] outputs to drive low when the link is down. By default, the REC_CLK[1] and REC_CLK[2] output a 25 MHz clock based on the REFCLKP/ REFCLKN clock input when the link is down. Once the link is lost in Auto-Clock Switching mode, it will take approximately 200 ns for the REC_CLK[1] and REC_CLK[2] outputs to be driven low.

- Enable Auto Clock Switching mode: SYNCE_AUTO_CLK_DIS bit (RDB_Register, offset 0x83C, bit[8] = 1’b1).
- Disable Auto Clock Switching mode: SYNCE_AUTO_CLK_DIS bit (RDB_Register, offset 0x83C, bit[8] = 1’b0).

Sync_E Auto-Switch Mode

Enabling Sync_E Auto-switch mode programs the REC_CLK[1] output to switch from the primary port’s recovered clock to the secondary port’s recovered clock when link is lost on the primary port. REF_CLK[2] output is still based on the secondary port’s recovered clock.

- The primary port is determined by REC_CLK1_SEL bits (RDB_Register, offset 0x83C, bits[2:0]).
- The secondary port is determined by REC_CLK2_SEL bits (RDB_Register, offset 0x83C, bits[6:4]).

The switch over from the primary port’s recovered clock to the secondary port’s recovered clock takes approximately 240 ns after the link goes down on the primary port. By default, Sync_E Auto-Switching mode is disabled.

- Enable Sync_E Auto-Switch mode: SYNCE_AUTO_SW_MODE bit (RDB_Register, offset 0x83C, bit[9] = 1'b1).
- Disable Sync_E Auto-Switch mode: SYNCE_AUTO_SW_MODE bit (RDB_Register, offset 0x83C, bit[9] = 1'b0).

LOC_REC_CLK[1] and LOC_REC_CLK[2]

When in Sync_E Auto-Clock Disable mode:

- LOC_REC_CLK[1] signal goes high when REC_CLK[1] is locked to the primary port's recovered clock.
- LOC_REC_CLK[1] signal goes low when REC_CLK[1] is not locked to the primary port's recovered clock or the link is lost.
- LOC_REC_CLK[2] signal goes high when REC_CLK[2] is locked to the secondary port's recovered clock.
- LOC_REC_CLK[2] signal goes low when REC_CLK[1] is not locked to the secondary port's recovered clock or the link is lost.

When in Sync_E Auto-Switching mode:

- LOC_REC_CLK[1] signal goes high when REC_CLK[1] is locked to the primary port's recovered clock, or when link is lost on the primary port and link is still up on the secondary port. LOCK_REC_CLK[1] will reflect the status of the secondary port's recovered clock when link is down on the primary port.
- LOC_REC_CLK[1] signal goes low when REC_CLK[1] primary port's is not locked to recovered clock, or when the link is lost and the REC_CLK[2] secondary port is not locked to the recovered clock or link is lost.
- LOC_REC_CLK[2] signal goes high when REC_CLK[2] is locked to the secondary port's recovered clock.
- LOC_REC_CLK[2] signal goes low when REC_CLK[1] is not locked to the secondary port's recovered clock or the link is lost.

Start of Frame

When receiving packets from the line-side (copper interface), the RX_SOP signal will go high at the start-of-frame-deliminator (SFD) and remain active high until the end-of-stream-deliminator (ESD).

Receive start-of-packet signal RX_SOP is available on LED[2] by programming RDB_Register, offset 0x01E, Bits[7:4] = 0x9. Transmit start-of- packet signal TX_SOP is not available.

Caution! RX_SOP is only available on Port 0. TX_SOP is not supported.

Cleanup PLL Considerations

The input clock jitter to the B50282 must be within the following specification:

- For input clocks = 25 MHz the input clock jitter must be ≤ 1.5ps-rms @ Fj = 1 kHz to 5 MHz offset and the clock PPM must be ≤ ±50 ppm.
- For input clocks > 25 MHz the input clock jitter must be ≤ 1.5ps-rms @ Fj = 12 kHz to 20 MHz offset and the clock PPM must be ≤ ±50 ppm.

Jitter attenuators meeting this requirement include the Valpey Fisher VFJA910 and Pericom PI6CX201A.

Fast Link Drop Detection

Some Synchronous Ethernet applications may quickly require detection and recovery from link impairments. Per IEEE 802.3 Clause 40, the link drop times are:

- 1000BASE-T Master: 750 ms
- 1000BASE-T Slave: 350 ms
- 100BASE-TX: 60 µs
- 10BASE-T: 100 ms

The 1000BASE-T link drop detect times can be decreased by using the LOCAL_RCVR_STAT_CHANGE bit in the COPPER_INTERRUPT_MASK Register (RDB_Register, offset 0x00B, bit[4]) to determine a Link Fail condition within 1 ms. Setting bit[4] = 1'b0 will cause any LED ball programmed for INTR to go high when the link goes down, within 1 ms. Multiple LED balls programmed for INTR can be connected together.

Note: Using this method does not change the time it takes for the link to go down. It only provides a method of detecting a possible link-down scenario that is faster than using the LINK-Down indicators in the PHY.

EEE and AutogrEEEn must be disabled on the primary and/or secondary ports.

Section 4: Interfaces

Overview

This section describes the various interfaces that the B50282 supports.

QSGMII: Quad Serial Gigabit Media Independent Interface

The B50282 can communicate with Ethernet switches that support a Quad Serial Gigabit Media Independent Interface (QSGMII). The QSGMII transmits serial data differentially at 5 Gbaud via TDP0, TDN0, TDP1 and TDN1, and receives serial data differentially via RDP0, RDN0, RDP1, and RDN0. Each differential pair has an 80Ω to 120Ω differential impedance. The B50282 recovers the clock from the QSGMII input data. The B50282 has two QSGMII cores. Each core supports four SGMII lanes. When configured to QSGMII mode, the B50282 copper interface auto-negotiates based on Clauses 28 and 40 of IEEE 802.3. The QSGMII auto-negotiates according to 1000BASE-X auto-negotiation, as described in IEEE 802.3, Clause 37, except for a few changes to operate in QSGMII mode. The link timer is reduced to 1.6 ms and the auto-negotiation codeword is changed to reflect the copper link, copper duplex, and copper speed. QSGMII, based on the PHY port's MDI negotiation, auto-negotiates per Clause 37 in IEEE 802.3 with several modifications for QSGMII operation.

Table 5: QSGMII Interface Balls

QSGMII Signal Ball	*Description*
• RDP0 and RDN0 • RDP1 and RDN0	• QSGMII differential input for ports 0 to 3. • QSGMII differential input for ports 4 to 7. Differential 5.0 Gbaud data from the switch to the B50282. These input balls have an on-chip internal 80Ω to 120Ω differential impedance. It is highly recommended to use 0.01 µF to 0.1 µF coupling capacitors be used.
• TDP0 and TDN0 • TDP1 and TDN1	• QSGMII differential output for ports 0 to 3. • QSGMII differential output for ports 4 to 7. Differential 5.0 Gbaud output data from the B50282 to the switch.

Copper Interface

The B50282 can communicate with Link Partners that support 10BASE-T, 100BASE-TX, or 1000BASE-T. The B50282 supports auto-negotiation for 10BASE-T, 100BASE-TX, or 1000BASE-T. The B50282 supports force mode for 10BASE-T and 100BASE-TX. Force mode is not supported for 1000BASE-T operation.

The following sections describe the internal circuitry and additional features of the copper interface.

Encoder

In 10BASE-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs pre-equalization for 100m of Category 3 cabling.

In 100BASE-TX mode, the B50282 transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start-of-stream delimiter (/J/K codes) and appending an end-of-stream delimiter (/T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in “Stream Cipher” on page 32. The scrambled data is then encoded into MLT-3 signal levels.

In 1000BASE-T mode, the B50282 simultaneously transmits and receives a continuous data stream on all four pairs of the Category 5 cable. Byte-wide data from the transmit data signals are scrambled when the transmit enable is asserted, and the trellis (a PAM5 symbol on each of the four twisted-pairs) is encoded into a four-dimensional code group and then inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first two bytes of the preamble with a start-of-stream delimiter, and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier extend code groups between packets. Carrier extension is used by the switch to separate packets within a multiple-packet burst, and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data signals while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The encoding complies with IEEE 802.3ab and is fully compatible with previous versions of the Broadcom 1000BASE-T PHYs.

Decoder

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT-3 to serial non-return to zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with zeros. The decoded data is driven onto the MII receive data outputs. When an invalid code group is detected in the data stream, the B50282 asserts the MII receive error (RX_ER) signal. RX_ER is also asserted when the link fails or when the descrambler loses lock during packet reception.

In 1000BASE-T mode, the receive data stream is:

- Passed through the Viterbi decoder
- Descrambled
- Translated back into byte-wide data

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 0x00. Carrier extend codes are replaced with 0x0F or 0x1F. The decoded data is driven onto the QSGMII receive data outputs. Decoding complies with IEEE 802.3ab and is fully compatible with previous versions of Broadcom 1000BASE-T PHYs.

Link Monitor

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the following pairs for the presence of valid link pulses.

- TDP_[7:0]_[0]/TDN_[7:0]_[0]
- TDP_[7:0]_[1]/TDN_[7:0]_[1]

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the Link Fail state, and the transmission and reception of data packets are disabled. When a valid signal is detected on the receive pair for a minimum of 1 ms, the link monitor enters the Link Pass state, and the transmit and receive functions are enabled.

Following auto-negotiation in 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver's timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been good for at least 1 μs, the link monitor enters the Link Pass state, and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 ms, the link monitor enters the Link Fail state, and the transmission and reception of data packets are then disabled.

Digital Adaptive Equalizer

The digital adaptive equalizer removes Intersymbol Interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The B50282 achieves an optimum signal-to-noise ratio by using a combination of feed-forward equalization (FFE) and decision-feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than 1×10^{-12} for transmissions of: up to 100 meters on Category 5 twisted-pair cabling for 1000BASE-T and 100BASE-TX mode; up to 100 meters on Category 3 UTP cable for 10BASE-T mode. The all-digital nature of the design makes the B50282 very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

Echo Canceler

Because of the bidirectional nature of the channel in 1000BASE-T, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

Crosstalk Canceler

The B50282 transmits and receives a continuous data stream on four channels in gigabit mode. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. It is possible to cancel the effect because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

Analog-to-Digital Converter

Each receive channel has its own 125 MHz ADC that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High-power supply noise rejection
- Fast settling time
- Low bit error rate

Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T, 100BASE-TX, and 10BASE-T operation.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the reference clock input, and the receive clock is locked to the incoming data stream.

In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to the reference clock input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

Baseline Wander Correction

1000BASE-T and 100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The B50282 automatically compensates for baseline wander by removing the DC offset from the input signal, significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides a perfect DC balance.

Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT-3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses a voltage drive output that is well-balanced and produces very low-noise transmit signals.

Stream Cipher

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require that there be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive ORing the encoded serial data stream. This is done with the output of an 11-bit wide linear feedback shift register (LFSR), producing a 2047-bit non-repeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive ORing the input data byte with an 8-bit wide cipher text word. The cipher text word generates each symbol period from eight uncorrelated maximal length data sequences that are produced by linear remapping of the output of a 33-bit wide LFSR. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bit wide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The B50282 enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that inter-packet gaps containing idles or frame extensions are received at expected intervals. When the B50282 detects loss of synchronization, it notifies the link partner of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the B50282 is forced into the Link Fail state.

In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

Wire Map and Pair Skew Correction

During 1000BASE-T operation, the B50282 can automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for the following errors at the PHY's receiver:

- Wiring errors caused by the swapping of pairs within the UTP cable. It can correct for (Pair A and B swap) and (Pair C and D swap). It cannot compensate for (Pair A and D swap), (Pair A and C swap), (Pair B and C swap) or (Pair B and D swap).
- Polarity errors caused by the swapping of wires within a pair.
- Delay skews caused by UTP cable pair propagation delay differences or PCB trace length differences. The B50282 automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the cable pairs. The B50282 can tolerate delay skews of up to 64 ns long.

During 10/100 Mbps operation, the B50282 can automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for the following errors at the PHY's receiver:

- Wiring errors caused by the swapping of pairs within the UTP cable. It can correct for (Pair A and B swap).
- Polarity errors caused by the swapping of wires within a pair.

Delay skew is not an issue for 10BASE-T or 100BASE-TX, since only one pair is used in each direction.

Caution! The Twisted Pair interface connection to the RJ-45 should always be done per the IEEE 802.3 specification even though the PHY can compensate for most errors in wiring. The reason is no compensation is done on the PHY's transmitter. If a Link Partner can't compensate for pair swaps or polarity errors, then the Link Partner will never be able to link up.

Automatic MDI Crossover

During copper auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The B50282 can perform an automatic media dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the B50282 normally transmits on TDP_[7:0]_0/TDN_[7:0]_0 and receives on TDP_[7:0]_1/TDN_[7:0]_1.

When connecting to another device that does not perform MDI crossover, the B50282 automatically switches its TDP_[7:0]_0/TDN_[7:0]_0 and TDP_[7:0]_1/TDN_[7:0]_1 pairs when necessary to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The MDI Crossover State can be determined by reading RDB_Register, offset 0x001, bit[13].

- 1'b0 = Normal MDI mode
- 1'b1 = Crossover MDI mode

1000BASE-T Operation

During 1000BASE-T operation, the B50282 swaps the transmit symbols on pairs 0 and 1 and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. The automatic MDI crossover function cannot be disabled when in 1000BASE-T mode.

10/100BASE-TX Operation (Auto-Negotiation Enabled)

During 10BASE-T and 100BASE-TX operation, pair swaps automatically occur within the device and do not require user intervention. The automatic MDI crossover function by default only works when auto-negotiation is enabled. This function can be disabled during auto-negotiation by writing to RDB_Register, offset 0x000, bit[14] = 1’b1.

10/100BASE-TX Operation (Forced Mode)

The automatic MDI crossover function can also be enabled when in forced 10BASE-T or forced 100BASE-TX mode. This feature allows the user to disable the copper auto-negotiation in either 10BASE-T or 100BASE-TX and still take advantage of the automatic MDI crossover function. This feature is enabled by writing RDB_Register, offset 0x02F, bit[9] = 1’b1.

When in forced 10BASE-T or 100BASE-TX mode, the B50282 has a feature that can manually swap the MDI state when the automatic MDI crossover function is disabled. Normally the B50282 transmits on TDP_[7:0]_[0]/TDN_[7:0]_[0] and receives on TDP_[7:0]_[1]/TDN_[7:0]_[1]. To change the MDI state to transmit on TDP_[7:0]_[1]/TDN_[7:0]_[1] and receive on TDP_[7:0]_[0]/TDN_[7:0]_[0] the following steps must be done.

- Put PHY in nonlink condition.
- Enable Manual Swap MDI (Write RDB_Register, offset 0x00E, bit[7] = 1’b1).
- Set PHY into Force 10BASE-T or 100BASE-TX mode.

Note: To change the MDI state when in forced 100BASE-TX mode, the PHY must first be put into a nonlink condition.

Full-Duplex Mode

The B50282 supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable. When auto-negotiation is disabled, full-duplex operation can be enabled by setting Register 0x00, bit[8] = 1’b1.

When auto-negotiation is enabled, full-duplex capability is advertised for:

- 10BASE-T: Register 0x04, bit[6] = 1’b1
- 100BASE-TX: Register 0x04, bit[8] = 1’b1
- 1000BASE-T: Register 0x09, bit[9] = 1’b1

Master/Slave Configuration

In 1000BASE-T mode, the B50282 and its link partner perform loop timing. One end of the link must be configured as the timing master and the other end as the slave. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port the slave. Each end generates an 11-bit random seed if the two settings are equal; the end with the higher seed is configured as the master. If the local PHY and the link partner generate the same random seed, then auto-negotiation is restarted.

If both ends of the link attempt to force the same manual configuration (both master or both slave), or the random seeds match seven consecutive times, then the B50282 sets the Master/Slave Configuration Fault bit in the 1000BASE-T Status register and auto-negotiation is restarted.

For setting the B50282 to manual master/slave configuration or to set the advertised repeater/DTE configuration, see 1000BASE-T Control Register (Address 0x09).

Next Page Exchange

The 1000BASE-T configuration requires the exchange of three auto-negotiation next pages between the B50282 and its link partner. Exchange of 1000BASE-T Next Page information takes place automatically when the B50282 is configured to advertise 1000BASE-T capability.

The B50282 also supports software-controlled Next Page exchanges. When Register 0x04, bit[15] = 1’b1, all Next Page transactions are controlled through the MII management interface. This includes the three 1000BASE-T Next Pages, which are always sent first. The B50282 automatically generates the appropriate message code field for the 1000BASE-T pages. When the B50282 is not configured to advertise 1000BASE-T capability, the 1000BASE-T Next Pages are not sent.

When the B50282 is not configured to advertise 1000BASE-T capability and Register 0x04, bit[15] = 1’b0, the B50282 does not advertise Next Page ability.

Auto-Negotiation

The B50282, when configured to Copper mode, negotiates its mode of operation over the copper media using the auto-negotiation mechanism, defined in the IEEE 802.3u and 802.3ab specifications. When the auto-negotiation function is enabled, the B50282 automatically chooses the mode of operation by advertising its abilities and comparing them with those received from its link partner. The B50282 can be configured to advertise the following modes:

- 1000BASE-T full-duplex and/or half-duplex.
- 100BASE-TX full-duplex and/or half-duplex.
- 10BASE-T full-duplex and/or half-duplex.

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD). Auto-negotiation can be enabled or disabled by hardware and software control, but is always required for 1000BASE-T operation.

Ethernet@Wirespeed

Ethernet@Wirespeed is an enhancement to auto-negotiation that allows a network connection over impaired cable plants. If a link cannot be established at the highest common denominator within a set number of link attempts then the B50282 advertises the next highest advertised speed using auto-negotiation. The set number of failed link attempts is programmable. See “Changing the Number of Failed Link Attempts” on page 37 for details.

The B50282 has a link up timer that times how long the link has been up. If the link stays up for less than three seconds, then the Link-Fail Counter will get incremented. If the link stays up for greater than 5 seconds, then the Link-Fail Counter is reset to zero.

The purpose of the link up timer is to prevent scenarios where an unstable link (link is going up and down quickly) causes the B50282 to continuously try to link at a given speed and not try to downgrade and link to a lower speed. In this situation, if the link is up for less than 3 seconds, the Link-Fail Counter will get incremented. Once the Link-Fail Counter exceeds the programmable failed link attempts the B50282 will start advertising the next lowest speed and try to establish a link.

The link up timer can be bypassed by setting RDB_Register, offset 0x02F, bit[10] = 1’b1. Setting this bit causes the number of failed link attempts to get reset to zero after every link up condition, no matter how short the link up time is.

Ethernet@Wirespeed Example

At start-up the B50282 is advertising 1000BASE-T, 100BASE-TX, and 10BASE-T capabilities per Register 0x04 and Register 0x09, and the Link Partner is also advertising the same capabilities:

- If a link cannot be established within a programmable number of link attempts (two to nine) with 1000BASE-T being advertised, then an Ethernet@Wirespeed downgrade occurs, the 1000BASE-T capability is masked out on the B50282 and the next highest advertised capability (100BASE-TX) is advertised.
- If a link cannot be established within a programmable number of link attempts (two to nine) with 100BASE-TX being advertised, then an Ethernet@Wirespeed downgrade occurs, the 100BASE-TX is masked out on the B50282 and the next highest advertised capability (10BASE-T) is advertised.

- If a link cannot be established within a programmable number of link attempts (two to nine) with 10BASE-T being advertised, then an Ethernet@Wirespeed downgrade occurs and all advertising capabilities are enabled (1000BASE-T, 100BASE-TX, and 10BASE-T) on the B50282 and the whole process begins again.

Enabling/Disabling Ethernet@Wirespeed

Enabling or disabling Ethernet@Wirespeed is done on a per-port basis.

- Enable: Write RDB_Register, offset 0x02F, bit[4] = 1'b1.
- Disable: Write RDB_Register, offset 0x02F, bit[4] = 1'b0.

Removing Ethernet@Wirespeed Downgrade

Ethernet@Wirespeed downgrade can be removed by any of the following events:

- Stable link up condition for greater than 5 seconds.
- Unplug cable (no energy) for 6 seconds.
- Hardware reset.
- Software reset (Write Register 0x00, bit[15] = 1'b1).
- Disable auto-negotiation (Write Register 0x00, bit[12] = 1'b0).
- Restart auto-negotiation (Write Register 0x00, bit[9] = 1'b1).
- Disabling Wirespeed (Write RDB_Register, offset 0x02F, bit[4] = 1'b0).
- Auto-negotiation resolves to no HCD (Highest Common Denominator).

Changing the Number of Failed Link Attempts

The number of failed link attempts before downgrading to a slower speed is programmable. The number can be programmed anywhere from two to nine failed link attempts before downgrading to a lower speed. The default value is five failed link attempts. The number of failed link attempts before downgrading to a lower speed can be programmed by writing to RDB_Register, offset 0x014, bits[4:2] as shown Table 6.

Table 6: Failed Link Attempts Before Downgrade

Bits[4:2]	*Description*
0x0	Number of failed link attempts before Ethernet@Wirespeed downgrade = 2.
0x1	Number of failed link attempts before Ethernet@Wirespeed downgrade = 3.
0x2	Number of failed link attempts before Ethernet@Wirespeed downgrade = 4.
0x3	Number of failed link attempts before Ethernet@Wirespeed downgrade = 5 (default value).
0x4	Number of failed link attempts before Ethernet@Wirespeed downgrade = 6.
0x5	Number of failed link attempts before Ethernet@Wirespeed downgrade = 7.
0x6	Number of failed link attempts before Ethernet@Wirespeed downgrade = 8.
0x7	Number of failed link attempts before Ethernet@Wirespeed downgrade = 9.

Monitoring Ethernet@Wirespeed

The status of the Ethernet@ Wirespeed downgrade can be monitored through the following registers and LEDs.

- Ethernet@Wirespeed Downgrade Status (Read RDB_Register, offset 0x001, bit[14]).
- Ethernet@Wirespeed Downgrade (Read RDB_Register, offset 0x00C, bit[12]).
- Ethernet@Wirespeed Disable Gigabit Advertising (Read RDB_Register, offset 0x00C, bit[14]).
- Ethernet@Wirespeed Disable 100BASE-TX Advertising (Read RDB_Register, offset 0x00C, bit[13]).
- HCD Status (Read RDB_Register, offset 0x00C, bits[11:0]).
- Auto-negotiation HCD and Current Status (Read RDB_Register, offset 0x009, bits[10:8]).
- Ethernet@Wirespeed downgrade LED on LED[0] (Write RDB_Register, offset 0x01D, bits[3:0] = 0x9).
- Ethernet@Wirespeed downgrade LED on LED[1] (Write RDB_Register, offset 0x01D, bits[7:4] = 0x9).

Super Isolate Mode

When in Super Isolate mode, the following occurs:

- The B50282's transmitter and receiver on the Copper Media Dependent Interface are disabled. The link partner will go into a link down state since it is not receiving any FLPs, NLPs, or 100BASE-TX idles.
- The B50282's QSGMII interface will be in QSGMII auto-negotiation mode. A QSGMII link between the B50282 and the switch is established if the switch sends back an acknowledgement to the B50282 through the QSGMII auto-negotiation link codeword. If the switch does not send back an acknowledgement, the PHY remains in QSGMII auto-negotiation mode.

Hardware Enable

The B50282 has an additional hardware-strapping ball that can put the B50282 into Super Isolate mode right after a software or hardware reset. When Super Isolate mode is entered via the hardware-strapping ball, all 8 ports are affected. To enable Super Isolate mode, pull SUPER_I high at reset. The Super Isolate ball is sampled at reset and has an internal pull-down resistor. Super Isolate mode can only be disabled by software on a per port basis.

Software Enable/Disable

The B50282 can be put into Super Isolate mode on a per port basis by software.

- To enable Super Isolate mode:

  Write RDB_Register, offset 0x02A, bit[5] = 1’b1 for each of the 8 ports.
- To disable Super Isolate mode:

  Write RDB_Register, offset 0x02A, bit[5] = 1’b0 for each of the 8 ports.

Standby Power-Down Mode

The B50282 can be placed into standby Power-down mode using software commands. In this mode, all PHY functions, except for the serial management interface, are disabled. To enter standby Power-down mode, write Register 0x00, bit[11] = 1’b1. There are three ways to exit standby Power-down mode:

- Write Register 0x00, bit[11] = 1’b0 (Clear MII Control register)
- Write Register 0x00, bit[15] = 1’b1 (Software reset)
- Assert the hardware $\overline{\text{RESET}}$

Reads or writes to any MII register, other than Register 0x00 while the device is in the standby Power-down mode, returns unpredictable results. Upon exiting standby Standby Power-down mode, the B50282 remains in an internal reset state for 40 µs, and then resumes normal operation.

Auto Power-Down Mode

When the B50282 is placed into Auto Power-Down (APD) mode the chip power is reduced when the signal from the copper link partner is not present. APD mode works whether the device is in auto-negotiation enabled or in forced mode. When APD mode is enabled, the B50282 automatically enters the low-power mode when energy on the line is lost, and it resumes normal operation when energy is detected. When the B50282 is in APD mode, the copper transmitter is disabled (Sleep Cycle) for 2.7 seconds or 5.4 seconds depending on the SLEEP_TIMER_SEL bit after which the transmitter is enabled (Wake Cycle) for a duration of 84 ms to 1260 ms depending on the settings on the WAKE_UP_TIMER_SEL bits. The B50282 enters normal operation and establishes a link if energy is detected, otherwise, the Sleep and Wake-up cycles repeat.

ADP Mode Enable (Auto-Negotiation Enabled)

- Write RDB_Register, offset 0x01A, bits[6:5] = 2’b01.
- Write RDB_Register, offset 0x1A, bit[8] = 1’b’1.

ADP Mode Enable (Auto-Negotiation Disabled)

- Write RDB_Register, offset 0x01A, bits[6:5] = 2’b11.
- Write RDB_Register, offset 0x1A, bit[8] = 1’b’1.

ADP Mode Disable

- Write RDB_Register, offset 0x01A, bits[6:5] = 2’b00.

Sleep Cycle Settings

Write RDB_Register, offset 0x01A, bit[4]:

- 1’b0 = Disable copper transmitter for 2.7 seconds.
- 1’b0 = Disable copper transmitter for 5.4 seconds.

Wake Cycle Settings

Write Register RDB_Register, offset 0x01A, bits[3:0]:

- 0x1 = Enable copper transmitter for 84 ms.
- 0x2 = Enable copper transmitter for 168 ms.
- 0x3 = Enable copper transmitter for 252 ms.
- 0xF = Enable copper transmitter for 1.26s.

Management Interface

The B50282 contains a large set of PHY registers. These registers are accessible through the MDIO and MDC serial interface. The functional and electrical interface complies with IEEE Std 802.3, Section 22, and also supports MDC clock rates of up to 12.5 MHz. The management interface supports the defined Status and Control registers of IEEE Std 802.3, Clauses 22, 28, 37, 40, and 45. In addition, the B50282 contains multipurpose registers for extended software control.

Caution! The B50282's MDIO/MDC will respond to Clause 45 transactions. If a Clause 45 device is on the same MDIO/MDC interface, make sure the Clause 45 devices's PHY address does not overlap with any of the B50282's PHY addresses.

MDIO/MDC Access

The B50282 has eight unique PHY addresses and one OSGMII PHY address for MDIO MII management. The default addresses depend on PHYA[4:0], MDIO_SEL[2:1] and PHYA_REV. Table 7 and Table 8 on page 42 show the various MDIO accesses modes that are supported.

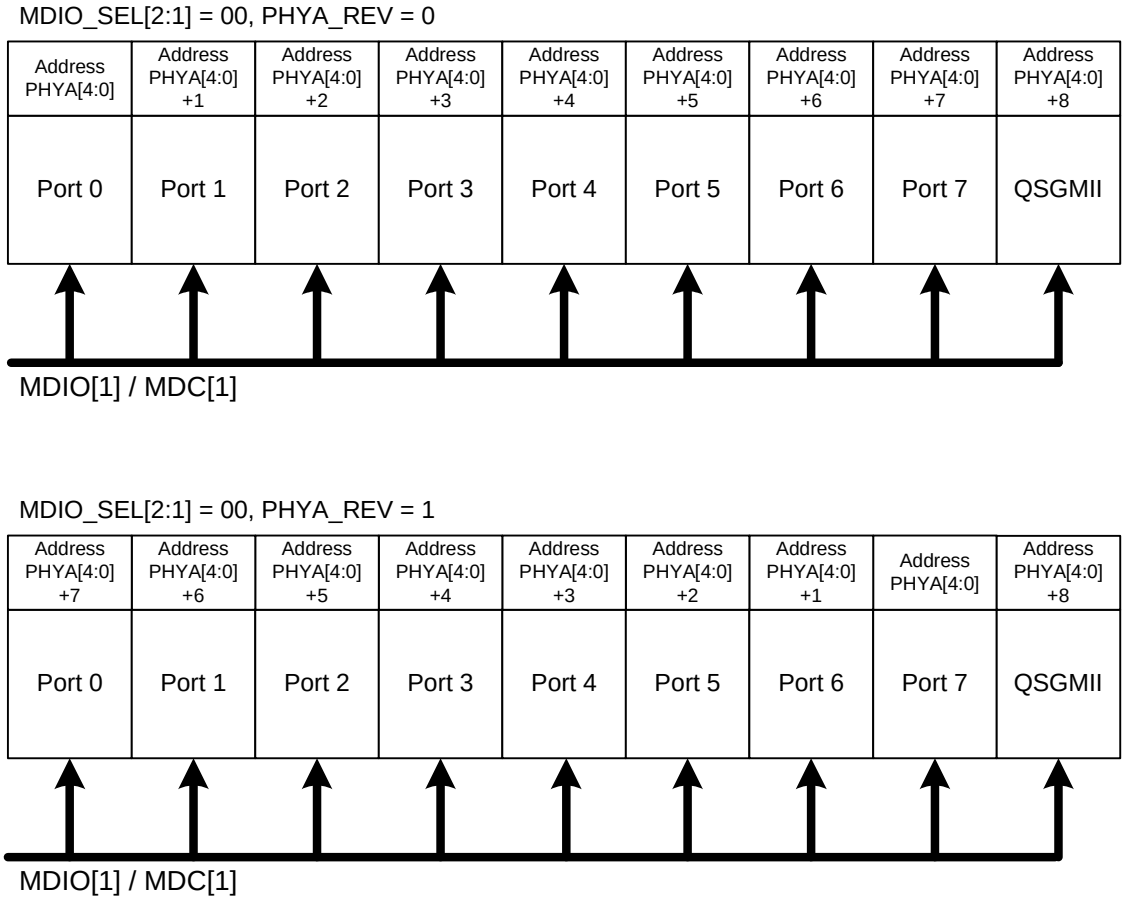
Table 7: MDIO_SEL[2:1] = 00

MDIO_SEL[2:1]	*PHYA_REV*	*Description*
00	0	**MDIO[1]/MDC[1]:** Port 0 to Port 7 and QSGMII. **MDIO[2]/MDC[2]:** Not used. • Port 0 PHY Address = PHYA[4:0] • Port 1 PHY Address = PHYA[4:0] + 1 • Port 2 PHY Address = PHYA[4:0] + 2 • Port 3 PHY Address = PHYA[4:0] + 3 • Port 4 PHY Address = PHYA[4:0] + 4 • Port 5 PHY Address = PHYA[4:0] + 5 • Port 6 PHY Address = PHYA[4:0] + 6 • Port 7 PHY Address = PHYA[4:0] + 7 • QSGMII Address = PHYA[4:0] + 8 See Figure 6 on page 41.
00	1	**MDIO[1]/MDC[1]:** Port 0 to Port 7 and QSGMII. **MDIO[2]/MDC[2]:** Not used. • Port 0 PHY Address = PHYA[4:0]+ 7 • Port 1 PHY Address = PHYA[4:0] + 6 • Port 2 PHY Address = PHYA[4:0] + 5 • Port 3 PHY Address = PHYA[4:0] + 4 • Port 4 PHY Address = PHYA[4:0] + 3 • Port 5 PHY Address = PHYA[4:0] + 2 • Port 6 PHY Address = PHYA[4:0] + 1 • Port 7 PHY Address = PHYA[4:0] • QSGMII Address = PHYA[4:0] + 8 See Figure 6 on page 41.

Table 7: MDIO_SEL[2:1] = 00

MDIO_SEL[2:1]	*PHYA_REV*	*Description*
Note: The QSGMII address can be programmed to share Port 3's PHY address (PHYA[4:0] + 3) by setting RDB_Register, offset 0x810, bit[3:2] = 2'b11. Since accesses to the QSGMII will be minimal, this option will save one PHY address.		

Figure 6: MDIO_SEL[2:1] = 2'b00

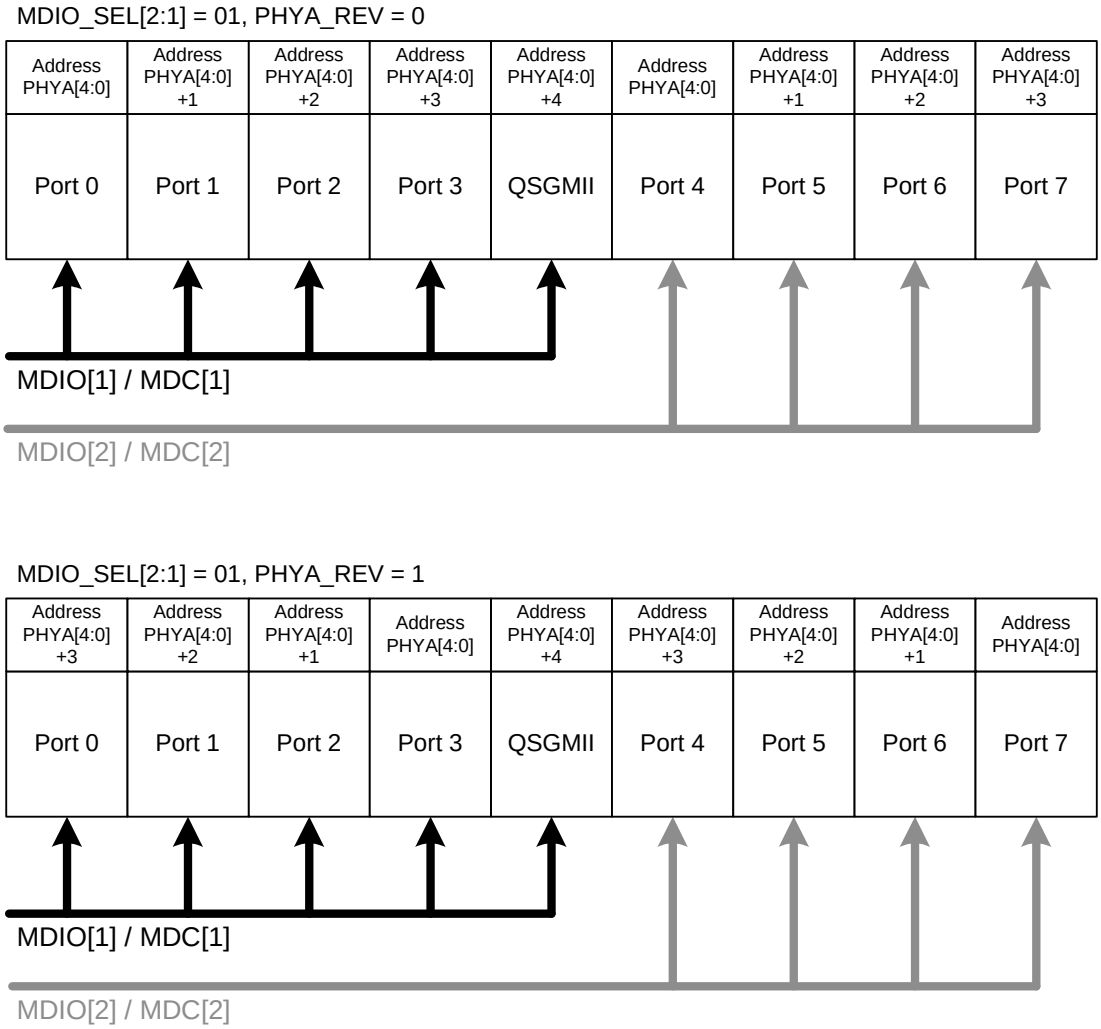


Note*:* The QSGMII PHY address can optionally be programmed to share Port 3's PHY address.

Table 8: MDIO_SEL[2:1] = 01

MDIO_SEL[2:1]	*PHYA_REV*	*Description*
01	0	**MDIO[1]/MDC[1]:** Port 0 to Port 3 and QSGMII. • Port 0 PHY Address = PHYA[4:0] • Port 1 PHY Address = PHYA[4:0] + 1 • Port 2 PHY Address = PHYA[4:0] + 2 • Port 3 PHY Address = PHYA[4:0] + 3 • QSGMII Address = PHYA[4:0] + 4 **MDIO[2]/MDC[2]:** Port 4 to Port 7. • Port 4 PHY Address = PHYA[4:0] • Port 5 PHY Address = PHYA[4:0] + 1 • Port 6 PHY Address = PHYA[4:0] + 2 • Port 7 PHY Address = PHYA[4:0] + 3 See Figure 7 on page 43.
01	1	**MDIO[1]/MDC[1]:** Port 0 to Port 7 and QSGMII. • Port 0 PHY Address = PHYA[4:0] +3 • Port 1 PHY Address = PHYA[4:0] + 2 • Port 2 PHY Address = PHYA[4:0] + 1 • Port 3 PHY Address = PHYA[4:0] • QSGMII Address = PHYA[4:0] + 4 **MDIO[2]/MDC[2]:** Port 4 to Port 7. • Port 4 PHY Address = PHYA[4:0]+ 3 • Port 5 PHY Address = PHYA[4:0] + 2 • Port 6 PHY Address = PHYA[4:0] + 1 • Port 7 PHY Address = PHYA[4:0] See Figure 7 on page 43.
Note: The QSGMII address can be programmed to share Port 3's PHY address (PHYA[4:0] + 4) by setting RDB_Register, offset 0x810, bit[3:2] = 2'b11. Since accesses to the QSGMII will be minimal, this option will save one PHY address.		

Figure 7: MDIO_SEL[2:1] = 2'b01

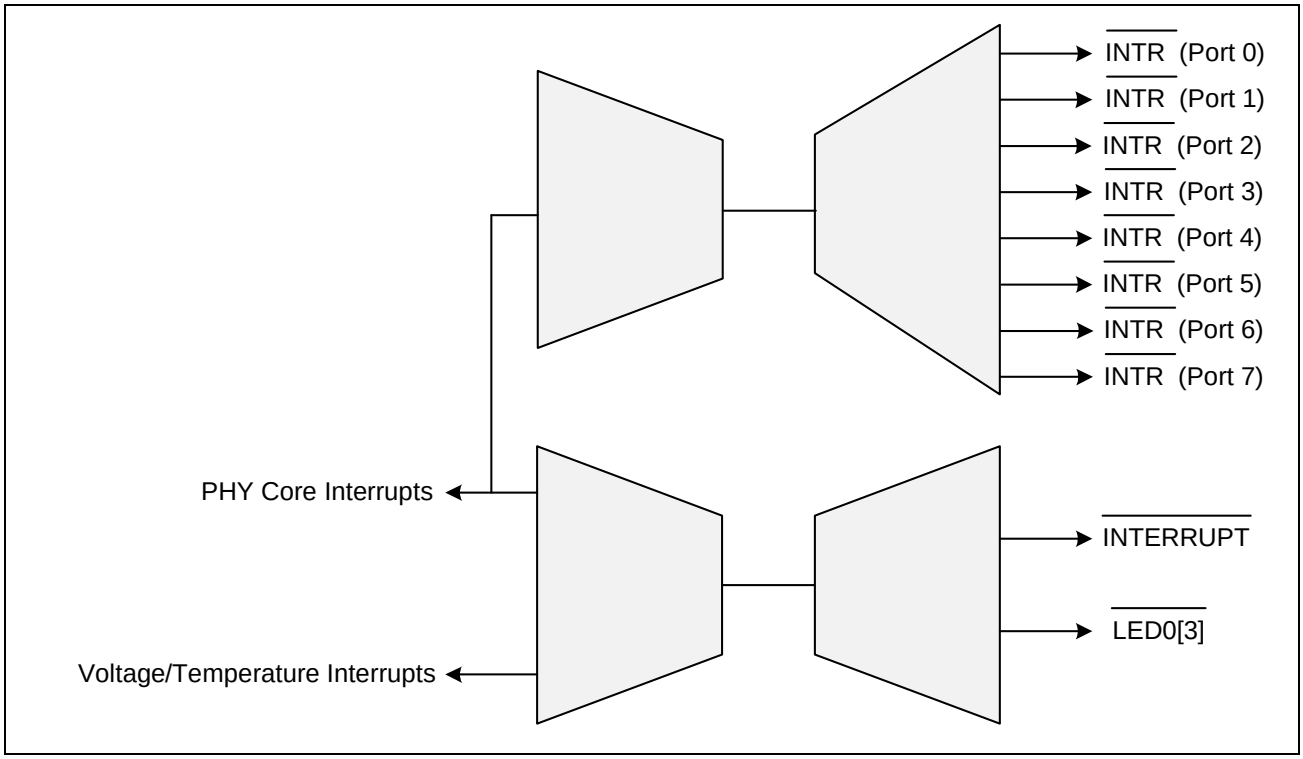


Note: The QSGMII PHY address can optionally be programmed to share Port 3's PHY address.

Interrupt Interface

The B50282 supports three types of interrupt sources and three types of interrupt outputs. Figure 8 shows a simplified interrupt block diagram.

Figure 8: Simplified Interrupt Block Diagram



Interrupt Sources

- PHY core interrupts.
- Voltage/temperature monitor interrupts.

Interrupt Outputs

- Interrupts on any LED programmed to $\overline{\text{INTR}}$ mode.
  - Only PHY Core interrupts are supported.
  - Enabled on a per port basis.
- Interrupts on the $\overline{\text{INTERRUPT}}$.
  - Ability to enable or disable any of the following interrupt sources: PHY Core, Voltage/Temperature interrupts.
  - Global interrupt for all ports.
- Interrupts on Port 0's $\overline{\text{LED0[3]}}$ when programmed to $\overline{\text{INTERRUPT}}$ mode.
  - Behaves exactly the same way as the $\overline{\text{INTERRUPT}}$.

PHY Core Interrupts

PHY Core interrupts can be programmed to be outputted to the following balls:

- LED programmed to $\overline{\text{INTR}}$
- $\overline{\text{INTERRUPT}}$
- $\overline{\text{LED0[3]}}$: (Port 0, $\overline{\text{LED[3]}}$) programmed to $\overline{\text{INTERRUPT}}$ mode

To program the PHY Core interrupts on LED programmed to $\overline{\text{INTR}}$, do the following register writes:

- RDB_Register, offset 0x01D, bits[3:0] = 0x6 (enable $\overline{\text{INTR}}$ on $\overline{\text{LED[0]}}$).
- RDB_Register, offset 0x01D, bits[7:4] = 0x6 (enable $\overline{\text{INTR}}$ on $\overline{\text{LED[1]}}$).
- RDB_Register, offset 0x01E, bits[3:0] = 0x6 (enable $\overline{\text{INTR}}$ on $\overline{\text{LED[2]}}$).
- RDB_Register, offset 0x01E, bits[7:4] = 0x6 (enable $\overline{\text{INTR}}$ on $\overline{\text{LED[3]}}$).

Note: Only one LED per port should be programmed for the $\overline{\text{INTR}}$, since all the LEDs for that port will behave exactly the same.

Note: Interrupts are done on a per port basis when $\overline{\text{INTR}}$ is used.

To program the PHY Core interrupts on the $\overline{\text{INTERRUPT}}$, do the following register writes:

- RDB_Register, offset 0x82D, bit[4] = 1’b0 (enable PHY Core interrupts on $\overline{\text{INTERRUPT}}$ for Port 0).
- RDB_Register, offset 0x82D, bit[5] = 1’b0 (enable PHY Core interrupts on $\overline{\text{INTERRUPT}}$ for Port 1).
- RDB_Register, offset 0x82D, bit[6] = 1’b0 (enable PHY Core interrupts on $\overline{\text{INTERRUPT}}$ for Port 2).
- RDB_Register, offset 0x82D, bit[7] = 1’b0 (enable PHY Core interrupts on $\overline{\text{INTERRUPT}}$ for Port 3).
- RDB_Register, offset 0x82D, bit[8] = 1’b0 (enable PHY Core interrupts on $\overline{\text{INTERRUPT}}$ for Port 4).
- RDB_Register, offset 0x82D, bit[9] = 1’b0 (enable PHY Core interrupts on $\overline{\text{INTERRUPT}}$ for Port 5).
- RDB_Register, offset 0x82D, bit[10] = 1’b01 (enable PHY Core interrupts on $\overline{\text{INTERRUPT}}$ for Port 6).
- RDB_Register, offset 0x82D, bit[11] = 1’b0 (enable PHY Core interrupts on $\overline{\text{INTERRUPT}}$ for Port 7).

To program the PHY Core interrupts on the $\overline{\text{LED0[3]}}$, do the following register writes:

- RDB_Register, offset 0x811, bit[7] = 1’b1 (enable $\overline{\text{INTERRUPT}}$ mode on $\overline{\text{LED0[3]}}$).
- RDB_Register, offset 0x82E, bit[4] = 1’b0 (enable PHY Core interrupts on $\overline{\text{LED0[3]}}$ for Port 0).
- RDB_Register, offset 0x82E, bit[5] = 1’b0 (enable PHY Core interrupts on $\overline{\text{LED0[3]}}$ for Port 1).
- RDB_Register, offset 0x82E, bit[6] = 1’b0 (enable PHY Core interrupts on $\overline{\text{LED0[3]}}$ for Port 2).
- RDB_Register, offset 0x82E, bit[7] = 1’b0 (enable PHY Core interrupts on $\overline{\text{LED0[3]}}$ for Port 3).
- RDB_Register, offset 0x82E, bit[8] = 1’b0 (enable PHY Core interrupts on $\overline{\text{LED0[3]}}$ for Port 4).
- RDB_Register, offset 0x802E, bit[9] = 1’b0 (enable PHY Core interrupts on $\overline{\text{LED0[3]}}$ for Port 5).
- RDB_Register, offset 0x82E, bit[10] = 1’b0 (enable PHY Core interrupts on $\overline{\text{LED0[3]}}$ for Port 6).
- RDB_Register, offset 0x82E, bit[11] = 1’b0 (enable PHY Core interrupts on $\overline{\text{LED0[3]}}$ for Port 7).

Determining/Clearing PHY Core Interrupt

The port that generated the interrupt can be determined by reading RDB_Register, offset 0x03B, bits[7:0].

- Bit[7] = 1'b1: Interrupt generated on Port 7.
- Bit[6] = 1'b1: Interrupt generated on Port 6.
- Bit[5] = 1'b1: Interrupt generated on Port 5.
- Bit[4] = 1'b1: Interrupt generated on Port 4.
- Bit[3] = 1'b1: Interrupt generated on Port 3.
- Bit[2] = 1'b1: Interrupt generated on Port 2.
- Bit[1] = 1'b1: Interrupt generated on Port 1.
- Bit[0] = 1'b1: Interrupt generated on Port 0.

The cause of the interrupt(s) and the clearing of the interrupt(s) is done by reading the following registers:

- COPPER_INTERRUPT_STATUS Register: RDB_Register, offset 0x00A.
- EXPANSION_INTERRUPT_STATUS Register: RDB_Register, offset 0x031, bit[15].

Voltage/Temperature Monitor Interrupts

Table 9 shows the Voltage/Temperature interrupt mask registers. Voltage/Temperature interrupts can be programmed to be outputted on the $\overline{\text{INTERRUPT}}$, and/or $\overline{\text{LED0[3]}}$ programmed to $\overline{\text{INTERRUPT}}$ mode. Interrupt output on LEDs programmed to $\overline{\text{INTR}}$ are not supported.

To program the Voltage/Temperature interrupts on the $\overline{\text{INTERRUPT}}$, perform the following register writes:

- RDB_Register, offset 0x82D, bit[3] = 1'b0 (Enable Voltage/Temperature Interrupts on $\overline{\text{INTERRUPT}}$.

To program the Voltage/Temperature interrupts on the $\overline{\text{LED0[3]}}$, perform the following register writes:

- RDB_Register, offset 0x811, bit[7] = 1'b1 (Enable $\overline{\text{INTERRUPT}}$ mode on $\overline{\text{LED0[3]}}$).
- RDB_Register, offset 0x82E, bit[3] = 1'b0 (Enable Voltage/Temperature Monitor Interrupts).

Determining/Clearing Voltage/Temperature Interrupts

The cause of the interrupt(s) and the clearing of the interrupt(s) is done by reading the VOLT_TEMP_MONITOR Register: RDB_Register, offset 0x83B, bits[2:0].

Table 9: Voltage/Temperature Interrupts

Interrupt Name	*Register*	*Comments*
VTMON_V3P3_2P5_INTR_MASK	VOLT_TEMP_MONITOR Register RDB_Register, offset 0x83B, bit[10] VOLT_TEMP_MONITOR Register RDB_Register, offset 0x83B, bit[2]	Voltage supply 3.3V/2.5V monitor interrupt. Voltage is out of threshold settings since last read. • High threshold is set by RDB_Register, offset 0x8039, bits[9:0]. • Low threshold is set by RDB_Register, offset 0x83A, bits[9:0].

Table 9: Voltage/Temperature Interrupts (Cont.)

Interrupt Name	*Register*	*Comments*
VTMON_V1P0_INTR_MASK	VOLT_TEMP_MONITOR Register RDB_Register, offset 0x83B, bit[9] VOLT_TEMP_MONITOR Register RDB_Register, offset 0x83B, bit[1]	Voltage supply 1.0V monitor interrupt. Voltage is out of threshold settings since last read. • High threshold is set by RDB_Register, offset 0x836, bits[9:0]. • Low threshold is set by RDB_Register, offset 0x837, bits[9:0].
VTMON_TEMP_INTR_MASK	VOLT_TEMP_MONITOR RDB_Register, offset 0x83B, bit[8] VOLT_TEMP_MONITOR Register RDB_Register, offset 0x83B, bit[0]	Temperature is out of threshold settings since last read. • High threshold is set by RDB_Register, offset 0x833, bits[9:0]. • Low threshold is set by RDB_Register, offset 0x834, bits[9:0].

LED Interface

The B50282 supports the following LED modes:

- “Parallel LED Mode” on page 47
- “Constant Current LED Mode” on page 48
- “Legacy Constant Current LED Mode” on page 48

Each port supports up to four LEDs: LED[0], LED[1], LED[2], and LED[3].

Parallel LED Mode

The B50282 has four programmable LED balls per port that perform different functions. Each of the B50282 LEDs can be individually programmed to any one of the many LED modes on a per port basis. The available LED modes are:

- LINKSPD1
- $\overline{\text{LINKSPD2}}$
- $\overline{\text{XMITLED}}$
- $\overline{\text{ACTIVITY}}$
- $\overline{\text{FDXLED}}$
- $\overline{\text{SLAVE}}$
- $\overline{\text{INTR}}$
- $\overline{\text{QUALITY}}$
- $\overline{\text{RCVLED}}$

- $\overline{\text{WIRESPEED DOWNGRADE}}$
- $\overline{\text{MULTICOLOR[1]}}$
- $\overline{\text{MULTICOLOR[2]}}$
- $\overline{\text{CABLE DIAG}}$ (Open/Short found)
- $\overline{\text{ON}}$
- $\overline{\text{OFF}}$

Any LED programmed for the above modes, except for $\overline{\text{INTR}}$ LED, behave as active low push-pull outputs. Any LED programmed to $\overline{\text{INTR}}$ behaves as an active low open-drain output. The LEDs can be programmed through RDB_Register, offset 0x01D and RDB_Register, offset 0x01E.

Constant Current LED Mode

Constant Current LED mode allows the LED output balls to output a constant current ranging from 2 mA to 16 mA in 2 mA increments. There is no need for external series resistors since the amount of current through the LEDs is programmable. The amount of current is set by the LED_PROGRAMMABLE_CURRENT_MODE_CONTROL Register (RDB_Register, offset 0x074, bits[15:0]).

Constant Current LED mode can be enabled for all ports through hardware, by setting the CRNT_LED_EN = OVDD. Constant Current LED Mode can be enabled or disabled on an individual LED basis by writing to RDB_Register, offset 0x01F, bits[3:0] for each port. Bit[3] controls LED[3], bit[2] controls LED[2], bit[1] controls LED[1], and bit[0] controls LED[0].

Legacy Constant Current LED Mode

Legacy Constant Current LED Mode allows the LEDs programmed in Parallel LED mode to output a constant current ranging from 2 mA to 16 mA in 2 mA increments Legacy Constant Current LED mode. The amount of current is set by RDB_Register, offset 0x074, bits[15:0].

Legacy Constant Current LED Mode is enabled by setting the CRNT_LED_EN = OVDD and setting RDB_Register, offset 0x820, bit[15] = 1’b1. Legacy Constant Current LED Mode can be disabled on an individual LED basis by writing to RDB_Register, offset 0x01F, bits[3:0] for each port. Bit[3] controls LED[3], bit[2] controls LED[2], bit[1] controls LED[1], and bit[0] controls LED[0].

Note: Legacy Constant Current LED Mode cannot be used for LEDs programmed for $\overline{\text{INTR}}$.

If the $\overline{\text{INTR}}$ function is needed, then the LED programmed for $\overline{\text{INTR}}$ must have Constant Current LED Mode disabled by writing to RDB_Register, offset 0x01F, bits[3:0].

Section 5: Ball Descriptions

The following conventions are used to identify the I/O types in Table 11 on page 50. The I/O ball type is useful in referencing the DC ball characteristics contained in Section 10: “Electrical Characteristics”.

Table 10: I/O Signal Type Definitions

Abbreviation	*Description*
I_D	LVCMOS input
I_{PU}	Input with internal pull-up resistor
I_{PD}	Input with internal pull-down resistor
I_{CS}	Input continuously sampled
I_{SOR}	Input sampled on reset
I_{ST}	Schmitt trigger input
I_{3T}	3.3V tolerant input
I/O	Bidirectional
O	Output
O_T	Tristateable output
O_D	LVCMOS output
O_{OD}	Open drain output
O_{OC}	Open collector output
A	Analog ball type
B	Bias ball type
Q	QSGMII ball type
XYZ	Active low signal
DNC	Do not connect
NC	No connect
PWR	Power ball
GND	Ground ball

Table 11: Ball Descriptions

Label	*I/O*	*Description*
Twisted-Pair Interface Connection		
In 1000BASE-T mode, differential data from the media is transmitted and received on all four signal pairs. The Twisted-Pair interface uses the following format: TDx_y_z. • TD is the Twisted-Pair Interface. • x is either polarity P = Positive or N = Negative. • y is the Port Number (0 to 7). • z is the pair (channel) number (0 to 3). ***Note:*** These balls have internal 50Ω series termination resistors. There is no need for external termination resistors. ***Note:*** Any unused pairs can be left floating.		
TDP_0_0, TDN_0_0 TDP_0_1, TDN_0_1 TDP_0_2, TDN_0_2 TDP_0_3, TDN_0_3	I/O_A	**Port 0 Copper Interface.**
TDP_1_0, TDN_1_0 TDP_1_1, TDN_1_1 TDP_1_2, TDN_1_2 TDP_1_3, TDN_1_3	I/O_A	**Port 1 Copper Interface.**
TDP_2_0, TDN_2_0 TDP_2_1, TDN_2_1 TDP_2_2, TDN_2_2 TDP_2_3, TDN_2_3	I/O_A	**Port 2 Copper Interface.**
TDP_3_0, TDN_3_0 TDP_3_1, TDN_3_1 TDP_3_2, TDN_3_2 TDP_3_3, TDN_3_3	I/O_A	**Port 3 Copper Interface.**
TDP_4_0, TDN_4_0 TDP_4_1, TDN_4_1 TDP_4_2, TDN_4_2 TDP_4_3, TDN_4_3	I/O_A	**Port 4 Copper Interface.**
TDP_5_0, TDN_5_0 TDP_5_1, TDN_5_1 TDP_5_2, TDN_5_2 TDP_5_3, TDN_5_3	I/O_A	**Port 5 Copper Interface.**
TDP_6_0, TDN_6_0 TDP_6_1, TDN_6_1 TDP_6_2, TDN_6_2 TDP_6_3, TDN_6_3	I/O_A	**Port 6 Copper Interface.**

Table 11: Ball Descriptions (Cont.)

Label	I/O	Description
TDP_7_0, TDN_7_0 TDP_7_1, TDN_7_1 TDP_7_2, TDN_7_2 TDP_7_3, TDN_7_3	I/O_A	**Port 7 Copper Interface.**
QSGMII Interface		
The QSGMII receive interface uses the following format: RDyz. • y is either the polarity. P = Positive, N = Negative. • z is the QSGMII quad number (0 to 1). The QSGMII transmit interface uses the following format: TDyz. • y is either the polarity. P = Positive, N = Negative. • z is the QSGMII quad number (0 to 1).		
RDP0, RDN0 RDP1, RDN1	I_Q	**QSGMII Interface Data Input.** Differential serial data input when the B50282 is in QSGMII mode. Data flow is from switch's QSGMII output to PHY's QSGMII input. • RDP0 and RDN0 support Ports 0, 1, 2, and 3. • RDP1 and RDN1 support Ports 4, 5, 6, and 7. ***Note:*** Each differential pair has an 80Ω to 120Ω differential impedance. it is highly recommended to use 0.1 µF to 0.01 µF coupling capacitors.
TDP0, TDN0 TDP1, TDN1	O_Q	**QSGMII Interface Data Output.** Differential serial data output when the B50282 is in QSGMII mode. Data flow is from PHY's QSGMII output to switch's QSGMII input. • TDP0 and TDN0 supports Ports 0, 1, 2, and 3. • TDP1 and TDN1 supports Ports 4, 5, 6, and 7.
MDIO/MDC Interface		
V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by OVDDMDIO. See Section 10: "Electrical Characteristics".		
MDIO[1] MDIO[2]	$I/O_{PU, CS, D}$	**Management Data I/O.** This serial management input/output is used to read from and write to the MII registers. The data value is valid and latched on the rising edge of MDC. These balls can operate at either 1.2V, 2.5V or 3.3V depending on the MDIO_LVL and OVDDMDIO settings listed below. • 1.2V operation: MDIO_LVL = 0, OVDDMDIO = 1.2V. • 2.5V operation: MDIO_LVL = 1, OVDDMDIO = 2.5V. • 3.3V operation: MDIO_LVL = 1, OVDDMDIO = 3.3V. ***Note:***
MDC[1] MDC[2]	$I_{PD, CS, ST}$	**Management Data Clock.** The MDC clock input must be provided to allow MII management functions. Clock frequencies of up to 12.5 MHz are supported. These balls can operate at either 1.2V, 2.5V or 3.3V depending on the MDIO_LVL and OVDDMDIO settings listed below. • 1.2V operation: MDIO_LVL = 0, OVDDMDIO = 1.2V. • 2.5V operation: MDIO_LVL = 1, OVDDMDIO = 2.5V. • 3.3V operation: MDIO_LVL = 1, OVDDMDIO = 3.3V. ***Note:***

Table 11: Ball Descriptions (Cont.)

Label	I/O	Description
MDIO/MDC Configuration		
V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by OVDD. See Section 10: "Electrical Characteristics".		
MDIO_LVL	I_{PU}	**MDIO/MDC Supply Level.** Sets the voltage the OVDDMDIO ball can operate at. • MDIO_LVL = 0: OVDDMDIO operates at 1.2V. • MDIO_LVL = 1: OVDDMDIO can operate at either 2.5V or 3.3V.
MDIO_SEL[1] MDIO_SEL[2]	$I_{PD, CS, D}$	**Management Data I/O Select.** Active high. Selects MDIO access method. See "Management Interface" on page 40.
PHYA[0] PHYA[1] PHYA[2] PHYA[3] PHYA[4]	$I_{PD, SOR, D}$	**PHY Address Select.** Active high. Sets the MII management PHY address. See "Management Interface" on page 40.
PHYA_REV	$I_{PD, SOR, D}$	**PHY Address Reverse.** Active high. When pulled high at reset, the PHY address the ports responds to is reversed. See "Management Interface" on page 40.
JTAG		
Note: V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by OVDDJTAG.		
$\overline{TRST}$	$I_{ST, PD, CS, D}$	**JTAG Reset.** Active-low. Resets the JTAG controller. This input must be pulled low during normal operation.
TDI	$I_{PU, CS, D}$	**JTAG Test Data Input.** Active-high. JTAG serial data input.
TCK	$I_{PU, CS, D}$	**JTAG Test Clock.** Active-high. JTAG serial clock input.
TMS	$I_{PU, CS, D}$	**JTAG Test Mode Select.** Active-high. JTAG mode select input.
TDO	$O_{T, D}$	**JTAG Test Data Output.** JTAG serial data output.
Test		
Note: V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by OVDD. See Section 10: "Electrical Characteristics".		
TEST[0] TEST[1]	$I_{PD, CS, D}$	**Test Mode Enables.** Active high. These balls must always be pulled low during normal operation. Pulling both balls high tristates all outputs. These balls are used by Broadcom for test purposes only. These balls should be tied to ground.
TVCO[1] TVCO[2]	O_A	**Transmit Test Clock.** 125 MHz transmit test clock used for IEEE conformance testing.

Table 11: Ball Descriptions (Cont.)

Label	I/O	Description
Reference Clock Configuration		
Note: V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by OVDD. See Section 10: "Electrical Characteristics".		
SCLK_TYPE[0] SCLK_TYPE[1]	I_{PD}, SOR, D	**Reference Clock Type.** Active high. Selects the type of reference clock REFCLKP and REFCLKN will accept. See "Reference Clock Using REFCLKP/N" on page 70. SCLK_TYPE[1:0] • 00 = CML Differential Clock Input on REFCLKP and REFCLKN. • 01 = Single-ended CMOS input on REFCLKP. • 10 = Crystal input on REFCLKP and REFCLKN. • 11 = NA.
SCLK_FREQ[0] SCLK_FREQ[1]	I_{PD}, SOR, D	**Reference Clock Frequency.** Active high. Selects the frequency the input reference clock. See "Reference Clock Using REFCLKP/N" on page 70. SCLK_FREQ[1:0] • 00 = 25 MHz • 01 = 125 MHz • 10 = 312.5 MHz • 11 = 156.25 MHz
Reference Clock Inputs		
Note: V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by CLKVDD. See Section 10: "Electrical Characteristics"		
REFCLKP REFCLKN	I_A	**Reference Clock Inputs.** configure REFCLKP and REFCLKP to accept differential, single-ended or crystal clock sources depending on the configuration of the balls listed below: • SCLK_TYPE[1:0] • SCLK_FREQ[1:0] See "Reference Clock Using REFCLKP/N" on page 70 for details.
Synchronous Ethernet		
Note: V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by OVDD. See Section 10: "Electrical Characteristics".		
REC_CLK[1] REC_CLK[2]	O_T	**Recovered Clock Output.** The recovery clock from the line-side link partner can be multiplexed onto the REC_CLK[1] and or REC_CLK[2] for Synchronous Ethernet applications. See "Synchronous Ethernet" on page 22.
LOC_REC_CLK[1] LOC_REC_CLK[2]	O_T	**PLL Reference Clock Lock.** Active high. When high, Indicates the recovered clock is locked to the incoming signal. These signals do not indicate the quality of the recovered clock. See "Synchronous Ethernet" on page 22. • LOC_REC_CLK[1]: Indicates REC_CLK[1] has achieved lock with the incoming signal. • LOC_REC_CLK[2]: Indicates REC_CLK[2] has achieved lock with the incoming signal.

Table 11: Ball Descriptions (Cont.)

Label	I/O	Description
Reset		
Note: V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by OVDD. See Section 10: "Electrical Characteristics".		
$\overline{\text{RESET}}$	$I_{PU, CS, ST, D}$	**Reset.** Active low. Resets the B50282. At reset, all internal registers are restored to the default state and reconfigured based on hardware configuration signals.
Twisted-Pair Media Configuration		
Note: V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by OVDD. See Section 10: "Electrical Characteristics".		
ANEN	$I_{PU, SOR, D}$	**Auto-negotiation Select.** Active high. When high, auto-negotiation is enabled; when low, auto-negotiation is disabled. After reset, the auto-negotiation function is under software control. This ball works in conjunction with the FDX, and SPD0 to set up the default duplex and speed of the twisted-pair interface.
SPD0	$I_{PD, SOR, D}$	**Speed Select.** Active high. Sets the default advertisement of the B50282, according to the following table. **ANEN** **SPD0** **Description** 0 X Force 1000BASE-T (See Note below) 1 0 Auto-negotiate advertise: 10/100/1000BASE-T 1 1 Auto-negotiate advertise: 1000BASE-T ***Note:*** FORCE 1000BASE-T mode is for test purposes only, and disabling auto-negotiation can lead to link-configuration mismatches and no-link situations. The *Annex 28D.5 Extensions Required for Clause 40 (1000BASE-T)* IEEE 802.3 specification requires that auto-negotiation be used in 1000BASE-T operation. There are no standards that govern a protocol for 1000BASE-T operation without auto-negotiation. Broadcom recommends enabling and using auto-negotiation. For systems that only need 1000BASE-T functionality, Broadcom recommends enabling auto-negotiation with only 1000BASE-T being advertised, and that the advertising bits for all other modes be disabled.
FDX	$I_{PU, SOR, D}$	**Full-duplex Select.** Active high**.** This input sets the default value of the Copper Interface Manual Duplex Mode bit in the MII Control register 0x00, bit[8]. This ball also sets the default value of the auto-negotiation advertised abilities for 10BASE-T, 100BASE-TX, and 1000BASE-T full-duplex capability. After reset, all duplex mode bits are under software control.
HUB	$I_{PD, SOR, D}$	**Repeater Select.** Active high. This input sets the default value of both the Hub/DTE bit and the master/slave configuration value bit in 1000BASE-T Control register (0x09, bits[11:10]) After reset, both bits are under software control.

Table 11: Ball Descriptions (Cont.)

Label	*I/O*	*Description*
Misc. Configuration		
Note: V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by OVDD. See Section 9: "Timing and AC Characteristics".		
SUPER_I	$I_{PD, CS, D}$	**Super Isolate Select.** Active high. Enable Super Isolate mode for all copper ports when pulled high. See "Super Isolate Mode" on page 38.
CRNT_LED_EN	$I_{PU, CS, D}$	**Constant Current LED Mode Enable.** Active high. Enables Constant Current LED Mode for all LED balls when pulled high or left floating. See "Constant Current LED Mode" on page 48 for details.
INTERRUPT	O_{PU}	**Interrupt.** Active low output with an internal pull-up resistor. Indicates the combined interrupt status of all ports.
LEDS		
These LEDs can be used when in: • Parallel LED mode • Constant Current LED mode • Legacy Constant Current LED mode		
Note: V_{OH}, V_{OL}, V_{IH} and V_{IL} values are set by OVDD. See Section 10: "Electrical Characteristics".		
LED0[0] LED0[1] LED0[2] LED0[3]	I/O	**Port 0 LEDs.** Active-low. ***Note:*** **LED0[3]** can be programmed to INTERRUPT mode. See "Interrupt Interface" on page 44. ***Note:***
LED1[0] LED1[1] LED1[2]	I/O	**Port 1 LEDs.** Active-low. ***Note:***
LED2[0] LED2[1] LED2[2]	I/O	**Port 2 LEDs.** Active-low. ***Note:***
LED3[0] LED3[1] LED3[2]	I/O_T	**Port 3 Status LEDs.** ***Note:*** Active-low. ***Note:***
LED4[0] LED4[1] LED4[2]	I/O	**Port 4 LEDs.** ***Note:*** Active-low. ***Note:***
LED5[0] LED5[1] LED5[2]	I/O	**Port 5 LEDs.** ***Note:*** Active-low. ***Note:***
LED6[0] LED6[1] LED6[2]	I/O	**Port 6 LEDs.** Active-low. ***Note:***
LED7[0] LED7[1] LED7[2]	I/O	**Port 7 LEDs.** Active-low. ***Note:***

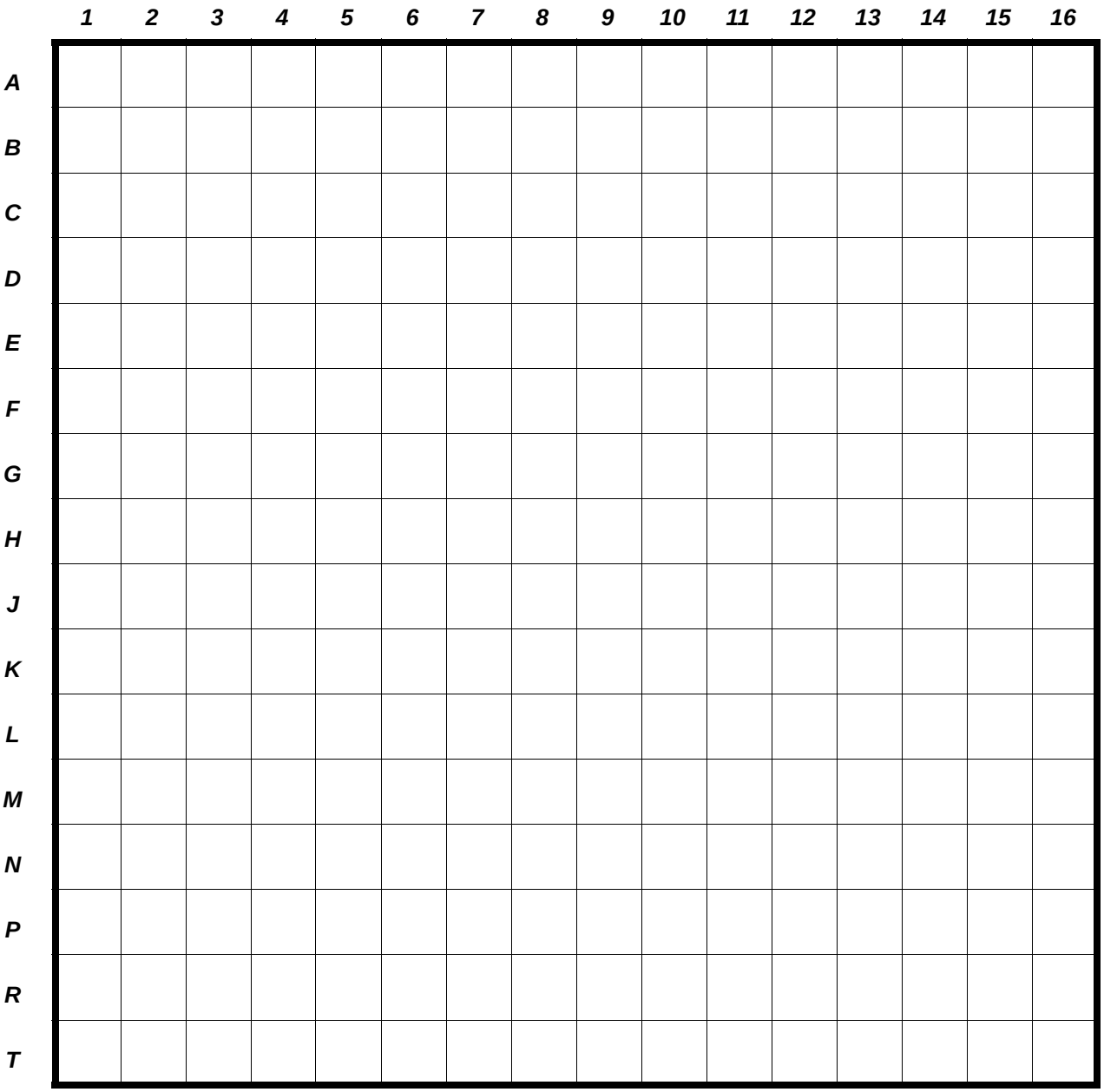
Table 11: Ball Descriptions (Cont.)

Label	*I/O*	*Description*
Bias		
RDAC[1] RDAC[2]	O_A	**DAC Bias Resistor.** Adjusts the reference current of the transmitter digital-to-analog converter. A resistor of 6.04 kΩ ±1% is connected between the RDAC and GND. ***Note:***
1.0V Power Supplies		
AVDDL	PWR	**Analog Low Voltage.** 1.0V.
DVDD	PWR	**Digital Low Core Voltage.** 1.0V.
PLLVDD	PWR	**PLL Voltage.** 1.0V.
QPVDD	PWR	**QSGMII PLL Voltage.** 1.0V
QRVDD	PWR	**QSGMII Receiver Voltage.** 1.0V
QTVDD	PWR	**QSGMII Transmitter Voltage.** 1.0V
3.3V Power Supplies		
AVDDH	PWR	**Analog High Voltage.** 3.3V.
BIASVDD	PWR	**Bias Voltage.** 3.3V.
CLKVDD	PWR	**Reference Clock Voltage.** 3.3V. The voltage supported for REFCLKP/ REFCLKN interface.
OVDD	PWR	**Digital Periphery Voltage.** 3.3V. This supply sets the V_{OH}, V_{OL}, V_{IH} and V_{IL} values for the following ball types: • Strap options • Twisted-pair configuration • Test • LEDs • Sync_E I/Os
Multi-Voltage Power Supplies		
OVDDMDIO	PWR	**MDIO/MDC Supply Voltage.** 1.2V, 2.5V, or 3.3V. The voltage supported by the MDIO interface is set by MDIO_LVL and applying 1.2V, 2.5V or 3.3V to OVDDMDIO. • MDIO_LVL = 0: OVDDMDIO operates at 1.2V. • MDIO_LVL = 1: OVDDMDIO can operate at either 2.5V or 3.3V.
OVDDJTAG	PWR	**JTAG Pad Supply Voltage.** 1.8V, 2.5V or 3.3V. The voltage supported by the JTAG interface is set by applying 1.8V, 2.5V or 3.3V to the OVDDJTAG.
Grounds		
GND	GND	**Ground.** 0.0V. Ground. All ground balls must be connected to a ground plane through vias.
No Connects		
DNC	DNC	**Do Not Connect.** These balls are for test purposes only and should not be connected. These balls must be left floating. Do not connect these balls together.
NC	NC	**Not Connected.** These balls have no internal connection in the device package. Leave these balls floating.

Section 6: Ball Locations

Ball Location Diagram

Figure 9: Top View: Ball Location Diagram



Ball Name Location Diagrams

Figure 10: Top View: Ball Name Location Diagram (Figure 1 of 2)

	1	2	3	4	5	6	7	8
A	TDN_4_0	TDP_4_0	SCLK_FREQ[0]	LED4[1]#	LED4[2]#	DNC	LED5[2]#	LED6[2]#
B	TDP_4_1	TDN_4_1	TEST[0]	LED4[0]#	LED6[1]#	OVDD	DNC	MDC[2]
C	TDN_4_2	TDP_4_2	SCLK_TYPE[1]	RESET#	LED6[0]#	GND	DVDD	OVDDMDIO
D	TDP_4_3	TDN_4_3	GND	LED7[1]#	LED5[0]#	MDIO_SEL[1]	ANEN	DNC
E	TDN_5_3	TDP_5_3	TRST#	OVDD	SCLK_TYPE[0]	DNC	LED5[1]#	MDIO[2]
F	TDP_5_2	TDN_5_2	GND	OVDDJTAG	TDO	LED7[0]#	LED7[2]#	MDC[1]
G	TDN_5_1	TDP_5_1	AVDDL	DVDD	AVDDH	GND	FDX	LED3[2]#
H	TDP_5_0	TDN_5_0	RDAC[2]	BIASVDD[2]	AVDDH	GND	GND	GND
J	TDN_6_0	TDP_6_0	TVCO[2]	AVDDH	PLLVDD[2]	GND	GND	GND
K	TDP_6_1	TDN_6_1	GND	AVDDH	AVDDL	GND	GND	GND
L	TDN_6_2	TDP_6_2	GND	AVDDL	OVDD	GND	GND	GND
M	TDP_6_3	TDN_6_3	CRNT_LED_EN	DVDD	REC_CLK[1]	REC_CLK[2]	OVDD	DVDD
N	TDN_7_3	TDP_7_3	GND	DVDD	LED0[3]#	INTERRUPT#	OVDD	PHYA[0]
P	TDP_7_2	TDN_7_2	PHYA[3]	MDIO_SEL[2]	GND	GND	QRVDD	QTVDD
R	TDN_7_1	TDP_7_1	PHYA[4]	PHYA[2]	RDN0	QRVDD	TDN0	DNC
T	TDP_7_0	TDN_7_0	GND	PHYA[1]	RDP0	GND	TDP0	DNC

Figure 11: Top View: Ball Name Location Diagram (Figure 2 of 2)

9	*10*	*11*	*12*	*13*	*14*	*15*	*16*	
MDIO[1]	DNC	DNC	$\overline{\text{LED1[2]}}$	SPD0	TCK	TDP_3_0	TDN_3_0	***A***
DNC	DNC	OVDD	$\overline{\text{LED2[1]}}$	$\overline{\text{LED0[1]}}$	TMS	TDN_3_1	TDP_3_1	***B***
HUB	TEST[1]	GND	$\overline{\text{LED1[1]}}$	$\overline{\text{LED3[1]}}$	GND	TDP_3_2	TDN_3_2	***C***
PHYA_REV	DNC	$\overline{\text{LED2[2]}}$	OVDD	$\overline{\text{LED3[0]}}$	LOC_REC_CLK[2]	TDN_3_3	TDP_3_3	***D***
SUPER_I	$\overline{\text{LED0[2]}}$	LOC_REC_CLK[1]	OVDDJTAG	$\overline{\text{LED0[0]}}$	GND	TDP_2_3	TDN_2_3	***E***
DNC	$\overline{\text{LED1[0]}}$	$\overline{\text{LED2[0]}}$	DVDD	GND	AVDDL	TDN_2_2	TDP_2_2	***F***
DNC	TDI	GND	AVDDH	TVCO[1]	BIASVDD[1]	TDP_2_1	TDN_2_1	***G***
GND	GND	GND	PLLVDD[1]	AVDDH	RDAC[1]	TDN_2_0	TDP_2_0	***H***
GND	GND	GND	AVDDL	AVDDH	GND	TDP_1_0	TDN_1_0	***J***
GND	GND	GND	AVDDL	SCLK_FREQ[1]	AVDDH	TDN_1_1	TDP_1_1	***K***
GND	GND	GND	DNC	DNC	DNC	TDP_1_2	TDN_1_2	***L***
GND	GND	GND	OVDD	DVDD	DNC	TDN_1_3	TDP_1_3	***M***
QTVDD	QTVDD	QTVDD	CLKVDD	GND	MDIO_LVL	TDP_0_3	TDN_0_3	***N***
QPVDD	QPVDD	QRVDD	GND	GND	GND	TDN_0_2	TDP_0_2	***P***
DNC	RDN1	QRVDD	TDP1	REFCLKN	GND	TDP_0_1	TDN_0_1	***R***
DNC	RDP1	GND	TDN1	REFCLKP	GND	TDN_0_0	TDP_0_0	***T***

Section 7: Ball Assignments

Ballout Listed by Ball Number

Table 12: Ballout Listed by Ball Number

Ball	Ball Name
A01	TDN_4_0
A02	TDP_4_0
A03	SCLK_FREQ[0]
A04	LED4[1]
A05	LED4[2]
A06	DNC
A07	LED5[2]
A08	LED6[2]
A09	MDIO[1]
A10	DNC
A11	DNC
A12	LED1[2]
A13	SPD0
A14	TCK
A15	TDP_3_0
A16	TDN_3_0
B01	TDP_4_1
B02	TDN_4_1
B03	TEST[0]
B04	LED4[0]
B05	LED6[1]
B06	OVDD
B07	DNC
B08	MDC[2]
B09	DNC
B10	DNC
B11	OVDD
B12	LED2[1]
B13	LED0[1]
B14	TMS
B15	TDN_3_1
B16	TDP_3_1
C01	TDN_4_2
C02	TDP_4_2
C03	SCLK_TYPE[1]
C04	RESET
C05	LED6[0]
C06	GND
C07	DVDD
C08	OVDDMDIO
C09	HUB
C10	TEST[1]
C11	GND
C12	LED1[1]
C13	LED3[1]
C14	GND
C15	TDP_3_2
C16	TDN_3_2
D01	TDP_4_3
D02	TDN_4_3
D03	GND
D04	LED7[1]
D05	LED5[0]
D06	MDIO_SEL[1]
D07	ANEN
D08	DNC
D09	PHYA_REV
D10	DNC
D11	LED2[2]
D12	OVDD
D13	LED3[0]
D14	LOC_REC_CLK[2]
D15	TDN_3_3
D16	TDP_3_3
E01	TDN_5_3
E02	TDP_5_3
E03	TRST
E04	OVDD
E05	SCLK_TYPE[0]
E06	DNC
E07	LED5[1]
E08	MDIO[2]
E09	SUPER_I
E10	LED0[2]
E11	LOC_REC_CLK[1]
E12	OVDDJTAG
E13	LED0[0]
E14	GND
E15	TDP_2_3
E16	TDN_2_3
F01	TDP_5_2
F02	TDN_5_2
F03	GND
F04	OVDDJTAG
F05	TDO
F06	LED7[0]
F07	LED7[2]
F08	MDC[1]
F09	DNC
F10	LED1[0]
F11	LED2[0]
F12	DVDD
F13	GND
F14	AVDDL
F15	TDN_2_2
F16	TDP_2_2
G01	TDN_5_1
G02	TDP_5_1
G03	AVDDL
G04	DVDD
G05	AVDDH
G06	GND
G07	FDX
G08	LED3[2]
G09	DNC
G10	TDI
G11	GND
G12	AVDDH
G13	TVCO[1]
G14	BIASVDD[1]
G15	TDP_2_1
G16	TDN_2_1
H01	TDP_5_0
H02	TDN_5_0
H03	RDAC[2]
H04	BIASVDD[2]
H05	AVDDH
H06	GND
H07	GND
H08	GND
H09	GND
H10	GND
H11	GND
H12	PLLVDD[1]
H13	AVDDH
H14	RDAC[1]
H15	TDN_2_0
H16	TDP_2_0
J01	TDN_6_0
J02	TDP_6_0
J03	TVCO[2]
J04	AVDDH
J05	PLLVDD[2]
J06	GND
J07	GND
J08	GND
J09	GND
J10	GND
J11	GND
J12	AVDDL
J13	AVDDH
J14	GND
J15	TDP_1_0
J16	TDN_1_0
K01	TDP_6_1
K02	TDN_6_1
K03	GND
K04	AVDDH
K05	AVDDL
K06	GND
K07	GND
K08	GND

Ball	Ball Name
K09	GND
K10	GND
K11	GND
K12	AVDDL
K13	SCLK_FREQ[1]
K14	AVDDH
K15	TDN_1_1
K16	TDP_1_1
L01	TDN_6_2
L02	TDP_6_2
L03	GND
L04	AVDDL
L05	OVDD
L06	GND
L07	GND
L08	GND
L09	GND
L10	GND
L11	GND
L12	DNC
L13	DNC
L14	DNC
L15	TDP_1_2
L16	TDN_1_2
M01	TDP_6_3
M02	TDN_6_3
M03	CRNT_LED_EN
M04	DVDD
M05	REC_CLK[1]
M06	REC_CLK[2]
M07	OVDD
M08	DVDD
M09	GND
M10	GND
M11	GND
M12	OVDD
M13	DVDD
M14	DNC
M15	TDN_1_3
M16	TDP_1_3
N01	TDN_7_3
N02	TDP_7_3
N03	GND
N04	DVDD
N05	LED0[3]
N06	INTERRUPT
N07	OVDD
N08	PHYA[0]
N09	QTVDD
N10	QTVDD
N11	QTVDD
N12	CLKVDD
N13	GND
N14	MDIO_LVL
N15	TDP_0_3
N16	TDN_0_3
P01	TDP_7_2
P02	TDN_7_2
P03	PHYA[3]
P04	MDIO_SEL[2]
P05	GND
P06	GND
P07	QRVDD
P08	QTVDD
P09	QPVDD
P10	QPVDD
P11	QRVDD
P12	GND
P13	GND
P14	GND
P15	TDN_0_2
P16	TDP_0_2
R01	TDN_7_1
R02	TDP_7_1
R03	PHYA[4]
R04	PHYA[2]
R05	RDN0
R06	QRVDD
R07	TDN0
R08	DNC
R09	DNC
R10	RDN1
R11	QRVDD
R12	TDP1
R13	REFCLKN
R14	GND
R15	TDP_0_1
R16	TDN_0_1
T01	TDP_7_0
T02	TDN_7_0
T03	GND
T04	PHYA[1]
T05	RDP0
T06	GND
T07	TDP0
T08	DNC
T09	DNC
T10	RDP1
T11	GND
T12	TDN1
T13	REFCLKP
T14	GND
T15	TDN_0_0
T16	TDP_0_0

Section 8: Operational Description

Power Sequencing

There are no specific power sequencing requirements for the B50282. It is recommended that the higher supply be brought up first (for example, 3.3V and then 1.0V) or at the same time as the lower supplies. This is only a recommendation and not a requirement.

Resetting the B50282

Hardware Reset

$\overline{\text{RESET}}$ resets all internal nodes to a known state. Hardware reset is accomplished by holding $\overline{\text{RESET}}$ low for at least 10 ms after the power supply voltages and clocks are stable. Once $\overline{\text{RESET}}$ is brought high, the PHY completes its reset sequence within 20 µs. All outputs are inactive until the PHY has completed its reset sequence. The PHY keeps the inputs inactive for 5 ms after the deassertion of hardware reset. The hardware configuration balls and the PHY address balls are read on the deassertion of hardware reset. See “Reset Timing” on page 84.

Caution! $\overline{\text{RESET}}$ must be asserted during power-up.

Software Reset

The B50282 has multiple reset bits to reset the different blocks/registers are as follows:

- Per Port Register Reset
- Global RDB Register Reset
- Clause 45 Register Reset
- QSGMII Registers

Per Port Register Reset

The B50282 has two methods for performing Per Port Register software reset.

The first method behaves like a hardware reset except it is done on a port-by-port basis. This reset will set the PHY registers listed below to the default values and hardware strap balls that are labelled *sample on reset* (SOR) are relatched.

- IEEE Registers (0x00 to 0x0F)
- Per Port RDB Registers (RDB_Registers, offset 0x00 to offset 0x2FF)

To enable software reset set Register 0x00, bit[15] = 1’b1. This needs to be done to every port that needs to be reset. This bit is self-clearing.

The second method issues a soft-reset for 640 ns that will clear the status registers/bits listed below and leave MDIO control registers/bits alone. Strap options are not relatched.

- IEEE Registers (0x00 to 0x0F)
- Per Port RDB Registers (RDB_Registers, offset 0x00 to offset 0x2FF)

This reset is done on a port-by-port basis. To enable the software reset, set RDB_Reg, offset 0x021, bit[0] = 1’b0 to access the copper register space and then set RDB_Register, offset 0x070, bit[0] = 1’b1. This needs to be done to every port that needs to be reset. This bit is self-clearing.

Note: This reset does not affect the QSGMII Registers.

Global RDB Register Reset

Global RDB Register reset will reset the Global RDB registers (RDB_Registers, offset 0x800 to offset 0xAFF) to their default values. This reset is done on a PHY basis. To enable the software reset, set RDB_Register, offset 0x82B, bit[15] = 1’b1. This needs to be done to PORT 0’s PHY address. This bit is self-clearing.

Note: This reset does not affect the following registers:

- Per Port Register (Reg. 0x00 to 0x0F and RDB_Registers, offset 0x00 to offset 0x2F)
- Clause 45 Registers
- QSGMII Registers.

Clause 45 Register Reset

Clause 45 Register reset will set the EEE block and registers to their default values. To enable the reset, set Clause 45 DEVAD 0x1, Address 0x0, bit[15] = 1’b0. This needs to be done to PORT 0’s PHY address. This bit is self-clearing.

Note: his reset does not affect the following registers:

- Per Port Register (Reg. 0x00 to 0x0F and RDB_Registers, offset 0x00 to offset 0x2F)
- Global RDB Registers (RDB_Registers, offset 0x800 to offset 0xAFF)
- QSGMII Registers.

QSGMII Register Reset

QSGMII Register reset will set the QSGMII block and registers to their default values. There are two resets bits, one for QSGMII Quad 0 and the other for QSGMII Quad 1.

To enable QSGMII Quad 0 reset, set QSGMII Register, BAR = 0x0000, REGAD = 0x00, AER = 0x000. To enable QSGMII Quad 0 reset, set QSGMII Register, BAR = 0x0000, REGAD = 0x00, AER = 0x004. This needs to be done to PORT 0’s PHY address. These bits are self-clearing.

Table 13: Reset Summary Table

Reset	*Blocks Affected*	*Registers Affected*
Per PHY Hardware Reset (Method 1)	• Twisted-pair • Reference clock • LEDs • Cable diagnostics • Hardware strap balls • Voltage/temp monitor • Sync_E • EEE • AutogrEEEn	• RDB_Reg, offset 0x021, bit[0] = 1'b0 – Reg. 0x0 to 0xF • RDB_Reg, offset 0x021, bit[0] = 1'b1 – Reg. 0x0 to 0xF • RDB_Reg., offset 0x00 to offset 0x2FF • RDB_Reg, offset 0x800 to offset 0xAFF • Clause 45 DEVAD 0x1 to DEVAD 0x7 • QSGMII Reg. BAR 0x0 to BAR 0x8300
Per Port Register Reset (Method 2) • RDB_Reg, offset 0x021, bit[0] = 1'b0 • Reg. 0x00, bit[15] = 1'b1	• Twisted-pair • Reference clock • LEDs • Cable diagnostics • Hardware strap balls	• RDB_Reg, offset 0x021, bit[0] = 1'b0 – Reg. 0x0 to 0xF • RDB_Reg., offset 0x00 to offset 0x2FF
Per Port Per Port Register Reset • RDB_Reg, offset 0x021, bit[0] = 1'b0 • RDB_Reg, offset 0x070, bit[0] = 1'b1	N/A	Status Registers/bits Only • Reg. 0x0 to 0xF • RDB_Reg, offset 0x00 to offset 0x2FF
Global RDB Register Reset • RDB_Reg, offset 0x82B, bit[15] = 1'b1	• Voltage/temp monitor • Sync_E	• RDB_Reg, offset 0x800 to offset 0xAFF
Clause 45 Register Reset • Clause 45 DEVAD 0x1, Address 0x0, bit[15] = 1'b0	• EEE	• Clause 45 DEVAD 0x1 to DEVAD 0x7
QSGMII Register Reset QSGMII[0] (QSGMII Quad 0) • BAR = 0x0000, REGAD = 0x00, AER = 0x000 QSGMII[1] (QSGMII Quad 1) • BAR = 0x0000, REGAD = 0x00, AER = 0x0004	• QSGMII	• QSGMII Reg. BAR 0x0 to BAR 0x8300

Reference Clock Using REFCLKP/N

The B50282 supports the various clock modes shown in Table 14.

Table 14: Reference Clock Modes

Mode	*SCLK_TYPE[1:0]*	*SCLK_FREQ[1:0]*
25 MHz crystal	10	00
25 MHz single-ended CMOS clock	01	00
25 MHz differential clock	00	00
125 MHz single-ended CMOS clock	01	01
125 MHz differential clock	00	01
156.25 MHz single-ended CMOS clock	01	11
156.25 MHz differential clock	00	11
312.5 MHz differential clock	00	10

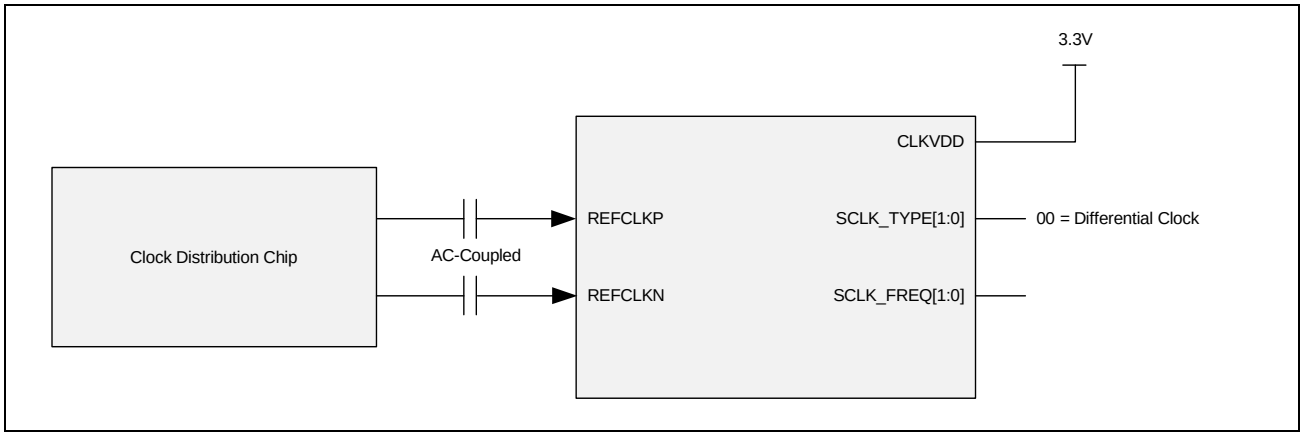
CML Differential Mode

Configurations for the CML Differential Clock modes are shown in Table 15. Figure 12 shows a typical differential clock connection. REFCLKP/REFCLKN have an internal 100 ohm differential must be AC-coupled to the differential clock source with a 0.1 µF cap.

Table 15: CML Differential Clock Mode Configurations

Mode	*SCLK_TYPE[1:0]*	*SCLK_FREQ[1:0]*
25 MHz differential clock	00	00
125 MHz differential clock	00	01
156.25 MHz differential clock	00	11
312.5 MHz differential clock	00	10

Figure 12: Differential Clock Input



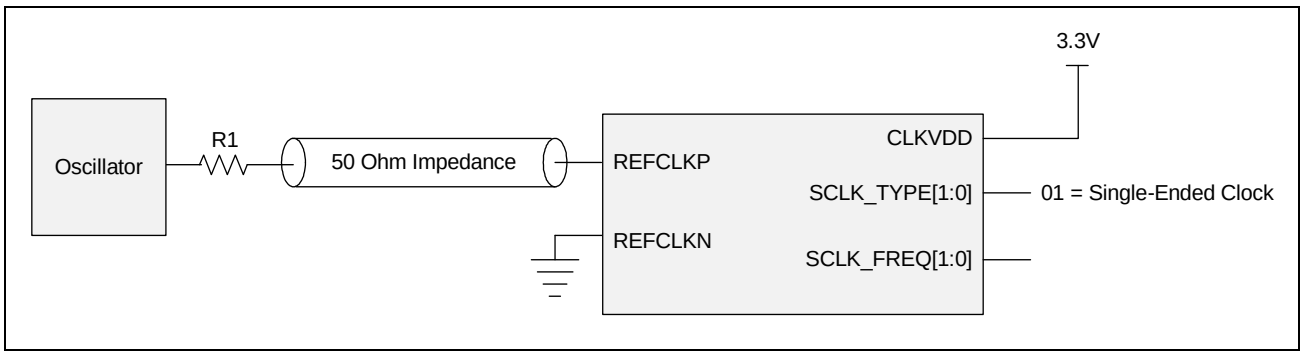
Single-Ended CMOS Mode

Configurations for single-ended CMOS clock modes are shown in Table 16. Figure 13 shows a typical Single-Ended CMOS clock connection. The REFCLKN input must be connected directly to ground. R1 = $Z_{Trace} - Z_{Driver}$ where R1 is a series termination resistor used to match the output impedance of the Oscillator (Z_{Driver}) to the trace impedance (Z_{Trace}).

Table 16: Single-Ended CMOS Clock Mode Configurations

Mode	*SCLK_TYPE[1:0]*	*SCLK_FREQ[1:0]*
25 MHz single-ended CMOS clock	01	00
125 MHz single-ended CMOS clock	01	01
156.25 MHz single-ended CMOS clock	01	11

Figure 13: Single-Ended CMOS Input



Crystal Mode

Configurations for crystals are shown in Table 17. Figure 14 on page 72 shows a typical crystal connection and Table 18 on page 72 shows typical crystal parameters. The B50282 can only support a 25 MHz crystal.

Table 17: Crystal Configuration

Mode	*SCLK_TYPE[1:0]*	*SCLK_FREQ[1:0]*
25 MHz crystal	10	00

Figure 14: Crystal Application

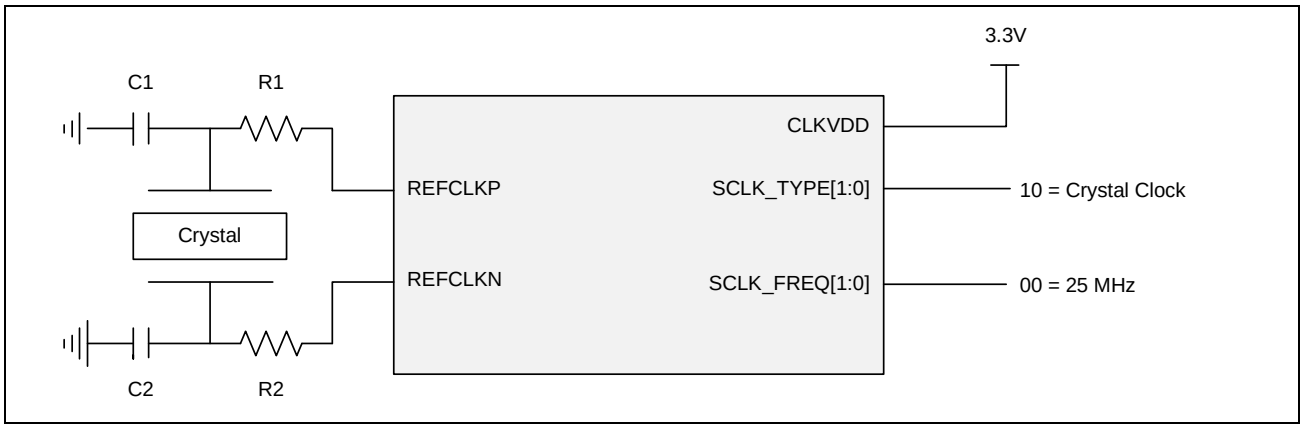


Table 18: Typical Crystal Parameters

Parameter	*Value*
Frequency	25.000 MHz
Tolerance	±50 ppm
Operating mode	Parallel resonance
ESR	< 40Ω
Crystal loading capacitance	18 pF typical
Crystal aging	5 ppm per year maximum
Crystal stability	±30 ppm minimum
Crystal drive level	500 µW

The differential input is designed to operate properly with an external crystal that has a maximum ESR of less than 40Ω and is parallel-resonant with a standard 18 pF load. There is not a general value for the off-chip components that work for all cases. Their values will depend on the crystal, board layout, and operation voltage. The values in Table 19 will get the oscillator working, but proper operation and characterization needs to be verified.

Table 19: Crystal Starting Values

C1	*C2*	*R1*	*R2*
27 pF to 30 pF	27 pF to 30 pF	10Ω	10Ω

Q Adjustment

There are two series resistors, R1 and R2, that have a typical value of 10Ω. R1 and R2 are used to adjust the Q of this circuit. No current-limiting series resistor to the crystal is needed because the current to the clock crystal is limited on the chip, thus eliminating the need for an additional external component. The loading capacitors for the remaining clock crystal tank circuit are determined based on the clock crystal data sheet loading specification.

Determining Load Capacitance

The load capacitance (C_{load}) is primarily determined by the specified frequency. The following equation gives the approximate load capacitance, where C_{stray} is the stray capacitance (board parasitics and so on).

$$C_{load} = C_{stray} + \frac{C_1 \times C_2}{C_1 + C_2}$$

C_{stray} is usually in the range of 2 pF to 5 pF. The crystal is specified with ±50 ppm tolerance for a given load capacitance. Therefore adjust the tank circuit loading capacitance values for C1 and C2 to force the oscillation frequency within the specified tolerance. If the load capacitance is too small, the frequency will be too high. If the board parasitic capacitances are too large or the crystal's specified load capacitance is too small, it may become difficult to adjust the frequency within limits. In this case, either choose another crystal with a larger specified load capacitance or reduce the parasitic capacitance.

Note:

- Usually $C_1 = C_1 = 2$ x Cload is used to adjust the frequency of the oscillator.
- R1 and R2 on REF_CLKP and REF_CLKN are used to adjust the Q of the circuit.

The following is an example calculation for a crystal with a typical load capacitance (C_{load} = 18 pF) and C_{stray} estimated at 4 pF maximum. From the equation:

$$C_{load} = C_{stray} + \frac{C_1 \times C_2}{C_1 + C_2}$$

Let $C_1 = C_2 = C$

$$C = 2(C_{load} - C_{stray})$$

$C = C_1 = C_2 = 2 \times (18\text{ pF} - 4\text{ pF}) = 28$ pF. The load capacitance value of 27 pF is chosen because this is an easily procured standard capacitor value.

Copper Loopback with Loopback Plug

This allows packets to be sent to the PHY's QSGMII receive input interface, to the copper twisted-pair interface, to the magnetics and RJ-45 connector and back to the PHY's QSGMII transmit interface. This mode is enabled on a per-port basis. The red dashed line in Figure 15 on page 74 shows the loopback path for Port 0. In 1000BASE-T, 100BASE-TX, and 10BASE-T modes, a Loopback Plug must be inserted into the RJ-45 connector. The jumper block should have the following RJ-45 pins connected together:

- Pin 1 connected to Pin 3

- Pin 2 connected to Pin 6
- Pin 4 connected to Pin 7
- Pin 5 connected to Pin 8

Note: Copper loopback with loopback plug is not guaranteed to work with EEE or AutogrEEEn enabled.

Note: To exit the copper loopback with loopback plug, Broadcom recommends a software or hardware reset.

Figure 15: Copper Loopback Mode with Loopback Plug on Port 0

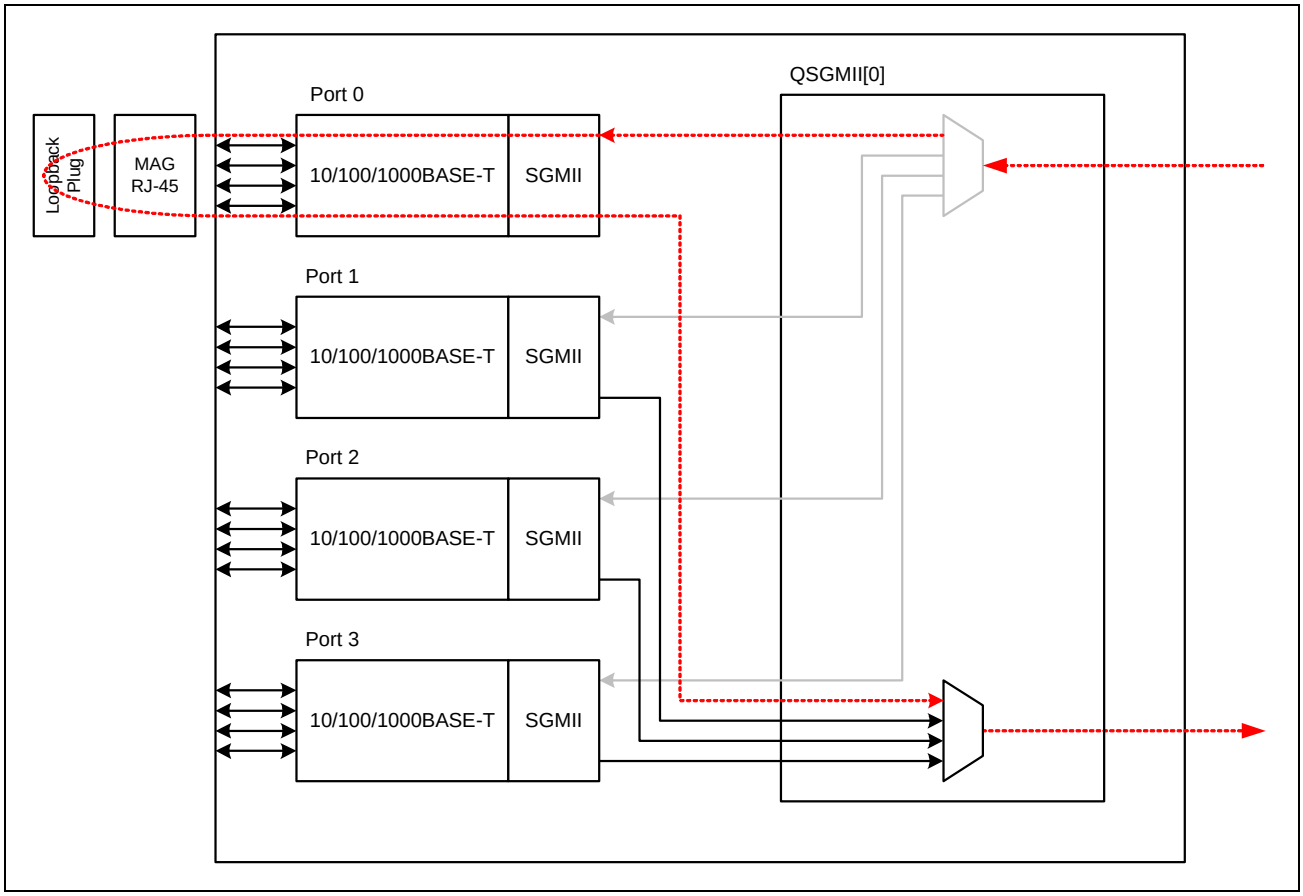


Table 20 through Table 22 describe how the copper loopback with loopback plug is enabled for 1000BASE-T, 100BASE-TX, and 10BASE-T modes.

Table 20: 1000BASE-T Loopback with Loopback Plug

Register Writes	*Comments*
Write Register 0x09 = 0x1800	Enable 1000BASE-T master mode
Write Register 0x00 = 0x0040	Enable force 1000BASE-T
Write RDB_Register, offset 0x028 = 0x8400	Enable 1000BASE-T loopback mode with loopback plug

Table 21: 100BASE-TX Loopback with Loopback Plug

Register Writes	*Comments*
Write Register 0x00 = 0x2100	Enable force 100BASE-TX full-duplex mode
Write RDB_Register, offset 0x028 = 0x8400	Enable 100BASE-TX loopback mode with loopback plug

Table 22: 10BASE-T Loopback with Loopback Plug

Register Writes	*Comments*
Write Register 0x00 = 0x0100	Enable force 10BASE-T full-duplex mode
Write RDB_Register, offset 0x028 = 0x8400	Enable 10BASE-T loopback mode with loopback plug

Copper Loopback without Loopback Plug

This allows packets to be sent to the PHY's QSGMII receive input interface, to the copper twisted-pair interface and back to the PHY's QSGMII transmit interface. This does not test the magnetics of RJ-45 connector. This is enabled on a per port basis. Figure 16 on page 76 shows the loopback path for Port 0.

Note: Copper loopback without loopback plug does not work properly if there is a jumper block or cable connected to the RJ-45 connector.
Copper loopback without loopback plug is not guaranteed to work with EEE or AutogrEEEn enabled.
To exit copper loopback without loopback plug, Broadcom recommends a software or hardware reset.

Figure 16: External Copper Loopback Mode without Loopback Plug on Port 0

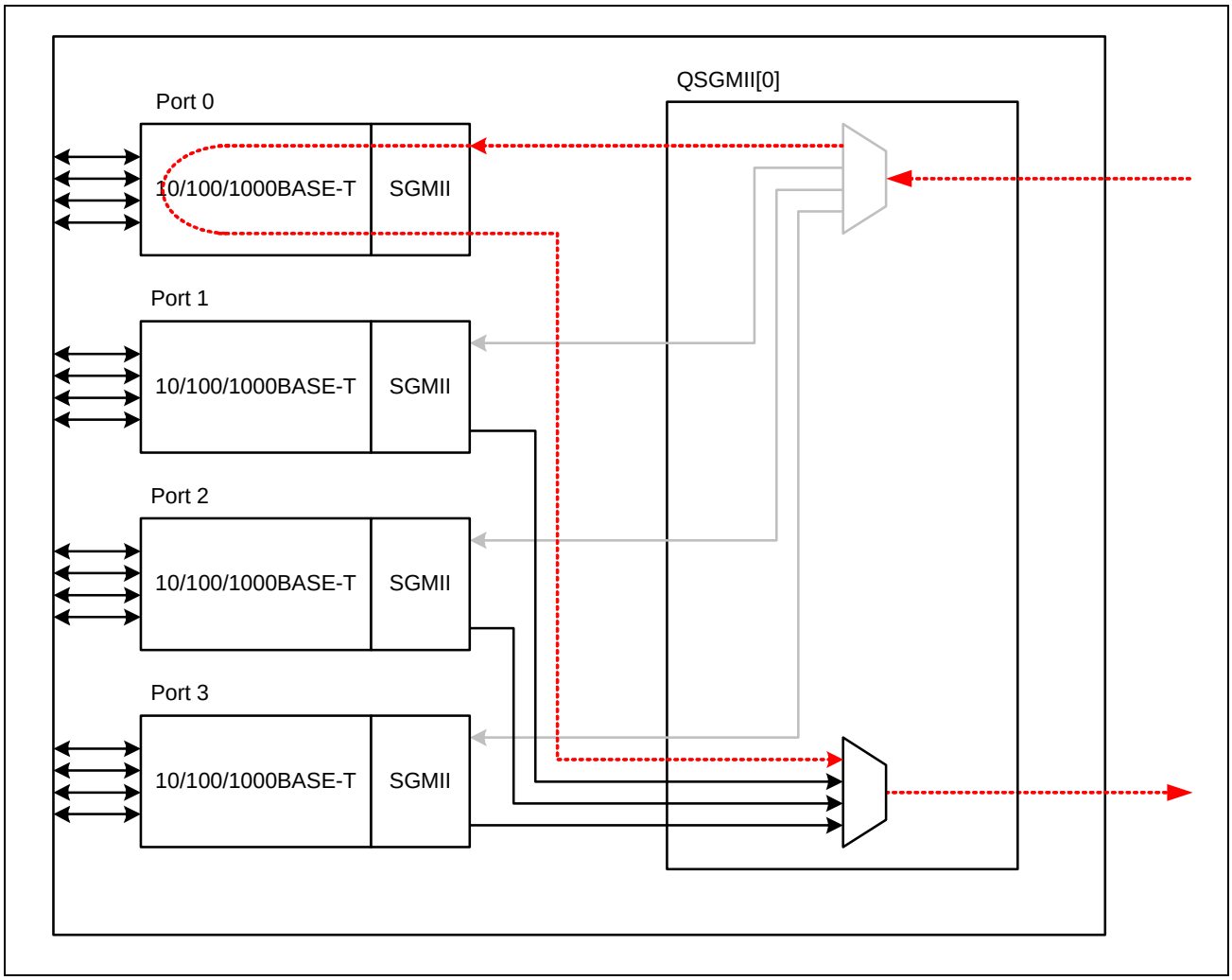


Table 23 through Table 25 describe how the copper loopback mode is enabled for 1000BASE-T, 100BASE-TX, and 10BASE-T modes with and without a loopback plug.

Table 23: 1000BASE-T Loopback without Loopback Plug

Register Writes	*Comments*
Write Register 0x09 = 0x1800	Enable 1000BASE-T master mode
Write Register 0x00 = 0x0040	Enable force 1000BASE-T
Write RDB_Register, offset 0x028 = 0x8400	Enable 1000BASE-T loopback mode
Write RDB_Register, offset 0x02C = 0x4014	Enable 1000BASE-T loopback mode without loopback plug

Table 24: 100BASE-TX Loopback without Loopback Plug

Register Writes	*Comments*
Write Register 0x00 = 0x2100	Enable force 100BASE-TX full-duplex mode
Write RDB_Register, offset 0x028 = 0x8400	Enable 100BASE-TX loopback mode with loopback plug
Write RDB_Register, offset 0x02C = 0x4014	Enable 100BASE-TX loopback mode without loopback plug

Table 25: 10BASE-T Loopback without Loopback Plug

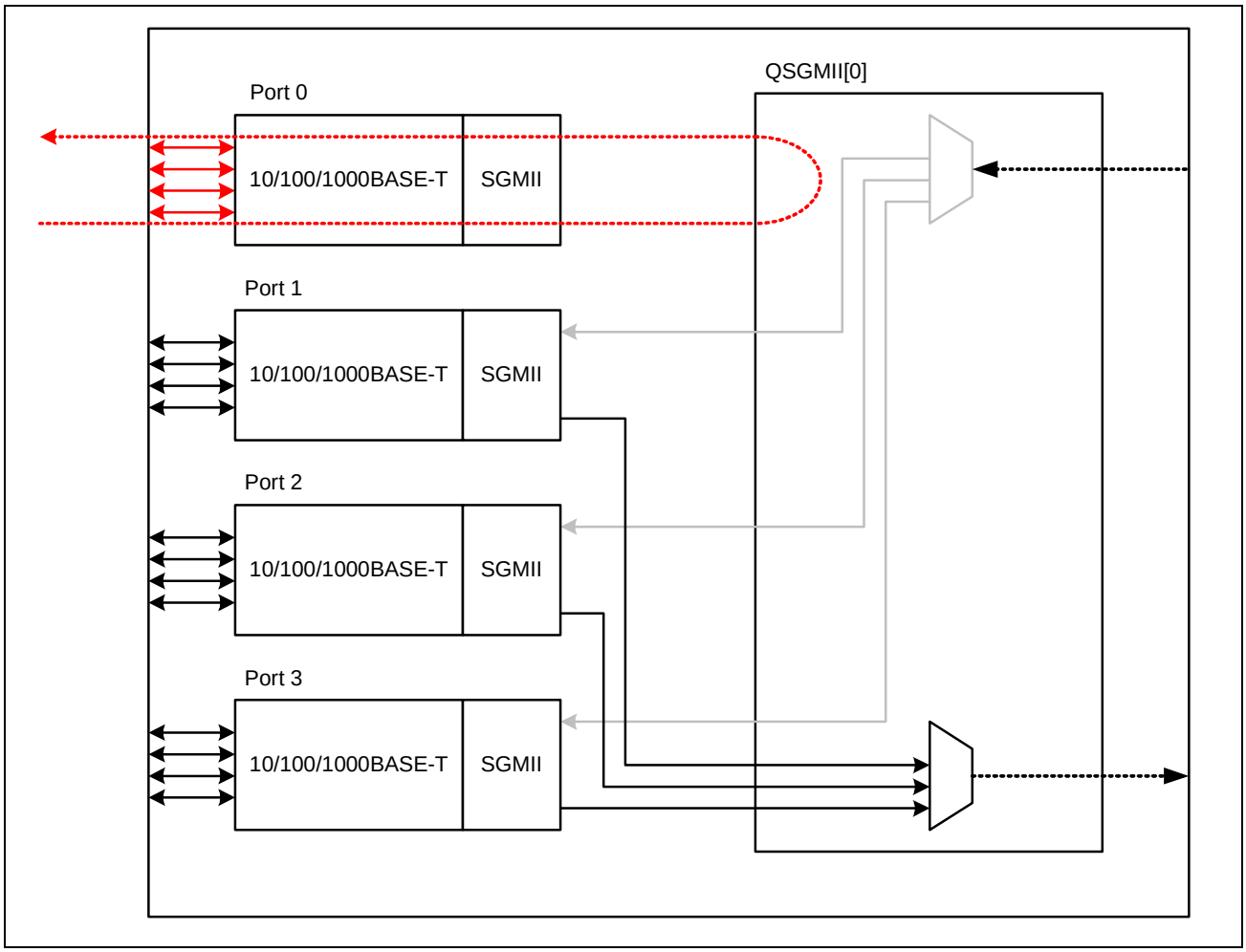
Register Writes	*Comments*
Write Register 0x00 = 0x0100	Enable force 10BASE-T full-duplex mode
Write RDB_Register, offset 0x028 = 0x8400	Enable 10BASE-T loopback mode with loopback plug
Write RDB_Register, offset 0x02C = 0x4014	Enable 10BASE-T loopback mode without loopback plug

Copper Line-Side Loopback

This allows packets to be sent to the PHY's twisted-pair interface to the PHY's PCS layer and back to the PHY's twisted-pair interface. This mode is enabled on a per port basis. The red dashed line in Figure 17 on page 78 shows the loopback path for Port 0.

Note: Copper line-side loopback is not guaranteed to work with EEE or AutogrEEEn enabled. To exit copper line-side loopback, Broadcom recommends a software or hardware reset.

Figure 17: Copper Line-Side Loopback on Port 0



To enable copper line-side loopback, do the following writes:

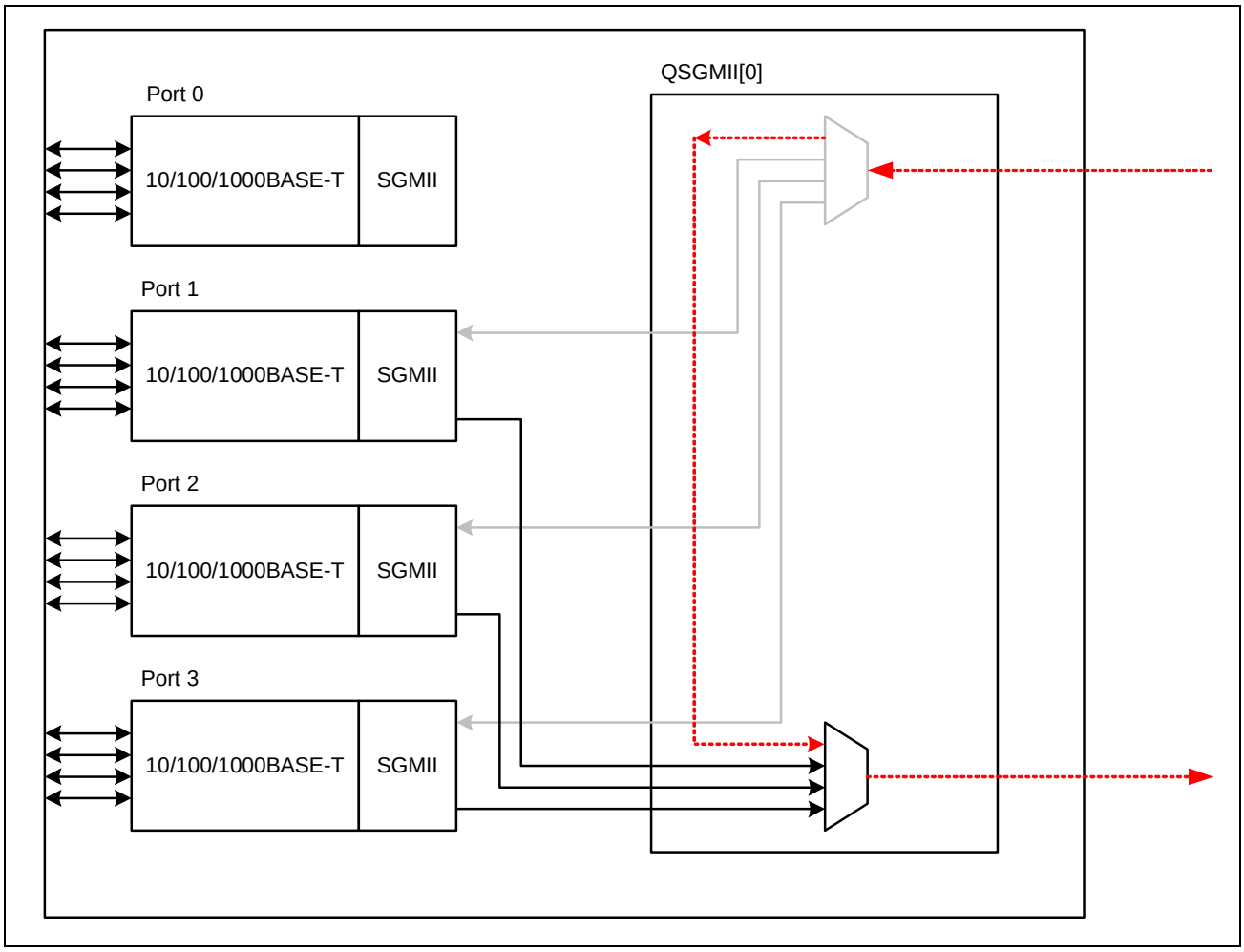
- Write RDB_Register, offset 0x02C, bit[15] = 1'b1 (copper line-side loopback enable)
- Write Register 0x0, bit[9] = 1'b1 (restart auto-negotiation)

Per Port QSGMII Packet Loopback

This allows data packets to be sent to the PHY's QSGMII receive input to the PHY's QSGMII PCS layer and back to the PHY's QSGMII transmit output. This mode is enabled on a per port basis (all four ports per QSGMII can be enabled). The speed of the PHY Port's QSGMII lane must match the speed of the switch's QSGMII lane. The red dashed line in Figure 18 on page 79 shows the loopback path for Port 0.

Note: To exit per port QSGMII packet loopback, Broadcom recommends a software or hardware reset.

Figure 18: Per Port QSGMII Loopback on Port 0



To enable per port QSGMII loopback, do the following writes:

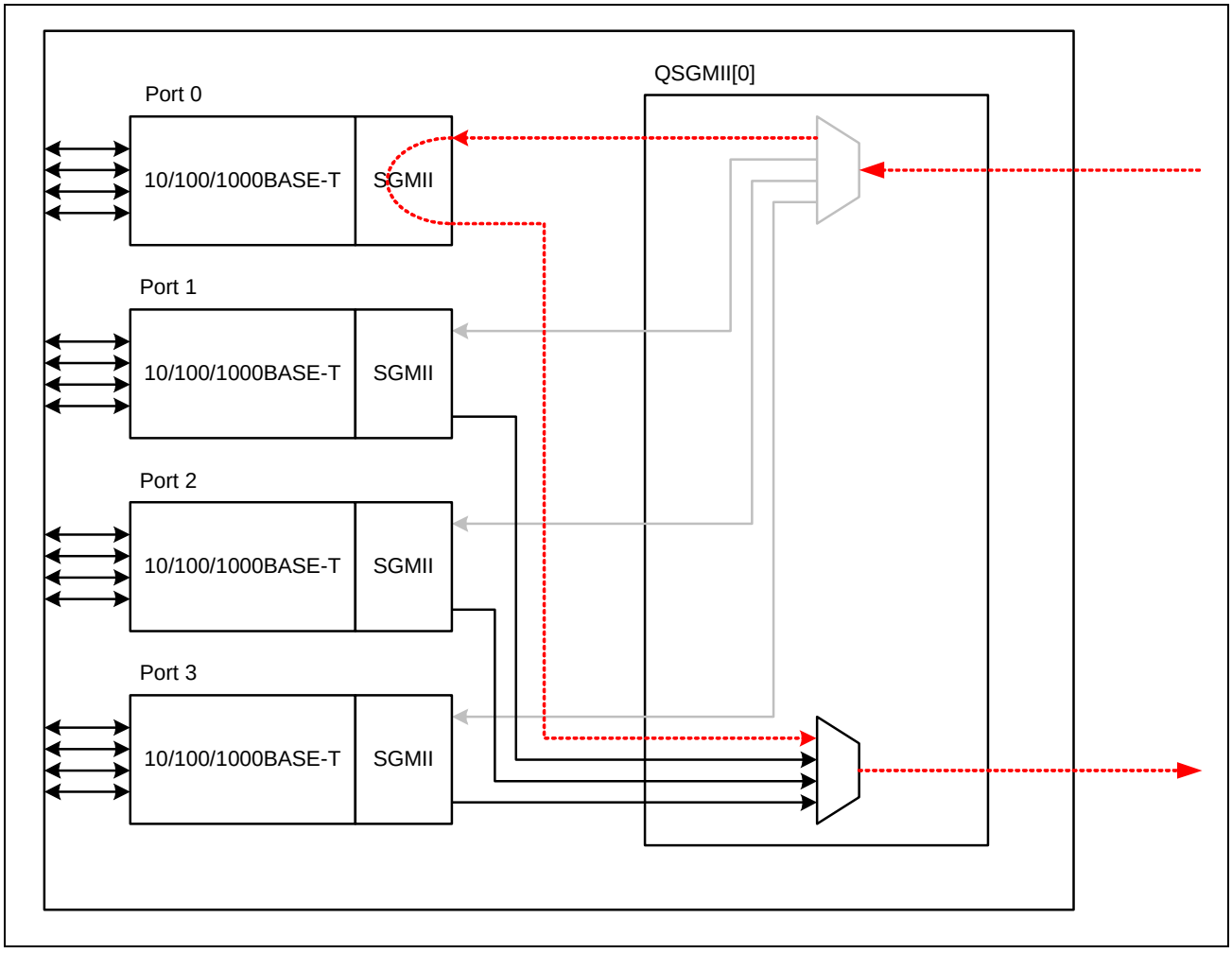
- Write Register 0x1F = 0xFFD0 (Set BAR to AER register)
  - Write Register 0x1E = 0x0 (Enable read/writes to Port 0) and/or
  - Write Register 0x1E = 0x1 (Enable read/writes to Port 1) and/or
  - Write Register 0x1E = 0x2 (Enable read/writes to Port 2) and/or
  - Write Register 0x1E = 0x3 (Enable read/writes to Port 3) and/or
  - Write Register 0x1E = 0x4 (Enable read/writes to Port 4) and/or
  - Write Register 0x1E = 0x5 (Enable read/writes to Port 5) and/or
  - Write Register 0x1E = 0x6 (Enable read/writes to Port 6) and/or
  - Write Register 0x1E = 0x7 (Enable read/writes to Port 7) and/or
  - Write Register 0x1E = 0x1F (Enable read/writes to all eight ports)
- Write QSGMII Register (BAR = 0x8300, REGAD = 0x10) = 0x05A0 (Enable loopback)

Per Port QSGMII/SGMII Packet Loopback

This allows data packets to be sent to the PHY's QSGMII receive input to the PHY's SGMII PCS layer and back to the PHY's QSGMII transmit output. This mode is enabled on a per port basis (all four ports per QSGMII can be enabled). The speed of the PHY port's QSGMII lane must match the speed of the switch's QSGMII lane. The red dashed line in Figure 19 shows the loopback path for Port 0.

Note: To exit per port QSGMII/SGMII packet loopback, Broadcom recommends a software or hardware reset.

Figure 19: Per Port QSGMII/SGMII Loopback on Port 0



To enable per port QSGMII/SGMII loopback, do the following writes:

- Write RDB_Register, offset 0x021, bit[0] = 1'b'0 (1000BASE-T register space selected.)
- Write RDB_Register, offset 0x00E, bit[12] = 1'b1 (Force link when in 10 Mbps or 100 Mbps mode. Not needed for 1000 Mbps mode.)

- Select the QSGMII speed for the port.
  - Write Register 0x0 = 0x4140 to enable 1000 Mbps loopback, or
  - Write Register 0x0 = 0x6100 to enable 100 Mbps loopback, or
  - Write Register 0x0 = 0x4100 to enable 10 Mbps loopback.

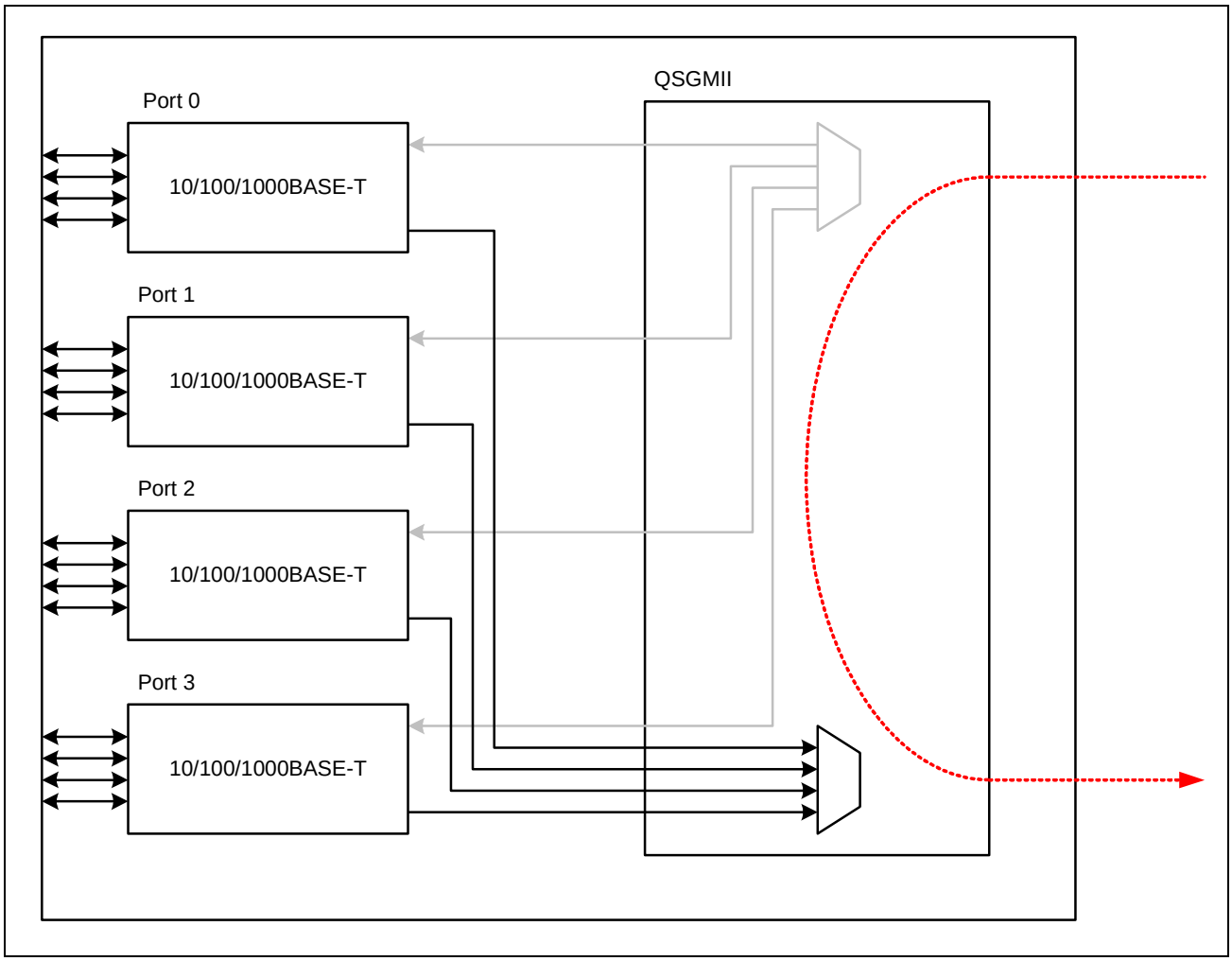
QSGMII PRBS Packet Loopback

This allows 5 Gbps PRBS data to be sent to the PHY's QSGMII receive input to the PHY's QSGMII transmit output. This mode is enabled on a per-QSGMII basis. The red dashed line in Figure 20 on page 82 shows the loopback path for the 5 Gbps PRBS data on QSGMII[0].

Caution! The reference clocks for the PHY and switch must be from the same reference clock source since there is no PHY FIFO clock compensation in the path.

Note: To exit per port QSGMII packet loopback, Broadcom recommends a software or hardware reset.

Figure 20: QSGMII 5 Gbps PRBS Loopback



To enable 5 Gbps PRBS loopback, do the following writes:

- Write Register 0x1F = 0xFFD0 (set BAR to AER register)
  - Write Register 0x1E = 0x0 (enable read/writes to QSGMII[0]) and or
  - Write Register 0x1E = 0x4 (enable read/writes to QSGMII[1]) or
  - Write Register 0x1E = 0x1F (enable read/writes to QSGMII[0] or QSGMII[1])
- Write QSGMII Register (BAR = 0x8000, REGAD = 0x10) = 0x202F (enable 5 Gbps mode)
- Write QSGMII Register (BAR = 0x8000, REGAD = 0x1E) = 0x0001 (enable 5 Gbps register space)
- QSGMII Register (BAR = 0x0000, REGAD = 0x0) = 0xA040 (soft reset)
- QSGMII Register (BAR = 0x8000, REGAD = 0x10) = 0x062F (clear PLL start sequencer)
- QSGMII Register (BAR = 0x8300, REGAD = 0x18) = (set PLL to match PHY/switch reference clock)
  - 0x5800 (for 25 MHz or 125 MHz reference clock) or
  - 0x6600 (for 156.25 MHz or 325.4 MHz reference clock)
- QSGMII Register (BAR = 0x8000, REGAD = 0x10) = 0x263F (clear PLL start sequencer)
- QSGMII Register (BAR = 0x8010, REGAD = 0x15) = 0x0000 (disable QSGMII Clause 36)

- QSGMII Register (BAR = 0x8010, REGAD = 0x16) = 0x0303 (set PLL Divider to 1)
- QSGMII Register (BAR = 0x8010, REGAD = 0x17) = 0x0010 (disable [8b/10b and comma detect], and enable loopback)
- QSGMII Register (BAR = 0x8010, REGAD = 0x19) = 0x0008 (enable PRBS mode)

Section 9: Timing and AC Characteristics

Reset Timing

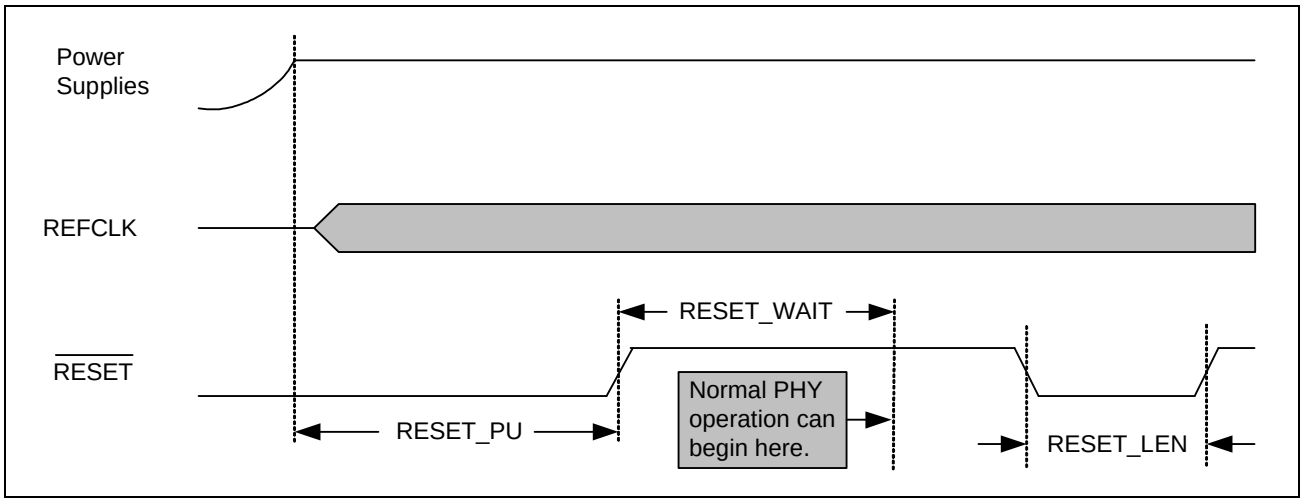
Table 26: Reset Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Power-up to $\overline{\text{RESET}}$ deassertion	RESET_PU	10	–	–	ms
$\overline{\text{RESET}}$ deassertion to normal PHY operation	RESET_WAIT	20	–	–	µs
$\overline{\text{RESET}}$ pulse length	RESET_LEN	2	–	–	µs
$\overline{\text{RESET}}$ rise/fall time	–	–	–	25	ns

Note:

- $\overline{\text{RESET}}$ must be low when power supplies are ramping up.
- When $\overline{\text{RESET}}$ is low, there must be a valid clock signal at the REFCLK input. All external power supplies need to be stable.
- MII register read/write access and normal PHY operation can start at the end of the RESET_WAIT time.
- RESET_PU must be performed when the device is first powered up. Software reset or RESET_LEN does not need to be performed after RESET_PU.
- Software reset or RESET_LEN should not be performed until after RESET_PU and RESET_WAIT have been completed. After issuing a software reset or a RESET_LEN, normal PHY operation can begin after waiting the RESET_WAIT time of 20 µs.

Figure 21: Reset Timing



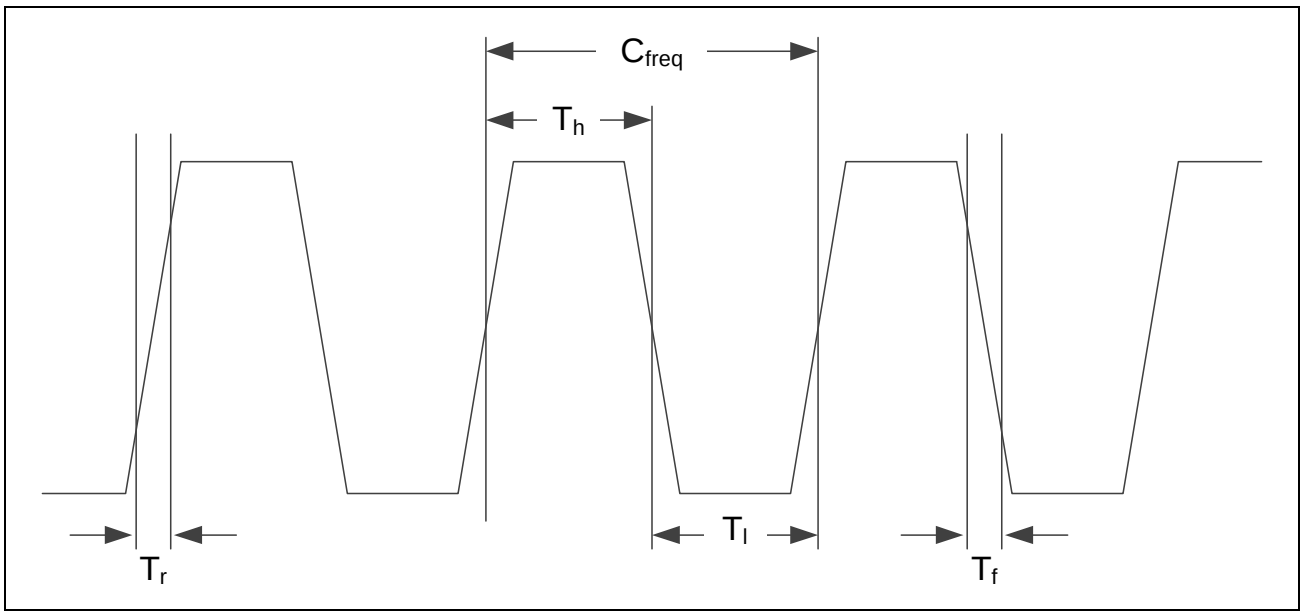
REFCLK Input Timing (Single-Ended Mode)

Table 27: REFCLK Input Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Frequency	C_{freq}	–	25	–	MHz
Frequency	C_{freq}	–	125	–	MHz
Frequency	C_{freq}	–	156.25	–	MHz
Accuracy	–	–50	–	+50	ppm
Duty Cycle Distortion[a]	–	40	–	60	%
Rise/Fall time[b]	T_r/T_f	–	–	1	ns
RMS Phase Jitter[c]	–	–	–	1.5	ps-rms
Do not use PLL-based oscillators or zero-delay buffers as a source for REFCLK because this introduces excessive jitter that may result in unacceptable bit error rate performance.					

a. Measured at 50% point.
b. Measured at the 20% to 80% points.
c. Frequency = 25 MHz: Fj = 1 kHz to 5 MHz offset frequency.
Frequency > 25 MHz: Fj = 12 kHz to 20 MHz offset frequency.

Figure 22: REFCLK Input Timing Single-Ended Mode



REFCLK Clock Input Timing (Differential Mode)

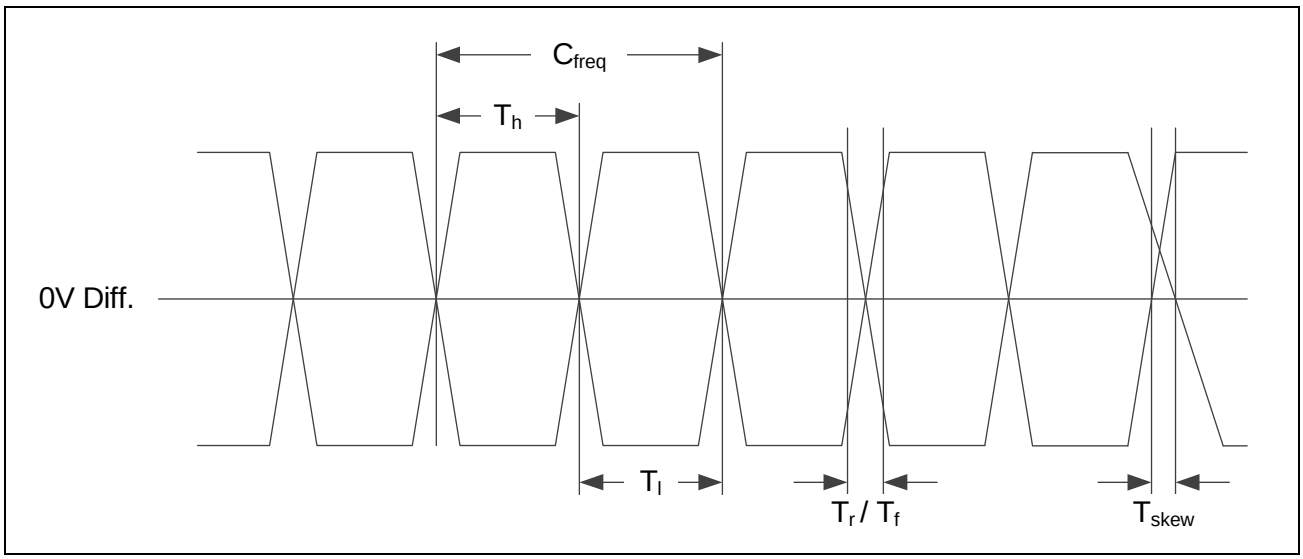
Table 28: REFCLKP/N Clock Input Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Frequency	C_{freq}	–	25	–	MHz
Frequency	C_{freq}	–	125	–	MHz
Frequency	C_{freq}	–	156.25	–	MHz
Frequency	C_{freq}	–	312.5	–	MHz
Frequency Deviation	PPM	–50	–	+50	PPM
Duty Cycle [a]	T_h/T_l	40	50	60	%
RMS Phase Jitter[b]	–	–	–	1.5	ps-rms
Rise/Fall time[c]	T_r/T_f	–	–	1	ns
Differential Skew[d]	T_{skew}	–	–	80	ps

a. Measured at 50% crossing-point.
b. Frequency = 25 MHz: Fj = 1 kHz to 5 MHz offset frequency.
Frequency > 25 MHz: Fj = 12 kHz to 20 MHz offset frequency.
c. Measured at 20%–80% points.
d. Skew between two members of a differential pair measured at 50% crossing-point.

Note: REFCLKP/N must be AC-coupled to the clock source.

Figure 23: REFCLK Input Timing Differential Mode

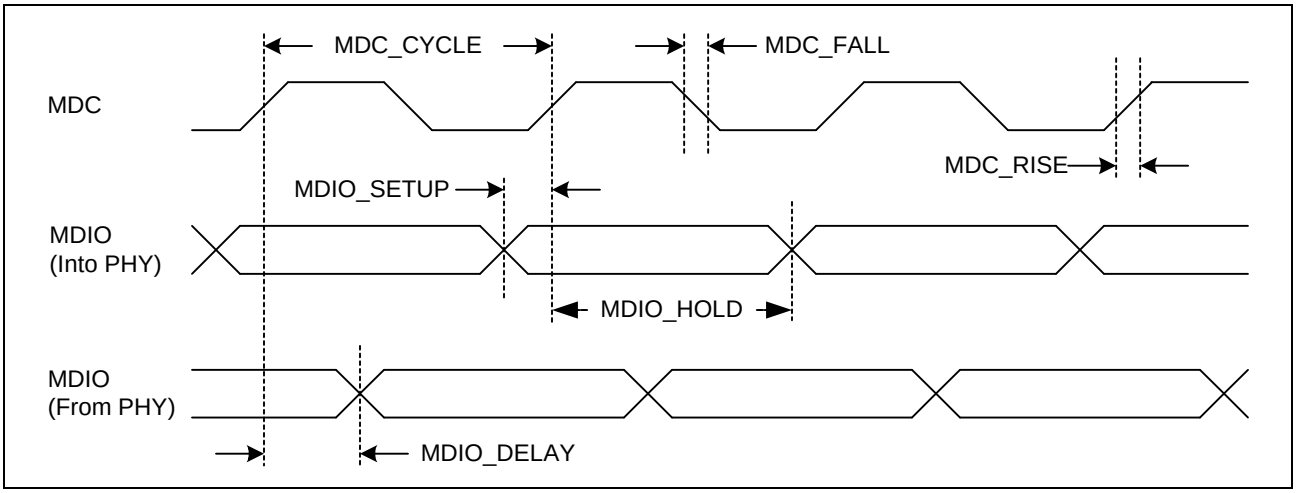


Management Interface Timing

Table 29: Management Interface Timing

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
MDC cycle time	MDC_CYCLE	80	–	–	ns
		–	–	12.5	MHz
MDC duty cycle	MDC_HI/LOW	30	–	70	%
MDIO input setup time to MDC rising	MDIO_SETUP	5	–	–	ns
MDIO input hold time from MDC rising	MDIO_HOLD	5	–	–	ns
MDIO output delay from MDC rising	MDIO_DELAY				
OVDDMDIO = 3.3V or 2.5V		5	–	15	ns
OVDDMDIO = 1.2V		5	–	50	ns

Figure 24: Management Interface Timing

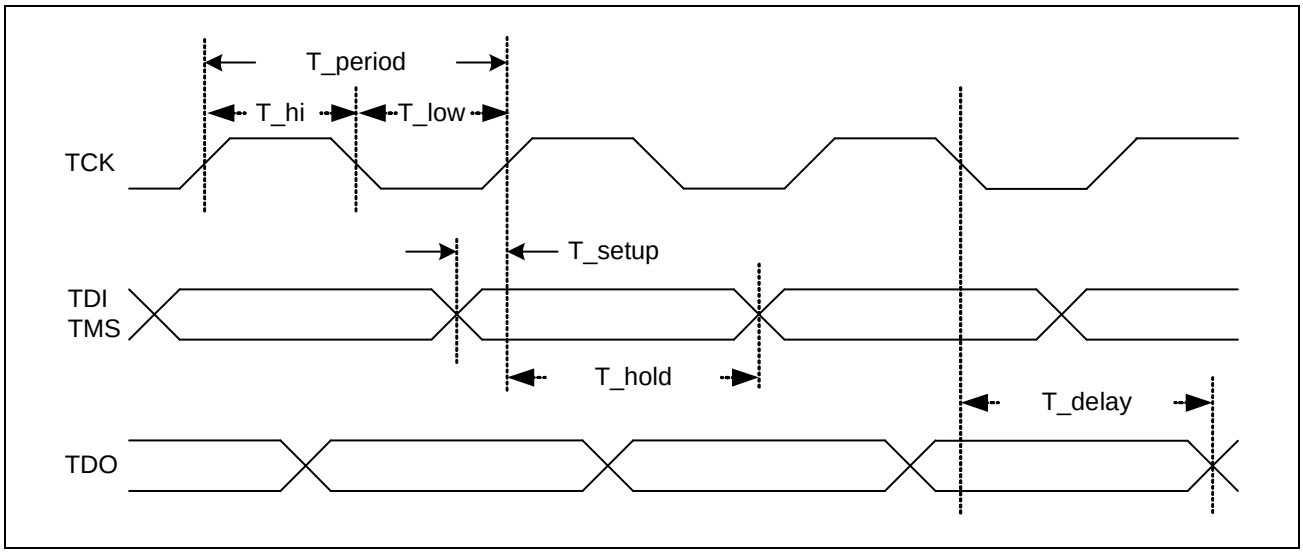


JTAG Timing

Table 30: JTAG Timing

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*
TCK Period	T_period	50	–	ns
TCK High Time	T_hi	15	–	ns
TCK Low Time	T_low	15	–	ns
TDI/TMS Set-up Time	T_setup	10	–	ns
TDI/TMS Hold Time	T_hold	5	–	ns
TCK to TDO Delay (5 pf load)	T_delay	4.5	20	ns

Figure 25: JTAG Timing



Section 10: Electrical Characteristics

Absolute Maximum Ratings

Table 31: Absolute Maximum Ratings

Parameter	*Min.*	*Max.*	*Unit*
1.0V supplies AVDDL, DVDD, PLLVDD, QRVDD, QTVDD, QPVDD,	GND – 0.5	1.37	V
1.2V supplies OVDDMDI0	GND – 0.5	1.37	V
1.8V supplies OVDDJTAG	GND – 0.5	2.10	V
2.5V supplies OVDDMDIO, OVDDJTAG	GND – 0.5	3.10	V
3.3V supplies AVDDH, BIASVDD, OVDD, OVDDMDIO, OVDDJTAG, CLKVDD	GND – 0.5	4.10	V
Digital input overshoot: < 700 mV above power rail for less than 3 ns. Overshoot: For any 3.3V I/O, the absolute maximum overshoot needs to be less than 4.1V. Recommend limiting the I/O overshoot to be less than 500 mV above OVDD supply for no more than 5% duty cycle.	OVDD + 0.700	–	V
Digital input undershoot: < 700 mV below ground for less than 3 ns. Undershoot: If the I/O undershoot is less than 500 mV below ground, there is no duration timing requirement. If the I/O undershoot is less than 700 mV below ground, it needs to be less than 3 ns duration.	GND – 0.700	–	V
Storage temperature	–40	125	°C
ESD protection	±1000	–	V
Note: These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.			

DC Characteristics

Power Parameters

Table 32: Recommended Power Supply Voltage Levels

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Supply voltage 1.0V	V_{AVDDL} V_{DVDD} V_{PLLVDD} V_{QTVDD} V_{QRVDD} V_{QPVDD}	0.95	1.0	1.05	V
Supply voltage 1.2V (3.3V tolerant)	$V_{OVDDMDIO}$	1.14	1.2	1.26	V
Supply voltage 1.8V (3.3V tolerant)	$V_{OVDDJTAG}$	1.71	1.8	1.89	V
Supply voltage 2.5V (3.3V tolerant)	$V_{OVDDMDIO}$ $V_{OVDDJTAG}$	2.375	2.5	2.625	V
Supply voltage 3.3V	V_{OVDD} V_{AVDDH} $V_{BIASVDD}$ V_{CLKVDD} $V_{OVDDMDIO}$ $V_{OVDDJTAG}$	3.135	3.3	3.465	V

Table 33: QSGMII to Copper Current Consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit
3.3V digital supply current	I_{OVDD} $I_{OVDDMDIO}$ $I_{OVDDJTAG}$	–	2	–	mA
3.3V analog supply current	I_{AVDDH} $I_{BIASVDD}$ I_{CLKVDD}	–	427	–	mA
1.0V digital supply current	I_{DVDD}	–	485	–	mA
1.0V analog supply current	I_{AVDDL} I_{PLLVDD} I_{QTVDD} I_{QRVDD} I_{QPVDD} $I_{SPLLVDD}$	–	395	–	mA
Total power	P_{Total}	–	2296	–	mW
Power per port	P_{PP}	–	287	–	mW

Note: Over process, voltage and temperature, the maximum power dissipation is approximately 15% to 20% higher than the typical value.

I/O Parameters

Table 34: I/O Operating at OVDD = 3.3V

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage	V_{IH}	2.00	–	V	–
Input low voltage	V_{IL}	–	0.80	V	–
Output high voltage	V_{OH}	OVDD – 0.40	–	V	I_{OH} = –8 mA
Output low voltage	V_{OL}	–	0.40	V	I_{OL} = 8 mA

Table 35: I/O Operating at OVDD = 2.5V

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage	V_{IH}	1.70	–	V	–
Input low voltage	V_{IL}	–	0.80	V	–
Output high voltage	V_{OH}	OVDD – 0.40	–	V	I_{OH} = –8 mA
Output low voltage	V_{OL}	–	0.40	V	I_{OL} = 8 mA

MDIO/MDC Parameters

Table 36: MDIO/MDC: OVDDMDIO Operating at 3.3V

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage	V_{IH}	2.00	–	V	–
Input low voltage	V_{IL}	–	0.80	V	–
Output high voltage	V_{OH}	OVDD – 0.40	–	V	I_{OH} = –8 mA
Output low voltage	V_{OL}	–	0.40	V	I_{OL} = 8 mA

Table 37: MDIO/MDC: OVDDMDIO Operating at 2.5V

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage	V_{IH}	1.70	–	V	–
Input low voltage	V_{IL}	–	0.70	V	–
Output high voltage	V_{OH}	OVDD – 0.40	–	V	I_{OH} = –8 mA
Output low voltage	V_{OL}	–	0.40	V	I_{OL} = 8 mA

Table 38: MDIO/MDC: OVDDMDIO Operating at 1.2V

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage	V_{IH}	0.84	–	V	–
Input low voltage	V_{IL}	–	0.36	V	–
Output high voltage	V_{OH}	OVDD – 0.40	–	V	I_{OH} = –8 mA
Output low voltage	V_{OL}	–	0.40	V	I_{OL} = 8 mA

JTAG Parameters

Table 39: JTAG: OVDDJTAG Operating at 3.3V

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage	V_{IH}	2.00	–	V	–
Input low voltage	V_{IL}	–	0.80	V	–
Output high voltage	V_{OH}	OVDD – 0.40	–	V	I_{OH} = –8 mA
Output low voltage	V_{OL}	–	0.40	V	I_{OL} = 8 mA

Table 40: JTAG: OVDDJTAG Operating at 2.5V

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage	V_{IH}	2.00	–	V	–
Input low voltage	V_{IL}	–	0.70	V	–
Output high voltage	V_{OH}	OVDD – 0.45	–	V	I_{OH} = –8 mA
Output low voltage	V_{OL}	–	0.40	V	I_{OL} = 8 mA

Table 41: JTAG: OVDDJTAG Operating at 1.8V

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage	V_{IH}	1.22	–	V	–
Input low voltage	V_{IL}	–	0.60	V	–
Output high voltage	V_{OH}	OVDD – 0.40	–	V	I_{OH} = –8 mA
Output low voltage	V_{OL}	–	0.40	V	I_{OL} = 8 mA

Reference Clock Parameters

Table 42: Single-Ended Reference Clock

Parameter	Symbol	Min.	Max.	Unit	Condition
Input high voltage	V_{IH}	2.1	–	V	–
Input low voltage	V_{IL}	–	0.70	V	–

Table 43: CML Differential Reference Clock

Parameter	Symbol	Min.	Max.	Unit	Condition
Reference clock input voltage swing differential	V_{pk-pk}	600	2000	mVppd	–
Differential Input Impedance	R_{IN}	90	130	Ω	–
Duty Cycle	%	40	60	%	–

QSGMII Parameters

Table 44: QSGMII Transmitter

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Baud rate	T_{Baud}	–	5.000	–	Gsym/s	–
Output differential voltage[a]	T_{DIFF}	400	–	1200	mVppd	Floating load R_{load} = 100Ω
Differential resistance	T_{RD}	80	100	120	Ω	–
Output rise and fall times	T_R, T_F	30	–	–	ps	20% to 80%
Differential output return loss	T_{SDD22}	–	–	–8	dB	100 MHz to 2.5 GHz
		–	–	–	dB	2.5 GHz to 5 GHz
Common mode return loss	T_{SCC22}	–	–	–6	dB	100 MHz to 2.5 GHz
Output common mode noise	TN_{CM}	–	–	5% of T_{DIFF}	mVppd	–
Output current short	T_{IS}	–	–	100	mA	Output shorted to GND or to each other.
Output common mode voltage	T_{CM}	550		1060	mV	Load Type 2[b]

a. Output differential voltage is programmable through bits[10:6] in QSGMII Address:
BAR = 0x8060, REGAD = 0x17, AER = 0x0000 for QSGMII[0] and AER = 0x0004 for QSGMII[1]

b. Load Type 2 specified per the IA # OIF-CEI-02.0 specification.

Table 45: QSGMII Transmit Jitter

Parameter	Symbol	Min.	Typ.	Max.	Unit
Uncorrelated high probability jitter	T_{UHPJ}	–	–	0.15	UIpp
Duty cycle distortion	T_{DCD}	–	–	0.05	UIpp
Total jitter	T_{TJ}	–	–	0.30	UIpp
Eye mask	T_{X1}	–	–	0.15	UI
	T_{X2}	–	–	0.40	UI
	T_{Y1}	200	–	–	mV
	T_{Y2}	–	–	450	mV

Figure 26: QSGMII Transmit Eye Mask

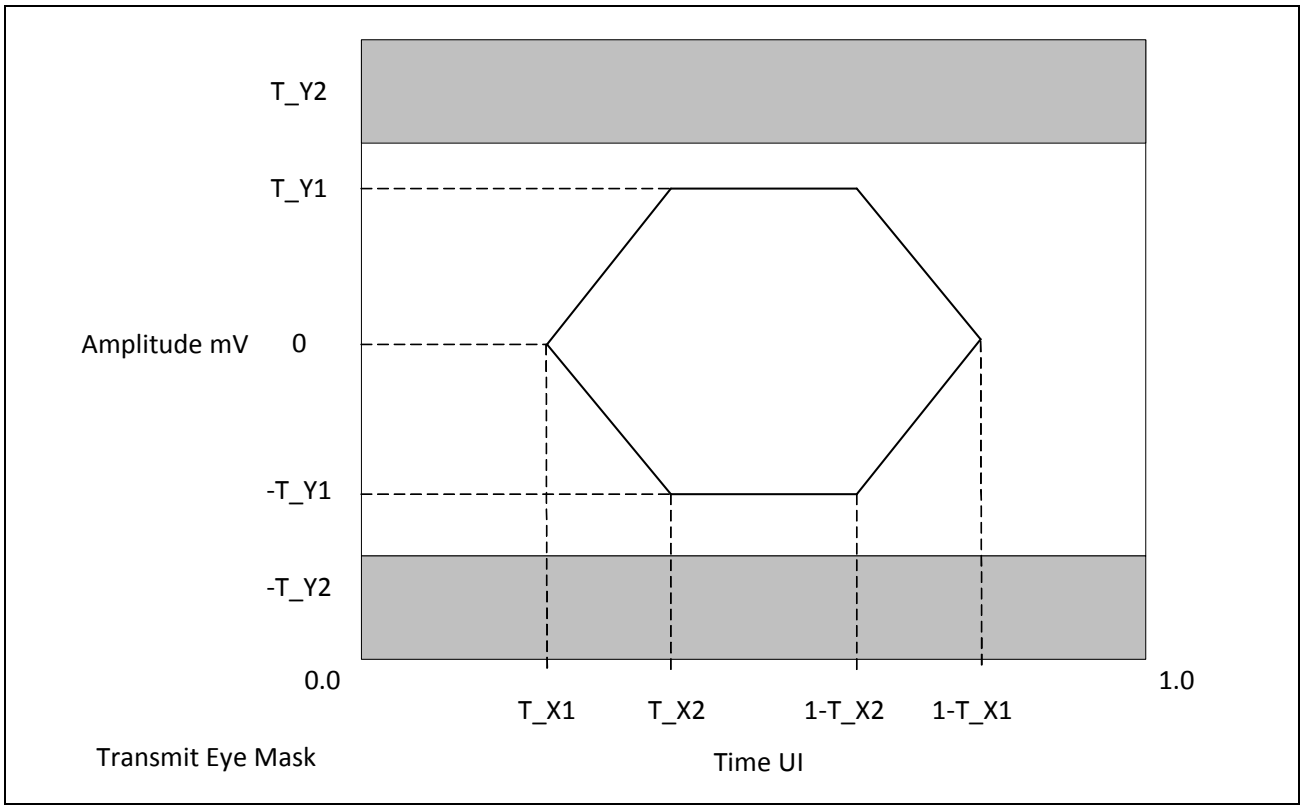


Table 46: QSGMII Receiver

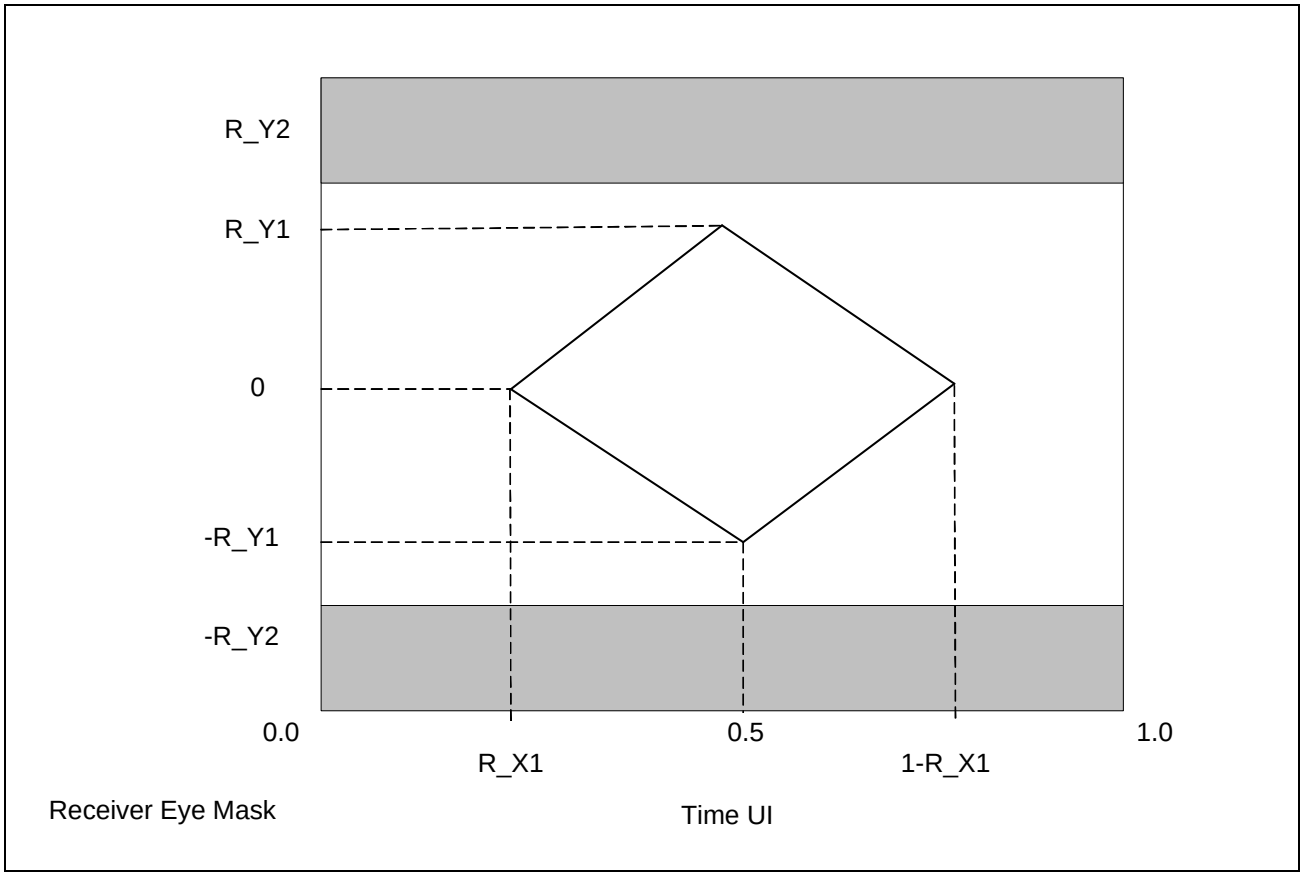
Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*	*Notes*
RX Baud rate	R_{BAUD}	–	5.0	–	Gsym/s	–
Input differential voltage	R_{DIFF}	100	–	900	mVppd	–
Differential resistance	R_{RDIN}	80	100	120	Ω	Load Type 2[a]
Bias voltage source impedance	R_{ZVTT}	–	–	30	Ω	Load Type 2
Differential input return loss	R_{SDD1}	–	–	30	Ω	100 MHz to 2.5 GHz
		–	–	–8	dB	2.5 GHz to 5 GHz
Common mode input return loss	R_{SCC1}	–	–	–6	dB	100 MHz to 2.5 GHz
		Loss dB = A0+16.6*log(f/2.5 GHz)			dB	f = 2.5 GHz to 5.0 GHz
Termination voltage	R_{VTT}	1.0 – 8%	–	1.0 + 5%	V	R_{VTT} = 1.0V nominal Load Type 2
Input common mode voltage	R_{CM}	535	–	R_{VTT} + 125 mV	mV	R_{VTT} = 1.0V nominal Load Type 2
Wander divider	n	–	–	10	–	–

a. Load Type 2 specified per the IA # OIF-CEI-02.0 specification.

Table 47: QSGMII Receive Jitter

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Bounded high probability jitter	R_{BHPJ}	–	–	0.45	UIpp
Sinusoidal jitter, maximum	R_{SJ-max}	–	–	5	UIpp
Sinusoidal jitter, high frequency	R_{SJ-hf}	–	–	0.05	UIpp
Total jitter (does not include sinusoidal jitter)	R_{TJ}	–	–	0.60	UIpp
Eye mask	R_{X1}	–	–	0.30	UI
	R_{Y1}	200	–	50	mV
	R_{Y2}	–	–	450	mV

Figure 27: QSGMII Receive Eye Mask



Section 11: Packaging Information

Thermal

This section includes thermal information for the B50282 package. Thermal numbers are based on JEDEC standards for 2s2p PCB (4 layer PCB board), wind tunnel and still air enclosures, therefore the temperatures might be different in the customers environment. Table 48 provides $Theta_{JB}$ and $Theta_{JC}$ data. Table 49 on page 97 provides $Theta_{JA}$ and Psi_{JT} thermal data.

Note: Maximum steady state die junction temperature in a stable environment of device ambient, airflow or heat sink is 110°C.

Note: Maximum excursion die junction temperature due to the loss of airflow or heat sink integrity or due to significant fluctuation of device ambient temperature or other events is 125°C. The duration of the excursion should be less than 1000 hours for the lifetime of the product.

Table 48: $Theta_{JB}$ and $Theta_{JC}$ Data

Parameter	*Value*	*Units*
θ_{JB}	13.58	°C/W
θ_{Jc}	10.82	°C/W

Table 49: $Theta_{JA}$ and Psi_{JT} Thermal Data

Air Velocity (m/s)	*0*	*0.508*	*1.016*	*2.032*	*3.048*	*Condition*
Air Velocity (ft/min)	*0*	*100*	*200*	*400*	*600*	
θ_{JA} (°C/W)	27.40	25.35	23.84	22.42	21.42	No heat sink
Ψ_{JT} (°C/W)	2.48	2.50	2.57	2.67	2.81	
θ_{JA} (°C/W)	20.42	16.95	15.01	13.80	13.47	External heat sink[a]
Ψ_{JT} (°C/W)	8.01	8.20	8.39	8.50	8.52	
θ_{JA} (°C/W)	20.28	16.90	14.70	13.25	12.91	External heat sink[b]
Ψ_{JT} (°C/W)	8.05	8.21	8.44	8.59	8.62	

a. Heat sink: 21x21x20 mm fin type heat sink, aluminum
b. Heat sink: 23x23x20 mm fin type heat sink, aluminum

Thermal Data Definitions

The thermal models for package Junction-to-Board ($Theta_{JB}$) and Junction-to-Case ($Theta_{JC}$) thermal resistances are constructed based on generic thermal resistance definitions. The simulated θ_{JB} and θ_{JC} values depend on package internal construction only. They are not dependent on the PCB used in either tests or applications. The simulated θ_{JB} and θ_{JC} values provide a package two-resistor compact model. The following are the equations for θ_{JA}, θ_{JB}, and θ_{JC}.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

Where:

- T_J = Junction temperature at steady-state condition. Units = °C.
- T_A = Package case top center temperature at steady-state condition. Units = °C.
- T_B = Package lead footprint temperature specified in thermal simulation. Units = °C.
- T_C = package case top surface temperature specified in thermal simulation. Units = °C.
- P = Device power dissipation. Units = Watts.

Psi_{JT} Versus $Theta_{JC}$ Junction Temperature Estimation

Package thermal characterization parameter Psi-J_T (Ψ_{JT}) yields a better estimation of actual device junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-J_C (θ_{JC}). The reason for this is θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom and sides of the package. The equation for calculating the device junction temperature is as follows.

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

- T_J = Junction temperature at steady-state condition. Units = °C.
- T_T = Package case top center temperature at steady-state condition. Units = °C.
- P = Device power dissipation. Units = Watts.
- Ψ_{JT} = Package thermal characteristics. Units = °C/W.

RoHS-Compliant Packaging

Broadcom's RoHS packages are in compliance with RoHS and WEEE directives. Broadcom may also offer standard parts that are also in compliance with these directives, with the exception of Pb (>1000 ppm). Table 50 shows the main differences between standard and RoHS-compliant parts.

RoHS-compliant parts have a letter 'G' added to the top line of the part marking. Standard parts (non Pb-free parts) are not compatible to the Pb-free surface mount process. See Section 12: "Ordering Information," on page 101 and refer to the following application notes:

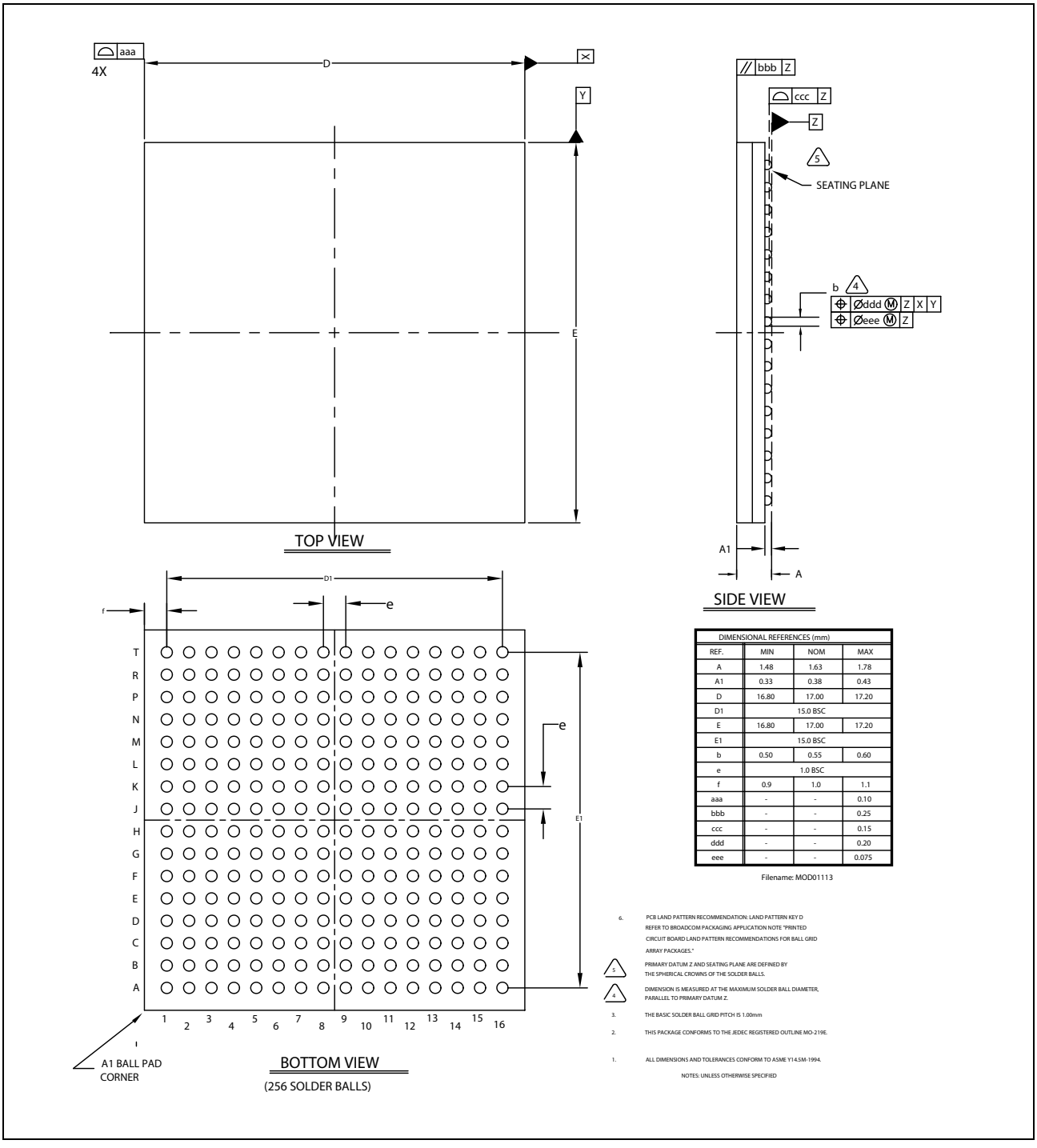
- *Reflow Process Guidelines for Surface Mount Assemblies* (PACKAGING-AN10x-R).
- *Printed Circuit Board Land Pattern Recommendations for Ball Grid Array* (Packaging-AN50x-R)

Table 50: Standard and RoHS-Compliant Package Differences

Package	*Solder Ball Composition*	*Maximum Reflow Temperature (°C)*
Standard package	63%Sn/37%Pb	225
RoHS-compliant package	96.5%Sn/3%Ag/0.5%Cu	255

Mechanical Information

Figure 28: 256-Ball FBGA Package



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	1.48	1.63	1.78
A1	0.33	0.38	0.43
D	16.80	17.00	17.20
D1		15.0 BSC	
E	16.80	17.00	17.20
E1		15.0 BSC	
b	0.50	0.55	0.60
e		1.0 BSC	
f	0.9	1.0	1.1
aaa	-	-	0.10
bbb	-	-	0.25
ccc	-	-	0.15
ddd	-	-	0.20
eee	-	-	0.075

Filename: MOD01113

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY D REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-219E.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Section 12: Ordering Information

Table 51: Ordering Information

Part Number	*Package*	*Ambient Temperature*
B50282C1KFBG	256-ball FBGA (RoHS-compliant)	0°C to 70°C

Appendix A: Acronyms and Abbreviations

Table 52 lists of acronyms and abbreviations applies specifically to Broadcom and associated products. These lists are updated regularly. If a term is not listed, but should be, contact a Broadcom representative.

For a more complete list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Table 52: Acronyms and Abbreviations

Term	*Description*
ADC	Analog-to-digital converter
APD	Auto Power-Down
BER	Bit error rate
BSC	Broadcom Serial Control
CESD	Cable electrostatic discharge
CF	Correction Fields
CLI	Command Line Interface
CML	Current/Common Mode Logic
CSP	Customer Support Portal
DAC	Digital-to-analog converter
DPLL	Digital Phase-Locked Loop
DFE	Decision-Feedback Equalization
EEE	Energy Efficient Ethernet
EOL	End-of-line
EMI	Electromagnetic interference
ESD	Electrostatic discharge
ESD	End-of-stream-deliminator
FBGA	Fine pitch ball grid array
FEC	Forward error correction
FFE	Feed-forward equalization
HCD	Highest common denominator
ISI	Intersymbol interference
JTAG	Joint Test Action Group
LFSR	Linear Feedback Shift Register
LLDP	Link Layer Discovery Protocol
LPI	Low-power idle
GM	Grand Master
GUI	Graphical user interface
LPI	Low-power idle
MDI	Media Dependent Interface
MDIO	Management data input/output

Table 52: Acronyms and Abbreviations

Term	*Description*
NSE	Network Synchronization Engine
NEXT	Near-end crosstalk
NRZ	Nonreturn to Zero
PDU	Protocol data unit
PHY	Physical layer
QSGMII	Quad Serial Gigabit Media Independent Interface
SC	Slave Clock
SFD	Start-of-frame-deliminator
SGMII	Serial Gigabit Media Independent Interface
RX_ER	Receive Error
SFD	Start Frame Delimiter
SoC	System-on-a-Chip
TC	Transparent Clock
UTP	Unshielded twisted pair: A twisted pair medium consisting of only a pair of conductors exposed to outside electrical interferences and noise.
WDT	Watchdog timer

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