

# 24-Port GbE Unmanaged Switch with 16 Copper PHYs

## GENERAL DESCRIPTION

The Broadcom® BCM53334 System-on-a-Chip (SoC) switch family offers industry-leading integration and performance in a small footprint. The device offers up to 2416 multilayer GbE ports in a 23 mm x 23 mm package. Offering the industry's highest level of integration, the BCM53334 has embedded 16 GPHYs and a powerful 125 MHz ARM Cortex-A9 single-core processor. The BCM53334 is ideal for cost-sensitive edge connectivity applications, such as unmanaged and WebSmart™-lite WebSmart™ switches for Small Medium Business.

The BCM53334 device offers multiple I/O configurations that address key segments of edge connectivity. A single BCM53334 device supports the popular 2416x GbE switch designs.

Furthermore, the BCM53334 device I/O is optimized for board layout. When used with the Broadcom QSGMII PHY, the BCM53334 device can be connected to the PHYs without any trace crossovers. The optimized I/O map reduces system design effort and enables low-cost PCB design.

The BCM53334 device offers many advanced features, such as IEEE 802.1Q VLAN, enhanced Denial of Service (DoS) protection, IPv4 and IPv6 support, advanced ContentAware™ Engine, IEEE 802.1p Quality of Service (QoS), Energy Efficient Ethernet™ (EEE)

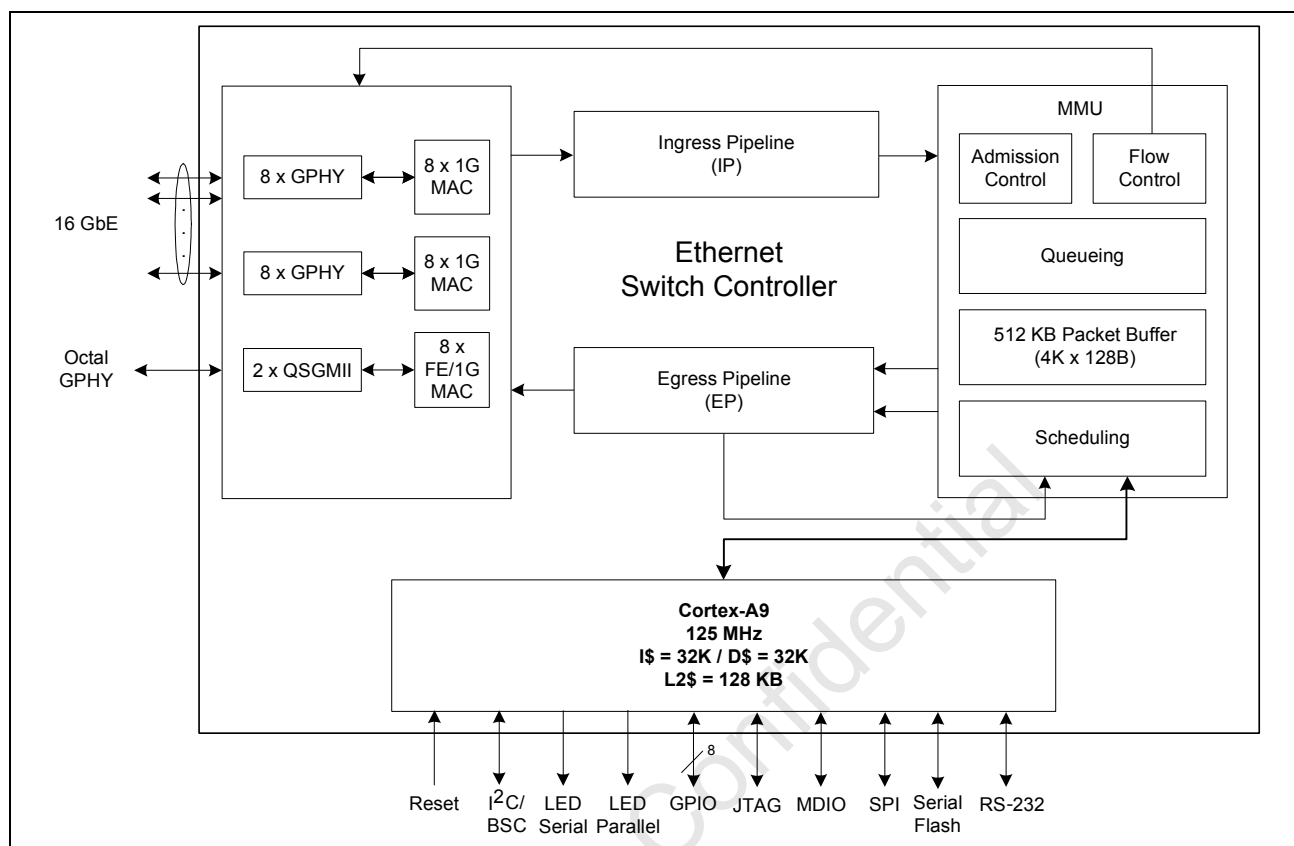
## BENEFITS

- Based on industry-leading and market-proven StrataXGS® IV architecture.
- Single-chip switch SoC optimized for unmanaged and WebSmart™-lite connectivity applications for SMB networks.
- Enhanced memory technology delivers optimum usage of packet-buffer resources.
- Eight flexible Class of Service (CoS) queues per port assure the lowest latency to high-priority traffic.
- IPv6 support provides future-proofing.
- Optimized ball pattern for low-cost PCB design and single-system clock source.
- Low-power 40 nm CMOS technology.

## FEATURES

- Highly integrated 2416-port 10/100/1000 Mbps Ethernet switch SoC.
- Embedded 16 integrated copper 10/100/1000 EEE PHYs.
- Two integrated QSGMII/1GbE interfaces
- Non-blocking architecture, line rate for all packet sizes.
- Fully integrated 512 KB packet buffer
- Intelligent Memory Management Unit (MMU) optimized for handling bursty data traffic.
- IPv4/IPv6 support.
- Flexible Access Control List (ACL).
- Enhanced DoS attack statistics gathering.
- Low-power Energy Efficient Ethernet (EEE) support with Burst and Batch control policy.
- AVB support.
- Support for Industrial Temperature.
- 40 nm CMOS process.

**Figure 1: BCM53334 Functional Block Diagram**



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## Revision History

| <i>Revision</i> | <i>Date</i> | <i>Change Description</i>   |
|-----------------|-------------|---|
| 53334-DS06-R    | 12/19/14    | <b>Updated:</b> <ul style="list-style-type: none"><li>• <a href="#">Table 38: "Ordering Information for RoHS6 Devices with Exemption 15 (Eutectic Bumps Internally Between Die and Substrate)," on page 97</a></li></ul> <b>Added:</b> <ul style="list-style-type: none"><li>• <a href="#">Table 37: "Ordering Information for RoHS6 Devices (Contact Broadcom for Availability)," on page 97</a></li></ul> |
| 53334-DS05-R    | 07/18/14    | <b>Updated:</b> <ul style="list-style-type: none"><li>• Change Advanced Data Sheet to Data Sheet.</li><li>• "Power Supply Current" on page 79 - Added power column to Power Supply Current Tables.</li></ul>  |

| Revision     | Date     | Change Description  |
|--------------|----------|---|
| 53334-DS04-R | 04/23/14 | <p><b>Updated:</b></p> <ul style="list-style-type: none"> <li>Changed AVS0 pin description to 'Reserved' in Table 8: "BCM5333X Hardware Signals," on page 54</li> <li>Table 12: "Operating Conditions," on page 77 - Remove 0.97V option and change 1.2V to <math>\pm 3\%</math>.</li> <li>Table 17: "BSC Signals," on page 81 <ul style="list-style-type: none"> <li>Input Low Voltage from 1.08V to <math>0.3 \cdot V_{DDO}</math>.</li> <li>Input High Voltage from 2.1V to <math>0.7 \cdot V_{DDO}</math>.</li> </ul> </li> <li>Table 23: "SPI Slave Fast Mode Timing," on page 86 - Change <math>t_{hold}</math> from 0 to 4 ns.</li> <li>Table 24: "MDC/MDIO Timing," on page 87 <ul style="list-style-type: none"> <li>MDC Cycle Time from 74 to 80 ns.</li> <li>MDIO Setup Time from 10 to 20 ns.</li> <li>MDIO hold time from 0 to 10 ns.</li> </ul> </li> <li>Table 26: "QSPI BSPI Mode Master Interface Timing Specifications," on page 89 <ul style="list-style-type: none"> <li><math>T_{WH}</math> from <math>\frac{1}{2}T_{CK}-3</math> to <math>0.4 \cdot T_{CK}</math> and max. <math>0.6 \cdot T_{CK}</math>.</li> <li><math>T_{WL}</math> from <math>\frac{1}{2}T_{CK}-3</math> to <math>0.4 \cdot T_{CK}</math> and max. <math>0.6 \cdot T_{CK}</math>.</li> <li>Updated footnote a.</li> </ul> </li> <li>Table 27: "QSPI MSPI Mode Master Interface Timing Specifications," on page 90 <ul style="list-style-type: none"> <li><math>T_{WH}</math> from <math>\frac{1}{2}T_{CK}-3</math> to <math>0.4 \cdot T_{CK}</math> and max. <math>0.6 \cdot T_{CK}</math>.</li> <li><math>T_{WL}</math> from <math>1/0.6F_{CLK}</math> to <math>0.4 \cdot T_{CK}</math> and max. <math>0.6 \cdot T_{CK}</math>.</li> <li>Updated footnote a.</li> </ul> </li> <li>Table 29: "XTALP/XTALN Input Requirements," on page 92 <ul style="list-style-type: none"> <li>Change <math>V_{IN}</math> Min. from 500 to 800 mV<sub>pp diff</sub>.</li> <li>Change "Internal 100<math>\Omega</math> termination" to "External 100<math>\Omega</math> termination required."</li> </ul> </li> <li>Table 30: "LC_PLL0_REFCLK Input Requirements," on page 93 <ul style="list-style-type: none"> <li>Remove Min/Max Input Voltage <math>V_{IL}</math> and <math>V_{IH}</math></li> <li>Change <math>V_{IN}</math> Min. from 500 to 700 mV<sub>pp diff</sub></li> </ul> </li> <li>Table 31: "EXT_QS2_CLKP/N Output Specifications," on page 94 <ul style="list-style-type: none"> <li>Change <math>V_{ODIFF}</math> Min from 500 to 300 mV<sub>pp diff</sub> and Max from 2000 to 500 mV<sub>pp diff</sub>.</li> <li>Remove Min/Max Output Voltage <math>V_{OL}</math> and <math>V_{OH}</math></li> <li>Change EXT_QS2_CLK Rise/Fall time from 1.0 to 0.22 ns Max.</li> <li>Change EXT_QS2_CLK jitter from 0.5 to 2 ps Max.</li> <li>Remove Note: Internal 100<math>\Omega</math> termination.</li> <li>Measured with 50<math>\Omega</math> termination as recommended in the Hardware Design Guide.</li> </ul> </li> <li>Table 35: "AC-JTAG Transmit Setting (Driver Bias Current)," on page 98 - the Transmit Amplitude of the entire table.</li> <li>"Power Supply Current" on page 79</li> <li>Section 9: "Thermal Characteristics," on page 99</li> </ul> <p><b>Removed:</b></p> <ul style="list-style-type: none"> <li>Hardware strapping pin description to enable Super Isolate Mode.</li> <li>MII Interface Timing.</li> </ul> |

| <b>Revision</b> | <b>Date</b> | <b>Change Description</b>  |
|-----------------|-------------|--|
| 53334-DS03-R    | 07/03/13    | <b>Updated:</b> <ul style="list-style-type: none"> <li>• For power sequencing add requirement to power up the core VDDC at the same time or before GP-AVDDL SUPPLY.</li> <li>• Remove SGMII/SerDes DC Characteristics</li> <li>• Update Parallel LED Interface.</li> <li>• Table 1: "5615X_5333X_5334XCT SoC Port Configurations," on page 14 - Remove DSCP</li> <li>• Table 2: "Switch Features," on page 29 - Adjust table sizes.</li> <li>• Table 3: "Switch Internal Memory Table," on page 35 - Remove DSCP</li> <li>• Table 15: "5615X_5333X_5334XCT Hardware Signals," on page 83 - Add PU/PD</li> <li>• Section 7: "Pin List Description" - Add PU/PD</li> </ul> |
| 53334-DS02-R    | 04/05/13    | <b>Updated:</b> <ul style="list-style-type: none"> <li>• Update entire document.</li> <li>• "Pin List by Signal Name" on page 143</li> <li>• "AC Characteristics" on page 192</li> </ul>   |
| 53334-DS01-R    | 12/21/12    | Updated entire document.   |
| 53334-DS00-R    | 09/26/12    | Initial release  |

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## About This Document

### Purpose and Audience

This document describes the Broadcom® BCM53334 System on Chip (SoC). The Broadcom BCM53334 integrates a high-performance 125 MHz ARM Cortex-A9 processor and an Ethernet Switch controller with 24 multilayer GbE ports. This document is intended for hardware design, application, and OEM engineers.

### Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

Acronyms and abbreviations in this document are also defined in [Appendix A: “Acronyms and Abbreviations,” on page 98](#).

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to:  
<http://www.broadcom.com/press/glossary.php>.

### Document Conventions

The following conventions may be used in this document:

| Convention             | Description   |
|------------------------|---|
| <b>Bold</b>            | User input and actions: for example, type <b>exit</b> , click <b>OK</b> , press <b>Alt+C</b>  |
| Monospace              | Code: <code>#include &lt;iostream&gt;</code><br>HTML: <code>&lt;td rowspan = 3&gt;</code><br>Command line commands and parameters: <code>w1 [-1] &lt;command&gt;</code> |
| <code>&lt; &gt;</code> | Placeholders for <i>required</i> elements: enter your <code>&lt;username&gt;</code> or <code>w1 &lt;command&gt;</code>  |
| <code>[]</code>        | Indicates <i>optional</i> command-line parameters: <code>w1 [-1]</code><br>Indicates bit and byte ranges (inclusive): <code>[0:3]</code> or <code>[7:0]</code>          |

## References

The references in this section may be used in conjunction with this document.



**Note:** Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads and Support site (see [Technical Support](#)).

## Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (<https://support.broadcom.com>). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads and Support site (<http://www.broadcom.com/support/>).

# Section 1: Introduction



**Note:** This is an Advanced Data Sheet; information presented in this document, including parameters, may change.

## Overview

The Broadcom BCM53334 is a System on Chip (SoC) optimized for power and cost without compromising performance. The BCM53334 integrates:

- A high-performance 125 MHz ARM Cortex-A9 processor
- An Ethernet Switch controller with 24 multilayer GbE ports
- Two QSGMII interfaces
- Up to 16 GbE transceivers

The Broadcom BCM53334 SoC port configurations are shown in [Table 1](#).

**Table 1: BCM53334 SoC Port Configurations**

| <i>Device</i> | <i>GbE Port</i> | <i>QSGMII</i> | <i>TSC 1</i> | <i>TSC 0</i> | <i>L3 Features</i> | <i>L2 Features</i> |
|---------------|-----------------|---------------|--------------|--------------|--------------------|--------------------|
| BCM53334      | 16              | 2             | –            | –            | Yes                | Yes                |

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## Ethernet Switch Controller

The Broadcom® BCM53334 integrates 16 GbE ports with embedded GPHYs and 8 GbE ports through QSGMII interfaces.

The BCM53334 is a highly integrated solution ideally suited for stand-alone GbE switches. The switch controller combines all the functions of a high-speed switch system, including packet buffer, SerDes, media access controllers, address management, and a non-blocking switch fabric. The BCM53334 device supports auto-DoS attack prevention and SNMP, IEEE 802.1x, Spanning Tree, and Rapid Spanning Tree protocols.

The BCM53334:

- Provides 16 full-duplex GbE ports with embedded GPHYs.
- Provides two QSGMII interface to external PHYs for additional 8 full-duplex GbE ports. These GbE ports support both copper and fiber media (via external PHY device).
- Integrates 512KB internal memory in the Common Buffer Pool (CBP) for packet buffering.
- Provides hardware support for IPv4 and IPv6 protocols.
- Supports a Broadcom Serial control (BSC) controller for communicating with external devices such as serial EEPROM, and Flash ROM devices.
- Supports a serial interface for the MII management (MDC/MDIO) of physical layer devices.
- Contains the memory needed to host L2 switching tables.
- Supports advanced QoS.



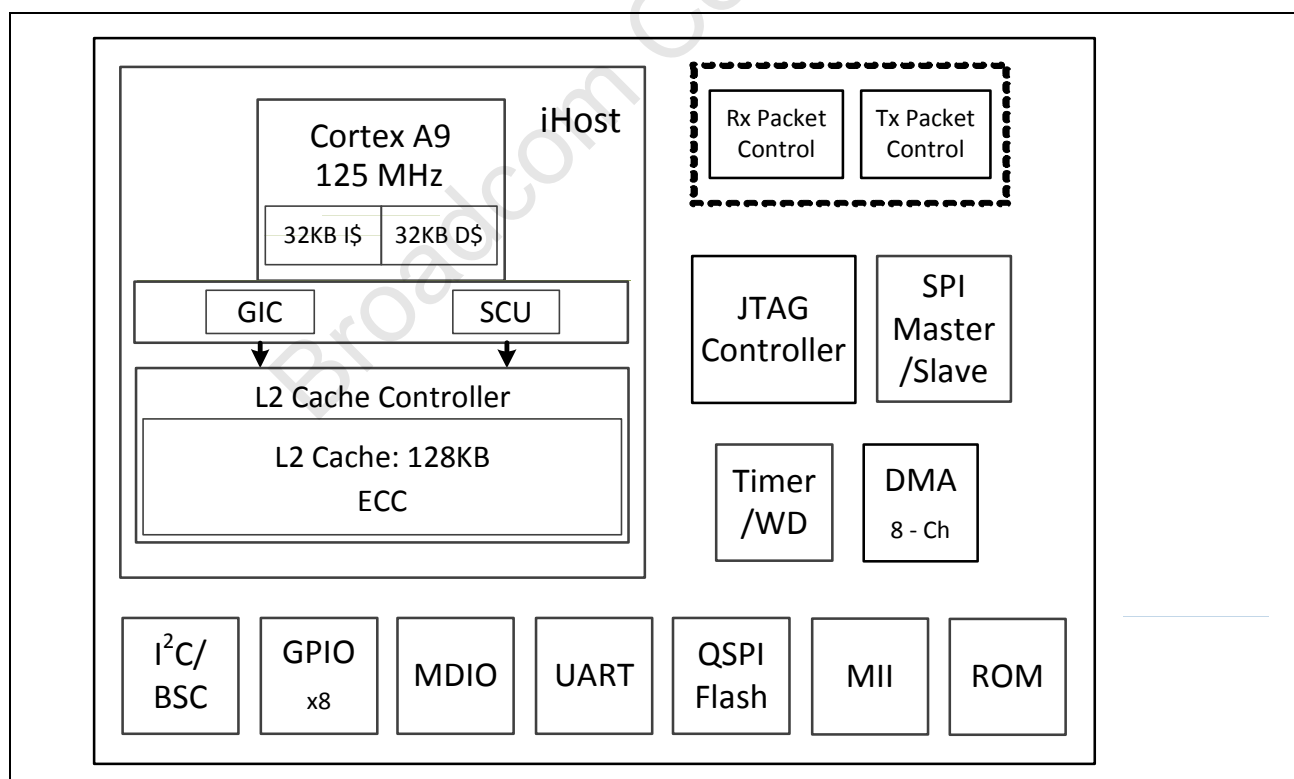
## ARM Cortex-A9 Processor

The BCM53334 Integrates a high-performance 125 MHz ARM Cortex-A9 processor with a 32 KB four-way set associative instruction cache, a 32 KB four-way set associative data cache, and a 128 KB L2 cache. The Cortex-A9 processor offers significant performance improvements in both transfer rates and CPU utilization.

The BCM53334 provides support for serial Flash port. There are up to 8 GPIOs on the Cortex-A9 processor. All inputs are capable of generating processor interrupts.

- Cortex-A9
- Maximum CPU speed 125 MHz
- 32 KB 4-way set associative I-cache and D-cache
- 128K L2 cache
- 128-entry TLB
- Serial flash ports
- 1 port BSC
- 1 UART port
- 8 GPIOs
- 1 MDIO interface
- 1 SPI port

**Figure 2: BCM53334 Embedded Processor Functional Block Diagram**

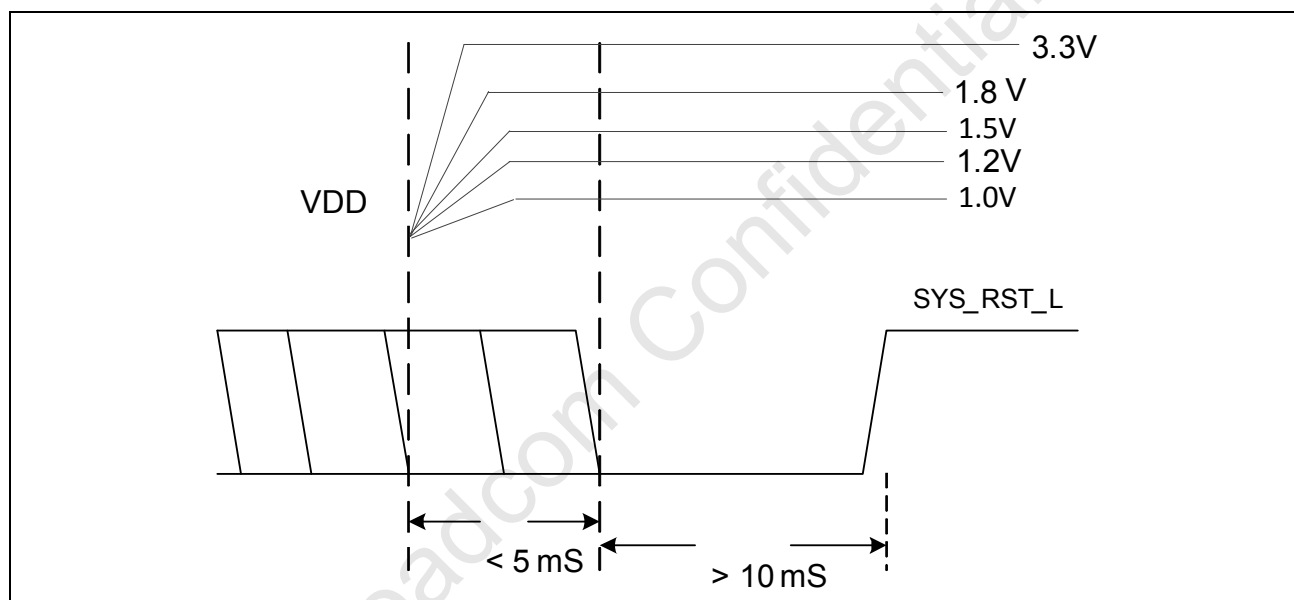


## Section 2: Common Interfaces

### System Reset

Upon system power-up, the device internal logic will stay in reset for roughly 5 ms. The power-up state is achieved when 1.0V, 1.2V, 1.5V, 1.8V, and 3.3V are at steady state voltage. It is recommended that the user asserts SYS\_RST\_L for at least 40 ms after the voltages are stable. Most external Power-on-Reset (POR) devices will properly keep the reset signal low immediately from power-on until the power supply is stable. When using an FPGA/CPLD to drive the reset, a pull-down resistor may be required to ensure the SYS\_RST\_L signal is low. [Figure 3](#) illustrates the reset sequence relative to the ramping power supplies.

Figure 3: System Reset Sequence



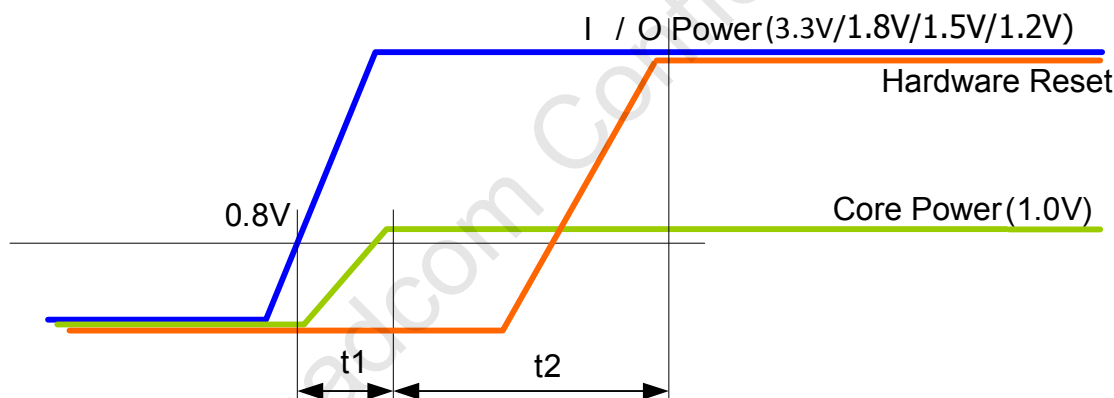
The initialization process loads all the pin configurable modes (such as BSC slave address bits), clears all switching tables that are automatically maintained by the device, and places the switch in a disabled and idle state. Using the active PCIe bus, further initialization must be performed to configure the ports, MACs, and the tables before switching of packets can occur.

## Power Sequencing

As in any multi-supply system, during the power ramp-up period, the I/O pads are in an undetermined state, and bus contention and current spikes could result. This can be minimized by an orderly and rapid power ramp up sequencing:

- The I/O power (3.3V/1.8V/1.5V/1.2V) should come up first, followed by the core power (1.0V). This implies that the core power (1.0V) should not be ON until the I/O power (3.3V/1.8V/1.5V/1.2V) reaches at least 1.0V.
- When the core power reaches the nominal core voltage (1.0V  $\pm$ 5%), the I/O power should be stable at the nominal I/O voltage (3.3V  $\pm$ 5%, 1.8V  $\pm$ 5%, 1.5V  $\pm$ 5%, 1.2V  $\pm$ 5%).
- The maximum ramp-up time for the core power 1.0V (from 0V to nominal voltage  $\pm$ 5%) is  $t_1 = 5$  ms as shown in Figure 4. Additionally, for a successful power-up sequence, Broadcom recommends that the external hardware reset should stay active for at least  $t_2 = 40$  ms after both the I/O and core powers are stable (see Figure 4).
- The VDDC (1.0V core) must be powered up at the same time or before the GP\_AVDDL (1.0V analog) supply.

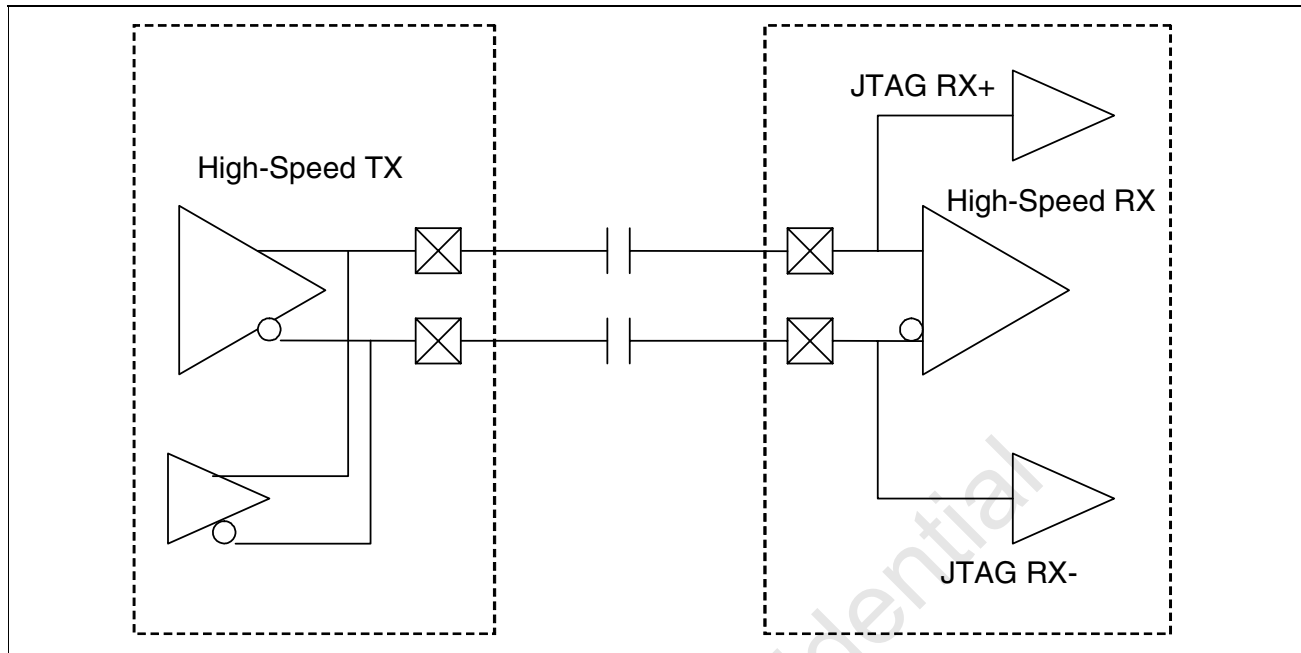
Figure 4: Power Sequencing



## JTAG

Traditional JTAG provides the capability to test for opens and shorts conditions when the device is mounted onto the PCB, based on a direct connection. Present technology, where most high-speed differential signals are required to be AC-coupled, can produce false results due to traditional DC tests for opens and shorts. To provide a means of testing high-speed differential signals, the BCM53334 supports the latest JTAG specification IEEE Std.1149.6 (also known as AC-JTAG). To determine manufacturing faults on a high-speed differential line within a PCB, the device incorporates independent transceivers with low-load capacitance to avoid any adverse effect on the high-speed differential line (see Figure 5).

Figure 5: AC-JTAG Test Block



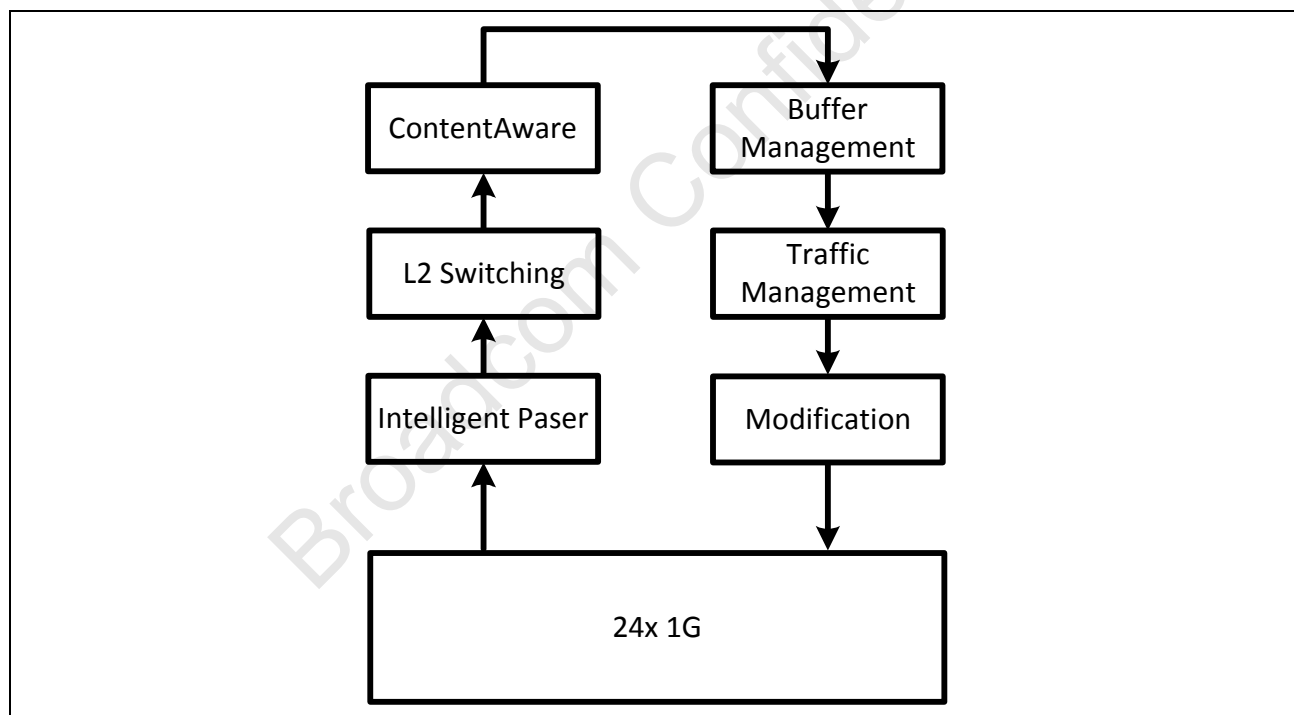
## Section 3: Ethernet Switch Controller Features Description

### Architecture

The integrated Ethernet Switch Controller has a modular, high-performance pipelined packet-switching (BroadScale®) architecture. This enables:

- Cost reduction
- Migration to different process technologies without architectural changes
- Flexible port configurations
- Scalable throughput
- Scalable custom features

**Figure 6: Typical BCM53334 BroadScale Switching Architecture**



## Feature Overview

Some switch features and port counts may vary depending on the device ID (see [“Overview” on page 15](#) for additional details).

**Table 2: Switch Features**

| <b>Feature</b>        | <b>Description</b>  |
|-----------------------|---|
| Configuration         | <ul style="list-style-type: none"> <li>• Versatile port configurations. See <a href="#">Table 1: “BCM53334 SoC Port Configurations,” on page 15</a> for overall configuration</li> <li>• Dynamic buffer management</li> <li>• Supports:               <ul style="list-style-type: none"> <li>– Ethernet/IEEE 802.3 packet sizes (64 bytes to 1522 bytes)</li> <li>– Jumbo packets up to 9216 bytes</li> </ul> </li> </ul>   |
| L2 Switching          | <ul style="list-style-type: none"> <li>• Supports:               <ul style="list-style-type: none"> <li>– Learning up to 8K MAC addresses depending on device</li> <li>– Static entries</li> <li>– MAC limiting per port/LAG/VLAN</li> </ul> </li> <li>• Line rate switching for all packet sizes</li> <li>• Shared and Independent VLAN learning</li> <li>• VLAN flooding for broadcast and DLF packets</li> <li>• Hardware-based address learning</li> <li>• Six CPU-Managed Learning (CML) modes per port</li> <li>• Hardware-and software-based aging</li> <li>• Software insertion/deletion/lookups of the L2 table</li> <li>• Same port bridging supported</li> </ul> |
| L2 Multicast          | <ul style="list-style-type: none"> <li>• Supports 256 L2 multicast groups</li> <li>• Line rate switching for all packet sizes</li> <li>• Three port filtering modes to control multicast packet behavior</li> </ul>   |
| VLAN                  | <ul style="list-style-type: none"> <li>• Supports 4K VLANs and assign VLAN for untagged and priority tagged packet on:               <ul style="list-style-type: none"> <li>– IEEE 802.1p</li> <li>– IEEE 802.1Q</li> </ul> </li> <li>• Port-based VLAN</li> </ul>  |
| Source Port Filtering | <ul style="list-style-type: none"> <li>• Egress port block masks</li> <li>• Trunk group blocking masks</li> </ul>   |

**Table 2: Switch Features (Cont.)**

| <b>Feature</b>           | <b>Description</b>   |
|--------------------------|--|
| Storm Control            | <ul style="list-style-type: none"> <li>• 4 meters for packet-based or byte-based rate control with the below packet types: <ul style="list-style-type: none"> <li>– Unknown unicast (DLF) packet rate control</li> <li>– Broadcast packet rate control</li> <li>– Known L2MC packets rate control</li> <li>– Unknown L2MC packets rate control</li> <li>– Known IPMC packets rate control</li> <li>– Unknown IPMC packets rate control</li> <li>– Enable individual threshold per port</li> </ul> </li> </ul>            |
| Spanning Tree            | <ul style="list-style-type: none"> <li>• Supports: <ul style="list-style-type: none"> <li>– IEEE 802.1D spanning tree protocol (single spanning tree per port).</li> <li>– IEEE 802.1s for multiple spanning trees.</li> <li>– IEEE 802.1w rapid spanning tree protocol—delete and/or replace per Port, per VLAN, or per Port per VLAN.</li> </ul> </li> <li>• Spanning tree protocol packets detected and sent to the CPU.</li> </ul>   |
| 802.3ad Link Aggregation | <ul style="list-style-type: none"> <li>• 128 trunk groups supported with up to eight members per group.</li> <li>• No adjacency limitation.</li> <li>• Traffic load distribution for L2 switched packets.</li> <li>• Trunk port selection based on hash on source/destination MAC, VLAN, EtherType, source/destination IP address, TCP/UDP ports.</li> <li>• Trunk port selection for DLF, broadcast, and multicast packets.</li> </ul>  |
| Mirroring                | <ul style="list-style-type: none"> <li>• Ingress/egress mirroring support.</li> <li>• Mirror-to-port receives unmodified packet for ingress mirroring.</li> <li>• Mirror-to-port receives modified packet for egress mirroring.</li> <li>• Mirroring across stacked modules.</li> <li>• Remote Switched Port Analyzer (RSPAN) mirroring, VLAN mirroring, flow mirroring.</li> <li>• Encapsulated Remote Switched Port Analyzer (ERSPAN) mirroring.</li> <li>• Mirror-to-port can be a link aggregation group.</li> </ul> |

**Table 2: Switch Features (Cont.)**

| <b>Feature</b>                           | <b>Description</b>  |
|--|---|
| ContentAware - Ingress Filter Processing | <ul style="list-style-type: none"> <li>• Up to 512 FP rules with 4 slices allowing 4 parallel lookup and match</li> <li>• Layer 2–7 packet classification</li> <li>• Intelligent Protocol Aware processor with backward compatible byte-based classification option</li> <li>• Parses up to 128 bytes per packet</li> <li>• Multiple look-ups per packet</li> <li>• Supports: <ul style="list-style-type: none"> <li>– Multiple matches and actions per packet</li> <li>– ACL-based policing</li> <li>– Ingress/egress port based filtering</li> <li>– MAC destination address remarking</li> <li>– Class-based marking for SLAs</li> <li>– Traffic class definition based on the filter</li> <li>– Classification of different packet formats (IPv6, IPv4, double tagged, HTLS, IEEE 802.1Q, Ether II, IEEE 802.3)</li> </ul> </li> <li>• Hierarchical min/max programmable meters allows policing of flows</li> <li>• Metering granularity from 8 Kbps to 1 Gbps</li> <li>• Dual leaky bucket meters support two rate three-color marking</li> <li>• srTCM, trTCM, and modified trTCM (RFC2697, RFC2698, RFC4115)</li> <li>• Metering support on ingress ports and CPU queues</li> <li>• Jumbo packet metering</li> <li>• TCP/UDP port number range checking</li> <li>• IPv6 filtering (128 bits)</li> <li>• Filtering IP packets with options</li> </ul> |
| QoS Features                             | <ul style="list-style-type: none"> <li>• Eight CoS queues per port</li> <li>• Enhanced 8 CoS queues for CPU</li> <li>• Three drop precedence colors</li> <li>• Per port, per CoS drop profiles</li> <li>• Minimum/maximum bandwidth guarantee (shaping) per CoS, per port</li> <li>• Traffic shaping available on CPU queues: bandwidth based and packet-per-second based</li> <li>• Programmable priority to CoS queue mapping</li> <li>• Provides two levels of drop precedence per queue</li> <li>• Strict Priority (SP), Weighted Round Robin (WRR), and Deficit Round Robin (DRR) mechanism for shaped queue selection</li> <li>• Programmable bucket size of egress port shaping and COS shaping</li> <li>• Support for ingress port rate based policing and pause flow control</li> <li>• Mapping of incoming priority, CFI to outgoing priority and drop precedence</li> </ul>  |



**Table 2: Switch Features (Cont.)**

| <b>Feature</b>  | <b>Description</b>  |
|---|---|
| Port Security   | <ul style="list-style-type: none"> <li>• Supports 802.1x</li> <li>• Blocking of egress ports on per ingress port or LAG basis (source port filtering)</li> <li>• Blocking of egress ports on per MAC address basis</li> <li>• Blocking of egress ports for broadcast, unknown unicast, and multicast packets</li> </ul>   |
| Denial of Service (DoS) Attack Prevention/Protocol Checkers | <ul style="list-style-type: none"> <li>• Built-in illegal address check (IPv4, IPv6)</li> <li>• Denial of Service detection/prevention</li> <li>• Land packets (SIP = DIP)</li> <li>• NullScan (TCP sequence number = 0, control bits = 0)</li> <li>• Ping flood (flood of IPMC packets)</li> <li>• SYN/SYN-ACK flooding</li> <li>• SYN with sPort &lt; 1024</li> <li>• Smurf attack</li> <li>• Individual control over handling of DOS packet</li> </ul> |
| CPU Protocol Packet Processing                              | <ul style="list-style-type: none"> <li>• Ability to individually control CPU protocol packet handling, including BPDU, Address Resolution Protocol (ARP), Internet Group Management Protocol (IGMP), Multicast Listener Discovery (MLD), and DHCP.</li> <li>• Individual control of trapping protocol packets and setting internal priority</li> <li>• Extensive control of handling of IGMP and MLD packet types</li> </ul>                              |
| Management Information Base                                 | <ul style="list-style-type: none"> <li>• RMON statistics group, IETF RFC2819</li> <li>• SNMP interface group, IETF RFC1213, 2836</li> <li>• Ethernet-like MIB, IETF RFC1643</li> <li>• Ethernet MIB, IEEE 802.3u</li> <li>• Bridge MIB, IETF RFC1493</li> </ul>   |
| Energy Efficient Ethernet™ (EEE)                            | <ul style="list-style-type: none"> <li>• System power saving by informing GPHYs into Low Power Idle (LPI) state.</li> <li>• EEE is only supported on 1GbE ports.</li> </ul>   |

## Memory

The BCM53334 device integrates all table memory necessary to support its functions. [Table 3](#) indicates the major internal table memory allocations and their functions for switching, routing, and classification.

**Table 3: Switch Internal Memory Table**

| Table Name                           | Size                                 | Function  |
|--------------------------------------|--------------------------------------|---|
| Port Table                           | One entry per each GbE, and CPU port | Per port configuration settings and attributes, i.e., L2 learning, port discards, VLAN handling, priority assignment.   |
| VLAN Table                           | 4K VLANs                             | Indicates port membership and spanning tree group for each VLAN.  |
| Spanning Tree Group Table            | 64 groups                            | Indicates spanning tree state for each port for each spanning tree group.   |
| MAC Address Table                    | 8K MAC addresses                     | Contains learned and programmed MAC addresses: indicates destination port and additional properties of each MAC address, i.e., source/destination discard, priority, blocking, mirroring.   |
| Reserved MAC Address Table           | 128 entries                          | Contains reserved MAC addresses, programmed by software for special handling, i.e., copy to CPU, drop, flood, for control packets, BPDUs. Reserved MAC Address table can also be used as an overflow for MAC address table. The only difference between these two tables is that the Reserved MAC table is managed by software. |
| MAC Block Table                      | 32 groups                            | Allows for selective blocking and flooding to egress ports based on source MAC address groups.  |
| Layer 2 Multicast Table              | 256 groups                           | Indicates port membership for Layer 2 multicast groups.   |
| Link Aggregation Group Table         | 128 groups                           | Indicates port membership of link aggregation groups and hash selection criteria.   |
| Ingress ContentAware Processor Table | 512 rules, 4 parallel lookups        | Rules for L2–L7 packet classification on ingress, ACLs, metering, statistics  |

## Address Management

The BCM53334 switch contains all of the tables required to manage station MAC addresses on the device. The address table (also referred to as the L2 table) has space for 8K entries. New entries in the table are automatically learned when packets are received on the ports. These entries can also be updated or created by the CPU. Learning is based on the source MAC address and VLAN ID. Entries that are not used for an extended period of time are automatically aged out. The device can be configured to age static entries as well.

For any valid incoming packet, the source MAC address along with the VLAN ID (either from the packet or from VLAN tables inside the device) is used to search the tables. On a successful match of (S-MAC, VLAN-ID) the device performs station move checks. If the incoming port does not match a port in the MAC table, the entry is relearned with the new incoming port value.

The destination MAC address, along with the VLAN ID, is used as a search key for the packet's output port. If a match is found, then the packet is switched out on that port. If a match is not found, then a Destination Lookup Failure (DLF) occurs, and the packet is switched out on all ports that are members of the VLAN.

---

## Class of Service

The IEEE 802.1D specification defines eight levels of priority 0–7, with priority 7 being the highest priority. This information is carried in the 3-bit priority field of the VLAN tag header. This service applies to all network ports.

The BCM53334 switch supports up to eight CoS queues per egress port. For tagged packets, the incoming packet priority can be mapped to one of the eight CoS queues, based on the priority field in the tag header or from the result of filtering mechanisms. For untagged packets, the CoS priority is derived either from a programmable field within the VLAN address tables or from the result of filtering mechanisms. After the packets are mapped into a CoS queue, they are forwarded or conditioned using either Strict Priority (SP), Deficit Round Robin (DRR), or Weighted Round Robin (WRR) schedulers.

### Strict Priority-Based Scheduling

In SP policy, any packet residing in the higher priority queues is transmitted first. Only when these queues are empty, will packets in lower priority queues be transmitted. The disadvantage of this scheme is potential starvation of packets in lower-priority queues.

### Weighted Round Robin Scheduling

In the WRR scheme, each queue is assigned a weight. The number of packets sent from each priority queue depends on the weight. Because the unit of the weight is one packet, the weight can be anywhere from 64 bytes to 1522 bytes, or 9216 bytes (when supporting jumbo frames).

**Example:** If there are four CoS queues of A, B, C, and D and the respective weights are 4, 3, 2, and 1, and if the packets are present in all the queues, the packets are sent in the sequence of A1, B1, C1, D1; A2, B2, C2; A3, B3; A4, accordingly.

### Deficit Round Robin Scheduling

The Deficit Round Robin (DRR) scheme provides relative bandwidth sharing across all active COS queues. The DRR weights are relative to each other. If minimum bandwidth is configured in this mode, then it is served first. Any excess bandwidth is then shared according to the DRR weights.

---

## Backpressure Handling

The BCM53334 switch supports mechanisms to handle backpressure, allowing for flexible flow control on packet transactions. The limit at which backpressure is detected is based on the amount of memory utilized by the packets on an input port. A backpressure message (XOFF) is sent when the lower of the two conditions (cell count limit or packet count limit) is reached. When the corresponding count goes below the high threshold and reaches the low threshold, an XON message is sent. This limit flow control is applied to the:

- IEEE 802.3x flow control. If the port is configured in full-duplex mode, IEEE 802.3x flow control is used and the MAC control PAUSE frame is sent to inhibit traffic on that port for a specified period of time.
- Enable jamming signal. If the port is configured in half-duplex mode and enabled to send a jamming signal, the jamming signal is asserted.

For ports that continue to receive packets, even after applying the above-noted flow control, the packets are discarded. Similarly, when the packets are switched out and the memory utilization falls below the limit, incoming packets are handled again. For full-duplex ports, another PAUSE frame is sent, with the time period set to 0, upon which the remote port can transmit again. For half-duplex ports, if the jamming signal was asserted, it will now be deasserted.

---

## Per Port Packet Rate (Storm) Control

The BCM53334 provides a per port packet or byte rate control mechanism to prevent the packets from flooding into other parts of the network. These programmable threshold limits apply to all ports. Several types of packets can be monitored:

- DLF/Unknown unicast packets
- Broadcast packets
- Unknown L2 Multicast packets
- Known L2 Multicast packets

The packet types are flexibly mapped to four leaky bucket mechanisms, and packets are discarded if the respective bucket becomes out of profile.

---

## Mirroring

Mirroring is a useful feature for monitoring the traffic coming in or going out on a particular port. A port can be ingress-mirrored or egress-mirrored. The mirrored-to port can be programmed as a sniffer port to monitor all traffic on the mirrored ports. When a port is ingress-mirrored, any packet received on that port is sent to a mirrored-to port, and any packet transmitted from the egress-mirrored port is also sent to the mirrored-to port.

The BCM53334 supports the following packet mirroring functions:

- Mirror frames destined for an egress-specific port (egress mirroring)
- Egress mirroring of packets sent by the CPU
- Mirror frames coming from ingress-specified port (ingress mirroring)

- Mirror frames coming from a specific ingress port sent to a specific egress port
- Mirror frames that match a certain rule in the filtering processor
- Mirror frames destined to a specific MAC address

The BCM53334 supports mirror across stack.

---

## Spanning Tree Support

The BCM53334 provides a number of features for compliance with the IEEE 802.1D and IEEE 802.1S spanning tree support specifications, as well as some optimizations for IEEE 802.1W rapid spanning tree support:

- The state bits in the spanning tree group are configured by the CPU to indicate a specific spanning tree state, and the necessary action is taken on the incoming packet. The spanning tree states supported are: disable, blocking, listening, learning, and forwarding.
- Entries marked as static in the MAC table are not aged out.
- The MAC table entry allows for detecting a hit on an address entry. If there is no hit on an entry for the spanning tree age limit duration, the address entry is deleted.
- All non-reserved addresses are self-learned.
- Reserved addresses from 0x0180c2000000 to 0x0180c2000010 and from 0x0180c2000020 to 0x0180c200002F are detectable, and these packets are forwarded to the CPU.
- Supports multiple 64 spanning trees (IEEE 802.1s). Each VLAN can be associated with one spanning tree group, which allows spanning tree-per-VLAN operation.
- Support for IEEE 802.1W Rapid Spanning Tree Protocol, with the ability to delete MAC table entries or replace the associated port information based on search criteria such as port and VLAN.

---

## IEEE 802.1D Support

The BCM53334 supports the IEEE 802.1D specification for traffic class expediting and dynamic multicast filtering support.

### Port Filtering Mode A

Forwards all addresses. In this mode, forwarding operates as bridge filtering mode 1. The port bitmap from the VLAN tables is used to determine the destination ports.

### Port Filtering Mode B

Forwards all unregistered addresses. In this mode, if the group MAC address registration entries exist in the multicast table, frames destined for the corresponding group MAC addresses are forwarded only on ports identified in the member port set, which is identified by the port bitmap. If the group MAC address does not exist in the multicast table, then Mode A filtering mechanism is used.

## Port Filtering Mode C

Filters all unregistered addresses. In this mode, frames destined for group MAC addresses are forwarded only if such forwarding is explicitly permitted by a group address entry in the multicast table. In other words, if the group MAC address exists in the multicast table, then the packets are forwarded using the port bitmap from that entry. Otherwise, the packets are dropped.

## IEEE 802.1Q Support

The BCM53334 supports the IEEE 802.1Q specification for virtual bridged local area networks by providing the following features:

- For untagged (frame without a VLAN header) or priority tagged (frame with a tag header of VLAN ID = 0) frames, the ability to assign a VLAN based on the Source MAC Address, Source IP Address, or on a protocol. If a match is not found via these tables, then a default VLAN ID can be assigned per ingress port.
- Identification of the GVRP address 0x01-80-C2-00-00-21 and forwarding these frames to the CPU.

## Link Aggregation

Link aggregation or trunking is a mechanism which bundles together up to eight ports to form a port bundle or a trunk. The port bundle is like one logical link and is useful when high bandwidth and/or redundancy between switches are required. The features include:

- Trunk ports in a bundle are always configured for full duplex.
- Trunking of network ports provides aggregate throughput up to a maximum of eight front-panel ports per trunk group.
- Provides incremental bandwidth dependent upon requirements.
- Provides link redundancy. In case of trunk port failure, the trunk group is modified and the port that failed is removed from the group.
- Provides load distribution on the trunk ports.

The BCM53334 supports 128 trunk groups, and each trunk group can have up to eight trunk ports. The trunk links are selected using a hashing function based on a combination of: MAC DA, MAC SA, VLAN, EtherType, IP DA, and IP SA. The BCM53334 supports link aggregation, with no adjacency limitation, within the same switch module and across stack.



**Note:** The Uplink ports may be included as trunk link members.

## Double-Tagging

The BCM53334 provides full support for double tagging as specified in the emerging IEEE standard, including the following features:

- The Service Provider VLAN ID (SPVID) can be inserted based on ingress port or ingress port and customer VLAN.
- The Protocol field on the SPVID is fully programmable.
- The priority bits in the SPVID can be programmed by the provider or from the customer VLAN tag in the packet.
- The ability to distinguish customer control packets (such as spanning tree BPDUs). They may be discarded or processed locally depending on configuration.

---

## Forwarding Control Block Mask

On certain ports in the switch, DLF unicast and multicast packets should be prevented from being forwarded. However, broadcast packets should always be forwarded to all ports.

To implement this feature:

1. Three separate registers, UNKNOWN\_UCAST\_BLOCK\_MASK, UNKNOWN\_MCAST\_BLOCK\_MASK, and BCAST\_BLOCK\_MASK are bitmasks for unknown unicast, unknown multicast, and unknown broadcast packets.
  - a. The bits not set in these bitmasks define a set of egress ports to which unknown unicast, multicast, and broadcast frames should be forwarded.
  - b. To block broadcast packets to a specific port, the appropriate bit is set in the BCAST\_BLOCK\_MASK.
  - c. To forward broadcast packets to all ports of the VLAN, set all the bits in BCAST\_BLOCK\_MASK to 0.
2. Ingress logic will pick up the port bitmap from the VLAN tables, using the VLAN ID assigned to the packet, for unknown unicast, unknown multicast, and broadcast packets.
  - a. For unknown unicast packets, the port bitmap is ANDed with the UNKNOWN\_UCAST\_BLOCK\_MASK bitmask.
  - b. For unknown multicast packets, the port bitmap is ANDed with the UNKNOWN\_MCAST\_BLOCK\_MASK bitmask.
  - c. For broadcast packets, the port bitmap is ANDed with the BCAST\_BLOCK\_MASK bitmask.

---

## ContentAware Processing

ContentAware processing is described in the following sections:

### Ingress Filter Processor (IFP)

For packets ingressing on the GbE ports. Ingress lookups occur on L2 and L3 pre-routed packets. The IFP is a flexible and powerful ContentAware Filter Processor. Filtering can be done by parsing the first 128 bytes of the packet using either predefined protocol fields such as VLAN, L2, and L3 addresses or using User Defined fields. Assigning a new priority, route, drop, or redirecting the packet are some of the actions that can be performed.

**Table 4: ContentAware Field Processor Sizes**

|     | <b>Slices</b> | <b>Rules per Slice</b> | <b>Total # of Rules</b> | <b>Meters</b> | <b>Counters</b> | <b>Bits per Rule (Single Wide)</b> |
|-----|---------------|------------------------|-------------------------|---------------|-----------------|------------------------------------|
| IFP | 4             | –                      | 512                     | 512           | 512             | –                                  |

## Network Management Support

The BCM53334 provides a set of counters to support the following Management Information Base (MIB) specifications:

- RMON statistics group (IETF RFC2819)
- SNMP interface group (IETF RFC1213 and 2863)
- Ethernet-like MIB (IETF RFC1643)
- Ethernet MIB (IEEE 802.3u)
- Bridge MIB (IETF RFC1493)

## Energy Efficient Ethernet

The BCM53334 device support Energy Efficient Ethernet (EEE) to reduce power consumption by enabling the internal PHYs to enter a Low Power Idle (LPI) state, during extended idle periods that may exist between packets. The power savings aspects of EEE are largely implemented in the PHYs. However, the PHYs are reliant upon the MACs to inform them of when to enter and leave the LPI state. The MACs make these determinations by examining the state of the transmit queues associated with each MAC. The EEE signaling between a MAC and its PHY is conveyed by the SGMII signals between them. The EEE feature is only supported on 1GbE ports, not supported on the TSC uplink/stacking ports.

When the transmit MAC asserts its LPI signal to the PHY, the PHY transmits a sleep symbols on the wire for a short period. This informs the link partner's receive PHY that it is entering the LPI state. After the sleep symbols have been transmitted, a quiet period is entered where there is no signaling. At the beginning of the first quiet period, the receive PHY indicates to its MAC that it has entered the LPI mode. The transmit PHY interrupts the quiet period periodically to send refresh symbols that are used to keep PLLs, filters, and other functions in sync, so that the LPI state can be exited quickly. When the transmit MAC deasserts, the PHY wakes up and transmits wake symbols for a short period to the link partner's PHY, informing it that it is time to wake up. The time between the transmit MAC deasserting and its resumption of packet transmission may be adjusted upward from the minimum PHY wake up time to allow for other system components to wake up and be ready for packet reception. Therefore, an idle period may precede the appearance of the first packet after a LPI sequence.

In general, EEE operates in an asymmetric mode. Meaning, the transmit direction and receive direction may enter and exit the LPI state independently. For 1000BASE-T, however, symmetric operation is required in order to truly benefit from EEE. In symmetric mode, both the transmit and receive paths must be indicating with sleep symbols before either side will enter the quiet state. Therefore, the transmit half of a PHY will send sleep signals until either sleep symbols are received from the link partner or the PHY has been commanded to exit the LPI state by the MAC.



## Section 4: Ethernet Switch Controller System Interfaces

### Overview

The BCM53334 includes the following physical layer interfaces:

- GbE (QSGMII): Allows connection to 10/100/1000BASE-T physical layer devices
- MIIM (IEEE 802.3u): Communication with physical layer devices
- JTAG: For IEEE Std. 1149.6 boundary scan
- BSC: For low-speed configuration (as a slave) and low-speed communications (as a CPU-controlled master/slave)
- LED: For system LED support

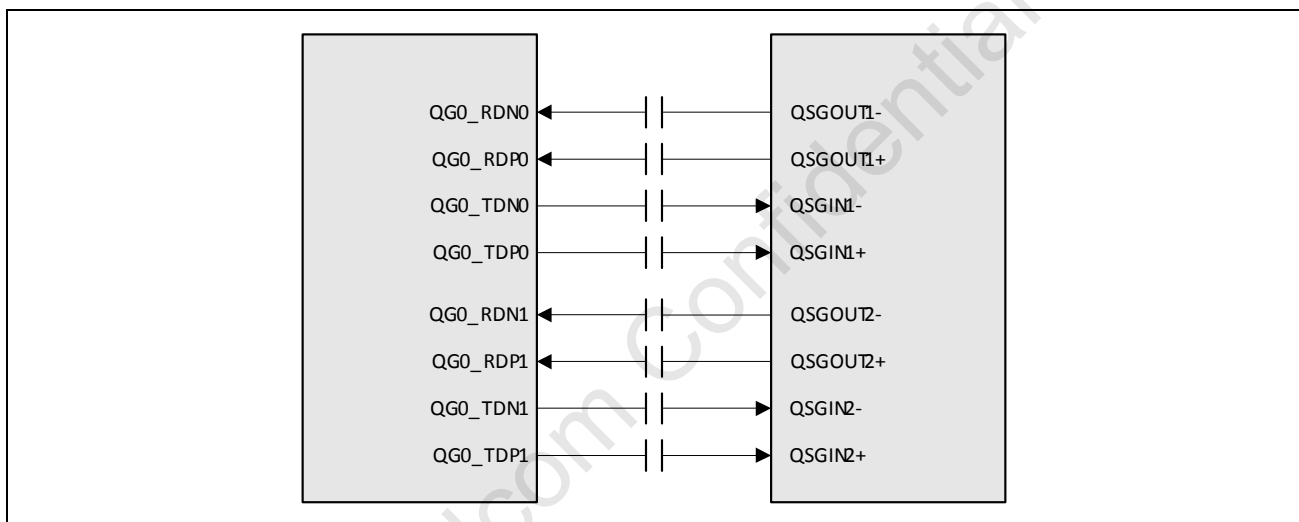
**Table 5: System Interfaces**

| <b>Interface</b>                  | <b>Description</b>  |
|-----------------------------------|---|
| GbE (SerDes) port                 | <ul style="list-style-type: none"> <li>• Up to 16 GbE ports, full-duplex mode of operation, compliant to IEEE 802.3</li> <li>• Support for 10/100/1000 Mbps using auto-negotiation</li> <li>• Supports 2 QSGMII interfaces</li> <li>• Support for jumbo frames up to 9216 bytes</li> </ul>  |
| Serial LED                        | <ul style="list-style-type: none"> <li>• Control of up to 255 system LEDs at a 30 Hz refresh rate</li> <li>• Simple microcontroller with instructions optimized for LED control</li> <li>• Low-cost two-wire interface to system LEDs</li> <li>• 256 bytes of program RAM</li> <li>• 256 bytes of data RAM</li> <li>• Direct access to per port speed, duplex state, flow control state, link state, transmit and receive activity, and collision activity</li> </ul> |
| Parallel LED                      | <ul style="list-style-type: none"> <li>• 16 embedded ports</li> <li>• 3 parallel drivers</li> </ul>   |
| MIIM (MDC/MDIO)                   | <ul style="list-style-type: none"> <li>• IEEE 802.3u-compliant MIIM interface for communication with external PHY devices</li> <li>• 2.5 MHz operation</li> <li>• IEEE 802.3 Clause 22-compliant</li> </ul>   |
| Broadcom Serial Control (BSC) bus | <ul style="list-style-type: none"> <li>• BSC-compliant interface—The Broadcom serial control (BSC) bus is Philips® I<sup>2</sup>C-compatible.</li> <li>• Supports slave mode, allowing an external microcontroller to configure the BCM53334 device</li> <li>• CPU-controlled master mode to communicate with other BSC devices</li> </ul>  |
| JTAG                              | <ul style="list-style-type: none"> <li>• JTAG-compliant interface used to support boundary scan operations</li> <li>• 20 MHz operation</li> </ul>   |

## 1GbE (QSGMII)

The BCM53334 provides up to 2 QSGMII links, each operating at 5.0 Gbps on two pairs of differential signals (1 TX pair and 1 RX pair). The QSGMII is a CML interface and connects to external QSGMII PHYs such as Broadcom's BCM54282. Each QSGMII link is an equivalent of four 1.25 Gbps SGMII links, conveying four ports of network data with significantly less number of signal pins compared to GMII or SGMII. With four GbE links multiplexed onto one QSGMII link, the data from port 0 will display first, followed by data from port 1, port 2, and port 3. This will then be followed by the next piece of data from port 0 and the rest of the ports following the same sequence. Since the data is 8b/10b encoded before being sent out the QSGMII link, the raw data throughput is 4 Gbps. The QSGMII operates in both half and full duplex and at all port speeds. The QSGMII link replicates the data 100 times and 10 times, respectively, when operating at 10 Mbps or 100 Mbps.

**Figure 7: BCM53334 QSGMII Interface**



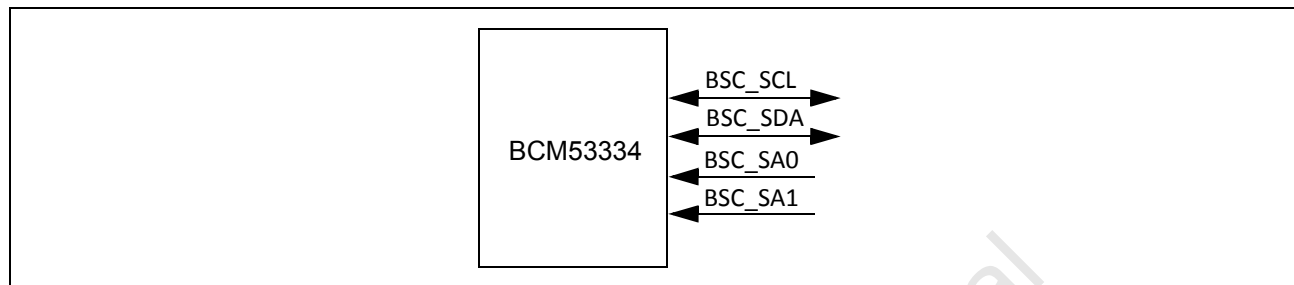
## MII Management

The CPU Management Interface Controller (CMIC) supports an IEEE 802.3u standard MII Management (MIIM) interface. This is a two-wire serial bus controlled by the CMIC. It allows register access to all system PHYs. PHY data can be read/written to using this interface. The two signals for MIIM are IP\_MDC (clock) and IP\_MDIO (bidirectional data). The CPU programs the PHY registers using this interface. After the initialization sequence, the CPU could read the link up/down register bit to detect any link changes. Alternatively, the CPU can enable the MIIM\_AUTO\_LINK\_SCAN\_EN bit. In this mode, CMIC will scan the PHYs and detect link status for each port. The link status register is updated at the end of each scan. If a link status change is detected, CMIC sends a notification to the CPU.

## Broadcom Serial Interface (BSC)

The BCM53334 switch provides an BSC interface to communicate with other devices that support a similar interface. The signals supported are shown in [Figure 8](#).

**Figure 8: BSC Interface**



The BSC interface can be configured to operate in either master or slave mode. The supported BSC data protocol format is big endian, which is consistent with the BSC protocol supported by other vendors.

Upon reset, the BCM53334 switch enters the default slave mode, provided BSC\_MODE strap is pulled high. In this mode, an external BSC master device can communicate with the BCM53334 switch and initialize the device using the BSC\_SDA and BSC\_SCL lines. The external master can write the 16-bit address of the register to be accessed, followed by the 32-bit data to be written. When all 32 bits (4 bytes) of data are provided, a write to the internal register is performed.



**Note:** There is no mechanism to support any interrupt structure or bus mastering in the BSC slave-only mode.

A default BSC slave address of 0b1000100 is used for the slave-only mode. Additionally, the BSC\_SA0 and BSC\_SA1 inputs can be strapped high or low, to change the default slave address, giving a range of 0b1000100 to 0b1000111. Both 7-bit and 10-bit addressing schemes are supported.

Optionally, CPU-controlled master/slave mode is supported. This mode is disabled by default and is useful to connect other BSC devices, such as a time-of-day chip, temperature sensors, parallel ports, and so forth, to the BCM53334 switch. In master mode, read and write BSC operations are initiated under program control of the host CPU. A block of registers accessible by the CPU controls this function.

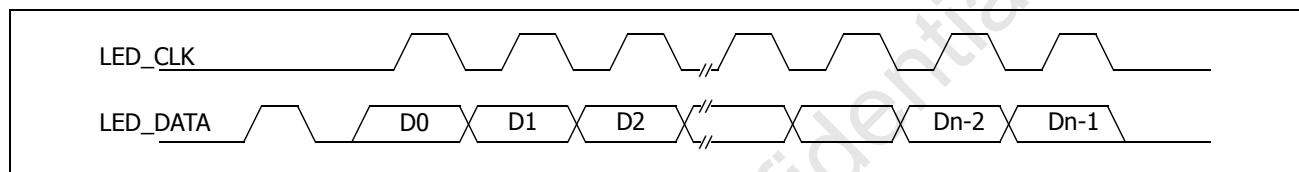
## LED Interfaces

### Serial LED Mode

A LED microprocessor controls the serial LED signals (clock and data). Both LED\_CLK and LED\_DATA are outputs. It can provide the port status for all GE and TSC ports. This requires programming some assembly code routines to run on the LED microprocessor. Please refer to the SDK and PRG for more details.

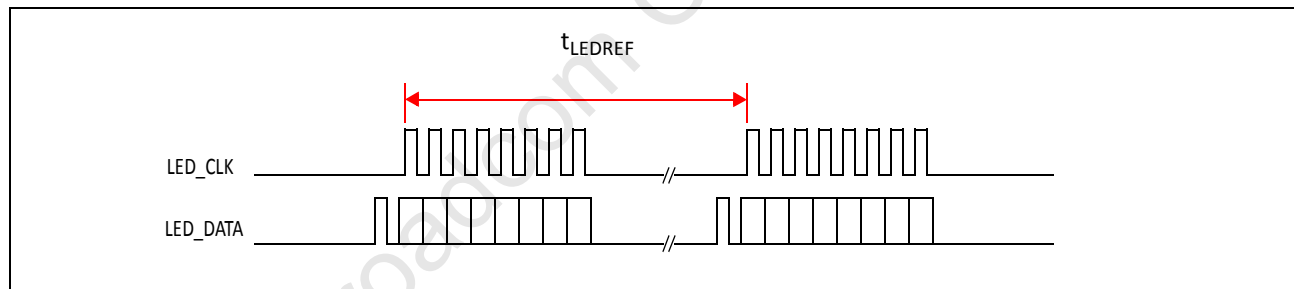
When active, LED\_CLK is a 5 MHz clock. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED\_DATA bits. The LED\_DATA signal is pulsed high at the start of each LED refresh cycle (see Figure 9). The LED refresh cycle is repeated every 30 ms to refresh the LEDs.

**Figure 9: Single LED Refresh Cycle**



The LED refresh cycle is repeated periodically (every 30 ms) to refresh the LEDs (see Figure 10).

**Figure 10: LED Refresh Cycle**



### PHY-Driven Parallel LED Mode

In addition to the serial LED interface which provides status for all 24 ports, a 48-output parallel LED interface is available for the 16 integrated PHYs. Parallel LED interface for the other 8 ports comes from the external QSGMII-based PHYs.



**Note:** Several LED pins behave as strap pins during reset and some LED pins are shared with the GPIO interfaces. When GPIO interface is enabled then the LED function is disabled. Refer to [Section 7: “Pin List Description,” on page 52](#) for more details.

The BCM53334 has three programmable LED balls per port that perform different functions. Each of the BCM53334 LEDs can be individually programmed to many available modes on a per port basis.

## Serial to Parallel LED Mode

When the LED microprocessor is enabled, the parallel LED interface is also controlled by the LED microprocessor. It inputs the serial LED signals to the internal shift register circuit and outputs the LED signals on the parallel LED interface. In this mode, the LED signals come from the port status. It can support all GE and TSC ports, same as in serial LED mode. The LED signal count per port is controlled by the LED microprocessor code. It is not limited to three signals per port as in PHY-driven parallel LED mode. Since there are 48 pins in the parallel LED interface, it can output up to 48 LED signals.

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## Section 5: Gigabit Ethernet Transceiver

### Copper Interface

The BCM53334 can communicate with Link Partners that support 10BASE-T, 100BASE-TX or 1000BASE-T. The BCM53334 supports auto-negotiation for 10BASE-T, 100BASE-TX or 1000BASE-T. The BCM53334 supports force mode for 10BASE-T and 100BASE-TX. Force mode is not supported for 1000BASE-T operation.

The following sections describe the internal circuitry and additional features of the copper interface.

### Encoder

In 10BASE-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs pre-equalization for 100m of Category 3 cabling.

In 100BASE-TX mode, the BCM53334 transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first 2 nibbles of preamble with a start-of-stream delimiter (/J/K codes) and appending an end-of-stream delimiter (/T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in [“Stream Cipher” on page 41](#). The scrambled data is then encoded into MLT-3 signal levels.

In 1000BASE-T mode, the BCM53334 simultaneously transmits and receives a continuous data stream on all four pairs of the Category 5 cable. Byte-wide data from the transmit data signals are scrambled when the transmit enable is asserted, and the trellis (a PAM5 symbol on each of the four twisted-pairs) is encoded into a four-dimensional code group and then inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first 2-bytes of the preamble with a start-of-stream delimiter, and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier extend code groups between packets. Carrier extension is used by the switch to separate packets within a multiple-packet burst, and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data signals while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The encoding complies with IEEE 802.3ab and is fully compatible with previous versions of the Broadcom 1000BASE-T PHYs.

### Decoder

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT-3 to serial non-return to zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with zeros. The decoded data is driven onto the MII receive data outputs. When an invalid code group is detected in the data stream, the BCM53334 asserts the MII receive error (RX\_ER) signal. RX\_ER is also asserted when the link fails or when the descrambler loses lock during packet reception.

In 1000BASE-T mode, the receive data stream is:

- Passed through the Viterbi decoder
- Descrambled
- Translated back into byte-wide data

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 0x00. Carrier extend codes are replaced with 0x0F or 0x1F. The decoded data is driven onto the QSGMII receive data outputs. Decoding complies with IEEE 802.3ab and is fully compatible with previous versions of Broadcom 1000BASE-T PHYs.

## Link Monitor

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the following pairs for the presence of valid link pulses.

- TDP\_[73:0]\_[0]/TDN\_[73:0]\_[0]
- TDP\_[73:0]\_[1]/TDN\_[73:0]\_[1]

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the Link Fail state, and the transmission and reception of data packets are disabled. When a valid signal is detected on the receive pair for a minimum of 1 ms, the link monitor enters the Link Pass state, and the transmit and receive functions are enabled.

Following auto-negotiation in 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver's timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been good for at least 1  $\mu$ s, the link monitor enters the Link Pass state, and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 ms, the link monitor enters the Link Fail state, and the transmission and reception of data packets are then disabled.

## Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The BCM53334 achieves an optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than  $1 \times 10^{-12}$  for transmissions of: up to 100 meters on Category 5 twisted-pair cabling for 1000BASE-T and 100BASE-TX mode; up to 100 meters on Category 3 UTP cable for 10BASE-T mode. The all-digital nature of the design makes the BCM53334 very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

## Echo Canceler

Because of the bidirectional nature of the channel in 1000BASE-T, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

## Crosstalk Canceler

The BCM53334 transmits and receives a continuous data stream on four channels in gigabit mode. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. It is possible to cancel the effect because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

## Analog-to-Digital Converter

Each receive channel has its own 125 MHz analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High-power supply noise rejection
- Fast settling time
- Low bit error rate

## Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T, 100BASE-TX, and 10BASE-T operation.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the reference clock input, and the receive clock is locked to the incoming data stream.



In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to the reference clock input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

## Baseline Wander Correction

1000BASE-T and 100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM53334 automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides a perfect DC balance.

## Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT-3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses a voltage drive output that is well-balanced, and therefore, produces very low-noise transmit signals.

## Stream Cipher

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require that there be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive ORing the encoded serial data stream. This is done with the output of an 11-bit wide linear feedback shift register (LFSR), producing a 2047-bit non-repeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive ORing the input data byte with an 8-bit wide cipher text word. The cipher text word generates each symbol period from 8 uncorrelated maximal length data sequences that are produced by linear remapping of the output of a 33-bit wide LFSR. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bit wide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The BCM53334 enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that inter-packet gaps containing idles or frame extensions are received at expected intervals. When the BCM53334 detects loss of synchronization, it notifies the link partner of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the BCM53334 is forced into the Link Fail state.

In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

## Wire Map and Pair Skew Correction

During 1000BASE-T operation, the BCM53334 has the ability to automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for (internal to the BCM53334) the following errors:

- Wiring errors caused by the swapping of pairs within the UTP cable
- Polarity errors caused by the swapping of wires within a pair

The BCM53334 also automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the wire pairs. The BCM53334 can tolerate delay skews of up to 64 ns long. Auto-negotiation must be enabled to take advantage of the wire map correction.

During 10/100Mb/s operation, pair swaps are corrected. Delay skew is not an issue though, because only one pair of wires is used in each direction.

## Automatic MDI Crossover

During copper auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM53334 can perform an automatic media dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the BCM53334 normally transmits on TDP\_[73:0]\_0/TDN\_[73:0]\_0 and receives on TDP\_[73:0]\_1/TDN\_[73:0]\_1.

When connecting to another device that does not perform MDI crossover, the BCM53334 automatically switches its TDP\_[73:0]\_0/TDN\_[73:0]\_0 and TDP\_[73:0]\_1/TDN\_[73:0]\_1 pairs when necessary to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The MDI Crossover State can be determined by reading RDB\_Register, offset 0x001, bit[13].

- 1'b0 = Normal MDI mode
- 1'b1 = Crossover MDI mode

## 1000BASE-T Operation

During 1000BASE-T operation, the BCM53334 swaps the transmit symbols on pairs 0 and 1 and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. The automatic MDI crossover function can not be disabled when in 1000BASE-T mode.

## 10/100BASE-TX Operation (Auto-Negotiation Enabled)

During 10BASE-T and 100BASE-TX operation, pair swaps automatically occur within the device and do not require user intervention. The automatic MDI crossover function by default only works when auto-negotiation is enabled. This function can be disabled during auto-negotiation by writing to RDB\_Register, offset 0x000, bit[14] = 1'b1.

## 10/100BASE-TX Operation (Forced Mode)

The automatic MDI crossover function can also be enabled when in forced 10BASE-T or forced 100BASE-TX mode. This feature allows the user to disable the copper auto-negotiation in either 10BASE-T or 100BASE-TX and still take advantage of the automatic MDI crossover function. This feature is enabled by writing RDB\_Register, offset 0x02F, bit[9] = 1'b1.

When in forced 10BASE-T or 100BASE-TX mode, the BCM53334 has a feature that can manually swap the MDI state when the automatic MDI crossover function is disabled. Normally the BCM53334 transmits on TDP\_[73:0]\_[0]/TDN\_[73:0]\_[0] and receives on TDP\_[73:0]\_[1]/TDN\_[73:0]\_[1]. To change the MDI state to transmit on TDP\_[73:0]\_[1]/TDN\_[73:0]\_[1] and receive on TDP\_[73:0]\_[0]/TDN\_[73:0]\_[0] the following steps must be done.

- Put PHY in non-link condition.
- Enable Manual Swap MDI (Write RDB\_Register, offset 0x00E, bit[7] = 1'b1).
- Set PHY into Force 10BASE-T or 100BASE-TX mode.



**Note:** To change the MDI state when in forced 100BASE-TX mode, the PHY must first be put into a non-link condition.

## Full-Duplex Mode

The BCM53334 supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable. When auto-negotiation is disabled, full-duplex operation can be enabled by setting Register 0x00, bit[8] = 1'b1.

When auto-negotiation is enabled, full-duplex capability is advertised for:

- 10BASE-T: Register 0x04, bit[6] = 1'b1.
- 100BASE-TX: Register 0x04, bit[8] = 1'b1.
- 1000BASE-T: Register 0x09, bit[9] = 1'b1.

## Master/Slave Configuration

In 1000BASE-T mode, the BCM53334 and its link partner perform loop timing. One end of the link must be configured as the timing master and the other end as the slave. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port the slave. Each end generates an 11-bit random seed if the two settings are equal; the end with the higher seed is configured as the master. If the local PHY and the link partner generate the same random seed, then auto-negotiation is restarted.

If both ends of the link attempt to force the same manual configuration (both master or both slave), or the random seeds match seven consecutive times, then the BCM53334 sets the Master/Slave Configuration Fault bit in the 1000BASE-T Status register and auto-negotiation is restarted.

For setting the BCM53334 to manual master/slave configuration or to set the advertised repeater/DTE configuration, see 1000BASE-T Control Register (Address 0x09).

## Next Page Exchange

The 1000BASE-T configuration requires the exchange of three auto-negotiation next pages between the BCM53334 and its link partner. Exchange of 1000BASE-T Next Page information takes place automatically when the BCM53334 is configured to advertise 1000BASE-T capability.

The BCM53334 also supports software-controlled Next Page exchanges. When Register 0x04, bit[15] = 1'b1, all Next Page transactions are controlled through the MII management interface. This includes the three 1000BASE-T Next Pages, which are always sent first. The BCM53334 automatically generates the appropriate message code field for the 1000BASE-T pages. When the BCM53334 is not configured to advertise 1000BASE-T capability, the 1000BASE-T Next Pages are not sent.

When the BCM53334 is not configured to advertise 1000BASE-T capability and Register 0x04, bit[15] = 1'b0, the BCM53334 does not advertise Next Page ability.

## Auto-Negotiation

The BCM53334, when configured to Copper mode, negotiates its mode of operation over the copper media using the auto-negotiation mechanism, defined in the IEEE 802.3u and 802.3ab specifications. When the auto-negotiation function is enabled, the BCM53334 automatically chooses the mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM53334 can be configured to advertise the following modes:

- 1000BASE-T full-duplex and/or half-duplex.
- 100BASE-TX full-duplex and/or half-duplex.
- 10BASE-T full-duplex and/or half-duplex.

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD). Auto-negotiation can be enabled or disabled by hardware and software control, but is always required for 1000BASE-T operation.

## Ethernet@Wirespeed

Ethernet@Wirespeed™ is an enhancement to auto-negotiation that allows a network connection over impaired cable plants. If a link can not be established at the highest common denominator within a set number of link attempts then the BCM53334 advertises the next highest advertised speed using auto-negotiation. The set number of failed link attempts is programmable. See [“Changing the Number of Failed Link Attempts” on page 46](#) for more details.

The BCM53334 has a link-up timer that times how long the link has been up. If the link stays up for less than 3 seconds then the Link-Fail Counter will get incremented. If the link stays up for greater than 5 seconds then the Link-Fail Counter is reset to zero.

The purpose of the link-up timer is to prevent scenarios where an unstable link (link is going up and down quickly) causes the BCM53334 to continuously try to link at a given speed and not try to downgrade and link to a lower speed. In this situation, if the link is up for less than 3 seconds, the Link-Fail Counter will get incremented. Once the Link-Fail Counter exceeds the programmable failed link attempts the BCM53334 will start advertising the next lowest speed and try to establish a link.

The link-up timer can be bypassed by setting RDB\_Register, offset 0x02F, bit[10] = 1'b1. Setting this bit causes the number of failed link attempts to get reset to zero after every link up condition, no matter how short the link-up time is.

## Ethernet@Wirespeed Example

At start-up the BCM53334 is advertising 1000BASE-T, 100BASE-TX, and 10BASE-T capabilities per Register 0x04 and Register 0x09 and the Link Partner is also advertising the same capabilities:

- If a link cannot be established within a programmable number of link attempts (two to nine) with 1000BASE-T being advertised then an Ethernet@Wirespeed downgrade occurs, the 1000BASE-T capability is masked out on the BCM53334 and the next highest advertised capability (100BASE-TX) is advertised.
- If a link cannot be established within a programmable number of link attempts (two to nine) with 100BASE-TX being advertised then an Ethernet@Wirespeed downgrade occurs, the 100BASE-TX is masked out on the BCM53334 and the next highest advertised capability (10BASE-T) is advertised.
- If a link can not be established within a programmable number of link attempts (two to nine) with 10BASE-T being advertised then an Ethernet@Wirespeed downgrade occurs and all advertising capabilities are enabled (1000BASE-T, 100BASE-TX, and 10BASE-T) on the BCM53334 and the whole process begins again.

## Enabling/Disabling Ethernet@Wirespeed

Enabling or disabling Ethernet@Wirespeed is done on a per-port basis.

- Enable: Write RDB\_Register, offset 0x02F, bit[4] = 1'b1.
- Disable: Write RDB\_Register, offset 0x02F, bit[4] = 1'b0.

## Removing Ethernet@Wirespeed Downgrade

Ethernet@Wirespeed downgrade can be removed by any of the following events:

- Stable link-up condition for greater than 5 seconds.
- Unplug cable (no energy) for 6 seconds.
- Hardware reset.
- Software reset (Write Register 0x00, bit[15] = 1'b1).
- Disable auto-negotiation (Write Register 0x00, bit[12] = 1'b0).
- Restart auto-negotiation (Write Register 0x00, bit[9] = 1'b1).
- Disabling Wirespeed (Write RDB\_Register, offset 0x02F, bit[4] = 1'b0).
- Auto-negotiation resolves to no HCD (Highest Common Denominator).

## Changing the Number of Failed Link Attempts

The number of failed link attempts before downgrading to a slower speed is programmable. The number can be programmed anywhere from two to nine failed link attempts before downgrading to a lower speed. The default value is five failed link attempts. The number of failed link attempts before downgrading to a lower speed can be programmed by writing to RDB\_Register, offset 0x014, bits[4:2] as shown [Table 6](#).

**Table 6: Changing the Number of Failed Link Attempts before Downgrade**

| <b>Bits[4:2]</b> | <b>Description</b>   |
|------------------|--|
| 0x0              | Number of failed link attempts before Ethernet@Wirespeed downgrade = 2                 |
| 0x1              | Number of failed link attempts before Ethernet@Wirespeed downgrade = 3                 |
| 0x2              | Number of failed link attempts before Ethernet@Wirespeed downgrade = 4                 |
| 0x3              | Number of failed link attempts before Ethernet@Wirespeed downgrade = 5 (Default Value) |
| 0x4              | Number of failed link attempts before Ethernet@Wirespeed downgrade = 6                 |
| 0x5              | Number of failed link attempts before Ethernet@Wirespeed downgrade = 7                 |
| 0x6              | Number of failed link attempts before Ethernet@Wirespeed downgrade = 8                 |
| 0x7              | Number of failed link attempts before Ethernet@Wirespeed downgrade = 9                 |

## Monitoring Ethernet@Wirespeed

The status of the Ethernet@ Wirespeed downgrade can be monitored through the following registers and LEDs.

- Ethernet@Wirespeed Downgrade Status (Read RDB\_Register, offset 0x001, bit[14]).
- Ethernet@Wirespeed Downgrade (Read RDB\_Register, offset 0x00C, bit[12]).
- Ethernet@Wirespeed Disable Gigabit Advertising (Read RDB\_Register, offset 0x00C, bit[14]).
- Ethernet@Wirespeed Disable 100BASE-TX Advertising (Read RDB\_Register, offset 0x00C, bit[13]).
- HCD Status (Read RDB\_Register, offset 0x00C, bits[11:0]).
- Auto-negotiation HCD and Current Status (Read RDB\_Register, offset 0x009, bits[10:8]).
- Ethernet@Wirespeed downgrade LED on LED[0] (Write RDB\_Register, offset 0x01D, bits[3:0] = 0x9).
- Ethernet@Wirespeed downgrade LED on LED[1] (Write RDB\_Register, offset 0x01D, bits[7:4] = 0x9).



## Super Isolate Mode

When in Super Isolate mode the following happens:

- The BCM53334's transmitter and receiver on the Copper Media Dependent Interface are disabled. The link partner will go into a link down state since it is not receiving any FLPs, NLPs, or 100BASE-TX idles.

## Software Enable/Disable

The BCM53334 can be put into Super Isolate mode on a per port basis by software.

- To enable Super Isolate mode:  
Write RDB\_Register, offset 0x02A, bit[5] = 1'b1 for each of the 84 ports.
- To disable Super Isolate mode:  
Write RDB\_Register, offset 0x02A, bit[5] = 1'b0 for each of the 84 ports.

## Standby Power-Down Mode

The BCM53334 can be placed into standby Power-down mode using software commands. In this mode, all PHY functions, except for the serial management interface, are disabled. To enter standby Power-down mode, write Register 0x00, bit[11] = 1'b1. There are three ways to exit standby Power-down mode:

- Write Register 0x00, bit[11] = 1'b0 (Clear MII Control register)
- Write Register 0x00, bit[15] = 1'b1 (Software reset)
- Assert the hardware  $\overline{\text{RESET}}$

Reads or writes to any MII register, other than Register 0x00 while the device is in the standby Power-down mode, returns unpredictable results. Upon exiting standby Standby Power-down mode, the BCM53334 remains in an internal reset state for 40  $\mu$ s, and then resumes normal operation.

## Auto Power-Down (APD) Mode

When the BCM53334 is placed into Auto Power-Down (APD) mode the chip power is reduced when the signal from the copper link partner is not present. APD mode works whether the device is in auto-negotiation enabled or in forced mode. When APD mode is enabled, the BCM53334 automatically enters the low-power mode when energy on the line is lost, and it resumes normal operation when energy is detected. When the BCM53334 is in APD mode, the copper transmitter is disabled (Sleep Cycle) for 2.7 seconds or 5.4 seconds depending on the SLEEP\_TIMER\_SEL bit after which the transmitter is enabled (Wake Cycle) for a duration of 84 ms to 1260 ms depending on the settings on the WAKE\_UP\_TIMER\_SEL bits. The BCM53334 enters normal operation and establishes a link if energy is detected, otherwise, the Sleep and Wake-up cycles repeat.

## ADP Mode Enable (Auto-Negotiation Enabled)

- Write RDB\_Register, offset 0x01A, bits[6:5] = 2'b01.
- Write RDB\_Register, offset 0x1A, bit[8] = 1'b1.

ADP Mode Enable (Auto-Negotiation Disabled)

- Write RDB\_Register, offset 0x01A, bits[6:5] = 2'b11.

- Write RDB\_Register, offset 0x1A, bit[8] = 1'b'1.

ADP Mode Disable

Write RDB\_Register, offset 0x01A, bits[6:5] = 2'b00.

## Sleep Cycle Settings

Write RDB\_Register, offset 0x01A, bit[4]

- 1'b0 = Disable copper transmitter for 2.7 seconds.
- 1'b0 = Disable copper transmitter for 5.4 seconds.

## Wake Cycle Settings

Write Register RDB\_Register, offset 0x01A, bits[3:0]

- 0x1 = Enable copper transmitter for 84 ms.
- 0x2 = Enable copper transmitter for 168 ms.
- 0x3 = Enable copper transmitter for 252 ms.
- 0xF = Enable copper transmitter for 1.26 seconds.



## Section 6: ARM Cortex-A9 Processor Subsystem Functional Description

### Cortex-A9

The Cortex-A9 processor has an integrated  $32 \times 32$ -bit single-cycle multiply/accumulate block running at CPU core speed, providing additional signal or media processing capabilities. The integrated MMU with a 128-entry TLB block allows support for common multi-threaded real-time operating systems (RTOS), such as the standard Linux<sup>®</sup> distribution.

### NOR Serial Flash Interface

The BCM53334 has a NOR Serial Flash interface and supports Execute in Place (XIP) as a boot source configured by the strapped option.

**Table 7: Serial Flash Interface**

| Feature                               | Value            | Comment  |
|---------------------------------------|------------------|--|
| Interface width                       | 1, 2, 4          | Supports single, dual, and quad SPI interfaces.  |
| In place execute (boot support) XIP   | Yes              | –  |
| Maximum number of physical devices    | 1                | –  |
| Extended addressing support (4B mode) | Yes              | Used to address greater than 16 MB.  |
| Devices size support                  | 128 Mb - 4 Gb    | Cannot boot from devices that support 32b addressing only. Devices that support either 24b only or mixed 24/32b addressing are supported as a boot device. |
| Block size                            | 32 KB, 64 KB     | –  |
| Page sizes                            | 2 KB, 4 KB, 8 KB | –  |
| Maximum frequency                     | 62.5 MHz         | –  |
| NOR Flash support                     | Yes              | Some Serial Flash in the managed NAND Flash that appears as a NOR.   |

### MIIM/UART/GPIO Interfaces

The BCM53334 supports:

- One MDC/MDIO interface.
- One UART1 interface with CTS and RTS signals.
- Eight 3.3V GPIO pins that can be used to connect to various external devices.

# SPI interface

SPI is a serial interface that is compatible with a subset of the Motorola Synchronous Serial Peripheral Interconnect (SPI) bus. The SPI interface can be configured to operate in either master or slave mode. The SPI interface consists of a set of four signals:

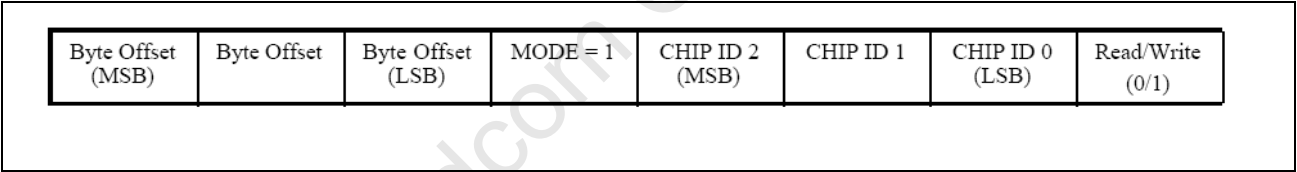
- Serial clock (SCK)
- Slave select (SS\_L)
- Master-in/slave-out (MISO)
- Master-out/slave-in (MISI)

When the SPI interface operates as an SPI slave device, in that it never initiates a transfer and allows external master to read and write to various internal register spaces and memory tables of the chip. During a transaction, data is captured on the rising edge of SCK and propagated at the falling edge of SCK. This corresponds to the modes 0 (SPO = 0 and SPH = 0) and 3 (SPO = 1 and SPH = 1) of the Motorola SPI format.

A layer of protocol is added to the basic SPI definition to facilitate data transfers from the chip. This protocol establishes the definition of the first two bytes issued by the external master to the SPI slave during a transfer. The first byte issued from the master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional address bytes and data bytes.

The SPI interface supports the fast SPI access mechanisms, determined by the content of the command byte. Figure 11 shows the fast SPI command byte.

Figure 11: Fast SPI Command Byte



In a fast command byte, the Mode bit (bit [4]) of the command byte is a 1. Bits [7:5] indicate the byte offset into the register that the access starts from and bits [3:0] indicate the Chip ID to be accessed. Bit 0 of the command byte is the Read/Write signal (0= Read, 1= Write) that determines the data direction for the transaction.

The 4 bytes following the command byte are register address bytes. The register address is 32 bits wide. The lower byte of the address is transmitted first, followed by the higher bytes.

In case of a write command, 4 data bytes follow the write address. As in the case of address, the lower byte is transmitted first. A write transaction is initiated once all the address and data bytes are received.

All write operations are of the form:

```
<CMD, CHIP_ID, W><REG ADDR0> <REG ADDR1><REG ADDR2><REG ADDR3><DATA0><DATA1><DATA2><DATA3>
```

In case of a read command, a read transaction is initiated once all the address bytes are received. The data received back from the chip is transmitted as the read response to the master.

All read operations are of the form:

<CMD, CHIP\_ID, R><REG ADDR0><REG ADDR1>><REG ADDR2><REG ADDR3>

SPI slave runs in Fast SPI mode. In Fast SPI mode, the SPI slave returns the ACK bit before transmitting the read data. The ACK bit is transferred as the LSB of each byte. Till the time the read access is on progress, SPI will return 0x00 on the MISO line. Once read data is available, SPI returns 0x01 followed by 4 bytes of read data.

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## Section 7: Pin List Description

### Signal Name Descriptions



**Note:** This is a preliminary pin assignment and is subject to change.

The section describes the BCM53334 hardware signals. The following conventions are used:

- I = Input signal
- O = Output signal
- B = Bidirectional signal
- BOD = Open-drain bidirectional signal
- BPU = Bidirectional signal with internal pull-up
- IPD = Input signal with internal pull-down
- IPU = Input signal with internal pull-up
- OOD = Open-drain output
- P = Power

**Table 8: BCM53334 Hardware Signals**

| Pin Names          | Quantity | I/O             | V    | Pin Description  |
|--------------------|----------|-----------------|------|--|
| <b>GPIO</b>        |          |                 |      |  |
| GPIO[7:0]          | 8        | I/O             | 3.3V | General-purpose I/O<br><b>Note:</b> GPIO[3:0] can be reset by resetting SYS_RST_L. GPIO[7:4] are reset only on power-on and cannot be reset by just doing the software chip reset alone. |
| <b>UART Port 1</b> |          |                 |      |  |
| UART1_RX           | 1        | I <sub>PD</sub> | 3.3V | UART port 1 Receive data input   |
| UART1_TX           | 1        | O               | 3.3V | UART port 1 Transmit data output.  |
| UART1_CTS_L        | 1        | I <sub>PU</sub> | 3.3V | UART port 1 Clear to Send  |
| UART1_RTS_L        | 1        | O               | 3.3V | UART port 1 Request to Send<br>Shared with SFLASH_BYTE_ADDR  |
| UART1_DTR_L        | 1        | O               | 3.3V | UART port 1 Data Terminal Ready  |
| UART1_DCD_L        | 1        | I <sub>PU</sub> | 3.3V | UART port 1 Data Carrier Detect  |
| UART1_DSR_L        | 1        | I <sub>PU</sub> | 3.3V | UART port 1 Data Set Ready   |
| UART1_RI_L         | 1        | I <sub>PU</sub> | 3.3V | UART port 1 Ring Indicator   |
| <b>SPI Port</b>    |          |                 |      |  |

**Table 8: BCM53334 Hardware Signals (Cont.)**

| <b>Pin Names</b>            | <b>Quantity</b> | <b>I/O</b>                           | <b>V</b> | <b>Pin Description</b>  |
|-----------------------------|-----------------|--------------------------------------|----------|---|
| SCK                         | 1               | I/O                                  | 3.3V     | Serial Port Interface Clock.<br>This clock output is driven low during idle in master mode. In slave mode it is the clock input to the serial port interface supplied by the SPI master.<br>Shared with LED_P8_2  |
| MISO                        | 1               | I/O                                  | 3.3V     | Master-In/Slave-Out.<br>Output signal driven with serial data during a serial port interface Read operations.<br>Shared with LED_P9_2   |
| MOSI                        | 1               | I/O                                  | 3.3V     | Master-Out/Slave-In.<br>This output is driven low during idle in master mode. In slave mode it is the input signal which receives control and address information for the serial port interface, as well as serial data during Write operations.<br>Shared with LED_P10_2 |
| SS_L                        | 1               | I/O                                  | 3.3V     | Slave Select.<br>This output is driven high during idle in master mode. In slave mode it is an active low signal that enables a serial port interface Read or Write operations.<br>Shared with LED_P11_2  |
| <b>QSPI FLASH Interface</b> |                 |                                      |          |   |
| SFLASH_CLK                  | 1               | O                                    | 3.3V     | SPI flash clock<br>This clock output is driven high during idle.  |
| SFLASH_CS_L                 | 1               | O                                    | 3.3V     | External SPI flash chip select<br>This chip select is driven high during idle.  |
| SFLASH_IO0                  | 1               | I/O                                  | 3.3V     | SFLASH_IO_0:<br><ul style="list-style-type: none"> <li>• SINGLE-SPI flash DO or MOSI</li> <li>• DUAL-SPI flash IO0</li> <li>• QUAD-SPI flash IO0</li> </ul> This output is driven low during idle.  |
| SFLASH_IO1                  | 1               | I <sub>PD</sub> /<br>O <sub>PD</sub> | 3.3V     | SFLASH_IO_1:<br><ul style="list-style-type: none"> <li>• SINGLE-SPI flash DI or MISO</li> <li>• DUAL-SPI flash IO1</li> <li>• QUAD-SPI flash IO1</li> </ul>   |
| SFLASH_IO2                  | 1               | I/O                                  | 3.3V     | SFLASH_IO_2:<br><ul style="list-style-type: none"> <li>• SINGLE-SPI flash WP_L</li> <li>• DUAL-SPI flash WP_L</li> <li>• QUAD-SPI flash IO2</li> </ul> This output is driven high during idle.  |

**Table 8: BCM53334 Hardware Signals (Cont.)**

| <b>Pin Names</b>              | <b>Quantity</b> | <b>I/O</b>      | <b>V</b> | <b>Pin Description</b>   |
|-------------------------------|-----------------|-----------------|----------|--|
| SFLASH_IO3                    | 1               | I/O             | 3.3V     | SFLASH_IO_3:<br><ul style="list-style-type: none"> <li>• SINGLE-SPI flash HOLD_L</li> <li>• DUAL-SPI flash HOLD_L</li> <li>• QUAD-SPI flash IO3</li> </ul> This output is driven high during idle.   |
| <b>Parallel LED Interface</b> |                 |                 |          |  |
| LED_P0_[2:0]                  | 3               | O               | 3.3V     | Per Port Parallel LED Indicators   |
| LED_P1_[2:0]                  | 3               | O               | 3.3V     | LED_P8_2 shared with SCK   |
| LED_P2_[2:0]                  | 3               | O               | 3.3V     | LED_P9_2 shared with MISO  |
| LED_P3_[2:0]                  | 3               | O               | 3.3V     | LED_P10_2 shared with MOSI   |
| LED_P4_[2:0]                  | 3               | O               | 3.3V     | LED_P11_2 shared with SS_L   |
| LED_P5_[2:0]                  | 3               | O               | 3.3V     |  |
| LED_P6_[2:0]                  | 3               | O               | 3.3V     |  |
| LED_P7_[2:0]                  | 3               | O               | 3.3V     |  |
| LED_P8_[2:0]                  | 3               | O               | 3.3V     |  |
| LED_P9_[2:0]                  | 3               | O               | 3.3V     |  |
| LED_P10_[2:0]                 | 3               | O               | 3.3V     |  |
| LED_P11_[2:0]                 | 3               | O               | 3.3V     |  |
| LED_P12_[2:0]                 | 3               | O               | 3.3V     |  |
| LED_P13_[2:0]                 | 3               | O               | 3.3V     |  |
| LED_P14_[2:0]                 | 3               | O               | 3.3V     |  |
| LED_P15_[2:0]                 | 3               | O               | 3.3V     |  |
| <b>Serial LED Interface</b>   |                 |                 |          |  |
| LED_CLK                       | 1               | O               | 3.3V     | Serial LED clock output  |
| LED_DATA                      | 1               | O               | 3.3V     | Serial LED data output<br>Shared with EXT_UC_IS_SPI  |
| <b>Strap Pins</b>             |                 |                 |          |  |
| OSC_XTAL_SEL                  | 1               | I <sub>PU</sub> | 3.3V     | Select External 25 MHz Oscillator or Crystal for system clock source<br>0: Use External Oscillator<br>1: Use External Crystal (Default)  |
| EXT_UC_PRESENT                | 1               | I <sub>PD</sub> | 3.3V     | [EXT_UC_PRESENT, EXT_UC_IS_SPI]  |
| EXT_UC_IS_SPI                 | 1               | I <sub>PD</sub> | 3.3V     | <ul style="list-style-type: none"> <li>• [0, x]: SPI master mode and BSC master mode</li> <li>• [1, 0]: SPI master mode and BSC slave mode</li> <li>• [1, 1]: SPI slave mode and BSC master mode</li> </ul> EXT_UC_IS_SPI shared with LED_DATA |
| IP_BOOT_DEV2                  | 1               | I <sub>PD</sub> | 3.3V     | IP_BOOT_DEV[2:0]   |
| IP_BOOT_DEV1                  | 1               | I <sub>PD</sub> | 3.3V     | CPU ARM boot device selection:   |
| IP_BOOT_DEV0                  | 1               | I <sub>PD</sub> | 3.3V     | <ul style="list-style-type: none"> <li>• 3'b000 - SPI-NOR Flash (BSPI/QSPI)</li> <li>• 3'b010 - Reserved</li> </ul>  |

**Table 8: BCM53334 Hardware Signals (Cont.)**

| <b>Pin Names</b>             | <b>Quantity</b> | <b>I/O</b>                     | <b>V</b> | <b>Pin Description</b>   |
|------------------------------|-----------------|--------------------------------|----------|--|
| LED_SPI_SEL[1:0]             | 2               | I <sub>PD</sub>                | 3.3V     | Select LED/SPI Function <ul style="list-style-type: none"> <li>• 0: LED Mode</li> <li>• 1: Reserved</li> <li>• 2: SPI Mode</li> <li>• 3: Reserved</li> </ul> |
| SFLASH_BYTE_ADDR             | 1               | I <sub>PU</sub>                | 3.3V     | SFLASH Byte Address <ul style="list-style-type: none"> <li>• 0: 4 byte address</li> <li>• 1: 3 byte address</li> </ul> Shared with UART1_RTS_L               |
| <b>Clock Input</b>           |                 |                                |          |  |
| XTALN                        | 1               | I                              | 1.0V     | 25M crystal differential input negative leg  |
| XTALP                        | 1               | I                              | 1.0V     | 25M crystal differential input positive leg  |
| <b>JTAG Interface</b>        |                 |                                |          |  |
| JTCK                         | 1               | I <sub>PD</sub>                | 3.3V     | JTAG test clock  |
| JTDO                         | 1               | O                              | 3.3V     | JTAG test data output  |
| JTMS                         | 1               | I <sub>PU</sub>                | 3.3V     | JTAG mode select   |
| JTRST                        | 1               | I <sub>PU</sub>                | 3.3V     | JTAG reset<br>Must be pulled low during normal switch operation.   |
| JTDI                         | 1               | I <sub>PU</sub>                | 3.3V     | JTAG test data input   |
| JTCE1, JTCE                  | 2               | I <sub>PD</sub>                | 3.3V     | JTAG test enable<br>[JTCE1, JTCE]<br>1X: JTAG Mode<br>01: ARM Debug Mode<br>00: Normal Mode<br>Must be pulled low during normal switch operation.            |
| <b>SWITCH GPHY Port 0-15</b> |                 |                                |          |  |
| GP0_TD0P                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 0 pair 0 positive leg   |
| GP0_TD0N                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 0 pair 0 negative leg   |
| GP0_TD1P                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 0 pair 1 positive leg   |
| GP0_TD1N                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 0 pair 1 negative leg   |
| GP0_TD2P                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 0 pair 2 positive leg   |
| GP0_TD2N                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 0 pair 2 negative leg   |
| GP0_TD3P                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 0 pair 3 positive leg   |
| GP0_TD3N                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 0 pair 3 negative leg   |
| GP1_TD0P                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 1 pair 0 positive leg   |
| GP1_TD0N                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 1 pair 0 negative leg   |
| GP1_TD1P                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 1 pair 1 positive leg   |
| GP1_TD1N                     | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 1 pair 1 negative leg   |

**Table 8: BCM53334 Hardware Signals (Cont.)**

| <b>Pin Names</b> | <b>Quantity</b> | <b>I/O</b>                     | <b>V</b> | <b>Pin Description</b>     |
|------------------|-----------------|--------------------------------|----------|----------------------------|
| GP1_TD2P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 1 pair 2 positive leg |
| GP1_TD2N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 1 pair 2 negative leg |
| GP1_TD3P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 1 pair 3 positive leg |
| GP1_TD3N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 1 pair 3 negative leg |
| GP2_TD0P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 2 pair 0 positive leg |
| GP2_TD0N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 2 pair 0 negative leg |
| GP2_TD1P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 2 pair 1 positive leg |
| GP2_TD1N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 2 pair 1 negative leg |
| GP2_TD2P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 2 pair 2 positive leg |
| GP2_TD2N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 2 pair 2 negative leg |
| GP2_TD3P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 2 pair 3 positive leg |
| GP2_TD3N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 2 pair 3 negative leg |
| GP3_TD0P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 3 pair 0 positive leg |
| GP3_TD0N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 3 pair 0 negative leg |
| GP3_TD1P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 3 pair 1 positive leg |
| GP3_TD1N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 3 pair 1 negative leg |
| GP3_TD2P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 3 pair 2 positive leg |
| GP3_TD2N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 3 pair 2 negative leg |
| GP3_TD3P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 3 pair 3 positive leg |
| GP3_TD3N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 3 pair 3 negative leg |
| GP4_TD0P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 4 pair 0 positive leg |
| GP4_TD0N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 4 pair 0 negative leg |
| GP4_TD1P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 4 pair 1 positive leg |
| GP4_TD1N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 4 pair 1 negative leg |
| GP4_TD2P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 4 pair 2 positive leg |
| GP4_TD2N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 4 pair 2 negative leg |
| GP4_TD3P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 4 pair 3 positive leg |
| GP4_TD3N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 4 pair 3 negative leg |
| GP5_TD0P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 5 pair 0 positive leg |
| GP5_TD0N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 5 pair 0 negative leg |
| GP5_TD1P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 5 pair 1 positive leg |
| GP5_TD1N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 5 pair 1 negative leg |
| GP5_TD2P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 5 pair 2 positive leg |
| GP5_TD2N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 5 pair 2 negative leg |
| GP5_TD3P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 5 pair 3 positive leg |



**Table 8: BCM53334 Hardware Signals (Cont.)**

| <b>Pin Names</b> | <b>Quantity</b> | <b>I/O</b>                     | <b>V</b> | <b>Pin Description</b>      |
|------------------|-----------------|--------------------------------|----------|-----------------------------|
| GP5_TD3N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 5 pair 3 negative leg  |
| GP6_TD0P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 6 pair 0 positive leg  |
| GP6_TD0N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 6 pair 0 negative leg  |
| GP6_TD1P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 6 pair 1 positive leg  |
| GP6_TD1N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 6 pair 1 negative leg  |
| GP6_TD2P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 6 pair 2 positive leg  |
| GP6_TD2N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 6 pair 2 negative leg  |
| GP6_TD3P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 6 pair 3 positive leg  |
| GP6_TD3N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 6 pair 3 negative leg  |
| GP7_TD0P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 7 pair 0 positive leg  |
| GP7_TD0N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 7 pair 0 negative leg  |
| GP7_TD1P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 7 pair 1 positive leg  |
| GP7_TD1N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 7 pair 1 negative leg  |
| GP7_TD2P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 7 pair 2 positive leg  |
| GP7_TD2N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 7 pair 2 negative leg  |
| GP7_TD3P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 7 pair 3 positive leg  |
| GP7_TD3N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 7 pair 3 negative leg  |
| GP8_TD0P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 8 pair 0 positive leg  |
| GP8_TD0N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 8 pair 0 negative leg  |
| GP8_TD1P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 8 pair 1 positive leg  |
| GP8_TD1N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 8 pair 1 negative leg  |
| GP8_TD2P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 8 pair 2 positive leg  |
| GP8_TD2N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 8 pair 2 negative leg  |
| GP8_TD3P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 8 pair 3 positive leg  |
| GP8_TD3N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 8 pair 3 negative leg  |
| GP9_TD0P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 9 pair 0 positive leg  |
| GP9_TD0N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 9 pair 0 negative leg  |
| GP9_TD1P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 9 pair 1 positive leg  |
| GP9_TD1N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 9 pair 1 negative leg  |
| GP9_TD2P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 9 pair 2 positive leg  |
| GP9_TD2N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 9 pair 2 negative leg  |
| GP9_TD3P         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 9 pair 3 positive leg  |
| GP9_TD3N         | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 9 pair 3 negative leg  |
| GP10_TD0P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 10 pair 0 positive leg |
| GP10_TD0N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 10 pair 0 negative leg |

**Table 8: BCM53334 Hardware Signals (Cont.)**

| <b>Pin Names</b> | <b>Quantity</b> | <b>I/O</b>                     | <b>V</b> | <b>Pin Description</b>      |
|------------------|-----------------|--------------------------------|----------|-----------------------------|
| GP10_TD1P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 10 pair 1 positive leg |
| GP10_TD1N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 10 pair 1 negative leg |
| GP10_TD2P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 10 pair 2 positive leg |
| GP10_TD2N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 10 pair 2 negative leg |
| GP10_TD3P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 10 pair 3 positive leg |
| GP10_TD3N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 10 pair 3 negative leg |
| GP11_TD0P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 11 pair 0 positive leg |
| GP11_TD0N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 11 pair 0 negative leg |
| GP11_TD1P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 11 pair 1 positive leg |
| GP11_TD1N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 11 pair 1 negative leg |
| GP11_TD2P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 11 pair 2 positive leg |
| GP11_TD2N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 11 pair 2 negative leg |
| GP11_TD3P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 11 pair 3 positive leg |
| GP11_TD3N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 11 pair 3 negative leg |
| GP12_TD0P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 12 pair 0 positive leg |
| GP12_TD0N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 12 pair 0 negative leg |
| GP12_TD1P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 12 pair 1 positive leg |
| GP12_TD1N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 12 pair 1 negative leg |
| GP12_TD2P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 12 pair 2 positive leg |
| GP12_TD2N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 12 pair 2 negative leg |
| GP12_TD3P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 12 pair 3 positive leg |
| GP12_TD3N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 12 pair 3 negative leg |
| GP13_TD0P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 13 pair 0 positive leg |
| GP13_TD0N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 13 pair 0 negative leg |
| GP13_TD1P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 13 pair 1 positive leg |
| GP13_TD1N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 13 pair 1 negative leg |
| GP13_TD2P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 13 pair 2 positive leg |
| GP13_TD2N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 13 pair 2 negative leg |
| GP13_TD3P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 13 pair 3 positive leg |
| GP13_TD3N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 13 pair 3 negative leg |
| GP14_TD0P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 14 pair 0 positive leg |
| GP14_TD0N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 14 pair 0 negative leg |
| GP14_TD1P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 14 pair 1 positive leg |
| GP14_TD1N        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 14 pair 1 negative leg |
| GP14_TD2P        | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 14 pair 2 positive leg |

**Table 8: BCM53334 Hardware Signals (Cont.)**

| <b>Pin Names</b>           | <b>Quantity</b> | <b>I/O</b>                     | <b>V</b> | <b>Pin Description</b>   |
|----------------------------|-----------------|--------------------------------|----------|--|
| GP14_TD2N                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 14 pair 2 negative leg  |
| GP14_TD3P                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 14 pair 3 positive leg  |
| GP14_TD3N                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 14 pair 3 negative leg  |
| GP15_TD0P                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 15 pair 0 positive leg  |
| GP15_TD0N                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 15 pair 0 negative leg  |
| GP15_TD1P                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 15 pair 1 positive leg  |
| GP15_TD1N                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 15 pair 1 negative leg  |
| GP15_TD2P                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 15 pair 2 positive leg  |
| GP15_TD2N                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 15 pair 2 negative leg  |
| GP15_TD3P                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 15 pair 3 positive leg  |
| GP15_TD3N                  | 1               | I <sub>A</sub> /O <sub>A</sub> | 1.0V     | Port 15 pair 3 negative leg  |
| <b>QSGMII Port Signals</b> |                 |                                |          |  |
| QS2_RD[1:0]N               | 2               | I                              | 1.0V     | QSGMII 2 received serial 5.0 Gbps data—Negative leg of the differential pair.  |
| QS2_RD[1:0]P               | 2               | I                              | 1.0V     | QSGMII 2 received serial 5.0 Gbps data—Positive leg of the differential pair.  |
| QS2_TD[1:0]N               | 2               | O                              | 1.0V     | QSGMII 2 transmit serial 5.0 Gbps data—Negative leg of the differential pair.  |
| QS2_TD[1:0]P               | 2               | O                              | 1.0V     | QSGMII 2 transmit serial 5.0 Gbps data—Positive leg of the differential pair.  |
| EXT_QS2_CLKP               | 1               | O                              |          | Positive leg of differential reference clock out for external PHY  |
| EXT_QS2_CLKN               | 1               | O                              |          | Negative leg of differential reference clock out for external PHY  |
| <b>MIIM Interface</b>      |                 |                                |          |  |
| GIG_MDC                    | 1               | B <sub>PU</sub>                | 3.3V     | Serial management clock, used to communicate to external GPHY devices under software control. Clause 22 compliant.         |
| GIG_MDIO                   | 1               | B <sub>PU</sub>                | 3.3V     | Serial management data, used to communicate to external GPHY devices under software control. Clause 22 compliant.          |
| XG_MDC                     | 1               | B <sub>PU</sub>                | 3.3V     | Serial management clock, used to communicate to external GPHY devices under software control. Clauses 22 and 45 compliant. |
| XG_MDIO                    | 1               | B <sub>PU</sub>                | 3.3V     | Serial management data, used to communicate to external GPHY devices under software control. Clauses 22 and 45 compliant.  |
| <b>BSC Interface</b>       |                 |                                |          |  |

**Table 8: BCM53334 Hardware Signals (Cont.)**

| <b>Pin Names</b>                 | <b>Quantity</b> | <b>I/O</b>                     | <b>V</b> | <b>Pin Description</b>  |
|----------------------------------|-----------------|--------------------------------|----------|---|
| BSC_SA[1:0]                      | 2               | I <sub>PD</sub>                | 3.3V     | BSC Address [1:0]. <ul style="list-style-type: none"> <li>0: Address is 0x80 (Default)</li> <li>1: Address is 0x81</li> <li>2: Address is 0x82</li> <li>3: Address is 0x83</li> </ul> |
| BSC_SCL                          | 1               | B <sub>OD</sub>                | 3.3V     | BSC master clock. External pull-up resistor is required   |
| BSC_SDA                          | 1               | B <sub>OD</sub>                | 3.3V     | BSC serial data. External pull-up resistor is required  |
| <b>Miscellaneous Signals</b>     |                 |                                |          |   |
| SYS_RST_L                        | 1               | I <sub>PU</sub>                | 3.3V     | Reset input for the whole chip  |
| RDAC[3:0]                        | 4               | I <sub>B</sub> /O <sub>B</sub> | –        | DAC Bias Resistor.<br>Adjusts the drive level of the transmit DAC.<br>A 6.04 K $\pm$ 1% resistor to GND is required.  |
| VSS_SENSE                        | 1               | O                              | 0V       | Ground monitor.<br>Required for remote sensing of GND rail. This pin connects directly to die GND rail.   |
| VDD_SENSE                        | 1               | O                              | 1.0V     | Core voltage monitor.<br>Required for remote sensing of VDDC rail. This pin connects directly to die VDDC rail.   |
| AVS0                             | 1               | O                              | 3.3V     | Reserved  |
| DNC                              | 29              | –                              | –        | Do not connect these pins.  |
| <b>Miscellaneous PLL Signals</b> |                 |                                |          |   |
| XG_PLL2_REFCLKN                  | 1               | I                              | 1.0V     | PLL external reference clock input  |
| XG_PLL2_REFCLKP                  | 1               | I                              | 1.0V     |   |
| LC_PLL0_REFCLKN                  | 1               | I                              | 1.0V     | QSGMII/QGPHYREFCLK PLL external reference clock input   |
| LC_PLL0_REFCLKP                  | 1               | I                              | 1.0V     |   |
| <b>DIGITAL POWER</b>             |                 |                                |          |   |
| QS2_VDD                          | –               | PWR                            | 1.0V     | Power for QSGMII 2  |
| VDDC                             | –               | PWR                            | 1.0V     | Power for core  |
| VDD33                            | –               | PWR                            | 3.3V     | 3.3V VDD  |
| IP_PFLASH_VDDO                   | –               | PWR                            | 3.3V     | Power for PFLASH  |
| CORE_PLL_VDD33                   | 1               | PWR                            | 3.3V     | Power for core PLL  |
| GEN_PLL_VDD10                    | 1               | PWR                            | 1.0V     | Power for generic PLL   |
| GP0_PLLVDD10                     | 1               | PWR                            | 1.0V     | 1.0V for QGPHY 0 PLL  |
| GP0_PLLVDD33                     | 1               | PWR                            | 3.3V     | 3.3V for QGPHY 0 PLL, should be connected to GP0_BVDD33 on PCB.   |
| GP1_PLLVDD10                     | 1               | PWR                            | 1.0V     | 1.0V for QGPHY 1 PLL  |
| GP1_PLLVDD33                     | 1               | PWR                            | 3.3V     | 3.3V for QGPHY 1 PLL, should be connected to GP1_BVDD33 on PCB.   |
| GP2_PLLVDD10                     | 1               | PWR                            | 1.0V     | 1.0V for QGPHY 2 PLL  |
| GP2_PLLVDD33                     | 1               | PWR                            | 3.3V     | 3.3V for QGPHY 2 PLL, should be connected to GP2_BVDD33 on PCB.   |

**Table 8: BCM53334 Hardware Signals (Cont.)**

| <b>Pin Names</b>     | <b>Quantity</b> | <b>I/O</b> | <b>V</b> | <b>Pin Description</b>  |
|----------------------|-----------------|------------|----------|---|
| GP3_PLLVDD10         | 1               | PWR        | 1.0V     | 1.0V for QGPHY 3 PLL  |
| GP3_PLLVDD33         | 1               | PWR        | 3.3V     | 3.3V for QGPHY 3 PLL, should be connected to GP3_BVDD33 on PCB.       |
| <b>ANALOG POWER</b>  |                 |            |          |   |
| GP_AVDDL             | –               | PWR        | 1.0V     | 1.0V for QGPHY analog supply  |
| GP_AVDDH             | –               | PWR        | 3.3V     | 3.3V for QGPHY analog supply  |
| LC_PLL0_AVDD33       | 1               | PWR        | 3.3V     | QGPHY and QSGMII PLL  |
| GP0_BVDD33           | 1               | PWR        | 3.3V     | 3.3V for QGPHY 0 Bandgap, should be connected to GP0_PLLVDD33 on PCB. |
| GP1_BVDD33           | 1               | PWR        | 3.3V     | 3.3V for QGPHY 1 Bandgap, should be connected to GP1_PLLVDD33 on PCB. |
| GP2_BVDD33           | 1               | PWR        | 3.3V     | 3.3V for QGPHY 2 Bandgap, should be connected to GP2_PLLVDD33 on PCB. |
| GP3_BVDD33           | 1               | PWR        | 3.3V     | 3.3V for QGPHY 3 Bandgap, should be connected to GP3_PLLVDD33 on PCB. |
| QS2_PVDD             | –               | PWR        | 1.0V     | 1.0V, Filtered PLL voltage for QSGMII 2 clock distribution.           |
| AVDD33               | 1               | PWR        | 3.3V     | Analog Power for PVT Monitor  |
| XTAL_AVDD            | 1               | PWR        | 1.0V     | Power for internal oscillator   |
| <b>GROUND</b>        |                 |            |          |   |
| GND                  | –               | GND        | 0V       | Ground  |
| GND_1K               | 1               | GND        | 0V       | This pin must be tied to ground through a 1K Ohm resistor.            |
| GEN_PLL_VSS          | 1               | GND        | 0V       | Ground  |
| <b>ANALOG GROUND</b> |                 |            |          |   |
| AVSS                 | –               | GND        | 0V       | Ground  |
| CORE_PLL_AVSS        | –               | GND        | 0V       | Ground  |
| LC_PLL0_AVSS         | –               | GND        | 0V       | Ground  |
| LC_PLL1_AVSS         | –               | GND        | 0V       | Ground  |
| QS2_AVSS             | –               | GND        | 0V       | Ground  |
| XG_PLL2_AVSS         | –               | GND        | 0V       | Ground  |
| XTAL_AVSS            | –               | GND        | 0V       | Ground  |

## Pin List by Pin Name

**Table 9: Pin List by Pin Name - BCM53334 Devices**

| Ball | Signal Name     | Ball | Signal Name  | Ball | Signal Name | Ball | Signal Name |
|------|-----------------|------|--------------|------|-------------|------|-------------|
| A10  | XG_PLL2_REFCLKN | AA23 | GP_AVDDH     | AB7  | GP_AVDDH    | AD16 | GP_AVDDH    |
| A11  | DNC             | AA24 | AVSS         | AB8  | GP_AVDDH    | AD17 | AVSS        |
| A12  | DNC             | AA25 | AVSS         | AB9  | AVSS        | AD18 | RDAC2       |
| A13  | AVSS            | AA26 | GP14_TD3P    | AC1  | GP2_TD0N    | AD19 | AVSS        |
| A14  | DNC             | AA27 | GP14_TD3N    | AC10 | GP1_BVDD33  | AD2  | GP2_TD2P    |
| A15  | AVSS            | AA3  | GP1_TD2P     | AC11 | AVSS        | AD20 | AVSS        |
| A17  | SFLASH_CLK      | AA4  | AVSS         | AC12 | AVSS        | AD21 | RDAC3       |
| A18  | DNC             | AA5  | AVSS         | AC13 | AVSS        | AD22 | AVSS        |
| A2   | GND             | AA6  | GP_AVDDH     | AC14 | AVSS        | AD23 | AVSS        |
| A20  | GPIO0           | AA7  | GP_AVDDH     | AC15 | AVSS        | AD24 | DNC         |
| A21  | GPIO2           | AA8  | GP_AVDDH     | AC16 | AVSS        | AD25 | AVSS        |
| A23  | JTDO            | AA9  | GP_AVDDH     | AC17 | AVSS        | AD26 | GP13_TD0P   |
| A24  | BSC_SCL         | AB1  | GP1_TD1N     | AC18 | AVSS        | AD27 | GP13_TD0N   |
| A25  | JTRST           | AB10 | GP0_BVDD33   | AC19 | AVSS        | AD3  | GP2_TD2N    |
| A26  | DNC             | AB11 | AVSS         | AC2  | GP2_TD0P    | AD4  | AVSS        |
| A27  | XTAL_AVSS       | AB12 | GP0_PLLVDD33 | AC20 | GP3_BVDD33  | AD5  | AVSS        |
| A3   | LED_SPI_SELO    | AB13 | AVSS         | AC21 | AVSS        | AD6  | DNC         |
| A4   | UART1_RI_L      | AB14 | GP1_PLLVDD33 | AC22 | AVSS        | AD7  | AVSS        |
| A6   | UART1_TX        | AB15 | AVSS         | AC23 | DNC         | AD8  | AVSS        |
| A7   | GIG_MDIO        | AB16 | GP2_PLLVDD33 | AC24 | AVSS        | AD9  | RDAC0       |
| A8   | XG_MDIO         | AB17 | AVSS         | AC25 | GP13_TD1P   | AE1  | GP2_TD3P    |
| A9   | XG_PLL2_AVSS    | AB18 | GP3_PLLVDD33 | AC26 | GP13_TD1N   | AE10 | GP6_TD1P    |
| AA10 | AVSS            | AB19 | AVSS         | AC27 | GP14_TD0P   | AE11 | GP6_TD3P    |
| AA11 | AVSS            | AB2  | GP1_TD1P     | AC28 | GP14_TD0N   | AE12 | AVSS        |
| AA12 | GP0_PLLVDD10    | AB20 | GP2_BVDD33   | AC3  | GP2_TD1P    | AE13 | GP7_TD1P    |
| AA13 | AVSS            | AB21 | AVSS         | AC4  | GP2_TD1N    | AE14 | GP8_TD0P    |
| AA14 | GP1_PLLVDD10    | AB22 | GP_AVDDH     | AC5  | AVSS        | AE15 | AVSS        |
| AA15 | AVSS            | AB23 | GP_AVDDH     | AC6  | AVSS        | AE16 | GP8_TD3P    |
| AA16 | GP2_PLLVDD10    | AB24 | AVSS         | AC7  | DNC         | AE17 | GP9_TD2P    |
| AA17 | AVSS            | AB25 | GP14_TD2P    | AC8  | AVSS        | AE18 | AVSS        |
| AA18 | GP3_PLLVDD10    | AB26 | GP14_TD2N    | AC9  | AVSS        | AE19 | GP10_TD0P   |
| AA19 | AVSS            | AB27 | GP14_TD1P    | AD10 | AVSS        | AE2  | GP2_TD3N    |
| AA2  | GP1_TD2N        | AB28 | GP14_TD1N    | AD11 | AVSS        | AE20 | GP10_TD2P   |
| AA20 | AVSS            | AB3  | GP1_TD0N     | AD12 | RDAC1       | AE21 | AVSS        |
| AA21 | GP_AVDDH        | AB4  | GP1_TD0P     | AD13 | AVSS        | AE22 | GP11_TD2P   |
| AA22 | GP_AVDDH        | AB5  | AVSS         | AD14 | GP_AVDDH    | AE23 | GP11_TD0P   |
|      |                 | AB6  | GP_AVDDH     | AD15 | GP_AVDDH    | AE24 | AVSS        |

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name     | Ball | Signal Name   |
|------|-------------|------|-------------|------|-----------------|------|---------------|
| AE25 | GP12_TD2P   | AG1  | GP6_TD0P    | AH10 | GP6_TD0N        | B3   | LED_SPI_SEL1  |
| AE26 | AVSS        | 0    |             | AH11 | GP6_TD2N        | B4   | UART1_DTR_L   |
| AE27 | GP13_TD2P   | AG11 | GP6_TD2P    | AH13 | GP7_TD2N        | B5   | UART1_DCD_L   |
| AE28 | GP13_TD2N   | AG1  | GP7_TD3N    | AH14 | GP7_TD0N        | B6   | UART1_RX      |
| AE3  | GP3_TD3P    | 2    |             | AH16 | GP8_TD2N        | B7   | GIG_MDC       |
| AE4  | GP3_TD3N    | AG1  | GP7_TD2P    | AH17 | GP9_TD3N        | B8   | XG_MDC        |
| AE5  | GP4_TD1P    | 3    |             | AH19 | GP9_TD0N        | B9   | XG_PLL2_AVSS  |
| AE6  | AVSS        | AG1  | GP7_TD0P    | AH2  | AVSS            | C1   | LED_P1_2      |
| AE7  | GP5_TD3P    | 4    |             | AH20 | GP10_TD1N       | C10  | XG_PLL2_AVDD3 |
| AE8  | GP5_TD1P    | AG1  | GP8_TD1N    | AH22 | GP11_TD3N       | 3    |               |
| AE9  | AVSS        | 5    |             | AH23 | GP11_TD1N       | C11  | CORE_PLL_VDD  |
| AF1  | GP3_TD2P    | AG1  | GP8_TD2P    | AH25 | GP12_TD1N       | 33   |               |
| AF10 | GP6_TD1N    | 6    |             | AH26 | GP12_TD3N       | C12  | AVSS          |
| AF11 | GP6_TD3N    | AG1  | GP9_TD3P    | AH27 | AVSS            | C13  | AVSS          |
| AF12 | GP7_TD3P    | 7    |             | AH3  | GP3_TD1P        | C14  | AVSS          |
| AF13 | GP7_TD1N    | AG1  | GP9_TD1N    | AH4  | GP3_TD0P        | C15  | GND           |
| AF14 | GP8_TD0N    | 8    |             | AH5  | GP4_TD0N        | C16  | SFLASH_IO1    |
| AF15 | GP8_TD1P    | AG2  | AVSS        | AH7  | GP4_TD3N        | C17  | SFLASH_IO0    |
| AF16 | GP8_TD3N    | AG2  | GP10_TD1P   | AH8  | GP5_TD2N        | C18  | IP_BOOT_DEV0  |
| AF17 | GP9_TD2N    | 0    |             | B1   | GND             | C19  | GPIO5         |
| AF18 | GP9_TD1P    | AG2  | GP10_TD3N   | B10  | XG_PLL2_REFCLKP | C2   | LED_P0_2      |
| AF19 | GP10_TD0N   | 1    |             | B11  | DNC             | C20  | GPIO6         |
| AF2  | GP3_TD2N    | AG2  | GP11_TD3P   | B12  | DNC             | C21  | GPIO7         |
| AF20 | GP10_TD2N   | 2    |             | B13  | AVSS            | C22  | SYS_RST_L     |
| AF21 | GP10_TD3P   | AG2  | GP11_TD1P   | B14  | DNC             | C23  | JTMS          |
| AF22 | GP11_TD2N   | 3    |             | B15  | AVSS            | C24  | BSC_SA0       |
| AF23 | GP11_TD0N   | AG2  | GP12_TD0N   | B16  | SFLASH_CS_L     | C25  | XTAL_AVSS     |
| AF24 | GP12_TD0P   | 4    |             | B17  | SFLASH_IO3      | C26  | XTAL_AVDD     |
| AF25 | GP12_TD2N   | AG2  | GP12_TD1P   | B18  | DNC             | C27  | XTALP         |
| AF26 | AVSS        | 5    |             | B19  | GPIO4           | C28  | XTALN         |
| AF27 | GP13_TD3P   | 6    |             | B2   | GND             | C3   | LED_DATA      |
| AF28 | GP13_TD3N   | AG2  | AVSS        | B20  | GPIO1           | C4   | GND           |
| AF3  | AVSS        | 7    |             | B21  | GPIO3           | C5   | UART1_DSR_L   |
| AF4  | AVSS        | AG2  | AVSS        | B22  | JTDI            | C6   | UART1_RTS_L   |
| AF5  | GP4_TD1N    | 8    |             | B23  | JTCK            | C7   | DNC           |
| AF6  | GP4_TD2P    | AG3  | GP3_TD1N    | B24  | BSC_SDA         | C8   | GND           |
| AF7  | GP5_TD3N    | AG4  | GP3_TD0N    | B25  | JTCE            | C9   | XG_PLL2_AVSS  |
| AF8  | GP5_TD1N    | AG5  | GP4_TD0P    | B26  | XTAL_AVSS       | D1   | LED_P3_2      |
| AF9  | GP5_TD0P    | AG6  | GP4_TD2N    | B27  | XTAL_AVSS       | D10  | XG_PLL2_AVSS  |
| AG1  | AVSS        | AG7  | GP4_TD3P    | B28  | XTAL_AVSS       | D11  | CORE_PLL_AVSS |
|      |             | AG8  | GP5_TD2P    |      |                 | S    |               |
|      |             | AG9  | GP5_TD0N    |      |                 |      |               |

| Ball | Signal Name        | Ball | Signal Name   | Ball | Signal Name        | Ball | Signal Name |
|------|--------------------|------|---------------|------|--------------------|------|-------------|
| D12  | GND                | E23  | GND           | G1   | LED_P12_2          | J5   | GND         |
| D13  | AVSS               | E24  | GND           | G2   | LED_P11_2/SS_L     | J8   | GND         |
| D14  | GND                | E25  | QS2_AVSS      | G24  | QS2_AVSS           | J9   | GND         |
| D15  | GND                | E26  | QS2_AVSS      | G25  | QS2_AVSS           | K1   | LED_P9_1    |
| D16  | AVS0               | E27  | QS2_AVSS      | G26  | QS2_AVSS           | K10  | GND         |
| D17  | SFLASH_IO2         | E28  | QS2_AVSS      | G27  | QS2_AVSS           | K11  | GND         |
| D18  | IP_BOOT_DEV1       | E3   | LED_P4_2      | G28  | QS2_AVSS           | K12  | GND         |
| D19  | DNC                | E4   | LED_P7_2      | G3   | LED_P10_2/<br>MOSI | K13  | GND         |
| D2   | LED_P2_2           | E5   | GND           | G4   | LED_P13_2          | K14  | GND         |
| D20  | IP_BOOT_DEV2       | E6   | GND           | G5   | GND                | K15  | GND         |
| D21  | GND                | E7   | DNC           | H1   | LED_P15_2          | K16  | GND         |
| D22  | GND                | E8   | GND           | H2   | LED_P14_2          | K17  | DNC         |
| D23  | GND                | E9   | DNC           | H24  | QS2_VDD            | K18  | DNC         |
| D24  | BSC_SA1            | F10  | GND           | H25  | QS2_VDD            | K19  | GND         |
| D25  | XTAL_AVSS          | F11  | AVSS          | H26  | QS2_AVSS           | K2   | LED_P7_1    |
| D26  | XTAL_AVSS          | F12  | AVDD33        | H27  | QS2_RD0P           | K20  | GND         |
| D27  | XTAL_AVSS          | F13  | AVDD33        | H28  | QS2_RD0N           | K21  | GND         |
| D28  | XTAL_AVSS          | F14  | AVSS          | H3   | LED_P3_0           | K24  | QS2_AVSS    |
| D3   | LED_CLK            | F15  | VDD33         | H4   | LED_P3_1           | K25  | QS2_AVSS    |
| D4   | GND                | F16  | GND           | H5   | VDD33              | K26  | QS2_AVSS    |
| D5   | GND                | F17  | VDD33         | J10  | GND_1K             | K27  | QS2_TD1N    |
| D6   | UART1_CTS_L        | F18  | GND           | J11  | GND                | K28  | QS2_TD1P    |
| D7   | DNC                | F19  | GND           | J12  | GND                | K3   | LED_P0_0    |
| D8   | DNC                | F2   | LED_P9_2/MISO | J13  | GND                | K4   | LED_P0_1    |
| D9   | GND                | F20  | VDD33         | J14  | GND                | K5   | VDD33       |
| E1   | LED_P6_2           | F21  | GND           | J15  | GND                | K8   | GND         |
| E10  | GND                | F22  | VDD33         | J16  | GND                | K9   | GND         |
| E11  | AVSS               | F23  | GND           | J17  | AVDD33             | L1   | LED_P2_0    |
| E12  | GND                | F24  | GND           | J18  | GND                | L10  | GND         |
| E13  | AVSS               | F25  | QS2_AVSS      | J19  | GND                | L11  | GND         |
| E14  | GND                | F26  | QS2_AVSS      | J2   | LED_P5_1           | L12  | GND         |
| E15  | GND                | F27  | QS2_TD0N      | J20  | GND                | L13  | GND         |
| E16  | GND                | F28  | QS2_TD0P      | J21  | GND                | L14  | GND         |
| E17  | DNC                | F3   | LED_P8_2/SCK  | J24  | QS2_VDD            | L15  | GND         |
| E18  | DNC                | F4   | GND           | J25  | QS2_VDD            | L16  | GND         |
| E19  | GND                | F5   | VDD33         | J26  | QS2_AVSS           | L17  | GND         |
| E2   | LED_P5_2           | F6   | GND           | J27  | QS2_AVSS           | L18  | GND         |
| E20  | DNC                | F7   | VDD33         | J28  | QS2_AVSS           | L19  | GND         |
| E21  | EXT_UC_PRESE<br>NT | F8   | GND           | J3   | LED_P7_0           | L2   | LED_P2_1    |
| E22  | JTCE1              | F9   | DNC           | J4   | GND                | L20  | GND         |



| Ball | Signal Name       | Ball | Signal Name         | Ball | Signal Name        | Ball | Signal Name  |
|------|-------------------|------|---------------------|------|--------------------|------|--------------|
| L21  | GND               | N15  | GND                 | P5   | VDD33              | T21  | GND          |
| L24  | DNC               | N16  | GND                 | P8   | GND                | T24  | GND          |
| L25  | DNC               | N17  | GND                 | P9   | GND                | T25  | GND          |
| L26  | QS2_AVSS          | N18  | GND                 | R10  | GND                | T26  | LC_PLL0_AVSS |
| L27  | QS2_AVSS          | N19  | GND                 | R11  | GND                | T27  | EXT_QS2_CLKP |
| L28  | QS2_AVSS          | N2   | LED_P8_1            | R12  | GND                | T28  | EXT_QS2_CLKN |
| L3   | LED_P4_0          | N20  | GND                 | R13  | VDDC               | T3   | LED_P11_1    |
| L4   | LED_P4_1          | N21  | GND                 | R14  | VDDC               | T4   | LED_P13_0    |
| L5   | GND               | N24  | QS2_AVSS            | R15  | VDDC               | T5   | VDD33        |
| L8   | GND               | N25  | QS2_AVSS            | R16  | VDDC               | T8   | GND          |
| L9   | GND               | N26  | QS2_AVSS            | R17  | VDDC               | T9   | GND          |
| M10  | GND               | N27  | QS2_AVSS            | R18  | VDDC               | U1   | LED_P15_0    |
| M11  | GND               | N28  | QS2_AVSS            | R19  | VDDC               | U10  | AVSS         |
| M12  | GND               | N3   | LED_P10_0           | R2   | LED_P1_0           | U11  | AVSS         |
| M13  | VDDC              | N4   | LED_P10_1           | R20  | VDDC               | U12  | AVSS         |
| M14  | VDDC              | N5   | GND                 | R21  | VDDC               | U13  | AVSS         |
| M15  | VDDC              | N8   | GND                 | R24  | LC_PLL0_AVDD3<br>3 | U14  | AVSS         |
| M16  | VDDC              | N9   | GND                 | R25  | LC_PLL0_AVDD3<br>3 | U15  | AVSS         |
| M17  | VDDC              | P1   | LED_P12_0           | R26  | LC_PLL0_AVSS       | U16  | AVSS         |
| M18  | VDDC              | P10  | VSS_SENSE           | R27  | LC_PLL0_AVSS       | U17  | AVSS         |
| M19  | VDDC              | P11  | VDD_SENSE           | R28  | LC_PLL0_AVSS       | U18  | AVSS         |
| M2   | LED_P6_0          | P12  | GND                 | R3   | LED_P5_0           | U19  | AVSS         |
| M20  | VDDC              | P13  | VDDC                | R4   | GND                | U2   | LED_P15_1    |
| M21  | VDDC              | P14  | VDDC                | R5   | GND                | U20  | AVSS         |
| M24  | QS2_PVDD          | P15  | VDDC                | R8   | GND                | U21  | AVSS         |
| M25  | QS2_PVDD          | P16  | VDDC                | R9   | GND                | U24  | GND          |
| M26  | QS2_AVSS          | P17  | VDDC                | T1   | LED_P1_1           | U25  | LC_PLL0_AVSS |
| M27  | QS2_RD1P          | P18  | VDDC                | T10  | GND                | U26  | LC_PLL0_AVSS |
| M28  | QS2_RD1N          | P19  | VDDC                | T11  | GND                | U27  | LC_PLL0_AVSS |
| M3   | LED_P6_1          | P2   | LED_P12_1           | T12  | GND                | U28  | LC_PLL0_AVSS |
| M4   | GND               | P20  | VDDC                | T13  | GND                | U3   | LED_P14_0    |
| M5   | VDD33             | P21  | VDDC                | T14  | GND                | U4   | LED_P14_1    |
| M8   | GEN_PLL_VDD1<br>0 | P24  | LC_PLL0_AVSS        | T15  | GND                | U5   | GND          |
| M9   | GEN_PLL_VSS       | P25  | LC_PLL0_AVSS        | T16  | GND                | U8   | AVSS         |
| N1   | LED_P8_0          | P26  | LC_PLL0_AVSS        | T17  | GND                | U9   | AVSS         |
| N10  | GND               | P27  | LC_PLL0_REFCL<br>KP | T18  | GND                | V10  | GP_AVDDL     |
| N11  | GND               | P28  | LC_PLL0_REFCL<br>KN | T19  | GND                | V11  | GP_AVDDL     |
| N12  | GND               | P3   | LED_P11_0           | T2   | LED_P9_0           | V12  | GP_AVDDL     |
| N13  | GND               | P4   | LED_P13_1           | T20  | GND                | V13  | GP_AVDDL     |
| N14  | GND               |      |                     |      |                    | V14  | GP_AVDDL     |

| <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> |
|-------------|--------------------|-------------|--------------------|
| V15         | GP_AVDDL           | W2          | GP0_TD2P           |
| V16         | GP_AVDDL           | W24         | AVSS               |
| V17         | GP_AVDDL           | W25         | AVSS               |
| V18         | GP_AVDDL           | W26         | AVSS               |
| V19         | GP_AVDDL           | W27         | GP15_TD1P          |
| V2          | GP0_TD0N           | W28         | GP15_TD1N          |
| V20         | GP_AVDDL           | W3          | GP0_TD1N           |
| V21         | GP_AVDDL           | W4          | GP0_TD1P           |
| V24         | OSC_XTAL_SEL       | W5          | AVSS               |
| V25         | AVSS               | Y1          | GP1_TD3N           |
| V26         | AVSS               | Y2          | GP1_TD3P           |
| V27         | GP15_TD0P          | Y24         | AVSS               |
| V28         | GP15_TD0N          | Y25         | GP15_TD2P          |
| V3          | GP0_TD0P           | Y26         | GP15_TD2N          |
| V4          | AVSS               | Y27         | GP15_TD3P          |
| V5          | AVSS               | Y28         | GP15_TD3N          |
| V8          | GP_AVDDL           | Y3          | GP0_TD3N           |
| V9          | GP_AVDDL           | Y4          | GP0_TD3P           |
| W1          | GP0_TD2N           | Y5          | AVSS               |

## Pin List by Signal Name

**Table 10: Pin List by Signal Name - BCM53334 Devices**

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name   | Ball |
|-------------|------|-------------|------|-------------|------|---------------|------|
| AVDD33      | F12  | AVSS        | AC18 | AVSS        | B13  | BSC_SDA       | B24  |
| AVDD33      | F13  | AVSS        | AC19 | AVSS        | B15  | CORE_PLL_AVSS | D11  |
| AVDD33      | J17  | AVSS        | AC21 | AVSS        | C12  | CORE_PLL_VDD  | C11  |
| AVS0        | D16  | AVSS        | AC22 | AVSS        | C13  | 33            |      |
| AVSS        | A13  | AVSS        | AC24 | AVSS        | C14  | DNC           | A11  |
| AVSS        | A15  | AVSS        | AD10 | AVSS        | D13  | DNC           | A12  |
| AVSS        | AA4  | AVSS        | AD11 | AVSS        | E11  | DNC           | A14  |
| AVSS        | AA5  | AVSS        | AD13 | AVSS        | E13  | DNC           | A18  |
| AVSS        | AA10 | AVSS        | AD17 | AVSS        | F11  | DNC           | A26  |
| AVSS        | AA11 | AVSS        | AD19 | AVSS        | F14  | DNC           | AC7  |
| AVSS        | AA13 | AVSS        | AD20 | AVSS        | U8   | DNC           | AC23 |
| AVSS        | AA15 | AVSS        | AD22 | AVSS        | U9   | DNC           | AD24 |
| AVSS        | AA17 | AVSS        | AD23 | AVSS        | U10  | DNC           | AD6  |
| AVSS        | AA19 | AVSS        | AD25 | AVSS        | U11  | DNC           | B11  |
| AVSS        | AA20 | AVSS        | AD4  | AVSS        | U12  | DNC           | B12  |
| AVSS        | AA24 | AVSS        | AD5  | AVSS        | U13  | DNC           | B14  |
| AVSS        | AA25 | AVSS        | AD7  | AVSS        | U14  | DNC           | B18  |
| AVSS        | AB5  | AVSS        | AD8  | AVSS        | U15  | DNC           | C7   |
| AVSS        | AB9  | AVSS        | AE6  | AVSS        | U16  | DNC           | D7   |
| AVSS        | AB11 | AVSS        | AE9  | AVSS        | U17  | DNC           | D8   |
| AVSS        | AB13 | AVSS        | AE12 | AVSS        | U18  | DNC           | D19  |
| AVSS        | AB15 | AVSS        | AE15 | AVSS        | U19  | DNC           | E7   |
| AVSS        | AB17 | AVSS        | AE18 | AVSS        | U20  | DNC           | E9   |
| AVSS        | AB19 | AVSS        | AE21 | AVSS        | U21  | DNC           | E17  |
| AVSS        | AB21 | AVSS        | AE24 | AVSS        | V4   | DNC           | E18  |
| AVSS        | AB24 | AVSS        | AE26 | AVSS        | V5   | DNC           | E20  |
| AVSS        | AC5  | AVSS        | AF3  | AVSS        | V25  | DNC           | F9   |
| AVSS        | AC6  | AVSS        | AF4  | AVSS        | V26  | DNC           | K17  |
| AVSS        | AC8  | AVSS        | AF26 | AVSS        | W24  | DNC           | K18  |
| AVSS        | AC9  | AVSS        | AG1  | AVSS        | W25  | DNC           | L24  |
| AVSS        | AC11 | AVSS        | AG2  | AVSS        | W26  | DNC           | L25  |
| AVSS        | AC12 | AVSS        | AG2  | AVSS        | W5   | EXT_QS2_CLKN  | T28  |
| AVSS        | AC13 |             | 7    | AVSS        | Y5   | EXT_QS2_CLKP  | T27  |
| AVSS        | AC14 | AVSS        | AG2  | AVSS        | Y24  | EXT_UC_PRESE  | E21  |
| AVSS        | AC15 |             | 8    | BSC_SA0     | C24  | NT            |      |
| AVSS        | AC16 | AVSS        | AH2  | BSC_SA1     | D24  | GEN_PLL_VDD1  | M8   |
| AVSS        | AC17 | AVSS        | AH27 | BSC_SCL     | A24  | 0             |      |

| <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> |
|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|
| GEN_PLL_VSS        | M9          | GND                | J4          | GND                | L21         | GND                | T18         |
| GIG_MDC            | B7          | GND                | J5          | GND                | M4          | GND                | T19         |
| GIG_MDIO           | A7          | GND                | J8          | GND                | M10         | GND                | T20         |
| GND                | A2          | GND                | J9          | GND                | M11         | GND                | T21         |
| GND                | B1          | GND                | J11         | GND                | M12         | GND                | U5          |
| GND                | B2          | GND                | J12         | GND                | N5          | GND                | U24         |
| GND                | C4          | GND                | J13         | GND                | N8          | GND                | T24         |
| GND                | C8          | GND                | J14         | GND                | N9          | GND                | T25         |
| GND                | C15         | GND                | J15         | GND                | N10         | GND_1K             | J10         |
| GND                | D4          | GND                | J16         | GND                | N11         | GP_AVDDH           | AA6         |
| GND                | D5          | GND                | J18         | GND                | N12         | GP_AVDDH           | AA7         |
| GND                | D9          | GND                | J19         | GND                | N13         | GP_AVDDH           | AA8         |
| GND                | D12         | GND                | J20         | GND                | N14         | GP_AVDDH           | AA9         |
| GND                | D14         | GND                | J21         | GND                | N15         | GP_AVDDH           | AA21        |
| GND                | D15         | GND                | K8          | GND                | N16         | GP_AVDDH           | AA22        |
| GND                | D21         | GND                | K9          | GND                | N17         | GP_AVDDH           | AA23        |
| GND                | D22         | GND                | K10         | GND                | N18         | GP_AVDDH           | AB6         |
| GND                | D23         | GND                | K11         | GND                | N19         | GP_AVDDH           | AB7         |
| GND                | E5          | GND                | K12         | GND                | N20         | GP_AVDDH           | AB8         |
| GND                | E6          | GND                | K13         | GND                | N21         | GP_AVDDH           | AB22        |
| GND                | E8          | GND                | K14         | GND                | P8          | GP_AVDDH           | AB23        |
| GND                | E10         | GND                | K15         | GND                | P9          | GP_AVDDH           | AD14        |
| GND                | E12         | GND                | K16         | GND                | P12         | GP_AVDDH           | AD15        |
| GND                | E14         | GND                | K19         | GND                | R4          | GP_AVDDH           | AD16        |
| GND                | E15         | GND                | K20         | GND                | R5          | GP_AVDDL           | V8          |
| GND                | E16         | GND                | K21         | GND                | R8          | GP_AVDDL           | V9          |
| GND                | E19         | GND                | L5          | GND                | R9          | GP_AVDDL           | V10         |
| GND                | E23         | GND                | L8          | GND                | R10         | GP_AVDDL           | V11         |
| GND                | E24         | GND                | L9          | GND                | R11         | GP_AVDDL           | V12         |
| GND                | F4          | GND                | L10         | GND                | R12         | GP_AVDDL           | V13         |
| GND                | F6          | GND                | L11         | GND                | T8          | GP_AVDDL           | V14         |
| GND                | F8          | GND                | L12         | GND                | T9          | GP_AVDDL           | V15         |
| GND                | F10         | GND                | L13         | GND                | T10         | GP_AVDDL           | V16         |
| GND                | F16         | GND                | L14         | GND                | T11         | GP_AVDDL           | V17         |
| GND                | F18         | GND                | L15         | GND                | T12         | GP_AVDDL           | V18         |
| GND                | F19         | GND                | L16         | GND                | T13         | GP_AVDDL           | V19         |
| GND                | F21         | GND                | L17         | GND                | T14         | GP_AVDDL           | V20         |
| GND                | F23         | GND                | L18         | GND                | T15         | GP_AVDDL           | V21         |
| GND                | F24         | GND                | L19         | GND                | T16         | GP0_BVDD33         | AB10        |
| GND                | G5          | GND                | L20         | GND                | T17         | GP0_PLLVDD10       | AA12        |

| <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> |
|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|
| GP0_PLLVDD33       | AB12        | GP12_TD0P          | AF24        | GP2_TD2P           | AD2         | GP7_TD0P           | AG1         |
| GP0_TD0N           | V2          | GP12_TD1N          | AH25        | GP2_TD3N           | AE2         |                    | 4           |
| GP0_TD0P           | V3          | GP12_TD1P          | AG2         | GP2_TD3P           | AE1         | GP7_TD1N           | AF13        |
| GP0_TD1N           | W3          |                    | 5           | GP3_BVDD33         | AC20        | GP7_TD1P           | AE13        |
| GP0_TD1P           | W4          | GP12_TD2N          | AF25        | GP3_PLLVDD10       | AA18        | GP7_TD2N           | AH13        |
| GP0_TD2N           | W1          | GP12_TD2P          | AE25        | GP3_PLLVDD33       | AB18        | GP7_TD2P           | AG1         |
| GP0_TD2P           | W2          | GP12_TD3N          | AH26        | GP3_TD0N           | AG4         |                    | 3           |
| GP0_TD3N           | Y3          | GP12_TD3P          | AG2         | GP3_TD0P           | AH4         | GP7_TD3N           | AG1         |
| GP0_TD3P           | Y4          |                    | 6           | GP3_TD1N           | AG3         |                    | 2           |
| GP1_BVDD33         | AC10        | GP13_TD0N          | AD27        | GP3_TD1P           | AH3         | GP7_TD3P           | AF12        |
| GP1_PLLVDD10       | AA14        | GP13_TD0P          | AD26        | GP3_TD2N           | AF2         | GP8_TD0N           | AF14        |
| GP1_PLLVDD33       | AB14        | GP13_TD1N          | AC26        | GP3_TD2P           | AF1         | GP8_TD0P           | AE14        |
| GP1_TD0N           | AB3         | GP13_TD1P          | AC25        | GP3_TD3N           | AE40        | GP8_TD1N           | AG1         |
| GP1_TD0P           | AB4         | GP13_TD2N          | AE28        | GP3_TD3P           | AE3         |                    | 5           |
| GP1_TD1N           | AB1         | GP13_TD2P          | AE27        | GP4_TD0N           | AH5         | GP8_TD1P           | AF15        |
| GP1_TD1P           | AB2         | GP13_TD3N          | AF28        | GP4_TD0P           | AG5         | GP8_TD2N           | AH16        |
| GP1_TD2N           | AA2         | GP13_TD3P          | AF27        | GP4_TD1N           | AF5         | GP8_TD2P           | AG1         |
| GP1_TD2P           | AA3         | GP14_TD0N          | AC28        | GP4_TD1P           | AE5         |                    | 6           |
| GP1_TD3N           | Y1          | GP14_TD0P          | AC27        | GP4_TD2N           | AG6         | GP8_TD3N           | AF16        |
| GP1_TD3P           | Y2          | GP14_TD1N          | AB28        | GP4_TD2P           | AF6         | GP8_TD3P           | AE16        |
| GP10_TD0N          | AF19        | GP14_TD1P          | AB27        | GP4_TD3N           | AH7         | GP9_TD0N           | AH19        |
| GP10_TD0P          | AE19        | GP14_TD2N          | AB26        | GP4_TD3P           | AG7         | GP9_TD0P           | AG1         |
| GP10_TD1N          | AH20        | GP14_TD2P          | AB25        | GP5_TD0N           | AG9         |                    | 9           |
| GP10_TD1P          | AG2         | GP14_TD3N          | AA27        | GP5_TD0P           | AF9         | GP9_TD1N           | AG1         |
|                    | 0           | GP14_TD3P          | AA26        | GP5_TD1N           | AF8         |                    | 8           |
| GP10_TD2N          | AF20        | GP15_TD0N          | V28         | GP5_TD1P           | AE8         | GP9_TD1P           | AF18        |
| GP10_TD2P          | AE20        | GP15_TD0P          | V27         | GP5_TD2N           | AH8         | GP9_TD2N           | AF17        |
| GP10_TD3N          | AG2         | GP15_TD1N          | W28         | GP5_TD2P           | AG8         | GP9_TD2P           | AE17        |
|                    | 1           | GP15_TD1P          | W27         | GP5_TD3N           | AF7         | GP9_TD3N           | AH17        |
| GP10_TD3P          | AF21        | GP15_TD2N          | Y26         | GP5_TD3P           | AE7         | GP9_TD3P           | AG1         |
| GP11_TD0N          | AF23        | GP15_TD2P          | Y25         | GP6_TD0N           | AH10        |                    | 7           |
| GP11_TD0P          | AE23        | GP15_TD3N          | Y28         | GP6_TD0P           | AG1         | GPI00              | A20         |
| GP11_TD1N          | AH23        | GP15_TD3P          | Y27         |                    | 0           | GPI01              | B20         |
| GP11_TD1P          | AG2         | GP2_BVDD33         | AB20        | GP6_TD1N           | AF10        | GPI02              | A21         |
|                    | 3           | GP2_PLLVDD10       | AA16        | GP6_TD1P           | AE10        | GPI03              | B21         |
| GP11_TD2N          | AF22        | GP2_PLLVDD33       | AB16        | GP6_TD2N           | AH11        | GPI04              | B19         |
| GP11_TD2P          | AE22        | GP2_TD0N           | AC1         | GP6_TD2P           | AG11        | GPI05              | C19         |
| GP11_TD3N          | AH22        | GP2_TD0P           | AC2         | GP6_TD3N           | AF11        | GPI06              | C20         |
| GP11_TD3P          | AG2         | GP2_TD1N           | AC4         | GP6_TD3P           | AE11        | GPI07              | C21         |
|                    | 2           | GP2_TD1P           | AC3         | GP7_TD0N           | AH14        | IP_BOOT_DEV0       | C18         |
| GP12_TD0N          | AG2         | GP2_TD2N           | AD3         |                    |             | IP_BOOT_DEV1       | D18         |
|                    | 4           |                    |             |                    |             | IP_BOOT_DEV2       | D20         |

| <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> |
|--------------------|-------------|--------------------|-------------|--------------------|-------------|--------------------|-------------|
| JTCE               | B25         | LED_P12_1          | P2          | QS2_AVSS           | E27         | RDAC1              | AD12        |
| JTCE1              | E22         | LED_P12_2          | G1          | QS2_AVSS           | E28         | RDAC2              | AD18        |
| JTCK               | B23         | LED_P13_0          | T4          | QS2_AVSS           | F25         | RDAC3              | AD21        |
| JTDI               | B22         | LED_P13_1          | P4          | QS2_AVSS           | F26         | SFLASH_CLK         | A17         |
| JTDO               | A23         | LED_P13_2          | G4          | QS2_AVSS           | G24         | SFLASH_CS_L        | B16         |
| JTMS               | C23         | LED_P14_0          | U3          | QS2_AVSS           | G25         | SFLASH_IO0         | C17         |
| JTRST              | A25         | LED_P14_1          | U4          | QS2_AVSS           | G26         | SFLASH_IO1         | C16         |
| LC_PLL0_AVDD3      | R24         | LED_P14_2          | H2          | QS2_AVSS           | G27         | SFLASH_IO2         | D17         |
| 3                  |             | LED_P15_0          | U1          | QS2_AVSS           | G28         | SFLASH_IO3         | B17         |
| LC_PLL0_AVDD3      | R25         | LED_P15_1          | U2          | QS2_AVSS           | H26         | SYS_RST_L          | C22         |
| 3                  |             | LED_P15_2          | H1          | QS2_AVSS           | J26         | UART1_CTS_L        | D6          |
| LC_PLL0_AVSS       | P24         | LED_P2_0           | L1          | QS2_AVSS           | J27         | UART1_DCD_L        | B5          |
| LC_PLL0_AVSS       | P25         | LED_P2_1           | L2          | QS2_AVSS           | J28         | UART1_DSR_L        | C5          |
| LC_PLL0_AVSS       | P26         | LED_P2_2           | D2          | QS2_AVSS           | K24         | UART1_DTR_L        | B4          |
| LC_PLL0_AVSS       | R26         | LED_P3_0           | H3          | QS2_AVSS           | K25         | UART1_RI_L         | A4          |
| LC_PLL0_AVSS       | R27         | LED_P3_1           | H4          | QS2_AVSS           | K26         | UART1_RTS_L        | C6          |
| LC_PLL0_AVSS       | R28         | LED_P3_2           | D1          | QS2_AVSS           | L26         | UART1_RX           | B6          |
| LC_PLL0_AVSS       | T26         | LED_P4_0           | L3          | QS2_AVSS           | L27         | UART1_TX           | A6          |
| LC_PLL0_AVSS       | U25         | LED_P4_1           | L4          | QS2_AVSS           | L28         | VDD_SENSE          | P11         |
| LC_PLL0_AVSS       | U26         | LED_P4_2           | E3          | QS2_AVSS           | M26         | VDD33              | F5          |
| LC_PLL0_AVSS       | U27         | LED_P5_0           | R3          | QS2_AVSS           | N24         | VDD33              | F7          |
| LC_PLL0_AVSS       | U28         | LED_P5_1           | J2          | QS2_AVSS           | N25         | VDD33              | F15         |
| LC_PLL0_REFCL      | P28         | LED_P5_2           | E2          | QS2_AVSS           | N26         | VDD33              | F17         |
| KN                 |             | LED_P6_0           | M2          | QS2_AVSS           | N27         | VDD33              | F20         |
| LC_PLL0_REFCL      | P27         | LED_P6_1           | M3          | QS2_AVSS           | N28         | VDD33              | F22         |
| KP                 |             | LED_P6_2           | E1          | QS2_PVDD           | M24         | VDD33              | H5          |
| LED_CLK            | D3          | LED_P7_0           | J3          | QS2_PVDD           | M25         | VDD33              | K5          |
| LED_DATA           | C3          | LED_P7_1           | K2          | QS2_RD0N           | H28         | VDD33              | M5          |
| LED_P0_0           | K3          | LED_P7_2           | E4          | QS2_RD0P           | H27         | VDD33              | P5          |
| LED_P0_1           | K4          | LED_P8_0           | N1          | QS2_RD1N           | M28         | VDD33              | T5          |
| LED_P0_2           | C2          | LED_P8_1           | N2          | QS2_RD1P           | M27         | VDDC               | M13         |
| LED_P1_0           | R2          | LED_P8_2/SCK       | F3          | QS2_TD0N           | F27         | VDDC               | M14         |
| LED_P1_1           | T1          | LED_P9_0           | T2          | QS2_TD0P           | F28         | VDDC               | M15         |
| LED_P1_2           | C1          | LED_P9_1           | K1          | QS2_TD1N           | K27         | VDDC               | M16         |
| LED_P10_0          | N3          | LED_P9_2/MISO      | F2          | QS2_TD1P           | K28         | VDDC               | M17         |
| LED_P10_1          | N4          | LED_SPI_SEL0       | A3          | QS2_VDD            | H24         | VDDC               | M18         |
| LED_P10_2/         | G3          | LED_SPI_SEL1       | B3          | QS2_VDD            | H25         | VDDC               | M19         |
| MOSI               |             | OSC_XTAL_SEL       | V24         | QS2_VDD            | J24         | VDDC               | M20         |
| LED_P11_0          | P3          | QS2_AVSS           | E25         | QS2_VDD            | J25         | VDDC               | M21         |
| LED_P11_1          | T3          | QS2_AVSS           | E26         | RDAC0              | AD9         | VDDC               | P13         |
| LED_P11_2/SS_L     | G2          |                    |             |                    |             |                    |             |
| LED_P12_0          | P1          |                    |             |                    |             |                    |             |

| <b>Signal Name</b> | <b>Ball</b> | <b>Signal Name</b> | <b>Ball</b> |
|--------------------|-------------|--------------------|-------------|
| VDDC               | P14         | XTALP              | C27         |
| VDDC               | P15         |                    |             |
| VDDC               | P16         |                    |             |
| VDDC               | P17         |                    |             |
| VDDC               | P18         |                    |             |
| VDDC               | P19         |                    |             |
| VDDC               | P20         |                    |             |
| VDDC               | P21         |                    |             |
| VDDC               | R13         |                    |             |
| VDDC               | R14         |                    |             |
| VDDC               | R15         |                    |             |
| VDDC               | R16         |                    |             |
| VDDC               | R17         |                    |             |
| VDDC               | R18         |                    |             |
| VDDC               | R19         |                    |             |
| VDDC               | R20         |                    |             |
| VDDC               | R21         |                    |             |
| VSS_SENSE          | P10         |                    |             |
| XG_MDC             | B8          |                    |             |
| XG_MDIO            | A8          |                    |             |
| XG_PLL2_AVDD3      | C10         |                    |             |
|                    | 3           |                    |             |
| XG_PLL2_AVSS       | A9          |                    |             |
| XG_PLL2_AVSS       | B9          |                    |             |
| XG_PLL2_AVSS       | C9          |                    |             |
| XG_PLL2_AVSS       | D10         |                    |             |
| XG_PLL2_REFCL      | A10         |                    |             |
|                    | KN          |                    |             |
| XG_PLL2_REFCL      | B10         |                    |             |
|                    | KP          |                    |             |
| XTAL_AVDD          | C26         |                    |             |
| XTAL_AVSS          | A27         |                    |             |
| XTAL_AVSS          | B26         |                    |             |
| XTAL_AVSS          | B27         |                    |             |
| XTAL_AVSS          | B28         |                    |             |
| XTAL_AVSS          | C25         |                    |             |
| XTAL_AVSS          | D25         |                    |             |
| XTAL_AVSS          | D26         |                    |             |
| XTAL_AVSS          | D27         |                    |             |
| XTAL_AVSS          | D28         |                    |             |
| XTALN              | C28         |                    |             |

## Section 8: Electrical Specifications

### Absolute Maximum Ratings

The specifications shown in [Table 12](#) indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

**Table 11: Absolute Maximum Ratings**

| Parameter  | Symbol           | Min.  | Max.  | Units | Notes |
|--|------------------|-------|-------|-------|-------|
| 1.00V, Core Voltage                              | –                | –0.50 | +1.37 | V     | –     |
| 1.00V, Analog Voltage                            | –                | –0.40 | +1.37 | V     | –     |
| 3.30V, I/O Voltage                               | –                | –0.50 | +4.10 | V     | –     |
| Storage Temperature                              | T <sub>STG</sub> | –40   | +125  | °C    | –     |
| Electrostatic Discharge (ESD) (non-SerDes pins)  | V <sub>ESD</sub> | –     | –     | –     | –     |
| – Human Body Model (HBM) per EIA/JESD22-A114-E   |                  | –     | ±2000 | V     | –     |
| – Machine Model (MM) per EIA/JESD-A115-A         |                  | –     | ±100  | V     | –     |
| – Charge Device Model (CDM) per EIA/JESD22-C101C |                  | –     | ±300  | V     | –     |
| ESD (QSGMII SerDes pins)                         | V <sub>ESD</sub> | –     | –     | –     | –     |
| – Human Body Model per EIA/JESD22-A114-E         |                  | –     | ±1400 | V     | –     |
| – Machine Model per EIA/JESD-A115-A              |                  | –     | ±75   | V     | –     |
| – Charge Device Model per EIA/JESD22-C101C       |                  | –     | ±200  | V     | –     |



## DC Characteristics

### Operating Conditions

Broadcom recommends operating the BCM53334 under the following conditions shown in [Table 12](#).

**Table 12: Operating Conditions**

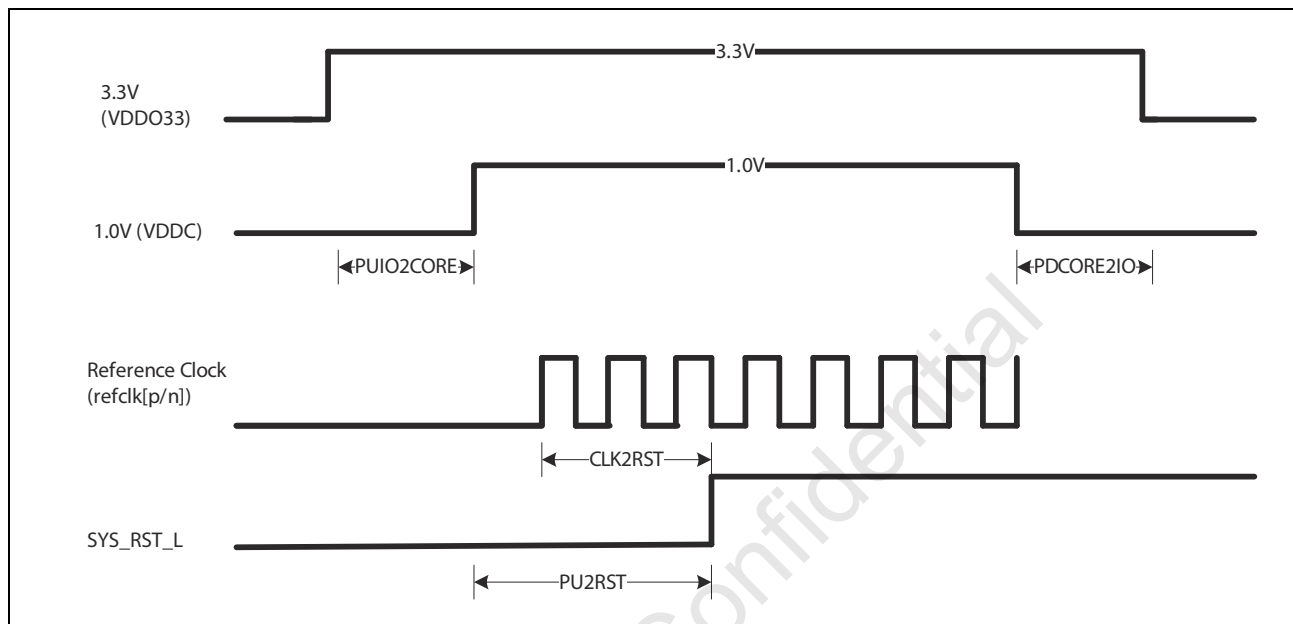
| <b>Parameter</b>                             | <b>Symbol</b>  | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b> | <b>Units</b> |
|--|----------------|-------------|-------------|-------------|--------------|
| 1.00V $\pm 2\%$ , Core Voltage               | –              | 0.980       | 1.00        | 1.020       | V            |
| 1.00V $\pm 2\%$ , Analog Voltage             | –              | 0.980       | 1.00        | 1.020       | V            |
| 3.30V $\pm 5\%$ , I/O Voltage                | –              | 3.135       | 3.30        | 3.465       | V            |
| Ambient Temperature                          | T <sub>A</sub> | 0           | –           | 70          | °C           |
| Ambient Temperature (Industrial Temperature) | T <sub>A</sub> | –40         | –           | +85         | °C           |
| Junction Temperature <sup>a</sup>            | T <sub>J</sub> | –           | –           | 125         | °C           |

- a. Device must not operate at Maximum junction temperature 125°C for extended periods of time. Steady state temperature is 110°C.

## Power-Up and Power-Down Specifications

The power-up and power-down requirements for the BCM53334 are outlined in [Figure 12](#). Violating sequencing can cause latch-up damage to the device.

**Figure 12: Power-Up and Power-Down Timing**



**Note:** When a crystal is used as the external clock source, there is no CLK2RST requirement.

**Table 13: AC Specifications for Power-Up and Power-Down**

| Symbol                 | Parameter  | Min.                    | Typ. | Max. | Unit | Notes |
|------------------------|--|-------------------------|------|------|------|-------|
| t <sub>PUIO2CORE</sub> | VDDO (3.3, 1.5/1.8, 1.2) to VDDC/Analog PWR (1.0V) power-up time               | 0                       | –    | 5    | ms   | 1     |
| t <sub>PDCORE2IO</sub> | VDDO (3.3, 1.5/1.8, 1.2) to VDDC/Analog PWR (1.0V) power-down time             | 0                       | –    | –    | ms   | 1, 4  |
| t <sub>PU2RST</sub>    | All voltages at valid operating conditions to the deassertion of sys_rst_n     | 40                      | –    | –    | ms   | 1, 3  |
| t <sub>CLK2RST</sub>   | All clocks valid to the deassertion of sys_rst_n                               | t <sub>PU2RST</sub> – 5 | –    | –    | ms   | 2, 3  |
| t <sub>COR2LCK</sub>   | Time for the core clock to internally become valid and allow register accesses | 1                       | –    | –    | ms   | 2, 3  |
| t <sub>RAMP</sub>      | Ramp time for each voltage rail 10% to 90%                                     | 0                       | –    | 5    | ms   | –     |

**Note:**

1. Valid operating conditions are listed in [Table 12 on page 73](#).
2. Valid clocks are described in the AC Characteristics section.
3. Ensures lock time on internal PLL.
4. The power-down has no sequencing requirements and no time limit to parameter t<sub>PDCORE2IO</sub>.
5. The VDDC (1.0V core) must be powered up at the same time or before the GP\_AVDDL (1.0V analog) supply.

## Power Supply Current

**Table 14: BCM53334 Power Supply Current for 24P 1G at 110°C Junction Temperature**

| Parameter           | Voltage (V) | Current (A) | Power (W) |
|---------------------|-------------|-------------|-----------|
| 1.0V Digital        | 1.02        | 5.64        | 5.75      |
| 1.0V Analog         | 1.02        | 0.60        | 0.61      |
| 1.2V/2.5V/3.3V MDIO | 2.55        | 0.02        | 0.05      |
| 3.3V                | 3.37        | 1.02        | 3.43      |
| Total               |             |             | 9.84      |

## Standard 3.3V Signals

The specifications shown in [Table 15](#) apply to all CMOS 3.3V general I/O signals, along with Synchronous Ethernet Interface, UART, GPIO, JTAG, and LED signals, except for BSC and MDIO/MDC.

**Table 15: Standard 3.3V Signals**

| <i>Parameter</i>          | <i>Symbol</i> | <i>Min.</i> | <i>Typ.</i> | <i>Max.</i> | <i>Units</i> |
|---------------------------|---------------|-------------|-------------|-------------|--------------|
| Input Voltage             | $V_{IN}$      | -0.25       | –           | +3.63       | V            |
| Input Low Voltage         | $V_{IL}$      | –           | –           | 0.8         | V            |
| Input High Voltage        | $V_{IH}$      | 2.0         | –           | –           | V            |
| Input Leakage Current     | $I_I$         | -15         | –           | +15         | $\mu A$      |
| Output Low Voltage        | $V_{OL}$      | –           | –           | 0.4         | V            |
| Output High Voltage       | $V_{OH}$      | VDDO33-0.4  | –           | –           | V            |
| I/O Pin Capacitance (GBD) | $C_I$         | –           | –           | TBD         | pF           |

## BSC Signals

BSC\_SCL and BSC\_SDA are bidirectional open-drain signals. An external pull-up to 3.3V should be provided on the board. BSC\_SA1 and BSC\_SA0 are standard 3.3V signals. It is recommended that they be pulled high to 3.3V or left unconnected.

**Table 16: BSC Signals<sup>a</sup>**

| Parameter                          | Symbol    | Condition               | Min.                  | Typ. | Max.                  | Units   |
|------------------------------------|-----------|-------------------------|-----------------------|------|-----------------------|---------|
| Input Voltage                      | $V_{IN}$  | –                       | –0.25                 | –    | +3.63                 | V       |
| Input Low Voltage                  | $V_{IL}$  | –                       | –                     | –    | 0.3*VDDO <sup>b</sup> | V       |
| Input High Voltage                 | $V_{IH}$  | –                       | 0.7*VDDO <sup>b</sup> | –    | –                     | V       |
| Input Leakage Current              | $I_I$     | –                       | –10                   | –    | +10                   | $\mu$ A |
| Output Low Voltage                 | $V_{OL}$  | $I_{OL} = 3 \text{ mA}$ | –                     | –    | 0.4                   | V       |
| Hysteresis of Schmitt Inputs (GBD) | $V_{HYS}$ | –                       | 0.18                  | –    | –                     | V       |
| I/O Pin Capacitance (GBD)          | $C_I$     | –                       | –                     | –    | TBD                   | pF      |

a. BSC I/Os are true open-drain type and require external pull-up resistors.

b. VDDO is 3.3V external pull-up supply.

## QSGMII SerDes Signals

**Table 17: QSGMII SerDes DC Characteristics**

| Parameter  | Symbol   | Min. | Typ. | Max. | Units    |
|--|----------|------|------|------|----------|
| <b>Receiver</b>  |          |      |      |      |          |
| RX Baud Rate   | R_Baud   | –    | 5.0  | –    | GSym/s   |
| Input Differential Voltage   | R_Vdiff  | 100  | –    | 900  | mVppd    |
| Differential Resistance  | R_Rdin   | 85   | 100  | 115  | $\Omega$ |
| Bias Voltage Source Impedance (Load Type 2)                          | R_Zvtt   | –    | –    | 30   | $\Omega$ |
| <b>Transmitter</b>   |          |      |      |      |          |
| Output Differential Voltage (into floating Load Rload=100 $\Omega$ ) | T_Vdiff  | 400  | 550  | 900  | mVppd    |
| Differential Resistance  | T_Rd     | 85   | 100  | 115  | $\Omega$ |
| Recommended Output Rise and Fall Times (20% to 80%)                  | 5 Gps    | 30   | 78   | –    | ps       |
|  | 3 Gps    | 67   | 136  | –    |          |
|  | 1.25 Gps | 100  | 200  | –    |          |

## MIIM (MDIO) Signals

**Table 18: MIIM (Clause 22 Electrical Characteristics)**

| <b>Parameter</b>          | <b>Symbol</b> | <b>Condition</b>                          | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b> | <b>Units</b> |
|---------------------------|---------------|---|-------------|-------------|-------------|--------------|
| Input Voltage             | $V_{IN}$      | –   | –0.3        | –           | +3.6        | V            |
| Input Low Voltage         | $V_{IL}$      | –   | –           | –           | 0.8         | V            |
| Input High Voltage        | $V_{IH}$      | –   | 2.0         | –           | –           | V            |
| Input Leakage Current     | $I_I$         | –   | –15         | –           | +15         | $\mu$ A      |
| Output Low Voltage        | $V_{OL}$      | $I_{OL} = 11 \text{ mA}$                  | –           | –           | 0.4         | V            |
| Output High Voltage       | $V_{OH}$      | $I_{OH} = -11 \text{ mA}$ $V_{DDO} - 0.4$ | –           | –           | –           | V            |
| I/O Pin Capacitance (GBD) | $C_I$         | –   | –           | –           | TBD         | pF           |

**Note:** GBD = Guaranteed by design are parameters that are not tested.

## AC Characteristics

### AC Timing for Reset

The SYS\_RST\_L signal is synchronized internal to the IC and, as such, asynchronous assertion and deassertion are acceptable.

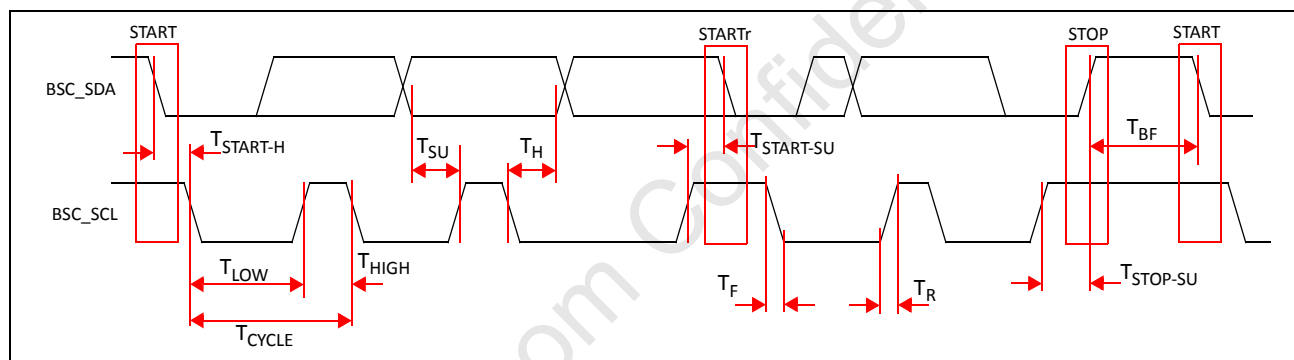
### BSC AC Characteristics

The BSC interface can be operated in two modes:

- Slave mode
- CPU-controlled master/slave mode

The external master drives BSC\_SDA during a write operation and samples BSC\_SDA during a read operation.

**Figure 13: BSC Timing Diagram**



**Table 19: BSC Master/Slave Fast-Mode Timing**

| Parameter                              | Symbol                | Min. | Typ. | Max. | Units         |
|--|-----------------------|------|------|------|---------------|
| BSC_SCL Cycle Time                     | $T_{\text{CYCLE}}$    | 2.5  | —    | —    | $\mu\text{s}$ |
| BSC_SCL Low Time                       | $T_{\text{LOW}}$      | 1.3  | —    | —    | $\mu\text{s}$ |
| BSC_SCL High Time                      | $T_{\text{HIGH}}$     | 0.6  | —    | —    | $\mu\text{s}$ |
| Data Hold Time                         | $T_{\text{H}}$        | 0    | —    | —    | $\mu\text{s}$ |
| Data Setup Time                        | $T_{\text{SU}}$       | 100  | —    | —    | ns            |
| Rise Time, Clock and Data (See Note)   | $T_{\text{R}}$        | —    | —    | 300  | ns            |
| Fall Time, Clock and Data (GBD)        | $T_{\text{F}}$        | —    | —    | 300  | ns            |
| Hold Time, START or repeated START     | $T_{\text{START-H}}$  | 0.6  | —    | —    | $\mu\text{s}$ |
| Setup Time, repeated START             | $T_{\text{START-SU}}$ | 0.6  | —    | —    | $\mu\text{s}$ |
| Setup Time, STOP                       | $T_{\text{STOP-SU}}$  | 0.6  | —    | —    | $\mu\text{s}$ |
| Bus Free Time (Between STOP and START) | $T_{\text{BF}}$       | 1.3  | —    | —    | $\mu\text{s}$ |

**Table 20: BSC Master/Slave Standard-Mode Timing**

| <b>Parameter</b>                       | <b>Symbol</b>         | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b> | <b>Units</b>  |
|--|-----------------------|-------------|-------------|-------------|---------------|
| BSC_SCL Cycle Time                     | $T_{\text{CYCLE}}$    | 2.5         | —           | —           | $\mu\text{s}$ |
| BSC_SCL Low Time                       | $T_{\text{LOW}}$      | 1.3         | —           | —           | $\mu\text{s}$ |
| BSC_SCL High Time                      | $T_{\text{HIGH}}$     | 0.6         | —           | —           | $\mu\text{s}$ |
| Data Hold Time                         | $T_{\text{H}}$        | 0           | —           | —           | $\mu\text{s}$ |
| Data Setup Time                        | $T_{\text{SU}}$       | 100         | —           | —           | ns            |
| Rise Time, Clock and Data (See Note)   | $T_{\text{R}}$        | —           | —           | 300         | ns            |
| Fall Time, Clock and Data (GBD)        | $T_{\text{F}}$        | —           | —           | 300         | ns            |
| Hold Time, START or repeated START     | $T_{\text{START-H}}$  | 0.6         | —           | —           | $\mu\text{s}$ |
| Setup Time, repeated START             | $T_{\text{START-SU}}$ | 0.6         | —           | —           | $\mu\text{s}$ |
| Setup Time, STOP                       | $T_{\text{STOP-SU}}$  | 0.6         | —           | —           | $\mu\text{s}$ |
| Bus Free Time (Between STOP and START) | $T_{\text{BF}}$       | 1.3         | —           | —           | $\mu\text{s}$ |



**Note:** BSC\_SCL and BSC\_SDA are open-drain outputs. The rise time is dependent on the strength of the external pull-up resistor, which should be chosen to meet the rise time requirement.

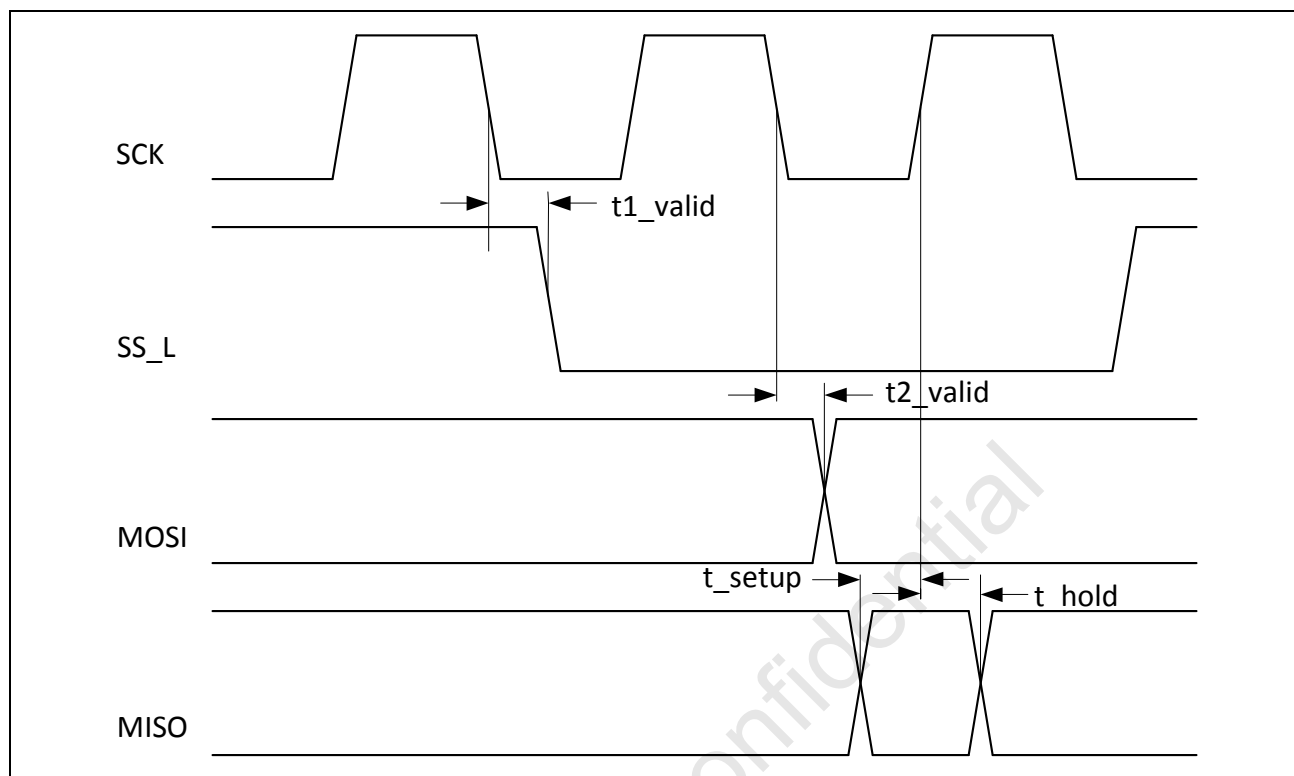
The BCM53334 device drives the BSC\_SCL clock, with a programmable speed of 100 kHz or 400 kHz based on the mode bit called MODE\_400. The BCM53334 drives BSC\_SDA during a write operation and samples BSC\_SDA during a read operation.

## SPI AC Characteristics

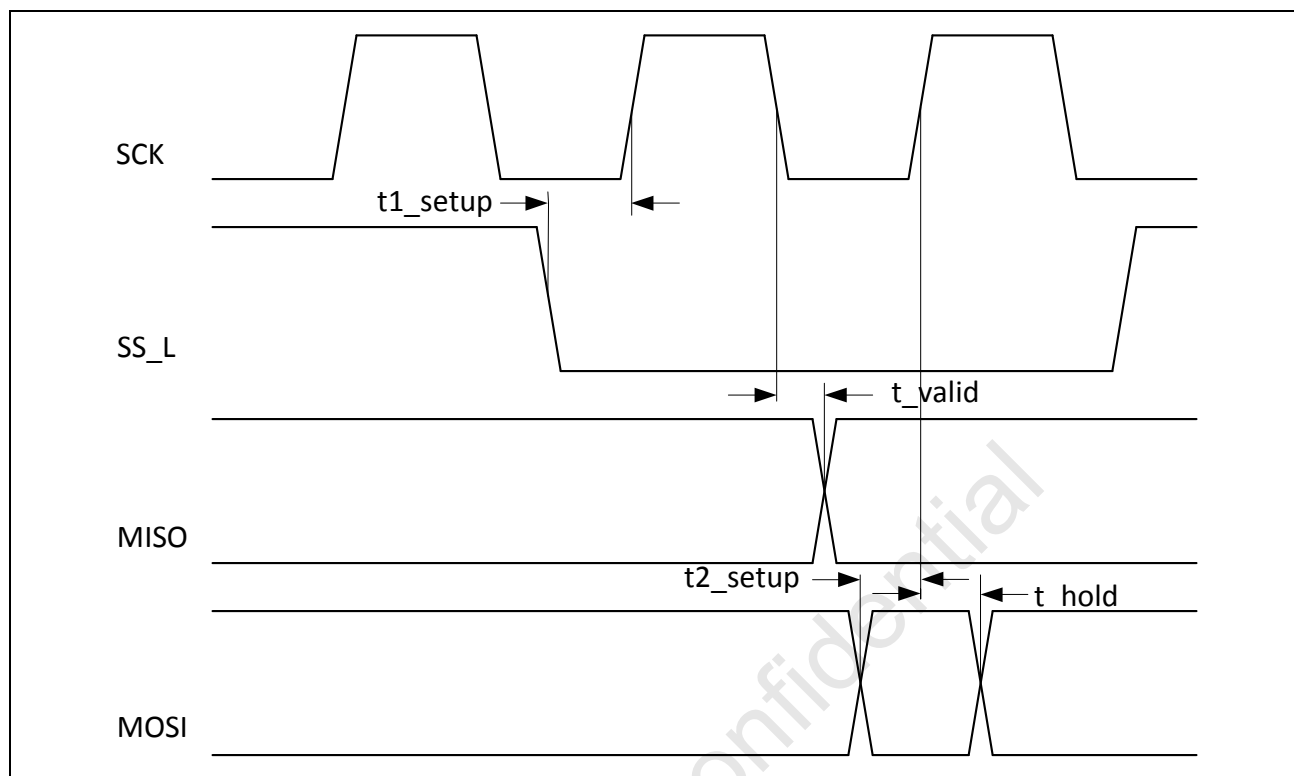
The SPI interface can be operated in two modes:

- Master mode
- Slave mode



**Figure 14: SPI Interface Master Mode Timing Diagram****Table 21: SPI Master Mode Timing**

| Parameter       | Symbol      | Min. | Typ. | Max. | Units |
|-----------------|-------------|------|------|------|-------|
| SCK Cycle Time  | $T_{CYCLE}$ | 32   | –    | –    | ns    |
| SS_L Valid Time | $t1\_valid$ | 5    | –    | –    | ns    |
| MOSI Valid Time | $t2\_valid$ | 5    | –    | –    | ns    |
| MISO Setup Time | $t\_setup$  | 5    | –    | –    | ns    |
| MISO Hold Time  | $t\_hold$   | 0    | –    | –    | ns    |

**Figure 15: SPI Interface Slave Mode Timing Diagram****Table 22: SPI Slave Fast Mode Timing**

| Parameter       | Symbol             | Min. | Typ. | Max. | Units |
|-----------------|--------------------|------|------|------|-------|
| SCK Cycle Time  | T <sub>CYCLE</sub> | 32   | –    | –    | ns    |
| SS_L Setup Time | t1_setup           | 4    | –    | –    | ns    |
| MOSI Setup Time | t2_setup           | 4    | –    | –    | ns    |
| MOSI Hold Time  | t_hold             | 4    | –    | –    | ns    |
| MISO Valid Time | t_val              | 9    | –    | –    | ns    |

## MDIO AC Characteristics

Figure 16: MIIM Interface Timing Diagram

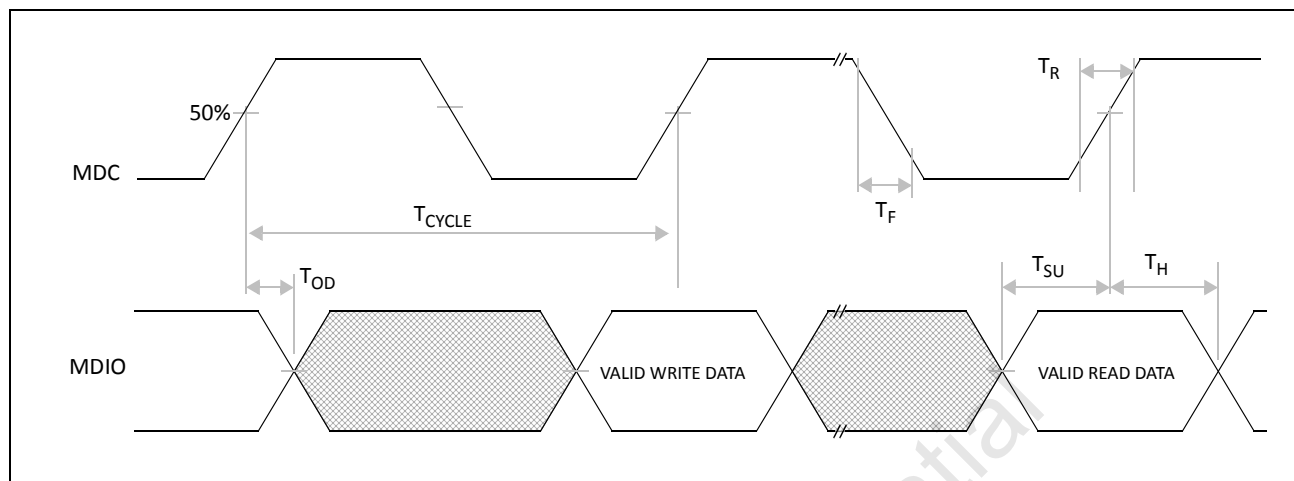


Table 23: MDC/MDIO Timing

| Parameter                                | Symbol                       | Min. | Typ. | Max. | Units |
|--|------------------------------|------|------|------|-------|
| MDC Cycle Time                           | $T_{\text{CYCLE}}$           | 80   | 400  | –    | ns    |
| MDC Duty Cycle                           | –                            | 40   | –    | 60   | %     |
| MDC Rise/Fall Time (Requirement 20%–80%) | $T_{\text{R}}, T_{\text{F}}$ | –    | –    | 10   | ns    |
| MDIO Setup Time                          | $T_{\text{S}}$               | 20   | –    | –    | ns    |
| MDIO Hold Time                           | $T_{\text{H}}$               | 10   | –    | –    | ns    |
| MDIO Output Delay                        | $T_{\text{OD}}$              | 0    | –    | 25   | ns    |

## JTAG AC Specifications

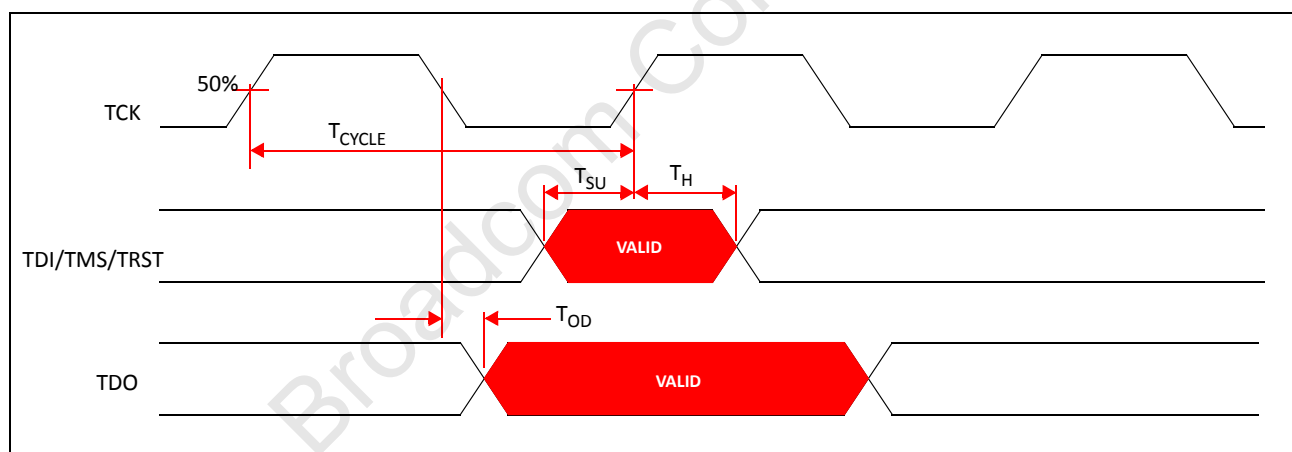
**Table 24: AC Characteristics for JTAG**

| Parameter   | Symbol                | Min. | Typ. | Max. | Unit |
|---|-----------------------|------|------|------|------|
| j_tck cycle time  | $t_{\text{CYCLE}}$    | 80.0 | –    | –    | ns   |
| j_tck falling edge to output valid.<br>Applicable to j_tdo.           | $t_{\text{OD}}$       | 0    | –    | 25   | ns   |
| Data input setup time before j_tck.<br>Applicable to j_tdi and j_tms. | $t_{\text{SU\_JT}}$   | 15   | –    | –    | ns   |
| Data hold time after j_tck rise<br>Applicable to j_tdi and j_tms.     | $t_{\text{H\_JT}}$    | 5    | –    | –    | ns   |
| Input setup time before j_tck rising edge.<br>Applicable to j_trst.   | $t_{\text{SU\_JTRS}}$ | 15   | –    | –    | ns   |
| Input hold time after j_tck rising edge.<br>Applicable to j_trst.     | $t_{\text{H\_JTRS}}$  | 5    | –    | –    | ns   |

**Note:** Unless otherwise noted, the specifications are valid across the following operating conditions:

- The threshold value is at 50% of the applicable I/O rail voltage.
- The default loading on an output is 5 pF.

**Figure 17: JTAG Timing**



## QSPI Flash Interface Timing

The QSPI interface operates as a Master, allowing access to an external SPI Flash or EEPROM from which the microcontroller boot code can be loaded. The SFLASH\_CLK, SFLASH\_CS\_L and SFLASH\_IO0 signals are outputs, while SFLASH\_IO1 is an input.

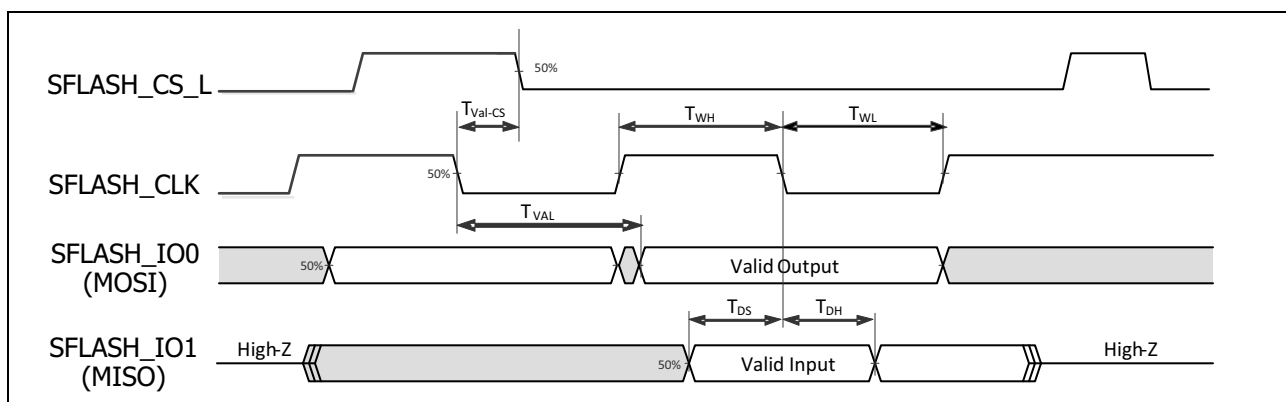


Figure 18: QSPI BSPI Mode Master Interface Timing



**Note:** Figure 18 BSPI Mode only shows single lane operation. SFLASH\_IO2 and SFLASH\_IO3 signals are used to support dual-lane and quad-lane operation.

Table 25: QSPI BSPI Mode Master Interface Timing Specifications

| Parameters                            | Symbol       | Conditions | Min.               | Typ.        | Max.               | Unit |
|---------------------------------------|--------------|------------|--------------------|-------------|--------------------|------|
| SFLASH Clock Frequency <sup>a</sup>   | $F_{CLK}$    | —          | —                  | 62.5        | 62.5               | MHz  |
| SFLASH Clock Cycle Time               | $T_{CK}$     | —          | —                  | $1/F_{CLK}$ | —                  | ns   |
| SFLASH_CLK Clock High time            | $T_{WH}$     | —          | $0.4 \cdot T_{CK}$ | —           | $0.6 \cdot T_{CK}$ | ns   |
| SFLASH_CLK Clock Low time             | $T_{WL}$     | —          | $0.4 \cdot T_{CK}$ | —           | $0.6 \cdot T_{CK}$ | ns   |
| Chip Select (SFLASH_CS_L) Valid time  | $T_{Val-CS}$ | —          | 0                  | —           | 4.0                | ns   |
| Data Out MOSI (SFLASH_IO0) Valid time | $T_{Val}$    | —          | –3.0               | —           | 4.0                | ns   |
| Data In MISO (SFLASH_IO1) Setup time  | $T_{DS}$     | —          | 4.0                | —           | —                  | ns   |
| Data In MISO (SFLASH_IO1) Hold time   | $T_{DH}$     | —          | 1.0                | —           | —                  | ns   |
| Rise Time                             | $T_R$        | 20% to 80% | —                  | —           | 1.5                | ns   |
| Fall Time                             | $T_F$        | 20% to 80% | —                  | —           | 1.5                | ns   |

- a. QSPI BSPI mode is used for initial code download when IP\_BOOT\_DEV=3'b000 and read operations during runtime. The frequency is set to a reset default value of 25 MHz through CRU\_CONTROL.QSPI\_CLK\_SEL. When register access is established, the same register can be written to change the QSPI interface frequency to a value of 25 MHz, 31.25 MHz, 50 MHz, or 62.5 MHz.

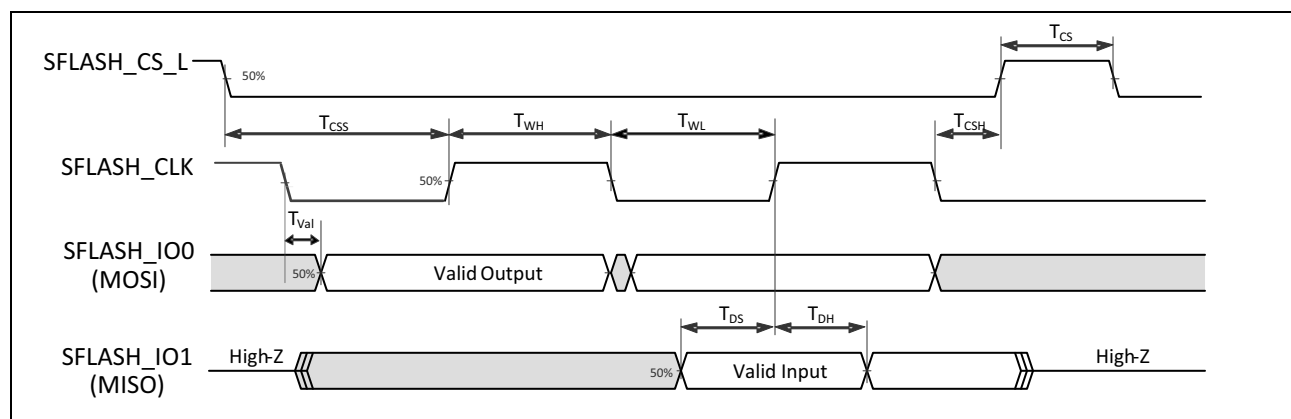


Figure 19: QSPI MSPI Mode Master Interface Timing

Table 26: QSPI MSPI Mode Master Interface Timing Specifications

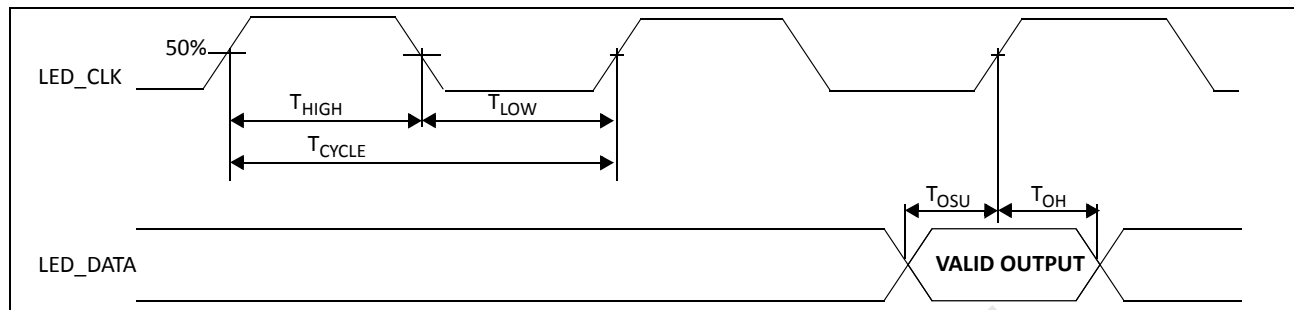
| Parameters                            | Symbol    | Conditions | Min.               | Typ.        | Max.               | Unit |
|---------------------------------------|-----------|------------|--------------------|-------------|--------------------|------|
| SFLASH Clock Frequency <sup>a</sup>   | $F_{CLK}$ | —          | —                  | 15.625      | 15.625             | MHz  |
| SFLASH Clock Cycle Time               | $T_{CK}$  | —          | —                  | $1/F_{CLK}$ | —                  | ns   |
| SFLASH_CLK Clock High time            | $T_{WH}$  | —          | $0.4 \cdot T_{CK}$ | —           | $0.6 \cdot T_{CK}$ | ns   |
| SFLASH_CLK Clock Low time             | $T_{WL}$  | —          | $0.4 \cdot T_{CK}$ | —           | $0.6 \cdot T_{CK}$ | ns   |
| Chip Select (SFLASH_CS_L) Setup time  | $T_{CSS}$ | —          | 12.0               | —           | —                  | ns   |
| Chip Select (SFLASH_CS_L) Hold time   | $T_{CSH}$ | —          | 1.0                | —           | —                  | ns   |
| Data Out MOSI (SFLASH_IO0) Valid time | $T_{Val}$ | —          | 0                  | —           | 4.0                | ns   |
| Data In MISO (SFLASH_IO1) Setup time  | $T_{DS}$  | —          | 12.0               | —           | —                  | ns   |
| Data In MISO (SFLASH_IO1) Hold time   | $T_{DH}$  | —          | 1.0                | —           | —                  | ns   |
| Rise Time                             | $T_R$     | 20% to 80% | —                  | —           | 1.5                | ns   |
| Fall Time                             | $T_F$     | 20% to 80% | —                  | —           | 1.5                | ns   |

a. QSPI MSPI mode is typically used during runtime whenever write or erase operations are required.

## LED Controller Interface

LED\_CLK and LED\_DATA are outputs. LED\_CLK output clock period is 200 ns (5.0 MHz).

**Figure 20: LED Timing Diagram**



**Table 27: LED Timing<sup>a</sup>**

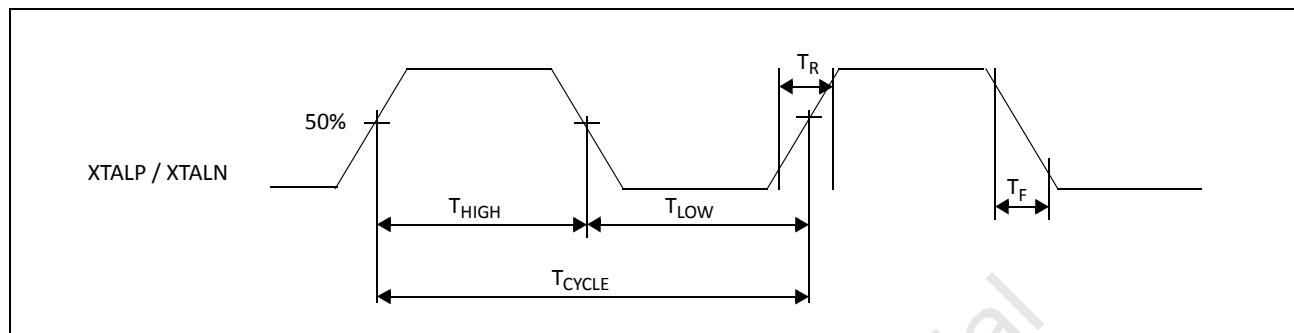
| Parameter                  | Symbol      | Min. | Typ. | Max. | Units |
|----------------------------|-------------|------|------|------|-------|
| LED_CLK Cycle Time         | $T_{CYCLE}$ | —    | 200  | 200  | ns    |
| LED_CLK High Time          | $T_{HIGH}$  | 70   | 100  | 130  | ns    |
| LED_CLK Low Time           | $T_{LOW}$   | 70   | 100  | 130  | ns    |
| LED_DATA Output Valid Time | $T_{OV}$    | 0    | —    | 30   | ns    |

a. Timing figures are specified at the 50% crossing thresholds.

## XTAL Clock Requirements

The Master clock (XTALP/XTALN), when driven by an external oscillator, requires a 25 MHz single-ended or differential source with characteristics shown in Figure 21 and meets requirements outlined in Table 28.

**Figure 21: XTALP/XTALN Input Timing Diagram**



**Table 28: XTALP/XTALN Input Requirements**

| Requirement                                     | Symbol                          | Min. | Typ. | Max. | Units     |
|---|---------------------------------|------|------|------|-----------|
| XTALP/XTALN Frequency                           | —                               | —    | 25   | —    | MHz       |
| XTALP/XTALN Accuracy                            | —                               | −50  | —    | +50  | ppm       |
| XTALP/XTALN Duty Cycle                          | —                               | 45   | —    | 55   | %         |
| Input Voltage Range                             | V <sub>IN</sub>                 | 800  | —    | 2000 | mVpp diff |
| Minimum Input Voltage                           | V <sub>IL</sub>                 | 0    | —    | —    | V         |
| Maximum Input Voltage                           | V <sub>IH</sub>                 | —    | —    | 1.0  | VDC       |
| XTALP/XTALN Rise/Fall Time (20% to 80%)         | T <sub>R</sub> , T <sub>F</sub> | 0.10 | —    | 1.0  | ns        |
| XTALP/XTALN Jitter RMS Max (12 kHz to 12.5 MHz) | —                               | —    | —    | 0.5  | ps        |

**Note:**

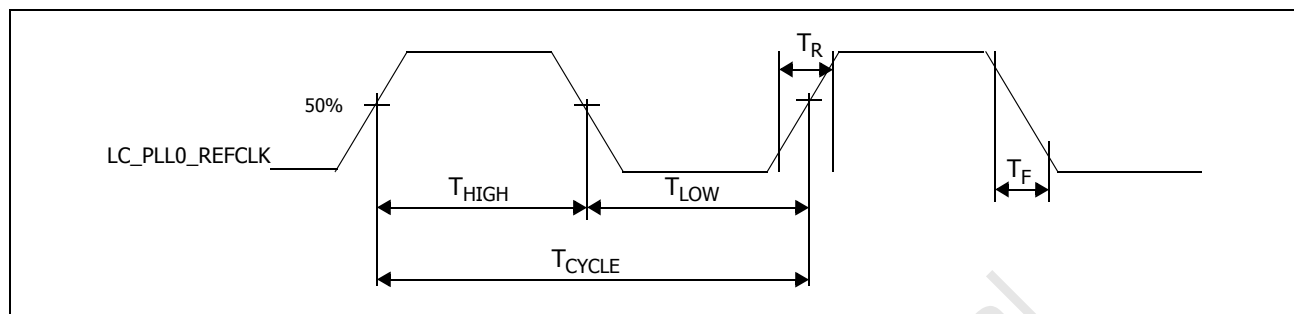
- Sample part Vectron VCC6-QAB-25M00 LVPECL Crystal Oscillator.
- AC-coupled externally.
- External 100Ω termination required.



## LC\_PLL0\_REFCLK Clock Requirements

The QSGMII/QGPHY clock (LC\_PLL0\_REFCLKP/N) requires a 25 MHz differential source with characteristics shown in Figure 22.

**Figure 22: LC\_PLL0\_REFCLKP/N Input Timing Diagram**



**Table 29: LC\_PLL0\_REFCLK Input Requirements**

| Requirement   | Symbol                          | Min. | Typ. | Max. | Units     |
|---|---------------------------------|------|------|------|-----------|
| LC_PLL0_REFCLK Frequency                                    | —                               | —    | 25   | —    | MHz       |
| LC_PLL0_REFCLK Accuracy                                     | —                               | -50  | —    | +50  | ppm       |
| LC_PLL0_REFCLK Duty Cycle                                   | —                               | 45   | —    | 55   | %         |
| Input Voltage Range   | V <sub>IN</sub>                 | 700  | —    | 2000 | mVpp diff |
| LC_PLL0_REFCLK Rise/Fall Time (20% to 80%)                  | T <sub>R</sub> , T <sub>F</sub> | 0.10 | —    | 1.0  | ns        |
| LC_PLL0_REFCLK (25 MHz) Jitter RMS Max (12 kHz to 12.5 MHz) | —                               | —    | —    | 0.5  | ps        |

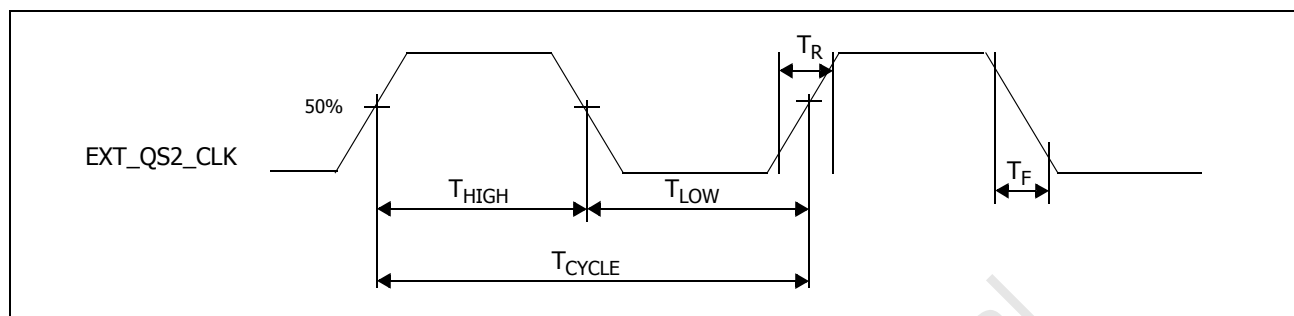
**Note:**

- AC-coupled externally.
- Internal 100 $\Omega$  termination.

## EXT\_QS2\_CLKP/N Clock Specifications

These clocks (EXT\_QS2\_CLKP/N) provide a 125 MHz differential clocks that can be directly connecting to external GPHY such as Broadcom BCM54282.

**Figure 23: EXT\_QS2\_CLKP/N Output Timing Diagram**



**Table 30: EXT\_QS2\_CLKP/N Output Specifications**

| Requirement                                     | Symbol      | Min. | Typ. | Max. | Units     |
|---|-------------|------|------|------|-----------|
| EXT_QS2_CLK Frequency                           | –           | –    | 125  | –    | MHz       |
| EXT_QS2_CLK Accuracy                            | –           | –50  | –    | +50  | ppm       |
| EXT_QS2_CLK Duty Cycle                          | –           | 45   | –    | 55   | %         |
| Output Voltage Range                            | $V_{ODIFF}$ | 300  | –    | 500  | mVpp diff |
| EXT_QS2_CLK Rise/Fall Time (20% to 80%)         | $T_R, T_F$  | 0.10 | –    | 0.22 | ns        |
| EXT_QS2_CLK Jitter RMS Max (12 kHz to 12.5 MHz) | –           | –    | –    | 2    | ps        |

**Note:**

- AC-coupled externally.
- Measured with 50Ω termination as recommended in the Hardware Design Guide.

## QSGMII AC Specifications

### Transmitter

Figure 24: QSGMII Transmit Eye Mask

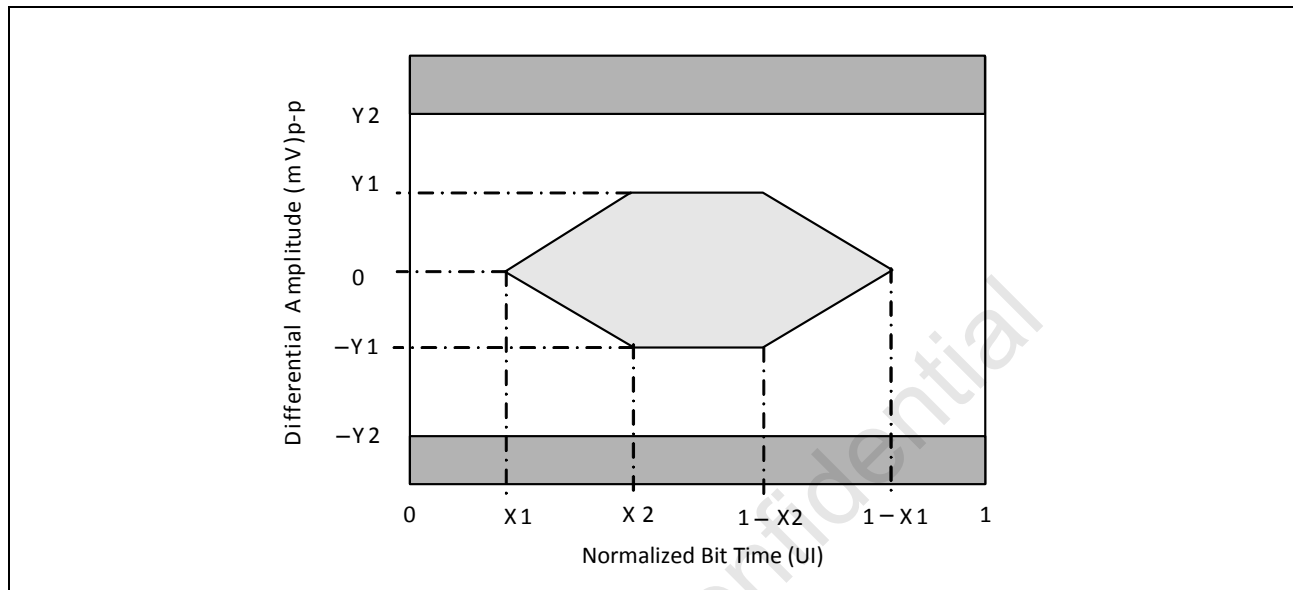


Table 31: QSGMII TX

| Parameters                            | Symbol                | Min.     | Typ. | Max.     | Units            |
|---------------------------------------|-----------------------|----------|------|----------|------------------|
| Output Speed per lane                 | –                     | –100 ppm | +5.0 | +100 ppm | Gbaud            |
| Differential Resistance               | Rin                   | 80       | 100  | 120      | $\Omega$         |
| Differential Output Voltage (pk-pk)   | VOD                   | 400      | –    | 900      | mVp-p            |
| Transmit Eye Mask (Figure 24)         | X1                    | –        | –    | 0.15     | UI               |
| Transmit Eye Mask (Figure 24)         | X2                    | –        | –    | 0.40     | UI               |
| Transmit Eye Mask (Figure 24)         | Y1                    | 200      | –    | –        | mV               |
| Transmit Eye Mask (Figure 24)         | Y2                    | –        | –    | 450      | mV               |
| Common Mode Voltage                   | VCM                   | 550      | –    | 1060     | mV               |
| Differential Output Return Loss (min) | Equation <sup>a</sup> | –        | –    | –8       | dB               |
| Common-mode Output Return Loss (min)  | Equation <sup>b</sup> | –        | –    | –6       | dB               |
| Output Rise Time (20%–80%)            | Tr                    | 30       | –    | –        | pS               |
| Output Fall Time (20%–80%)            | Tf                    | 30       | –    | –        | pS               |
| Output Jitter @ $1e^{-12}$ BER        |                       |          |      |          |                  |
| Uncorrelated                          | sut                   | –        | –    | 0.15     | U <sub>lpp</sub> |
| Total                                 | st                    | –        | –    | 0.30     | U <sub>lpp</sub> |

a. Return Loss ( $f$ ) –8 dB for  $100 \text{ MHz} \leq f < 2.5 \text{ GHz}$

Return Loss ( $f$ )  $\leq [-8 + 16.6 \log(f/2.5)] \text{ dB}$  for  $2.5 \text{ GHz} \leq f \leq 5 \text{ GHz}$ , where  $f$  is in Gigahertz.

b. Return Loss ( $f$ )  $\leq -6 \text{ dB}$  for  $100 \text{ MHz} \leq f < 2.5 \text{ GHz}$

## Receiver

Figure 25: QSGMII Receive Eye Mask

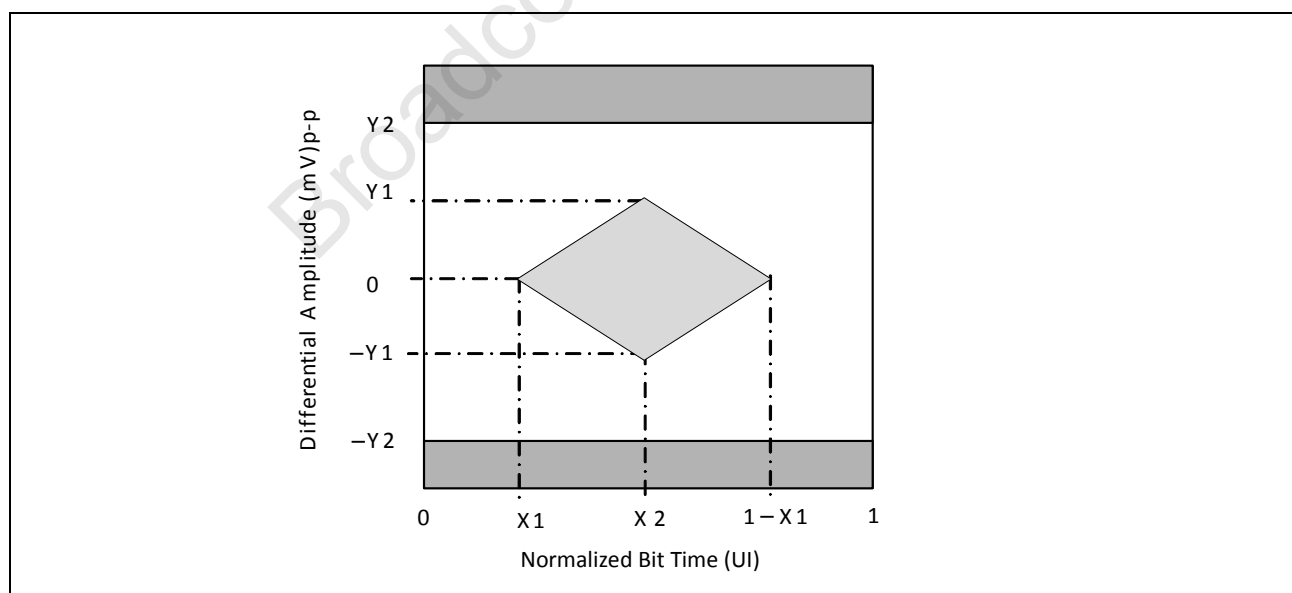
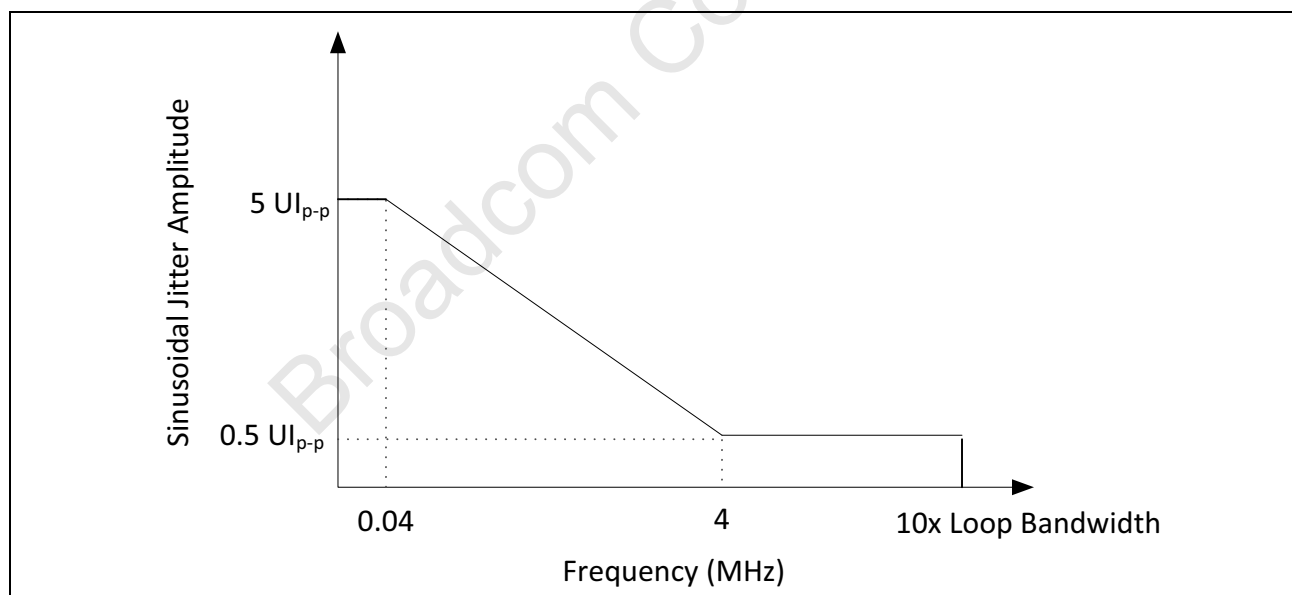


Table 32: QSGMII RX

| Parameters  | Symbol                | Min.     | Typ. | Max.     | Units         |
|---|-----------------------|----------|------|----------|---------------|
| Receiver coupling   | AC                    | —        | 0.1  | —        | $\mu\text{F}$ |
| Differential Resistance   | Rin                   | 80       | 100  | 120      | $\Omega$      |
| Receive eye mask (Figure 25 on page 92)                                     | X1                    | —        | —    | 0.30     | UI            |
| Receive eye mask (Figure 25 on page 92)                                     | X2                    | —        | —    | 0.5      | UI            |
| Receive eye mask (Figure 25 on page 92)                                     | Y1                    | 50       | —    | —        | mV            |
| Receive eye mask (Figure 25 on page 92)                                     | Y2                    | —        | —    | 450      | mV            |
| Differential input return loss  | Equation <sup>a</sup> | —        | —    | −8       | dB            |
| Common mode input return loss   | Equation <sup>b</sup> | —        | —    | −6       | dB            |
| Receiving speed per lane  | —                     | −100 ppm | +5.0 | +100 ppm | Gbaud         |
| Sinusoidal jitter tolerance   | Figure 26 on page 93  | —        | —    | 0.05     | UIpp          |
| Bit error rate based channel characteristics per Clause 83A in IEEE802.3ba. | —                     | —        | —    | 1e-12    | bps           |

- a. Return loss ( $f$ )  $\leq -8$  dB for  $100 \text{ MHz} \leq f < 2.5 \text{ GHz}$ .  
 Return loss  $\leq [-8 + 16.6\log(f/2.5)]\text{dB}$  for  $2.5 \text{ GHz} \leq f \leq 5 \text{ GHz}$ , where  $f$  is in Gigahertz.
- b. Return loss ( $f$ )  $\leq -6$  dB for  $100 \text{ MHz} \leq f < 2.5 \text{ GHz}$ , where  $f$  is in Gigahertz.

Figure 26: Single-Tone Sinusoidal Jitter Mask



## AC-JTAG

The serial interface AC-JTAG characteristics are shown in Table 33.

**Table 33: Serial Interface AC-JTAG Characteristics**

| Parameter                          | Symbol           | Description      | Min. | Typ. | Max.                 | Unit |
|------------------------------------|------------------|------------------|------|------|----------------------|------|
| Fault Resistance Detect            | R <sub>sc</sub>  | Short Circuit    | 0    | –    | 5                    | Ω    |
|                                    | R <sub>oc</sub>  | Open Circuit     | 20   | –    | –                    | kΩ   |
| Transmit Voltage Levels            | V <sub>TX</sub>  | Differential p-p | 0.5  | 1.0  | 1.3                  | V    |
| Transmit Data Rate                 | –                | EXTEST_TRAIN     | 1    | –    | 30                   | Mbps |
| Output Resistance                  | R <sub>DRV</sub> | DP or DM to VDD  | –    | 50   | –                    | Ω    |
| Transmit Supply Current            | I <sub>DD</sub>  | Operating mode   | –    | 56   | –                    | mA   |
| Receiver Input Capacitance         | C <sub>IN</sub>  | DP or DM to GND  | –    | 0.5  | 0.6                  | pF   |
| Common-Mode Voltage                | V <sub>CM</sub>  | –                | –    | –    | V <sub>DD</sub> –0.2 | V    |
| Comparator Hysteresis <sup>a</sup> | V <sub>HYS</sub> | Peak-to-peak     | 25   | 150  | 300                  | mV   |
| Receive Data Rate                  | –                | EXTEST_TRAIN     | 1    | –    | 30                   | Mbps |

a. Transmit voltage levels, as well as receiver hysteresis, are user programmable.

Table 34 and Table 35 show the AC-JTAG settings and the corresponding typical voltages.

**Table 34: AC-JTAG Transmit Setting (Driver Bias Current)**

| Cfg Value | Transmit Amplitude [Vpp] | Cfg Value | Transmit Amplitude [Vpp] |
|-----------|--------------------------|-----------|--------------------------|
| 0111      | 0.68                     | 1111      | 1.04                     |
| 0110      | 0.73                     | 1110      | 1.06                     |
| 0101      | 0.78                     | 1101      | 1.07                     |
| 0100      | 0.83                     | 1100      | 1.08                     |
| 0011      | 0.88                     | 1011      | 1.08                     |
| 0010      | 0.93                     | 1010      | 1.09                     |
| 0001      | 0.98                     | 1001      | 1.09                     |
| 0000      | 1.01                     | 1000      | 1.10                     |

**Table 35: AC-JTAG Receive Configuration**

| Cfg Value | Rx Hysteresis (mVpp) | Cfg Value | Rx Hysteresis (mVpp) |
|-----------|----------------------|-----------|----------------------|
| 111       | 130                  | 011       | 0                    |
| 110       | 100                  | 010       | 300                  |
| 101       | 70                   | 001       | 230                  |
| 100       | 40                   | 000       | 170                  |

## Section 9: Thermal Characteristics

Table 36 shows the thermal characteristics of BCM53334 in 24x 1G configuration at  $T_A=40^{\circ}\text{C}$  with 50 x 50 x 30 mm<sup>3</sup> heatsink.

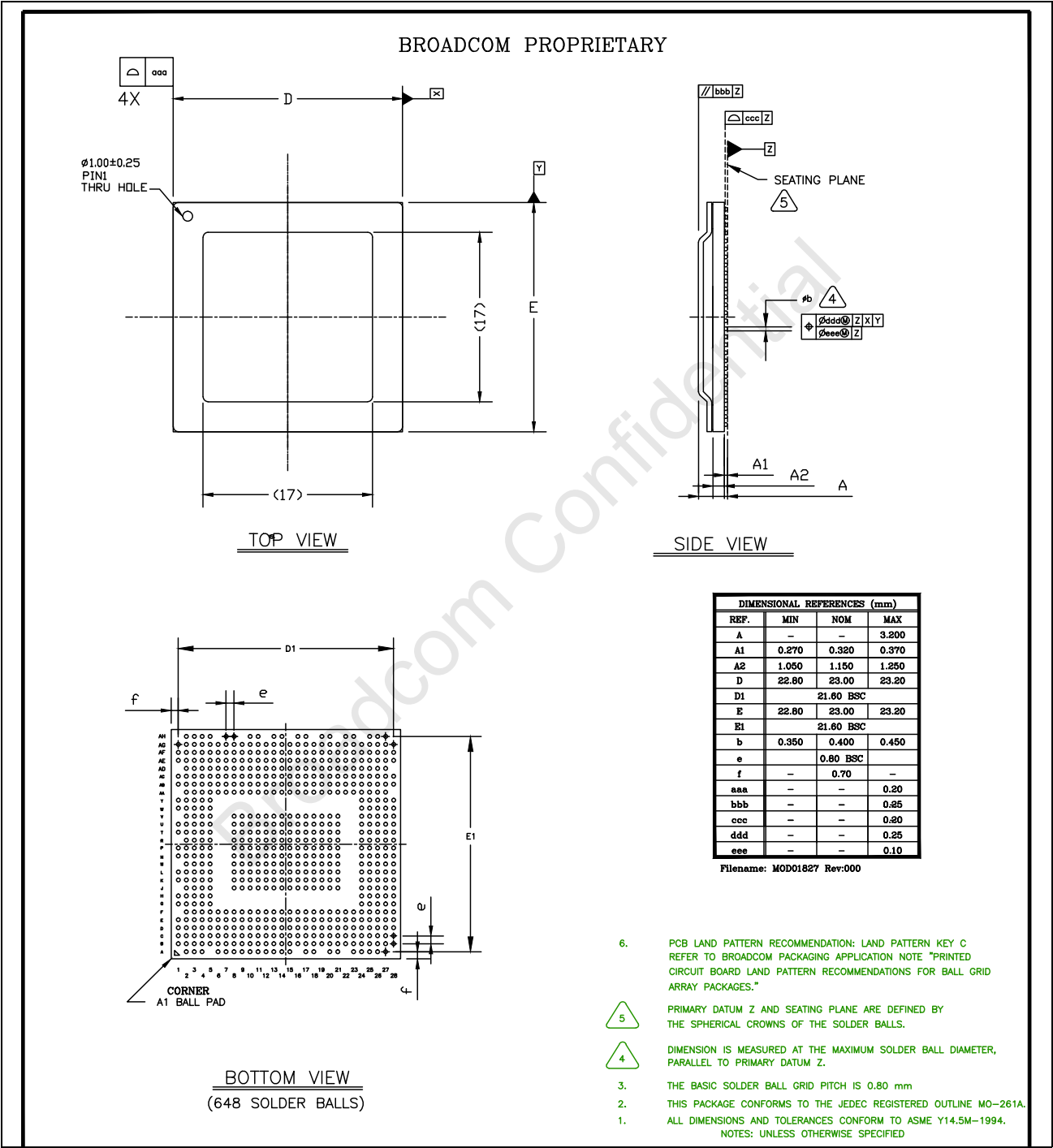
**Table 36: 648-FCBGA+HS Thermal Characteristics with 50 x 50 x 35 mm<sup>3</sup> External Heat Sink at  $T_A = 40^{\circ}\text{C}$ ,  $P = 9.84\text{W}$**

| <b>Air Flow (LFPM)</b>   | <b>0</b> | <b>100</b> | <b>200</b> | <b>400</b> | <b>600</b> |
|--|----------|------------|------------|------------|------------|
| Theta-JA ( $^{\circ}\text{C/W}$ )                                      | 6.00     | 3.27       | 2.49       | 2.16       | 2.06       |
| Theta-JB ( $^{\circ}\text{C/W}$ )                                      | 3.25     | —          | —          | —          | —          |
| Theta-JC ( $^{\circ}\text{C/W}$ )                                      | 0.85     | —          | —          | —          | —          |
| Maximum Junction Temperature $T_J$ ( $^{\circ}\text{C}$ ) <sup>a</sup> | 99.07    | 72.19      | 64.51      | 61.26      | 60.28      |
| Heatsink: 50 mm x 50 mm x 30 mm  |          |            |            |            |            |

a. Steady state junction temperature should not exceed 110  $^{\circ}\text{C}$ .

Section 10: Mechanical Information

Figure 27: 23 mm x 23 mm Package





## Section 11: Ordering Information

**Table 37: Ordering Information for RoHS6 Devices (Contact Broadcom for Availability)**

| <b>Part Number</b> | <b>Package</b>                                    | <b>Ambient Temperature</b> |
|--------------------|---|----------------------------|
| BCM53334A0KFSBLG   | 648-pin FCBGA +HS (23 mm x 23 mm) RoHS6 Compliant | 0°C to 70°C                |
| BCM53334A0IFSBLG   | 648-pin FCBGA +HS (23 mm x 23 mm) RoHS6 Compliant | –40°C to 85°C              |

**Table 38: Ordering Information for RoHS6 Devices with Exemption 15 (Eutectic Bumps Internally Between Die and Substrate)**

| <b>Part Number</b> | <b>Package</b>                    | <b>Ambient Temperature</b> |
|--------------------|-----------------------------------|----------------------------|
| BCM53334A0KFSBG    | 648-pin FCBGA +HS (23 mm x 23 mm) | 0°C to 70°C                |
| BCM53334A0IFSBG    | 648-pin FCBGA +HS (23 mm x 23 mm) | –40°C to 85°C              |

# Appendix A: Acronyms and Abbreviations

For a more complete list of acronyms and other terms used in Broadcom documents, go to: <http://www.broadcom.com/press/glossary.php>.

| <b>Term</b> | <b>Description/Usage</b>   |
|-------------|--|
| ACA         | Accessory Charger Adapter  |
| ACI         | Adjacent Channel Interference  |
| ACL         | Access Control Logic   |
| ACP         | Accelerator Coherency Port   |
| AH          | Authentication   |
| AHB         | Advanced High Performance Bus  |
| ALU         | Arithmetic and Logic Unit<br>1. The unit of a computing system that contains the circuits that perform arithmetic operations.<br>2. A functional component of a computer system that performs arithmetic operations. See <i>vector unit</i> and <i>scalar unit</i> . |
| AOPC        | Always-On Power Controller   |
| APB         | Advanced Peripheral Bus  |
| AS          | 1. Autonomous System (ATM)<br>2. access stratum (3GPP)   |
| ATB         | Advanced Trace Bus   |
| AUTN        | authentication token (3GPP)  |
| AXI         | Advanced eXtensible Interface  |
| BB          | Baseband. ( <i>Bluetooth</i> )   |
| BBC         | backup battery charger   |
| BCCH        | Broadcast Control Channel  |
| BER         | Bit Error Rate   |
| BIF         | Battery Interface (MIPI Alliance)  |
| BMC         | Best Master Clock  |
| BPS         | Bits-Per-Second  |
| BSC         | Broadcom Serial Control: A proprietary Broadcom bus or interface that is compatible with the Philips® I <sup>2</sup> C bus or interface.   |
| CC          | 1. Call Control. ( <i>Bluetooth</i> )<br>2. Constant Current   |
| CCBS        | Completion of Calls to Busy Subscribers or Call Completion on Busy Subscriber  |
| CCI         | Camera Control Interface   |
| CCP         | Compact Camera Port  |
| CCP2        | Compact Camera Port 2 -  |
| CCU         | Clock Control Unit   |
| CDP         | 1. compact display port<br>2. Charging Downstream Port   |

| <b>Term</b> | <b>Description/Usage</b>  |
|-------------|---|
| CFP         | Compact Field Processor   |
| CM          | 1. configuration management: The detailed recording and updating of information that describes an enterprise's computer systems and networks, including all hardware and software components.<br>2. congestion management<br>3. Connection Manager or Connection Management |
| CML         | Common Mode Logic   |
| CMSP        | Content Management Service Provider   |
| CoS         | Class-of-Service  |
| CPE         | Customer Premise Equipment  |
| CSI         | Camera Serial Interface   |
| CSI2        | Camera Serial Interface 2 - 02/18/10  |
| CSR         | 1. Control and Status Register<br>2. core switching regulator   |
| CTI         | cross trigger interface   |
| CTM         | Cross Trigger Matrix  |
| CV          | 1. Credential Vault<br>2. Constant Voltage  |
| DA          | Destination Address   |
| DAP         | Debug Access Port   |
| DBI         | Display Bus Interface   |
| DCP         | Dedicated Charging Port   |
| DCXO        | Digitally Compensated Crystal Oscillator  |
| DF          | Don't Fragment  |
| DigRF       | Baseband/RF Digital interface specification   |
| DLL         | Data Link Layer   |
| DLLP        | Data Link Layer Packet  |
| DMU         | Device Management Unit  |
| DoS         | Denial of Service   |
| DPI         | Display Pixel Interface   |
| DRM         | 1. Digital Rights Management<br>2. Digital Restrictions Management  |
| DSI         | 1. Display Stream Interface: A high-speed serial interface for LCD modules.<br>2. Display Serial Interface  |
| DT          | Double Tag  |
| DTE         | Digital Timing Engine   |
| DVFS        | Dynamic Voltage and Frequency Scaling   |
| DVS         | Dynamic Voltage Scaling   |
| EAPOL       | Extensible Authentication Protocol over LAN   |
| ECC         | Error-Correction Code   |
| ECRC        | End-to-end CRC  |
| ENS         | Enhanced Network Selection (GPS)  |

| <b>Term</b>      | <b>Description/Usage</b>   |
|------------------|--|
| ESP              | Encapsulating Security Payload   |
| ETB              | Embedded Trace Buffer  |
| ETM              | Embedded Trace Macrocell (ARM Microprocessors)   |
| EVM              | Error Vector Magnitude   |
| FG               | fuel gauge   |
| GIC              | General Interrupt Controller   |
| GMM              | GPRS Mobility Management   |
| GPRS             | General Packet Radio Service: A standard for wireless communications that run at speeds of up to 171 Kbps, compared with GSM systems, which run at 9.6 Kbps. GPRS, which supports a wide range of bandwidths, is an efficient use of limited bandwidth particularly suited for sending and receiving small bursts of data, such as for e-mail and Web browsing, as well as large volumes of data.  |
| GSM              | Global System for Mobile Communications: A second generation digital cellular technology developed by European countries in the 1980s to facilitate pan-European roaming. GSM uses time division multiple access technology and operates at both cellular and PCS frequencies (900 MHz, 1800 MHz, 1900 MHz). Other technologies used are CDMA, PDC & TDMA. In 1999, 66% of the world's cell phones were GSM (source: EMC World Cellular Database). |
| HOSTON           | PMU state is on  |
| HPLMN            | Home Public Land Mobile Network  |
| HSDPA            | High-Speed Downlink Packet Access  |
| HSUPA            | High-Speed Upload Packet Access  |
| HVS              | Hardware Video Scaler  |
| I <sup>2</sup> S | 1. Inter-IC Sound<br>2. Integrated Interchip Sound<br>3. Internet Information Server ( <i>Microsoft</i> )<br>Electrical serial bus interface standard for connecting digital audio devices. Up to 16 audio channels at up to 192 kHz.  |
| IDT              | Intelligent Double Tag   |
| IF               | 1. interface<br>2. Intermediate Frequency: A frequency below Radio Frequency (RF). In a GPS receiver, the RF chip converts the analog RF signal to IF and then converts it to a digital signal that is processed by the baseband device.   |
| IHL              | Internet Header Length   |
| IMSI             | International Mobile Subscriber Identity   |
| IOSR             | Input/Output Service Request   |
| ISI              | Intersymbol Interference   |
| ITM              | Instruction Trace Module   |
| ITU              | International Telecommunications Union   |
| LA               | Location Area  |
| LAI              | Location Area Identification   |
| LDO              | 1. Low-Dropout<br>2. low dropout regulator   |
| Li-ion           | Lithium ion battery  |

| <b>Term</b> | <b>Description/Usage</b>   |
|-------------|--|
| LNA         | low noise amplifier: Analog radio amplifier, used as the first stage in a GPS front-end. The GL-LN22 RF chip contains an integrated LNA on-chip.   |
| LPM         | 1. Longest Prefix Match: IP packet forwarding mechanism.<br>2. Longest Prefix Match: An algorithm used by routers in Internet Protocol (IP) networking to select an entry from a routing table.<br>3. low power mode |
| MBC         | main battery charger   |
| MBRDY       | PMU state is off but it is ready to turn on  |
| MBWV        | Main Battery Working Voltage   |
| MEMC        | memory controller  |
| MF          | More Fragments   |
| MIDI        | Musical Instrument Digital Interface   |
| MIPI        | Mobile Industry Processor Interface  |
| MLC         | Multi-Level Cell   |
| MM          | 1. multimedia<br>2. Mixed Mode<br>3. ESD Machine Model   |
| MMA         | Mobility Management Adaptation   |
| MME         | Mobility Management Entity   |
| MMR         | Mobility Management Router   |
| MS          | 1. mobile station: Refers to the handset or mobile wireless device in a C-plane architecture.<br>2. mobile subscriber  |
| MSTP        | Multiple Spanning Tree Protocol  |
| MTT         | Mobile Trace Terminal  |
| NCO         | Numerically Controlled Oscillator  |
| NM          | normal mode  |
| NNI         | Service-Provider Network Interface   |
| NTC         | Negative Temperature Coefficient   |
| OAM         | Operations, Administration, and Maintenance  |
| OCP         | Open Core Protocol   |
| ONFI        | Open NAND Flash Interface  |
| OTG         | On-the-Go  |
| P-TMSI      | Packet Temporary Mobile Subscriber Identity (GSM 03.60 version 7.4.1)  |
| PA          | power amplifier  |
| PCGUI       | Phone Control Graphical User Interface   |
| PCIe™       | PCI Express®   |
| PCP         | Priority Code Point  |
| PD          | 1. Protocol Discriminator (GPRS LLC-layer address field format) -<br>2. Phase Detector   |
| PDM         | pulse density modulation   |
| PDP         | Packet Data Protocol   |

| <b>Term</b> | <b>Description/Usage</b>   |
|-------------|--|
| PDU         | protocol data unit<br>1. OSI term for packet.<br>2. Information that is delivered as a unit between peer entities of a LAN or a MAN and contains control information, address information, and may contain user data.<br>3. A block of data that is exchanged between two devices using a protocol.  |
| PHY         | Physical Layer   |
| PIM         | 1. Protocol-Independent Multicast: Multicast routing architecture that allows the addition of IP multicast routing protocols. Packets are forwarded on all outgoing interfaces until pruning and truncation occur. In dense mode, receivers are densely populated, and it is assumed that the downstream networks want to receive and will use the datagrams that are forwarded to them. The cost of using dense mode is its default flooding behavior. Sometimes referred to as Dense Mode PIM or PIM DM. Contrast with PIM Sparse Mode.<br>2. personal information manager<br>3. personal information management |
| PLMN        | Public Land Mobile Network   |
| PMM         | 1. Packet Mobility Management (in GPRS)<br>2. Performance Measurement Matrix<br>3. Pressurized Multipurpose Module   |
| PMU         | Power Management Unit  |
| PPS         | Packet-Per-Second  |
| PSMS        | Power System Monitoring and Simulation   |
| PSRR        | Power Supply Rejection Ratio   |
| PTI         | Parallel Trace-Data Interface  |
| PTM         | Program Trace Macrocell  |
| PWM         | Pulse-Width Modulator  |
| PWRUP       | PMU state is off and it is not ready to turn on  |
| QoS         | Quality of Service   |
| RAI         | Routing Area Identification  |
| RNTI        | Radio Network Temporary Identifier (3GPP)  |
| RPLMN       | Registered Public Land Mobile Network  |
| RR          | Radio Resource   |
| RTOS        | Real-time Operating Systems  |
| RV          | Rate Violation   |
| S/PDIF      | Sony/Philips Digital Interconnect Format   |
| SAIC        | Single Antenna Interference Cancellation   |
| SCU         | Snoop Control Unit   |
| SDIO        | Secure Digital Input/Output  |
| SDP         | 1. Service Discovery Protocol<br>2. Session Description Protocol<br>3. Sockets Direct Protocol<br>4. Standard Downstream Port  |
| SDSR        | SD switching regulator   |
| SLC         | Single-Level Cell  |

| <b>Term</b> | <b>Description/Usage</b>  |
|-------------|---|
| SP          | Strict Priority   |
| SS          | Supplementary Services  |
| STM         | System Trace Module   |
| STP         | System Trace Protocol   |
| SWD         | Serial Wire Debug   |
| TBF         | Temporary Block Flow  |
| TC          | Traffic Class   |
| TL          | Transaction Layer   |
| TLB         | Translation Lookaside Buffer  |
| TLLI        | Temporary Logical Link Identity (GPRS protocols, LLC layer)   |
| TLP         | Transaction Layer Packet  |
| TOS         | Type Of Service   |
| TPID        | Tag Protocol ID   |
| TPIU        | Trace Port Interface Unit   |
| TTL         | Time To Live  |
| UDFs        | User-Defined Fields   |
| UMI         | Unified Memory Interface  |
| UMTS        | Universal Mobile Telecommunications System: The third generation mobile standards that will build on the success of GSM/GPRS and on the GSM operators' existing investment in infrastructure. Data rates offered will be up to 2 million bits per second. |
| UNI         | User Network Interface  |
| USBC        | USB charger   |
| USIM        | 1. User Services Identity Module (UMTS)<br>2. Universal Mobile Telecommunications System<br>3. UMTS subscriber identity mode  |
| USIMAP      | USIM application process  |
| UTRAN       | UMTS Terrestrial Radio Access Network: A conceptual term identifying that part of the network which consists of Radio Network Controllers and Node Base stations.   |
| VID         | VLAN ID   |
| VLAN        | Virtual LAN   |
| VMBAT       | Main Battery Voltage  |
| WAC         | wall adapter charger  |
| WDT         | watchdog timer  |
| WRR         | Weighted-Round-Robin  |
| XIP         | Execute in Place  |

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