Name :parmar Jignesh
Roll no: 112101035

Objective:

In this lab you will analyze the efficiency of different adder/subtractor topologies in terms of processing delay and power consumption.

Problem:

You are given two 4 bit unsigned numbers A and B in two 4 bit registers. You are required to implement the below mentioned scenarios in Verilog:

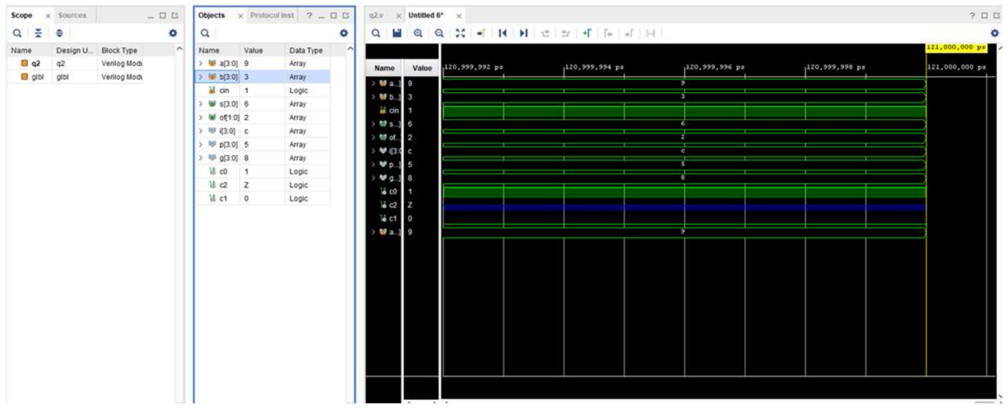
(a) Implement an adder that uses carry generate and propagate logic to add A and B.

Solution::

Code::

```
module  q1(input [3:0] a,b,  input c0,  output [3:0] s, output c4);
wire c1,c2,c3;
wire [3:0] p,g;
xor (p[0],a[0],b[0]);
xor (p[1],a[1],b[1]);
xor (p[2],a[2],b[2]);
xor (p[3],a[3],b[3]);
and (g[0],a[0],b[0]);
and (g[1],a[1],b[1]);
and (g[2],a[2],b[2]);
and (g[3],a[3],b[3]);
assign c1 = g[0]||(p[0]&&c0);
assign c2 = g[1]||(p[1]&&g[0])||(p[1]&&p[0]&&c0);
assign c3 = g[2]||(p[2]&&g[1])||(p[2]&&p[1]&&g[0])||(p[2]&&p[1]&&p[0]&&c0);
xor (s[0],p[0],c0);
xor (s[1],p[1],c1);
xor (s[2],p[2],c2);
xor (s[3],p[3],c3);
assign c4=g[3]||(p[3]&&c3);
endmodule
```

Wave diagram



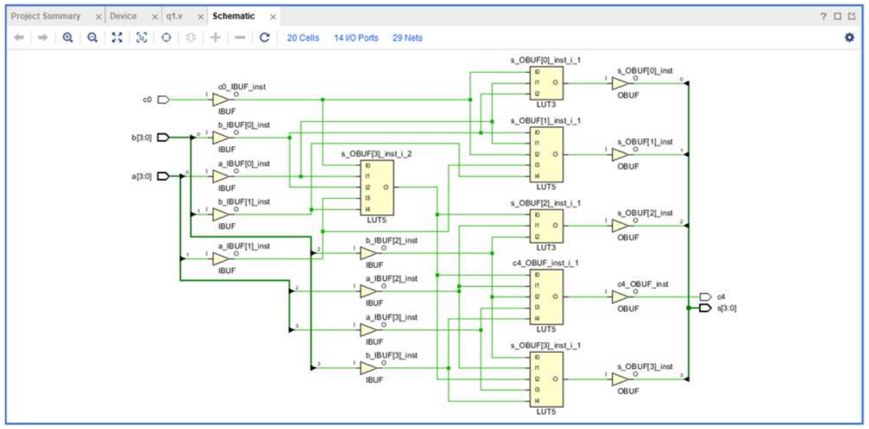
Scope | Sources

Name	Design U...	Block Type
q2	q2	Verilog Modu
glbl	glbl	Verilog Modu

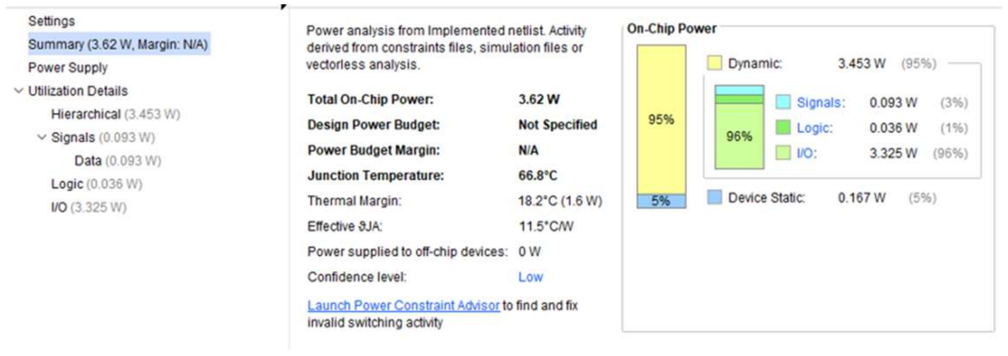
Objects | Protocol Inst

Name	Value	Data Type
a[3:0]	9	Array
b[3:0]	3	Array
cin	1	Logic
s[3:0]	6	Array
of[1:0]	2	Array
i[3:0]	c	Array
p[3:0]	5	Array
g[3:0]	8	Array
c0	1	Logic
c2	Z	Logic
c1	0	Logic

Design of logic



Power consumptin



Settings
Summary (3.62 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (3.453 W)
Signals (0.093 W)
Data (0.093 W)
Logic (0.036 W)
I/O (3.325 W)

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

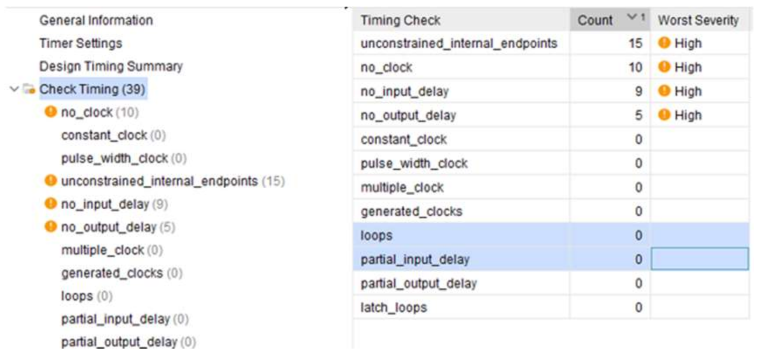
Total On-Chip Power:	**3.62 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**66.8°C**
Thermal Margin:	18.2°C (1.6 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	3.453 W	(95%)
Signals:	0.093 W	(3%)
Logic:	0.036 W	(1%)
I/O:	3.325 W	(96%)
Device Static:	0.167 W	(5%)

Timing diagram



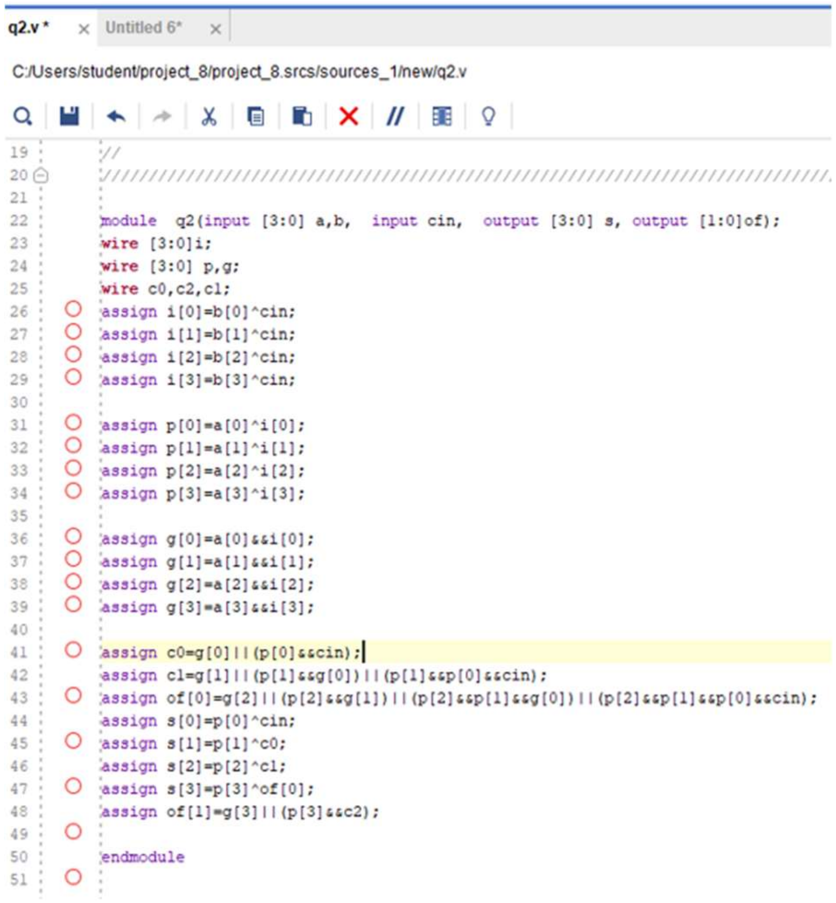
General Information
Timer Settings
Design Timing Summary
Check Timing (39)
no_clock (10)
constant_clock (0)
pulse_width_clock (0)
unconstrained_internal_endpoints (15)
no_input_delay (9)
no_output_delay (5)
multiple_clock (0)
generated_clocks (0)
loops (0)
partial_input_delay (0)
partial_output_delay (0)

Timing Check	Count	Worst Severity
unconstrained_internal_endpoints	15	High
no_clock	10	High
no_input_delay	9	High
no_output_delay	5	High
constant_clock	0	
pulse_width_clock	0	
multiple_clock	0	
generated_clocks	0	
loops	0	
partial_input_delay	0	
partial_output_delay	0	
latch_loops	0	

(b) Implement a subtractor that uses carry generate and propagate logic to subtract B from A.

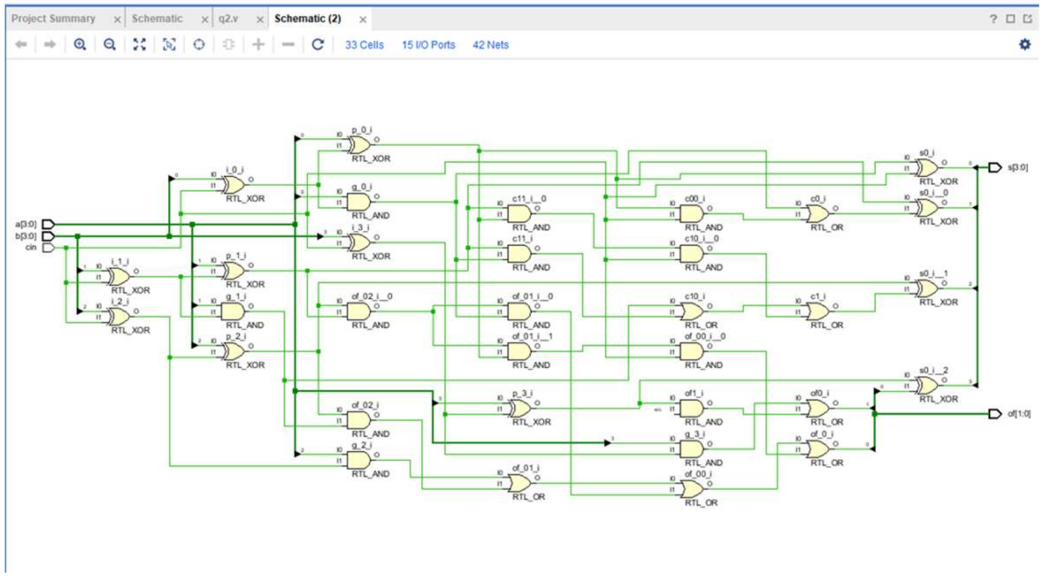
Solution::

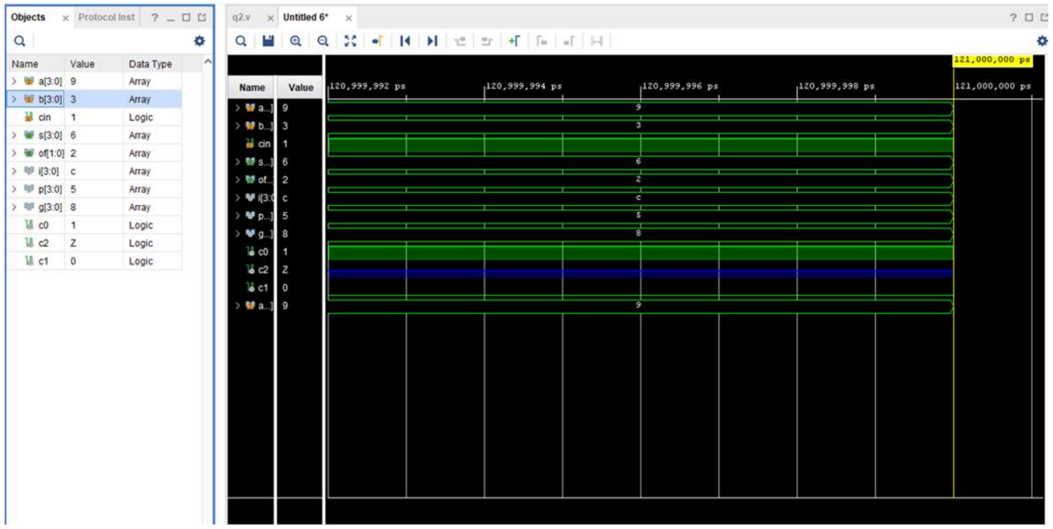
Code:



C:/Users/student/project_8/project_8.srcs/sources_1/new/q2.v

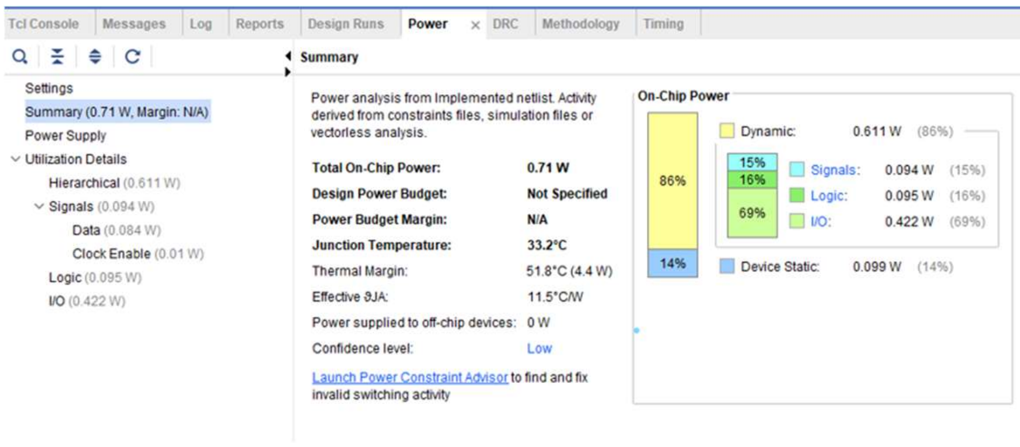
```verilog
//
///////////////////////////////////////////////////////////////////////

module  q2(input [3:0] a,b,  input cin,  output [3:0] s, output [1:0]of);
wire [3:0]i;
wire [3:0] p,g;
wire c0,c2,cl;
assign i[0]=b[0]^cin;
assign i[1]=b[1]^cin;
assign i[2]=b[2]^cin;
assign i[3]=b[3]^cin;

assign p[0]=a[0]^i[0];
assign p[1]=a[1]^i[1];
assign p[2]=a[2]^i[2];
assign p[3]=a[3]^i[3];

assign g[0]=a[0]&&i[0];
assign g[1]=a[1]&&i[1];
assign g[2]=a[2]&&i[2];
assign g[3]=a[3]&&i[3];

assign c0=g[0]||(p[0]&&cin);
assign cl=g[1]||(p[1]&&g[0])||(p[1]&&p[0]&&cin);
assign of[0]=g[2]||(p[2]&&g[1])||(p[2]&&p[1]&&g[0])||(p[2]&&p[1]&&p[0]&&cin);
assign s[0]=p[0]^cin;
assign s[1]=p[1]^c0;
assign s[2]=p[2]^cl;
assign s[3]=p[3]^of[0];
assign of[1]=g[3]||(p[3]&&c2);

endmodule
```





Name	Value	Data Type
a[3:0]	9	Array
b[3:0]	3	Array
cin	1	Logic
s[3:0]	6	Array
of[1:0]	2	Array
i[3:0]	c	Array
p[3:0]	5	Array
g[3:0]	8	Array
c0	1	Logic
c2	Z	Logic
c1	0	Logic

Name	Value
a...]	9
b...]	3
cin	1
s...]	6
of...	2
i[3:0	c
p...]	5
g...]	8
c0	1
c2	Z
c1	0
a...]	9



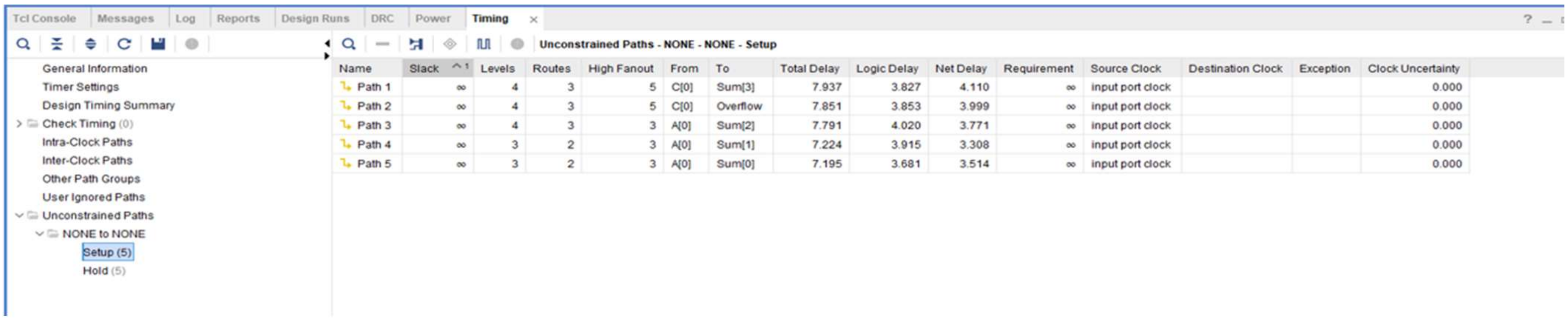
Settings
Summary (0.71 W, Margin: N/A)
Power Supply
Utilization Details
- Hierarchical (0.611 W)
- Signals (0.094 W)
  - Data (0.084 W)
  - Clock Enable (0.01 W)
- Logic (0.095 W)
- I/O (0.422 W)

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.71 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**33.2°C**
Thermal Margin:	51.8°C (4.4 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

Dynamic:	0.611 W	(86%)
Signals:	0.094 W	(15%)
Logic:	0.095 W	(16%)
I/O:	0.422 W	(69%)
Device Static:	0.099 W	(14%)



General Information
Timer Settings
Design Timing Summary
Check Timing (0)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
- NONE to NONE
  - Setup (5)
  - Hold (5)

Unconstrained Paths - NONE - NONE - Setup

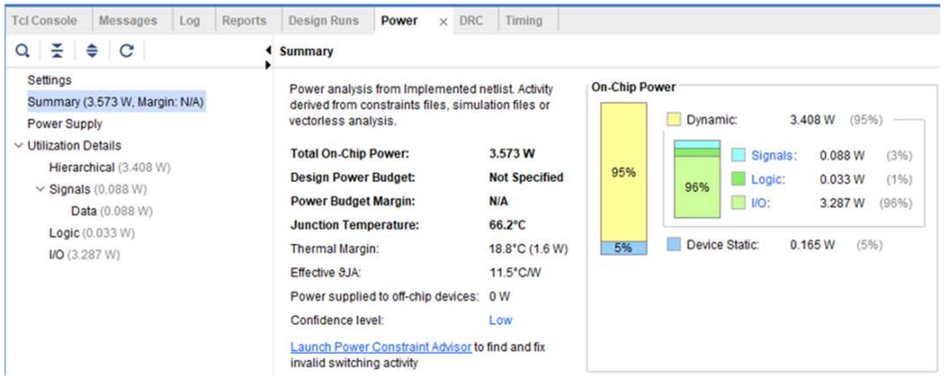
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clock Uncertainty
Path 1	∞	4	3	5	C[0]	Sum[3]	7.937	3.827	4.110	∞	input port clock			0.000
Path 2	∞	4	3	5	C[0]	Overflow	7.851	3.853	3.999	∞	input port clock			0.000
Path 3	∞	4	3	3	A[0]	Sum[2]	7.791	4.020	3.771	∞	input port clock			0.000
Path 4	∞	3	2	3	A[0]	Sum[1]	7.224	3.915	3.308	∞	input port clock			0.000
Path 5	∞	3	2	3	A[0]	Sum[0]	7.195	3.681	3.514	∞	input port clock			0.000

(c) Implement a subtractor using ripple carry adder in Lab 1 to subtract B from A

Solution::

Code::

```
module full_adder(input x, input y,                  input ci,                  output s,                  output co);
wire w1,w2,w3;
xor g1(w1,x,y);
xor g2(s,w1,ci);
and g3(w2,w1,ci);
and g4(w3,x,y);
or g5(co,w2,w3);
endmodule
module adder_1(input [3:0]a, input[3:0]b,  input cin, output[3:0]sum, output cout,overflow);
wire [3:0]i;
assign i[0]= b[0]^cin;assign i[1]= b[1]^cin;assign i[2]= b[2]^cin;assign i[3]= b[3]^cin;
wire c0,c1,c2,c3;
full_adder fa0(a[0],i[0],cin,sum[0],c0);    full_adder fa1(a[1],i[1],c0,sum[1],c1);
full_adder fa2(a[2],i[2],c1,sum[2],c2);    full_adder fa3(a[3],i[3],c2,sum[3],cout);
assign overflow = cout^c2;
endmodule
```



Summary

Settings
Summary (3.573 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (3.408 W)
Signals (0.088 W)
Data (0.088 W)
Logic (0.033 W)
I/O (3.287 W)

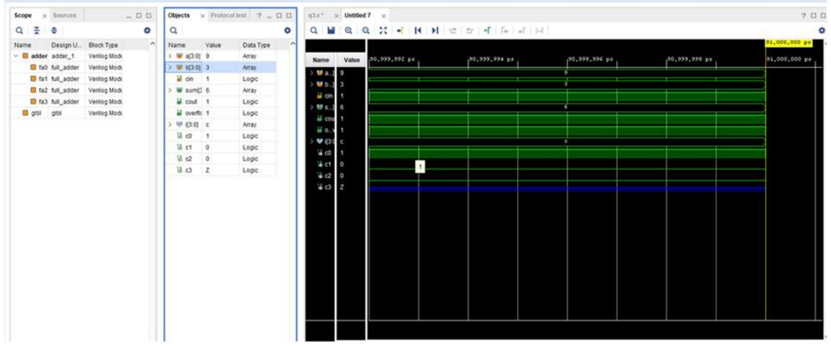
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**3.573 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**66.2°C**
Thermal Margin:	18.8°C (1.6 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

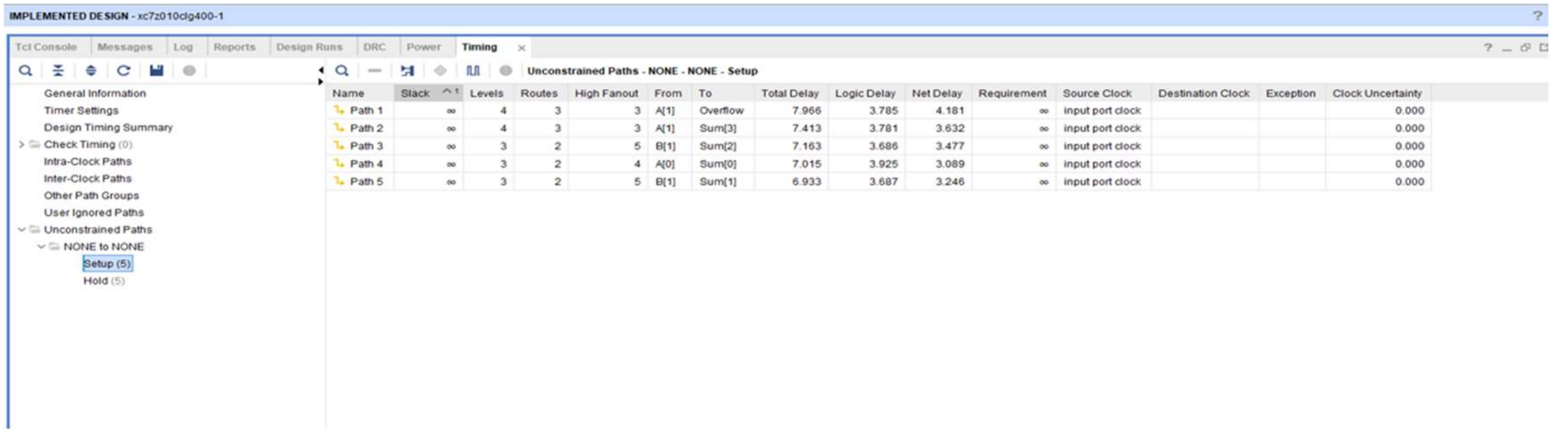
On-Chip Power

95%	Dynamic:	3.408 W	(95%)
96%	Signals:	0.088 W	(3%)
	Logic:	0.033 W	(1%)
	I/O:	3.287 W	(96%)
5%	Device Static:	0.165 W	(5%)



Name	Design U...	Block Type
adder	adder_1	Verilog Modu
fa0	full_adder	Verilog Modu
fa1	full_adder	Verilog Modu
fa2	full_adder	Verilog Modu
fa3	full_adder	Verilog Modu
glbl	glbl	Verilog Modu

Name	Value	Data Type
a[3:0]	9	Array
b[3:0]	3	Array
cin	1	Logic
sum[3	6	Array
cout	1	Logic
overfl	1	Logic
c[3:0]	c	Array
c0	1	Logic
c1	0	Logic
c2	0	Logic
c3	Z	Logic

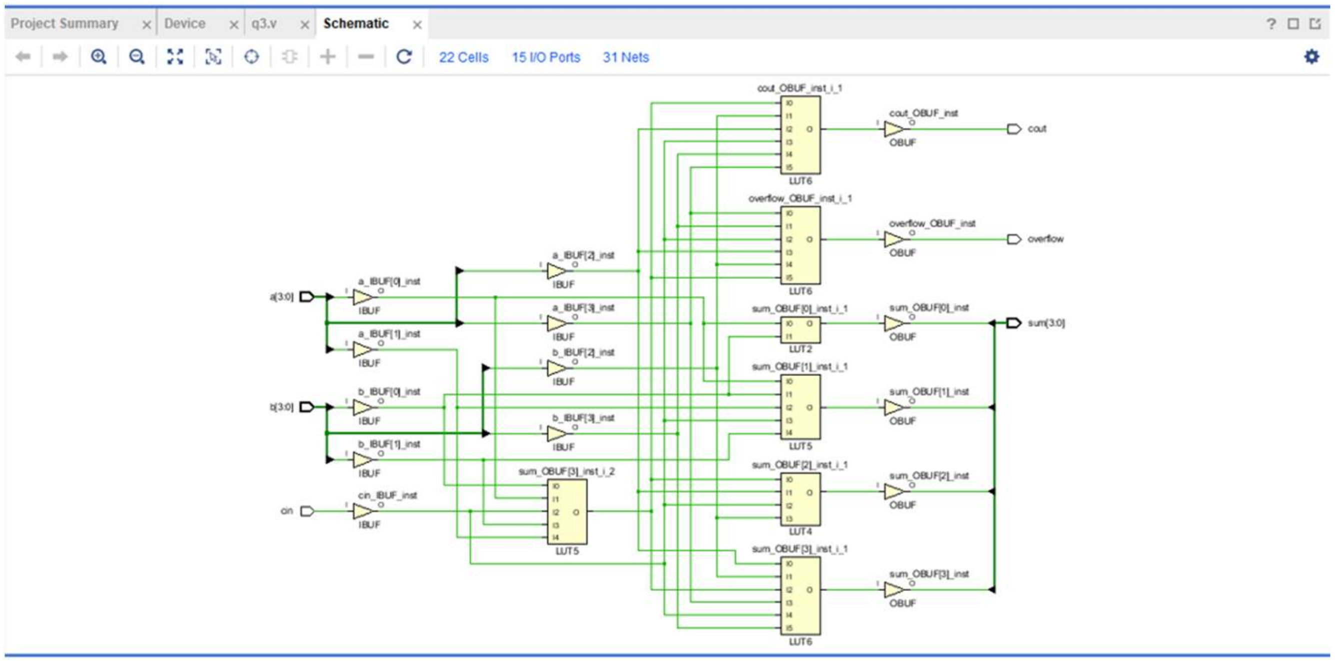


IMPLEMENTED DESIGN - xc7z010clg400-1

Unconstrained Paths - NONE - NONE - Setup

General Information
Timer Settings
Design Timing Summary
Check Timing (0)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
NONE to NONE
Setup (5)
Hold (5)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clock Uncertainty
Path 1	∞	4	3	3	A[1]	Overflow	7.966	3.785	4.181	∞	input port clock			0.000
Path 2	∞	4	3	3	A[1]	Sum[3]	7.413	3.781	3.632	∞	input port clock			0.000
Path 3	∞	3	2	5	B[1]	Sum[2]	7.163	3.686	3.477	∞	input port clock			0.000
Path 4	∞	3	2	4	A[0]	Sum[0]	7.015	3.925	3.089	∞	input port clock			0.000
Path 5	∞	3	2	5	B[1]	Sum[1]	6.933	3.687	3.246	∞	input port clock			0.000



Conclusion::

Power consumption of ripple carry adder is more than and it has less time delay comared to another one