CS2610: Computer Organization and Architecture

Lab 4

Problem Statement:
In this lab you will design a RISC-V Instruction Decoder unit and a Register File Unit having following features:

Decoder Unit

i. The input to the decoder unit will be a 32-bit instruction based on RISC-V ISA (restricted to R-type and I-type instructions only)
ii. There are four outputs of the decoder:
    a. Output 1 is for opcode
    b. Output 2 is address of source register 1
    c. Output 3 is address of source register 2
    d. Output 4 is address of destination register
    e. Output 5 is for immediate value

Register File

i. There are thirty-two 32-bit registers (x_0 **to** x_{31}) where the description of each register is provided below.
ii. Register File has two read ports (32 bits) and one write port (32 bits)
iii. Input to the Register File is the addresses of source registers and address of the destination register. Additionally, one input is required which determine a read/write cycle and one input (32 bit is required that will be loaded inside register based on write address.
iv. Based on the input, Register File should read the source registers and output its value during read cycle or update the specific register during the write cycle.

- x0: the constant value 0
- x1: return address
- x2: stack pointer
- x3: global pointer
- x4: thread pointer
- x5 – x7, x28 – x31: temporaries
- x8: frame pointer
- x9, x18 – x27: saved registers
- x10 – x11: function arguments/results
- x12 – x17: function arguments