CS2610: Computer Organization and Architecture

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Problem:
You are given two 4-bit unsigned numbers A and B in two 4-bit registers. You are required to
implement the addition of A and B in Verilog for the below mentioned scenarios:

1. You are provided with 4 full adders and two 4-bit registers R0 and R1.

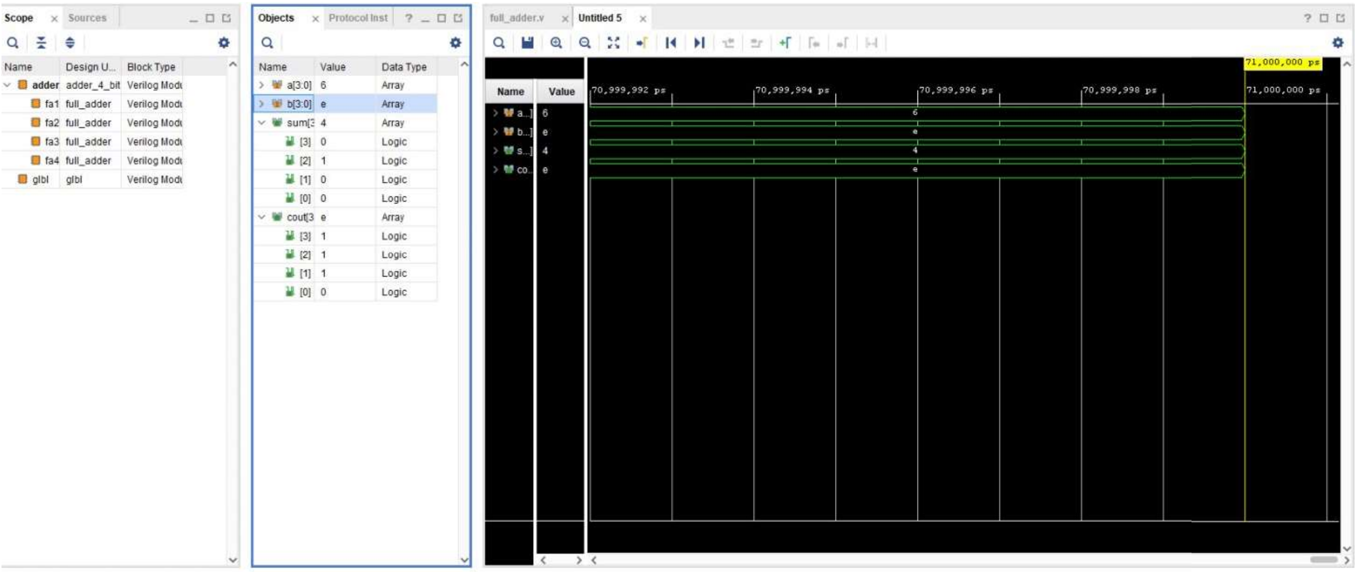
Solution:

Code :

```
Module full_adder(input a,b,c_in,output sum,c_out) assign sum =a^b^c;
assign c_out=(a&b) | c_in &(a^b);
endmodule

module adder_4_bit(input[3:0]a,b, output[3:0]sum,cout) full_adder
fa1(a[0],b[0],0,sum[0],cout[0]);
full_adder fa1(a[1],b[1],cout[1],sum[1],cout[1]);
full_adder fa1(a[2],b[2],cout[2],sum[2],cout[2]);
full_adder fa1(a[3],b[3],cout[3],sum[3],cout[3]); endmodule
```

Wave diagram:

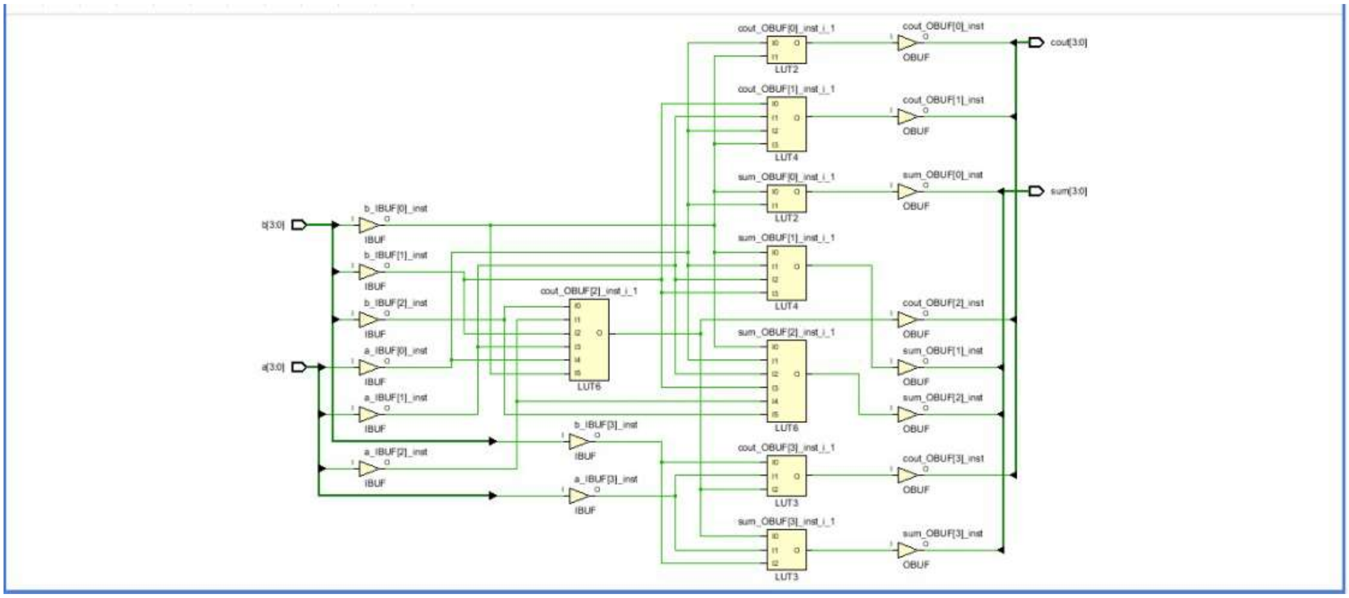


Name	Design U...	Block Type
adder	adder_4_bit	Verilog Modu
fa1	full_adder	Verilog Modu
fa2	full_adder	Verilog Modu
fa3	full_adder	Verilog Modu
fa4	full_adder	Verilog Modu
glbl	glbl	Verilog Modu

Name	Value	Data Type
a[3:0]	6	Array
b[3:0]	e	Array
sum[3	4	Array
[3]	0	Logic
[2]	1	Logic
[1]	0	Logic
[0]	0	Logic
cout[3	e	Array
[3]	1	Logic
[2]	1	Logic
[1]	1	Logic
[0]	0	Logic

Name	Value
a...]	6
b...]	e
s...]	4
co...	e

Logic diagram:



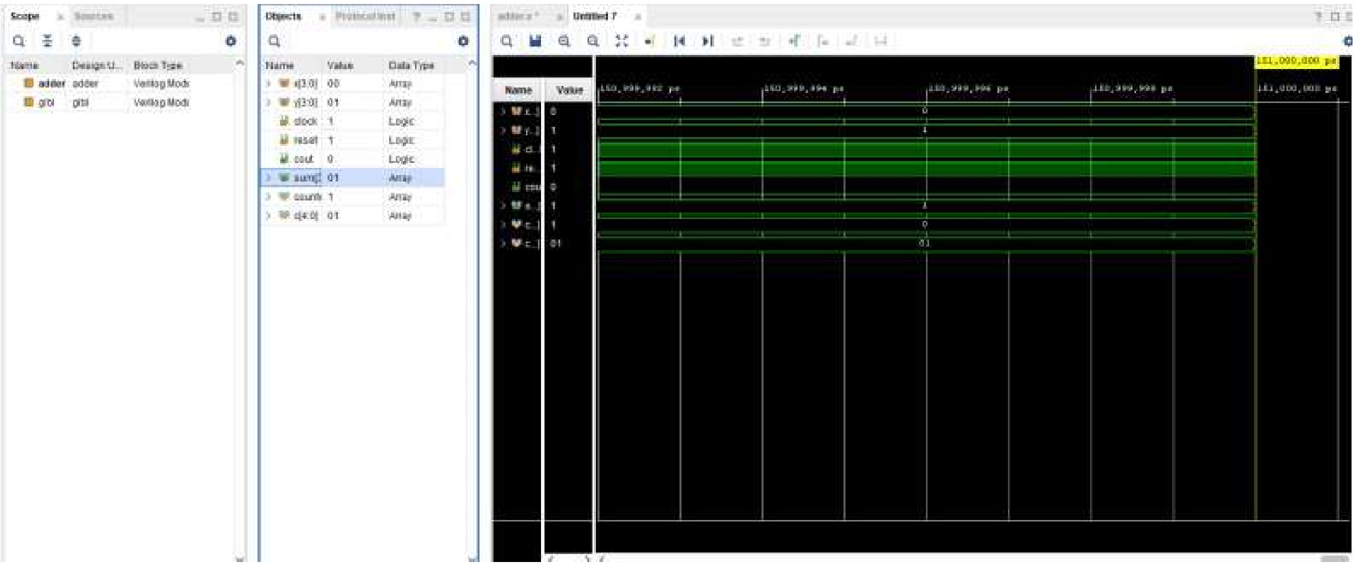
2. You are provided with only 1 full adder and two 4-bit registers R0 and R1.

Solution:

Code :

```
module adder(input [3:0],x,y,input clock,reset,output out,output reg [3;0]sum)
reg [1:0]counter;
reg [4:0]c;
always@(posedge clock)
begin
if(reset==1)
        begin
                counter<=0;
                c[0]=1'b0;
                end
else
        begin
                sum[counter]<=x[counter]^y[counter]^c[counter];
                c[counter]<=(x[counter]&y[counter])|(x[counter]^y[counter] & c[counter]);
                counter<=counter+1;
                end
        end
assign cout=c[4];
endmodule
```

Wave diagram:



Scope | Sources

Name	Design U...	Block Type
adder	adder	Verilog Modu
glbl	glbl	Verilog Modu

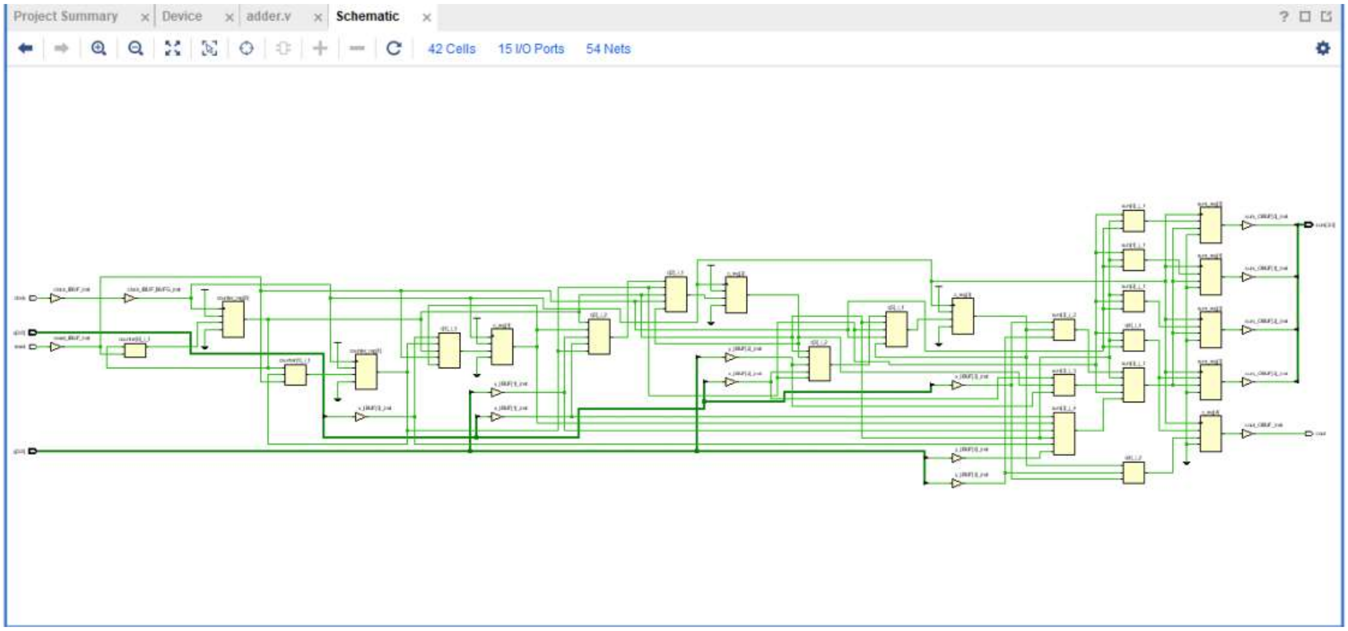
Objects | Protocol Inst

Name	Value	Data Type
x[3:0]	00	Array
y[3:0]	01	Array
clock	1	Logic
reset	1	Logic
cout	0	Logic
sum[	01	Array
count	1	Array
d[4:0]	01	Array

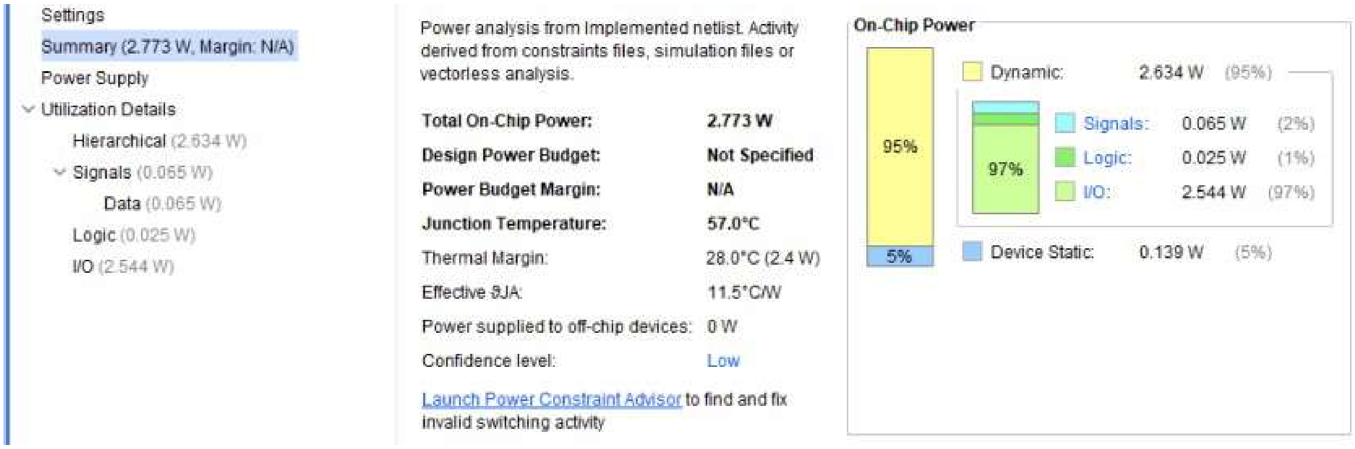
adder.v* | Untitled 7

Name	Value
x_]	0
y_]	1
cl...	1
re...	1
cou	0
s_]	1
c_]	1
c_]	01

Logic diagram:



Power consuption for 1st



Settings
Summary (2.773 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (2.634 W)
Signals (0.065 W)
Data (0.065 W)
Logic (0.025 W)
I/O (2.544 W)

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

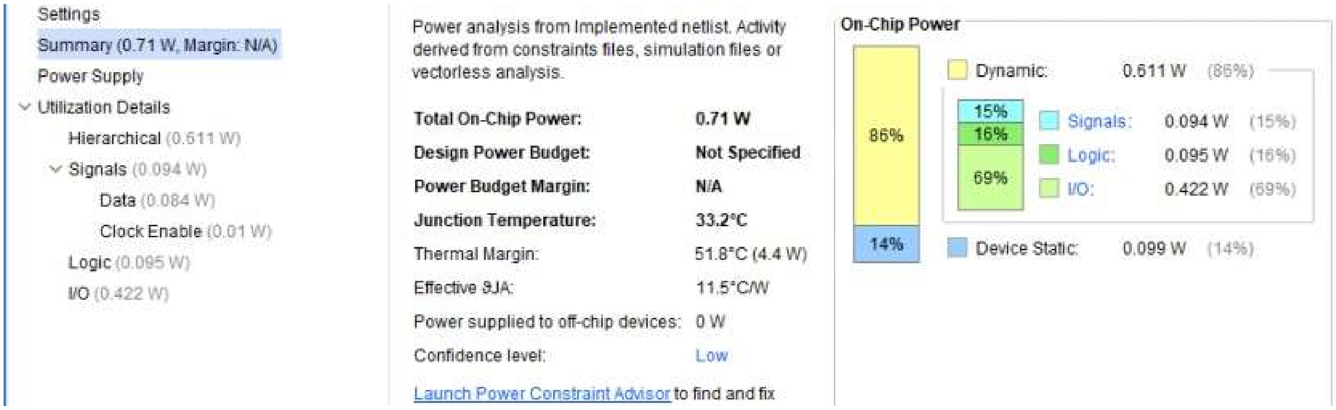
Total On-Chip Power:	**2.773 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**57.0°C**
Thermal Margin:	28.0°C (2.4 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	2.634 W	(95%)
Signals:	0.065 W	(2%)
Logic:	0.025 W	(1%)
I/O:	2.544 W	(97%)
Device Static:	0.139 W	(5%)

Power consuption for 2nd



Settings
Summary (0.71 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.611 W)
Signals (0.094 W)
Data (0.084 W)
Clock Enable (0.01 W)
Logic (0.095 W)
I/O (0.422 W)

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

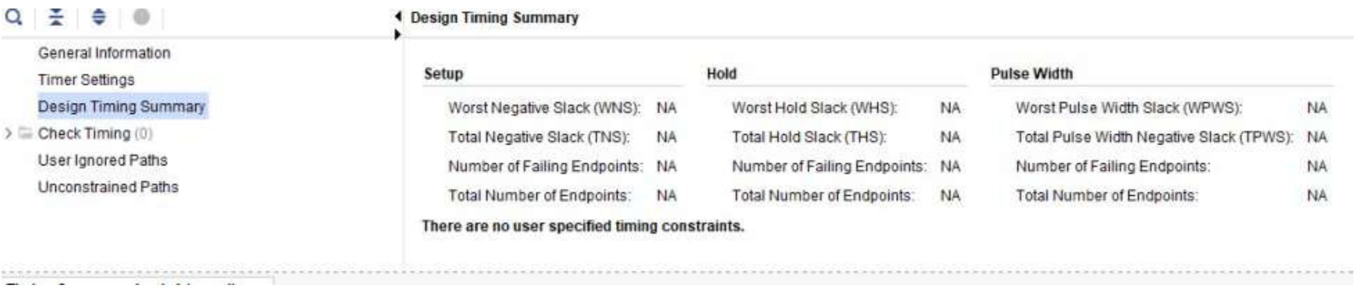
Total On-Chip Power:	**0.71 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**33.2°C**
Thermal Margin:	51.8°C (4.4 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix

On-Chip Power

Dynamic:	0.611 W	(86%)
Signals:	0.094 W	(15%)
Logic:	0.095 W	(16%)
I/O:	0.422 W	(69%)
Device Static:	0.099 W	(14%)

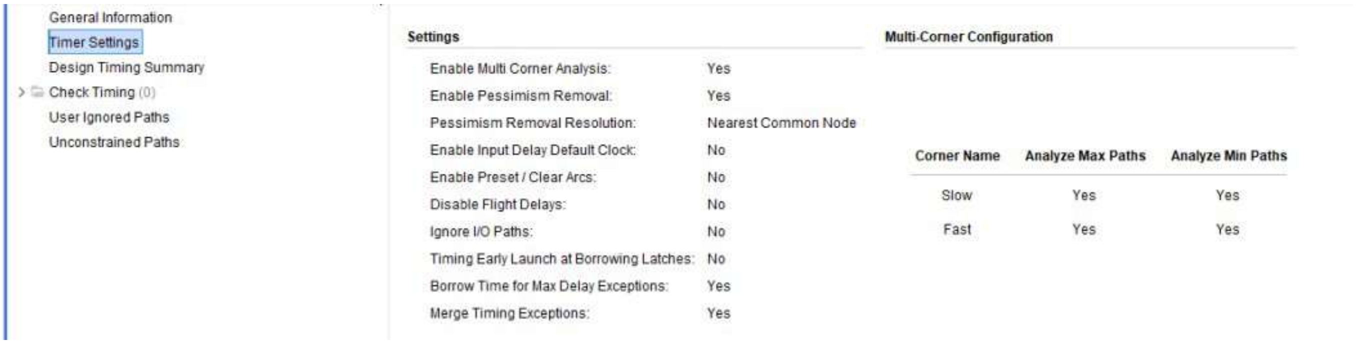
Time delay for 1st question:



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	NA	Worst Hold Slack (WHS):	NA	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	NA	Total Hold Slack (THS):	NA	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA	Total Number of Endpoints:	NA	Total Number of Endpoints:	NA

There are no user specified timing constraints.

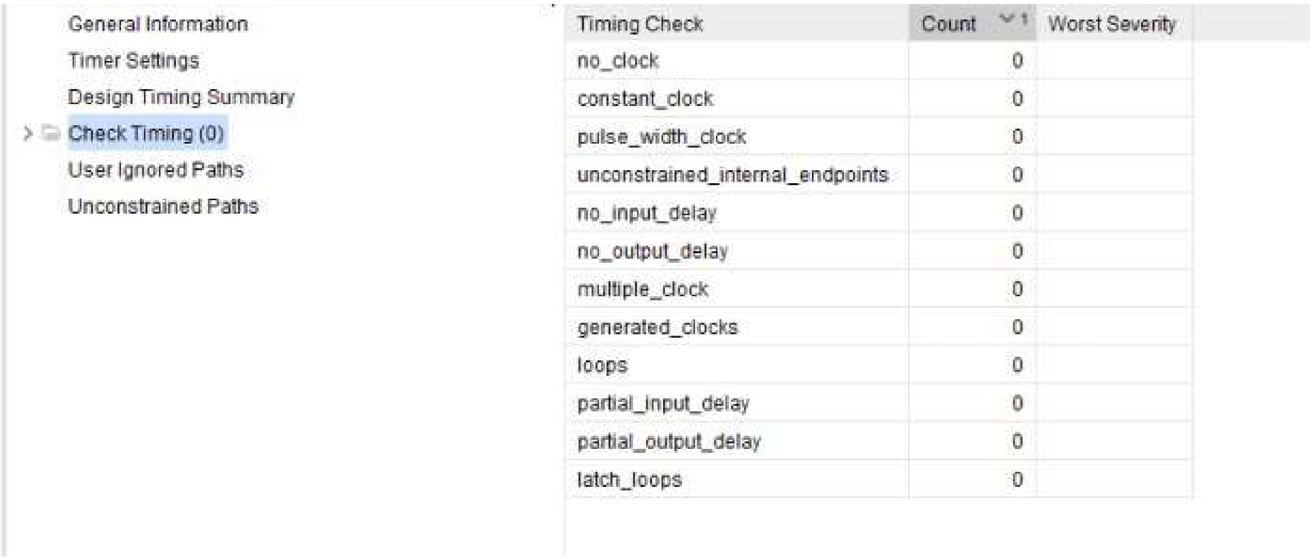


Settings

Enable Multi Corner Analysis:	Yes
Enable Pessimism Removal:	Yes
Pessimism Removal Resolution:	Nearest Common Node
Enable Input Delay Default Clock:	No
Enable Preset / Clear Arcs:	No
Disable Flight Delays:	No
Ignore I/O Paths:	No
Timing Early Launch at Borrowing Latches:	No
Borrow Time for Max Delay Exceptions:	Yes
Merge Timing Exceptions:	Yes

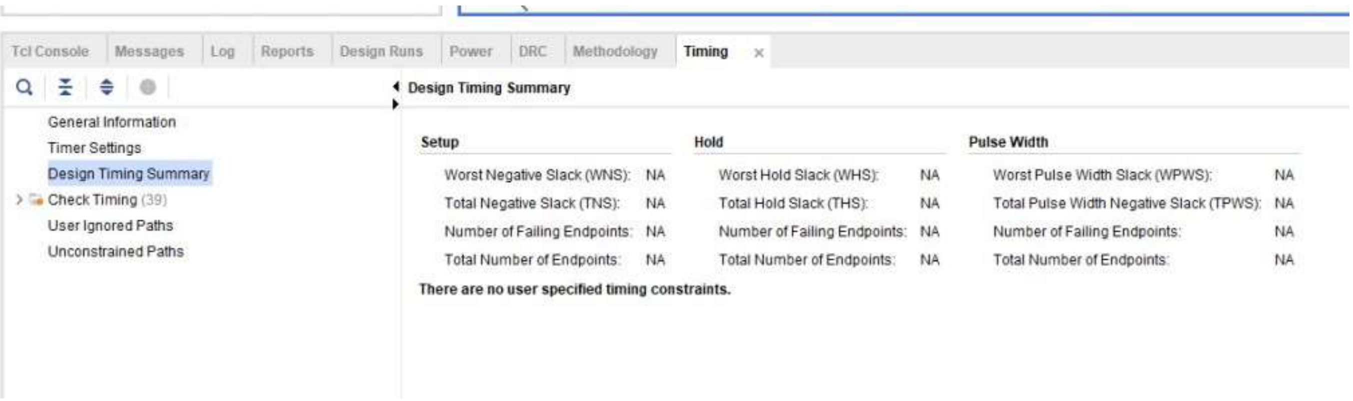
Multi-Corner Configuration

Corner Name	Analyze Max Paths	Analyze Min Paths
Slow	Yes	Yes
Fast	Yes	Yes



Timing Check	Count	Worst Severity
no_clock	0	
constant_clock	0	
pulse_width_clock	0	
unconstrained_internal_endpoints	0	
no_input_delay	0	
no_output_delay	0	
multiple_clock	0	
generated_clocks	0	
loops	0	
partial_input_delay	0	
partial_output_delay	0	
latch_loops	0	

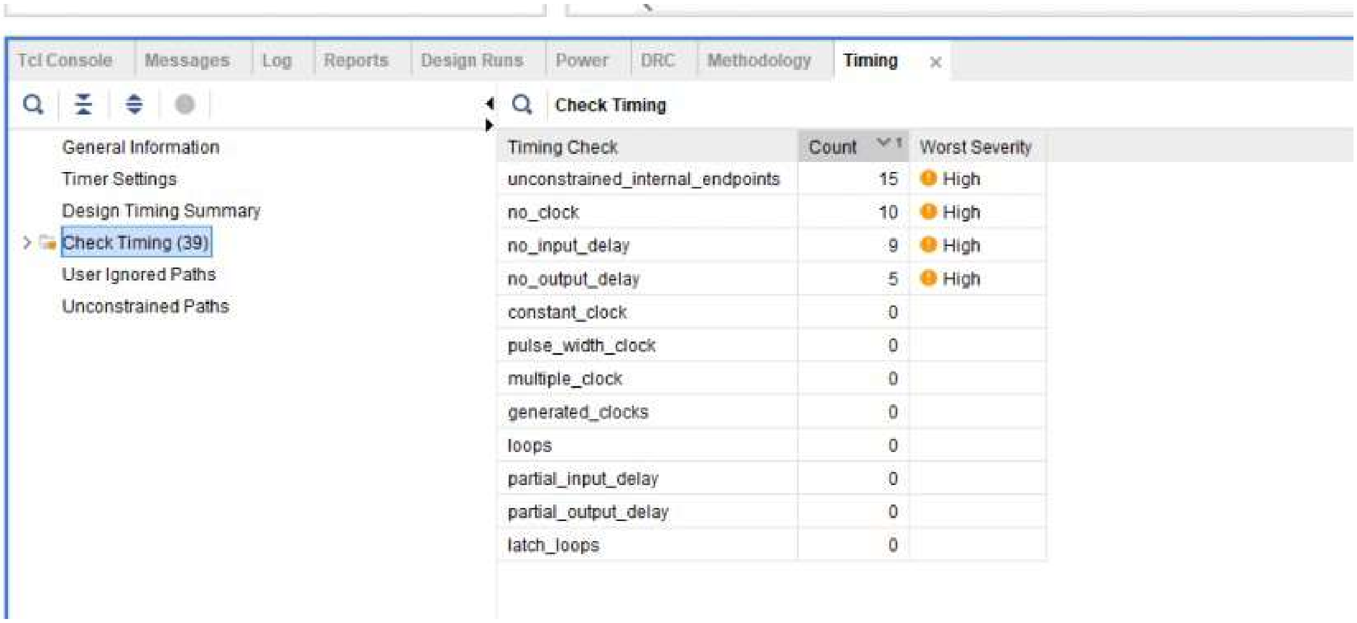
Time delay for 2nd question:



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	NA	Worst Hold Slack (WHS):	NA	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	NA	Total Hold Slack (THS):	NA	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA	Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA	Total Number of Endpoints:	NA	Total Number of Endpoints:	NA

There are no user specified timing constraints.



Check Timing

Timing Check	Count	Worst Severity
unconstrained_internal_endpoints	15	● High
no_clock	10	● High
no_input_delay	9	● High
no_output_delay	5	● High
constant_clock	0	
pulse_width_clock	0	
multiple_clock	0	
generated_clocks	0	
loops	0	
partial_input_delay	0	
partial_output_delay	0	
latch_loops	0	

Thus from the above time delay and power consumption diagrams we can conclude that second one is better than first one cause first one is consuming around 0.139 w at a time and second has less consumption 0.099 w as compared to first.