CS2610: Computer Organization and Architecture

Lab 6

Problem Statement:

In this lab you will design a two stage a RISC-V Pipeline that combines the ALU and Register File modules that you designed in Lab 4 and Lab 5. Input to the pipeline will be a sequence of 32-bit instructions of R-type and I-type. The pipeline will perform operations based on your ALU capabilities (i.e. addition, subtraction and multiplication). Since this is a pipelined implementation, you will require pipeline registers to hold intermediate data and control values. The size of pipeline registers should be identified for each stage. A representative figure of the data-path is shown below in Figure 1.

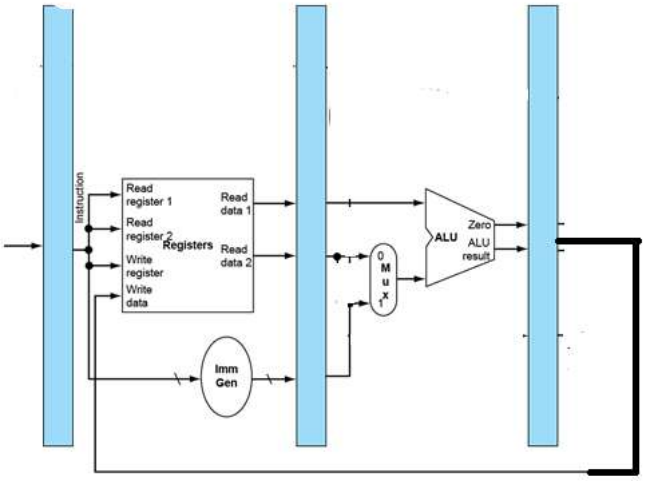

Figure 1: RISC-V Two-Stage Pipeline

Mandatory Submission:

1) This is a team project (max 3 students)
2) A lab report (softcopy) is due on Sunday (02-04-2023) by 11:59 PM.
3) The report must be submitted via moodle. Must contain timing, power consumption and test bench (with details on testing strategy)
4) The report must clearly describe your approach in solving the given problem, experiment results and conclusions.
5) Please use snapshots from the tool to discuss your findings.
6) Strictly no Plagiarism! Copied report will lead to zero marks.
7) Late submissions will not be entertained.