JIHO KIM

Computer Architecture Research and Engineering

jihokimhi@gmail.com https://sites.google.com/view/jihokim/ Last update: May. 2025

ABOUT ME

I've studied the computer architecture that includes interconnection networks, storage, GPU and RDMA. Fortunately, I was able to work on different architectures during my graduate school. I enjoyed contributing to all the work and I am truly proud of the results of all research projects to which I have contributed :). After graduation, my working domain has been a bit extended from device-specific scope to a computer system that includes user/kernel drivers to work with custom hardware design in addition to hardware offloaded architecture. I always like to find solutions to see how novel ideas have an effect on real-world challenges, and I would love to experience a practical solution.

WORK EXPERIENCE

System Architect

Mangoboost

May. 2023 – Current Seoul, Korea

- **RDMA:** Development of FPGA-based RoCEv2 to accelerate AI infrastructure and HPC

Research Intern

Samsung Memory

Dec. 2022 – Feb. 2023 Hwaseong, Korea

- **SmartSSD 2.0:** Enabling device-to-device communication (Advanced Development Team)

Research Assistant

KAIST

Aug. 2017 – Aug. 2018 Daejeon, Korea

- **GPU NoC:** Implications of HBM on GPU On-chip Network (advised by Prof. John Kim)
- **Multi-tenant GPU:** GPU Multitasking and kernel scheduling (advised by Prof. Yongjun Park)

EDUCATION

Ph.D. in Electrical Engineering

Korea Advanced Institution of Science and Technology (KAIST)

Aug. 2018 – Feb. 2024

Thesis title: Communication-centric Storage Architecture for High-bandwidth SSD

M.S. in Electrical Engineering

Hongik University

Mar. 2015 – Jul. 2017

B.S. in Electrical Engineering

Hongik University

Mar. 2009 – Feb. 2015

PUBLICATIONS

Conference Proceedings

- Z. Jin, J. Ahn, **Jiho Kim**, *et al.*, "Ghost arbitration: Mitigating interconnect side-channel timing attacks," in *2024 57th IEEE/ACM International Symposium on Microarchitecture **(MICRO)***, 2024, pp. 1–13.
- Z. Jin, C. Rocca, **Jiho Kim**, *et al.*, "Uncovering real gpu noc characteristics: Implications on interconnect architecture," in *2024 57th IEEE/ACM International Symposium on Microarchitecture **(MICRO)***, 2024, pp. 1–13.
- **Jiho Kim**, M. Jung, and J. Kim, "Decoupled ssd: Rethinking ssd architecture through network-based flash controllers," in *Proceedings of the 50th Annual International Symposium on Computer Architecture **(ISCA)***, 2023, pp. 1–13.
- **Jiho Kim**, S. Kang, Y. Park, and J. Kim, "Networked ssd: Flash memory interconnection network for high-bandwidth ssd," in *2022 55th IEEE/ACM International Symposium on Microarchitecture **(MICRO)***, IEEE, 2022, pp. 388–403.
- J. Ahn, **Jiho Kim**, H. Kasan, *et al.*, "Network-on-chip microarchitecture-based covert channel in gpus," in *MICRO-54: 54th Annual IEEE/ACM International Symposium on Microarchitecture **(MICRO)***, 2021, pp. 565–577.
- J. Ahn, C. Jin, **Jiho Kim**, *et al.*, "Trident: A hybrid correlation-collision gpu cache timing attack for aes key recovery," in *2021 IEEE International Symposium on High-Performance Computer Architecture **(HPCA)***, IEEE, 2021, pp. 332–344.
- **Jiho Kim**, S. Cho, M. Rhu, A. Bakhoda, T. M. Aamodt, and J. Kim, "Bandwidth bottleneck in network-on-chip for high-throughput processors," in *Proceedings of the ACM International Conference on Parallel Architectures and Compilation Techniques **(PACT-Poster)***, 2020, pp. 157–158.
- **Jiho Kim**, J. Kim, and Y. Park, "Navigator: Dynamic multi-kernel scheduling to improve gpu performance," in *2020 57th ACM/IEEE Design Automation Conference **(DAC)***, IEEE, 2020, pp. 1–6.
- S. Kang, Y. Yu, **Jiho Kim**, and Y. Park, "Gate: A generalized dataflow-level approximation tuning engine for data parallel architectures," in *Proceedings of the 56th Annual Design Automation Conference **(DAC)***, 2019, pp. 1–6.
- J. Cha, **Jiho Kim**, and Y. Park, "Core-level dvfs for spatial multitasking gpus," in ***TENCON** 2018-2018 IEEE Region 10 Conference*, IEEE, 2018, pp. 1525–1528.

Journal Articles

- **Jiho Kim**, M. Jung, and J. Kim, "Decoupled ssd: Reducing data movement on nand-based flash ssd," *IEEE Computer Architecture Letters **(CAL)***, vol. 20, no. 2, pp. 150–153, 2021.
- **Jiho Kim**, J. Cha, J. J. K. Park, D. Jeon, and Y. Park, "Improving gpu multitasking efficiency using dynamic resource sharing," *IEEE Computer Architecture Letters **(CAL)***, vol. 18, no. 1, pp. 1–5, 2018.
- **Jiho Kim**, M. Chu, and Y. Park, "Efficient gpu multitasking with latency minimization and cache boosting," ***IEICE Electronics Express***, vol. 14, no. 7, pp. 20 161 158–20 161 158, 2017.

ACADEMIC EXPERIENCE

High-Performance Computer Architecture (HPCA)
Light Program Committee (2024)

Transactions on Architecture and Code Optimization (TACO)
Reviewer

STRENGTHS

Hard-working | Cooperative | Enthusiastic | Never give-up
Strong C/C++ | Python | Verilog | SystemC | FPGA
Computer Architecture | SSD | RDMA | GPU | Interconnect | Simulations

LANGUAGES

Korean ●●●●●

English ●●◐○○

REFEREES

Prof. John Kim
@ KAIST, Daejeon, Korea
iamjohnkim@gmail.com
https://icn.kaist.ac.kr/~jjk12/

Prof. Yongjun Park
@ Yonsei Univerisy, Seoul, Korea
yongjunpark@yonsei.com
https://sites.google.com/view/asolabysu/home