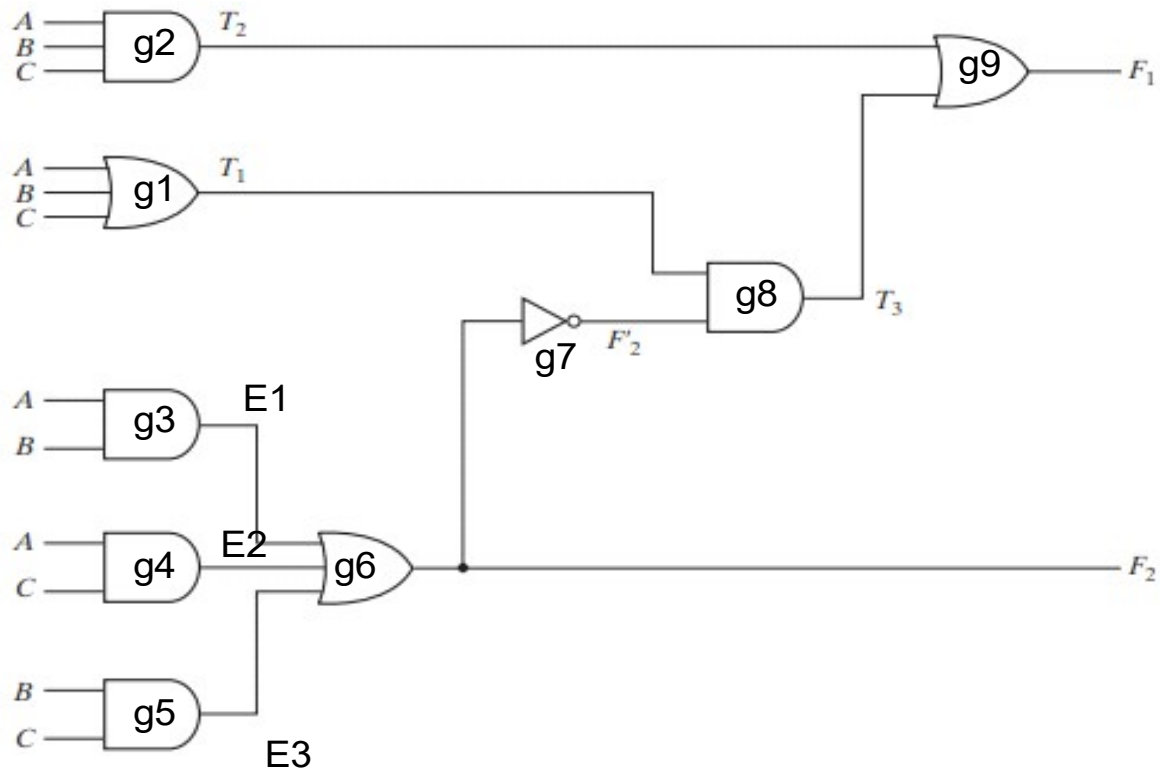


Circuito combinacional para analizar:



Determinación de la tabla de verdad del circuito combinacional

A	B	C	F1	F2
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

The screenshot displays the EDA Playground web interface. The left sidebar contains the following sections:

- Languages & Libraries**
  - Testbench + Design**: SystemVerilog/Verilog (selected)
  - UVM / OVM**: None (selected)
  - Other Libraries**: None (selected), with options for OVL 2.8.1 and SVUnit 2.11.
  - Enable TL-Verilog (unchecked)
  - Enable Easier UVM (unchecked)
  - Enable VUnit (unchecked)
- Tools & Simulators**: Icarus Verilog 0.10.0 11/23 (selected)
- Compile Options**: Compile Options (text input)
- Run Options**: Run Options (text input)
- Options**:
  - ☒ Open EPWave after run
  - ☐ Show output file after run
  - ☐ Download files after run
- Examples**: using EDA Playground (button)

The right pane shows a Verilog testbench file named `testbench.sv` with the following code:

```
1 //tes
2 modul
3 reg
4 win
5 ana
6 ini
7 b
8
9
10
11 el
12 ini
13 b
14
15
16
17 el
18 endmo
```

Below the code is a **Log** button and a list of simulation results:

```
ABC = 011
ABC = 100
ABC = 101
ABC = 110
ABC = 111
Finding vc
./dump.vcc
[2023-09-
Done
```

Arrows indicate the configuration steps:

- Arrow 1 points to the **Open EPWave after run** checkbox.
- Arrow 2 points to the **Download files after run** checkbox.

El resto de los parámetros no se modifican.

- 1.- En primera instancia dejar elegida la opción Open EPWare after run, con el propósito de obtener las formas de onda digitales del circuito de este ejemplo
- 2.- Enseguida conviene bajar los archivos después de la ejecución y guardarlos en una carpeta ad-hoc

Al ejecutar el punto 2 se obtienen dos archivos de nuestro interés inmediato:

```
//design.sv
module analisis(A,B,C,F1,F2);
  input A,B,C;
  output F1,F2;
  wire T1,T2,T3,F2not,E1,E2,E3;
  or g1(T1,A,B,C);
  and g2(T2,A,B,C);
  and g3(E1,A,B);
  and g4(E2,A,C);
  and g5(E3,B,C);
  or g6(F2,E1,E2,E3);
  not g7(F2not,F2);
  and g8(T3,T1,F2not);
  or g9(F1,T2,T3);
endmodule
```

```
//test bench
module probar_circuito;
  reg[2:0]D;
  wire F1,F2;
  analisis cto(D[2], D[1], D[0],F1,F2);
  initial
    begin
      D=3'b000;
      repeat(7)
        #10 D=D+1'b1;
      end
  initial
    begin
      $monitor("ABC = %b F1 = %b F2 = %b",D,F1,F2);
      $dumpfile("dump.vcd");
      $dumpvars(1);
    end
endmodule
```

## Resultados del análisis

```
4 while F1,F2,  
5 analisis cto(D[2], D[1], D[0],F1,F2);  
6 initial
```

[Log](#)[Share](#)

[2023-09-14 21:15:09 UTC] iverilog '-wall' '-g2012'

VCD info: dumpfile dump.vcd opened for output.

ABC = 000 F1 = 0 F2 = 0

ABC = 001 F1 = 1 F2 = 0

ABC = 010 F1 = 1 F2 = 0

ABC = 011 F1 = 0 F2 = 1

ABC = 100 F1 = 1 F2 = 0

ABC = 101 F1 = 0 F2 = 1

ABC = 110 F1 = 0 F2 = 1

ABC = 111 F1 = 1 F2 = 1

Creating result.zip...

adding: a.out (deflated 68%)

adding: dump.vcd (deflated 39%)

adding: testbench.sv (deflated 36%)

adding: design.sv (deflated 42%)

adding: run.sh (deflated 34%)

[2023-09-14 21:15:10 UTC] waiting for download...

Done

Diagrama de temporización

