### mux2\_1

Corso di ASE anno 18/19 Realizzato dal Gruppo 14

## **Contents**

1	Clas	s Index	1
	1.1	Class List	1
2	File	Index	3
	2.1	File List	3
3	Clas	s Documentation	5
	3.1	mux2_1 Entity Reference	5
		3.1.1 Detailed Description	5
	3.2	mux2_1_testbench Entity Reference	6
4	File	Documentation	7
	4.1	mux2_1.vhd File Reference	7
		4.1.1 Detailed Description	7
Inc	dex		9

## **Class Index**

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Here are the classes, structs, unions and interfaces with brief descriptions:	
entity mux2_1	ļ
entity mux2_1_testbench	(

2 Class Index

# File Index

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Here is a list of all documented files with brief descriptions:

mux2	_1.vhd								
	Mux2 1 describes a multiplex with 2 ingress and 1 output								7

File Index

## **Class Documentation**

### 3.1 mux2\_1 Entity Reference

#### Libraries

• IEEE

Use standard library.

#### **Use Clauses**

• STD\_LOGIC\_1164

Use logic elements.

#### **Ports**

• SEL in STD\_LOGIC

Mux select input.

A in STD\_LOGIC

Mux first input.

• B in STD\_LOGIC

Mux second input.

X out STD\_LOGIC

Mux output.

#### 3.1.1 Detailed Description

When SEL is low the output is the value of signal on input A, otherwise if select is high the output is the value of signal B

The documentation for this class was generated from the following file:

mux2\_1.vhd

6 Class Documentation

### 3.2 mux2\_1\_testbench Entity Reference

#### Libraries

• IEEE

#### **Use Clauses**

• STD\_LOGIC\_1164

The documentation for this class was generated from the following file:

• mux2\_1\_testbench.vhd

## **File Documentation**

### 4.1 mux2\_1.vhd File Reference

mux2\_1 describes a multiplex with 2 ingress and 1 output

#### **Entities**

• mux2\_1 entity

#### 4.1.1 Detailed Description

mux2\_1 describes a multiplex with 2 ingress and 1 output

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Date

15/10/2018

Version

0.1

8 File Documentation

# Index

```
mux2_1, 5
mux2_1.vhd, 7
mux2_1_testbench, 6
```