

carry\_select

Corso di ASE anno 18/19

Gruppo 14

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# Chapter 1

## Class Index

### 1.1 Class List

Here are the classes, structs, unions and interfaces with brief descriptions:

entity <a href="#">carry_select_adder</a> . . . . .	5
entity <a href="#">carry_select_block</a> . . . . .	6
entity <a href="#">carry_select_timing</a> Uncomment the following library declaration if instantiating any XilinX primitives in this code . . .	6
entity <a href="#">d_edge</a> . . . . .	7
entity <a href="#">full_adder</a> . . . . .	8
entity <a href="#">mux2_1</a> Definisco il componente e la sua interfaccia . . . . .	9
entity <a href="#">rippleCarry_adder</a> . . . . .	11



## Chapter 2

# File Index

### 2.1 File List

Here is a list of all documented files with brief descriptions:

<a href="#">carrySelect_adder.vhd</a>	
Sommatore Carry Select . . . . .	13
<a href="#">carrySelect_cell.vhd</a>	
Singolo blocco di un sommatore carry Select . . . . .	13





## Chapter 3

# Class Documentation

### 3.1 carry\_select\_adder Entity Reference

#### Libraries

- [IEEE](#)

#### Use Clauses

- [STD\\_LOGIC\\_1164](#)

#### Generics

- **M NATURAL:= 8**  
*parallelismo dei ripplecarry adder nei blocchi*
- **P NATURAL:= 8**  
*numero di blocchi del carry select*

#### Ports

- **A in STD\_LOGIC\_VECTOR(((M \*P)- 1 )downto 0 )**  
*input addendo*
- **B in STD\_LOGIC\_VECTOR(((M \*P)- 1 )downto 0 )**  
*input addendo*
- **c\_in in STD\_LOGIC**  
*input carry in ingresso*
- **S out STD\_LOGIC\_VECTOR(((M \*P)- 1 )downto 0 )**  
*output somma*
- **c\_out out STD\_LOGIC**  
*output carry in uscita*

The documentation for this class was generated from the following file:

- [carrySelect\\_adder.vhd](#)

## 3.2 carry\_select\_block Entity Reference

### Use Clauses

- [STD\\_LOGIC\\_1164](#)

### Generics

- [width](#) **NATURAL** := 4

### Ports

- [A](#) in **STD\_LOGIC\_VECTOR**((width- 1 )downto 0 )
- [B](#) in **STD\_LOGIC\_VECTOR**((width- 1 )downto 0 )
- [c\\_in](#) in **STD\_LOGIC**
- [S](#) out **STD\_LOGIC\_VECTOR**((width- 1 )downto 0 )
- [c\\_out](#) out **STD\_LOGIC**

### 3.2.1 Detailed Description

blocco carry select è formato da due RCA e due multiplexer 2-1. I due addizionatori si occuperanno di sommare le due stringhe in ingresso A e B (di lunghezza generica width) con c\_in pari, rispettivamente, a 0 e 1. In base al valore c\_in effettivo in ingresso al blocco, i due multiplexer sceglieranno quali dei due valori S e c\_out, calcolati dai due RCA, riportare in uscita.

The documentation for this class was generated from the following file:

- [carrySelect\\_cell.vhd](#)

## 3.3 carry\_select\_timing Entity Reference

Uncomment the following library declaration if instantiating any Xilinx primitives in this code.

### Libraries

- [IEEE](#)

### Use Clauses

- [STD\\_LOGIC\\_1164](#)

### Generics

- **M** **NATURAL** := 8  
*parallelismo dei ripplecarry adder nei blocchi*
- **P** **NATURAL** := 8

## Ports

- [clock](#) in STD\_LOGIC
- [A](#) in STD\_LOGIC\_VECTOR(([M](#) \* [P](#))- 1 downto 0 )
- [B](#) in STD\_LOGIC\_VECTOR(([M](#) \* [P](#))- 1 downto 0 )
- [c\\_in](#) in STD\_LOGIC
- [S](#) out STD\_LOGIC\_VECTOR(([M](#) \* [P](#))- 1 downto 0 )
- [c\\_out](#) out STD\_LOGIC

### 3.3.1 Detailed Description

Uncomment the following library declaration if instantiating any Xilinx primitives in this code.

Uncomment the following library declaration if using arithmetic functions with Signed or Unsigned values

### 3.3.2 Member Data Documentation

#### 3.3.2.1 IEEE

[IEEE](#) [Library]

Company: Engineer:

Create Date: 12:07:17 02/16/2019 Design Name: Module Name: [carry\\_select\\_timing](#) - Behavioral Project Name:  
Target Devices: Tool versions: Description:

#### 3.3.2.2 STD\_LOGIC\_1164

[STD\\_LOGIC\\_1164](#) [Package]

Revision: Revision 0.01 - File Created Additional Comments:

The documentation for this class was generated from the following file:

- [carry\\_select\\_timing.vhd](#)

## 3.4 d\_edge Entity Reference

### Libraries

- [ieee](#)

## Use Clauses

- [std\\_logic\\_1164](#)
- [all](#)

## Generics

- [width](#) **natural** := **8**

## Ports

- [clock](#) in **STD\_LOGIC**
- [D](#) in **STD\_LOGIC\_VECTOR**(width- **1** downto **0** )
- [Q](#) out **STD\_LOGIC\_VECTOR**(width- **1** downto **0** )

### 3.4.1 Member Data Documentation

#### 3.4.1.1 ieee

[ieee](#) [Library]

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#### 3.4.1.2 std\_logic\_1164

[std\\_logic\\_1164](#) [Package]

last changes: <14/11/2018> <13/11/2018> <log> create

The documentation for this class was generated from the following file:

- [d\\_edge\\_behav.vhd](#)

## 3.5 full\_adder Entity Reference

### Libraries

- [IEEE](#)

### Use Clauses

- [STD\\_LOGIC\\_1164](#)

## Ports

- **x in STD\_LOGIC**  
*full\_adder input : addendo*
- **y in STD\_LOGIC**  
*full\_adder input : addendo*
- **c\_in in STD\_LOGIC**  
*full\_adder input : carry in ingresso*
- **s out STD\_LOGIC**  
*full\_adder output : somma*
- **c\_out out STD\_LOGIC**  
*full\_adder output : carry*

### 3.5.1 Detailed Description

Descrizione Somma i 3 bit in ingresso (2 addendi e 1 carry in ingresso).  
In uscita abbiamo il risultato della somma sul bit S e il riporto sul bit C.

### 3.5.2 Member Data Documentation

#### 3.5.2.1 IEEE

IEEE [Library]

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#### 3.5.2.2 STD\_LOGIC\_1164

STD\_LOGIC\_1164 [Package]

last changes: <11/11/2018> <15/10/2018> <log> Aggiunta doc doxygen

The documentation for this class was generated from the following file:

- full\_adder.vhd

## 3.6 mux2\_1 Entity Reference

definisco il componente e la sua interfaccia

## Libraries

- IEEE

## Use Clauses

- [STD\\_LOGIC\\_1164](#)

## Generics

- **width natural:= 1**  
*parallelismo dell' I/O del multiplexer*

## Ports

- **SEL in STD\_LOGIC**  
*mux2\_1 input: selezione*
- **A in STD\_LOGIC\_VECTOR((width - 1)downto 0 )**  
*mux2\_1 input: A*
- **B in STD\_LOGIC\_VECTOR((width - 1)downto 0 )**  
*mux2\_1 input: B*
- **X out STD\_LOGIC\_VECTOR((width - 1)downto 0 )**  
*mux2\_1 output: X*

### 3.6.1 Detailed Description

definisco il componente e la sua interfaccia

Descrizione Quando l'ingresso SEL è basso, l'uscita assume il valore del segnale A, altrimenti quando il segnale SEL è alto l'uscita assume il valore del segnale B.

### 3.6.2 Member Data Documentation

#### 3.6.2.1 IEEE

[IEEE](#) [Library]

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#### 3.6.2.2 STD\_LOGIC\_1164

[STD\\_LOGIC\\_1164](#) [Package]

last changes: <14/11/2018> <13/11/2018> <log> create

The documentation for this class was generated from the following file:

- mux2\_1.vhd

## 3.7 rippleCarry\_adder Entity Reference

### Libraries

- [IEEE](#)

*architecture dataflow of [mux2\\_1](#) end*

### Use Clauses

- [STD\\_LOGIC\\_1164](#)

### Generics

- [width](#) **NATURAL** := 8

### Ports

- [X](#) in **STD\_LOGIC\_VECTOR**([width](#) - 1 downto 0 )
- [Y](#) in **STD\_LOGIC\_VECTOR**([width](#) - 1 downto 0 )
- [c\\_in](#) in **STD\_LOGIC**
- [S](#) out **STD\_LOGIC\_VECTOR**([width](#) - 1 downto 0 )
- [c\\_out](#) out **STD\_LOGIC**

*rippleCarry\_adder output: carry*

### 3.7.1 Detailed Description

Descrizione Somma le 2 stringe di bit in ingresso (2 addendi ) e 1 bit (carry in ingresso). Caratterizzato da una serie di [full\\_adder](#) in cascata che propagano il riporto.

In uscita abbiamo il risultato della somma sul bit S e il riporto sul bit C.

### 3.7.2 Member Data Documentation

#### 3.7.2.1 c\_in

[c\\_in](#) in **STD\_LOGIC** [Port]

[rippleCarry\\_adder](#) input: addendo

#### 3.7.2.2 c\_out

[c\\_out](#) out **STD\_LOGIC** [Port]

[rippleCarry\\_adder](#) output: carry

[rippleCarry\\_adder](#) output: somma

### 3.7.2.3 S

`S out STD_LOGIC_VECTOR(width - 1 downto 0 )` [Port]

`rippleCarry_adder` input : carry in ingresso

### 3.7.2.4 STD\_LOGIC\_1164

`STD_LOGIC_1164` [Package]

last changes: <11/11/2018> <15/10/2018> <log> Aggiunta doc doxygen

### 3.7.2.5 width

`width NATURAL:= 8` [Generic]

usato per definire il parallelismo del `rippleCarry_adder`

### 3.7.2.6 Y

`Y in STD_LOGIC_VECTOR(width - 1 downto 0 )` [Port]

`rippleCarry_adder` input: addendo

The documentation for this class was generated from the following file:

- `rippleCarry_adder.vhd`



## Chapter 4

# File Documentation

### 4.1 carrySelect\_adder.vhd File Reference

Sommatore Carry Select.

#### Entities

- [carry\\_select\\_adder](#) entity

#### 4.1.1 Detailed Description

Sommatore Carry Select.

#### Author

Gabriele Previtera, Mirko Pennone, Simone Penna

#### Date

04/03/2019

#### Version

0.2

#### Dependencies:

Nothings

### 4.2 carrySelect\_cell.vhd File Reference

Singolo blocco di un sommatore carry Select.

## Entities

- [carry\\_select\\_block](#) entity

### 4.2.1 Detailed Description

Singolo blocco di un sommatore carry Select.

#### Author

Gabriele Previtera, Mirko Pennone, Simone Penna

#### Date

04/03/2019

#### Version

0.2

#### Dependencies:

Nothings

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