Test_clock

Corso di ASE anno 18/19

Gruppo 14
PREVITERA GABRIELE
PENNONE MIRKO
PENNA SIMONE

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2.1 File List

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Class Documentation

3.1 clk_tester Entity Reference

Libraries

- IEEE

Use Clauses

- STD_LOGIC_1164

Generics

- N **integer:=** 8

Ports

- clock_in **in STD_LOGIC**
- enable **in STD_LOGIC**
- reset_n **in STD_LOGIC**
- d_in **in STD_LOGIC**
- q_out **out STD_LOGIC**
- Q **out STD_LOGIC_VECTOR(N-** 1 **downto** 0 **)**
- half_clock **out STD_LOGIC**
- quarter_clock **out STD_LOGIC**
- tenth_clock **out STD_LOGIC**
- locked **out STD_LOGIC**

The documentation for this class was generated from the following file:

- clock_tester.vhd

3.2 left_right_shift_register Entity Reference

Libraries

- IEEE

Use Clauses

- STD_LOGIC_1164

Generics

- N **integer:=** 8

Ports

- clock **in STD_LOGIC**
- enable **in STD_LOGIC**
- reset_n **in STD_LOGIC**
- left **in STD_LOGIC**
- d_in **in STD_LOGIC**
- q_out **out STD_LOGIC**
- Q **out STD_LOGIC_VECTOR(N-** 1 **downto** 0 **)**

The documentation for this class was generated from the following file:

- left_right_shift_register.vhd

3.3 my_clock Entity Reference

Libraries

- ieee
- unisim

Use Clauses

- std_logic_1164

  __primary_____100.000_____0.010
- std_logic_unsigned
- std_logic_arith
- numeric_std
- vcomponents

Ports

- CLK_IN1 **in std_logic**

  Clock in ports.
- CLK_OUT1 **out std_logic**

  Clock out ports.
- CLK_OUT2 **out std_logic**
- CLK_OUT3 **out std_logic**
- LOCKED **out std_logic**

  Status and control signals.

3.3.1 Member Data Documentation

3.3.1.1 ieee

```
ieee  [Library]
```

file: my_clock.vhd

The documentation for this class was generated from the following file:

- my_clock.vhd

Chapter 4

File Documentation

4.1 left_right_shift_register.vhd File Reference

Registro a scorrimento con ingresso seriale e uscita seriale e parallela. se left = '1' shifta a sinistra se left = '0' shifta a destra.

Entities

- left_right_shift_register entity

4.1.1 Detailed Description

Registro a scorrimento con ingresso seriale e uscita seriale e parallela. se left = '1' shifta a sinistra se left = '0' shifta a destra.

Author

Gabriele Previtera, Mirko Pennone, Simone Penna

Date

04/03/2019

Version

0.2

Dependencies:
Nothings

4.2 my_clock.vhd File Reference

Clock generato tramite Wizard.

Entities

- my_clock entity

4.2.1 Detailed Description

Clock generato tramite Wizard.

Author

Gabriele Previtera, Mirko Pennone, Simone Penna

Date

04/03/2019

Version

0.2

Dependencies:
Nothings

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