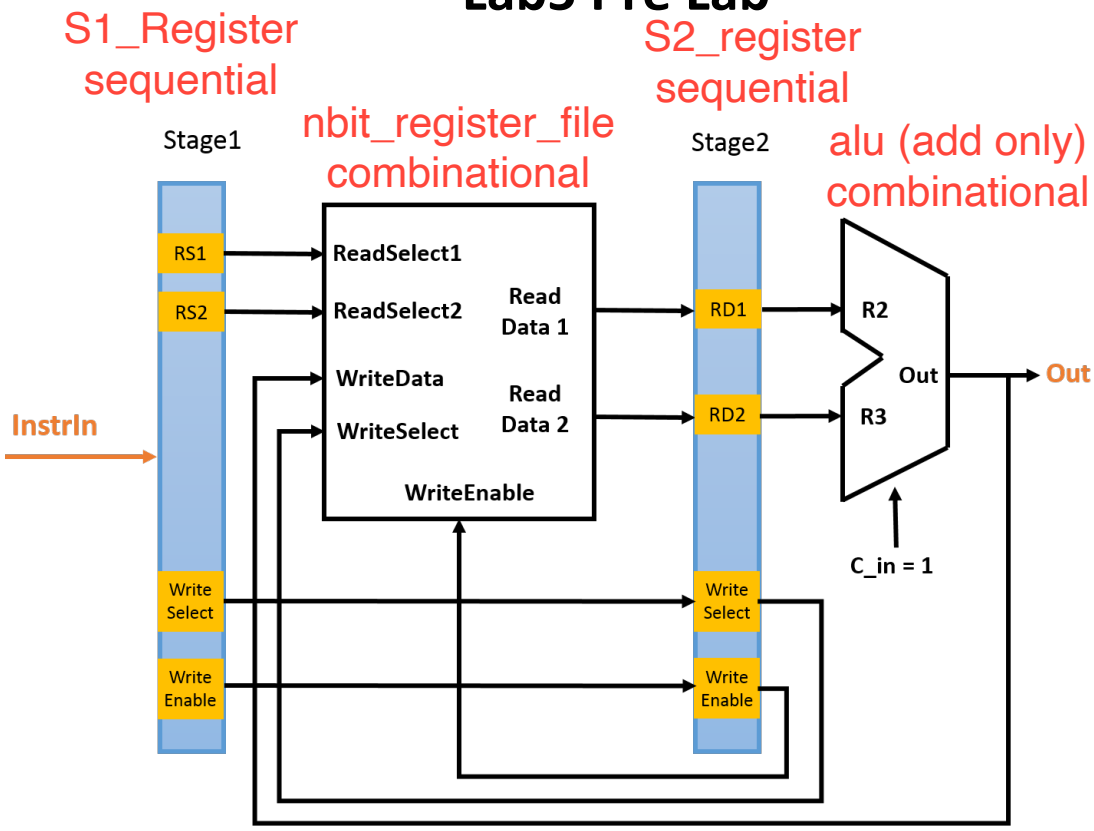
Lab5 Pre Lab



Part of the Lab 5 datapath is shown above. The design and testbench will be distributed in class.

Note: The register values are initialized to be 10x the register number to make value changes more apparent. For example, R1 = 10, R3 = 30, etc. For the prelab, this is hardwired in the register file.

The ALU in this design is simplified – only "add" is implemented – so the opcode is a "don't care."

The format of input instructions is as follows:

Type	**31**	**format (bits)**			**0**
R	OPCODE (NA)	R1(5)	R2(5)	R3(5)	

1. Simulate the design, watch the value changing in datapath with respect to timing.
2. Modify the input instructions in the testbench to use different input and output registers and perform simulation. Again observe and confirm the changes. Fill in the values in the spreadsheet.
3. Submit the new testbench and spreadsheet.