EC413 DISCUSSION 9

Hafsah Shahzad

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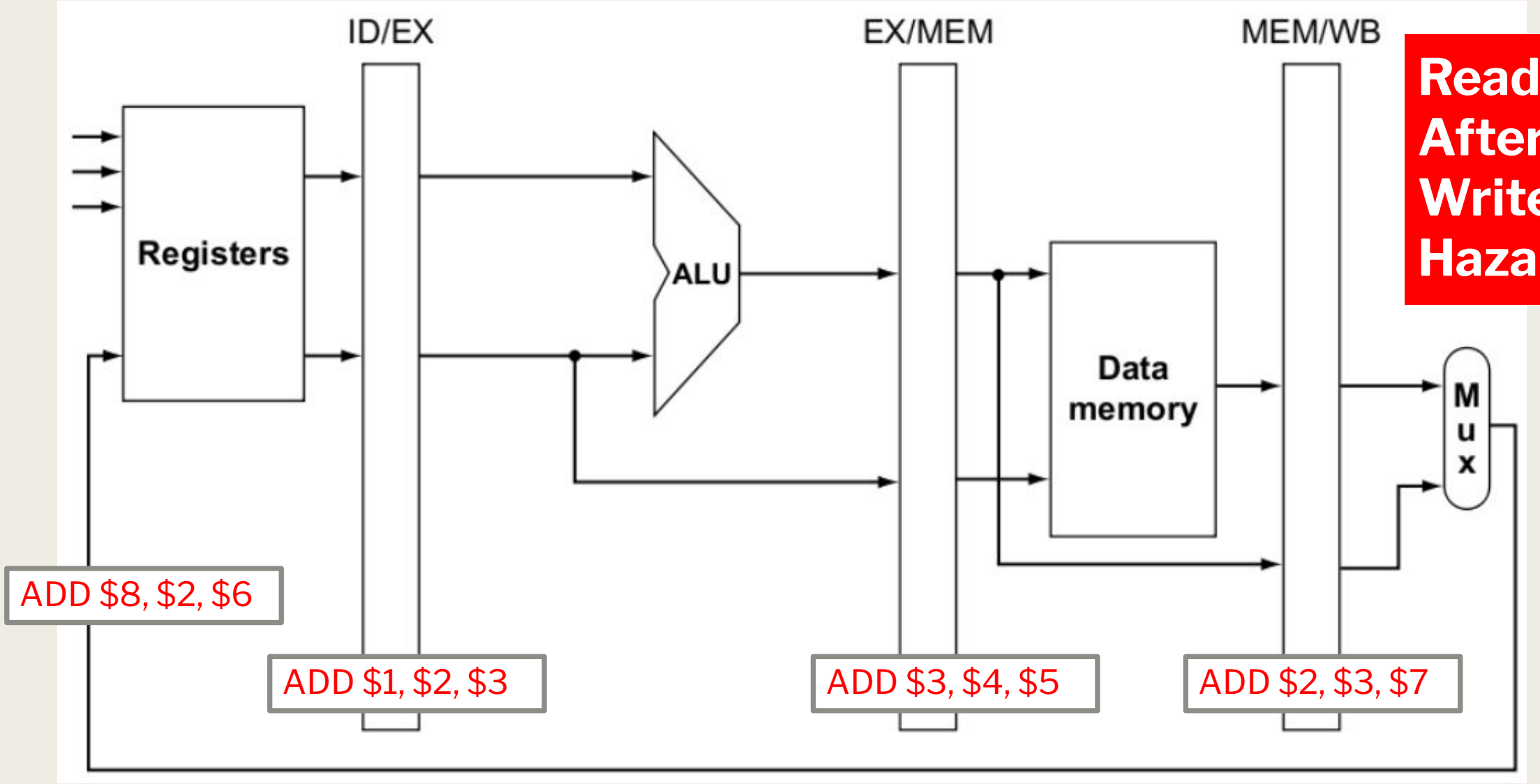
Running Vivado

In a terminal (on eng-grid) type the following:

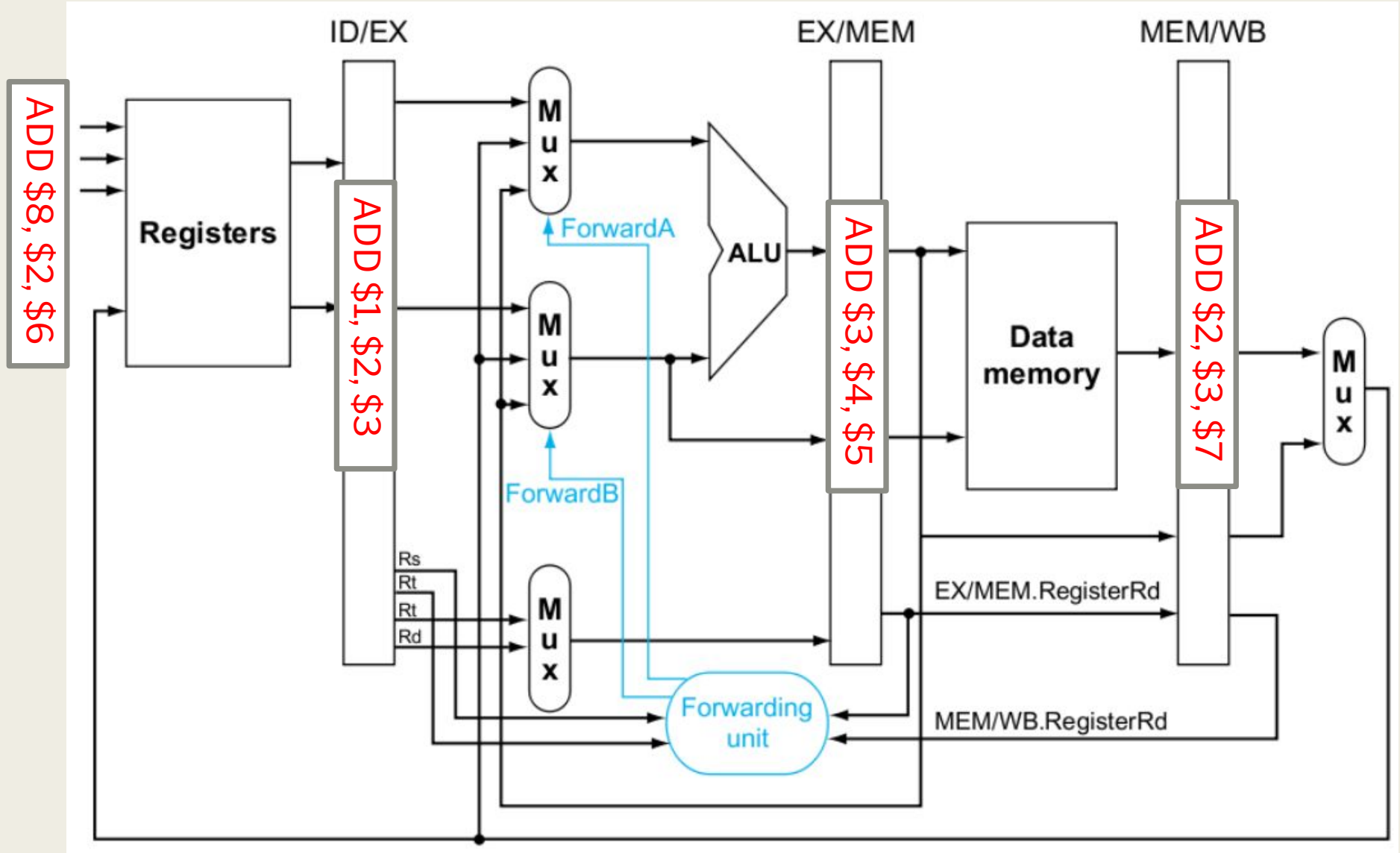
- source /ad/eng/opt/xilinx/Vivado/2019.1/settings64.sh
- vivado

Data Hazards

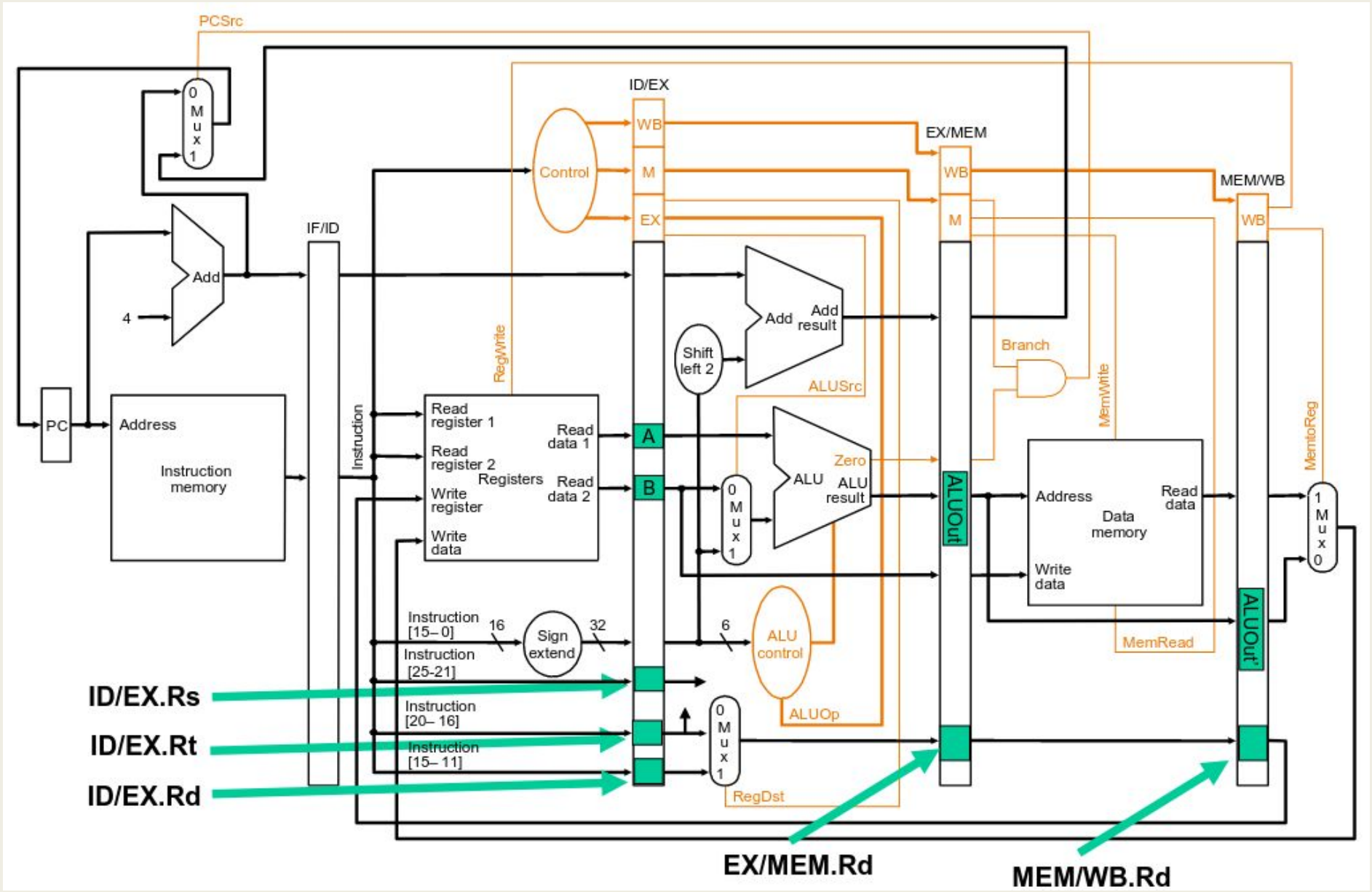


Read After Write Hazard!

One Solution: Data Forwarding

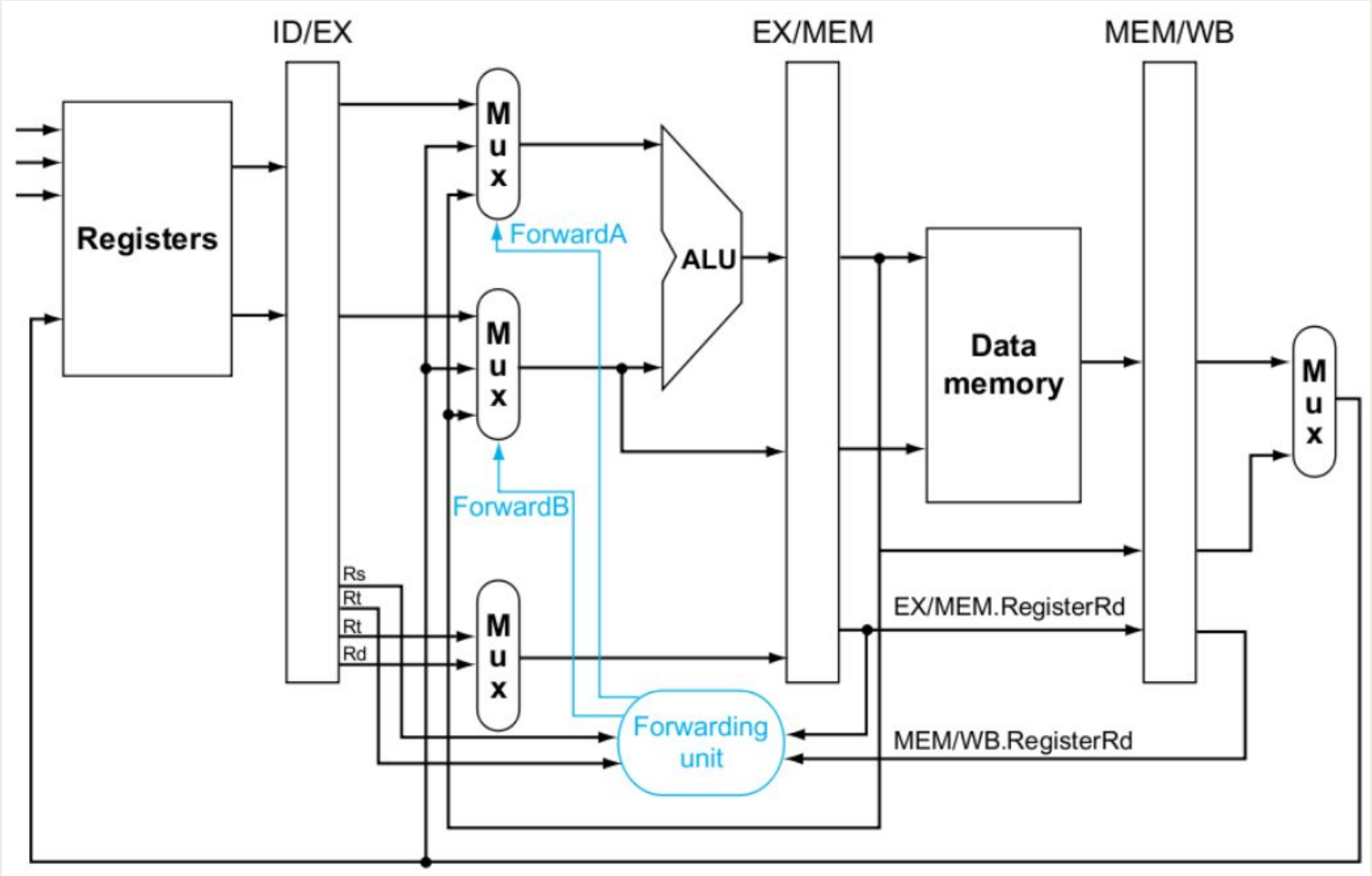


Processor Pipeline



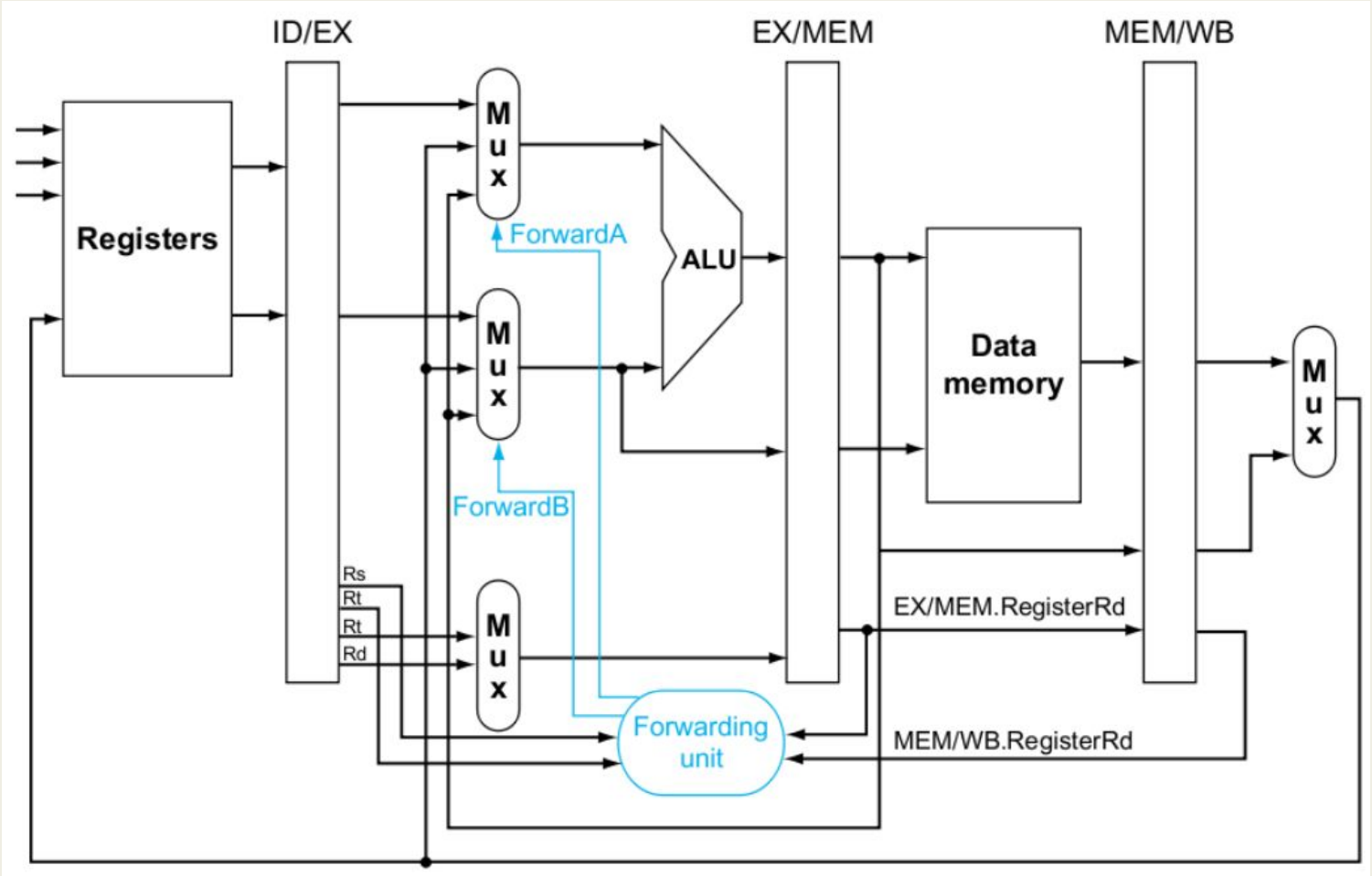
“1 Ahead” Forwarding

- (EX/MEM).Rd is the same as:
  - *(ID/EX).Rs*
  - *(ID/EX).Rt*

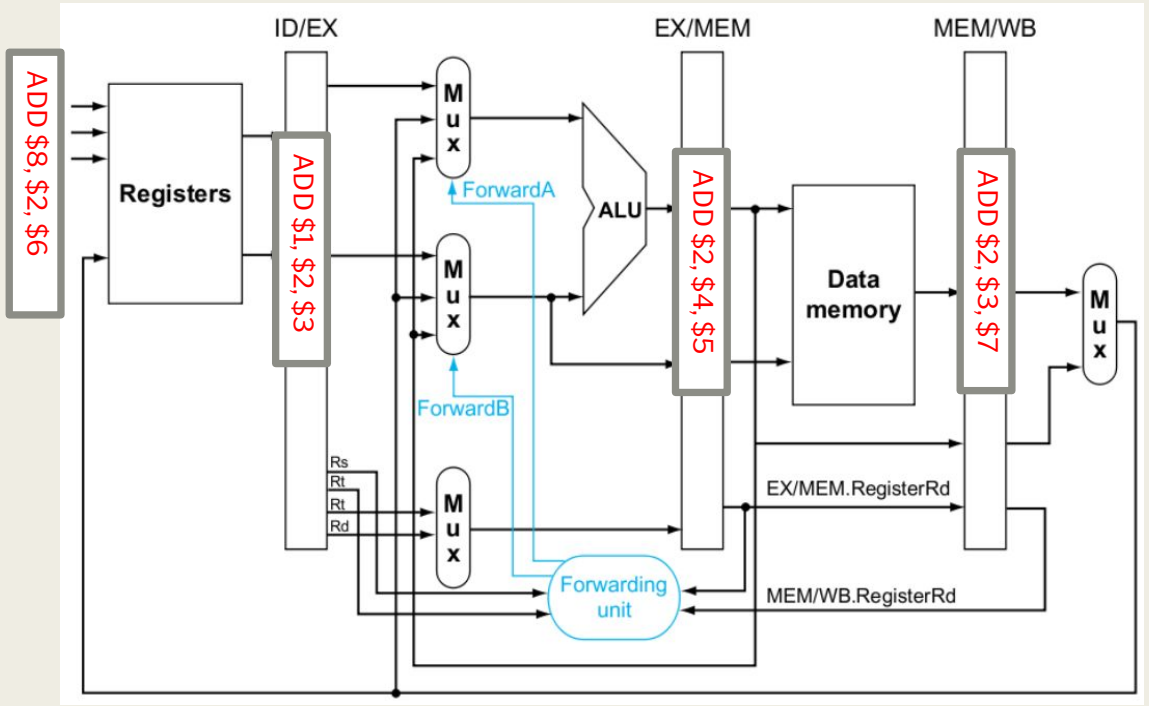


“2 Ahead” Forwarding

- (MEM/WB).Rd is the same as:
  - *(ID/EX).Rs*
  - *(ID/EX).Rt*



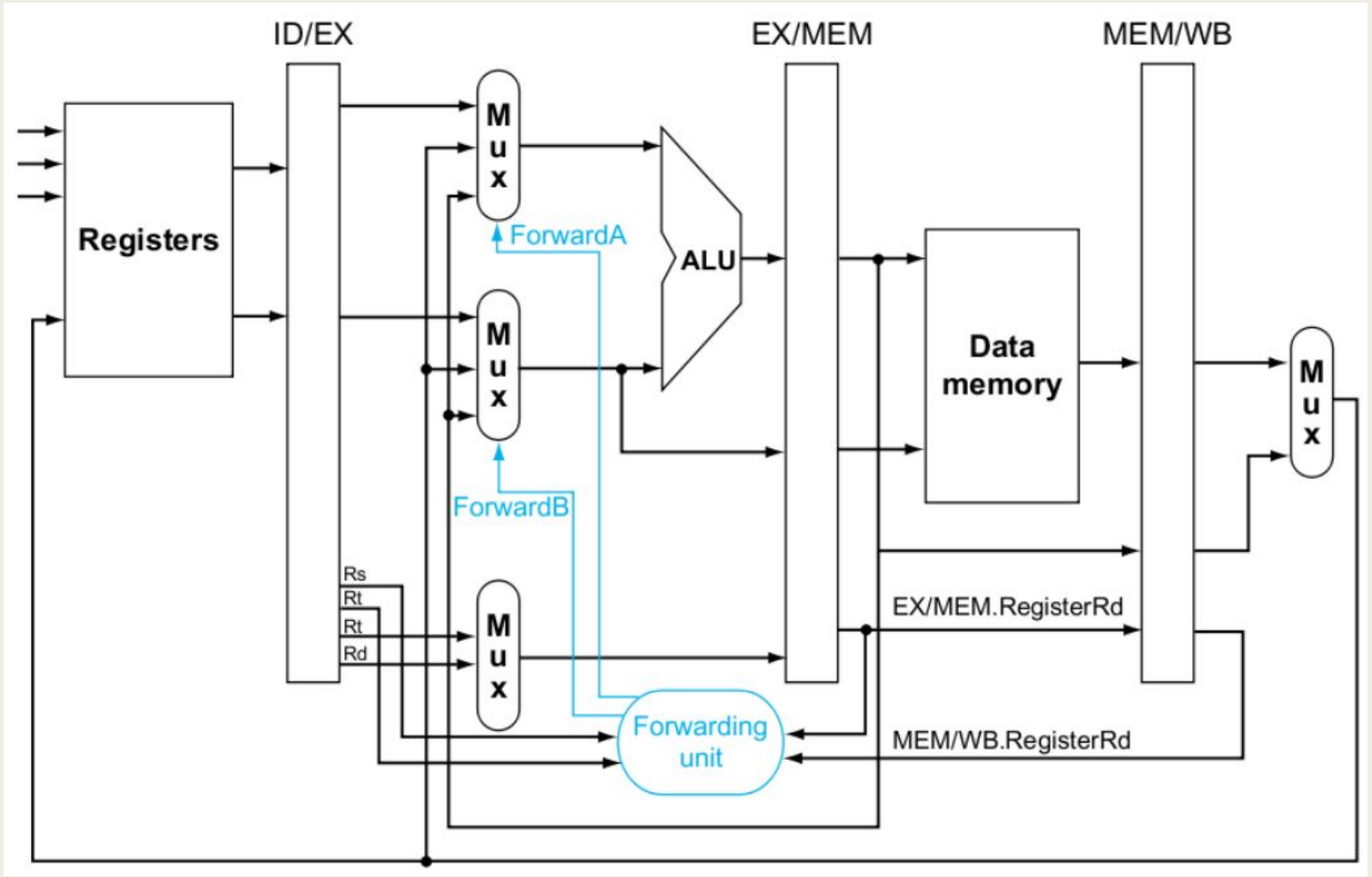
Arbitration between 1 and 2 ahead




```
ForwardA = ForwardB = 00          //initialize
IF (EX/MEM.RegisterRd == ID/EX.RegisterRs) ForwardA = 10
IF (EX/MEM.RegisterRd == ID/EX.RegisterRt) ForwardB = 10
IF (EX/MEM.RegisterRd ~= ID/EX.RegisterRs &&
     MEM/WB.RegisterRd == ID/EX.RegisterRs) ForwardA = 01
IF (EX/MEM.RegisterRd ~= ID/EX.RegisterRt &&
     MEM/WB.RegisterRd == ID/EX.RegisterRt) ForwardB = 01
```

(Rd == $0) ?

- $0 is hardwired to zero
- (Rd == 0) ?
  - *Do not forward*

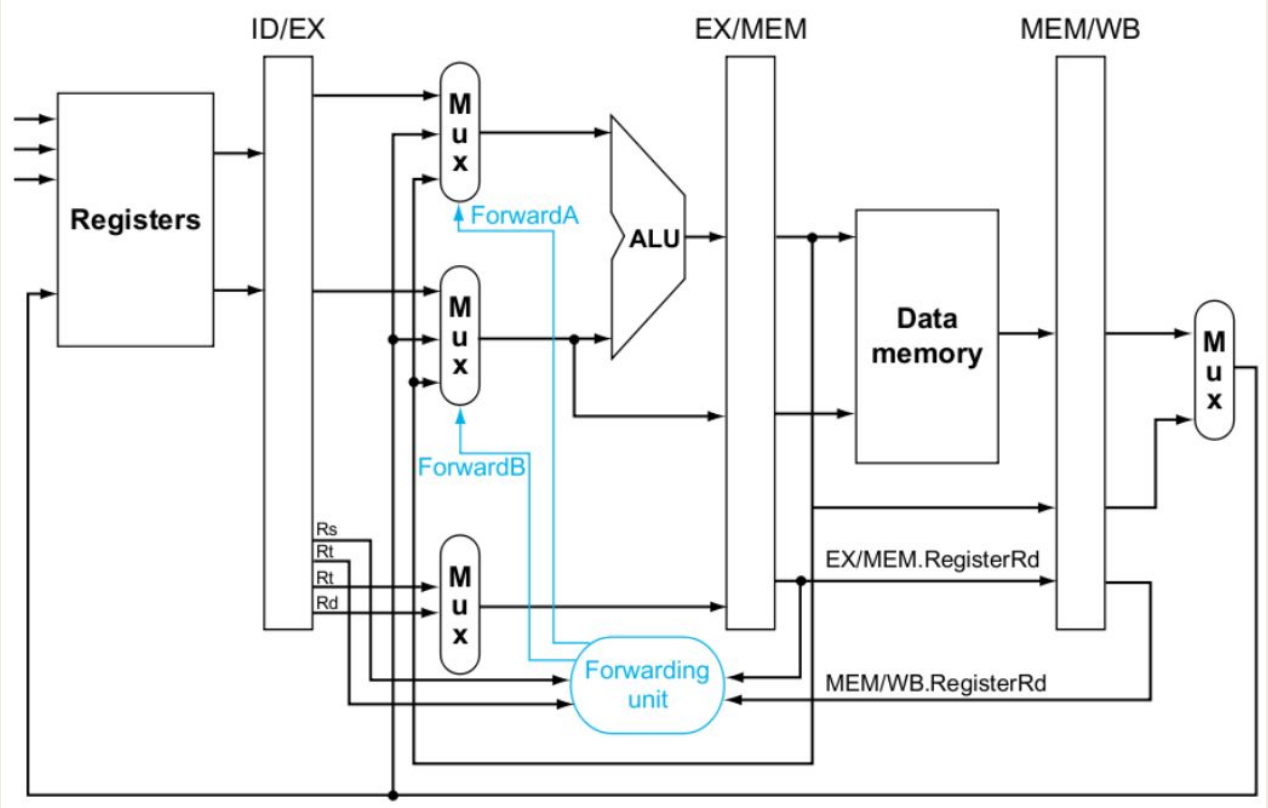


No write

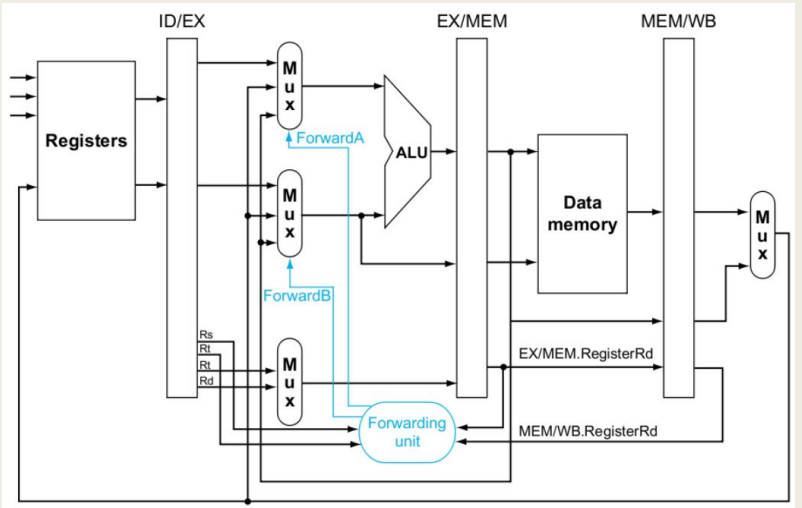
Q1: What if the instruction doesn't write to the RF?
Can't tell from looking at register number.

A: ***Can*** tell from RegWrite flag.

- (EX/MEM).RegWrite == 0
  - *No 1 ahead forwarding*
- (MEM/WB).RegWrite == 0
  - *No 2 ahead forwarding*



Hazard Detection Unit

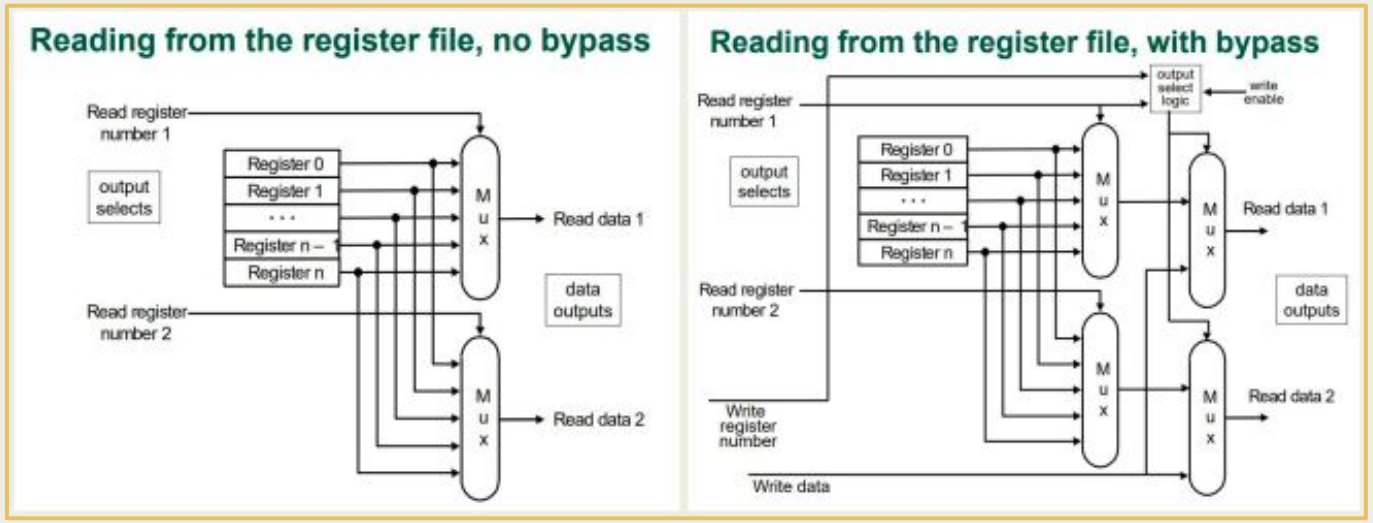



```
ForwardA = ForwardB = 00                                    //initialize
IF (EX/MEM.RegWrite && EX/MEM.RegisterRd ~= 0 &&
    EX/MEM.RegisterRd == ID/EX.RegisterRs) ForwardA = 10
IF (EX/MEM.RegWrite && EX/MEM.RegisterRd ~= 0 &&
    EX/MEM.RegisterRd == ID/EX.RegisterRt) ForwardB = 10
IF (MEM/WB.RegWrite && MEM/WB.RegisterRd ~= 0 &&
     EX/MEM.RegisterRd ~= ID/EX.RegisterRs &&
     MEM/WB.RegisterRd == ID/EX.RegisterRs) ForwardA = 01
IF (MEM/WB.RegWrite && MEM/WB.RegisterRd ~= 0 &&
     EX/MEM.RegisterRd ~= ID/EX.RegisterRt &&
     MEM/WB.RegisterRd == ID/EX.RegisterRt) ForwardB = 01
```

Later: **no need to check *earlier***

Earlier: **need to check *later***

Register Bypass




```
always @(ReadReg1 or ReadReg2 or WriteRegister or WriteData)
  begin
     ReadData1 = Reg_File[ReadReg1];
     ReadData2 = Reg_File[ReadReg2];
     //Register File Write Through
     if (ReadReg1 == WriteRegister && (ReadReg1 != 0) )
       ReadData1 = WriteData;
     if (ReadReg2 == WriteRegister && (ReadReg2 != 0) )
       ReadData2 = WriteData;
  end
```

Extra Credit

- Read After Write (RAW) hazard

  ADD $1, $2, $3
  ADD $4, $4, $1

- RAW following LW

  LW $1, 10($2)
  ADD $4, $4, $1

- RAW (LW followed by SW)

  LW $1, 10($2)
  SW $1, 0($4)