EC413 DISCUSSION 7

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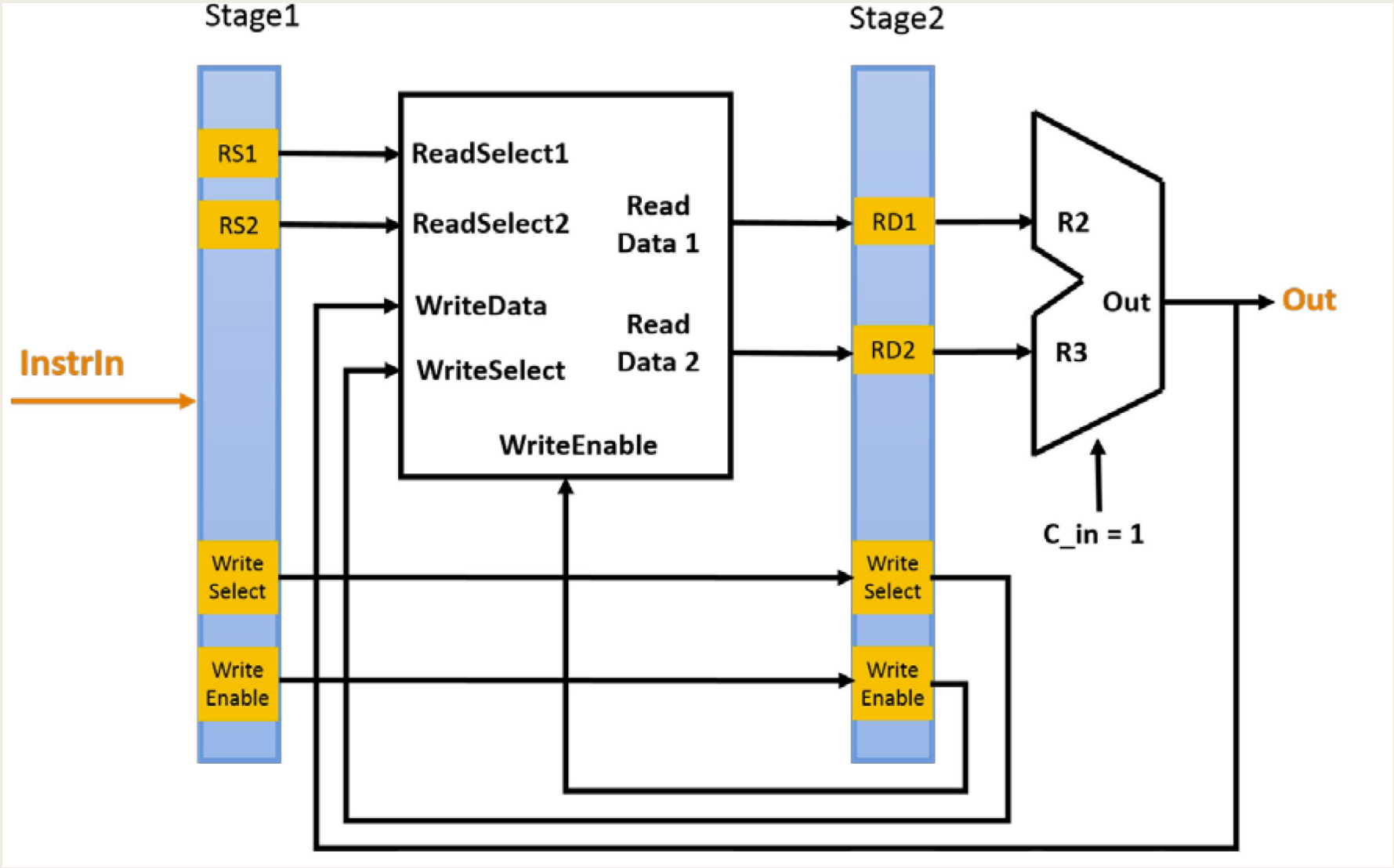
Running Vivado

In a terminal (on eng-grid) type the following:

- source /ad/eng/opt/xilinx/Vivado/2019.1/settings64.sh
- vivado

Lab 5 Prelab: 2-stage Pipeline



Lab 5 Prelab

- Instruction format

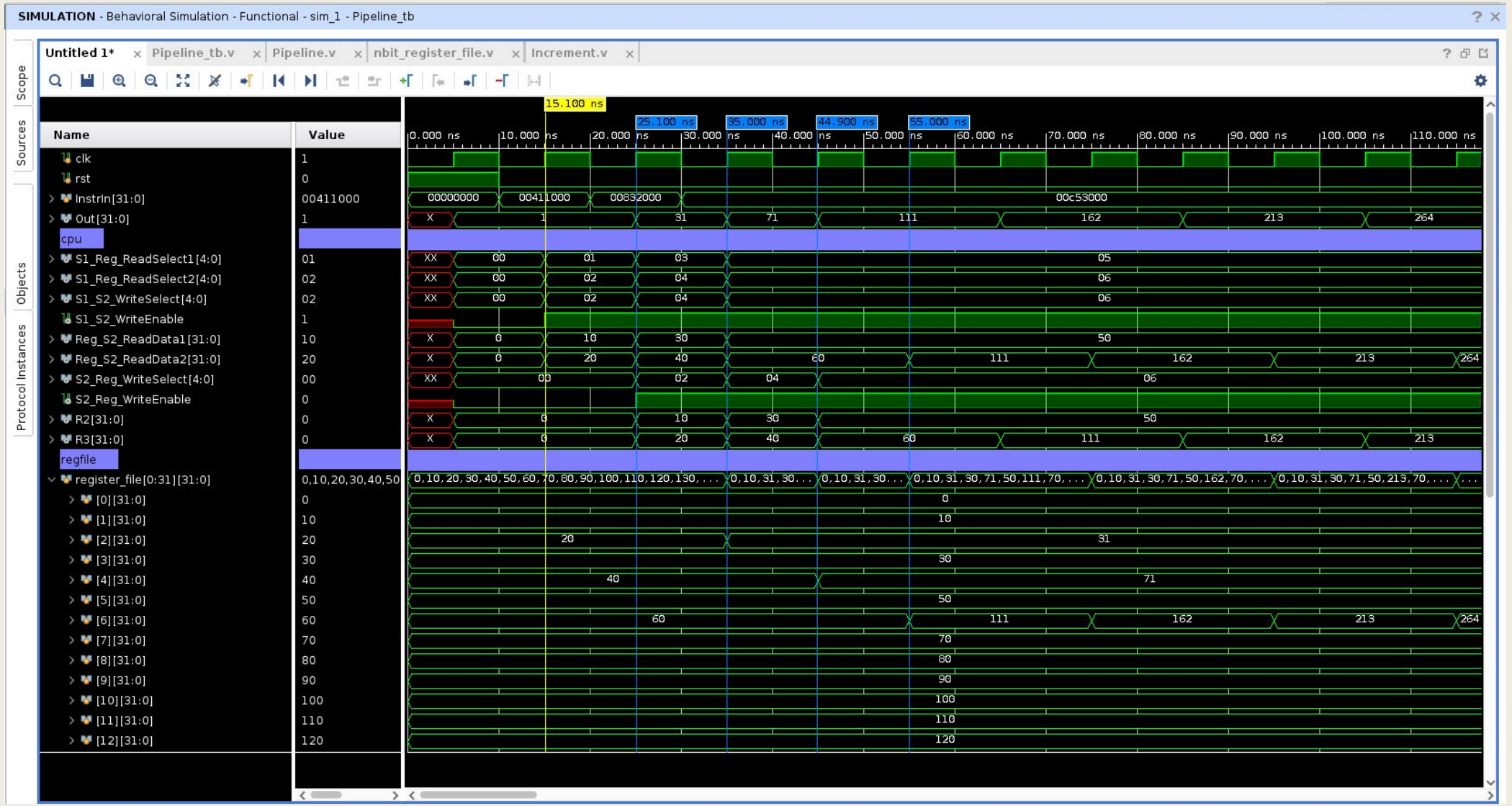
Type	31		format (bits)		0
R	OPCODE (NA)	R1(5)	R2(5)	R3(5)	

- Register values (10 x register number)

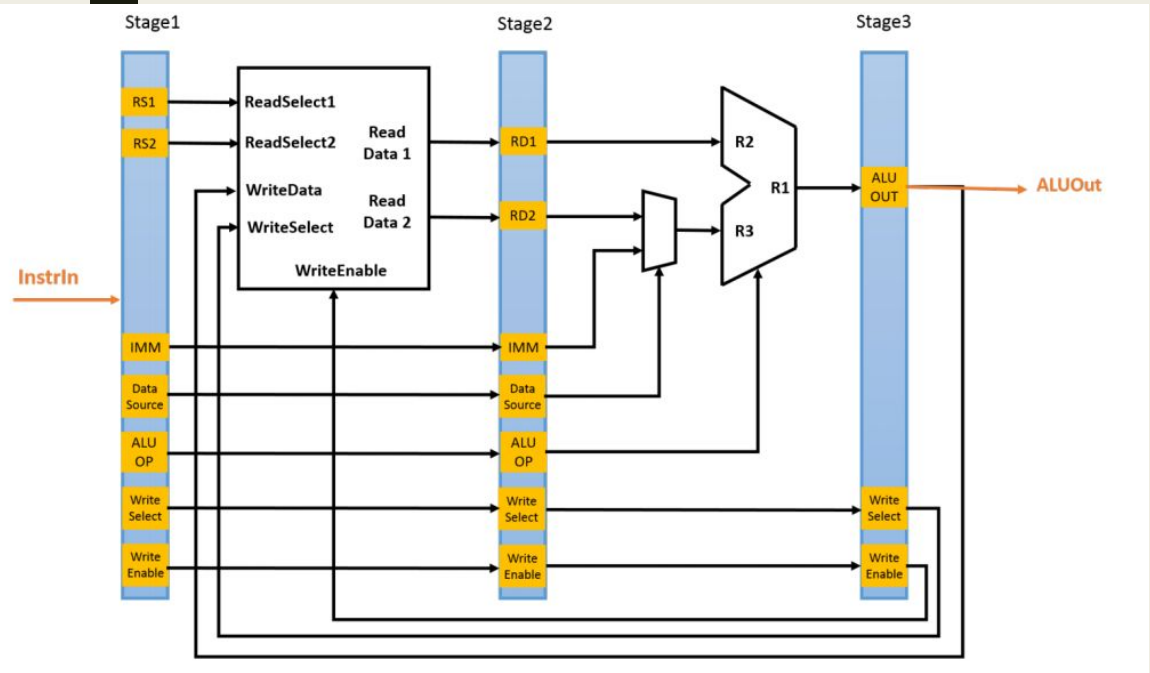
0	0
1	10
2	20
….	
31	310

- ALU: Only ADD implemented. (C_in = 1)

Lab 5 Prelab- **Understanding how data flows in a pipeline**



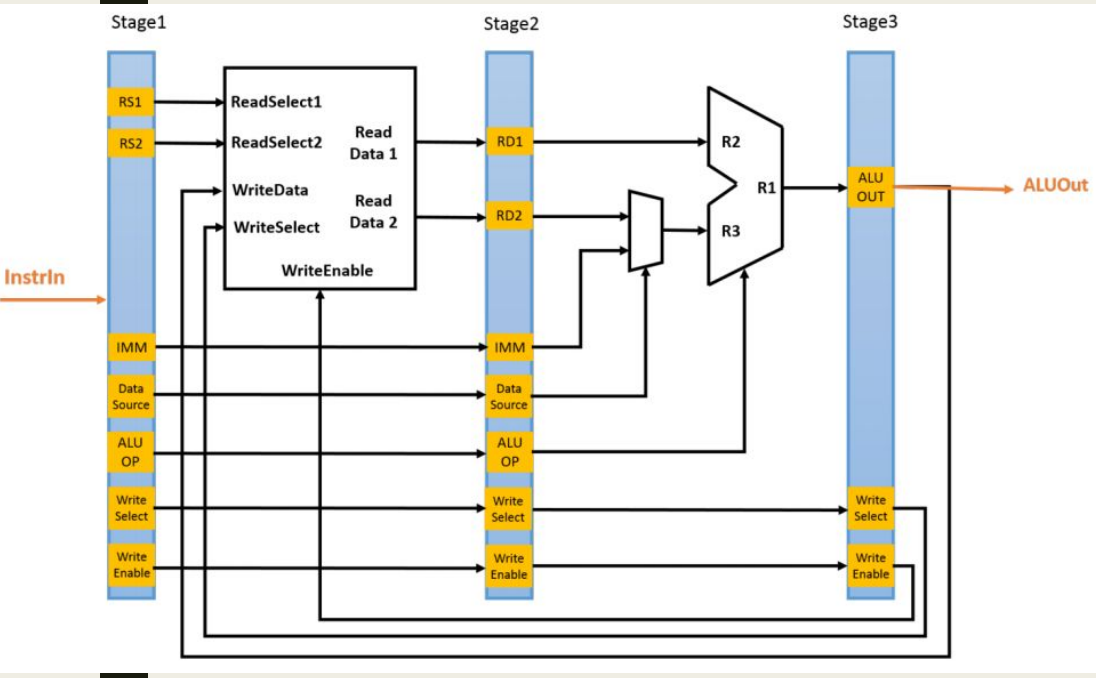
Datapath Execution Example



Register	Value
0	10010
1	11010
2	00100
3	00001
4	00111
5	10101
6	00000

	T1	T2	T3	T4	T5
Instruction	AND R6, R0, R1	ADDI R1, R2, 15	SLT R3, R4, R5	OR R0, R6, R0	SUB R2, R1, R2
Read Select 1	0	2	4	6	1
Read Select 2	1	3	5	0	2
ALU Op PR1	0000b (AND)	0010b (ADDI)	0111b (SLT)	0001b (OR)	0110b (SUB)
Read Data 1					
Read Data 2					
IMM PR1	10	15	11	13	16
Data Source PR1					
Write Select PR1	6	1	3	0	2
Write Enable PR1					
RD1 PR2	-				
RD2 PR2	-				
IMM PR2	-				
Data Source PR2	-				
R3	-				
ALU Op PR2	-				
R1	-				
Write Select PR2	-				
Write Enable PR2	-				
ALU OUT / Write Data	-	-			
Write Select PR3	-	-			
Write Enable PR3	-	-			

Datapath Execution Ex:**Soln**



Register	Value
0	10010
1	11010
2	00100
3	00001
4	00111
5	10101
6	00000

	T1	T2	T3	T4	T5
Instruction	AND R6, R0, R1	ADDI R1, R2, 15	SLT R3, R4, R5	OR R0, R6, R0	SUB R2, R1, R2
Read Select 1	0	2	4	6	1
Read Select 2	1	3	5	0	2
ALU Op PR1	0000b (AND)	0010b (ADDI)	0111b (SLT)	0001b (OR)	0110b (SUB)
Read Data 1	10010	00100	00111	10010	10011
Read Data 2	11010	00001	10101	10010	00100
IMM PR1	10	15	11	13	16
Data Source PR1	0	1	0	0	0
Write Select PR1	6	1	3	0	2
Write Enable PR1	1	1	1	1	1
RD1 PR2	-	10010	00100	00111	10010
RD2 PR2	-	11010	00001	10101	10010
IMM PR2	-	10	01111 (15)	11	13
Data Source PR2	-	0	1	0	0
R3	-	11010	01111	10101	10010
ALU Op PR2	-	AND	ADD	SLT	OR
R1	-	10010	10011	00001	10010
Write Select PR2	-	6	1	3	0
Write Enable PR2	-	1	1	1	1
ALU OUT / Write Data	-	-	10010	10011	00001
Write Select PR3	-	-	6	1	3
Write Enable PR3	-	-	1	1	1

Lab 5: 3-stage Pipeline