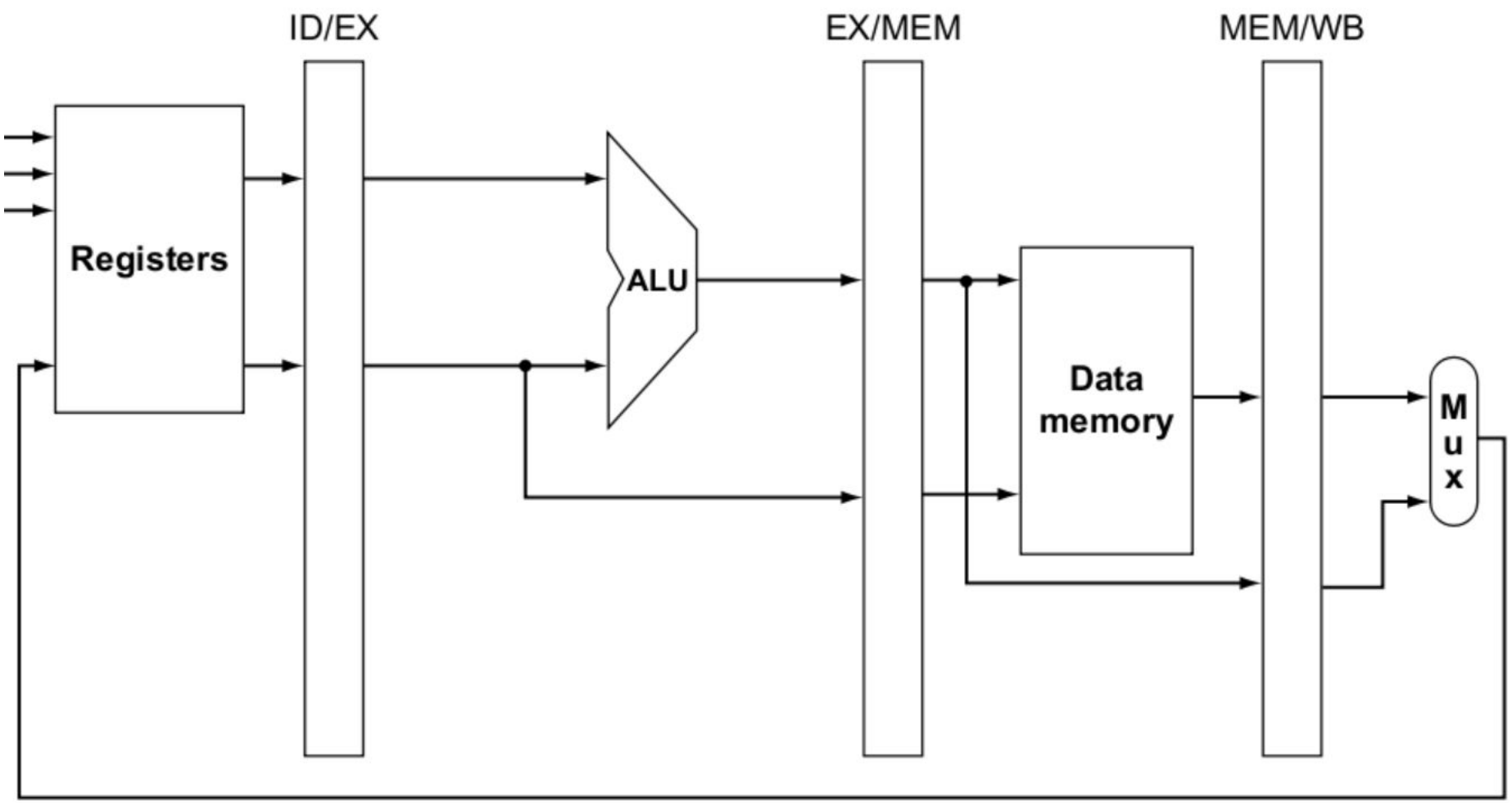
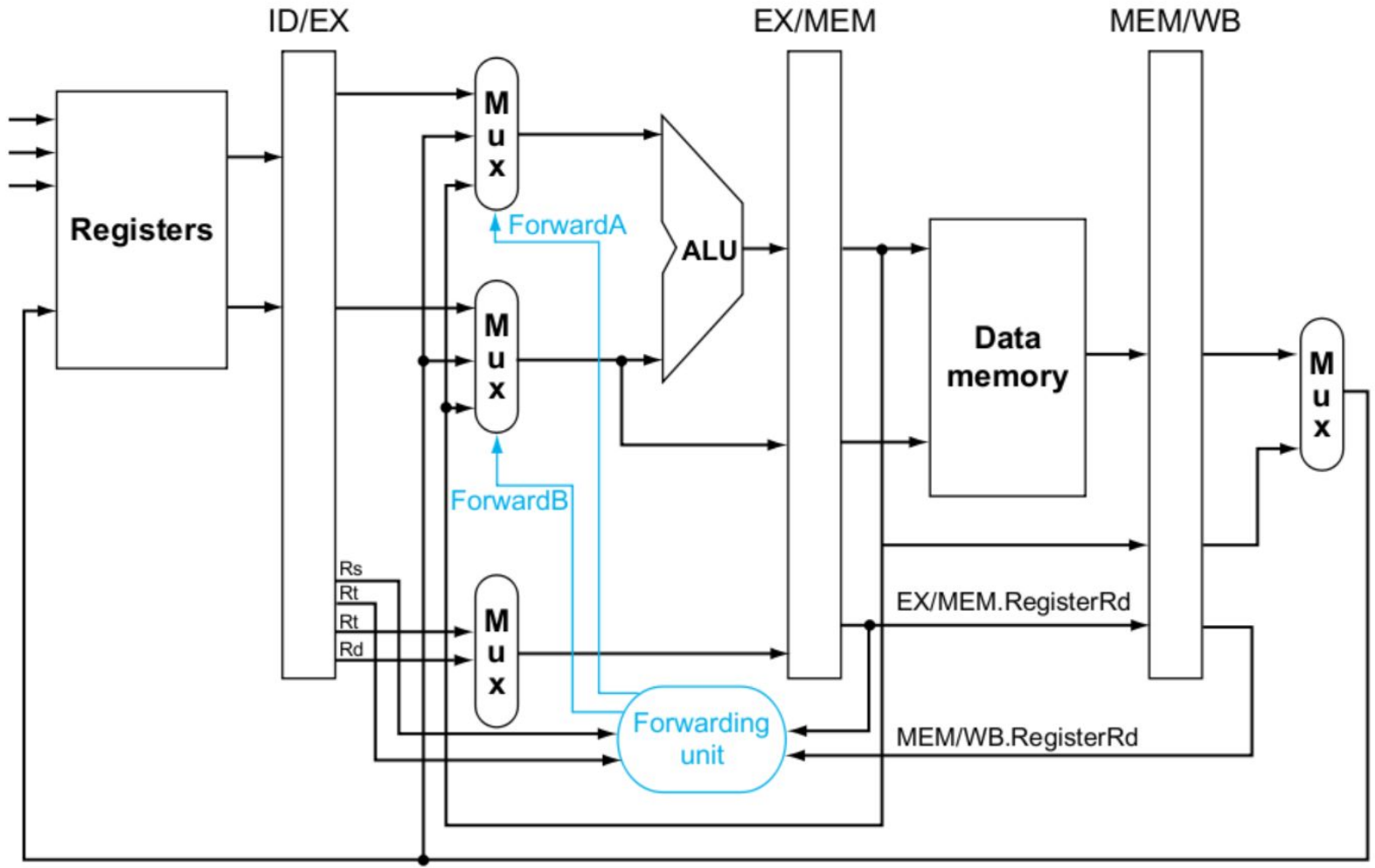
EC413 Discussion 9
Lab 7

Xiteng Yao



a. No forwarding



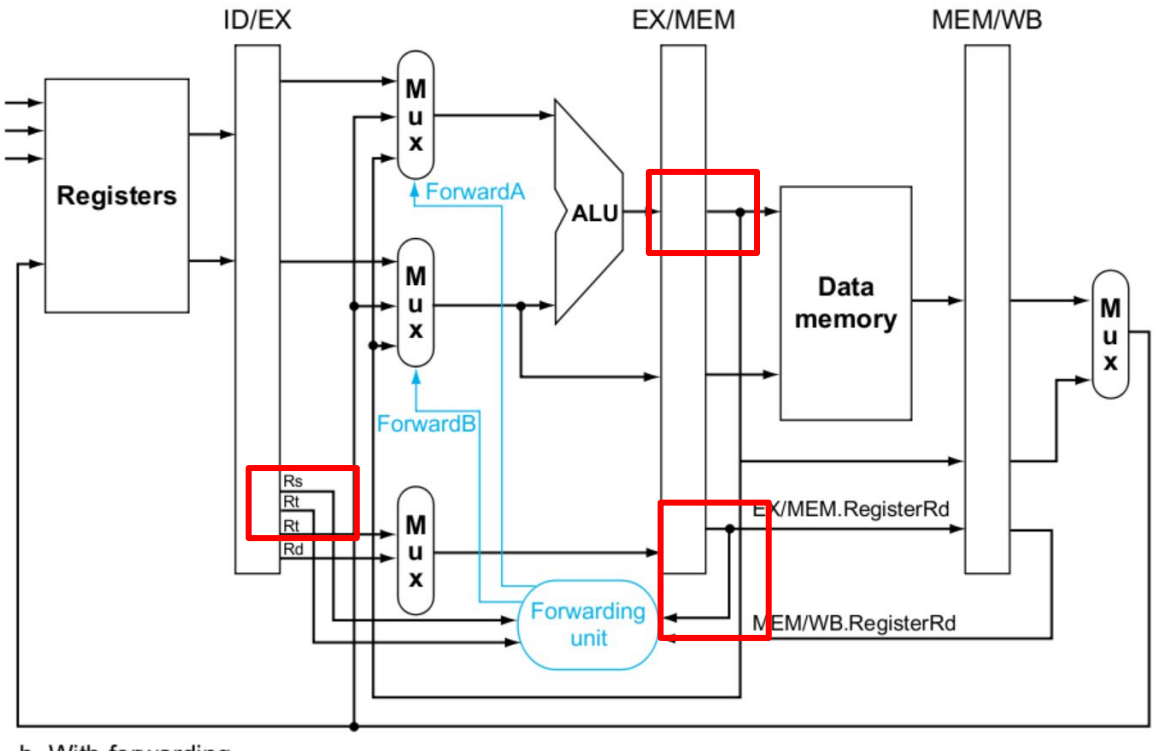
b. With forwarding

1 Ahead Forwarding

Implement a forwarding unit module

Checks if there is a regwrite at EX/MEM and check if the dest is Rs/Rt

If yes, forward output as input

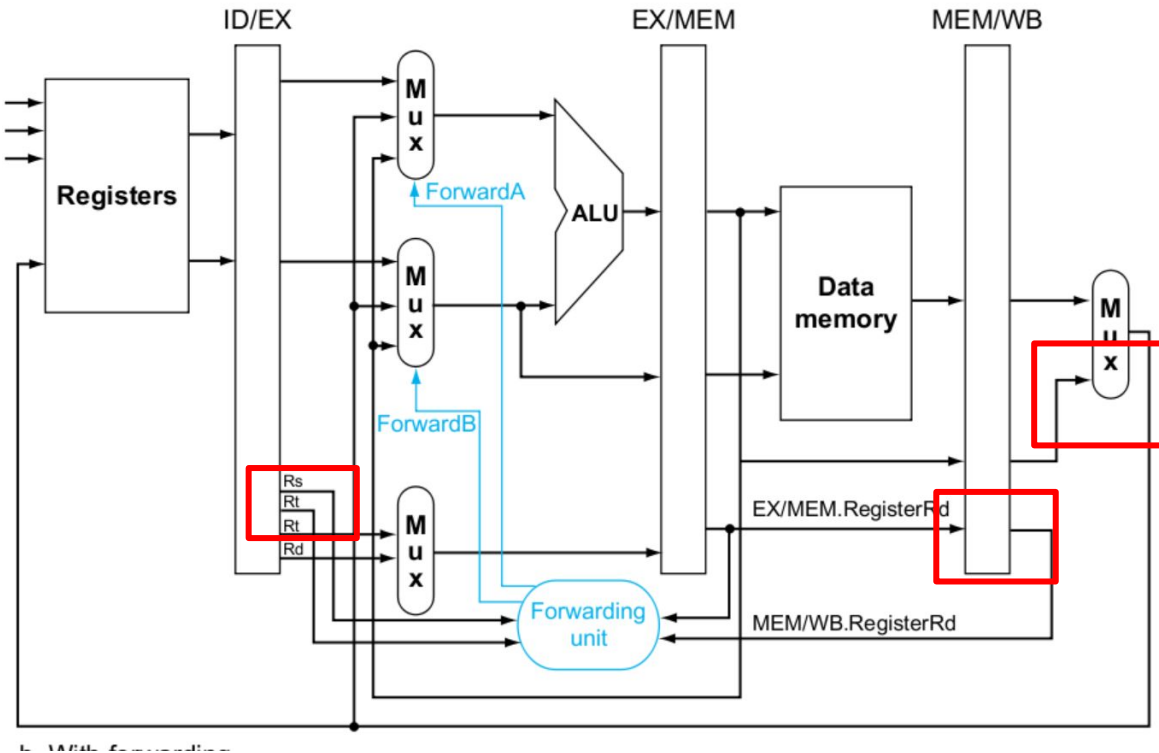


2 Ahead Forwarding

Similarly, add logics to the forwarding module

Now instead of checking the EX/MEM. Checks the MEM/WB stage.

Make sure that 1 and 2 ahead forwarding logics do not have any conflict.



Arbitration, $0 write logic, and No write

- Examine the logic in the forwarding unit so that it selects from the 1 and 2 ahead forwarding correctly
  - 1 ahead has higher priority
  - If no regwrite in 1 ahead, check 2 ahead
  - If neither has regwrite, read from register normally
- $0 is a special register
  - It is always 0
  - So read and write of this register shall also be considered in the forwarding unit

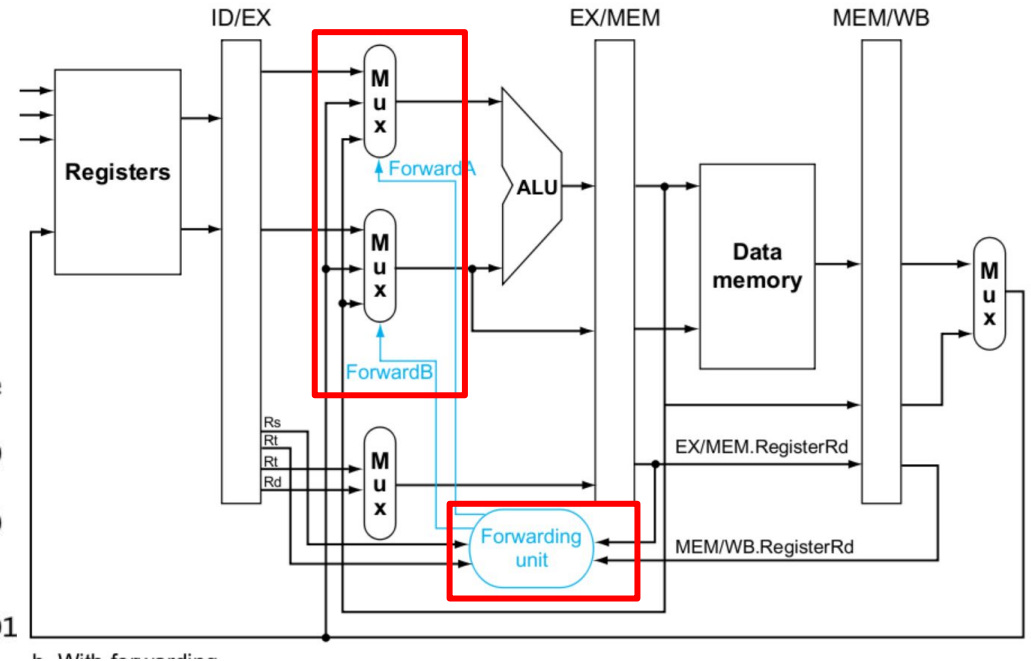
Summary

You need to implement a forwarding unit and 2 muxes

Connect them to different signals in the CPU module

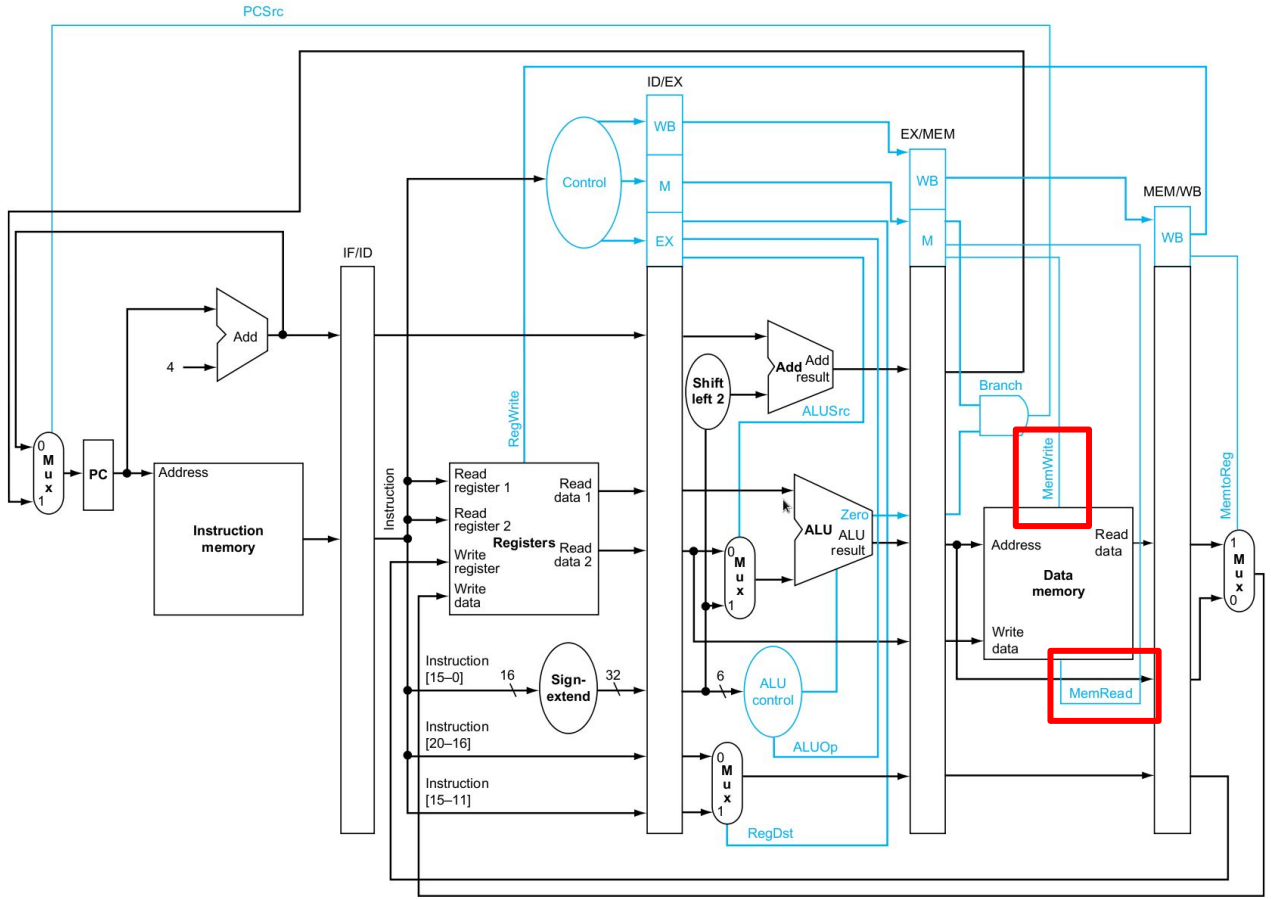
Example logic shown below, just for understanding, don't copy it

```
ForwardA = ForwardB = 00                          //initialize
IF (EX/MEM.RegWrite && EX/MEM.RegisterRd ~= 0 &&
    EX/MEM.RegisterRd == ID/EX.RegisterRs) ForwardA = 10
IF (EX/MEM.RegWrite && EX/MEM.RegisterRd ~= 0 &&
    EX/MEM.RegisterRd == ID/EX.RegisterRt) ForwardB = 10
IF (MEM/WB.RegWrite && MEM/WB.RegisterRd ~= 0 &&
     EX/MEM.RegisterRd ~= ID/EX.RegisterRs &&
     MEM/WB.RegisterRd == ID/EX.RegisterRs) ForwardA = 01
IF (MEM/WB.RegWrite && MEM/WB.RegisterRd ~= 0 &&
     EX/MEM.RegisterRd ~= ID/EX.RegisterRt &&
     MEM/WB.RegisterRd == ID/EX.RegisterRt) ForwardB = 01
```



EC: LW after SW

- Add a similar Memory Forwarding unit
- Check memread and memwrite signal and forward as needed
- No stall needed



Extra EC opportunities - 10 points

Participate an experiment of using Github CI/CD for grading this lab

Sign up here

Need to commit and push to Github during completion of the lab and provide feedbacks

Limited availability, depending on my progress and feedback

Invitations will be out on Tuesday