System on Chip Design

Jil Zerndt HS 2025
Summary

Introduction

Course Information

Course: System on Chip Design (SCD)
Institution: Zürcher Hochschule für Angewandte Wissenschaften (ZHAW)
Instructors:
- Tobias Welti (welo@zhaw.ch, +41 58 934 67 30)
- Dominique Cachin (cacd@zhaw.ch, +41 79 45559 01)

Course Materials and Schedule

- **Platform:** Moodle - https://moodle.zhaw.ch/course/view.php?id=25948
- **Script:** Available on Moodle (scd_script.pdf)
- **Lab Instructions:** https://github.zhaw.ch/pages/hpmm/scd-labs/index.html

Assessment and Grading

Grading Components

- **Electronic Quiz:** 15% (November 11, 2025, Moodle test)
- **Lab Exercises:** 15% (6 labs during semester, graded by lecturer)
- **Written Exam:** 70% (January 2026, Moodle test)

Lab Grading System

Seven labs (four lessons each) contribute to the lab grade.
Credits per Lab:
- Not done: 0 points
- Required tasks done with small errors: 1 point
- Required tasks done without errors: 2 points

Lab Grade Formula:

$$\text{Lab Grade} = \frac{\text{Sum of Points}}{12} \times 5 + 1$$

Exam Guidelines:
- Open book: lecture and lab notes, personal notes, books allowed
- No generative AI such as ChatGPT
- Calculators allowed

Course Objectives

Target Audience

This course is designed for engineers who want to:
- Design high-performance digital circuits with SoC-FPGAs, beyond writing VHDL code
- Gain in-depth background knowledge of SoC and FPGA (for software engineers)
- Design systems with Linux on SoC-FPGA
- Obtain introduction and basic knowledge of Integrated Circuit design
- Design general high-speed digital systems with complex peripherals (DDRAM)

Learning Goals

By the end of this course, students will be able to:

- Work with FPGA block memory
- Configure a FPGA-SoC with ARM hardcore processor
- Configure the I/O and computer peripherals (DRAM) of a FPGA
- Port Yocto Linux to SoC-FPGA
- Configure and analyse timing to drive synthesis
- Configure clock generators in FPGA and route clocks on PCB
- Check signal integrity of clock and data lines on PCB
- Explain differences between different signaling standards
- Connect high-speed FPGA peripherals with differential signals
- Realize a project with video and audio output (Pacman game)

Lab Setup

Laboratory Environment

Location: Lab TE 519

Equipment:

- Lab PCs with required software setup running on Linux
- DE1-SoC Development Board with Intel Cyclone V SoC FPGA
- Hardware only available in lab (not distributed to students)

Work Organization:

- Students work in teams of two
- Lab instructions available on GitHub