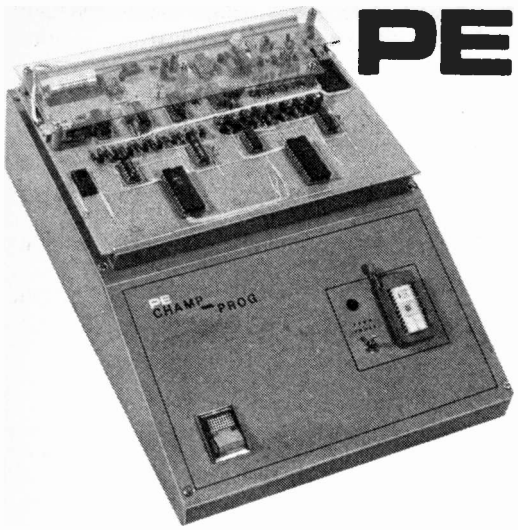


PE CHAMP

R.W.COLES B.CULLEN

PART EIGHT

CHAMP-PROG

THOSE readers who have successfully completed the construction of CHAMP can now look forward to many interesting and rewarding hours of programming and experimentation. Their systems can be used as learning aids to gain practical experience of the exciting new microprocessor technology, and as development aid to encourage the fulfillment of a multitude of software and hardware ambitions. When CHAMP is used in the latter mode, as a proving ground for hardware circuits and software programs which perform some useful function, there will come a time when programs tried out in CHAMP program RAM will need to be committed to a more permanent kind of storage for eventual use in some other small, dedicated, 4040 based system. This is when CHAMP-PROG and CHAMP-U.V. become very useful, if not essential, as additions to the CHAMP family. CHAMP-PROG is a PROM programming attachment which allows the user to copy a program stored in CHAMP program RAM into a 4702A device mounted in a "zero insertion force" (z.i.f.) front panel socket. CHAMP-U.V. is a simple erase light unit for 4702A and similar PROMS which allows a single device to be programmed and re-programmed many times over.

These facilities make for extremely low cost program amendment or enhancement when it is required, and represent a big improvement over the one-shot fusible-link PROM techniques sometimes used in m.p.u. system development.

This month we shall be looking at the operating principles and circuit of CHAMP-PROG, and how this unit is integrated with CHAMP itself.

CHAMP-PROG

As you can see from the title picture, CHAMP-PROG is built using the same system principles which were developed for CHAMP itself. The circuitry is carried on a fairly large sheet of Veroboard, which is mounted above a stylish low profile plinth made of wood and aluminium. The front panel carries a mains ON/OFF rocker switch in addition to the special 24 pin programming socket for the PROM being programmed. CHAMP-PROG has its own separate mains connector, and housed inside the plinth is a special +80V programming supply. The standard +5V and −10V supplies also required are provided by the main CHAMP power source over the same 16 way connector that is used to transmit and receive programming data. In accordance with standard CHAMP techniques, the 16 way umbilical link terminates at low cost 16 pin d.i.l. sockets, the link itself being made from d.i.l. header plugs, and ribbon or multiway cable.

The programming operation requires the application of voltage pulses with an amplitude considerably in excess of the 15 Volts used during normal operation, and the level and timing of these pulses must be kept within tight limits. The CHAMP-PROG board carries all the voltage regulation, switching, and timing functions required for successful programming of 4702A type PROMS, together with the necessary data and address drivers which are driven in their turn by two 4265 programmable interface chips.

PROMPT

The programming operation is carried out under the control of a program called PROMPT (PROM Programming Technique) which is housed in a 4702A PROM plugged into the second socket on the CHAMP main board (Chip-One). PROMPT is an interactive program which uses the keyboard interrupt routine and display driver subroutine of the CHOMP program, which *must* also be present in the Chip-Zero socket (as usual) before programming can take place. PROMPT is entered via CHOMP on the depression of the TEST button on the CHAMP front panel. (You may recall that when TEST is detected, CHOMP carries out a JUN to 100H, which is the start of PROMPT when *it* is resident in the Chip-One socket). After the depression of TEST, the 7 segment display will show "Adr 1" which is a cue to the user that a three digit hexadecimal address is required which corresponds with the *start* of the source data block in CHAMP program memory. After entering a suitable address, which will appear as usual on the left of the display, the ENTER DATA button is pressed to confirm that entry is complete. The display will now change to show "Adr 2", and a similar procedure is followed to enter an address which indicates the *end* of the source data block in CHAMP program memory. A display of "Adr 3" is next, and on this cue an address is entered which represents the *start* of the destination area in the PROM to be programmed. Although the last address need only be a two digit hexadecimal quantity (because there are only 256 locations in a 4702A PROM), a three digit address is nevertheless expected by PROMPT since this makes the initialisation procedure as uniform as possible. The most significant digit, or chip-select hexadecimal digit, is in fact ignored, and so you can enter anything you like in this position; but usually a zero of course to prevent confusion!

After the entry of Adr 3, but *before* depression of the ENTER DATA key, the PROGRAM POWER switch adjacent to the programming socket is turned ON. Subsequent depression of the ENTER DATA key starts the programming sequence which takes about 2·5 minutes for 256 locations. Completion is signalled by a display of "done", but if any location was not erased properly, or failed to program at any point in the sequence, programming will stop prematurely and a display of "Fail" will result.

THREE ADDRESS SYSTEM

The fact that PROMPT uses a three address system makes CHAMP-PROG extremely versatile since blocks of data from CHAMP program memory can be moved to new locations in the PROM being programmed, and a PROM can be loaded with blocks of data from several sources if necessary. For example:

(i) To duplicate Chip-Zero, (CHOMP), Adr 1 is entered as 000H, Adr 2 as OFFH, and Adr 3 as 000H.

(ii) To put the first half of Chip-Two into the second half of the PROM being programmed, Adr 1 = 200H, Adr 2 = 27FH, Adr 3 = 080H.

(iii) To put the single line of data at address 300H into address 020H of the PROM Adr 1 = 300H, Adr 2 = 300H, Adr 3 = 020H.

Of course, when relocating blocks of data in this way, account must be taken of the label destinations of any JUN, JMS, JCN, or ISZ instructions in the source block because these will probably be incorrect when loaded into the PROM. In the usual case the source block will be in program RAM, Chip-Two or Chip-Three, and so these label destination addresses can be temporarily changed (using CHOMP), to those applicable in the new PROM *and* its intended hardware system. (Obviously the 12 bit JUN and JMS addresses must also refer to the correct *chips* in the new system).

FAMOS PROMS

The 4702A is an MOS device using the FAMOS (Floating gate, Avalanche injection, Metal, Oxide, Semiconductor) technology to store data in the form of isolated charges on the gates of an array of MOSFET transistors. Each of the 2,048 memory cells (Fig. 8.1) consists of a single MOSFET with its gate electrode unconnected and isolated by means of a silicon dioxide insulating layer. When a cell is unprogrammed or erased there is no charge on the gate, and the source-to-drain resistance, RDS, is very high. To program a logic one into a cell, a drain to source voltage of about 47 volts is applied for a short period of time and this causes an avalanche breakdown between the drain and the substrate material. Electrons are swept across the junction, and some are energetic enough to penetrate the silicon dioxide insulator to become trapped on the buried gate electrode. A negative charge builds up on the gate and this opens a low resistance channel between source and drain in normal enhancement mode MOSFET fashion. The charge accumulated on the buried gate is proportional to both the programming voltage and to the length of time that the voltage is applied, and so these must be carefully controlled by the programmer circuitry.

In addition, the avalanche action generates considerable heat, and so the programming must be carried out not with one long pulse but with a succession of narrow pulses with a "cooling-off" period between each one. Fortunately the 4702A data sheet (Page 5-153, MCS40 manual) contains full details of the voltages and duty cycles which must be used to provide reliable programming without overheating.

BLOCK DIAGRAM

The CHAMP-PROG design is based on an original circuit supplied by Intel and used in their "Intellec" development systems. The circuit has been simplified and in many cases components have been changed to make them easier to obtain in this country. The full circuit (Fig. 8.2) is still quite complex, and contains facilities such as current limiting and crowbar overvoltage protection to protect the PROM being programmed.

The best way to appreciate the way it works is to first study the block diagram Fig. 8.3. The voltage regulator block is required to generate the programming waveforms, and it actually contains two separate regulators, one a high current +47V circuit from which the VCCS, CS, Vgg, Vdd and Program pulses are derived, and the other a +60V low current circuit which supplies Vbb. The outputs from the regulator block are not continuous d.c. voltages, but pulses of accurately determined amplitude, and the switching which generates these pulses is carried out in the regulator block under the control of the timing circuit. This consists of a chain of t.t.l. monostables

Fig. 8.1. Memory cell used in the 1702A PROM. The cell is an f.e.t. whose gate has no lead. Source to drain resistance is a function of gate charge

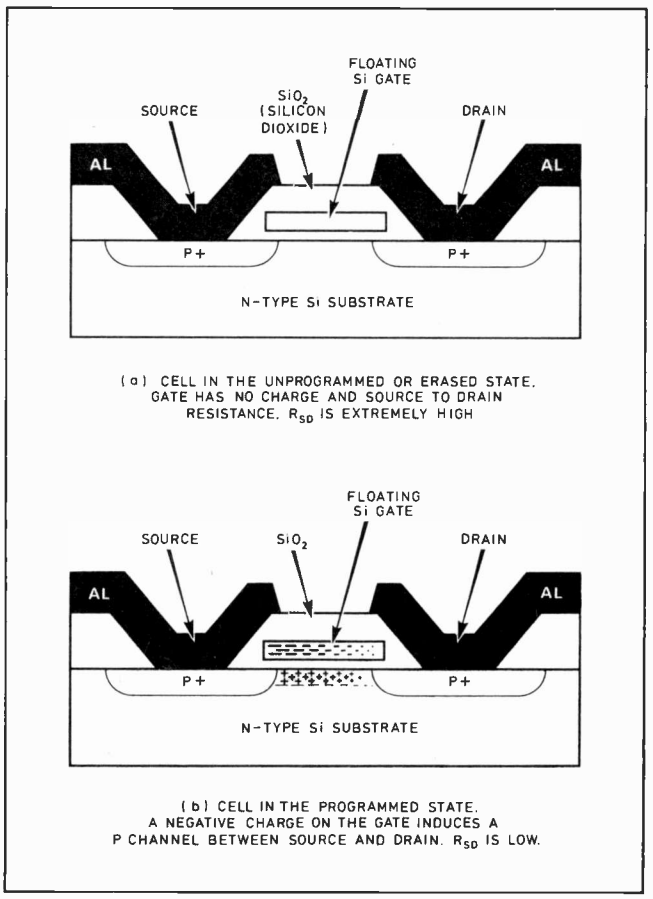
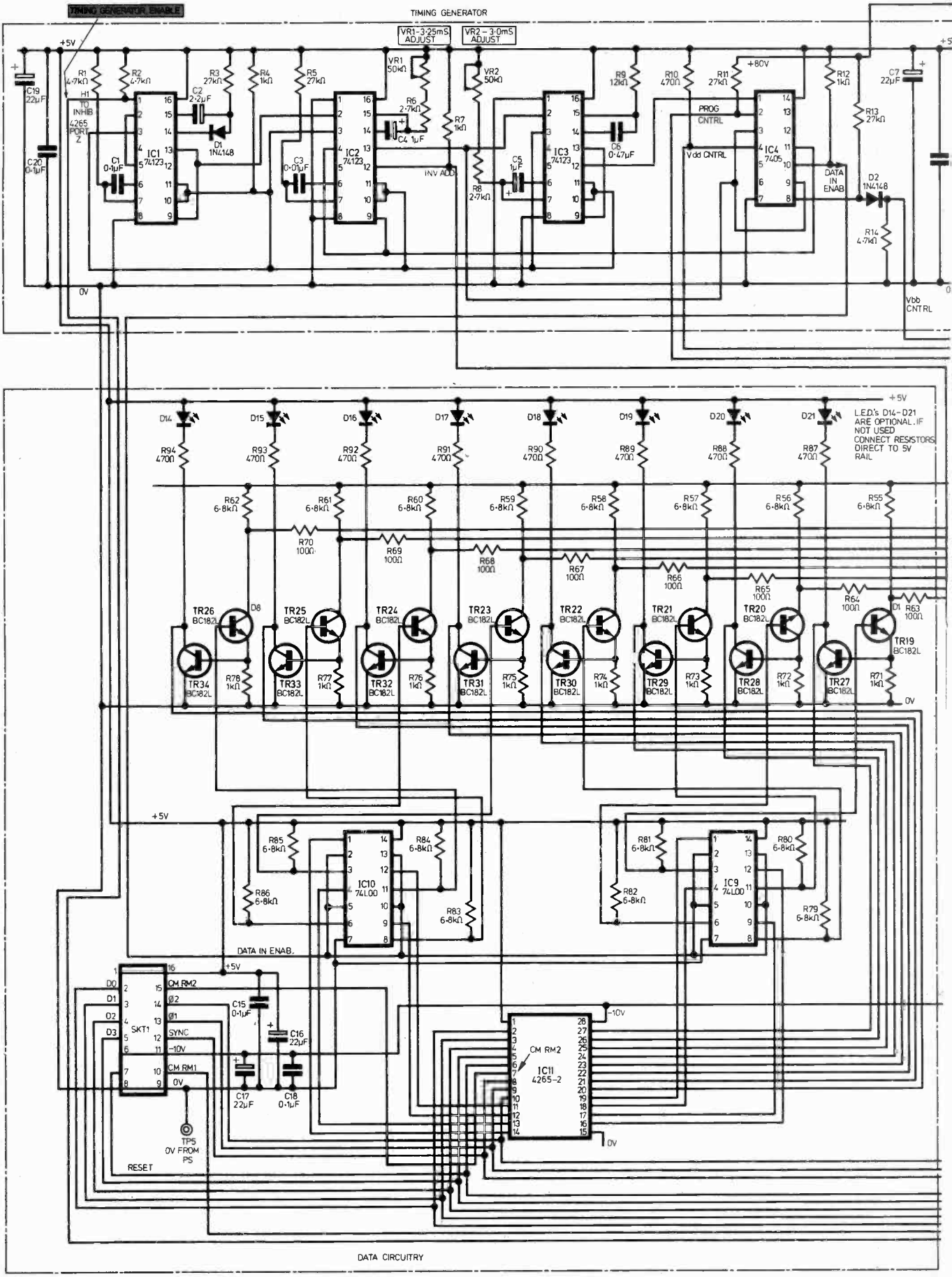
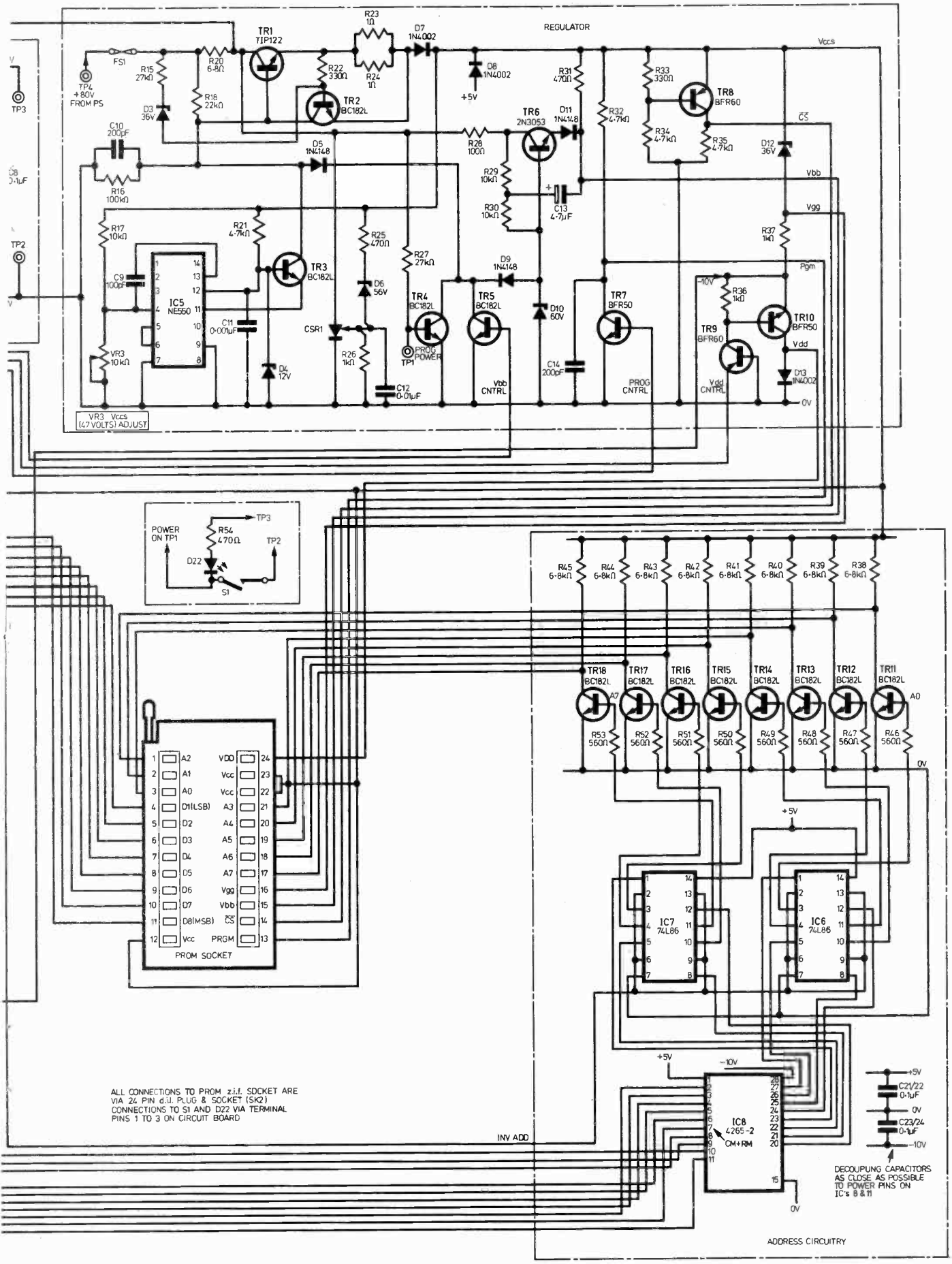


Fig. 8.2. CHAMP-PROG circuit diagram




REGULATOR
TR1 TIP122
TR2 BC182L
TR3 BC182L
TR4 BC182L
TR5 BC182L
TR6 2N3053
TR7 BFR50
TR8 BFR60
TR9 BFR60
TR10 BFR50
IC5 NE556
VR3 10kΩ
VR3 Vccs (4.7 VOLTS) ADJUST
TP1 PROG POWER
TP2
TP3
TP4 +80V FROM PS
FS1
D1 1N4002
D2 1N4002
D3 36V
D4 12V
D5 1N4148
D6 56V
D7 1N4002
D8 1N4002
D9 1N4148
D10 60V
D11 1N4148
D12 36V
D13 1N4002
C9 100pF
C10 200pF
C11 0·001µF
C12 0·01µF
C13 4·7µF
C14 200pF
R15 27kΩ
R16 100kΩ
R17 10kΩ
R20 6·8Ω
R21 4·7kΩ
R22 330Ω
R23 1Ω
R24 1Ω
R25 470Ω
R26 1kΩ
R27 27kΩ
R28 100Ω
R29 10kΩ
R30 10kΩ
R31 470Ω
R32 4·7kΩ
R33 330Ω
R34 4·7kΩ
R35 4·7kΩ
R36 1kΩ
R37 1kΩ
CSR1
Vccs
Vbb
Vgg
Pgm
Vdd
0V
-10V
+5V
Vbb CNTRL
PROG CNTRL
Vdd CNTRL
POWER ON TP1
R54 470Ω
D22
S1
R38 6·8kΩ
R39 6·8kΩ
R40 6·8kΩ
R41 6·8kΩ
R42 6·8kΩ
R43 6·8kΩ
R44 6·8kΩ
R45 6·8kΩ
R46 560Ω
R47 560Ω
R48 560Ω
R49 560Ω
R50 560Ω
R51 560Ω
R52 560Ω
R53 560Ω
TR11 BC182L
TR12 BC182L
TR13 BC182L
TR14 BC182L
TR15 BC182L
TR16 BC182L
TR17 BC182L
TR18 BC182L
A0
A7
PROM SOCKET
A2 A1 A0 D1(LSB) D2 D3 D4 D5 D6 D7 D8(MSB) Vcc
VDD Vcc Vcc A3 A4 A5 A6 A7 Vgg Vbb CS PRGM
IC6 74L86
IC7 74L86
IC8 4265-2 CM+RM
INV ADD
C21/22 0·1µF
C23/24 0·1µF
DECOUPLING CAPACITORS AS CLOSE AS POSSIBLE TO POWER PINS ON IC's 8 & 11
ALL CONNECTIONS TO PROM z.i.f. SOCKET ARE VIA 24 PIN d.i.l. PLUG & SOCKET (SK2)
CONNECTIONS TO S1 AND D22 VIA TERMINAL PINS 1 TO 3 ON CIRCUIT BOARD
ADDRESS CIRCUITRY

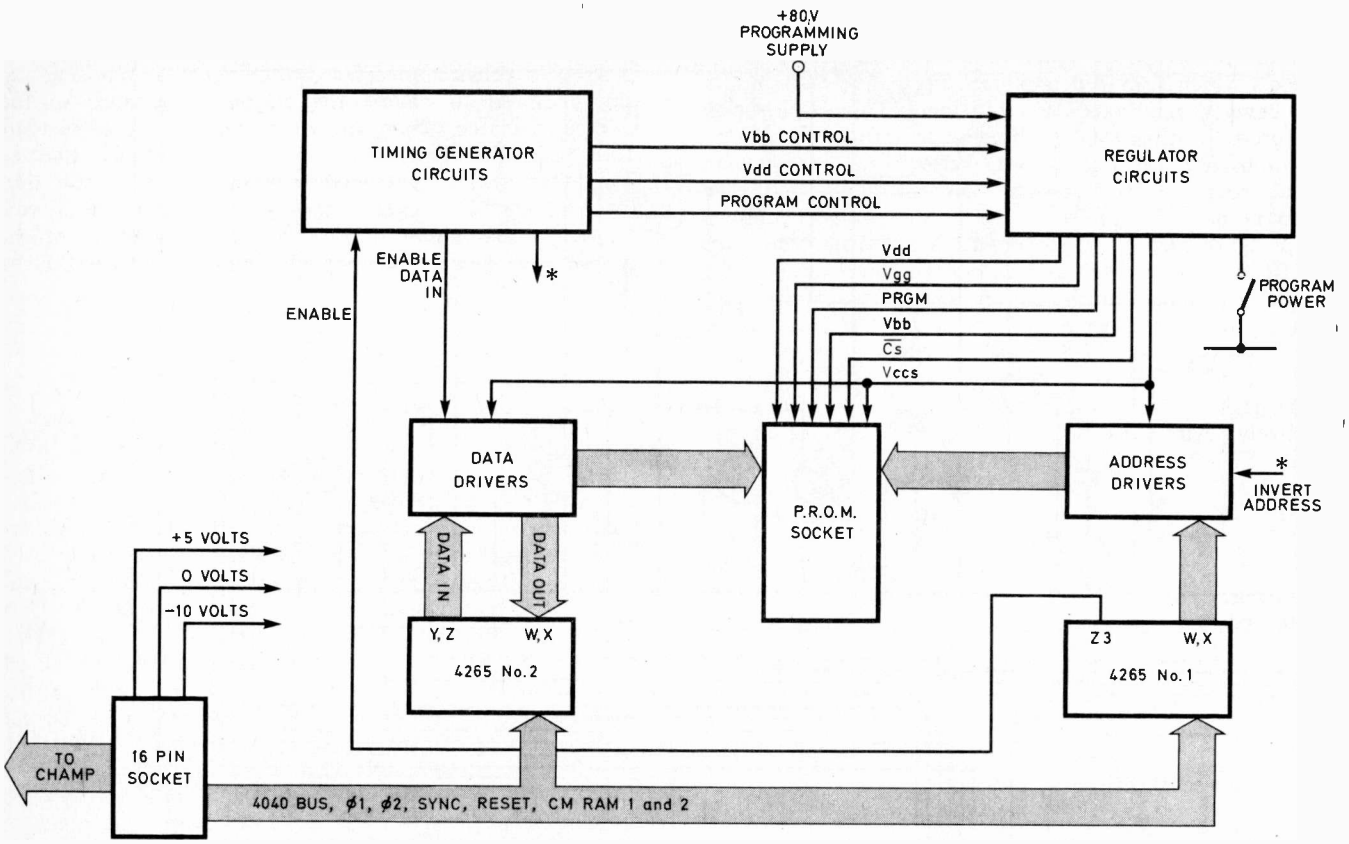


Fig. 8.3. CHAMP-PROG block diagram

that trigger each other continuously in the presence of a logic zero on the output of 4265 Number 1 port Z3. The timing generator produces a 3ms program pulse every 15ms, to give a 5:1 duty cycle, and also provides pulses to enable the program data input, and to invert the address information while Vdd and Vgg are in transition.

Because of the need to control the pulse timings to within tens of microseconds the timing function could not be carried out effectively by the 4040 itself, and so *it* has to be content with merely controlling the total *number* of 3ms pulses applied by means of port Z3 of 4265 Number 1. At present about thirty five consecutive pulses are applied, and this is determined by a 540ms software delay controlled by PROMPT. Some commercial PROM programmers operate in a slightly different way in that they provide four times the number of program pulses initially required to program a particular location, and thus adjust themselves to the needs of individual locations, using *less* pulses than CHAMP-PROG for most locations, but *more* for the stubborn ones. This latter technique has the advantage of faster (and some say more reliable) programming, but needs more complicated software. We mention it here in case anyone would care to modify the PROMPT software and try it, but there's no need to worry about this since we have never had a programming failure, and none of our PROMS ever forget! Intel themselves use the fixed duration programming techniques.

CHAMP INTERFACE

As mentioned earlier, all data, address, and control information is passed to and from the CHAMP-PROG circuit over the four-bit 4040 main data bus which is interfaced to two 4265 chips on the programmer circuit board. Up to four 4265's (including the one on the CHAMP main board) can be used with the basic CHAMP system, one to each CM-RAM line where it will respond to the RAM Chip-Two SRC address, 80H. 4265 Number 1 (IC8) is controlled by CM RAM 1 and is set to mode 4 (four four-bit output ports) as soon as PROMPT is initialised. This chip provides an eight bit address to select a PROM location on ports W and X, and uses output Z3 to control the timing generator. The other outputs are unused. 4265 number two (IC11) is set to mode 6 (two four-bit input ports, two four-bit output ports) and provides the data to be programmed on ports Y and Z, and monitors the data from the PROM between program pulses, using ports W and X. Monitoring the results of a programming sequence is necessary because after programming a location PROMPT checks the data output against the data sent earlier to ports Y and Z, to ensure that they are the same. Any discrepancy results in a program abort and a FAIL message. During programming, the data and address inputs to the PROM must take up voltage levels commensurate with the programming supplies, and so the outputs of the 4265 chips are connected to the PROM via discrete transistor drive circuits and low power t.t.l. gates. The address drivers are fed by 74L86 EXCLUSIVE OR gates which are controlled by the timing generator and used to invert the address information from 4265 number one during the transition period of 60 microseconds.

If you are wondering how the input data is presented to the 4702A when these devices do not *have* any inputs, the answer is that the data *outputs* are used as inputs during programming.

LED DISPLAY

On the prototype of CHAMP-PROG, an in-line array of l.e.d.s which provided a binary display of data in the PROM being programmed, was provided. This display was very pretty but was later thought to provide little information that was not available elsewhere, and so was deleted from the final version, with the happy result of a gain in noise immunity at the inputs to 4265 number two ports W and X. These l.e.d.s are shown dotted on the circuit and can be used if desired, they do at least provide helpful data during circuit debugging operations!

The output data from the PROM is monitored in a rather unusual way. The emitters of the PROM data line drivers (i.e. TR19) have a resistor in series, and in between program pulses the collector of this driver transistor is effectively "wire-ORed" with the PROM output driver. If the stored data is a logic 1, the collector voltage of the driver becomes +5V, and a voltage is developed across the emitter resistor due to the current through the transistor. If a logic 0 is stored however, the driver transistor collector is clamped to zero volts and it turns OFE, therefore no voltage is developed across the emitter resistor. Thus, the emitter resistor voltage is an indicator of the stored data, and this voltage is used to control another transistor (TR27) which provides a 5 Volt logic level at its collector to drive the 4265 inputs and the l.e.d.s if fitted.

TIMING GENERATOR CIRCUIT

The timing generator and voltage regulator sections of Fig. 8.2 are complicated enough to deserve a more complete explanation. IC's 1, 2 and 3 form the heart of the timing generator, and are 74123 (or 74L123 if you can get them) dual monostable circuits. IC1 provides the basic 15 millisecond P.R.F. and is a free running multivibrator which produces narrow negative going pulses at the pin 13 Q output. These pulses trigger IC2a which provides an accurately timed pulse of 3·25ms, its length being adjustable by means of VR1. The leading edge of this pulse triggers IC3a which provides a 155μs delay before triggering the actual program pulse monostable (IC3b). IC3b is set to 3·0ms by VR2. IC2b is triggered at the same time as IC3a, and this mono provides a pulse of about 60μs to invert the 4702A addresses while the supplies move to their programming levels. Four separate control outputs are produced by the timing generator, and these are buffered by means of 7405 (not low power) open collector inverters before distribution. The timing of these outputs is summarised in Fig. 8.4.

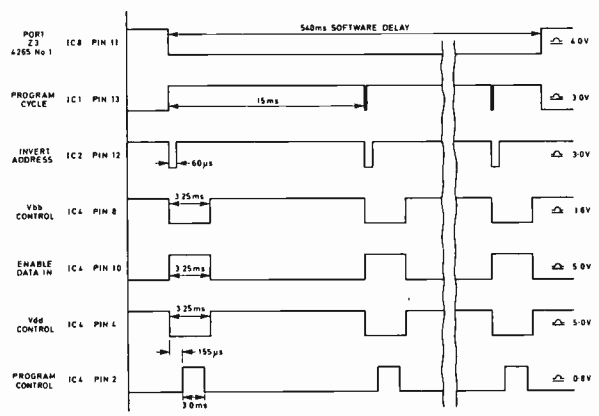


Fig. 8.4. Timing generator waveforms (not to scale)

You may have noticed that two of the 7405 outputs are returned, via 27 kΩ resistors to the +80V rail. This is done to provide superfast switching by minimising the time required to charge the wiring capacitance to the voltage regulator switch transistors, but the use of 80 volts does mean that these outputs should *never* be disconnected from their following transistor stage (during circuit testing for example), because the 7405 would be destroyed. Under normal circumstances the clamping effect of the base-emitter diode of the switch transistors makes the use of an 80V supply quite safe.

VOLTAGE REGULATOR CIRCUIT

The heart of the +47V regulator circuit is formed with IC5, TR3 and TR1. IC5 is a 14-pin 200mA regulator chip type NE550, similar to the more common LM123, and this device is used to provide the basic voltage reference and error amplifier functions required by any regulator circuit. The output of this chip controls the collector current of TR3, which has its base clamped to +12V by D4 and operates in the unusual "common base" mode. The collector load of TR3 is returned to the +80V supply rail, and the collector itself drives the base of TR1, which is the device which forms the "business end" of the regulator. TR1 has 80V at its collector, and during programming provides a +47V output at its emitter whilst passing current pulses of up to 0·5A. Obviously this is a demanding job, and the transistor chosen is a Texas TIP 122 monolithic darlington with a 100V 5A specification, and a current gain of at least 1,000 at 3A. The output voltage of the regulator is sensed at the cathode of D7 via a resistive divider, R17 and VR3, and is fed to the non-inverting input of the error amplifier in IC5. VR3 is of course used to set the output voltage to the required 47·0V.

PROTECTION

A double measure of protection is provided by the regulator circuit. TR2 acts as a current limiter when turned on by a voltage drop across R23||24 (0·5 ohms) which exceeds its Vbe threshold, thus diverting TR1 base current which clamps the output current to a level low enough to prevent destruction of the regulator during short-circuits. CSR1 and D6 act as a crowbar overvoltage protection circuit to prevent damage to other regulator components on the PROM being programmed should TR1 ever fail. On the appearance of a potential in excess of about 56V at the cathode of D7, D6 turns on and triggers CSR1 causing it to short out the 80V supply via R20 and blow FS1 (1A). A ruthless procedure perhaps, but without doubt the simplest and neatest way to disconnect supplies in an emergency!

Transistor TR6 and D10 form the other 60V regulator circuit, and in this case a simple Zener/emitter follower combination is all that is necessary.

SWITCHING CIRCUITS

Up to now I have referred to the regulators as though they were standard d.c. circuits, but of course they are not, because pulsed operation is necessary for proper programming. Both regulators are turned off by means of the clamp transistor TR5 which when not turned off itself by means of the 3·25ms Vbb CNTRL pulse from the timing generator, conducts to clamp the bases of TR1 and TR6 to a low voltage so that they cease to function.

COMPONENTS . . .

Resistors

2 off 1Ω 1W 5%	R23, R24
1 off 6·8Ω 5W 5%	R20
1 off 100Ω 1W	R28
8 off 100Ω	R63–R70
2 off 330Ω	R22, R33
11 off 470Ω	R10, R25, R31, R87–R94
8 off 560Ω	R46–R53
14 off 1kΩ	R4, R7, R12, R26, R36, R37, R71–R78
2 off 2·7kΩ	R6, R8
7 off 4·7kΩ	R1, R2, R14, R21, R32, R34, R35
24 off 6·8Ω	R38–R45, R55–R62, R79–R86
3 off 10kΩ	R17, R29, R30
1 off 12kΩ	R9
1 off 22kΩ	R18
6 off 27kΩ	R3, R5, R11, R13, R15, R27
1 off 100kΩ	R16

All resistors ⅛W 2% unless otherwise stated, R87–R94 are optional l.e.d. resistors

Potentiometers

1 off 10kΩ 20 turn min preset	VR3
2 off 50kΩ 20 turn min preset (Doram)	VR1, VR2

Capacitors

1 off 100pF polyester	C9
2 off 200pF polyester	C10, C14
1 off 0·001μF ceramic	C11
2 off 0·01μF	C3, C12
9 off 0·1μF disc ceramic (2 for IC8 and 2 for IC11)	C1, C8, C15, C18, C20–C24
1 off 0·47μF ceramic	C6
2 off 1μF	C4, C5
1 off 2·2μF/35V tant bead	C2
1 off 4·7μF/35V tant bead	C13
4 off 22μF/25V tant bead	C7, C16, C17, C19

Diodes and Rectifiers

5 off 1N4148	D1, D2, D5, D9, D11
3 off 1N4002	D7, D8, D13
1 off 12V zener 1W	D4
2 off 36V zener 1W	D3, D12
1 off 56V zener 1W	D6
1 off 60V zener 1W	D10
8 off Min red l.e.d. (optional)	D14–D21
1 off Front panel red l.e.d.	D22
1 off Thyristor 400V/4A	CSR1

In parallel with TR5 is TR4, and this transistor is capable of the same clamping action, but in this case it is controlled manually by means of the PROGRAM POWER switch on the front panel.

PROGRAMMING SUPPLIES

The other active components, TR7, TR8, TR9 and TR10 are used to generate the required PRGM, Cs, Vgg and Vdd voltage pulses from the "raw material" provided by the 47V Vccs line, the +5V line and the −10V line. The full complement of program voltage waveforms is shown in Fig. 8.5, and no doubt most readers will be able to see for themselves just how these are generated by the circuit. The Vccs line actually switches between +5V and +47V, and D8 provides the clamping action to maintain the +5V level in the absence of program pulses. Notice also that the 3·0ms PRGM pulse itself is actually a *negative* going waveform (+47V to 0V).

Transistors

1 off TIP122	TR1
28 off BC182L	TR2–TR5, TR11–TR34
1 off ZN3053	TR6
2 off BFR50	TR7, TR10
2 off BFR60	TR8, TR9

Integrated Circuits

3 off 74123 or 74L123	IC1–IC3
1 off 7405	IC4
1 off Signetics NE550	IC5
2 off 74L86	IC6–IC7
2 off 4265–2	IC8, IC11
2 off 74L00	IC9, IC10

Miscellaneous

PROM socket 2, which is a 24-pin d.i.l. low profile p.c.b. type. Also a 24-pin d.i.l. header plug and suitable miniature flexible wire to form a loom.
Zero insertion force 24-pin PROM socket.
Fuse holder (p.c.b. type) and 1A fuse.
Reel of Kynar wire or similar
Piece of VB24 Veroboard cut to 88 holes × 160mm.
Soldercon pins (approx 200).
Terminal pins (0·1 inch).
One single sided 16-way d.i.l. low profile p.c.b. socket, complete with two 16-way d.i.l. header plugs joined by a 16-way ribbon cable to form a link between CHAMP and CHAMP-PROG, approx. 300mm long.
Fine 4BA plastics pillars cut to 20mm and glued to p.c.b.
Thin clear perspex sheet 650 × 220mm (to be fastened to pillars).

Constructor's Note

The zero insertion force 24-pin PROM socket (*Type 2, part No. 224-3344-00-0602)* is available from:
B.F.I. Electronics, Sinclair House, The Avenue, West Ealing, London W13.

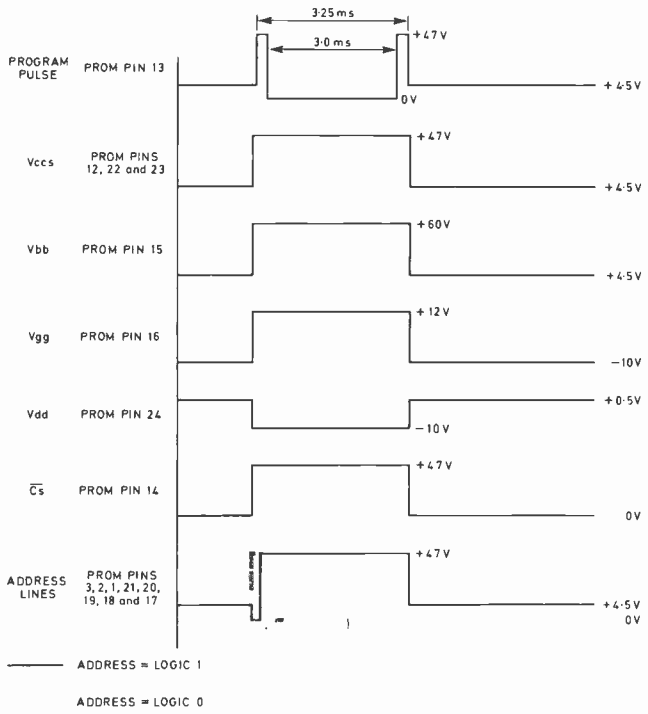


Fig. 8.5. Address lines and regulator circuit outputs during program pulse

SUCCESSFUL

CHAMP-PROG has proved to be a really useful addition to the CHAMP system, and the prototype has been used to program a total of more than 50 PROMS of mixed origin without a failure.

Intel 4702A and 1702A devices have been tried together with low cost surplus devices of unknown origin, and CHAMP-PROG has coped with them all. Anyone who has tried to develop their own software while using the CHAMP "postal programming service" will know just how expensive and unsatisfactory this can be. CHAMP-PROG will enable CHAMP programmers to be completely independent in their activities, and consequently very productive! ★

NEXT MONTH: CHAMP-PROG construction and PROMPT

A number of Intel MCS-40 User's Manuals and 4004/4040 Programming Manuals are held by P.E. at Poole, which we are willing to give away in sets on a "first come first serve" basis to anyone supplying a strong 11 × 13 inch s.a.e. with 54p stamp (67p 1st class).

NEWS BRIEFS

Ring A Rig

COULD a worker on a North Sea oil rig 150 miles north-east of the Shetlands, pick up a normal telephone and dial directly to anywhere on the mainland? The answer is yes! Thanks to a £5 million top priority Post Office project, even the most distant oil platform, Thistle "A", came into the telephone network last November, giving workers there a telephone dial capable of calling 355 million phones in 67 different countries, just like subscribers on the mainland!

Over the next 15 months there are a number of platforms still to be linked into the system, known as the technique of trans-horizon radio, and which has never before been used by the PO. It all relies on the tropospheric scattering of microwave frequencies normally used for line-of-sight communication, but which are still visible to aerials far beyond the horizon. Turbulence in the troposphere (Earth's lower atmosphere) will cause this "fringe" of radio signals in much the same way as the glow from a distant searchlight might be seen, even when the beam itself is out of sight.

A powerful signal is beamed in the direction of the production platform, and a signal reduced in strength by something in the order of $1/10^{10}$ will reach the directional aerial waiting for it.

The control station is located near Fraserburgh, Aberdeenshire, and two relay stations are sited on South Shetland. Two separate troposcatter paths link land to a pair of platforms up to 30 miles apart, which are linked to each other by line-of-sight microwave. This completes the triangle for alternative path operation, giving high service reliability.

Traffic Computer

NOT all drivers in the Leicester area will realise that they are being told what to do by a computer, and have been since the Leicester Area Traffic Control Scheme became operational in October 1974.

The traffic plan swung into action with 96 traffic signals and Pelican crossings linked to a central computer via Telecommand/5 remote control systems, built by Plessey Controls Ltd of Poole, Dorset. As additional urban area signals were installed, they too were connected to the computer, bringing the total to 128 signals with expansion capability to 192.

Some of that spare capacity is now being used with an extension of the traffic control system to Loughborough, 11 miles away. Fourteen extra signals, including 7 on the A6, will spread the improved traffic flow situation, which was found in Leicester to give a 12 per cent decrease in delays to general traffic, and save travel time to buses of about 6 per cent during peak periods. There are now also 53 *special* detectors continuously relaying traffic information.

The Leicester Control Centre monitors both cities, where consoles comprising VDUs, closed circuit television, and a large mosaic map showing the condition at each intersection can be used to call up reserve plans for relieving congestion. Be it caused by a breakdown, an accident or any other unexpected event, the use of a reserve plan will activate a warning light at the appropriate point on the mosaic map. Any predictable problems such as the rush hour or football matches, will be dealt with by one of the computerised traffic plans.

A side-benefit of this system is immediate location of the majority of traffic light faults, and the computer even runs a special program during the night to check out all the signal timings and report any errors.