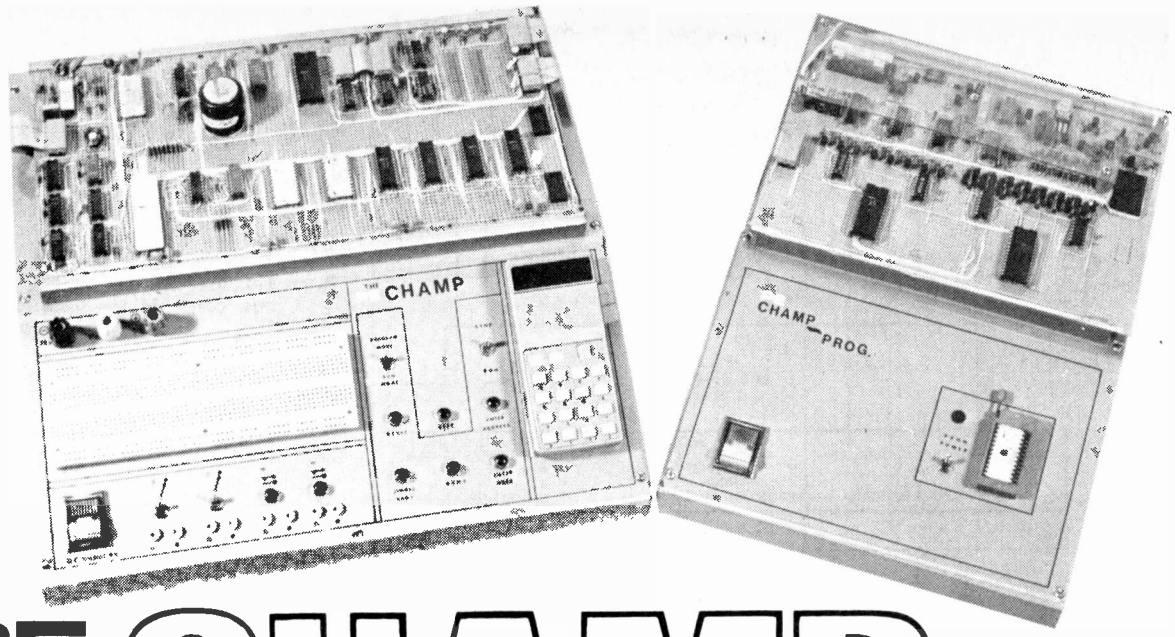


PE CHAMP

R.W. COLES
B.CULLEN

PART TWO

LAST month we examined the CHAMP "family" concept of combining a microprocessor unit (CHAMP itself), PROM programmer (CHAMP-PROG), and a PROM eraser (CHAMP-UV) to produce a self-sufficient and capable development system.

This month we shall start to look in detail at the circuitry on the CHAMP microprocessor board, and at the 4040 MPU chip around which the system is constructed.

MAIN BOARD

The main objective of the CHAMP design was to produce a *complete* microprocessor system at the lowest possible cost, and in keeping with this objective no expensive plug-in cards and edge connectors are used at all. Major circuitry is mounted on a single piece of 0·1in matrix Veroboard which, in fact, is a much more convenient packaging solution than more expensive plug-in cards anyway!

Connections to the board are made via 16-way d.i.l. plugs and sockets, and in the basic system, only two of these are occupied with the others available for system expansion and debugging purposes. Power is coupled to the board via three hardwired leads terminated in wander plugs. These can be plugged into sockets on the power supply itself, or, when the board is in its vertical position, into sockets adjacent to the breadboard.

CONSTRUCTOR'S NOTE

A kit comprising the main i.c.s for CHAMP:

4040	4289	2 off 5101-8
4201A	1 off 4702A	Plus
4265	3205	4040 XTAL
1 off 4002-1		

is available from Rapid Recall Ltd., Dep. N, 9 Betterton Street, Drury Lane, London WC2H 9BS at the special price of £49·68 including post, packing and VAT

The board can be removed rapidly when necessary by simply uncoupling the connectors mentioned above and then sliding it sideways out of the self adhesive card guides in which it rests. Under the board, on the plinth, is another card guide which can be used to support the board in the vertical position with all connections remade, on those occasions where access to *both* sides of the board is required.

The board itself measures 305 × 159mm and carries 25 integrated circuits including PMOS, CMOS and TTL devices.

4040 MPU CHIP

At the heart of the board is of course the 4040 microprocessor chip. The 4040 is a development of the Intel 4004, which had the honour of being the first microprocessor ever produced. As mentioned last month, CHAMP is downwards compatible with the 4004 chips, allowing the development of very low cost dedicated systems when the more sophisticated features of the 4040 are not required.

The 4004 chip is housed in a 16-pin package whereas of course the 4040 uses the larger 24-pin version; both chips are made using the well tried PMOS technology and need 15 volt supplies. In CHAMP, supplies of −5V and −10V are used so that interface to TTL and CMOS can be simply achieved without recourse to level translation.

The 4040 and 4004 are "four-bit" microprocessors, which means that their arithmetic units operate on "words" of four binary bits, and that transfer of data within a 4040 or 4004 system is carried out four bits at a time. This does *not* of course mean that arithmetic resolution is limited to four bits: *any* arithmetic resolution can be achieved by simply cascading four-bit operations. "Natural" 4040 arithmetic resolutions are in fact 64 bits binary or 16 digits decimal, as we shall see when we consider the arrangement of data memory.

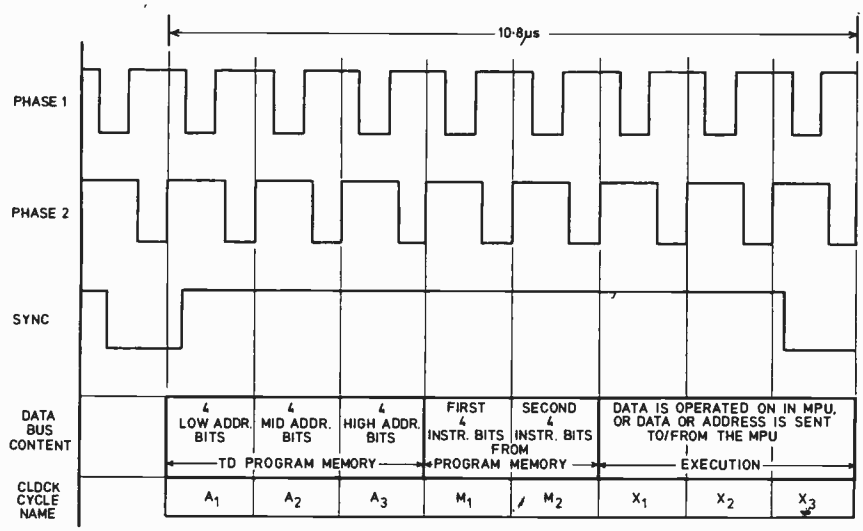


Fig. 2.1. System timing and data bus contents for the 4040

COMPONENTS . . .

CHAMP BOARD

Resistors

4 off	47Ω	R1–3, R40
2 off	100Ω	R33, 59
8 off	150Ω	R51–58
1 off	270Ω	R32
17 off	1kΩ	R6, R8–13, R15, 17, 26, 31, 34, R35–38, R60
13 off	5·1kΩ	R14, R18–25, R45–48
9 off	10kΩ	R4, 7, 16, 39, R41–44, R49
4 off	12kΩ	R27–30
1 off	47kΩ	R50
1 off	1MΩ	R5

All 2% ⅛W carbon film

Capacitors

2 off	33pF	Sub-min ceramic	C4, 5
7 off	10nF	Ceramic disc 18V	C6–11, C14
1 off	0·1μF	Ceramic disc 18V	C12
3 off	0·22μF	Polyester	C1, 2, 13
1 off	1μF	Tantalum bead 35V	C3
1 off	4·7μF	Tantalum bead 35V	C15

Transistors

5 off BC108	TR1–5

Diodes

1 off BYZ88C3V9	Zener, 3·9V 400mW D13
14 off OA47	D1–12, D19–20
6 off 1N4148	D14–18, D21

Integrated Circuits

1 off 3205	IC17
2 off 4002	IC4, 5
1 off 4040	IC2
1 off 4201	IC1
1 off 4265	IC6
1 off 4289	IC15
2 off 4702A	IC18, 19
4 off 5101	IC20–23
3 off 74L00*	IC3, 10, 24
1 off 74L02*	IC25
3 off 74L74*	IC11–13
1 off 74123	IC9
1 off 74125	IC14
1 off 74157	IC16
2 off 75491	IC7, 8

*See Text

Miscellaneous

B1 Nickel Cadmium stack, 4·8V 225mAh
XL1 Crystal 5·185MHz
8 off 16-pin d.i.l. low profile sockets, SK1–8
500 off Soldercon sockets
Veroboard VB124 179 × 454mm

4040 INSTRUCTIONS

Although the 4040 is a "four-bit" device, its instruction set is based on an eight-bit word length which means that program memory (which is separate to data memory) is organised as consecutive locations each containing *eight* bits. A popular name for an eight-bit word is "byte", and a four-bit word is often called a "nibble" (for obvious reasons!). From now on we will be using these terms when appropriate.

The 4040 has a total of 60 separate instructions, some of which are 16 bits long and require two consecutive bytes in program memory.

For dedicated applications, program memory would normally consist of ROMs or PROMs, but because CHAMP is a development system, an area of RAM program memory is also provided, for user programs, and this makes it important for us to differentiate between program and data RAM which are of course used for different purposes. The 4040 uses a 12-bit address counter which allows up to 4096 bytes of program memory to be directly addressed, although only 1024 locations are actually used in the CHAMP system as it stands, 512 bytes being assigned to PROM and 512 bytes to RAM. The CHOMP system firmware occupies 256 bytes only; when the PROMPT programmer firmware is added however, the full 512 bytes of PROM are utilised.

USER'S MANUAL

It is important that any intending CHAMP constructor should obtain a copy of the "Intel MCS-40 User's Manual" preferably of the March 1976 or later edition. This is provided free when a chip set is purchased, and is a mine of information on 4040 operation, programming, and interfacing, and contains data sheets on systems components like RAMs and PROMs.

The description of 4040 operation provided here is necessarily limited by space considerations, and most CHAMP users will soon find themselves wanting to know more! The User's Manual provides all the answers to technical questions and includes many programming and applications examples to whet one's appetite!

4040 OPERATION

The 4040 uses the dynamic mode of operation which means that it must be continuously clocked to ensure proper data retention. The necessary 2-phase clock is best provided by the Intel 4201 clock generator which is produced especially for

this purpose, since in addition to containing the clock circuitry this device provides the power-on reset logic and the single step logic which forms an essential part of any development system. The basic clock frequency is determined with the aid of a crystal, and is normally set, as in CHAMP, to 5·185MHz to give the data sheet instruction cycle time of 10·8 microseconds. The basic clock frequency is divided in the 4201 to give two 740kHz non-overlapping pulse trains which are used to drive the MPU chip clock inputs.

Inside the 4040 this clock frequency is further divided into "instruction cycles" which each consist of eight clock periods. The instruction cycle is really the shortest interval which can be isolated in an operational system. When the SINGLE SHOT mode is used it initiates either one or two of these instruction cycles depending on whether a one- or two-byte instruction is involved. The 4040 signals the start of a *new* instruction cycle with a pulse output on its SYNC pin, and this signal is wired to all the other devices which interface directly with the 4040 bus so that they can keep in step with processor timing.

The 4040 uses a four-bit data bus (D_0 D_1 D_2 D_3) to communicate with its associated flock of program memory, data memory, and input/output ports. In fact this so called data bus is really a combined data and address bus, since there is no separate address bus as in most other microprocessors.

Now, if you have followed me so far, you may be wondering how on earth the 4040 manages, during the execution of a single instruction, to send *out* 12-bit addresses, *retrieve* 8-bit instructions, and *shift* 4-bit data nibbles around when all it has to do it with is a single four-bit bus! The answer, of course, is provided by time multiplexing, and now we can begin to see why one instruction cycle consists of eight clock cycles.

DATA BUS CONTENTS

Immediately after the 4040 SYNC pulse, the low order four bits of a program memory address are sent out on the data bus followed one clock cycle later by the middle four bits, and then the high order four bits, after this back to the 4040 come the first four bits of the instruction, followed by the second four bits. This leaves three clock cycles out of the eight for the execution phase of the instruction, when the accumulator contents and data RAM addresses are able to use the bus as required by the particular instruction which was fetched.

The use of a time multiplexed bus of this type drastically reduces the number of interconnections required (at least 20 wires would be required by a non multiplexed bus) but it does impose a time penalty. It is our contention that for home built systems this is a trade-off worth making, after all, even with a 10·8 microsecond instruction cycle, 92,592 single-byte instructions can be carried out in one second! System timing and data bus contents are summed up in Fig. 2.1.

ADDRESSING DATA MEMORY

The data memory used with a 4040 system is of a special type, organised in a unique way. The chips used are coded 4002 and they contain, in a 16-pin package, four RAM registers and a four-bit output port. Each register consists of 20 separately addressable locations of four bits, subdivided into 16 main memory locations and 4 status characters (Fig. 2.2).

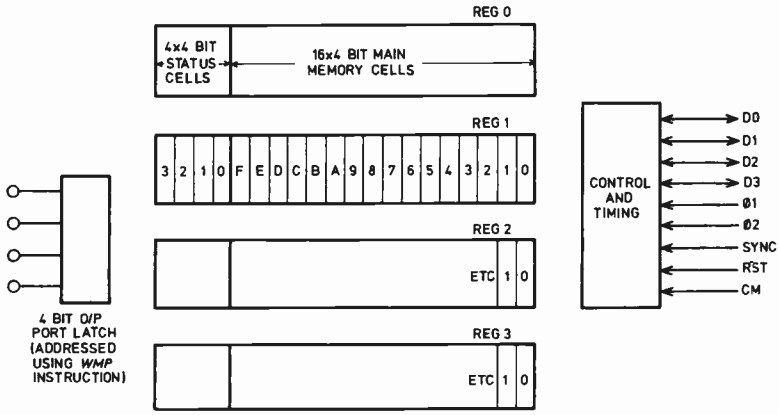


Fig. 2.2. Organisation of 4040 system data memory

This memory organisation was originally intended for the convenient storage of 16-digit binary coded decimal floating point numbers, the status characters being intended for storage of the mantissa sign, two-digit exponent, and exponent sign. Despite this design intention, the 4002 structure is quite suitable for all other likely uses and can readily be used for the storage of binary arithmetic operands, status flags, counters, and what-you-will. The status characters are directly addressable within a register and are therefore useful as "overspill" registers to take the load off the internal 4040 register array when space is limited.

Addressing a particular 4002 location is achieved with the aid of an instruction called *SRC* (Send Register Control) which causes the eight-bit address of a RAM location to be sent out on the 4040 data bus in two consecutive nibbles. The 4002 contains all the necessary demultiplexing circuitry to unscramble and latch this address.

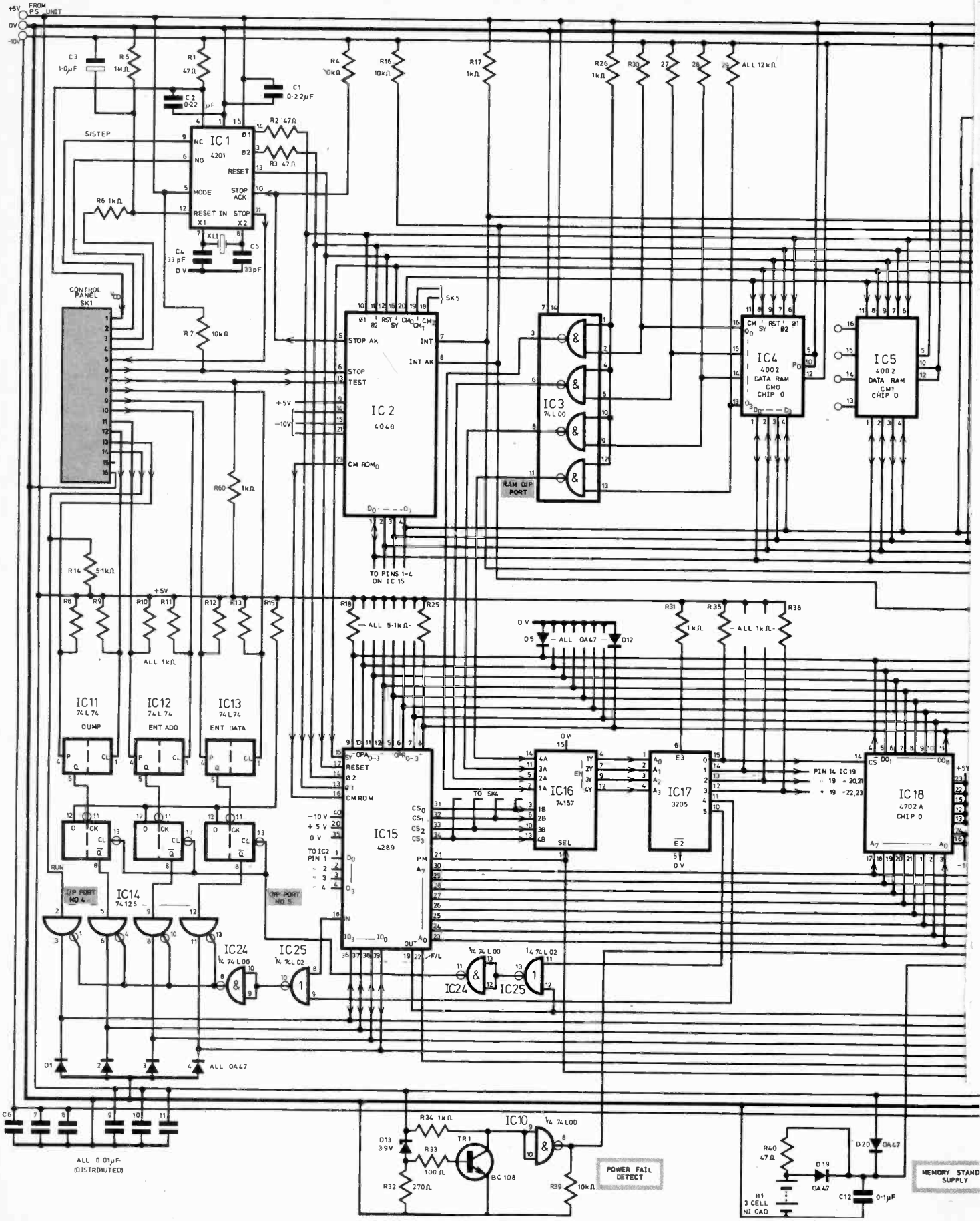
ADDRESSING PROGRAM MEMORY

The CHAMP system uses standard 4702A EPROM chips and 5101 256 × 4 RAM chips to form the program array, but these chips have no internal facilities for demultiplexing the 4040 bus. To provide the necessary multiplexing and demultiplexing functions, another member of the 4040 family, the 4289 memory interface chip, is used. The 4289 "unscrambles" the 4040 bus to give twelve parallel address outputs, and also "scrambles" the eight-bit instruction words *from* the program memory so that they can be sent back to the MPU chip over the bus.

The combination of 4289 and standard memory components is therefore equivalent to the 4308 mask-programmed ROMS which *do* contain 4040 bus interface logic but which are of course unsuitable for use with a development system because they cannot be reprogrammed. The 4308 parts also contain a number of input/output ports which can be accessed using the *RDR* and *WRR* instructions, after selection with an appropriate *SRC*. To duplicate this function the 4289 provides a four-bit bidirectional I/O bus which interfaces with up to 16 input and 16 output ports built with TTL or CMOS logic.

INPUT/OUTPUT

In the CHAMP system this "ROM I/O" facility is used only by the CHOMP firmware for control functions and for writing programs into program RAM. CHAMP *users* would normally concern themselves only with the data RAM based I/O provided by the 4265 programmable general purpose I/O chip.


+5V FROM P.S. UNIT
0V
-10V
IC1 4201
IC2 4040
IC3 74L00
IC4 4002 DATA RAM CHIP 0
IC5 4002 DATA RAM CHIP 1
IC11 74L74 DUMP
IC12 74L74 ENT ADD
IC13 74L74 ENT DATA
IC14 74125
IC15 4289
IC16 74157
IC17 3205
IC18 4702A CHIP 0
IC24 ¼ 74L00
IC25 ¼ 74L02
S/STEP
CONTROL PANEL SK1
SK5
SK4
RAM O/P PORT
O/P PORT NO 4
O/P PORT NO 5
RUN
TO PINS 1-4 ON IC 15
ALL 1kΩ
ALL 5·1kΩ
ALL 12kΩ
ALL 0·01μF (DISTRIBUTED)
ALL OA47
POWER FAIL DETECT
MEMORY STAND BY SUPPLY
B1 3 CELL NI CAD
BC 108

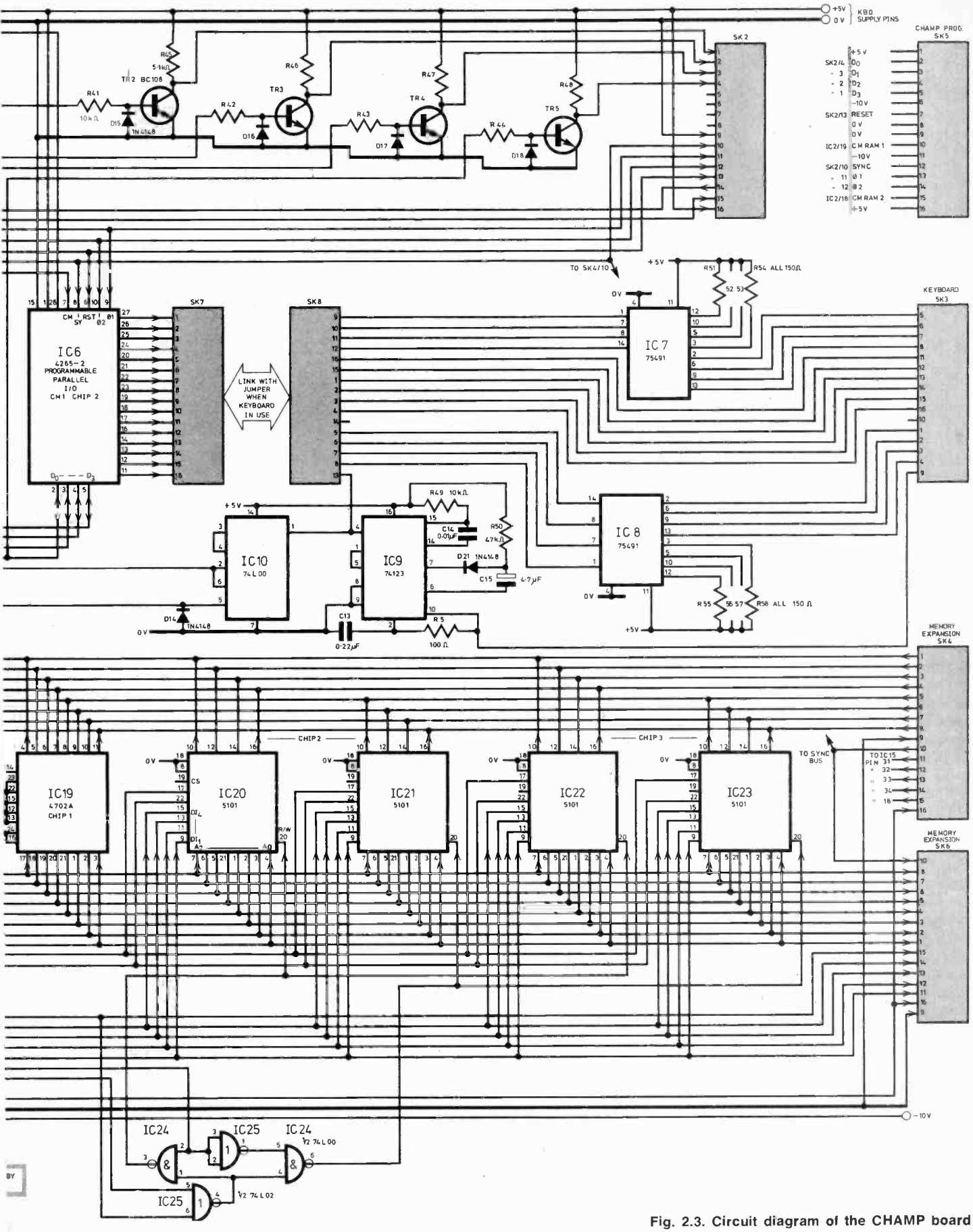
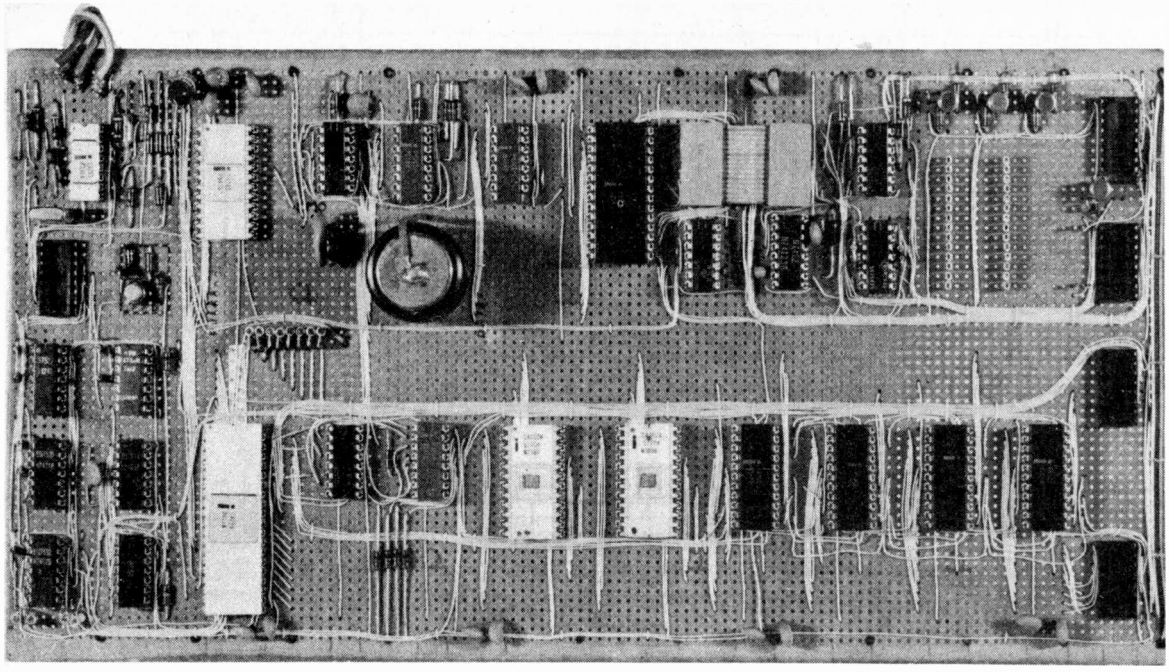


Fig. 2.3. Circuit diagram of the CHAMP board



Bird's-eye view of the CHAMP board

The 4265 is a powerful addition to the 4040 family which can live at the end of the 4040 bus and yet provide 16 input/output lines which may be configured *using software* into any one of 14 separate operating modes. The 4040 system can directly address up to four 4265 chips, and one is provided on the CHAMP main board. If CHAMP-PROG is added, then a further two 4265s come with it, their ability to talk directly to the 4040 bus being demonstrated by the fact that only a single 16-way flat cable is needed to pass all programming data and power supplies between the two units!

The 4265s occupy address space normally used by 4002 data RAM chips, and are in fact addressed and accessed in the same way, using the same instructions. The mode of operation for each 4265 is programmed during system initialisation by means of the *WMP* instruction, subsequent data transfers being made by use of the *WR0* to *WR3*, *RD0* to *RD3*, *WRM*, *RDM*, *ADM* or *SBM* instructions.

The CHAMP "on board" 4265 is put into mode 9 during initialisation and used as the keyboard/display interface during program load and debug. When a user program is run, however, the same 4265 can be reprogrammed to a *different* mode, with connections to user circuitry made via the 16-way d.i.l. socket provided for this purpose. Needless to say, this is a very useful and powerful facility! The 4265 chips even have a mode which allows them to be used as a data memory interface for use with standard memory chips like the 2111. This is very useful where a lot of data RAM is required because a 4265 and four 2111 chips provide 1024 four-bit nibbles in a much more compact form than the 16 4002 chips otherwise required. It is only fair to point out, however, that *most* 4040 applications do not need that much data RAM!

INTERRUPTS

The 4040 has a single-level interrupt which can be extended externally to any number of lines. CHAMP uses the interrupt facility for keyboard entries, although user programs can reallocate the interrupt to another source or sources as required, multiple interrupts being resolved by using an input port to "poll" all possible sources.

The 4040 has an internal seven-level hardware address register stack which is used to save the current address value when an interrupt occurs. This stack is also used for saving subroutine return addresses.

PUTTING THE PIECES TOGETHER

In Fig. 2.3 we show the overall circuit of the CHAMP board and you should now be able to pick out the main system components like the 4201 clock generator, the 4002 data RAM, the 4289 program memory interface, the 4702A and 5101 program memory chips, the 4265 programmable I/O and of course the 4040 MPU chip itself. You will also see that scattered among these major systems components there are a number of TTL gates and flip-flops and of course a variety of discrete components, which together form an essential part of the CHAMP microprocessor circuit. Next month we shall be examining the operation of this circuitry in detail, but meanwhile a word about interfacing is necessary.

TTL COMPATIBLE

CHAMP brings together on one board PMOS system chips, CMOS memory chips and TTL gates and flip-flops, all of which differ in their interface requirements. Most 4040 system parts have a variety of options available via their supply pins so that their output drive levels may be programmed to be compatible with all the logic families likely to be encountered.

In CHAMP, TTL interfacing has been chosen since this is practical and uncomplicated and is also suitable for use with 5 volt CMOS. For complete details of the interface considerations involved, refer to chapter three of the user handbook where the 4040, 4289, 4265, and the 4002 are dealt with.

In general it is best to use *low power* TTL in an MCS40 system since it is both sufficiently fast and easy to drive, although certain 4289 and 4265 outputs *are* capable of driving standard TTL loads if necessary. In CHAMP, low power TTL is recommended, although it is only *essential* in the IC3 position.

NEXT MONTH: CHAMP Development System circuit description