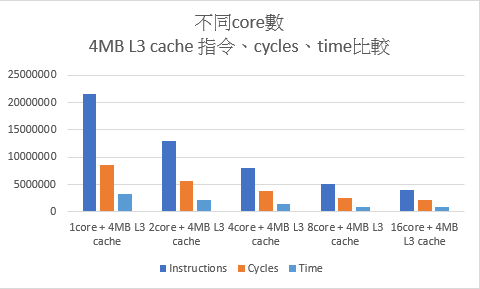
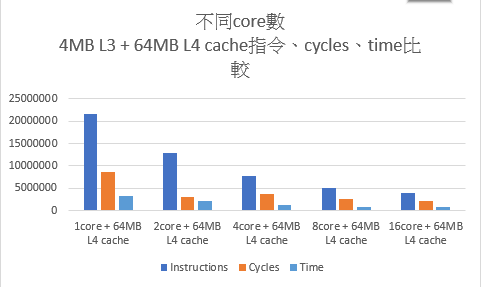
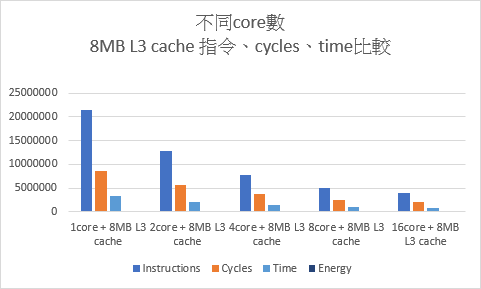
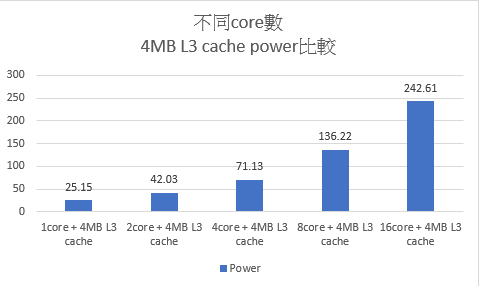
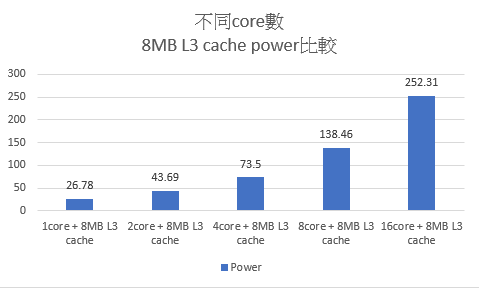
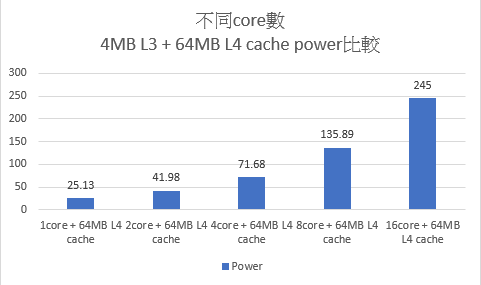
CAProject3 M113040064 李冠宏

1. Please analyze the performance (power, energy, latency…) under different conditions (number of cores, cache levels, cache size, access time…). Paste the result images and configuration images in the file. Analyze the relationship between the conditions and performance clearly.



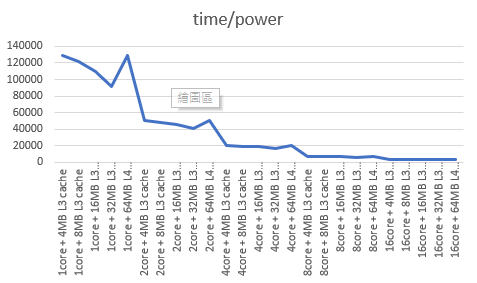
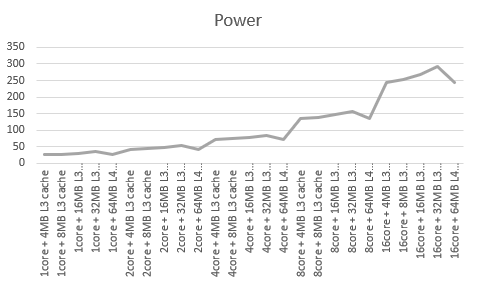
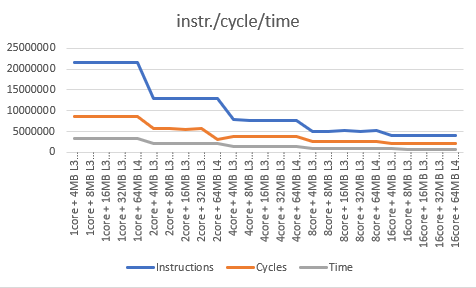
本次模擬了L3 cache不同size以及包含一個64MB L4 cache的情況。論instruction、cycles和time的比較，因為多核系統可以將指令透過不同cores平行執行的特性，因此單個core要負責的指令較少，而時間也較短。而power的話會隨著core的數量變多而增加。Energy和latency的部分則都差不多(詳情見分析之excel檔)

b. Submit the corresponding resulting file if you can’t screenshot in one figure. (i.e. sim.out)

如附檔(simulation\_data、excel以及圖片)

c. (bonus) Find the optimal performance under the specific condition. Paste the result images and configuration images in the file.

一張含有 桌 的圖片

自動產生的描述

如果只考慮time的話，16cores + 32MB L3 cache的時間最短，然而，多核且容量較大的配置會帶來較高的能耗(power)。若有L4 cache，則可以使整體的效能最好，執行時間短且time/power低，是為最佳的選項。但如果只有L3 cache，則多核的選項能帶給我們比較好的整體性能。