Stack/Accumulator ISA with five PDP11 addressing modes **James C. Brakefield (2021)** Most instructions use two bytes, this sheet has the three and four byte op-codes

Op	# ops	description	std. stack operation	detailed descripton	comments
ADD	1	Three input add		if the 2nd ddnnn field is same as first, third operand is omitted	additional op-code bits used for sign control & signed/unsigned/float
DIV	0.5	Two input dividend		if the 2nd ddnnn field is same as first, third operand is omitted	additional op-code bits used for sign control & signed/unsigned/float
MAC	0.5	Multiply/accumulate		if the 2nd ddnnn field is same as first, third operand is omitted	additional op-code bits used for sign control & signed/unsigned/float
MEDIAN	0.125	Three element median		if the 2nd ddnnn field is same as first, third operand is omitted	additional op-code bits used for sign control & signed/unsigned/float
LSL	0.125	Logical shift left using residue		if the 2nd ddnnn field is same as first, third operand is omitted	additional op-code bits used for sign control & signed/unsigned/float
LSR	0.125	Logical shift right using residue		if the 2nd ddnnn field is same as first, third operand is omitted	additional op-code bits used for sign control & signed/unsigned/float
ASR	0.125	Arithmetic shift right using residue		if the 2nd ddnnn field is same as first, third operand is omitted	additional op-code bits used for sign control & signed/unsigned/float
SELECT	0.125	Boolean select			Zero/non-zero 1st operand selects either 2nd or 3rd operand
MERGE	0.125	Boolean mask select			1st operand bit by bit selects 2nd or 3rd operand bits
MOV2	0.125	Two operands to or from data stack			Can be used for swap or two element shift
INSERT	0.125	Insert truncated source into destination			Uses 12-bit immediate or LSBs of operand
MAX	0.25	Three element max		if the 2nd ddnnn field is same as first, third operand is omitted	additional op-code bits used for sign control & signed/unsigned/float
MIN	0.25	Three element min		if the 2nd ddnnn field is same as first, third operand is omitted	additional op-code bits used for sign control & signed/unsigned/float
CALLRF	0.125	Relative call and set new frame		3rd byte specifies # results and # of parameters	FP & SP pushed to return stack as single non-program "address"
CALLF	0.125	Call and set new frame		specifies # results and # of parameters	FP & SP pushed to return stack as single non-program "address"
LDX	0.25	Load indexed		2nd register file operand is index value	Can be combined with all addressing modes, 2-bit index multiplier
STX	0.25	Store indexed		2nd register file operand is index value	Can be combined with all addressing modes, 2-bit index multiplier
BBR		Bit branch relative			
AND	0.5	complementation of two operands		Three input AND	three additional op-code bits used for Boolean complement
OR	0.5	complementation of two operands		Three input OR	three additional op-code bits used for Boolean complement
MUX	0.125	complementation of any of the three operands		Two input mux	two additional op-code bits used for Boolean complement
MAJ	0.125	complementation of any of the three operands		Three input majority	three additional op-code bits used for Boolean complement
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