ROC32_8 operator list

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register zero used to hold return address
register zero as index register reads as zero
Y scale factor is data size times (1 to 4)

five bit immediate field is value of -8..15 or length - 1 of postfixed immediate in bytes
last four registers are condition code, frame pointer, stack pointer & PC
combined interger & floating-point register file

format name	eventual layout	usage	address arithmetic
fmt24drsi	00xxxxxx ddddd i rrrrr sssss	basic 24-bit instruction	
fmt24drs	00xxxxxx ddddd 0 rrrrr sssss	R op S ->D	
fmt24dri	00xxxxxx ddddd 1 rrrrr nnnnn	R op immediate ->D	
fmt24dbx	00xxxxxx ddddd 0 bbbbb jjjjj	load/store base + scaled index	B + J * ds
fmt24dbn	00xxxxxx ddddd 1 bbbbb nnnnn	load/store base + offset	B + N
fmt24dr	00xxxxxx ddddd z rrrrr xxxxx	op R -> D; 32 single operand instructions	
fmt24dn	00xxxxxx ddddd n nnnnn nnnnn	eleven bit signed offset or immediate	PC + N
fmt32drsc	01xxxxxx ddddd i rrrrr sssss zzu ccccc	basic 32-bit instruction	
fmt32drsc	01xxxxxx ddddd 0 rrrrr sssss zzu ccccc	R op S ->D; execute on predicate match	
fmt32drnc	01xxxxxx ddddd 1 rrrrr nnnnn zvu ccccc	R op imm ->D; execute on predicate match	
fmt32dbjs	01xxxxxx ddddd 0 bbbbb sssss yyu jjjjj	load from base + index * scaling + offset	B + J * Y + S
fmt32dbjn	01xxxxxx ddddd 1 bbbbb nnnnn yyu jjjjj	load from base + index * scaling + offset	B + J * Y + N
fmt32dbjs	01xxxxxx ddddd 0 bbbbb sssss yy0 jjjjj	store to base + index * scaling + offset	B + J * Y + S
fmt32dbjn	01xxxxxx ddddd 1 bbbbb nnnnn yy0 jjjjj	store to base + scaled index + offset	B + J * Y + N
fmt32mbjs	01xxxxxx mmmmm 0 bbbbb sssss yy1 jjjjj	store immediate to base + index * scaling + offset	B + J * Y + S
fmt32mbjn	01xxxxxx mmmmm 1 bbbbb nnnnn yy1 jjjjj	store immediate to base + index * scaling + offset	B + J * Y + N
fmt32dr	00xxxxxx ddddd z rrrrr xxxxx xxu ccccc	op R -> D; 128 single operand instructions	
fmt32drst	01xxxxxx ddddd i rrrrr sssss zzu ttttt	op(R, S, T) -> D; triple operand instructions	
fmt32dn	01xxxxxx ddddd n nnnnn nnnnn nnn nnnnn	nineteen bit signed offset or immediate	PC + N
fmt40drsct	10xxxxxx ddddd i rrrrr sssss zzu ccccc xxx ttttt	basic 40-bit instruction with three source registers & predication	
fmt48drscte	11xxxxxx ddddd i rrrrr sssss zzu ccccc xxx ttttt xxx eeeee	basic 48-bit instruction with 3 source, 2 destination & predication	
fmt48drsctwe	11xxxxxx ddddd i rrrrr sssss zzu ccccc xww ttttt www eeeee	basic 48-bit instruction with 4 source, 2 destination & predication	

b	base address register #
c	condition code predicate (execute instruction if condition true)
d	result register #
ds	data size in bytes
e	2nd result register #
i	s is immediate field if i = 1
j	register # for scaled index
m	small constant or length of following immediate for store immediate value
n	small constant or length of following immediate
r	operand register #
s	2nd operand register #
t	3rd operand register #
u	update CC enable, for ST instructions is store immediate enable
v	swap operands enable
w	4th operand register #
x	op-code bits
y	2-bit code for: ds * (1..4)
z	negate/invert enables for one or two operands

Some 32-bit instructions support three operand operations
40-bit load/store instructions support predication
40-bit instructions support three operands and predication
40 and 48-bit instructions support CARRY mechanism: register field(s) for extended operand and extended result