FPGA Timeline & Applications

FPGAs past, present & future

Jim Brakefield

FPGA Application Areas

- Communications
- DSP
- Software-defined radio
- Aerospace and defense systems
- ASIC prototyping
- Medical imaging
- Computer vision
- Speech recognition
- Cryptography
- Bioinformatics
- Computer hardware emulation

$6-7B yearly sales

<u>Advantages:</u>

Low NRE

Low volume products

Updates/patches

Parallelism

Portable code

Soft dev || Hard dev

<u>Disadvantages:</u>

ASICs are cheaper, faster and lower power in high volumes

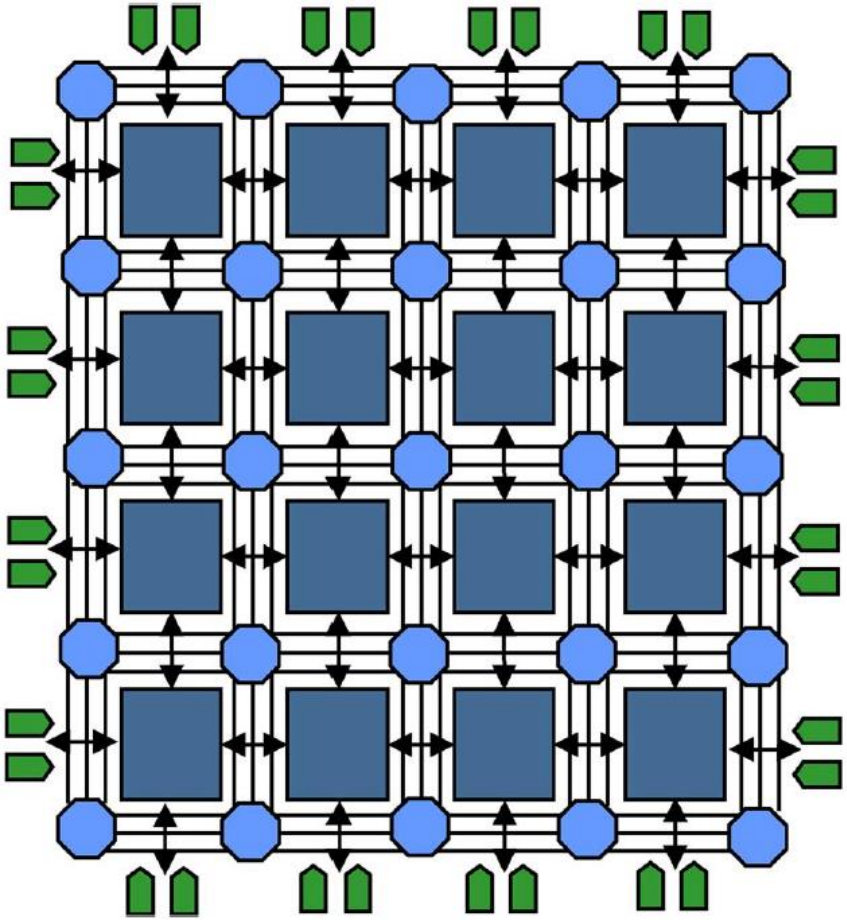
Intro: Experience

- PowerPC emulation of Pentium
  - Decided to learn VHDL 1995
- AMD/Vantis/Lattice Semi
  - Competive benchmarking 1998-2002
- OnBoard Software/BAE Systems 2004-2012
  - FLR-9, IP over 1553, Weather RADAR
- ROIS24_24uP
  - 24-bit soft core processor 2016

Intro: The Vendors

- Altera (now Intel): www.altera.com
  - Originally CPLDs, currently #2 in FPGAs.
- Cypress (under PSoC): www.cypress.com
  - Had line of CPLDs, now ARM + programmable IO
- Lattice Semiconductor: www.latticesemi.com
  - Originally memory, now diversifying away from FPGAs
- Microsemi (was Actel): www.actel.com
  - Originally anti-fuse, then flash, now SRAM & flash based
- Xilinx: www.xilinx.com
  - Originated FPGAs, tried anti-fuse, flash & CPLD, now #1

Intro: The FPGA



Generic FPGA diagram

Green: IOs

Squares: LUT groups/slices/blocks

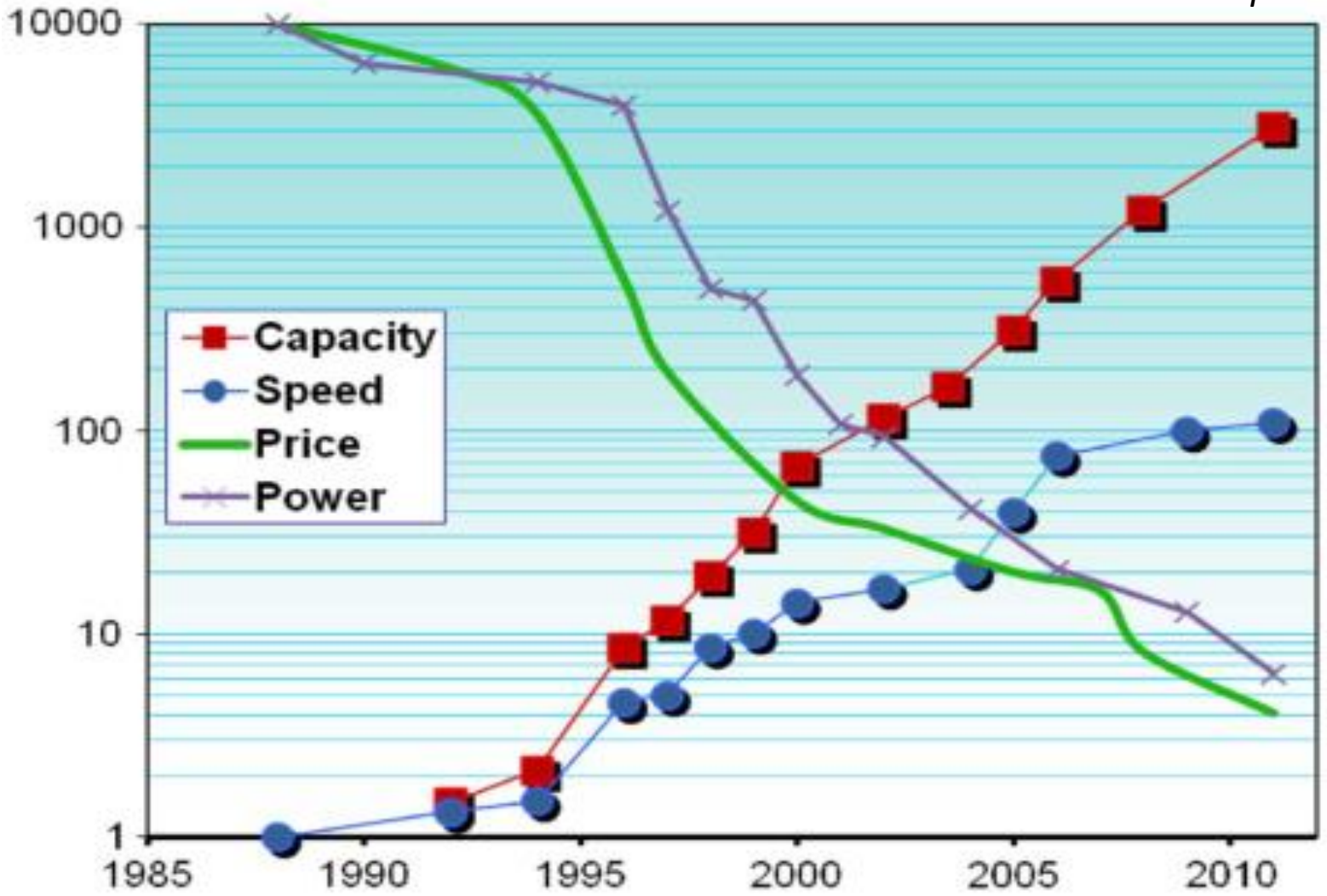
Octagons: Wiring interconnections

Lines: Wire segment bundles

From: Trimberger, 2015 Proc IEEE v103 #03 pg320

Intro: The FPGA

Not far off:
1GHz performance
7nm silicon
On chip DRAM



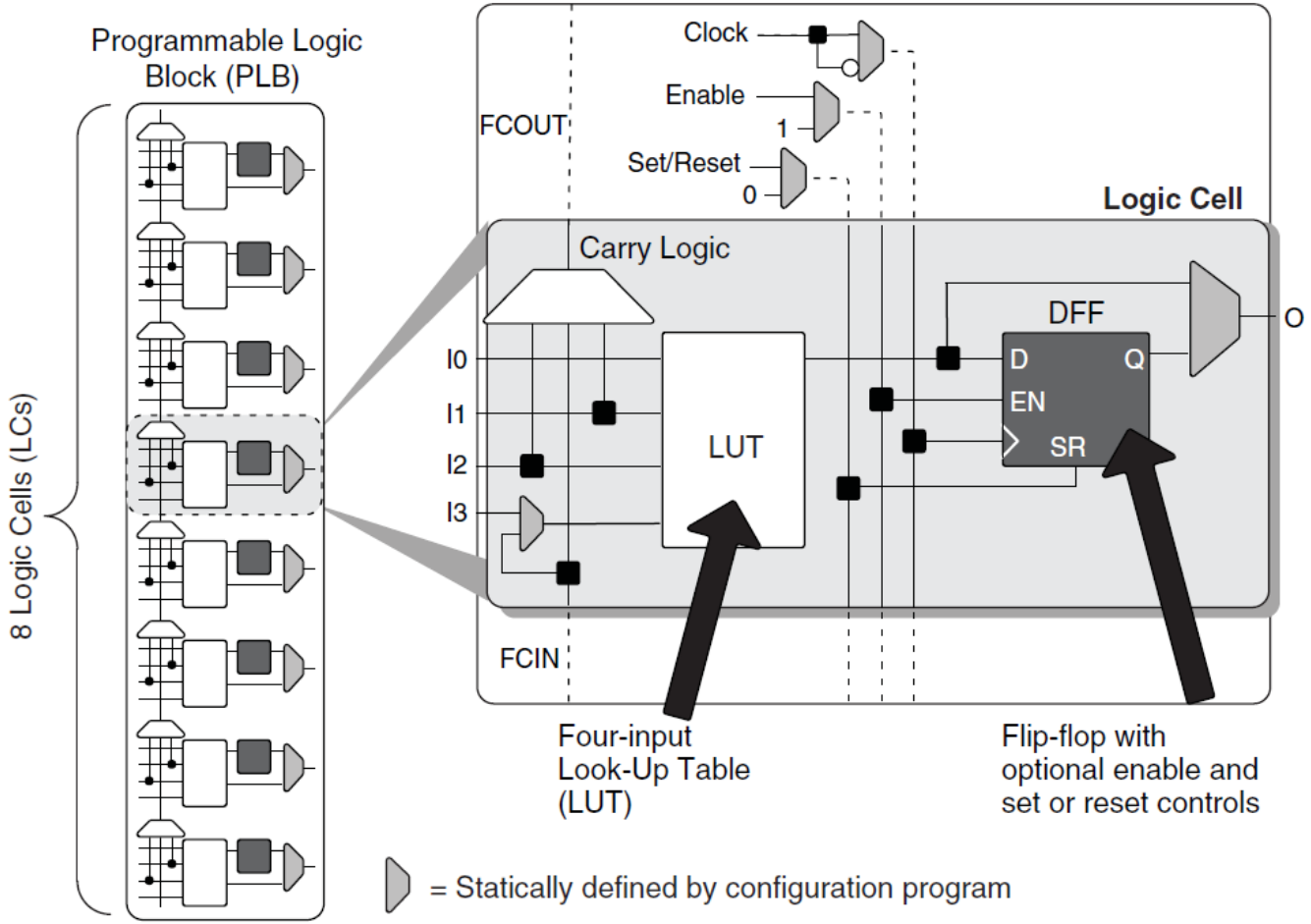
From: Trimberger, 2015 Proc IEEE v103 #03 pg318

Basic LUT (Look-Up Table)

Currently up to 2.5M LUTs
at 300-1000 LUTs/$

- 1985 LUTs plus DFF Xilinx XC2000
  - Clocking facilities
  - Configuration memory
  - Routing wires
- 1991 Carry chain Xilinx XC4000
  - LUT RAM (16x1)
  - Shift Registers

LUT + DFF



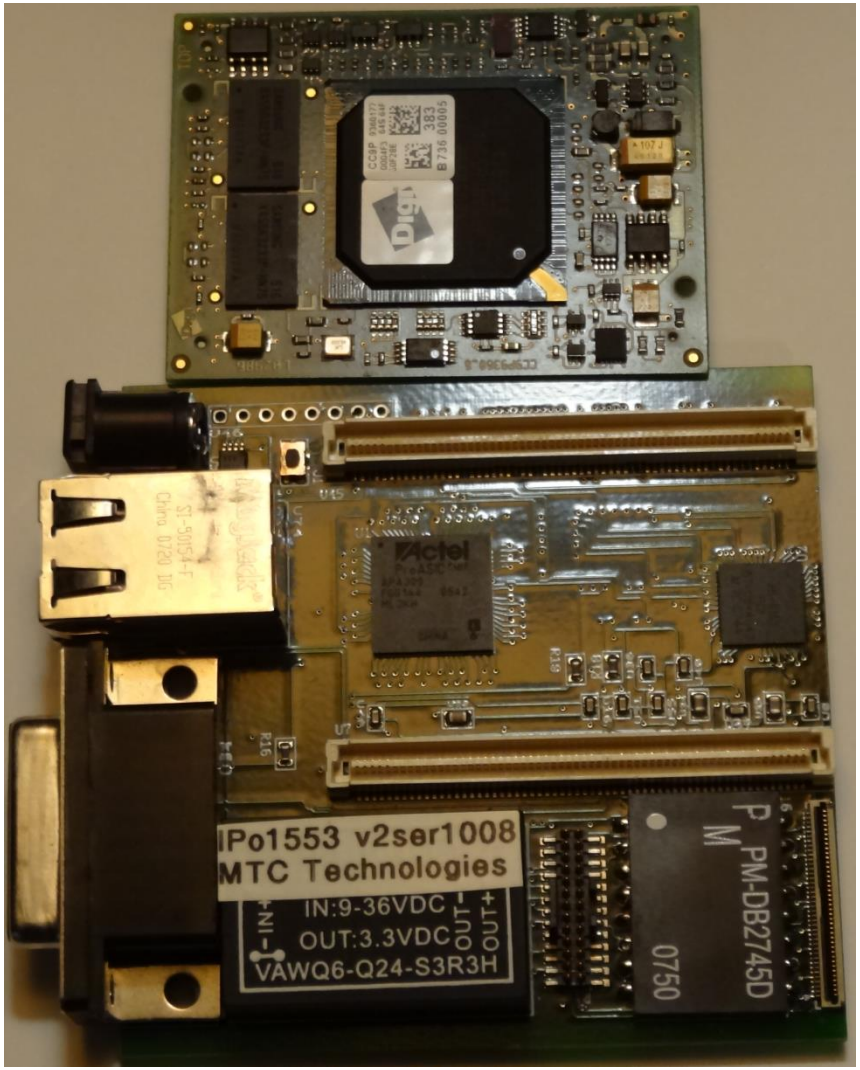
3LUTs tried
6LUTs in use
ALM: ~two 5LUTs with multiple configurations

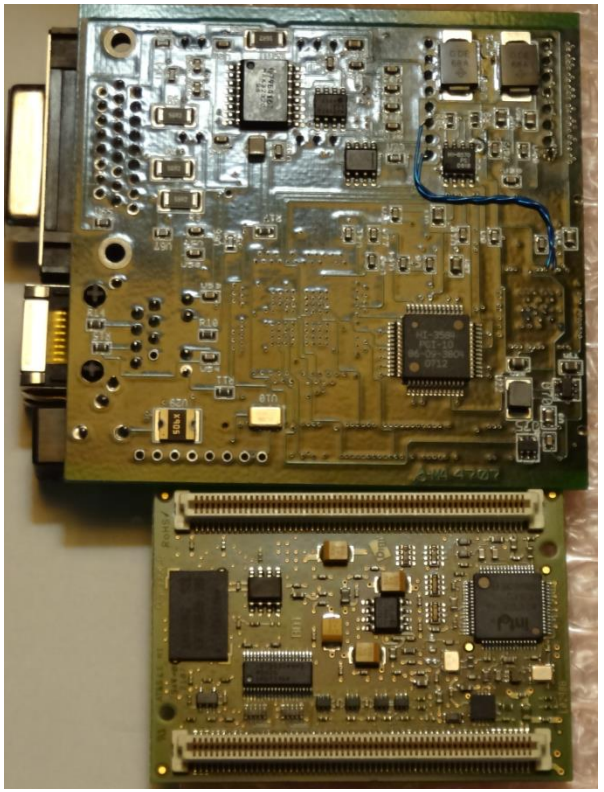
4LUT: 16 bits of memory & a 16:1 MUX

Lattice Semiconductor iCE40FamilyHandbook.pdf pg6-2

Uses:

"glue" logic
Reprogrammable (field changes)
Reliability (parts count and wiring reduction)





IPo1553 module (BAE Systems): ARINC 429, MIL-STD 1553, RJ45, CAN

Block RAM

up to ~7K block RAMs
up to 200M bits

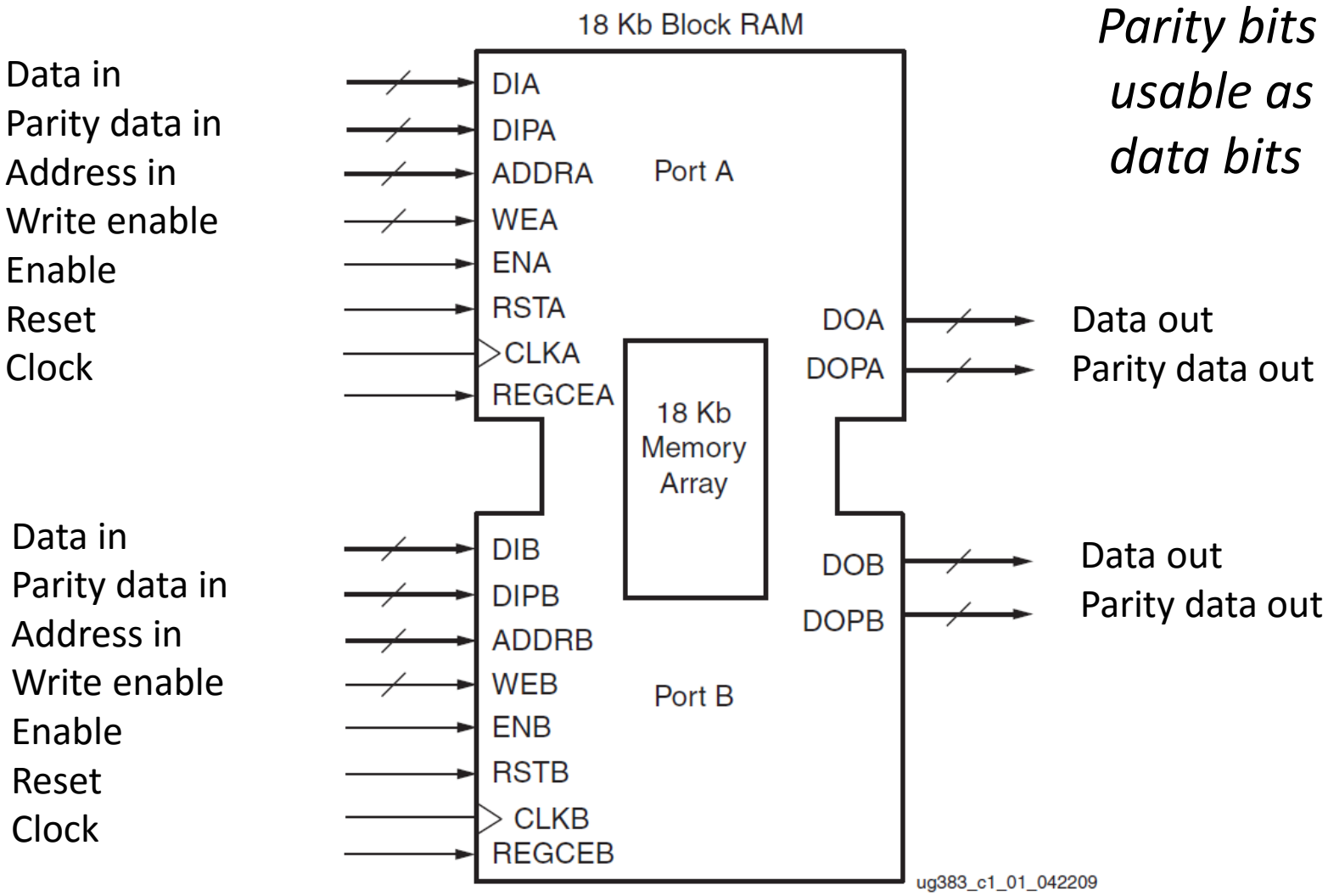
- 1995 Dual port RAM Altera FLEX
- Variable aspect ratio (on each port)

  16Kx1, 8Kx2, 4Kx4, 2Kx8/9, 1Kx16/18, 512x32/36
- A variety of RAM capacities

  LUT RAM (16x1), small block RAM (~32x18), block RAM (~512x36), large block RAM (~4Kx72)
- Uses:

  Buffers, FIFOs, shift registers, scratch pad memory, DSP coefficients, two single port RAMs, u-code

Block RAM



Parity bits usable as data bits

Xilinx Spartan-6 FPGA Block RAM Resources User Guide pg12

PLL (Phase Locked Loop)

FPGA internal clocks to 800MHz

- 1996 Altera FLEX 10K
- FPGAs can have dozens of distinct clocks
- All the analog (of the PLL) inside FPGA
- Uses: Reduce chip count, precise clock phase control

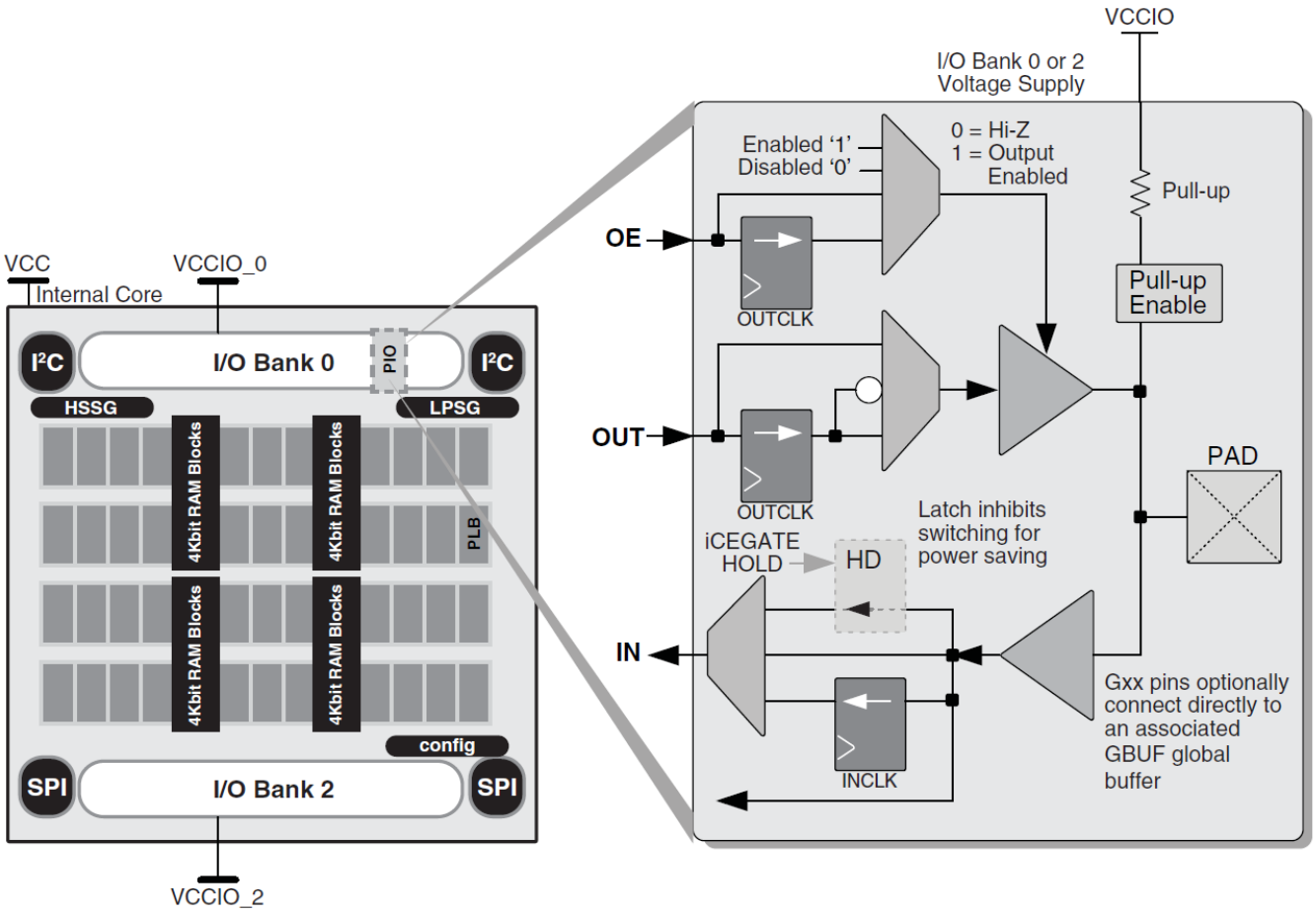
“ASIC” IO

- 1998 Universal IO Xilinx Virtex
- 1.2, 1.8, 2.5, 3.3, 5.0 VDC
  each bank of IO pins has its own power supply
- LVTTL, CMOS, HSTL, SSTL, PECL, LVDM …
  (via constraint file)
- 4, 8, 12, 16, 24ma, pullup/pulldown (ibid)
- resistive termination, slow/fast edges (ibid)
- Uses:

  general purpose IO, DRAM hookup, PWM, logic analyzer, etc.

“ASIC” IO

Global input buffers used for clocks and reset



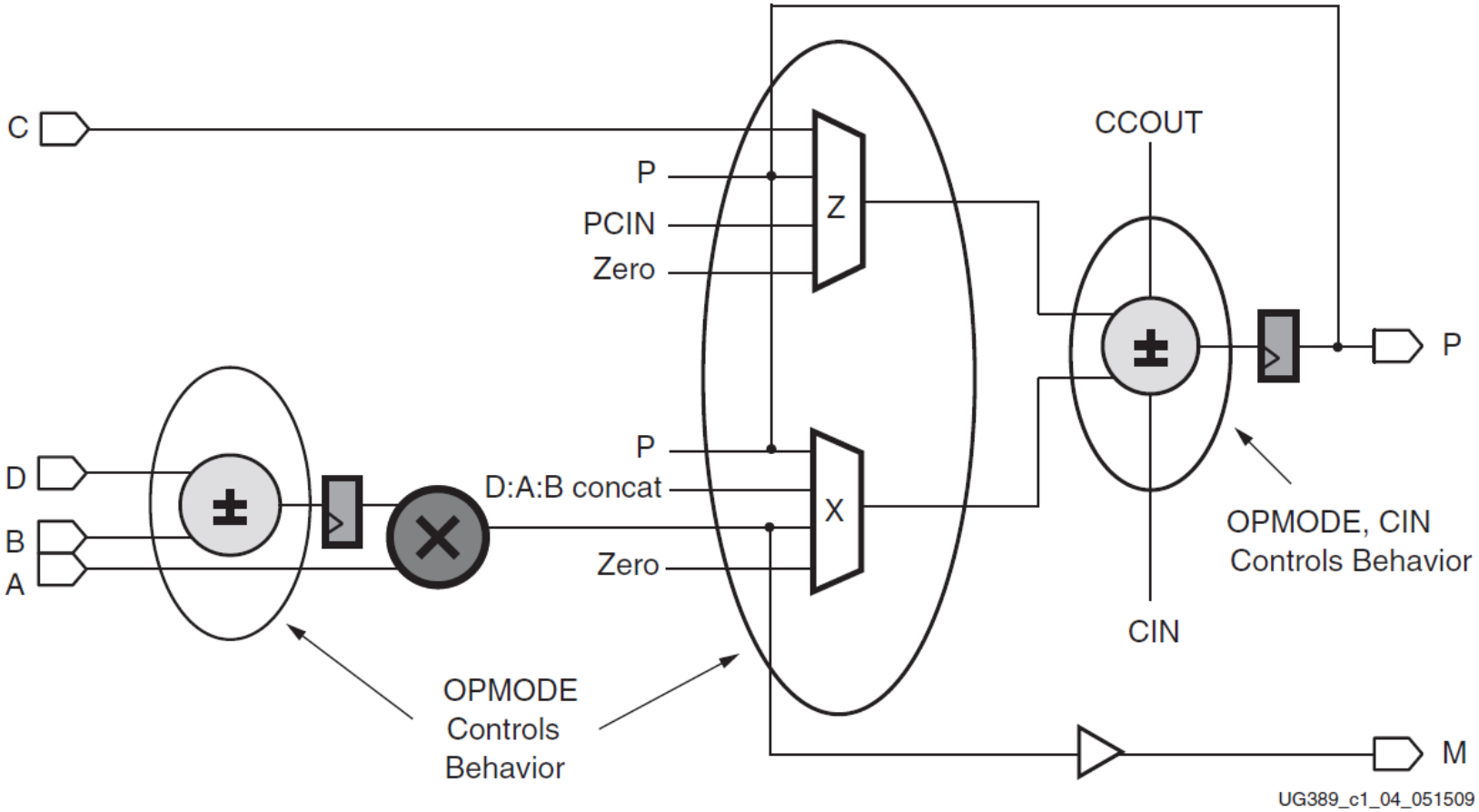
Lattice Semiconductor iCE40FamilyHandbook.pdf pg6-7

Multiply/accumulator

up to ~5K per chip running at 800MHz

- 2000 18x18 signed Xilinx Virtex-2
- 2002 DSP block Altera Stratix
- Initially no accumulator, accumulators now include ALU capability and floating-point
- Use pipelining for maximum speed
- Multiplier shapes: 16x16, 18x18, 18x27; (3)9x9, (2)18x18 or (1)27x27
- Uses: DSP, FFT, ALU

Simplified DSP slice



Xilinx Spartan-6 FPGA DSP48A1 Slice pg 17

SERDES (Serialize/De-serialize)

up to ~100 per chip
up to 32GHz

- 2001 Source synchronous transceiver
  Xilinx Virtex-II
- 2002 SERDES Transceiver
  Xilinx Virtex-II Pro
- Uses:

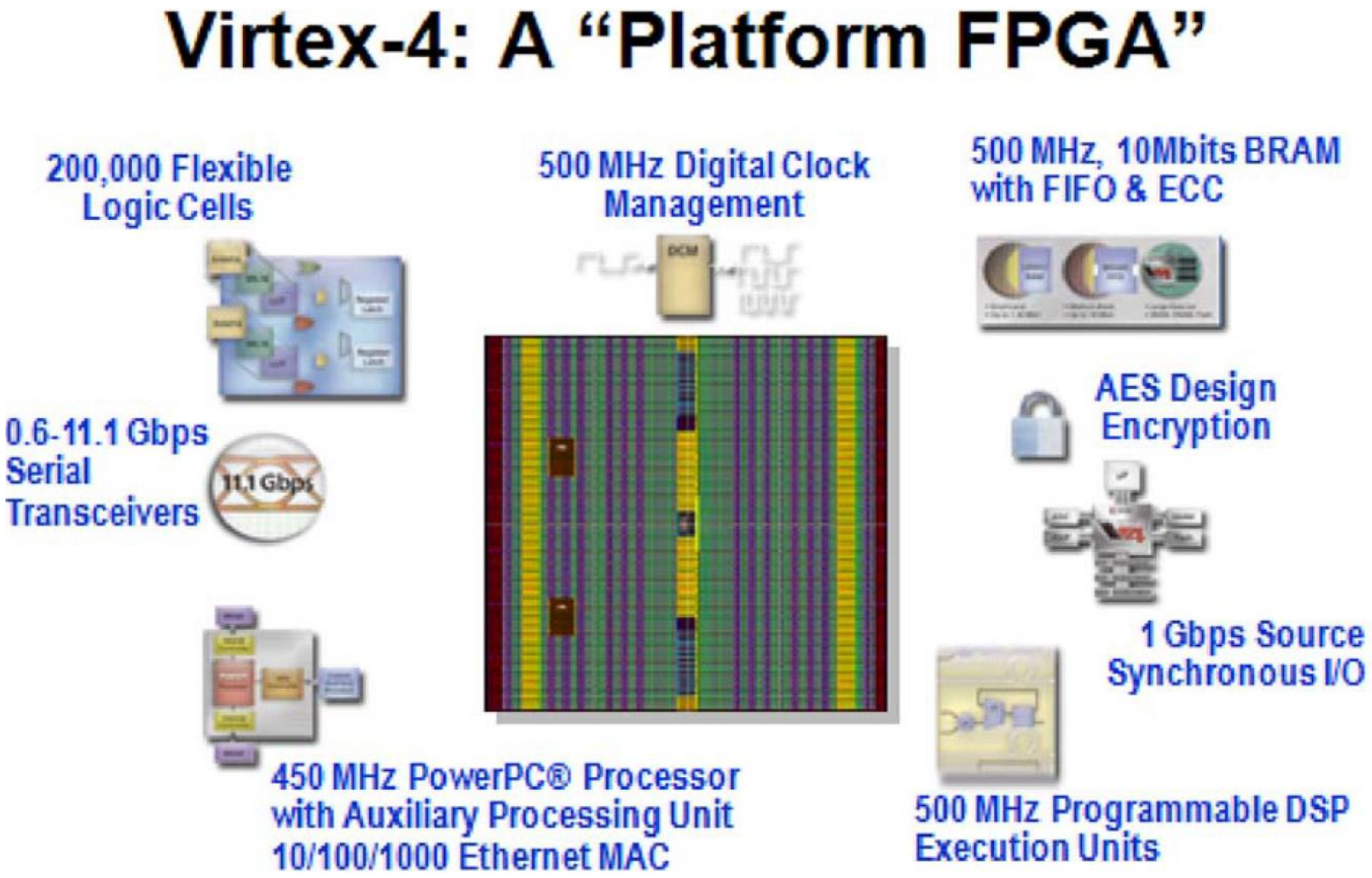
  Communication links: Fiber connections, Ethernet, PCI-express, Interlaken, etc

ASIC processor(s)

1 to 6 per chip, 100MHz to 1.5GHz

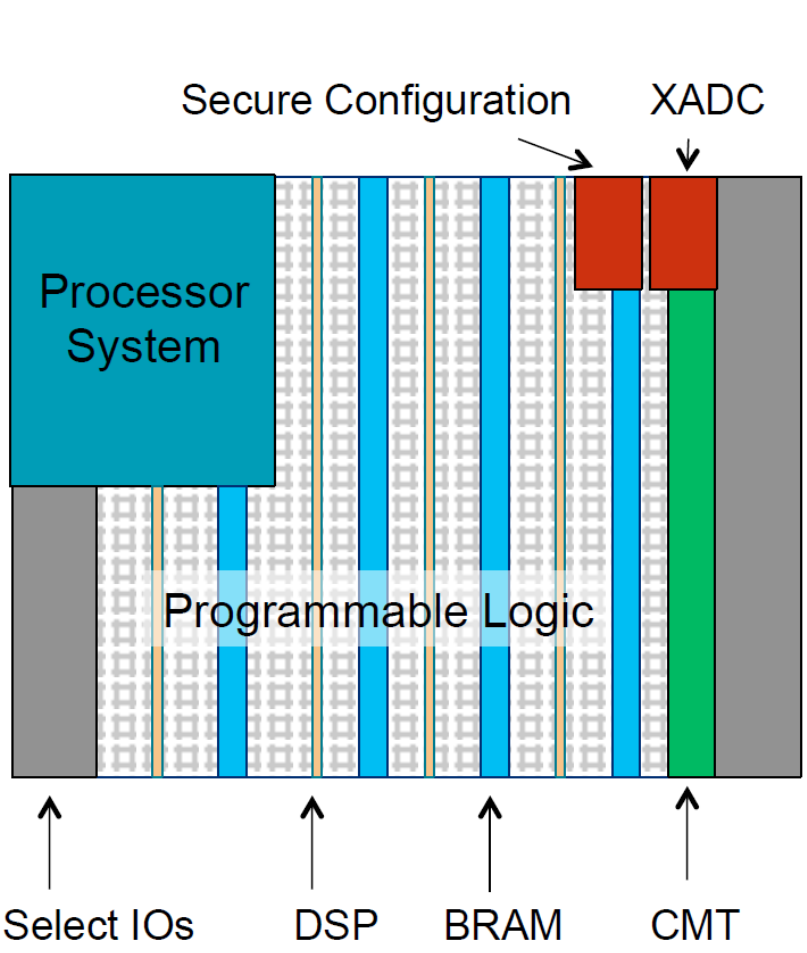
- 2000 ARM 9 Altera Excalibur
- 2002 PowerPC Xilinx Virtex-II Pro
- 2010 ARM Cortex M3 Actel Smart Fusion
- 2010 ARM dual Cortex A9
  Xilinx Zynq, Altera Cyclone V
- 2015 ARM quad A53 & dual R5, GPU
  Xilinx Zynq Ultrascale+
- All have microprocessor peripherals
  fast ones have cache & MMU
- Uses: Reduce chip count, cleaner interface between uP and FPGA fabric

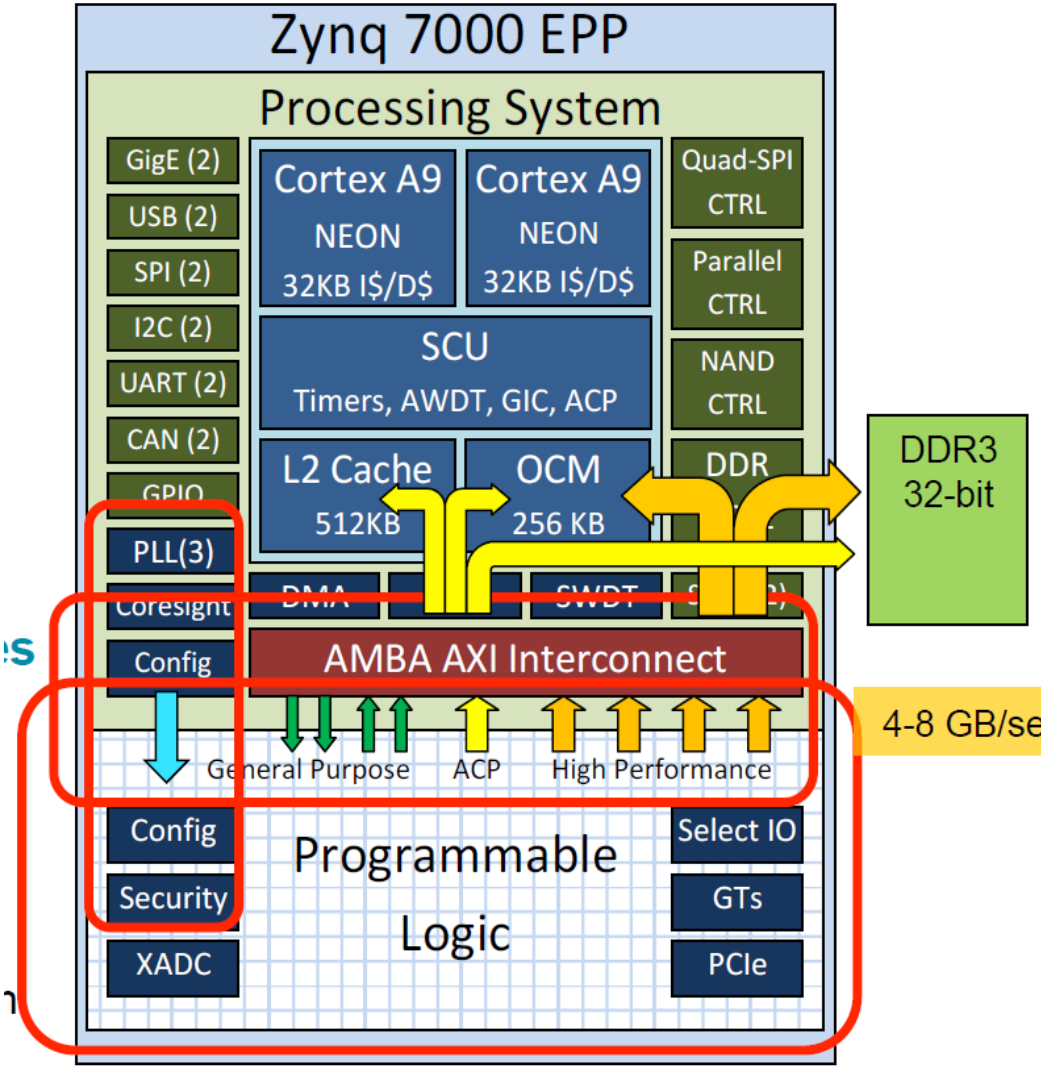
SOC chip



From: Trimberger, 2015 Proc IEEE v103 #03 pg327

Zynq: ARM + FPGA chip



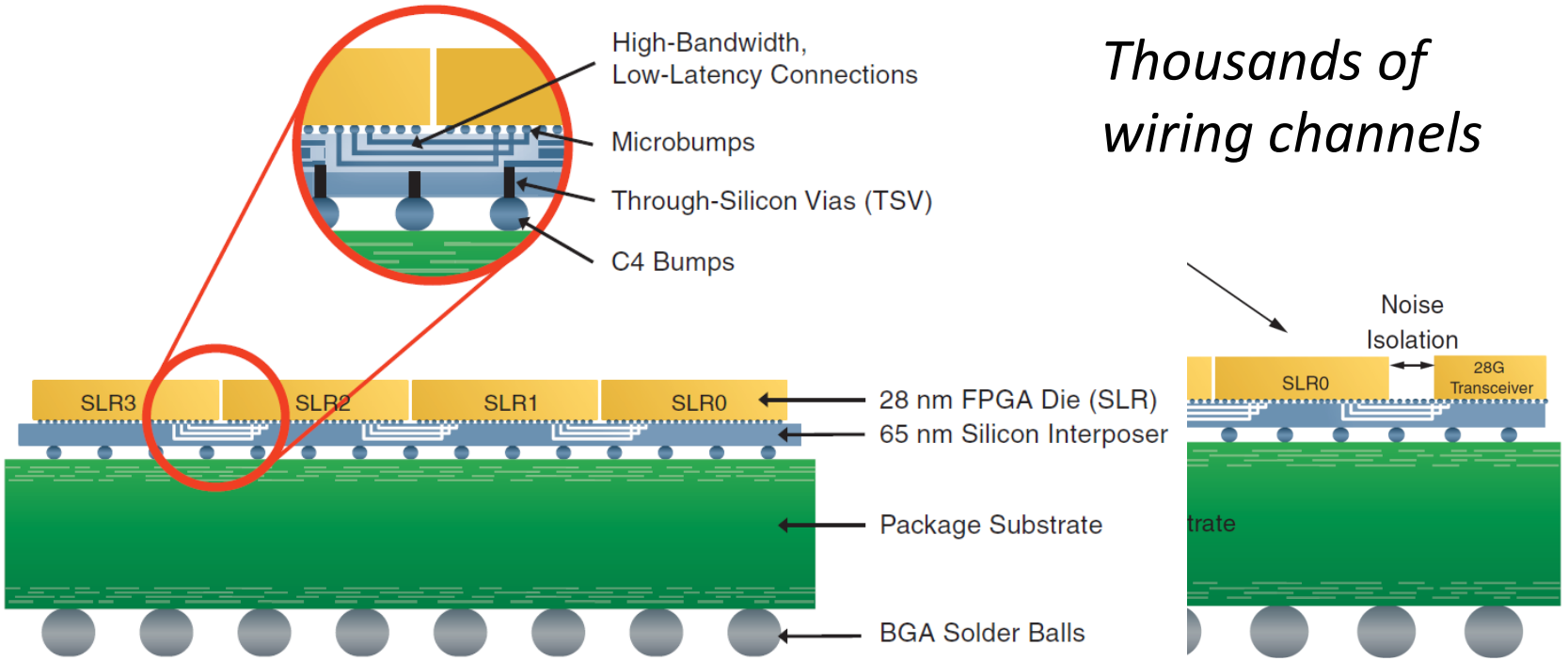


HC23.18.322.Zynq-7000-EPP-Dutta_Xilinxrevised.pdf

Silicon interposer (3D silicon)

- 2009 Multi-chip FPGA Xilinx Virtex-6

Uses: Yield improvement, reduced wiring capacitance, augmentation with SERDES & DRAM chips



Thousands of wiring channels

Xilinx white paper #380 pg 4 & 7, 2012: Stacked Silicon Interconnect Technology

HLS (High Level Synthesis)

"Work in Progress"

- 1980s VHDL & Verilog RTL
  (Register Transfer Language)
- 2004 C, C++ or SystemC to VHDL/Verilog
  Matlab to VHDL/Verilog
- 2011 Xilinx bought AutoESL, incorporated HLS technology into their Vivado tool.
- 2011 OpenCL for uP, DSP, GPU & FPGAs
- Uses: Productivity
  FPGA development by software engineers

Floating-point

- 2015 32-bit Add/subtract/multiply
  Altera Arria-10 & Stratix-10
- IEEE floating-point library: exponent & mantissa size bit adjustable
- Uses:

  Super computer applications

  Wide dynamic range DSP

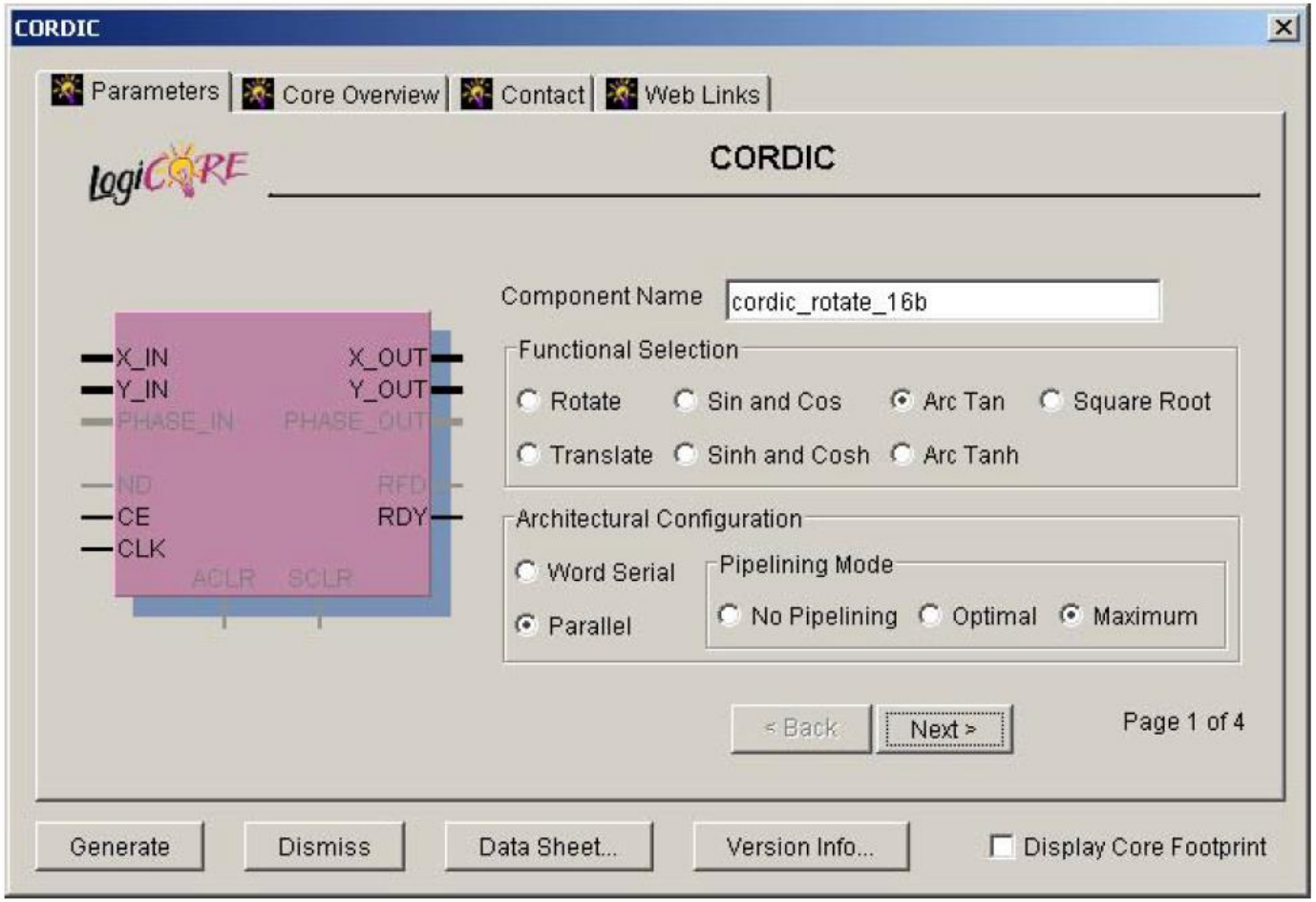
IP (Intellectual Property)

Pre-packaged modules, macros & generators

- TTL logic equivalents (with schematic entry)
- Simple macros (also with schematic entry)
- Vendor free IP: soft-core processors, CORDIC, FFT, Floating-point, PCI-express, memory controllers …
- Open source IP: www.opencores.org
- Vendor and 3rd party non-free IP (various interfaces, soft core processors, image processing…)
- Uses: save time & money

Xilinx CORDIC GUI

Ray Andraka 1998: A survey of CORDIC algorithms for FPGA based computers



FPGA Code & Test Process

- Schematic capture (doesn't scale)
- Or write RTL (Register Transfer Logic) which evolved into Verilog and VHDL (1980s)
- Simulate
  - Faster than compile/map-pack-P&R-bit-stream/download
  - Use test-bench
  - Not perfect
- Compile: synthesize VHDL/Verilog to gates or FPGA primitives
- Map, Pack, timing driven Place & Route
- Bit-stream generation
- Download & test

Low End Applications

1.5-3mm pkg, 2K LUTs
.1Mb block RAM

- Glue logic
  - Connection of disparate devices to a uP
  - Last minute patches

20K LUTs, 40 DSP,
1Mb block RAM

- Logic funnel
  - Legacy design re-hosting
  - Soft core processors & peripherals (www.opencores.org)

Mid-scale Applications

200K LUTs, 1K DSP,
15Mb block RAM

- Communications: Internet routers, Telephone switches, Protocol conversion
- Signal Processing: Software defined radio, Camera, Audio, Video, Radar …
- Test & Measurement: high speed A2D & D2A,
- Big science: Super-collider, SETI, etc.
- Aerospace: radiation hardened, military temperature range
- SOC (System On a Chip): driverless vehicles

High End Applications

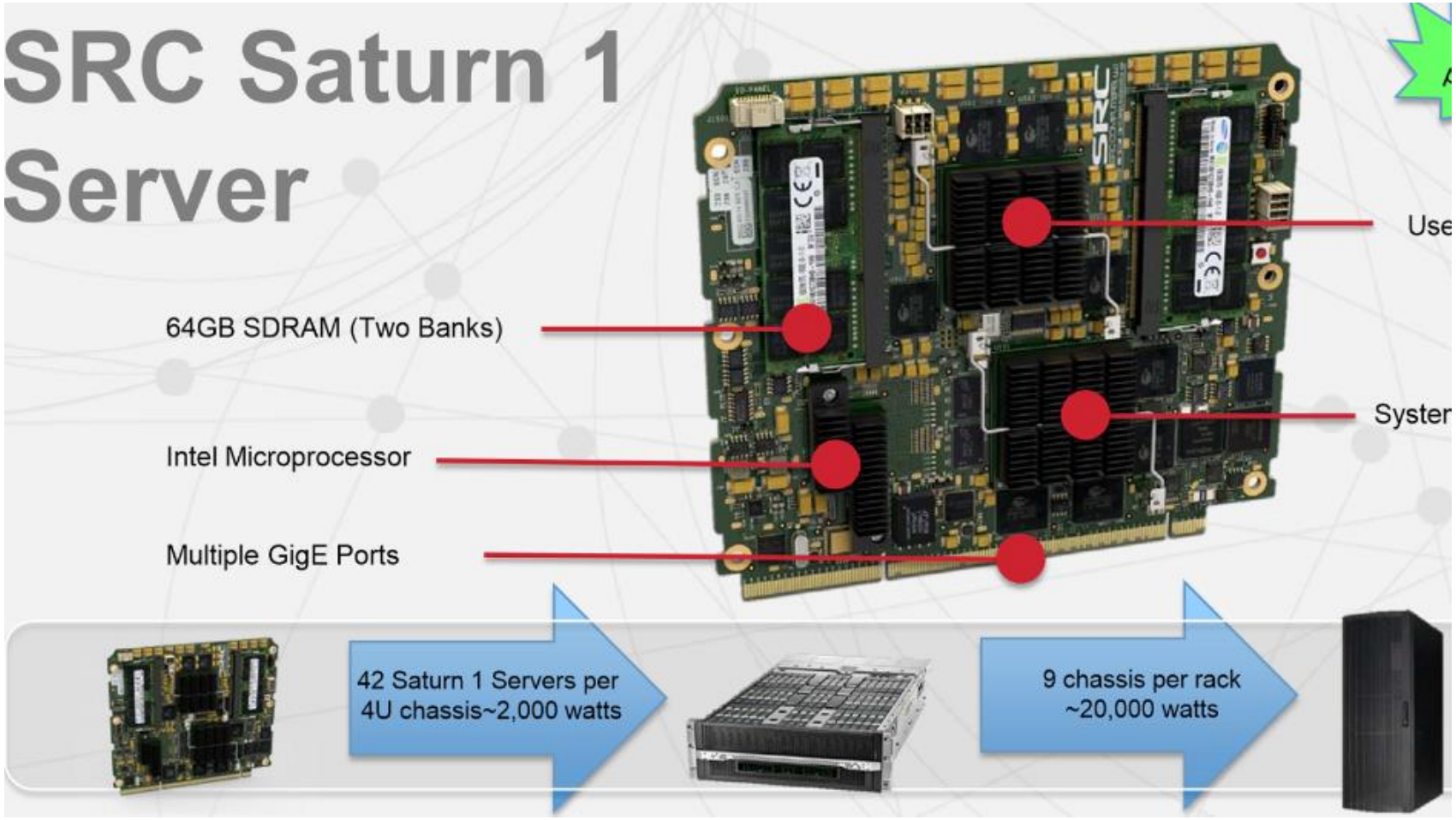
2.5M LUTs, 5K DSP,
200Mb block RAM

- ASIC (Applications Specific Integrated Circuit) emulation
- High end weapons, who knows what else?
- Super-computing coprocessor

  Intel bought Altera
- Wall street (high frequency trading)
- Research

High End Applications

Typical FPGA & uP module



High End Applications

ALDEC HES-7
Board using
(6) Virtex-7 2000
with 1.1M LUTs
each
Used to simulate
600M ASIC gates

References

- *Three Ages of FPGAs: A Retrospective*…, Steve Trimberger, Proc. IEEEE v103#3p318, 2015

  www.cpe.virginia.edu/grads/pdfs/January%202016/VLSI.pdf

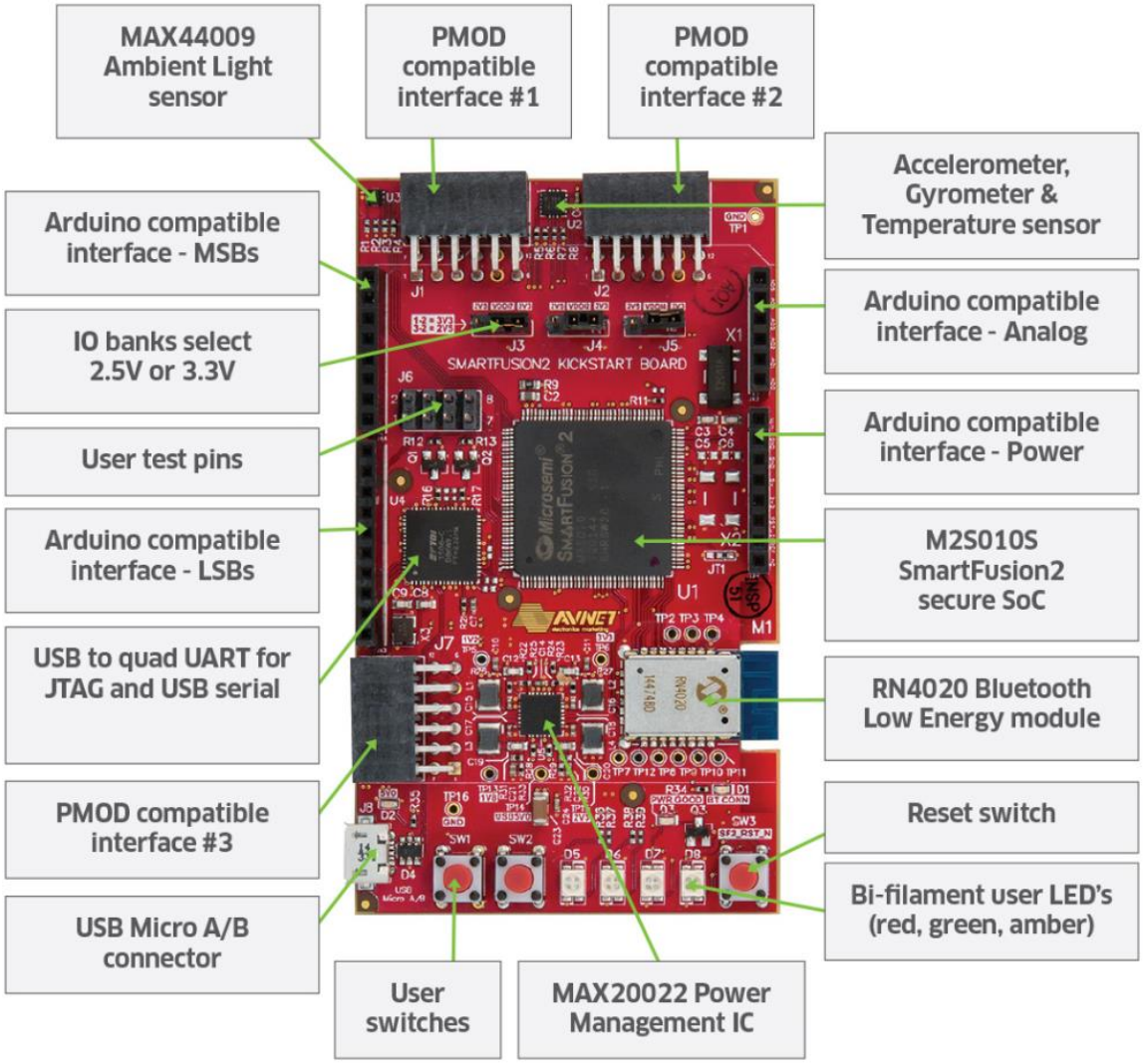
  forums.xilinx.com/t5/Xcell-Daily-Blog/Video-The-Three-Ages-of-the-FPGA-and-the-Age-of-the-Design/ba-p/644396
- *Xilinx Part Family History*, John Lazzaro,

  www-inst.eecs.berkeley.edu/~cs294-59/fa10/resources/Xilinx-history/Xilinx-history.html
- *Altera History*, corporate,

  www.altera.com/about/company/history.html
- HLS (High Level Synthesis)

  en.wikipedia.org/wiki/High-level_synthesis

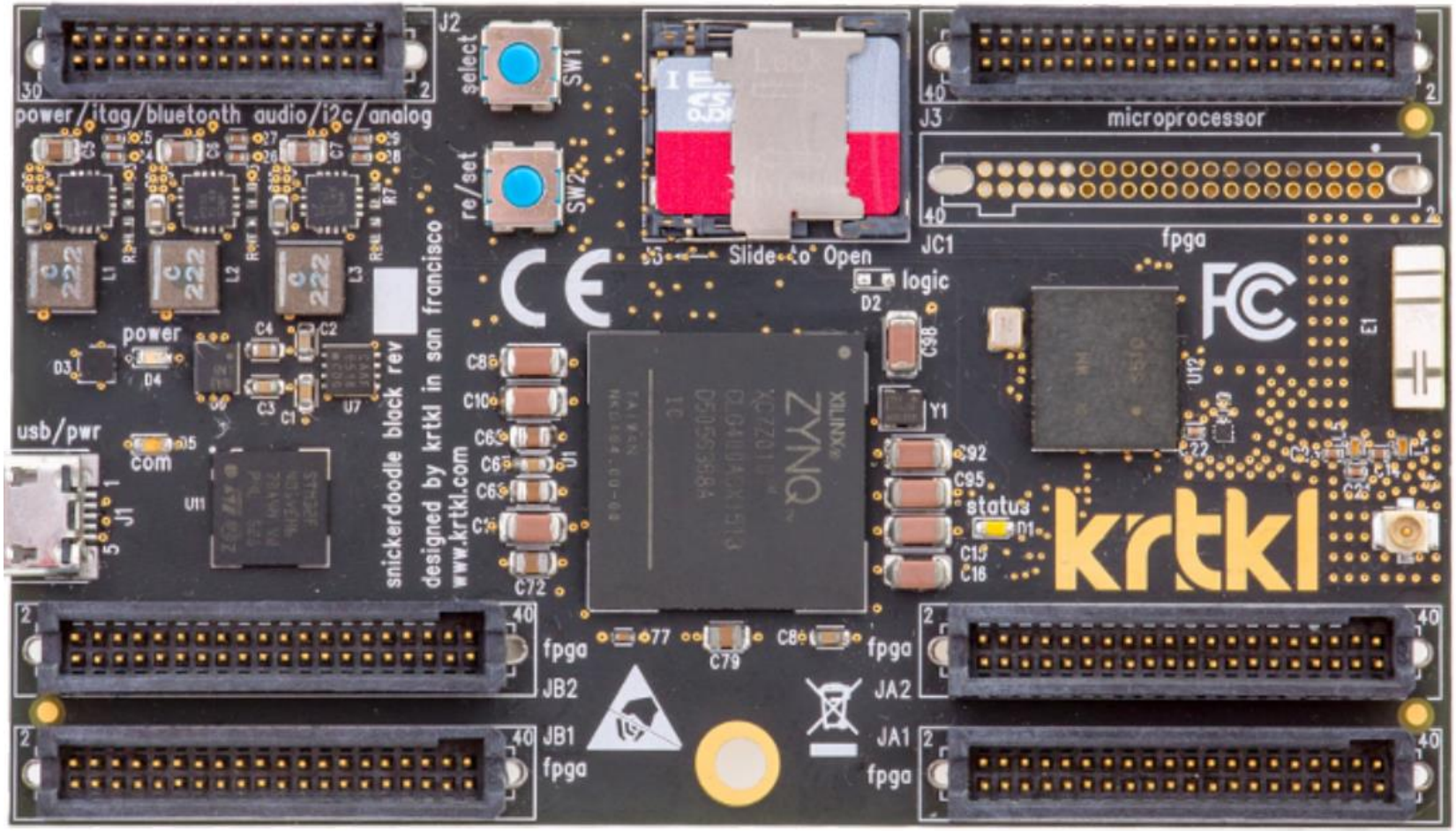
Actel SmartFusion2 KickStart Kit



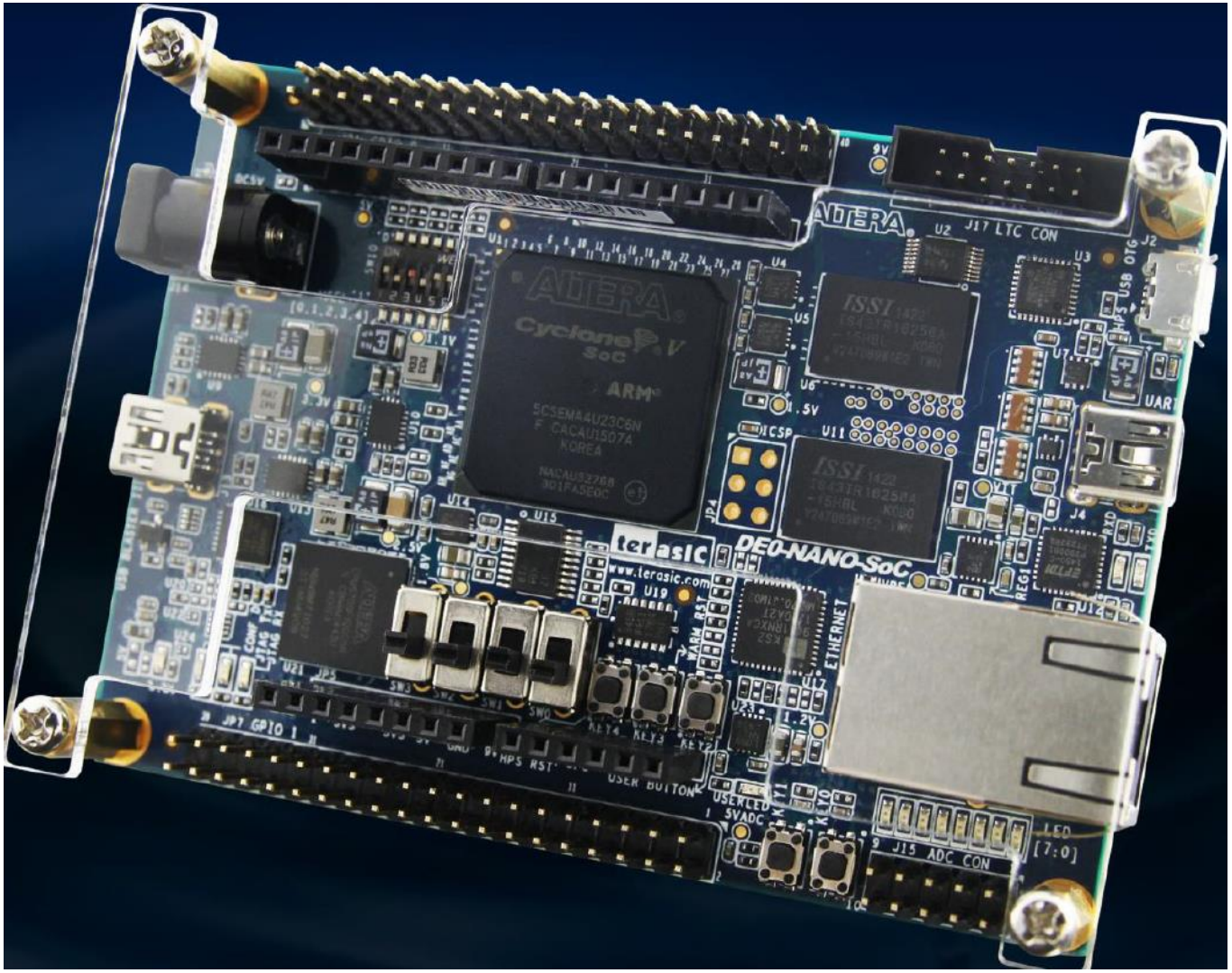
Avnet
AES-SF2-KSB-G
$59.95
Has ARM
Cortex M3

Xilinx Zynq SOC kit

Snickerdoodle with WiFi & Bluetooth $72



Altera Cyclone V SOC kit



Terasic
DE-0
Nano SoC
$99

Cypress PSoC5 kit

CY8CKIT-059 for $10 with: ARM Cortex M3, Analog & Digital IO