FPGA talks and reports of James Brakefield

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Date	Format	Topic	Author	Nature	Where	Web Link	location	Title	Comments	Abstract
2/24/2025	pptx	uP Arch	JCB	info	C16	https://events.vtools.ieee.org/m/467923	Web page	A Digital Processor of RISC Variety Suitable for Architecture Exploration	Includes slides from earlier 2/16/2016 talk Covers TROC16; 6 attachments	RISC computer architecture of my design in an effort to achieve high code density, deterministic execution and a uniform base for diversity. Architecture provdes for four data sizes and four data types.
2/21/2023	pptx	FPGA ed	JCB	info	C16	https://events.vtools.ieee.org/m/345505	Web page	Progress report and Education Review and update on FPGA Boot Camp grant	Abbreviated slides, full slides at github	A look at more advanced FPGA education: boards, tools and research. Slide deck includes link to $20 FPGA Kit sildes
1/27/2023	pptx	FPGA	JCB	report		https://github.com/jimbrake/20-dollar-FPGA-kit	Git hub	A $20 FPGA kit	Pictures of each component on the web page	One of the goals of the FPGA Boot Camp grant was a lowest cost FPGA kit. Using a $14 FPGA board from China it is possible.
3/22/2022	pptx	FPGA ed	JCB	info	C16	https://events.vtools.ieee.org/m/306653	Web page	Economies of Scale for FPGA Education	AKA Low Cost FPGA Boards	idea is to do for FPGAs what Raspberry Pi and Arduino have done for microprocessor education
10/20/2020	ppt	Sys Arch	JCB	info	LMAG C16	https://events.vtools.ieee.org/m/241803	Web page	Legacy Updates for Avionics	Work at BAE, neat pictures	Work on RIU, FLR-9 and IPo1553, all used FPGAs
2/19/2020	pptx	gaming	JCB	info	C16	https://events.vtools.ieee.org/m/220917	Web page	Review of the MiSTer Gamming Console	Raffled Altera card	MiSTer is an open project that aims to recreate various classic computers, game consoles and arcade machines, using modern hardware.
5/23/2018	pptx	FPGA	JCB	info	Austin Consult	https://events.vtools.ieee.org/m/173193	Git hub	FPGA Chips: Introduction, History, and Applications	PoK-e-Jo's Smokehouse	30 years of FPGAs & are now into their 3rd generation. A way to study them & their applications is the timeline & their expanding capabilities.
4/17/2018	pptx	uP Arch	JCB	info	C16	https://events.vtools.ieee.org/m/170930	Web page	**Soft-Core CPUs An inventory of ~600 designs**	https://github.com/jimbrake/cpu_soft_cores	One of the most exciting parts of learning VHDL or Verilog is creating a CPU of your own design.
6/16/2016	pptx	FPGA	JCB	info	LMAG	https://events.vtools.ieee.org/m/135581	Web page	FPGA chips: Intro, History and Applications	Very dated	30 years of FPGAs & are now into their 3rd generation. A way to study them & their applications is the timeline & their expanding capabilities.
3/7/2016	ISE proj	uP Arch	JCB	report	open cores	https://opencores.org/projects/rois	Git hub	Register Oriented Instruction Sets.	rois24_24min.zip /jimbrake/ISA-Exploratorium/tree/ROIS24_24	architectural exploration with a goal of a high performance FPGA soft core processor
2/16/2016	pptx	FPGA to uP	JCB	info	C16	https://events.vtools.ieee.org/m/38087	Web page	DIY soft-core uP Microprocessor design using an FPGA	Now has correct slides	will cover FPGA resource utilization, instruction set design, data path considerations, getting to "Hello World" & completing the implementation.
3/17/2015	pptx	FPGA	JCB	info	C16	https://events.vtools.ieee.org/m/32967	Web page	Le Grande Tour of FPGA Land	posted 2022 slide deck version, borad prices out of date	a simple introduction to FPGAs, their role, their limitations and promise with some mention of hardware description languages
2/22/2014	pdf, xlsx	soft uP	JCB	spread sheet	open cores	https://opencores.org/projects/up_core_list/	Web page	An inventory of soft processor cores. Processor project at www.opencores.org	https://github.com/jimbrake/cpu_soft_cores	An Inventory of mostly open-source Soft Core Processors. Although many have FPGA stats, many do not. Very large spreadsheet
2/15/2006	ppt	FPGA	JCB	info	On Board		Git hub	Introduction to Programmable Logic as Software Process	Presented to SASPIN	FPGA 101 and its process aspect
4/8/2005	ISE	uP Arch	JCB	report	open cores	https://opencores.org/projects/lem1_9min	Web page	Logic Emulation Machine Processor project at www.opencores.org & github.com/jimbrake/lem1_9min	Four new variants of LEM1_9 are now implemented:	Small soft core processors that operate on a single bit (or four bits) of data at a time. Can be used for logic simulation, software interrupt handlers, low resource soft-core processing and BCD calculators.
11/29/2004	pdf	FPGA	JCB	info	Trinity Un		Git hub	Trinity University classroom presentation: FPGA RAD Process for micro-controller design	LEM1_9min talk	Design & Implement a Custom Micro-Controller in One Week or Less
6/27/2004	pdf	NN	JCB	info	Santa Fe		Git hub	**Use of Neural Models for Cognitive Processing**	2004 Sandia-UNM Cognitive Systems Workshop	Results of a feasibility study show that system level neuron and synapse models can be implemented in affordable scalable real-time systems

Column B	Date	presentation date or publication date
Column C	Format	powerpoint, PDF, txt, scanned pdf, docx, doc, xlsx, xilinx ISE project
Column D	Topic	one or two words
Column E	Author	JCB: James C. Brakefield, others as listed in comments
Column F	Nature	info (STEM level presentation), course, paper, patent, report
Column G	Where	Where presented, often IEEE Lonestar section at LMAG or Computer chapter
Column H	Web Link	Web page for paper or presentation
Column I	location	Location of slides/paper: listed Web page, Github (github/jimbrake), opencores.org, other
Column J	Title	Web page title and pptx file title may differ
Column K	Comments	Side information
Column L	Abstract	Culled from web page announcement or source file