Presentations, papers,

Date	Format	Topic	Author	Nature	Where	Web Link	location
2/24/2025	pptx	uP Arch	JCB	info	C16	https://events.vtools.ieee.org/m/467923	Web page
2/26/2024	pptx	Niklaus Wirth	JCB	info	C16	https://events.vtools.ieee.org/m/404641	Web page
11/6/2023	pptx	fltg-pt	JCB	info	C16	https://events.vtools.ieee.org/m/381287	Web page
2/21/2023	pptx	FPGA ed	JCB	info	C16	https://events.vtools.ieee.org/m/345505	Web page
1/27/2023	pptx	FPGA	JCB	report		https://github.com/jimbrake/20-dollar-FPGA-kit	Git hub
10/15/2022	pptx	FPGA ed	JCB	FPGA course	St. Marys	https://events.vtools.ieee.org/m/329364	Git hub
9/3/2022	pptx	FPGA ed	JCB	FPGA course	St. Marys	https://events.vtools.ieee.org/m/321263	Web page
8/27/2022	pptx	FPGA ed	JCB	FPGA course	St. Marys	https://events.vtools.ieee.org/m/321262	Web page
7/16/2022	pptx	FPGA ed	JCB	FPGA course	St. Marys	https://events.vtools.ieee.org/m/318519	Web page
6/25/2022	pptx	FPGA ed	JCB	FPGA course	St. Marys	https://events.vtools.ieee.org/m/317075	Web page
6/16/2022	pptx	FPGA ed	JCB	FPGA course	St. Marys	https://events.vtools.ieee.org/m/316786	Web page
5/25/2022	pptx	FPGA ed	JCB	FPGA course	St. Marys	https://events.vtools.ieee.org/m/317075	Web page
5/18/2022	pptx	FPGA ed	JCB	FPGA course	St. Marys	https://events.vtools.ieee.org/m/316786	Web page
5/11/2022	pptx	FPGA ed	JCB	FPGA course	St. Marys	https://events.vtools.ieee.org/m/316279	Web page
3/22/2022	pptx	FPGA ed	JCB	info	C16	https://events.vtools.ieee.org/m/306653	Web page
6/7/2021	text	Sys Arch	JCB	info	note	https://www.embeddedrela	Web page
3/16/2021	pptx	ICs	JCB	info	LMAG C16	https://events.vtools.ieee.org/m/263773	Web page
10/20/2020	ppt	Sys Arch	JCB	info	LMAG C16	https://events.vtools.ieee.org/m/241803	Web page
2/19/2020	pptx	gaming	JCB	info	C16	https://events.vtools.ieee.org/m/220917	Web page

9/17/2019	pptx	fltg-pt	JCB	info	C16	https://events.vtools.ieee.org/m/203892	Web page
10/19/2018	pptx	uP timeline	JCB	info	LMAG	https://events.vtools.ieee.org/m/178555	Web page
5/23/2018	pptx	FPGA	JCB	info	Austin Consult	https://events.vtools.ieee.org/m/173193	Git hub
4/17/2018	pptx	uP Arch	JCB	info	C16	https://events.vtools.ieee.org/m/170930	Web page
7/20/2017	pptx	uP ed	JCB	info	LMAG	https://events.vtools.ieee.org/m/46028	Web page
6/16/2016	pptx	FPGA	JCB	info	LMAG	https://events.vtools.ieee.org/m/135581	Web page
3/7/2016	ISE	uP Arch	JCB	report	open cores	https://opencores.org/projects/rois	Git hub
2/16/2016	pptx	FPGA to uP	JCB	info	C16	https://events.vtools.ieee.org/m/38087	Web page
3/17/2015	pptx	FPGA	JCB	info	C16	https://events.vtools.ieee.org/m/32967	Web page
2/22/2014	pdf, xlsx	soft uP	JCB	spread sheet	open cores	https://opencores.org/projects/up_core_list/	Web page
4/8/2005	ISE	uP Arch	JCB	report	open cores	https://opencores.org/projects/lem1_9min	Web page
4/6/1999	pdf	fltg-pt	JCB	patent	USPTO	https://patents.google.com/patent/US5892697A/en	Web page
10/1/1991	scan pdf	Forth Journ	JCB	paper	Fourth Journal	https://dl.forth.com:8443/jfar/vol3/no2/article13.pdf	Web page
3/7/1988	pdf	Forth	JCB	paper	Forth worksh	https://dl.acm.org/doi/10.1145/259965.260007	Git hub
8/1/1988	scan pdf	Laser Lab	Zuclich etal	report	DTIC	https://apps.dtic.mil/sti/citations/ADA200528	Web page
6/1/1986		uP Arch	JCB	paper	Fourth Journal	https://dl.acm.org/doi/10.5555/19899.19958	Git hub
2/1/1983	pdf	uP Arch	JCB	paper	Open Channel	https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=1654303	Web page
12/1/1982	pdf	Forth	JCB	paper	Sigarch	https://dl.acm.org/doi/10.1145/641567.641570	Web page
6/1/1982	pdf	uP Arch	JCB	paper	Sigarch	https://dl.acm.org/doi/10.1145/641542.641547	Web page
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10/1/1980	pdf	Sys Arch	JCB	paper	Sigarch	https://dl.acm.org/doi/10.1145/641914.641920	Web page
10/1/1980	pdf	uP Arch	JCB	paper	Sigarch	https://dl.acm.org/doi/10.1145/641914.641919	Web page
3/1/1979	scan pdf	Laser Lab	Zuchlich etal	report	DTIC	https://apps.dtic.mil/sti/citations/ADA068022	Web page

https://www.forth.com/forth-bool

https://dl.acm.org/profile/81100118660

Column B	Date	presentation date or publication date
Column C	Format	powerpoint, PDF, txt, scanned pdf, docx, doc, xlsx, xilinx ISE proje
Column D	Topic	one or two words
Column E	Author	JCB: James C. Brakefield, others as listed in comments
Column F	Nature	info (STEM level presentation), course, paper, patent, report
Column G	Where	Where presented, often IEEE Lonestar section at LMAG or Comp
Column H	Web Link	Web page for paper or presentation, those without an external v
Column I	location	Location of slides/paper: listed Web page, Github (github/jimbra
Column J	Title	Web page title and pptx file title may differ
Column K	Comments	
Column L	Abstract	Culled from web page announcement or source file

reports and one day courses of James Brakefield

Column header info at bottom

Title	Comments
A Digital Processor of RISC Variety Suitable for Architecture Exploration	Many slides from 2/16/2016 talk Covers TROC16; 6 attachments
A retrospective on Niklaus Wirth	Carrol Redford provided Pascal examples
Floating-Point Arithmetic and Brakefield's Patent	https://patents.google.com/patent/US5892697A/en
Progress report and Education Review and update on FPGA Boot Camp grant	Abbreviated slides, full slides at github
A $20 FPGA kit	Pictures of each component on the web page, most FPGA boards are over $100
Single day Boot camp for Digital Systems Education	Meeting set up by Carol Redfield, both 1st day & 2nd day slides
Boot camp for Digital Systems Education, 2nd week	FPGA Boot camp presentation, 2nd day slide deck
Boot camp for Digital Systems Education, 1st week	First day slides, adgenda listed
Boot camp for Digital Systems Education, 2nd week	FPGA Boot camp presentation, 2nd day slide deck
Boot camp for Digital Systems Education, 1st week	First day slides, adgenda listed
Boot camp for Digital Systems Education 2nd Saturday	Second day slides, adgenda listed
Boot camp for Digital Systems Education, 1st week	First day slides, adgenda listed
Boot camp for Digital Systems Education 2nd Saturday	Second day slides, adgenda listed
Boot camp for Digital Systems Education, 1st week	First day slides, adgenda listed
Economies of Scale for FPGA Education	AKA Low Cost PPGA Boards
64-bit embedded computing is here and now	embedded journal blog entry
Small Chips and their Usages	Passed around microscope & card with chips glued on
Legacy Updates for Avionics	Work at BAE, neat pictures
Review of the MiSTer Gamming Console	Raffled Altera card

Introduction to Posit™ Arithmetic	Figures and some slides curtesy of John Gustafson
Provisioning a 64-bit computer with 2^64 bytes of virtual memory	Used grain of rice on checker-board story
FPGA Chips: Introduction, History, and Applications	PoK-e-Jo's Smokehouse
Soft-Core CPUs An inventory of ~600 designs	https://github.com/jimbrake/cpu_soft_cores
Microprocessor Tools and Kits Suitable for Education	exhibited Raspberry Pi zero and Arduino vehicle
FPGA chips: Intro, History and Applications	
Register Oriented Instruction Sets.	rois24_24min.zip /jimbrake/ISA-Exploratorium/tree/ROIS24_24
DIY soft-core uP Microprocessor design using an FPGA	La Grande Tour attachment, replaced
Le Grande Tour of FPGA Land	posted 2022 slide deck version
An inventory of soft processor cores. Processor project at www.opencores.org	https://github.com/jimbrake/cpu_soft_cores
Logic Emulation Machine Processor project at www.opencores.org & github.com/jimbrake/lem1_9min	Four new variants of LEM1_9 are now implemented:
US Patent 5,892,687: Method and Apparatus for Handling Overflow and Underflow in Processing Floating-Point Numbers.	filed 12/19/1995, currently cited by 71 other patentss
An alternate Forth dictionary structure	
Challenges for Forth	never submitted for publication, mystery as to how got published
Research on the ocular effects of laser radiation: executive summary, SAM-TP-88-8, Sep 88.	Zuclich, J.A., R.D. Glickman, D.C. Varner, W.D. Kosnik, J.C. Brakefield
Signal space, address space, & symbol space	philosphical, one of my best "triples"
Address space unification	Virtual communications, Extensible machine language, The programmer's algebra
Talk on interpreters	Forth generalizations, has the "C as bastard Pascal" comment
Just what is an op-code?: or a universal computer design	references to five of my papers
From the other side of the Alantic: how to improve upon the MU5 design	includes my address descriptors

The peripheral bus	strobed data bus
Is 32 bits of address too much?	my address descriptor idea
Research on the ocular effects of laser radiation	Zuclich, J.A., G.A. Greiss, J.M. Harrison, and J.C. Brakefield

Archive: Journal of Forth Application and Research (JFAR)	volumes 1, 2 & 3; from Forth Inc.
Brakefield's ACM publications, citations and downloads	Many of the ACM papers were first given as DECUS talks

ect

uter chapter
web link are on my github pages
ke), opencores.org, other

Abstract
RISC computer architecture of my design an effort to achieve high code density, deterministic execution and a uniform base for diversity
Niklaus Wirth's legacy includes several programming languages, computer workstations and FPGA courseware. Simplicity was his hallmark
balanced talk on computer floating-point arithmetic and his often cited patent 4 attachments
A look at more advanced FPGA education: boards, tools and research
One of the goals of the FPGA Boot Camp grant was a lowest cost FPGA kit. Using a $14 FPGA board from China it is possible. Gowin tools still early however Tang boards are getting noticed
Conducted over one Saturday at St. Mary's University
Conducted over two Saturdays at St. Mary's University
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idea is to do for FPGAs what Raspberry Pi and Arduino have done for microprocessor education
Talk will cover what’s available in “tiny” integrated circuits and other related components: in many cases smaller than a cubic millimeter.
Work on RIU, FLR-9 and IPo1553, all used FPGAs
MiSTer is an open project that aims to recreate various classic computers, game consoles and arcade machines, using modern hardware.

New floating-point format originated by John Gustafson. Posits take, in many cases, half the memory space as IEEE-754
A light hearted look at processor generations over the years.
30 years of FPGAs & are now into their 3rd generation. A way to study them & their applications is the timeline & their expanding capabilities.
One of the most exciting parts of learning VHDL or Verilog is creating a CPU of your own design.
variety exists in the small microprocessor kits targeted towards the “educational” market. Examples of each genre will be shown
30 years of FPGAs & are now into their 3rd generation. A way to study them & their applications is the timeline & their expanding capabilities.
architectural exploration with a goal of a high performance FPGA soft core processor
will cover FPGA resource utilization, instruction set design, data path considerations, getting to “Hello World” & completing the implementation.
a simple introduction to FPGAs, their role, their limitations and promise with some mention of hardware description languages
An Inventory of mostly open-source Soft Core Processors. Although many have FPGA stats, many do not. Very large spreadsheet
Small soft core processors that operate on a single bit (or four bits) of data at a time. Can be used for logic simulation, software interrupt handlers, low resource soft-core processing and BCD calculators.
means for converting the resulting floating-point value from the floating-point register representation to the random access memory representation
The data structures used for definitions and the word search of Forth can facilitate various utilizations of the same. My goal is completeness and efficiency.
ways for Forth to progress beyond it's 16-bit roots
evaluate the bioeffects of laser radiation in order to quantify threats, primarily losses of visual function transient or permanent
conjures up "spaces" for binary signals, computer addresses & verbal thoughts as mathematical frameworks for binary circuits, computer programs & ideas
Computers show man's tendency to isolate things that are different in nature and later, as they are better understood, to unify these differences under a more general category.
different kinds of inner interpreters for stack machines (Forth)
extensible machine langague
where the MU5 architecture leads

microprocessor pherpherial bus
memory descriptor encoding for unsigned, signed and floating-point, bit, two bit and four bit alignment, power of two sizes
ELECTRONICS AND SOFTWARE FOR THE VISUAL STIMULUS LAB