

## The Peripheral Bus

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The following bus was originally considered for microcomputer to peripheral transfers of data, but can be adapted for microcomputer-to-microcomputer messages.

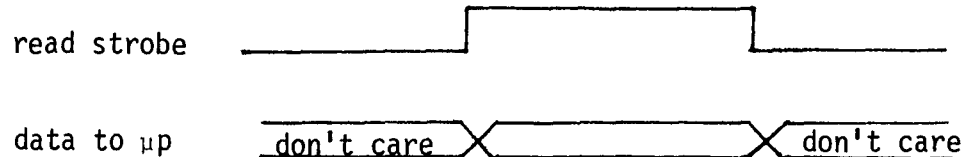
The bus is basically a strobed data bus. Its implementation can take several forms. The strongest being differential transmission. In this form a maximum of 12 differential drivers and receivers are required at a given station. Current IC implementation will take 6 IC's. In single ended form, single IC (24-28 pin) implementation is possible.

All the bus signals are tri-stated in order to keep power consumption as low as possible. This makes for a more restrictive protocol than an open collector bus. However, it is felt that the advantages of tri-state are sufficient and that the loss is minimal.

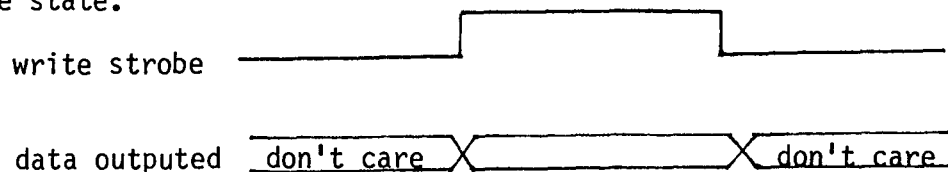
There are nominally 8 data lines, this being the right number for parallel interface to microprocessors and being a number that does not require many IC's for registers and buffers. (Octal buffers and registers being available).

There are two strobes. This again is the minimal useful number. In a typical protocol, one would be a read strobe and the other a write. If both are strobed at the same time it is considered a select operation. Six of the 8 data lines are then considered the device no. and the other 2 the function code.

In greater detail:

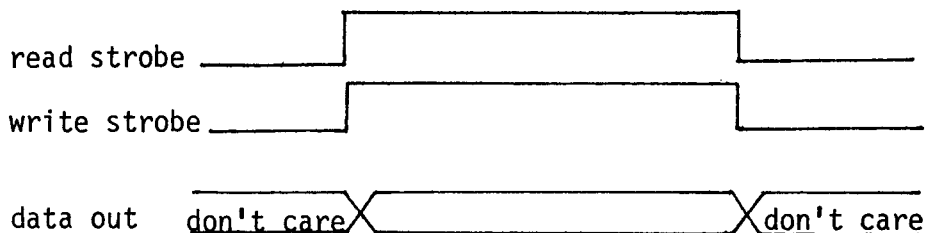


The microprocessor or other receiving device outputs the read strobe. In response the sending device (previously selected) outputs data. On the trailing edge of the read strobe, the receiving device clocks in the data and the sending device returns its outputs to the high impedance state.



The outputting device transmits the write strobe and the data. The receiving device clocks in the data at the trailing edge of the write strobe. The sending device returns the output transmitters to the high impedance state after the trailing edge of the write strobe.

It is preferable to use latches and flip-flops with zero hold time as the strobes can be used to enable and disable the data output transmitters.

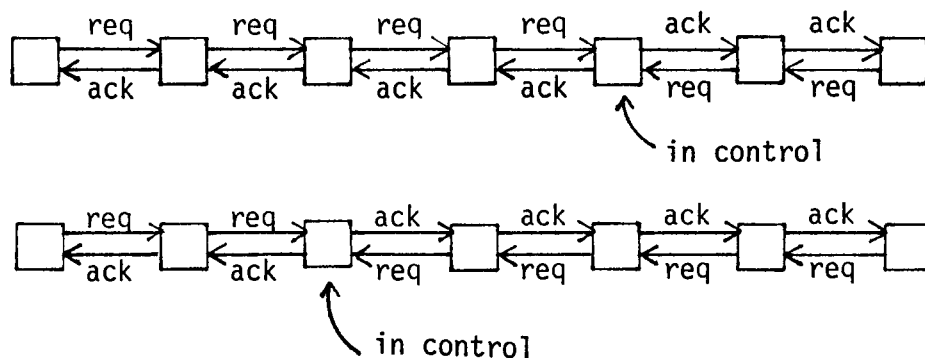


If both strobes are simultaneously used it is considered a select operation. All devices on the bus examine the data lines. If the 6 bit device no. on the data lines matches a given device no., that device becomes selected (i.e., will respond to individual read and write strobes). All other devices become de-selected. To ensure proper operations, both strobes should start at the same time, in this way there will be no confusion as to what is happening.

A 6 bit device no. should normally be adequate and is a convenient size from implementation consideration point of view. The remaining 2 bits can be used to signal four different modes of operation (or different signaling protocols).

If there was only one controlling device on the bus, these 10 signal lines would be sufficient. However, to be completely general, to allow more than one controlling device, a means should be provided to transfer control from device to device. This will also provide the means of initiating and acknowledging interrupts.

Two lines are used for control purposes. One is a request line and the other, the acknowledge line. These lines are not bussed, but are serially connected from device to device. Most importantly, which line is request and which is acknowledge varies dynamically depending on which device is in control. When control switches from one device to another, all devices in between reverse the lines used for request and acknowledge.



Those devices which never seek control, do not need drivers for the request and acknowledge lines. In these cases, the lines bypass the devices. Similarly, those devices which never generate strobes do not need strobe drivers.

Thus, the hardware for a device which neither seeks control nor generates strobes can be very straightforward. Bus drivers and receivers are required for the data lines and receivers are required for the strobes. Combinatorial logic can generate clock and control signals from the strobes. A six bit bus comparator is used to detect the select operation (DN8131, DN8136, DN8160).