<https://opencores.org/projects/rois>

Register Oriented Instruction Sets

The project is microprocessor (uP) architectural exploration with a goal of a high performance FPGA soft core processor(s) over a range of word sizes and instruction encodings. Basic resources are a register file, a block RAM and a "load/store" architecture. Most instructions have 6-bit op-code and three 6-bit source & destination register addresses. Some instructions use 6/12/18 bit immediate fields with corresponding reduction in number of register addresses.  
  
The rois24\_24min.zip download has a Xilinx ISE project for the Avnet Spartan-6 FPGA LX9 Micro-Board. It has a full set of basic instructions with a test bench exercising each instruction and condition code. Blinking LEDs code runs on the micro-board. Test bench runs correctly in simulation. This processor uses a 24-bit instruction, 24-bit data and has word addressing.  
  
Performance:  
Processor Device LUT count Fmax (in MHz)  
ROIS24\_24min Kintex-7-3 384 170  
  
Implementation:  
LUT RAM for the register file. Block RAM for program and data.  
Single clock pipe: Read next instruction, decode, read operands from LUT RAM, do operation, write result & fetch next instruction on next clock.  
  
Previously:  
The rois24\_24up\_s6\_noram.zip download has a Xilinx ISE project for the Avnet Spartan-6 FPGA LX9 Micro-Board. It is a very minimal processor with four instructions: add immediate, add immediate with carry, output and branch. This is sufficient to create blinking LEDs on the Micro-Board via a 48-bit binary counter.