Abstract and Bio for a IEEE Talk on 2/24/2025

James Brakefield

**A Digital Processor of RISC Variety Suitable for Architecture Exploration**

**Abstract:**

It is computer architecture of my design, of the RISC variety. It is an effort to achieve high code density, deterministic execution and a uniform base for diversity.

The 16-bit instructions are now running on a FPGA board, with specifications for the 24 & 32-bit instructions written. The basic template is written and it is straightforward to add more instructions.

That said, I would welcome help: do trade-off studies (resource utilization and performance) on each additional instruction.  Assembler, compiler and other help is very much needed.

As a sneak preview, the architecture supports four data sizes and four data types.  Those interested can do experiments on:

Different word sizes (16, 18, 24, 32, 36, 42 ...)

Different data types (unsigned, two's complement, sign & magnitude, IEEE 754, POSIT, PT-floats, 16-bit fixed point logarithms ...)

Different implementations (single cycle, pipelining, multiple issue, out-of-order … microarchitectures)

**BIO:**

Jim Brakefield became interested in computer architecture upon encountering the IBM 1620 and the CDC 1604 in his first semester of college. He went on to get degrees in Applied Math, Computer Science and Electrical Engineering. His work experience was primarily real-time embedded software and circuit board design. As a second career he pursued FPGAs and VHDL. He has one patent and has given many talks on a variety of STEM topics.