Small soft core uP Inventory

Opencore and other soft core processors

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe line	start year	last revis	secondary web link	note worthy	comments
ibm360-30	https://github.com/ibm2(		Lawrence Wilkinson	360	8	16	zu-3e	James	errors			6				##	v21.1	1.00	20.0		X		vhdl	72	ibm2030	Y	yes			24M	24M	Y	160		16		2012	2021	https://www.ljw.u	gate level clone, emulation only?	original 4Kx55 microcode, 8K RAM
1410	https://github.com/cube1		Jay Jaeger	1401	6	6x																	vhdl	700			Y		N	16K	16K	Y					2019	2022	https://www.com	superset of IBM1401, gate level vhdl,	was student at UW
1802-pico-basi	https://github.c	beta	Steve Teal	1802	8	8	**zu-3e**	James	area o	247	136	6		2	427	##	v21.1	0.33	12.0	47.6	LX		vhdl	6	pico_basic	Y	yes	N		64K	64K	Y	52		16		2016	2016	https://wiki.forth-	VHDL 1802 Core with TinyBASIC	tiny Basic in ROM, Interrupts & DMA not imple
1802-soc	https://github.c	no RTL	Scott Baker	1802	8	8																Y	vhdl				Y	yes	N	64K	64K	Y	52		16		2016			1802 CPU + UART + Timer + I/O Ports	no RTL, probably uses 1802-pico-basic
cosmac	https://github.c	beta	Eric Smith	1802	8	8	kintex-7-3	James	Brakef	244		6			270	##	14.7	0.33	1.0	365.5	X		vhdl	1	cosmac	Y	asm	N	N	64K	64K	Y	100		16		2009	2020		AKA COSMAC ELF of 1976	Fmax is for bare core, runs CamelForth
cosmac	https://github.c	beta	Eric Smith	1802	8	8	kintex-7-3	James	inferre	598		6		17	87	##	14.7	0.33	1.0	48.0	X	X	vhdl	14	elf	Y	asm	N	N	64K	64K	Y	100		16		2009	2020		uses PIXIE graphics core	modified to use block RAM
cosmacELF	https://hackaday.	stable	Winston Lowe	1802	8	8												0.33	1.0		X		scala	8	toplevel	Y	asm	N	N	64K	64K	Y	100		16			2020	https://hackaday.(	AKA COSMAC ELF of 1976	instructions on using Scala
sys_180x	https://github.com/zpeki		Zoltan Pekic	1802	8	8																Y	vhdl	65	CDP180X	Y	yes	N		64K	64K	Y	100		16			2020	https://hackaday.(	ucoded 1802 using mcc ucode compil	https://github.com/zpekic/MicroCodeCompile
verilog1802	https://github.c	errors	James Bowman	1802	8	8	kintex-7-3	James	errors			6				##	14.7	0.33	4.0				verilog	3	cdp1802	Y	yes	N	N	64K	64K	Y					2015	2017		runs CamelForth	all except RAM in one source file
mcs-4	https://opencor	alpha	Reece Pollack	4004	4	4	kintex-7-3	James	Brakef	228		6			376	##	14.7	0.16	4.0	66.0	X		verilog	7	i4004			N		4K	4K	N					2012	2012		4004 was multi-chip	4004 CPU & MCS-4
af65k	https://github.c	alpha	Andre Fachat	6502	32	8	kintex-7-3	James	Brakef	4424		6			69	##	14.7	1.00	4.0	3.9	X		vhdl	13	gecko65k	Y		N	N								2011	2019	http://www.6502	extended 6502 AKA 65K with 16, 32 or 64 bit data	
af65k	https://github.c	alpha	Andre Fachat	6502	32	8	**zu-3e**	James	vivado	4424		6			69	##	v21.1	1.00	4.0	3.9	X		vhdl	13	gecko65k	Y		N	N								2011	2019	http://www.6502	extended 6502 AKA 65K with 16, 32 or 64 bit data	
ag_6502	https://opencor	beta	Oleg Odintsov	6502	8	8	kintex-7-3	James	Brakef	824		6			176	##	14.7	0.33	4.0	17.7	ILX		verilog	2	ag_6502		yes	N	N	64K	64K	Y					2012	2012		verilog code generation, "phase level accurate"	
ag_6502	https://opencor	beta	Oleg Odintsov	6502	8	8	**zu-3e**	James	vivado	824		6			176	##	v21.1	0.33	4.0	17.7	ILX		verilog	2	ag_6502		yes	N	N	64K	64K	Y					2012	2012		verilog code generation, "phase level accurate"	
apple2fpga	http://www.cs.c	stable	Stephen A Edwards	6502	8	8	**zu-3e**	James	vivado	1238	706	6		7	195	##	v21.1	0.33	4.0	13.0	IX	Y	vhdl	19	de2_top	Y	yes	N	Y	64K	64K	Y					2007	2022		emulation of Apple II computer	replaced Altera PLL with stub
apple2fpga	http://www.cs.c	stable	Stephen A Edwards	6502	8	8	kintex-7-3	James	uncon	1417		6		9	159	##	14.7	0.33	4.0	9.2	IX	Y	vhdl	19	de2_top	Y	yes	N	Y	64K	64K	Y					2007	2022		emulation of Apple II computer	replaced Altera PLL with stub
bc6502	http://finitron.c	beta	Robert Finch	6502	8	8	kintex-7-3	James	Brakef	619		6			197	##	14.7	0.33	4.0	26.2	X		verilog	18	bc6502		yes	N	N	64K	64K	Y					2012	2012			bare source
bc6502	http://finitron.c	beta	Robert Finch	6502	8	8	**zu-3e**	James	vivado	583		6			286	##	v21.1	0.33	4.0	40.4	X		verilog	18	bc6502		yes	N	N	64K	64K	Y					2012	2012			bare source
cpu6502_true	https://opencor	stable	Jens Gutschmidt	6502	8	8	kintex-7-3	James	Brakef	1678		6			159	##	14.7	0.33	4.0	7.8	X		vhdl	7	r6502_tc		yes	N	N	64K	64K	Y					2008	2018		cycle accurate	
cpu65c02_true	https://opencor	stable	Jens Gutschmidt	6502	8	8	spartan-6	James	latch v	4794		6			47	##	14.7	0.33	4.0	0.8	X		vhdl	8	core		yes	N	N	64K	64K	Y					2008	2021		cycle accurate	
electronfpga	https://github.c	mature	David Banks	6502	8	8															IX	Y	vhdl				Y	yes	N	N	64K	64K	Y					2014	2020	https://en.wikiped	Acorn Electron ULA in various FPGAs	uses T65 core
fpga-64	http://www.syn	stable	Peter Wendrich	6502	8	8	kintex-7-3	James	Brakef	2210		6		2	156	##	14.7	0.33	4.0	5.8	X	Y	vhdl	26	fpga64_co	Y	yes	N	N	64K	64K	Y			26		2005	2008		Rendition of Commodore 64	altera top level schematic
fpga-bbc	https://github.c	untested	Mike Stirling	6502	8	8																	vhdl						N	65K	65K						2011	2016	https://www.mike	BBC micro, uses t65 uP	also ZX-spectrum retro project
free6502	http://web.arch	stable	David Kessner	6502	8	8	kintex-7-3	James	Brakef	646		6			193	##	14.7	0.33	4.0	24.6	X		vhdl	5	free6502	Y	yes	N	N	64K	64K	Y					1999	2000	http://www.sprow	microcoded	
ladybug	https://github.c	untested	Arlet Ottens	6502	8	8																	verilog					yes	N	N	64K	64K	Y						2016	http://ladybug.xs4all.nl/arlet/fpga/6502/		
lattice6502	https://opencor	beta	Ian Chapman	6502	8	8	kintex-7-3	James	Brakef	4942		6			214	##	14.7	0.33	4.0	3.6	X		vhdl	3	ghdl_proc	Y	yes	N	N	64K	64K	Y					2010	2010		targeted to LCMXO2280	
m65	www.ip-arch.jp/	stable	Naohiko Shimizu	6502	8	8	arria-2	James	Brakef	483		A			110	##	q13.1	0.33	4.0	18.8	X		sfl & TDI	8	m65cpu	Y	yes	N	N	4K	4K	Y					2001	2002			
m65c02	https://opencor	mature	Michael Morris	6502	8	8	spartan-6	James	Brakef	466		6		3	118	##	14.7	0.33	4.0	20.8	X	Y	verilog	13	M65C02	Y	yes	N	N	64K	64K	Y					2013	2020	https://github.com	also a m65c02a version	micro-coded via F9408 soft sequencer
m65c02a	https://github.com/Morri		Michael Morris	6502	8	8	**zu-3e**	James	portmap	mismatch		6				##	v21.1	0.33	4.0				verilog	61	M65C02A	Y	yes	N	N	64K	64K	Y						2021		enhanced 8/16-bit version of 65c02	PDFs on his figForth for M65C02A
mcl65	http://www.mic	stable	Ted Fried	6502	8	8	atrix-7-3	Ted Fried		252		6		2	196	##	14.7	0.33	4.0	64.2	X		verilog	1	mcl65	Y	yes	N	N	64K	64K	Y					2017	2021	https://github.com	**microcoded, cycle exact**	**excellent micro-coding LUT counts**
mcl65	http://www.mic	stable	Ted Fried	6502	8	8	kintex-7-3	James	inserte	326		6		2	196	##	14.7	0.33	4.0	49.6	X		verilog	1	mcl65	Y	yes	N	N	64K	64K	Y					2017	2021		**microcoded, cycle exact**	**excellent micro-coding LUT counts**
mega65	https://github.c	untested	Paul Gardner-Stephen	6502	8	8	kintex-7-3	James	bash script			6				##	14.7	0.33	2.0		X	Y	vhdl	114	machine	Y	yes	N	N	64K	64K	Y					2017	2022		Enhanced c65 running in FPGA	seeks high performance
mega65	https://github.c	untested	Paul Gardner-Stephen	6502	8	8		James	missing file			6				##	v20.1	0.33	2.0		X	Y	vhdl	114	nocpu	Y	yes	N	N	64K	64K	Y					2017	2022		Enhanced c65 running in FPGA	seeks high performance
minicpu_morri	https://github.com/Morri		Michael Morris	6502	8	8	spartan-6	Michael Morr		276		6			104			0.33	2.0	62.2	X		verilog	15	minicpu_c	Y		N		64K	64K	Y	31					2017		simplified 6502, see m65c02a	RE: 8-bit CPU challenge of Arlet Ottens
mx65	https://github.com/Steve-		Steve Teal	6502	8	8	**zu-3e**	James	Brakef	485	148	6		2	370	##	v21.2	0.33	4.0	63.0			vhdl	5	apple1	Y	yes	N		64K	64K	Y					2022	2022		cycle accurate, passes Klaus Dormann 6502 functional tests, has uart	
pet_fpga	https://github.c	stable	Thomas Skibo	6502	8	8	kintex-7-3	James	Brakef	1052		6			242	##	14.7	0.33	4.0	19.0	X		verilog	1	cpu6502	Y	yes	N	N	64K	64K	Y					2007	2011	https://github.com	for Commodore PET	
t65	https://opencor	stable	Daniel Wallner	6502	8	8	kintex-7-3	James	Brakef	575		6			291	##	14.7	0.33	4.0	41.7	IX		vhdl	7	T65	Y	yes	N	N	64K	64K	Y					2002	2010		6502, 65C02 & 65C816; wide use	
t6507lp	https://opencor	beta	Gabriel Oshiro, Samue	6502	8	8	spartan-6	James	errors								14.7		4.0				verilog	22	t6507lp	Y	yes	N	N	64K	64K	Y					2009	2010		for use in ATARI 2600	
v6502	https://github.c	untested	Daniel Loffgren	6502	8	8	**zu-3e**	James	bare c	868	131	6			250	##	v21.1	0.33	3.0	31.7	X		vhdl	23	v6502	Y	yes	N	N	64K	64K	Y					2019	2020	https://opencores	6502 with extras: 16-bit stack pointer	www.youtube.com/watch?v=K3jH-f_r80E
verilog-6502	https://github.c	stable	Arlet Ottens	6502	8	8	kintex-7-3	James	Brakef	407		6			200	##	14.7	0.33	4.0	40.6	X		verilog	2	cpu		yes	N	N	64K	64K	Y					2007	2018	http://ladybug.xs4all.nl/arlet/fpga/6502/		
verilog-6502	https://github.c	stable	Arlet Ottens	6502	8	8	**zu-3e**	James	vivado	475	112	6			333	##	v21.1	0.33	3.0	77.2	X		verilog	2	cpu		yes	N	N	64K	64K	Y					2007	2018	http://ladybug.xs4all.nl/arlet/fpga/6502/		
verilog-65C02	https://github.c	alpha	Arlet Ottens	6502	16	8	kintex-7-3	James	remov	599		6		2	204	##	14.7	0.67	4.0	57.1			verilog	5	gop16		yes	N	N	4G	4G						2011	2018	http://forum.6502	16-bit data RAM "bytes"	boot ROM mapped to LUTs?
verilog-65C02	https://github.c	alpha	Arlet Ottens	6502	16	8	**zu-3e**	James	vivado	327	98	6			370	##	v21.1	0.33	3.0	124.6	X		verilog	26	cpu		yes	N	N	64K	64K	Y					2011	2021	https://github.com	used in 100MHZ 6502 DIP module	rewritten for 6LUTs, spartan6 version has blac
hd63701	https://opencor	planning	Tsuyoshi Hasegawa	6801	8	8	spartan-6	James	Brakef	1412		6	1	3	31	##	14.7	0.33	4.0	1.8	X		verilog	6	HD63701_CORE					64K	64K	Y					2014			Used in Atari game console, 6801 clone?	
system01	http://members	beta	John Kent, David Burn	6801	8	8	kintex-7-3	James	Brakefield			6					14.7	0.33	4.0				vhdl				Y	yes	N	64K	64K	Y					2003	2009			
system68	https://opencor	stable	John Kent, David Burn	6801	8	8	spartan-3	James	Brakef	2235		4		4	46	##	14.7	0.33	4.0	1.7	X	Y	vhdl	21	cpu68	Y	yes	N	N	64K	64K	Y					2003	2009	http://members.op	tushome.com.au/jekent/	
system6801	https://opencor	stable	Michael L. Hasenfratz	6801	8	8	cyclone-3	James	Brakef	1507		4		3	73	##	14.7	0.33	4.0	4.0	I		vhdl	15	wb_cyclon	Y	yes	N	N	64K	64K	Y					2003	2009	http://members.o	based on John Kent's 6801	tested on Apex20K, Cyclone & Straix boards
mc6803	https://opencor	stable	Dukov	6803	8	8												0.33	3.0				system verilog				Y	yes	N	64K	64K	Y					1999			based on System68 and System01 by John E. Kent, translated CPU core from VHDL to	
68hc05	https://opencor	stable	Ulrich Riedel	6805	8	8	**zu-3e**	James	vivado	1106	117	6			485	##	v21.1	0.33	4.0	36.2	X		vhdl	1	6805		yes	N	N	64K	64K	Y					2007	2009			68c05 & 68c08 very different Fmax
68hc05	https://opencor	stable	Ulrich Riedel	6805	8	8	kintex-7-3	James	Brakef	1112		6			300	##	14.7	0.33	4.0	22.2	X		vhdl	1	6805		yes	N	N	64K	64K	Y					2007	2009			
df6805	www.hitechglob	proprietar	Hitech Global	6805	8	8	stratix-1	Hitech Global		1690		4			83			0.33	4.0	4.1	I		proprietary				Y	yes	N	N	64K	64K	Y							6805 data sheets		
system05	https://opencor	beta	John Kent, David Burn	6805	8	8	kintex-7-3	James	Brakef	834		6			204	##	14.7	0.33	4.0	20.2	X	Y	vhdl	10	System05	Y	yes	N	N	64K	64K	Y					2003	2009	http://members.op	tushome.com.au/jekent/	
68hc08	https://opencor	stable	Ulrich Riedel	6808	8	8	**zu-3e**	James	vivado	1875	128	6			164	##	v21.1	0.33	4.0	7.2	X		vhdl	1	x68ur08		yes	N	N	64K	64K	Y					2007	2009			68c05 & 68c08 very different Fmax
68hc08	https://opencor	stable	Ulrich Riedel	6808	8	8	kintex-7-3	James	Brakef	2290		6			101	##	14.7	0.33	4.0	3.6	X		vhdl	1	x68ur08		yes	N	N	64K	64K	Y					2007	2009			
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	6809	8	8	**zu-3e**	James	vivado	1690	367	6			333	##	v21.1	0.33	3.0	21.7	AILX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y					2012	2015		6309 op-codes not implemented	does not match timing results of zynq+
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	6809	8	8	stratix-5	James	Brakef	1711		A			223	##	q14.0	0.33	3.0	14.3	AILX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y	44	13	8		2012	2015		6309 op-codes not implemented	
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	6809	8	8	kintex-7-3	James	Brakef	1996	370	6			175	##	14.7	0.33	3.0	9.7	AILX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y	44	13	8		2012	2015		6309 op-codes not implemented	
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	6809	8	8	arria-2	James	Brakef	1680		A			145	##	q18.0	0.33	3.0	9.5	AILX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y	44	13	8		2012	2015		6309 op-codes not implemented	
coco3fpga	https://github.c	mature	Gary Becker	6809	8	8																	verilog	39			Y	yes	N		64K	64K		44	13	8		2007	2015	http://www.davet	uses John Kent's 6809 & adds color computer SOC	
mc6809	https://github.c	stable	Greg Miller	6809	8	8																	vhdl	6	gd6809	Y	yes	N	N	64K	64K	Y	44	13	8		2016	2017	https://shop.trenz	Cycle Accurate MC6809 Core	emphasis on cycle accuracy, DIP replacement
mc6809e		beta	Flint Weller	6809	8	8	kintex-7-3	James	gate level primitives en			6					14.7	0.33	3.0				vhdl	26	core_6809	Y	yes	N	N	64K	64K	Y	44	13	8		1999		https://www.linke	course work, ASIC orientation	
rf6809	https://opencores.org/pr		Robert Finch	6809	8	8	artix-7	Robert Finch		4200		6		4	120	##	v21.2	0.33	4.0	2.4	X	Y	system v	21	rf6809	Y	yes	N		16M	16M	Y	44	13	8		2022	2022	http://www.finitr	Different from rtf6809: 24-bit adrs, op	8-bit version, has inst. Cache
rf6809	https://opencores.org/pr		Robert Finch	6809	12	12	artix-7	Robert Finch		6500		6		5	120	##	v21.2	0.50	4.0	2.3	X	Y	system v	21	rf6809	Y	asm	N		64G	64G	Y	44	13	8		2022	2022	http://www.finitr	Different from rtf6809: 36-bit adrs, op	12-bit version, has inst. Cache
rf6809	https://opencores.org/pr		Robert Finch	6809	12	12	artix-7	James Brakefield				6		5		##	v21.2	0.50	4.0		X	Y	system v	21	rf6809	Y	asm	N		64G	64G	Y	44	13	8		2022	2022	http://www.finitr	Different from rtf6809: 36-bit adrs, op	12-bit version, has inst. Cache
rtf6809	https://github.c	alpha	Robert Finch	6809	8	8	kintex-7-3	James	many	7506		6	1	2	106	##	14.7	0.33	4.0	1.2	X		verilog	4	rtf6809	Y	yes	N	N	4G	4G	Y	44	13	8		2012	2015	http://www.finitr	6809 with 32-bit "FAR" addressing	see also rtf6809 variant
system09	https://opencor	stable	John Kent, David Burn	6809	8	8	kintex-7-3	James	Brakef	1631		6		41	88	##	14.7	0.33	3.0	6.0	IX	Y	vhdl	40	cpu09l	Y	yes	N	N	64K	64K	Y	44	13	8		2003	2021	http://members.o	from John Kent web page	opencores download URL incorrect, use col E
8051	https://opencor	alpha	Simon Teran, Jakas	8051	8	8	**zu-3e**	James	area o	1424	645	6			242	##	v21.1	0.33	4.0	14.0	ILX		verilog	32	oc8051_tc	Y	yes	N		64K	64K	Y					2001	2016		8051 core includes several on-chip peripherals, like timers and counters	
8051	https://opencor	alpha	Simon Teran, Jakas	8051	8	8	kintex-7-3	James	tunred	1744		6	1		111	##	14.7	0.33	4.0	5.3	ILX		verilog	32	oc8051_tc	Y	yes	N		64K	64K	Y					2001	2016		8051 core includes several on-chip peripherals, like timers and counters	
altium/TSK51A	http://techdocs	proprietar	Altium	8051	8	8	spartan-3	Altium		1890		4		1	50			0.33	6.0	1.5	AILX		proprietary				Y	yes	N	N	64K	64K	Y					2004	2017	CR0140.pdf, CR01	frozen, asm, C, C++, schem, VHDL & V	default clock speed is 50MHz
cast_8051	http://www.cas	proprietar	CAST Inc	8051	8	8	virtex-6	CAST I	820 sli	1800		6		2	81	##	12.1	0.33	3.0	5.0	X		proprietary				Y	yes			64K	64K	Y			32				http://www.cast-i	Cast has uP related IP	several versions, FPGA kits
dalton_8051	www.cs.ucr.edu	stable	Tony Givargis	8051	8	8	kintex-7-3	James	Brakef	2725		6	1	1	105	##	14.7	0.33	1.0	12.7	X		vhdl	7	i8051_all	Y	yes	N	N	64K	64K	Y					1999	2003		ASIC	
dp8051	https://www.do	proprietar	Digital Core Design	8051	8	8	virtex-5	Digital Core D		1699		6			200	##	14.7	0.30	1.0	35.3	ILX		proprietary				Y	yes	N		64K	64K						1999	1999		also PIC, HC11, 68000, 680x, d32pro	full system with RAM
i8051		stable	Tony Givargis	8051	8	8	kintex-7-3	James	Brakef	2690		6	1	1	105	##	14.7	0.33	4.0	3.2	X		vhdl	9	i8051_all	Y	yes	N		64K	64K	Y					1999	1999		author has book & course	Embedded System Design: A Unified Hardware
light52	https://opencor	beta	Jose Ruiz	8051	8	8	kintex-7-3	James	Brakef	1022		6	1	1	154	##	14.7	0.33	6.0	8.3	IX	Y	vhdl	8	light52_m	Y	yes	N	N	64K	64K	Y					2012	2018		targeted to balanced	~ 6 clocks/inst
mc8051	http://www.ore	stable	Helmut Mayrhofer	8051	8	8	kintex-7-3	James	Brakef	3022		6	1		83	##	14.7	0.33	4.0	2.3	X		vhdl	49	mc8051cc	Y	yes	N	N	256	64K	Y					1999	2013	www.oreganosyst	fast 8051, version available with floating-point by David Lundgren	
mcl51	http://www.mic	stable	Ted Fried	8051	8	8	atrix-7-3	Ted Fried		312		6		2	180			0.33	8.0	23.8	X		verilog	3	mcl51_TO	Y	yes	N	N	64K	64K	Y					2016	2021	https://github.com	**micro-coded**	
oms8051mini	https://opencor	alpha	Simon Teran, Dinesh A	8051	8	8	kintex-7-3	James	Brakef	1991		6	1	32	133	##	14.7	0.33	5.0	4.4	X	Y	verilog	66	digital_co	Y	yes	N		64K	64K	Y					2000	2018			
pulserain	https://github.c	errors	PulseRain Tech LLC	8051	8	8	arria-2	James	missing files			A				##	q18.0	0.33	3.0		I		system verilo	PulseRain	Y	yes	N	Y	64K	64K	Y					2017	2018	https://www.puls	intended for Max10	
pulserain	https://github.c	stable	PulseRain Tech LLC	8051	8	8	arria-2	James	some	2376		A	2	41	130	##	q18.0	0.33	3.0	6.0	I		system v	25	FP51_fast	Y	yes	N	Y	64K	64K	Y					2017	2018	https://www.puls	1 clk/inst, intended for Max10	

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe line	start year	last revis	secondary web link	note worthy	comments
r8051	https://github.c	stable	Li Xinbing	8051	8	8	kintex-7-3	James Brakef		1031		6	1		139	##	14.7	0.33	4.0	11.1	X		verilog	2	r8051	Y	yes	N	N	64K	64K	Y					2015	2019			
t51	https://opencor	stable	Andreas Voggeneder	8051	8	8	kintex-7-3	James Brakef		1942		6	1		147	##	14.7	0.33	4.0	6.2	IX		vhdl	17	T8032	Y	yes	N	N	64K	64K	Y					2002	2010		8052 & 8032	8032 SoC
turbo8051	https://opencor	beta	Dinesh Annayya	8051	8	8	kintex-7-3	James Brakef		1985		6	1		127	##	14.7	0.33	4.0	5.3	IX		verilog	74	oc8051_tc	Y	yes	N	N	64K	64K	Y					2011	2016		includes perpherials	
am9080	https://opencor	beta	Moshe Shavit	8080	8	8	kintex-7-3	James	hung in synthesis			6				##	14.7	0.33	9.0		X		vhdl	31	cpu	Y	yes	N	N	64K	64K	Y					2917	2018	https://en.wikichi	emulation of AM9080 using bit-slice 8	has VHDL for AMD bit-slice chips
am9080	https://opencor	beta	Moshe Shavit	8080	8	8	kintex-7-3	James	hung in synthesis			6				##	14.7	0.33	9.0		X	Y	vhdl	31	sys9080	Y	yes	N	N	64K	64K	Y					2917	2018	https://en.wikichi	emulation of AM9080 using bit-slice 8	has VHDL for AMD bit-slice chips
cpu8080	https://opencor	stable	Scott Moore	8080	8	8	kintex-7-3	James Brakef		1179		6			299	##	14.7	0.33	9.0	9.3	X		verilog	1	m8080	Y	yes	N	N	64K	64K	Y					2006	2016		includes VGA display generator, three	variants
ep8080	https://github.c	beta	C.H. Ting	8080	8	8	kintex-7-3	James Brakef		1276		6			184	##	14.7	0.33	9.0	5.3	X		vhdl	4	ep80.vhd	Y	yes	N	N	64K	64K	Y					2002	2016	8080 data sheets	initialized Lattice memory blocks	work related to eP16
light8080	https://opencor	stable	Jose Ruiz, Moti Litoche	8080	8	8	kintex-7-3	James Brakef		154		6		1	247		14.7	0.33	9.0	58.9	IX		verilog	5	i80soc	Y	yes	N	N	64K	64K	Y					2007	2019	https://github.cor	targeted to area, includes UART, inter	older versions have both VHDL & Verilog
pmd85	https://github.com/PetrM		PetrM1	8080	8	8																Y	system v	28	sys_top	Y	yes	N		64K	64K	Y						2021	https://www.yout	Czechoslovakian PC using Intel 8080	clone, for use in MISTer
sys9080	https://github.c	stable	Zoltan Pekic	8080	8	8																	vhdl	15	sys9080	Y	yes	N	N	64K	64K	Y					2017	2018	https://opencores	8-bit 8080 CPU based on 29XX bit-slice	series of devices AMD 1978 51 pge ap note
vm80a	https://github.c	untested	1801BM1	8080	8	8	cyclone-3			607		4			104								verilog													2014	2018		Two versions of Soviet i8080a reverse	engineered from silicon die, 607 4LUTs, 104M
gl85	http://simlab.ec	stable	Alex Miczo	8085	8	8	kintex-7-3	James	gate level design			6					14.7	0.33	4.0		X		vhdl	1	i8085	Y	yes	N	N	64K	64K	Y					1993		http://www.fpga.a	also a TTL implementation in VHDL	
my8085light	https://github.com/debta		Debtanu Mukherjee	8085	8	8																	verilog	7	my8085	Y		N		64K	64K	Y	18		8			2020	https://opencores	light weight 8085 with 18 inst	
ssppu	https://github.com/redos		redoste	8085	8	16															X	Y	vhdl	20	board		asm	N		64K	64K	Y	5					2022	https://archive.or	SAP-1 (Simple-As-Possible) architectu	small subset of 8085
ep994a	https://github.c	stable	Erik Piehl	9900	16	16	kintex-7-3	James Brakef		1340		6		5	286	##	14.7	0.83	3.0	59.0	X		vhdl	10	ep994a	Y	yes	N	N	64K	64K	Y			16		2016	2019	https://hackaday.i	TI 990 emulation	also tms9902 (uart) core by Paul Urbanus?
ep994a/icy99	https://github.c	stable	Erik Piehl	9900	16	16												0.83	3.0		L		verilog	29	tms9900	Y	yes	N	N	64K	64K	Y			16		2016	2020	https://hackaday.i	TI 990 emulation	also tms9902 (uart) core by Paul Urbanus?
ao68000	https://opencor	beta	Aleksander Osman	68000	16	16	arria-2	James Brakef		3479		A		6	169	##	q13.1	0.67	4.0	8.1	I	Y	verilog	1	ao68000	bm	yes	N		4G	4G	Y					2010	2012		uses microcode, instruction prefetch	buffer
aoocs	https://github.c	beta	Aleksander Osman	68000	16	16	cyclone-2	Aleksander O		26227		4	2	65		##	q10.1	0.67	4.0		I	Y	verilog	22	aoOCS	bm	yes	N		4G	4G	Y					2010	2011		uses ao68000 core, Amiga chip set en	Wishbone Amiga OCS SoC
aoocs	https://github.c	beta	Aleksander Osman	68000	16	16	kintex-7-3	James	altera pimitives			6				##	14.7	1.00	1.0		I	Y	verilog	22	aoOCS	bm	yes	N		4G	4G	Y					2010	2011		uses ao68000 core, Amiga chip set en	Wishbone Amiga OCS SoC
aoocs	https://github.c	beta	Aleksander Osman	68000	16	16	arria-2	James Brakef		17852		A	2	43	57	##	q18.0	0.67	4.0	0.5	I	Y	verilog	22	aoOCS	bm	yes	N		4G	4G	Y					2010	2011		uses ao68000 core, Amiga chip set en	Wishbone Amiga OCS SoC
aoocs	https://github.c	beta	Aleksander Osman	68000	16	16	cyclone-1	James Brakef		26009		4	2	67	45	##	q18.0	0.67	4.0	0.3	I	Y	verilog	22	aoOCS	bm	yes	N		4G	4G	Y					2010	2011		uses ao68000 core, Amiga chip set en	Wishbone Amiga OCS SoC
apollo_68080	http://www.apc	proprieta	Gunnar von Boehn	68000	8	16	cyclone-V	Gunnar von Boehn															vhdl			Y	yes	N		4G	4G	Y			32		2012	2022	http://www.apoll	sells Amiga card, "68080" with 64-bit	claims very fast FPGA versions
fx68k	http://fx68k.fxa	untested	Jorge Cwik	68000	16	16																	system v	3	fx68k	Y	yes	N	N	4G	4G	Y			16		2018	2021	https://github.cor	Cycle accurate, see http://atari-forum.com/viewtopic.php?f=28&t=34730#p358139	
J68	https://github.com/fredre		Frédéric Requin	68000	16	16	cyclone3	Frédéric Requ		1900		4		9	90			1.00	6.0	7.9			verilog	38	soc_j68		yes	N	N	64K	64K	Y			16			2018		A Size-Optimized Microcoded 68000 (	Stack based CPU with Forth-like microcode	
j68	https://code.go	stable	Frederic Requin	68000	32	16	stratix-2	Freder	speed	1900		4		4	180			1.00	6.0	15.8	I		verilog	1	j68	Y	yes	N		4G	4G	Y			16		2009	2014		for use with Minimig	micro-coded on stack machine
k68	https://opencor	alpha	Shawn Tan	68000	16	16	kintex-7-3	James Brakef		2392		6			24	##	14.7	0.67	4.0	1.7	X		verilog	15	k68_cpu	Y	yes	N	N	4K	4G	Y			16		2003	2009		68K binary compatible	
m68k	https://github.com/usoki		Salvador Garcia	68000	32	16																	vhdl	13	cpu3017												2018			simplified 68K	
mc68kods	https://sites.goo	beta	Olivier De Smet	68000	32	16	kintex-7-3	James	errors	4617		6				##	14.7	1.00	8.0			Y	vhdl	10	mc68kods												2011			SOC for HP9816 computer emulation	
rf68000	https://opencor	alpha	Robert Finch	68000	32	16	zu5e	James	missing IP														system v	7	rf68000	Y	yes	N	N	4G	4G	Y			16		2008	2022		mc68000 similar core, BCD instructions	have variances
rtf68ksys	https://github.c	alpha	Robert Finch	68000	16	16	spartan-3	James	need t	13639		4	12	17		##	14.7	0.67	4.0		X	Y	verilog	49	rtf68kSys	Y	yes	N	N	4G	4G	Y			16		2011	2011	https://github.cor	based on Tobias Gubener's TG68	
suska-III	http://www.exp	beta	Wolfgang Forster	68000	16	16	arria-2	James Brakef		7388		A			55	##	q13.1	0.67	4.0	1.3	I		vhdl	11	wf68k00ip	Y	yes	N	N	4G	4G	Y			16		2003	2013		for use as an Atari ST	
terracresta	https://github.c	beta	Darren Olafson	68000	16	16															I		verilog	50			yes	N		4G	4G	Y			16		2018	2022		FPGA compatible core of Nichibutsu M	fx86k & t80 cores
tg68	https://opencor	stable	Tobias Gubener	68000	16	16	kintex-7-3	James Brakef		2331		6			44	##	14.7	0.67	4.0	3.2	X		vhdl	2	TG68_fast	Y	yes	N	N	4G	4G	Y			16		2007	2012		TG68 - execute 68000 Code	for use with Minimig
tg68kc	https://opencor	stable	Tobias Gubener	68000	16	16	kintex-7-3	James Brakefield										0.67	4.0		X		vhdl	3	TG68docC	Y	yes	N	N	4G	4G	Y			16		2013	2021		68020 ISA (68000, 68010 & 68020 choice)	
v1_coldfire	https://www.silv	proprietar	IPextreme	68000	16	16	cyclone-3	freescale		5000		4			80			0.89	1.0	14.2	I		verilog			Y	yes	N	N	4G	4G	Y			16		2008		https://www.silva	free for Altera	3500 LUTs on Stratix-III
whitham_68k	https://www.jw	errors	Jack Whitham	68000	32	16	kintex-7-3	James	no top module							##	14.7	0.67	4.0				vhdl			Y	asm			4G	4G	Y			16		2002	2003		university project, 68020 subset	read thesis, code generator for top modules
cf_ssp	https://opencor	stable	Tom Hawkins	?																			confluence			Y		N									2003	2009		confluence to VHDL	CF State Space Processor
gup	https://opencor	stable	Kevin Phillipson	68HC11	8	8	arria-2	James Brakef		925		A	1	1	127	##	q13.1	0.33	4.0	11.3	I		vhdl	25	gator_upr	Y	yes	N	N	64K	64K	Y					2008	2011	https://www.mil.u	top level is schematic	
hc11core	http://www.gm	stable	Green Mountain Comp	68HC11	8	8	kintex-7-3	James Brakef		2190		6			127	##	14.7	0.33	4.0	4.8	X		vhdl	1	hc11rtl	Y	yes	?	N	64K	64K	N	53		8	2	2000		6811 data sheets	restricted use license, with corrections	
system11	https://opencor	alpha	John Kent, David Burn	68HC11	8	8	kintex-7-3	James Brakef		1218		6			153	##	14.7	0.33	4.0	10.3	X	Y	vhdl	17	cpu11	Y	yes	N	N	64K	64K	Y					2003	2009	http://members.q	known bugs & untested instructions	
legv8	https://github.c	simulatior	Warren Seto	AA64	64	32	kintex-7-3	James Brakefield				6				##	14.7	1.00	1.0			B	verilog	2	arm_cpu	Y	yes	N		4G	4G	Y	10		32		2018	2019		coursework, limited ISA, 3 versions	single cycle, inst: LDUR, STUR, ADD, SUB, ORR,
legv8	https://github.c	stable	Warren Seto	AA64	64	32	kintex-7-3	James Brakef		731		6		2	154	##	14.7	1.00	1.0	210.5	X	B	verilog	2	arm_cpu	Y	yes	N		4G	4G	Y	10		32		2018	2019		coursework, limited ISA, 3 versions	pipelined, inst: LDUR, STUR, ADD, SUB, ORR, A
legv8	https://github.c	stable	Warren Seto	AA64	64	32	kintex-7-3	James Brakef		884		6		2	137	##	14.7	1.00	1.0	155.0	X	B	verilog	2	arm_cpu	Y	yes	N		4G	4G	Y	10		32		2018	2019		coursework, limited ISA, 3 versions	inst: LDUR, STUR, ADD, SUB, ORR, AND, CBZ, B
legv8	https://github.com/matt	stable	Matthew Olsson	AA64	64	32	kintex-7-3	James Brakef		884		6		2	137	##	14.7	1.00	1.0	155.0			verilog			Y	yes	N		4G	4G	Y	10		32		2018	2019		another implementation	legv8 from Patterson & Hennessy 2017
legv8	https://github.c	stable	Seninha phillbush	AA64	64	32																	verilog	28		Y	asm	N		4G	4G	Y	10		32		2018	2019		single cycle & pipeline versions	course project
8bit-verilog_mcu		stable	Josh Friend	accum	8	8	**zu-2e**	James	timing	392		6		1	500	##	v20.1	0.33	2.0	210.5	X		verilog	11	cpu						512	512	Y	16					2012	2012		for class project, small data stack	PB clock, students to add features
acc	https://github.c	stable	Juan Gonzalez-Gomez	accum	15	15	kintex-7-3	James	rom &	88		6		1	227	##	14.7	0.67	2.0	865.2	IX		verilog	1	acc2	Y	yes	N			4K							2016	2016	https://github.cor	26 chptr course using Apollo Comma	??why LUT count different from agcnorm
acc	https://github.c	stable	Juan Gonzalez-Gomez	accum	15	15	**zu-3e**	James	DFF ex	88		6		1		##	v21.1	0.67	2.0		IX		verilog	1	acc2	Y	yes	N			4K							2016	2016	https://github.cor	26 chptr course using Apollo Comma	??why LUT count different from agcnorm
agcnorm	https://opencor	beta	Dave Roberts	accum	15	15	spartan-3	James Brakef		3732		4		2	20	##	14.7	0.66	1.0	3.5	X		vhdl	5	AGC	Y			N	Y	4K	72K	N	11		1		1962	2012	http://klabs.org/h	Apollo Guidance Computer via 3-input	NOR gate emulation
ahmes	https://github.c	stable	Fabio Pereira	accum	8	8	kintex-7-3	James Brakef		186		6			476	##	14.7	0.33	3.0	281.6	X	B	vhdl	3	ahmes				N	N	256	256	Y	15	1			2016	2017	http://embeddedsystems.io/ahmes-a-simple-8-bit-cpu-i	bare CPU with no RAM	
asip38	https://aaltodoc.aalto.fi/b		Lauri Isola	accum	32	38															X	Y	vhdl	14	top	Y	asm	N	Y	16K	16K	N	30				2018	2021	http://www.kolur	Application-Specific Instruction set	Processor, masters thesis
ben_eater_8bi	https://github.com/hneer		Paul Kappmeyer	accum	8	8																	schemat	5															https://github.cor	Digital schematic, Ben Eater uP	
ben_eater_up	https://github.com/ajitho		Ajith Thomas	accum	8	8																	vhdl	27	test_cpu	Y	asm	N		256	16	Y	10					2020	https://eater.net/	based on Ben Eater's tutorial on building	an 8-Bit breadboard computer
ben_eater_up	https://github.com/hsnav		Humberto Silva Naves	accum	8	8																	verilog	14	computer		asm	N		256	16	Y					2015	2019	https://eater.net/	Ben Eater's 8-bit breadboard comput	microcode?
ben_eater_up	https://github.com/XarkL		Ken Jordan	accum	8	8																	vhdl	6	system	Y	asm	N		256	16	Y					2015	2019	https://eater.net/	Ben Eater's 8-bit breadboard computer	
ben_eater_up	https://github.com/JetSta		XarkLabs	accum	8	8																	vhdl	38	computer	Y	asm	N		256	16	Y					2015	2019	https://eater.net/	Ben Eater's 8-bit breadboard computer	
bit-serial	https://github.com/howe		Richard Howe	accum	16	16	**zu-3e**	James	errors init bkRAM			6				##	v21.1	0.67	51.0				vhdl	6	top	Y		N		4K	4K	N	15				2020	2021		bit serial, 16-bit uP, very simple	supports Forth
blue	https://opencor	stable	Al Williams	accum	16	16	spartan-3	James	remov	1025		4			63	##	14.7	0.67	1.0	41.1	X		verilog	16	topbox	web		N		4K	4K	N	16		2		2009	2010		derived from Caxton Foster's Blue	http://www.youtube.com/watch?v=dt4zezZP8
blue_fpga	https://github.com/Geckc		Jaime Centeno	accum	16	16															X		vhdl	47	system	Y		N		4K	4K	N	16		2		2021	2022		gate level png's, simulator exe	
c16	https://opencor	stable	Jsauermann	accum	16	8	spartan-3	James Brakef		1751		4		16	57	##	14.7	0.33	1.0	10.7	X		vhdl	22	Board_cpl	mi	yes	N		64K	64K	Y			5		2003	2012		8080 derivative, optional UART, 8-bit	xilinx 4K RAM primitives
c88	https://github.c	alpha	Daniiel Bailey	accum	8	8	kintex-7-3	James Brakef		3088		6	2		167	##	14.7	0.33	2.0	8.9	X		vhdl	25	C88	Y	asm	N		8	256	Y	10		8		2015	2015	https://www.yout	only 8 memory locations	used 3658 Dff, doesn't infer block or LUT RAM
c88	https://github.c	alpha	Daniiel Bailey	accum	8	8	spartan-3	James	Dff ge	2664		4	2		54	##	14.7	0.33	1.0	6.7	X		vhdl	25	C88	Y	asm	N		8	256	Y	10		8		2015	2015	https://www.yout	only 8 memory locations	used 3785 Dff, doesn't infer block or LUT RAM
cardiac	https://opencor	mature	Al Williams	accum	13	12	spartan-3	James Brakef		557		4			71	##	14.7	0.30	1.0	38.5	X		verilog	16	vtach	Y	asm	N		100	100	N	10				2013	2019	https://www.cs.d	CARDboard Illustrative Aid to Comput	3 digit BCD arithmetic
classic_HP_cal	https://github.c	stable	Brian Nemetz	accum	56	10	kintex-7-3	James Brakef		1750		6		3	233	##	14.7	0.17	10.0	2.2	X		vhdl	15	classichp	Y		N		30	4K	N	40		7		2012			processor & ROMs for HP-55, 45 & 35	includes LED display driver & UART, for Papilio
cpu_mcnally	https://www.so	untested	Iain McNally	accum	16	16																B	system verilog			Y		N	N	4K	4K							2011		for course, SystemVerilog HDL - Exam	possibly same as simplecpu	
eight32	https://github.com/robins		Alastair M. Robinson	accum	32	8	cyclone-4	Alasta	approx	1300		4			133			1.00	1.0	102.3			vhdl	17	eighthirty	Y	yes	N		500M	500M	Y	28		8		2019	2021	https://retroramb	5-bit op-code & 3-bit reg #	full tool set, see github page for ISA description
ez8	https://github.c	stable	Howard Mao	accum	8	16	kintex-7-3	James	replac	644		6		2	233	##	14.7	0.33	2.0	59.6	X		verilog	13	ez8_cpu					256	4K						2014	2014	http://zhehaomao.com/	not sure inferred RAM correct?	
fpga4_8bit_up	http://www.fpg	stable	Van Loi Le	accum	8	8	kintex-7-3	James Brakef		258		6		1	200	##	14.7	0.33	3.0	85.3	X		vhdl	9	computer	bme		N		96	128	Y	10		2		2016	2016	book: LaMeres Int	educational	16 input & 16 output ports fill out 256 byte adr
fpga4_up8_12	http://www.fpg	errors	Van Loi Le	accum	8	12	kintex-7-3	James	degenerate design			6				##	14.7	0.33	1.0				verilog	7	microcontroller			N									2016	2016		educational, simplified PIC12	incomplete
hack	https://github.com/jopdo		Jegor van Opdorp	accum	16	16																	system verilog			Y		N	Y	32K	32K	N			2			2021		SystemVerilog version of the course	materials on hardware design	
hack	https://github.com/theap		Peter Clarke	accum	16	16															X		verilog	22	cpu	Y		N	Y	32K	32K	N			2			2016	https://www.nand	CPU used to run Tetris	book: Elements of Computing Systems
hack	https://github.com/philzo		Philip Zucker	accum	16	16																	verilog			Y		N	Y	32K	32K	N			2			2021		educational formally verified version of	the Nand 2 Tetris course using Coq	
hack	https://github.com/wuha		Wu Han	accum	16	16		Wu Ha	not co	267		4		4							L		verilog	22	hack	Y		N	Y	32K	32K	N			2			2020	https://www.nand	CPU used to run Tetris	book: Elements of Computing Systems
hack	https://gitlab.com/x653/n		Michael Schroder	accum	16	16															I		vierilog	24	cpu	Y		N	Y	32K	32K	N			2			2016	https://www.nand	CPU used to run Tetris	book: Elements of Computing Systems
hamblen_scon	http://hamblen.	stable	James O. Hamblen	accum	16	16	cyclone-1	James	altera	80		4		1	204	##	q18.0	0.67	2.0	852.7	I		verilog	1	scomp			N	N	256	256	N	4					2008	http://hamblen.ed	from Hamblen 2008 "Rapid prototypi	tiny edu, high IO count	
hamblen_scon	http://hamblen.	stable	James O. Hamblen	accum	16	16	cyclone-1	James	altera	196		4		1	166	##	q18.0	0.67	2.0	283.5	I		verilog	2	DE2_TOP			N	N	256	256	N	4					2008	http://hamblen.ed	from Hamblen 2008 "Rapid prototypi	tiny edu, high IO count	
hrm-cpu	https://github.c	untested	Alexandre Dumont	accum	8	16																	verilog			Y		N				Y	16	2			2018	2019		modelled on "Human Resource Machine"	
inst_list_proce	https://opencor	planning	Mahesh Palve	accum	8	15	kintex-7-3	James	using x	786		6		1	340	##	14.7	0.33	1.0	142.6	X		verilog	34	top	Y		N		128	1K		32				2014			pipelined, state machine	UART, SPI & timer included
lem1_9	https://opencor	alpha	James Brakefield	accum	1	9	kintex-7-3	James	1 stage	75		6		1	171	##	14.5	0.04	1.0	91.2	IX		vhdl	2	lem1_9	Y		N	Y	32	2K	N	24			1	2016	2017		single bit at a time, absolute adrs	
lem1_9min	https://opencor	stable	James Brakefield	accum	1	9	kintex-7	James	1 stage	63		6		1	358	##	14.5	0.04	1.0	227.2	ILX		vhdl	3	lem1_9mi	Y	asm	N	Y	64	2K	N	8		64	1	2003	2009		logic emulation machine	
lem1_9ptr	https://opencor	beta	James Brakefield	accum	1	9	kintex-7-3	James	1 stage	147		6		1	176	##	14.5	0.06	1.0	72.0	IX		vhdl	2	lem1_9pti	Y		N	Y	512	2K	N	24			1	2016			use speed opt, logic emulation machi	4 index registers: (ix),(--ix),(ix++),(ix+off)

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hard'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe line	start year	last revis	secondary web link	note worthy	comments
lem16_18		alpha	James Brakefield	accum	16	18	kintex-7-3	James Brakef		483		6		1	294	##	14.5	0.16	1.0	97.4	X		vhdl	2	lem16_18m			N		256	1K		77			1	2010	2018		variable bit-length memory read/writ	op-codes coded, untested
lem4_9	https://opencor	beta	James Brakefield	accum	4	9	kintex-7-3	James	1 stage	144		6		1	195	##	14.5	0.16	1.0	216.7	IX		vhdl	2	lem1_9	Y		N	Y	32	2K	N	24			1	2016			binary & BCD digit addition, speed mode	
lem4_9ptr	https://opencor	beta	James Brakefield	accum	4	9	**zu-2e**	James	1 stage	210		6		0	397	##	v20.1	0.24	1.0	453.5	IX		vhdl	2	lem1_9ptr	Y		N	Y	512	2K	N	24			1	2016			binary & BCD digit addition, speed mo	4 index registers: (ix),(--ix),(ix++),(ix+off)
lem4_9ptr	https://opencor	beta	James Brakefield	accum	4	9	kintex-7-3	James	1 stage	151		6		1	151	##	14.5	0.24	1.0	240.0	IX		vhdl	2	lem1_9ptr	Y		N	Y	512	2K	N	24			1	2016			binary & BCD digit addition, speed mo	4 index registers: (ix),(--ix),(ix++),(ix+off)
leros	https://opencor	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin	Schoe	112		6		1	182			0.67	1.0	#####	IX		vhdl	5	leros	Y	yes	N	Y	256	64K				2	2	2008	2020	https://github.cor	256 word data RAM, PIC like	short LUT inst ROM
lgp30	http://www.e-b	stable	Stanley Frankel	accum	32	32																Y	vhdl	42	LGP-30	Y	yes	N		4K	4K	N			3		2017		FPGA version of LGP30 drum computer	also LGP21, RPC4000, 65F02
lipsi	https://github.c	stable	Martin Schoeberl	accum	8	8	cyclone4	Martin	Schoe	162		4		1	162			0.17	1.0	167.0			scala	2		Y		N	N	64K	64K	Y	9	3	16		2017	2019	https://github.cor	goal is 100 LUTs, program mapped to	"Lipsi, a very tiny processor"
lwrisc	https://opencor	stable	Li Wu	accum	8	12	arria-2	James	Brakef	88		A		1	230	##	q13.1	0.17	1.0	443.6	I		verilog	9	risc_core		asm	N	Y	256	2K	Y	16				2008	2009		ClaiRISC simplified PIC, 4 reg rtn stack	absolute addressing only, lowered MIPS/clk
magic-1	http://www.homebrewcp	Bill Buzbee	accum	8	8																		schematic			Y	yes	N		2M	2M	Y	256	5	7		2004	2014	https://hackaday.i	TTL computer, 6809ish, schematics o	magic-16 planning, 200 TTL chips
mano_machine	https://github.c	stable	Susam Pal	accum	16	16	kintex-7-3	James	needs	364		6				##	14.7	0.67	2.0				vhdl	5	microproc	Y		N		4K	4K	N	25				2005	2016	https://en.wikiped	course project, bidir mem data	for XC9572 CPLD, large # of latches
mano-compute	https://github.com/Amin	Amin Aliari	accum	16	16																		vhdl	19	sayeh	Y		N		4K	4K	N	25				2020		https://en.wikiped	Mano uP implementation, course pro	different use of sayeh: *simple & yet enough*
mcpu	https://opencor	stable	Tim Boscke	accum	8	8	spartan-6	James	Brakef	41		6			384	##	14.7	0.08	1.0	749.0	X		vhdl	1	tb02cpu2	Y	asm	N		64	64	Y	4				2007	2018	https://github.cor	MCPU A minimal CPU for a CPLD	reduced MIPS/clk due to only 4 inst
mcu8	https://opencor	alpha	Dimo Pepelyashev	accum	8	8	kintex-7-3	James	Brakef	274		6			299	##	14.7	0.33	1.0	360.1	X		vhdl	16	processor_E		asm			256	256	Y	17				2008	2009		asm, simulated, builds?	
micro16b	http://members	beta	John Kent	accum	16	16	kintex-7	James	Brakef	205		6			434	##	14.7	0.33	2.0	349.0	X		vhdl	1	u16bcpu	Y	asm	N	N	64K	4K	Y	8				2002	2008	http://members.o	very limited inst set	MIPS/clk adj'd, 2 clks/inst
micro8a	http://members	beta	John Kent	accum	8	16	kintex-7	James	Brakef	531		6			204	##	14.7	0.33	3.0	42.3	X		vhdl	11	Micro8	Y		N	N	2K	2K	Y					2002	2002	http://members.o	derived from Tim Boscke's mcpu	also micro8 and micro8b variants
mimafpga	https://github.c	stable	Manuel Killinger	accum	24	24																Y	vhdl	32	mimapprc	Y		N					19				2019			Minimal Machine processor taught at	has testbench
misc16	https://github.com/Steve	Steve Teal	accum	16	16	**zu-3e**	James	Brakef	197	78	6			500	##	v21.2	0.22	1.0	558.4	X	B	vhdl	1	misc	Y	yes	N		64K	64K	N	10				2021		https://github.cor	16-bit minimal CPU, has a single instruction 'mov' & eforth	
misc16	https://github.com/Steve	Steve Teal	accum	16	16	**zu-3e**	James	Altera	mem		6				##	v21.2	0.22	1.0		I	Y	vhdl	9	misc_forth	Y	yes	N		64K	64K	N	10				2021			16-bit minimal CPU which only has a single instruction 'mov'	
mitecpu	https://github.c	untested	Jeff Bush	accum	8	11																						N	Y	256		Y	7				2017	2017		only 7 inst, also: RISC-Processsor, **ChiselGPU,** LispMicrocontroller, **PASC** & NyuziProc	
mix-fpga	https://opencor	alpha	Michael Schroeder	accum	31	31																	verilog	29	mix	Y		Y		4K	4K	N	49	4	8		2021		https://en.wikiped	binary version of the MIX-Computer as described in "The Art of Computer Programm	
mocha	https://github.c	stable	Sanjay Gupta	accum	8	8																	vhdl	29	processor	Y	asm	N		64K	64K	Y	31				2018			8-bit microcontroller developed at NIIT University, course materials include full RTL &	
mroell_cpu	https://bitbucke	stable	Matthias Roell	accum	8	8	kintex-7-3	James	added	185		6			357	##	14.7	0.33	1.0	637.1	X		vhdl	8	cpu	Y							10				2014	2016		university course project	
multicomp	http://searle.ho	untested	Grant Searle	accum	8	8																															2014		https://blog.gadge	6502, 6800, 6809 & Z80 on Cyclone II;	Basic, CamelForth and CPM; also SD card, UAR
multicomp	https://github.c	untested	Doug Gilliland	accum	8	8																															2021		https://hackaday.i	6502, 6800, 6809 & Z80 on Cyclone II;	console available
mycpu	http://www.my	mature	Dennis Kuschel	accum	8	8	kintex-7-3	James	Brakef	3428		6	1		155	##	14.7	0.33	3.0	5.0	X		vhdl	28	cpu_top	Y		N		64M	64M	Y					2010			originally in TTL	micro-coded
ncore	https://opencor	alpha	Stefan Istvan	accum	16	8	kintex-7-3	James	Brakef	223		6			105	##	14.7	0.67	1.0	316.3	X		verilog	3	nCore	Y		N		128K	64K		16		16		2006	2018		This is a little-little processor core	
nibblercpu	https://github.com/bchan	Bryan Chan	accum	4	8																		system v	24	nibbler	Y		N	Y	4K	4K						2017		http://www.rayslo	originally a TTL project	
nibblercpu	https://gist.github.com/e	erin candescent	accum	4	8																		vhdl	1	nibblercpu	Y		N	Y	4K	4K						2014		https://www.bigm	4-bit CPU in VHDL	seondary web link has documentation
non-von-1	https://www.ch	stable	Christopher Fenton	accum	8	8	kintex-7-3	James	Brakef	230		6			556	##	14.7	0.33	1.0	797.1			verilog	1	nonvontop		no	N		64		Y	30							SIMID in tree structure	A & B regs, instructions broadcast	
opc.opc2cpu	https://github.c	stable	revaldinho	accum	8	16	kintex-7-3	James	reduce	117		6			556	##	14.7	0.15	4.0	178.1	X		verilog	2	opc2cpu	Y	asm	N	N	256	1K	Y	12	3			2017	2019	https://revaldinho	OPC2 revised OPC1, for XC9572 CPLD	see hackaday One Page Computing Challenge
opc.opc3cpu	https://github.c	stable	revaldinho	accum	16	16	kintex-7-3	James	reduce	174		6			526	##	14.7	0.30	4.0	226.9	X		verilog	2	opc3cpu	Y	asm	N	N	64K	64K	N	13	3			2017	2019	https://revaldinho	OPC3 16-bit OPC1, for XC95144 CPLD	see hackaday One Page Computing Challenge
opc.opccpu	https://github.c	stable	revaldinho	accum	8	16	kintex-7-3	James	reduce	101		6			526	##	14.7	0.15	4.0	195.4	X		verilog	2	opccpu	Y	asm	N	N	256	2K	Y	13	3			2017	2019	https://revaldinho	OPC1 one page computer for CPLD	**see hackaday One Page Computing Challe**
osu8	https://www.pi	alpha	Paul Stoffregen	accum	8	8																	schematic				Y	asm	N	N	64K	64K	Y	24				1994	2005	https://github.cor	OSU8 Microprocessor Project "instruc	*.1 schematics, doc at web page, currently acti
parwan		stable	Zainalabedin Navabi	accum	8	8	kintex-7-3	James	Brakef	157		6			435	##	14.7	0.33	4.0	228.5	X		verilog	16	par_beh	Y	yes	N	N	4K	4K	Y					1995	1997	2nd uP in director	from VHDL: Analysis and Modeling of	AKA cpu8, both vhdl & verilog versions
parwan		stable	Zainalabedin Navabi	accum	8	8	kintex-7-3	James	Brakef	161		6			76	##	14.7	0.33	4.0	38.8	X		vhdl	2	parwan	Y	yes	N	N	4K	4K	Y					1995	1997	2nd uP in director	from VHDL: Analysis and Modeling of	AKA cpu8, both vhdl & verilog versions
pcycle	https://github.com/domir	Dominik Salvet	accum	4	8																		vhdl	5	pcycle	Y		N	Y	16	128		12				2015	2021		inspired by redstone processor in Mine	craft, 1st custom VHDL design by author
popcorn	http://www.fpg	stable	Jeung Joon Lee	accum	8	8x	kintex-7-3	James	Brakef	267		6			347	##	14.7	0.33	1.0	428.4	X		verilog	4	pc	Y		N		64K	64K	Y	43				1998	2000		small 8 bit uP	
prawn		errors	Tadatoshi Ishii	accum	8	8	spartan_6	James	missing	files		6				##	14.7	0.33	3.0				vhdl	2	prawn	Y	yes	N	N	4K	4K	Y					1992			reduced version of parwan from VHDL: Analysis and Modeling of Digital Systems, 19	
pt13	http://www.sing	stable	Daniel Ogilvie	accum	8	8	kintex-7-3	James	Brakef	301		6			357	##	14.7	0.33	3.0	130.5			verilog	1	pt13	Y	asm	N	Y	64K	8K	Y	40	3			2011	2018	https://www.edn.	PT13 is optimized to be completely e	micro-code & register updates, minimal ISA
pumpkin	https://github.com/Steve	Steve Teal	accum	16	16	**zu-3e**	James	Brakef	166	67	6			625	##	v21.2	0.67	2.0	1261			vhdl	6	hello_wor	Y	asm	N		4K	4K		14				2020			scalable, 16-bit, 16 instruction soft CP	LUT RAM inferred (small size)
pumpkin	https://github.com/Steve	Steve Teal	accum	16	16	**zu-3e**	James	Brakef	230	131	6		1	450	##	v21.2	0.67	2.0	656			vhdl	6	myco	Y	asm	N		4K	4K		14				2020			scalable, 16-bit, 16 instruction soft CP	emulates Myco, forced block RAM
reflet	https://github.com/Arkae	Maxime Bouillot	accum	8	8																		verilog															https://github.cor	original design	most ops between accumulator & register, risc
risc_cpu	https://electron	untested		accum	8	8																	vhdl					N		32	32	Y	8				2017				
rtf65002	https://opencor	alpha	Robert Finch	accum	32	8	kintex-7-3	James	Brakef	11216		6	4	6	123	##	v14.1	0.67	2.0	3.7	X		verilog	10	rtf65002d	Y		N		4G	4G	Y			16		2013	2013	https://github.cor	32-bit 6502 + 6502 emulation	"proven"
sap	https://opencor	stable	Ahmed Shahein	accum	8	8	kintex-7-3	James	no LUT	48		6			200	##	14.7	0.10	4.0	104.2	X		vhdl	15	mp_struct			N		16	16	Y	5				2012	2022	https://shirishkoir	Simple as Possible Computer from MA	https://www.youtube.com/watch?v=prpyEFxZ
scamp-cpu	https://github.c	beta	James Stanley	accum	16	16																	verilog	76	fpga-cpuii	Y	asm	N		64K	64K						2022		https://hackaday.i	TTL & Verilog home built, has OS	pictures of TTL version
simple_ttl_cpu	https://github.com/mons	Ken Boak	accum	8	8																		schemat	10													2021			Digital schematic, very minimal	
suite-16	https://github.com/mons	Ken Boak	accum	16	8																		schemat	7													2020			Digital schematic, version of sweet-16	
t180-cpu		stable	Leonard Brandwein	accum	16	8	kintex-7-3	James	bypass	709		6			83	##	14.7	0.67	3.0	26.2	X		vhdl	23	cpu	Y		N	N	64K	64K	Y	182				2016	2016	https://www.vtto	8-bitter with pc, sp, a, b, c & d regs	based on Viktor Toth's 4 bit microcontroller
td4	https://github.c	stable	cielo_ee	accum	8	8	spartan-3	James	Brakef	102					200	##	14.7	0.20	1.0	392.2	X		verilog	5	td4_top						16	Y					2012	2015			very small uP
tiny8	https://opencor	altera dsg	Ulrich Riedel	accum	8	8	arria-2	James	needs	async ROM		A				##	q18.0	0.33	3.0		I		ahdl							256	64K	Y			256		2002	2009		Altera megafunctions	
tinyfpga	https://github.c	stable	Ken Jordan	accum	8	8	kintex-7-3	James	Brakef	185		6		1	175	##	14.7	0.33	3.6	86.9	X		vhdl	12	system			N	N	16	16	Y	10				2017	2017		educational 8-bitter with 4-bit addres	why use block RAM?
tis-100	https://github.com/Maste	Felix Queißner	accum	8	8																		vhdl	2	tis100	Y	asm	N		256	256	Y	13				2015	2016	https://en.wikiped	programming/puzzle video game by Zac	htronics Industries
tisc	https://opencor	beta	Vincent Crabtree	accum	8	8	kintex-7-3	James	Brakef	195		6			87	##	14.7	0.33	1.0	147.1	X		vhdl	1	TISC			N		256	1K	Y			2		2009	2009		Tiny Instruction Set Computer	minimal accumulator machine
uos	https://opencor	mature	Daniel Roggen	accum	8	16	kintex-7-3	James	Brakef	441		6			270	##	14.7	0.33	3.0	67.4	X		vhdl	14	cpu	Y								3	4		2014	2017		UoS Educational Processor	inspired by x86 ISA
up3	https://people.e	stable	Bruce Land	accum			cyclone-2	Bruce	Land	186		4		1		##	q8.0						vhdl	1	de2_top															Cornell ECE576	basic core is scomp, used by up3 & de2_top'
usimplez	https://opencor	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo	Salvade	48		4			134		q9.1	0.17	2.0	237.9	I		vhdl	3	usimplez_cpu			N		512	512		8				2011		http://www-gti.de	part of university course, simplez+i4	has an index register
vhdl_cpu	https://github.com/CGras	Charles Grassin	accum	8	16	spartan-3	Charl			203		4					14.7	0.20	2.0				vhdl	6	computer	Y	asm	N	N	256	256	N	14				2017	2020	http://charleslabs	educational, very simple	case statement program
ARC	https://www.sy	proprietar	Synopsys	ARC	32	16	porprietary												1.0				proprietary			Y	yes			4G	4G							https://www.sync	several families each with options	for ASIC use, FPGA versions avail
arm_cpu_ddca	https://github.com/nguye	Evan Nguyen	arm	32	32	**zu-3e**	James	LUT RAM for inst & dat		6						##	v21.1	1.00	1.0				system v	23	top	Y	yes	Y		4G	4G	Y			16		2021		from "Digital design and computer ar	single cycle, empty synthesis	
arm_rusian	https://github.com/0xD5(	ruslan	arm	32	32	**zu-3e**	James	LUT RA	2360	4815	6			200	##	v21.1	1.00	1.0	84.7			system v	6	ARM_Mul	Y	yes	Y		4G	4G	Y			16		2019		from "Digital design and computer ar	single cycle,	
arm_rusian	https://github.com/0xD5(	ruslan	arm	32	32	**zu-3e**	James	LUT RA	392		6				##	v21.1	1.00	1.0				system verilo		ARM_Pipe	Y	yes	Y		4G	4G	Y			16		2019		from "Digital design and computer ar	incomplete RTL, prob 4 student exercise	
arm_rusian	https://github.com/0xD5(	ruslan	arm	32	32	**zu-3e**	James	LUT RA	3563		6			147	##	v21.1	1.00	1.0	41.2			system verilo		ARM_Sing	Y	yes	Y		4G	4G	Y			16		2019		from "Digital design and computer ar	multi-cycle	
arm4u	https://opencores.org/pr	Jonathan Masur	arm	32	32	**zu-3e**	James	altera	primitives		6				##	v21.1	1.00	1.0		A		vhdl	12	cpu	Y	yes	Y		4G	4G	Y	80		16		2014	2014		ARMv3 ISA, clones early ARM processors in functionality	
cbox16	https://github.com/Engin	engineersbox	arm	16	16	spartan7	James	errors			6				##	v22.1							schemat	10	manual_cpu					64K	64K				8		2022			ARMv7 / MIPS IV hybrid ISA microarc	Digital schematic, VHDL & verilog
core_arm	https://opencor	beta	Konrad Eisele	ARM	32	16	kintex-7-3	James	Brakef	1239		6		3	250	##	14.7	1.00	1.0	201.8	X	Y	vhdl	151	arm_proc	Y	yes	N		256M	256M				16		2004	2009	http://cfw.source	very large project with many unused	missing files found in sourceforge dir, very litt
cortex_m3	http://www.clo	proprietar	Tobias Strauch	ARM	32	16																	proprietary												16		2013		cortex M3 data sh	claims to be mature	various academic papers, several projects
cpu-arm	https://github.com/techc	Ankit Solanki	ARM	32	32																		vhdl	18	processor	Y	yes	Y		4G	4G	Y	80		16		2018			Design, implementation and simulatic	probably course work
nnarm	ftp://ftp.gwdg.d	untested	Sheng Shen	ARM	32	16																																		mentioned at https://en.wikipedia.org	/wiki/Amber_(processor_core), ran afoul of A
ARM_Cortex_A	https://develope	ASIC	ARM	ARM A53	64	32	asic	Xilinx		6000		A			1500			2.00	0.5	#####			asic					Y	yes	Y			Y						https://en.wikiped	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
ARM_Cortex_A	https://develope	ASIC	ARM	ARM A9	32	16	arrira V	altera		4500		A			1050			2.50	1.0	583.3			asic					Y	yes	Y								2012	https://en.wikiped	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
ARM_Cortex_M	https://www.ar	proprietar	ARM	ARM M1	32	16						6						1.00	1.0		X		encrypted					Y	yes	N		4G	4G	Y			16	3	2019	https://www.arm	free use on Xilinx Vivado, encrypted	RTL, uses Digilent A7 or S7 board, AIX bus interfa
ARM_Cortex_M	http://www.arm	proprietar	ARM	ARM M1	32	16	virtex-5	ARM	65nm	1900		6			200			1.00	1.0	105.3	AIX		proprietary					Y	yes	N		4G	4G	Y			16	3	2007		https://en.wikiped	ARM Cortex M0, M1 & M3 avail for FR	see xilinx Xcell64
ARM_Cortex_R	https://develope	ASIC	ARM	ARM R5	32	16	asic	Xilinx				A			600				1.0				asic					Y	yes	Y		4G	4G	Y	80		16				https://en.wikiped	uses pro-rated LC area	real-time interrupt handling
amber	https://opencor	stable	Conor Santifort	ARM7	32	32	**zu-3e**	James	area o	3105	1857	6		10	168	##	v21.1	0.75	1.0	40.7	ILX		verilog	25	a23_core	Y	yes	N		4G	4G	Y	80		16	3	2010	2017	https://en.wikiped	no MMU, shared cache	
amber	https://opencor	stable	Conor Santifort	ARM7	32	32	**zu-3e**	James	area o	5066	2382	6		20	175	##	v21.1	1.05	1.0	36.4	ILX		verilog	25	a25_core	Y	yes	N		4G	4G	Y	80		16	5	2010	2017	https://en.wikiped	no MMU	
amber	https://opencor	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James	Brakef	6103		6		18	127	##	v18.2	1.05	1.0	21.8	ILX		verilog	25	a25_core	Y	yes	N		4G	4G	Y	80		16	3	2010	2017	https://en.wikiped	no MMU	
amber	https://opencor	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James	Brakef	6409		6		2	82	##	14.7	0.75	1.0	9.6	ILX		verilog	25	a23_core	Y	yes	N		4G	4G	Y	80		16	3	2010	2017	https://en.wikiped	no MMU, shared cache	2048 LUTs used as single port RAM
oks8	https://opencor	alpha	Kongzilee	ARM7	32	32	kintex-7-3	James	bad coding	practice		6				##	14.7	0.67	1.0				verilog	8	oks8	Y	yes	N		64K	64K	Y					2006	2009		clone of KS86C4204/C4208/P4208, SAM	87RI instruction set
storm_core	https://opencor	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James	Brakef	2312		6	3		179	##	14.7	1.00	1.0	77.4	IX		vhdl	16	core	Y	yes	N		4G	4G	Y			32	8	2011	2014		Storm Core (ARM7 compatible)	I & D caches not compiled
storm_soc	https://opencor	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James	Brakef	3514		6	3	4	159	##	14.7	1.00	1.0	45.2	X	Y	vhdl	40	storm_top	Y	yes	N		4G	4G	Y			32	8	2012	2015		STORM SoC	cache & no peripherals
zap	https://opencor	alpha	Revanth Kamaraj	ARM7	32	32	kintex-7-3	James	Brakef	7558		6	1	9	135	##	14.7	1.00	1.0	17.9	X		verilog	37	zap_top	Y	yes	N	N	4G	4G	Y			16		2017	2022	https://github.cor	ARMv4T & Thumbv1	has cache & mmu

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe lan	start year	last revis	secondary web link	note worthy	comments
zap	https://opencor	alpha	Revanth Kamaraj	ARM7	32	32	arria-2	James	high D	10284		A	2	38	111	##	q18.0	1.00	1.0	10.8	X		verilog	37	zap_top	Y	yes	N	N	4G	4G	Y				2017	2022	ddi0100e_armv1-	ARMv4T & Thumbv1	has cache & mmu
arm9-soft-cpu	https://github.com/risclit		Li Xinbing	ARM9	32	32	**zu-3e**	James	vivado	3914	1257	6	4		167	##	v21.1	1.00	1.0	42.6			verilog	4	arm9_cor	Y	yes	Y		4G	4G	Y				2020		ARMv4-compatible CPU core	Dhrystone value: 1.2 DMIPS/MHz
arm9-soft-cpu	https://github.com/risclit		Li Xinbing	ARM9	32	32	**zu-3e**	James	vivado	2098	778	6	4		238	##	v21.1	1.00	1.0	113.5			verilog	4	risclite_m	Y	yes	Y		4G	4G	Y				2020		ARMv4-compatible CPU core	no interrupts or reg banks
arm9-soft-cpu	https://github.com/risclit		Li Xinbing	ARM9	32	32	**zu-3e**	James	vivado	1807	736	6			357	##	v21.1	1.00	1.0	197.6			verilog	4	risclite_m	Y	yes	Y		4G	4G	Y				2020		ARMv4-compatible CPU core	no mult, interrupts or reg banks
armv4_uarch	https://github.com/grant		Grant Wilk	ARM9	32	32	**max10**	Grant Wilk		2860		4			50	##	q18.0	1.00	1.0	17.5	A		vhdl	18		Y	yes	N		4G	4G	Y		16		2020	https://grantwilk.c	custom uarch for the ARMv4 ISA on I	course work, top level is schematic
armv4_uarch	https://github.com/grant		Grant Wilk	ARM9	32	32	**zu-3e**	James	vivado defaults			6				##	v21.1	1.00	1.0		A		vhdl	18		Y	yes	N		4G	4G	Y		16		2020	https://grantwilk.c	custom uarch for the ARMv4 ISA on I	course work, Quartus project
atmega8_pong	https://fr.wikive	stable	Juergen Sauermann	AVR	8	16	spartan-3	James	clock d	2767		4	1	10	53	##	14.7	0.33	1.0	6.3	X	Y	vhdl	37	avr_fpga_	Y	yes	N		64K	64K	Y	17		4	2017	2017		several projects using avr core	uses Sauermann core
atmega8_pong	https://fr.wikive	stable	Juergen Sauermann	AVR	8	16	spartan-3	James	clock d	2898		4	1	11	53	##	14.7	0.33	1.0	6.0	X	Y	vhdl	37	pacman_M	Y	yes	N		64K	64K	Y	17		4	2017	2017		several projects using avr core	uses Sauermann atmega16 core
attiny_atmega	https://opencor	beta	Gheorghiu Iulian	AVR	8	16	**zu-3e**	James	vivado	1366	116	6			179	##	v21.1	0.33	1.0	43.1	X	Y	verilog	9	mega_cor	Y	yes	N		64K	128K	Y	72		32	2018	2019	https://git.morgot	configurable AVR processor w/8 configurations	
avr_core	https://opencor	stable	Rusian Lepetenok	AVR	8	16	**zu-3e**	James	vivado	1624	519	6			250	##	v21.1	0.33	1.0	50.8	X		verilog	70	avr_core	Y	yes	N		64K	128K	Y	72		32	2002	2017		VHDL core also	
avr_core	https://opencor	stable	Rusian Lepetenok	AVR	8	16	kintex-7-3	James	Brakef	2135		6			127	##	14.7	0.33	1.0	19.7	X		verilog	15	avr_core	Y	yes	N		64K	128K	Y	72		32	2002	2017		VHDL core also	
avr_fpga	https://opencor	stable	Juergen Sauermann	AVR	8	16	kintex-7-3	James	Brakef	1606		6	1	6	120	##	14.7	0.33	1.0	24.7	X		vhdl	20	cpu_core	Y	yes	N		64K	128K	Y	72		32	2009	2010		extended lecture on FPGA uP design	
avr_fpga	https://opencor	stable	Juergen Sauermann	AVR	8	16	kintex-7-3	James	Brakef	1877		6	1	6	115	##	14.7	0.33	1.0	20.2	X	Y	vhdl	20	avr_fpga	Y	yes	N		64K	128K	Y	72		32	2009	2010	https://fr.wikivers	extended lecture on FPGA uP design	missing module in atmega8_pong_vga
avr_fpga	https://opencor	stable	Juergen Sauermann	AVR	8	16	**zu-3e**	James	vivado	1606		6	1	6		##	v21.1	0.33	1.0		X		vhdl	20	cpu_core	Y	yes	N		64K	128K	Y	72		32	2009	2010		extended lecture on FPGA uP design	
avr_fpga	https://opencor	stable	Juergen Sauermann	AVR	8	16	**zu-3e**	James	vivado	1877		6	1	6		##	v21.1	0.33	1.0		X	Y	vhdl	20	avr_fpga	Y	yes	N		64K	128K	Y	72		32	2009	2010	https://fr.wikivers	extended lecture on FPGA uP design	missing module in atmega8_pong_vga
avr_hp	https://opencor	stable	Strauch Tobias	AVR	8	16	kintex-7-3	James	2 slot l	1554		6			223	##	14.7	0.33	1.0	47.4	X		vhdl	10	avr_core_on	Y	yes	N		64K	128K	Y	72		32	2010	2012		hyper pipelined (eg barrel) AVR	
avr8	https://opencor	beta	Nick Kovach	AVR	8	16	kintex-7-3	James	Brakef	174		6			418	##	14.7	0.33	1.0	792.2	X		verilog	1	rAVR	Y	yes	N		64K	64K	Y	17		4	2010	2010		Reduced AVR Core for CPLD	not a full clone, doc is opencores page
avr-cpu	https://github.c	stable	Sung Hoon Choi	AVR	8	16	**zu-3e**	James	vhdl 2008 usage			6				##	v21.1	0.33	1.0				vhdl	15	avr_cpu	Y	yes	N		64K	128K	Y	72		32		2019			
avrtinyx61core	https://opencor	beta	Andreas Hilvarsson	AVR	8	16	kintex-7-3	James	Brakef	1243		6			194	##	14.7	0.33	1.0	51.5	X		vhdl	1	mcu_core	yes		N		64K	128K	Y	72		32	2008	2009			
ax8	https://opencor	stable	Daniel Wallner	AVR	8	16	spartan-6	James	missin	1549		6		1	213	##	14.7	0.33	1.0	45.3	X		vhdl	14	A90S1200	yes		N		64K	128K	Y	72		32	2002	2010		both A90S1200 & A90S2313	inserted fake inst ROM
classy_core_17	https://github.com/classy		Andreas Schweizer	AVR	8	16	spartan-3	Andreas Schw		358		4			164	##	14.7	0.33	1.0	151.2			vhdl	8	top	Y	yes	N		64K	128K	Y	72		32		2019	https://blog.classy	adjuct to some custom logic	Implementing a CPU in VHDL parts 1..3
navre	https://opencor	stable	Sebastien Bourdeaudu	AVR	8	16	kintex-7-3	James	Brakef	990		6			207	##	14.7	0.33	1.0	69.0	AILX		verilog	1	softusb_n	Y	yes	N		64K	64K	Y	72		32	2	2010	2013	https://www.milk	AVR clone, part of www.milkymist.org	
openxlr8	https://github.com/Aloriu		alorium technology	AVR	8	16																Y	verilog														2019	https://www.alori	AVR clone, Snō and Hinj Arduino com	https://www.youtube.com/watch?v=Drr1M9z
pavr	https://opencor	alpha	Doru Cuturela	AVR	8	16	kintex-7-3	James	Brakef	2630		6		1	132	##	14.7	0.33	1.0	16.5	X		vhdl	18	pavr_cont	Y	yes	N	Y	4K	4M	Y	72		32	6	2003	2009		superset of AVR	
risc8softcore	https://github.com/osres		Trammell Hudson	AVR	8	16																	verilog	6	risc8-soc	Y	yes	N	Y	64K	64K	Y					2020	2020		mostly compatible with the AVR instruction set	
riscmcu	https://opencor	stable	Yap Zi He	AVR	8	16	arria-2	James	LPM parameter errors			4				##	q18.0	0.33	1.0		I		vhdl	15	v_riscmcu	Y	yes	N	Y	128	512	Y	92		16	3	2002	2009		thesis	added 5 inst to AVR
softavrcore	https://opencores.org/pr		Andras Pal	AVR	8	16	atrix-7-3														XL	Y	verilog	8	top	Y	yes	N		64K	64K	Y					2019	2020	https://szofi.net/p	full implementation of AVR 2-stage pi	variants: VR2, AVR2.5, AVR3, AVR4 & AVR5
xmega_core	https://opencor	beta	Gheorghiu Iulian	AVR	8	16	kintex-7-3	James	Brakef	1116		6			120	##	14.7	0.33	1.0	35.6	X		verilog	34	mega_cor	Y	yes	N		64K	128K	Y	72		32	2017	2018	https://git.morgot	8 AVR cores, 4 sets LUT counts poste	https://git.morgothdisk.com/VERILOG/VERILO
c2650_mister	https://github.com/Grabu		Grabulosaure	c2650	8	8															I	Y	vhdl & V	39	sys_top	Y		N		32K	32K	Y					2018	2020	https://en.wikiped	clone of Signetics 2650 uP	based on the IBM 1130, Altera project & PLL
hp86b	https://sites.goo	errors	Olivier De Smet	Capricorn	8	8	spartan-3	James	unresolved xilinx interf			4				##	14.7	0.33	2.0				verilog	85	cpu										64		2010		https://en.wikiped	uses PicoBlaze, emualtes HP86B	picoblaze uart uses LUT4s
btsr1arch	https://github.c	alpha	Brendan Bohannon	CISC	64	16											14.7				X		verilog	149	bjx2	Y	yes	Y	N	256T	256T	Y	64		32	2018	2022	https://www.yout	64-bit regs, 16x inst, 48-bit VM	BJX2 is superset of BtSR1, 4 data sizes
btsr1arch	https://github.c	beta	Brendan Bohannon	CISC	32	16	kintex-7-3	James	Brakef	4762		6		10	167	##	14.7	1.00	1.5	23.3	X		verilog	11	bsrexunit	Y	yes	Y	N	64K	64K	Y	64		32	2018	2022		is BtSR1, msp430 like, fltg-pt defined	3 data sizes, no (R++) or (--R) modes
copro6502	https://github.c	stable	David Banks	CISC	8	8			ISE projects for each core													Y	VHDL & Verilog			Y										2014	2017	https://stardot.or	65C102, Z80, 80286, 6809, PDP11, ARM2 & 32016 cores selectable by DIP switch on	
forwardcom	https://github.com/Forwa		Agner Fog	cisc	64	32	atrix-7	Agner Fog		12026		6			70	##	v20.1	1.00	1.0	5.8	X		system v	18	top	Y	asm	Y		64K	32K	Y		64		2016	2021	https://github.com	x86 like, complete ISA, MMX & vector	16-bit compressed inst, x86 adr modes
lc-2	http://www.cs.u	mature	Eric Frohnhoefer	CISC	16	16	kintex-7-3	James	gate level primitives			6				##	14.7	0.67	2.0				vhdl	13	lc2_all	Y	yes	N		64K	64K	N	16		8	2002	2002	https://en.wikiped	from book: 978-0072467505 by Patt &	educational, compiled via Synopsys
one-der	http://www.drd	untested	Al Williams	CISC	32		spartan-3	James	missimg file			4				##	14.7	1.00	1.0				verilog	18	topbox												2009	2009		The One Instruction Wonder	TTA
raptor16	www.spacewire	stable	Steve Haywood	CISC	16	16	kintex-7-3	James	Brakef	590		6			319	##	14.7	1.40	2.7	280.2	X		vhdl	1	raptor16	Y	yes	N	N	64K	64K	N					2004			8 data & 8 adr regs	no multiply, 8 adr modes
w450		errors	Ze Long	CISC	8	8	kintex-7-3	James	blocking & non-blockin			6				##	14.7	0.33	3.0				verilog	3	w450					256	256	Y	8		4	3	2012			appears to be class project	3 versions of w450, used latest, patches cause
xproz	http://www.bitl	stable	Herbert Kleebauer	CISC	16	16			schematic based										1.0				schematic			Y	asm	N		64K	64K						1993	1995		documentation in German	*.1 schematic design
z3	https://opencor	stable	Charles Cole	CISC	8	8	arria-2	James	Brakef	3495		A	2		141	##	q18.0	0.33	3.0	4.4	I		verilog	3	boss	Y				128K	128K						2014	2014	https://en.wikiped	Infocom Z-Machine V3, youtube vide	http://inform-fiction.org/zmachine/standards/
z-machine	https://github.com/stem	veril	Robert Baruch	CISC	8	8	arria-2	James	Brakefield			A				##	q18.0	0.33	3.0		I		system v	15	plugh	Y		N									2016		http://inform-ficti	Z-machine (Zork)	https://www.youtube.com/watch?v=2fNBkUC
t400	https://opencor	stable	Arnim Laeuger	COP400	4	8	spartan-2	Arnim Laeugg		643		3		2	60			0.16	4.0	3.7	IX		vhdl	36	t400_core	Y	yes	N	Y	64	1K	Y					2006	2009		implementation of National's 4-bit COP400 microcontroller	
cray1	www.chrisfento	alpha	Christopher Fenton	CRAY1	64	16	kintex-7-3	James	Brakef	13463		6	19	10	127	##	14.7	6.00	1.0	56.6	X		verilog	46	cray_sys_	Y	yes	Y	N	4M	4M	N	128		536		2010	2015	https://www.chris	homebrew Cray1	24-bit address registers
cray1	www.chrisfento	alpha	Christopher Fenton	CRAY1	64	16	**zu-3e**	James	undefi	11510		6	15	1		##	v21.1	6.00	1.0		X		verilog	46	cray_sys_	Y	yes	Y	N	4M	4M	N	128		536		2010	2015	CRAY data sheets	homebrew Cray1	24-bit address registers
cray2_reboot	https://opencor	beta	John Kula	CRAY2	64	16																	non-EDIF	gate & module	Y	yes	Y	N	256M	256M	N	128		528		2016	2017	Cray 1, 2 & 3 docs	gate level code	32-bit address registers
aspida	https://opencor	stable	Sotiriou	DLX	32	32	**zu-2e**	James	dated xilinx primitives			6				##	v20.1	1.00	1.0		X		verilog	10	DLX_top	Y	yes			4G	4G						2002	2009		DLX	compiled sync version
aspida	https://opencor	stable	Sotiriou	DLX	32	32	kintex-7-3	James	dated	3586		6			257	##	14.7	1.00	1.0	71.7	X		verilog	10	DLX_top	Y	yes			4G	4G						2002	2009		DLX	compiled sync version
dlx		errors	Martin Gumm	DLX	32	32	kintex-7-3	James	errors			6				##	14.7	1.00	1.0				vhdl	120		Y	asm								32		1995	2014		University of Stuttgart, asic dsgn	case statmt others clause has problems
dlx_calvino	https://github.com/aleter		Alessandro Calvino	DLX	32	32																	vhdl			Y	yes	N		4G	4G			32			2019		masters thesis	also supports Synopsys Design Compiler
dlx_chiara	https://github.c	stable	Alessandro Di Chiara	DLX	32	32	kintex-7-3	James	Brakef	2915		6			90	##	14.7	1.00	1.0	30.9	X		vhdl	32	a-dlx	Y	yes	N		4G	4G			32	5	2017	2017		Course project, no RTL comments, VHDL via instructor?	
dlx_nicola	https://github.c	stable	Nicola Vianello	DLX	32	32																	vhdl	37	a-dlx	Y	asm	N		4G	4G			32			2019		masters thesis	five stage pipeline, forwarding, automatic haza
dlx_palmiero	https://github.c	ASIC	Christian Palmiero	DLX	32	32	kintex-7-3	James	design heiarchy proble			6				##	14.7	1.00	1.0				vhdl	41	a-dlx	Y	yes	N		4G	4G			32	5	2015	2017		Course project, VHDL to netlist (STM	ASIC design
dlx_superscala	https://www.rs.	errors	Joachim Horch	DLX	32	32	kintex-7-3	James	degnerate			6				##	14.7	1.00	1.0				vhdl	4	dlx	Y	yes	N		4G	4G			32		1997	1998		Course project, Two inst/clock, doc in	collapses for no apparent reason
bobcat		beta	Stan Drey	DSP	16	24	kintex-7-3	James	Brakef	1622		6	1		107	##	14.7	0.67	1.0	44.0	X		vhdl	30	bobcat_co	Y		N		64K	64K						1998	2000			dead web links
dsp16	https://github.com/jotego		Jose Tejada	dsp	16	16	cyclone5	Jose Tejada		2471	612	A		12							I		verilog	12	jtdsp16	Y	asm	N	Y	64K	64K	N	29		16	2020	2021		compatible with ATT WE DSP16	
dspuva16	http://www.DTI	stable	Santiago de Pablo	DSP	16	16	kintex-7-3	James	Brakef	332		6			317	##	14.7	0.67	1.0	640.7	X		verilog	1	dspuva16		asm	N	Y	256	4K		40		16	2001	2004	www.1-core.com/	16 bit data memory, 24 bit regs	broken web link
oc54x	https://opencor	beta	Richard Herveille	DSP	16	16	kintex-7-3	James	Brakef	2225		6	1		180	##	14.7	0.67	1.0	54.1	X		verilog	10	oc54_cpu	Y	yes	N	Y	64K	64K						2002	2009		40-bit accumulator, barrel shifter	C54x clone
ensilica	http://www.ens	propriet	ensilica.com	eSi-1600	16	16	virtex-5	ensilica		1100		6			160			1.00	1.0	145.5	IX		verilog		eSi-1600	Y	yes			64K	64K	Y	92	10	16	5	2001	2016		verilog source included with license	room for 90 user inst, also as ASIC
ensilica	http://www.ens	propriet	ensilica.com	eSi-1600	16	16	virtex-5	ensilica		1100		6			160			1.00	1.0	145.5	IX		verilog		eSi-1650	Y	yes			64K	64K	Y	92	10	16	5	2001	2016		verilog source included with license	room for 90 user inst, also as ASIC
ensilica	http://www.ens	propriet	ensilica.com	eSi-3200	32	16	stratix-4	ensilica		2200		A			200			2.00	1.0	181.8	IX		verilog		eSi-3250	Y	yes			4G	4G	Y	104	10	16	5	2001	2016		verilog source included with license	room for 90 user inst, also as ASIC
ensilica	http://www.ens	propriet	ensilica.com	eSi-3200	32	16	stratix-4	ensilica		1800		A			200			1.50	1.0	166.7	IX		verilog		eSi-3200	Y	yes			4G	4G	Y	104	10	16	5	2001	2016		verilog source included with license	room for 90 user inst, also as ASIC
8bit_chapman	http://www.ece	beta	Rob Chapman, Steven	forth	8	8	**zu-3e**	James	vivado	132	63	6			305	##	v21.1	0.33	1.0	762.2	ILX		vhdl	10	stack_pro	Y		N		256	256	Y	24				1998	1998		course work	
8bit_chapman	http://www.ece	beta	Rob Chapman, Steven	forth	8	8	kintex-7-3	James	Brakef	176		6			131	##	14.7	0.33	1.0	245.5	ILX		vhdl	10	stack_pro	Y		N		256	256	Y	24				1998	1998		course work	
b16	www.bernd-pay	stable	Bernd Paysan	forth	16	5	spartan-6	James	Brakef	554		6			134	##	14.7	0.67	1.0	161.7	IX		verilog	15	b16	Y	yes	N		64K	64K	N					2002	2017	https://github.com	two versions: one/15 source files, derived from c18	
b16	www.bernd-pay	stable	Bernd Paysan	forth	16	5		James	Brakefield			6						0.67	1.0		IX		verilog	1	b16-small	Y	yes	N		64K	64K	N					2002	2019	https://github.com	two versions: one/15 source files, derived from c18	
bugs18	https://drive.google.com/		Myron Plichota	forth	16	18	spartan-7	Myron Plichota				6			48						X	Y	verilog	18	Bugs18_S	Y	asm	N		64K	64K	N	19				2022		Four bit op-codes, Python assembler	full set of RTL SOC devices
bytemachine	https://github.c	mature	c0pperdragon	forth	8	8	kintex-7-3	James	Brakef	319		6		1	250	##	14.7	0.33	2.0	129.3	IX		vhdl	7	bytemachine			N	N		4K	Y	30			2016	2017		top is Altera schematic	results are for 2016 bare core
cd16	http://anycpu.o	stable	Brad Eckert	forth	16	16	kintex-7-3	James	Brakef	681		4			83	##	14.7	0.67	2.0	41.0	IX	B	vhdl	16	cd16			N		128K	8M					2003	2003	http://web.archiv	Spartan-3 block RAM	bare core
cd16	http://anycpu.o	stable	Brad Eckert	forth	16	16	spartan-3	James	Brakef	618		4		7	31	##	14.7	0.67	2.0	16.9	IX	Y	vhdl	16	demosocext			N		128K	8M					2003	2003	http://web.archiv	Spartan-3 block RAM	includes stack RAMs & some inst RAM
cfm	https://github.com/cbiffle		Cliff L. Biffle	forth	16	16																	haskell	23				N		64K	64K					2018	2018	https://clash-lang	Forth-inspired processor targeting th	alu inst is ucoded, some missing ops
chad	https://github.com/bradle		Brad Eckert	forth	18	16	atrix-7-1	James	DFF ex	1982		6		5	127	##	v21.1	0.80	1.0	51.4	XIML		verilog	33	mcu_arty	Y	yes	N		64K	64K	N	23		16		2021			verilog, .f &.c code; fpga project files	max SOC, -1 speed grad
chad	https://github.com/bradle		Brad Eckert	forth	18	16	atrix-7-3	James	DFF ex	1995		6		5	175	##	v21.1	0.80	1.0	70.4	XIML		verilog	33	mcu_arty	Y	yes	N		64K	64K	N	23		16		2021			verilog, .f &.c code; fpga project files	max SOC, -3 speed grade
chad	https://github.com/bradle		Brad Eckert	forth	18	16	**zu-3e**	James	vivado	2196	2211	6		5	250	##	v21.1	0.80	1.0	91.1	XIML		verilog	33	mcu_arty	Y	yes	N		64K	64K	N	23		16		2021			verilog, .f &.c code; fpga project files	
chad	https://github.com/bradle		Brad Eckert	forth	18	16	atrix-7-3	James	option	1972		6		3	196	##	v21.1	0.80	1.0	79.5	XIML		verilog	33	mcu	Y	yes	N		64K	64K	N	23		16		2021			verilog, .f &.c code; fpga project files	min SOC, -3 speed grade
cpu16	http://www.ultr	stable	C.H. Ting	forth	16	5	kintex-7-3	James	Brakef	347		6			364	##	14.7	0.67	1.0	702.1	X		vhdl	1	cpu16			N	N	64K	64K	N	28				2000	2000		P16 in VHDL	CPU24.vhd with width=16
dataflow_chap	https://opencor	alpha	Rob Chapman, Steven	forth	16	16	kintex-7-3	James	file WebCase report			6					14.7	0.33	1.0				vhdl	27	DataFlowE	Y		N		256	256						2003			course work	
dfp	https://opencor	stable	Ron Chapman	forth	8	8	kintex-7-3	James	Brakef	297		6			192	##	14.7	0.33	1.0	213.2	X		vhdl	25	DataFlowE	Y											2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
ep16	https://github.c	beta	C.H. Ting	forth	16	5	kintex-7-3	James	Brakef	837		6			254	##	14.7	0.67	1.0	203.6	X		vhdl	5	ep16.vhd	Y	yes	N	N	32K	32K	N	32				2005	2012	PDF files	initialized Lattice memory blocks	5-bit instructions
ep24		stable	C.H. Ting	forth	24	6	kintex-7-3	James	substit	1020		6		3	167	##	14.7	0.83	1.0	135.6	X		vhdl	1	ep24	Y	asm	N	N		4K		27			2002	2002		room for 37 additional op-codes	removing stack clear: 503 LUT6 & 143MHz
ep32	https://www.am	propriet	C.H. Ting	forth	32	6	XP2	C.H. Ting		3368		4					ispL	1.00	1.0				proprietary														2007	2018	https://wiki.forth-	kindle book & RTL available: EP32 RIS	RTL: $25 from C.H. Ting
ep32	http://forth.org/	mature	CH Ting	forth	32	5																	vhdl	7	ep32	Y	forth	N									2012			has eForth binary & source	now free

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hard'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
eric5	http://www.ent	proprietar	Thomas Entner	forth	9	8	cyclone-4	entner-electr		110		4	opt		60			0.42	1.0	229.1	I		proprietary							512	1K				3-4		2005	2011		25 MIPS: ERIC5xs, ERIC5Q	
f18a	http://www.gre	asic	Chuck Moore	forth																			proprietary			Y	yes											AKA G144A12: 12x12 array	family of parallel processors
f21	http://www.ultr	asic	Jeff Fox	forth	21	5																	proprietary													1997	2011	http://www.ultrat	"machine forth", crazy address space	chip & simulator, AKA MuP21 or F21
fc16		paper	Richard Haskell	forth	16																		proprietary															PDF papers	chpt 11: VHDL By Example: Fundamentals of D
forth_cpu	https://anycpu.g	untested	Richard Howe	forth	16	16																	vhdl	11	top											2013	2021	http://www.aholn	https://github.com/howerj/forth-cpu	based on J1 uP, used to operate DIY GPS recie
forth_kf532	https://github.c	stable	Tarasov Ilia	forth	32	6	kintex-7-3	James	no *.c	1719		6	4	4	172	##	14.7	1.00	1.0	100.3	X		vhdl	1	kf532	N		N	Y	1K	16K						2013	2013		no trace of source code on web	
forth-cpu/h2	https://opencor	stable	Richard Howe	forth	16	16	kintex-7-3	James	Brakef	1858		6		9	149	##	14.7	0.67	1.0	53.8	X	Y	vhdl	11	top					64K	64K		25				2017	2020	https://github.cor	H2 Forth SoC, VHDL reads *.hex & *.b	derived from J1, hex & bin files in 2/16/2018 ta
ignite_ptsc		asic	George Shaw	forth	32	8													1.0				proprietary					N		4G	4G						1995	2002		ShBoom clone, fast ASIC with high co	PTSC web site had full documentation
J1	www.excamera	stable	James Bowman	forth	16	16	**zu-2e**	James	area o	253		6		1	336	##	v20.1	0.80	1.0	#####	X		vhdl	1	j1	Y	forth	N		64K	64K		20		2	2006	2015	https://github.cor	uCode inst, dual port block RAM	16 deep data & return stacks
J1	www.excamera	stable	James Bowman	forth	16	16	kintex-7-3	James	Brakef	335		6		1	180	##	14.7	0.80	1.0	431.0	X		vhdl	1	j1	Y	forth	N		64K	64K		20		2	2006	2015	https://github.cor	uCode inst, dual port block RAM	16 deep data & return stacks
J1a	www.excamera	stable	James Bowman	forth	16	16	kintex-7-3	James	DFF ex	518		6			412	##	14.7	0.80	1.0	636.1	X		verilog	3	j1	Y	forth	N		64K	64K		20		2	2006	2017	https://github.cor	uCode inst, dual port block RAM	DFF used for 18 deep data & return stacks
J1a32	www.excamera	stable	James Bowman	forth	32	16	kintex-7-3	James	DFF ex	930		6			358	##	14.7	1.00	1.0	384.4	X		verilog	3	j1	Y	forth	N		64K	64K		20		2	2006	2017		uCode inst, dual port block RAM	DFF used for 18 deep data & return stacks
J1b	www.excamera	stable	James Bowman	forth	32	16	kintex-7-3	James	DFF ex	2612		6			302	##	14.7	1.00	1.0	115.5	X		verilog	3	j1	Y	forth	N		64K	64K		20		2	2006	2017		uCode inst, dual port block RAM	DFF used for 32 deep data & return stacks
J1b_16	www.excamera	stable	James Bowman	forth	32	16	kintex-7-3	James	DFF ex	1588		6			355	##	14.7	1.00	1.0	223.4	X		verilog	3	j1	Y	forth	N		64K	64K		20		2	2006	2017		uCode inst, dual port block RAM	DFF used for 16 deep data & return stacks
j1sc	https://github.c	scala	Steffen Reith	forth	32	16																	scala	11	j1	Y	forth	N		64K	64K		20				2017	2018		J1 reimplemented using Scala/Spinal to	generate VHDL or Verilog
j1vh	https://github.com/flamir		Theo Hussey	forth	32	16															I		vhdl	5	j1vh	Y	forth	N		64K	64K		20					2019		VHDL clone of J1 forth CPU	altera block RAM
jop	https://opencor	stable	Martin Schoeberl etal	forth	16	16	cyclone-1	Martin	Schoe	2000		4			100		q10.0	0.67	1.0	33.5	I		vhdl	11	core	Y	yes	N		256K	256K						2004	2014		https://github.com/jop-devel/jop	java app builds some source code files
k1	http://mcforth.net/		Klaus Kohl-Schoepe	forth	16	16																	verilog	11	K1	Y	forth	N		64K	64K		24					2020		based on J1, Quartus project file	
kestrel-2	kestrelcompute	stable	Samuel Falvo II	forth	16	16	kintex-7-3	James	Brakef	735		6		8	172	##	14.7	0.67	1.0	157.2	X	Y	verilog	27	M_kestrel	Y	yes	N		64K	64K		20		2	2012	2015	https://hackaday.i	J1 with wishbone bus	M_j1a runs at 244MHz & 368 LUTs
microcore	http://www.pld	beta	Klaus Schleisiek	forth	12	8	kintex-7-3	James	Brakef	399		6		1	294	##	14.7	0.40	2.0	147.4	X		vhdl	30	ucore110	Y	asm	N	Y	512	2K						1999	2022	www.microcore.o	indexing into return stack, auto inc/d	only one block RAM? simplest core
microcore	http://www.pld	beta	Klaus Schleisiek	forth	16	8	kintex-7-3	James	Brakef	1101		6			168	##	14.7	0.67	2.0	51.1	X		vhdl	17	ucore120	Y	asm	N	Y	4K	4K						1999	2022		indexing into return stack, auto inc/d	no block RAM?, uses tri-state signals
microcore	https://github.c	beta	Klaus Schleisiek	forth	16	8						6			168	##	14.7	0.67	2.0		X		vhdl	17	ucore	Y	asm	N	Y	4K	4K							2021			
microforth	https://github.com/Forth		Jess Totorica	forth	18	18															I	Y	verilog	34	top	Y		N	Y	64K	64K	N	25				2019	2020	http://mindworks	Arduino-like board/platform based up	AKA F18, educational, loop stack
msl16		beta	Philip Leong, Tsang, Le	forth	16	4	kintex-7-3	James	Brakef	303		6			256	##	14.7	0.67	1.0	566.4	X		vhdl	13	cpu	Y	asm	N		256			16				2001			CPLD prototype	
myforthproces	https://opencor	stable	Gerhard Hohner	forth	32	8	SP-kintex	James	Brakef	2959		6		6	223	##	14.7	1.00	1.0	75.3	X		vhdl	58	mycpu	Y	yes	N		64M	64M		96				2004	2012		DPANS'94 32-bit Forth, masters thesis	25.15 Whetstones
nc4016	https://en.wikic	asic	Chuck Moore	forth	16																		proprietary															chapter in Koopman	
nige_machine	https://github.c	stable	Andrew Read	forth	32	8	kintex-7-3	James	Brakef	5033		6	8	33	123	##	14.7	1.00	1.0	24.5	X		vhdl	29	Board	Y	yes	N		16M	16M		512		512			2014		standalone Forth system	https://www.youtube.com/watch?v=PRItE8q6
nybbleForth	https://github.c	errors	Lars Brinkhoff	forth	16	4	kintex-7-3	James	missing init file			6				##	14.7	0.67	1.0				verilog	1	cpu	Y	yes			4K	4K	Y	11				2017	2017		empty design, no init file	tiny
p16	http://www.ultratechnolc		Don Golding	forth	16	5	kintex-7-3	James	bad syntax			6					14.7	0.67	1.0				vhdl	1	p16			N		64K	64K						2000				
p16b		beta	C. H. Ting	forth	16	5	kintex-7-3	James	case c	367		6			355	##	14.7	0.67	1.0	648.1	X		vhdl	1	cpu16	Y	asm	N		64K	64K		28				2000			part of eForth?	data width can be expanded
p24e		beta	C. H. Ting	forth	24	6	spartan_3	James	Brakef	1175		4		16	51	##	14.7	0.83	1.0	36.0	X		vhdl	1	p24c	Y	asm	N		2K	2K		28				2000			part of eForth?	data width can be expanded
rtx2000	http://www.mp	asic	Tom Hand	forth	16	16																	proprietary															Harris Corp., FPGA version at MPEforth	
s16x4a	https://github.c	stable	Samuel Falvo II	forth	16	4	kintex-7-3	James	Brakef	514		6			476	##	14.7	0.67	1.0	620.7	X	B	verilog	1	s16x4a	Y		N	N	64K	64K	Y	12				2012	2017		kestrel #2, byte & word data	derived from Myron Plichota's design (streame
s4pu	https://baioc.github.io/pc		Gabriel de Sant'Anna	forth	16	16	cyclone2	Gabriel	de Sa	3306	1622	4		86	50	##	q13.1	0.67	1.0	10.1	I		vhdl	17	s4pu	Y	asm	N		64K	64K		32				2017	2020	https://gitlab.com/baioc/s4pu		in Portuguese
s64x7	https://github.c	stable	Samuel Falvo II	forth	64	8																	verilog	4	s64x7					16E	16E	Y	56				2017			64-bit simple Forth engine	very little doc
sc20	http://www.forp	proprietar	Brad Eckert	forth	32	8	virtex-6	Brad Eckert		1977		6			150			1.00	1.0	75.9	X		proprietary														2010		PDF file, Forth Inc.	
ssbcc	https://opencor	stable	Rodney Sinclair	forth	8	9	kintex-7	Rodney	Sincla	196		6			474		14.7	0.33	1.0	797.9	ILX		verilog	3	core	Y	asm	N	Y	1K	8K	Y	41		3		2012	2014	https://github.cor	Python program generates the Verilo	inst after branch/call/rtn always execs
stack_machine	http://people.ec	stable	Bruce R. Land	forth	16	5	cyclone10	James	Brakef	5101		4	6	29	66	##	q18.0	0.67	0.3	25.9	X		verilog	9	VGA_stan	Y	asm	N	N	64K	4K	N					2009	2011	https://people.ec	(3) uP cores, Cornell course material	VGA output, uses Nakano's tiny_cpu
streamer16	http://www.ultr	stable	Myron Plichota	forth	16	3	kintex-7-3	James	Brakef	143		6			417	##	14.7	0.20	1.2	485.6	X		vhdl	8	streamer	Y	yes	N	N	64K	64K	N	8	2			2001	2001	http://www3.sym	MIPS/inst reduced	2nd web adr non-functional
x32	http://citeseerx.	stable	Sijmen Woutersen	forth	32	8	kintex-7-3	James	missing defines			6				##	14.7	1.00	1.0				vhdl	32	core	Y	yes	N		4G	4G	Y					2006	2007	https://pdfs.sema	MS thesis, byte code, needs caches	uses preprocessor on VHDL
xpu	http://excamera	macros	James Bowman	forth	16	8	kintex-7-3	James	requres preprocessor			6					14.7	0.67	1.0				vhdl	1	c2a												2003	2003		predates J1	uses preprocessor on VHDL
yafc	https://github.c	alpha	Tim Wawrzynczak	forth	16		kintex-7-3	James	Brakef	617		6		4	247	##	14.7	0.67	1.0	268.5	X		vhdl	20	cpu		asm	N	Y	8K	8K		26				2014				influenced by J1, F16 & C18
zpu	https://github.c	stable	Oyvind Harboe	forth	32	8	kintex-7-3	James	Brakef	1073		6	3		283	##	14.7	1.00	4.0	65.9	X		vhdl	23	zpu_core	Y	yes	N		4G	4G	Y	37				2008	2009		zpu4: 16 & 32 bit versions, code size 8	ZPU the worlds smallest 32 bit CPU with GCC t
zpuflex	https://github.c	mature	Alastair M. Robinson	forth	32	8	cyclone-3	Alasta	appro	1000		4											vhdl	4	zpu_core	Y	yes	N	N	4G	4G	Y	37				2014	2015	https://github.cor	addditional instrucitons	
zpuino	http://alvie.com	alpha	Alvaro Lopes	forth	32	8	spartan_6	James	Brakef	2547		6	4	12	126	##	14.7	1.00	4.0	12.3	X	Y	vhdl		papilio_pr	Y	yes	N		4G	4G	Y	37				2008	2012		SoC version of modified ZPU	pipelined, removed ucf file
flexgrip	http://www.ecs	paper	Kevin Andryc	GPGPU	32	32	atrix-7	James	Brakef	72649		6	156	119	100	##	14.7	1.00	0.1	11.0	X		vhdl	46	gpgpu_ml	505_top_level											2013	2016	http://www.ecs.u	eight GPU processors	requested & received source files
flexgripplus	https://github.c	mature	Josie Condia	GPGPU	32	32																	vhdl														2020	https://opencores	GPGPU based on G80 architecture of	NVIDIA, heavly based on flexgrip
nyuzi_gpu	https://github.c	stable	Jeff Bush	GPGPU	32	32	arria-2	James	syntax errors		A				####		18.0	1.00	1.0				system v	70	nyuzi	Y	yes							64		2015	2022		32 scalar & 32 vector reg	should run on either altera or xilinx
rfPhoenix	https://github.c	alpha	Robert Finch	GPGPU	32	40																	system v	83						4G	4G	Y						2022		gpgpu Under Construction, derived from	Nyuzi core by Jeff Bush
cpus-caddr	https://github.c	untested	Brad Parker	lisp	32	48																	verilog			Y	lisp		Y	16M	16K						2011	2016	https://dspace.mi	Verilog FPGA re-implementation of M	uses 48-bit u-code
igor	https://github.c	errors		lisp			kintex-7-3	James	missing files			6				##	14.7	0.33	1.0				vhdl	25	leval												2010	2010		IGOR - A microprogrammed LISP mac	two versions, spartan3 LUT4
lispmicrocontr	http://nyuzi.org	errors	Jeff Bush	lisp	32	32	kintex-7-3	James	missing init file			6				##	14.7	1.00	1.0				verilog	10	ulisp	Y		N												program.hex missing	
latticemico32	http://www.latt	stable	Yann Siommeau, Mich	LM32	32	32	arria_2	James	Brakef	2166		A	4	30	149	##	q13.1	0.80	1.0	55.0	LX		verilog	24	lm32_cpu	Y	yes	N	Y	4G	4G	Y			32	6	2006	2017	https://en.wikiped	optional data & inst caches	Diamond3.10; see lm32 & misoc folders
latticemico32	http://www.latt	stable	Yann Siommeau, Mich	LM32	32	32	ECP3	Lattice	Semic	2370		4	4	30	115			0.80	1.0	38.8	LX		verilog	24	lm32_cpu	Y	yes	N	Y	4G	4G	Y			32	6	2006	2017	https://en.wikiped	optional data & inst caches	Diamond3.10; see lm32 & misoc folders
lm32	https://github.c	mature	Sebastien Bourdeaudu	LM32	32	32																	verilog	24	lm32-top	Y	yes	N	Y	4G	4G	Y			32	6		2014		cleaned up lattice micro32, see milkymist	
milkymist	https://github.c	stable	Sebastien Bourdeaudu	LM32	32	32	spartan-6	James	failed	13531		6	31	78	50	##	14.7	0.80	1.0	3.0	X	Y	verilog	169	system	Y	yes	N	Y	4G	4G	Y			32	6	2007	2014		uses LM32, uses Spartan-6 IO	failed in mapper
t48	https://opencor	stable	Arnim Laeuger	MCS-48	8	8	cyclone-1	Arnim	Laeuge	738		4		1	59			0.33	4.0	6.6	IX		vhdl	70	t48_core	Y	asm	N		256	1K						2004	2022		T48 uController	used in several projects
brainfuckcpu	https://opencor	beta	Aleksander Kaminski	mem	8	3	kintex-7-3	James	Brakef	110		6			432	##	14.7	0.08	2.0	157.2	X		verilog	1	brainfuck_cpu			N	Y				8		0		2014	2015	http://www.cliffo	Touring machine like, 2ndary link is a	adj prog & data mem size, terrible name
verysimplecpu	https://github.com/MC2S		Abdullah Yıldız	mem	32	32																	verilog			Y	yes	N	N	16K	16K	N	8	2			2014	2019	https://github.cor	educational, 2 address, public version is	missing processor RTL
16bit_processo	https://github.com/prant		Md Badiuzzaman Pran	MIPS	16	16																	schematic														2018	2018	https://prantoam	course project, schematics only	simple up with well done schematics
32-bit_MIPS	https://sourcefo	beta	Cairo University	MIPS	32	32	**zu-3e**	James	very slow synthesis			6	1		100	##	v21.1	1.00	1.0				vhdl	18	mips_mod	Y	yes	N		4G	4G	Y			32		2011	2018		Cairo University EE dept	stopped run in synthesis
aor3000	https://opencor	beta	Aleksander Osman	MIPS	32	32	**zu-3e**	James	high F	4199	2520	6	4	8	175	##	v21.1	1.00	1.0	41.8	IX		verilog	19	aoR3000	Y	yes	N		4G	4G	Y			32	5	2014	2015		MIPS R3000A compatible, has MMU	moved declarations forward
aor3000	https://opencor	beta	Aleksander Osman	MIPS	32	32	kintex-7-3	James	Brakef	5307		6	4	9	129	##	14.7	1.00	1.0	24.2	IX		verilog	19	aoR3000	Y	yes	N		4G	4G	Y			32	5	2014	2015		MIPS R3000A compatible, has MMU	moved declarations forward
beri	https://www.cl	mature	Gregory Chadwick	MIPS	64	32																	bluespec	34	mipstop	Y	yes								32		2012	2017	https://github.cor	Bluespec Extensible RISC Implementa	CHERI (Capability Hardware Enhanced RISC Ins
cmips	https://github.c	mature	Roberto Hexsel	MIPS	32	32															I		vhdl	22	core	Y	yes	N	N	4G	4G	Y			32	5	2017	2019	http://www.inf.uf	5-stage pipeline, MIPS32r2 core	
digital_up	https://github.com/hneer		Helmut Neemann	mips	16	16	spartan7	James	clockir	716	309	6	1		182	##	v22.1	0.67	1.0	170.1	X		schemat	46	processorHD	asm	N	Y	64K	64K		60		16		2016	2022	https://github.cor	uP implemented as schematic	has assembler and ISA pdf, 2Kx16 RAM?
digital_up	https://github.com/hneer		Helmut Neemann	mips	16	16	zu-5e	James	clockir	709	310	6	1		250	##	v22.1	0.67	1.0	236.2	X		schemat	46	processorHD	asm	N	Y	64K	64K		60		16		2016	2022	https://github.cor	uP implemented as schematic	has assembler and ISA pdf, 2Kx16 RAM?
edge	https://opencor	alpha	Hesham ALMatary	MIPS	32	32	spartan-6	James	Brakef	5345		6	7	1	8	##	14.7	1.00	1.0	1.5	X		verilog	30	edge_core	Y	yes	N	N	4G	4G	Y			32	5	2014	2014		Edge Processor (MIPS)	MIPS1 clone
fpga4_mips_5p	http://www.fpg	errors	Van Loi Le	MIPS	32	32	kintex-7-3	James	degenerate design			6				##	14.7	1.00	1.0				verilog			Y	yes	N	N	4G	4G	Y			32	5	2017	2017		educational, full pipelined MIPS	incomplete
hf-risc	https://opencor	stable	Sergio Johann Filho	MIPS	32	32	kintex-7-3	James	Brakef	1446		6		4	115	##	14.7	1.00	1.0	79.2	X		vhdl	9	spartan3e_n	Y	yes	N	N	4G	4G	Y	41		32		2016		https://github.cor	MIPS I subset, no multiplier	
ion	https://opencor	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James	Brakef	1533		6			163	##	14.7	1.00	1.0	106.0	IX		vhdl	12	mips_soc	Y	yes	N		4G	4G	Y			32		2011	2018	https://github.cor	new version: moving to MIPS32r1	new version not ready, keeping old numbers
mais		stable	Rene Doss	MIPS	32	32	kintex-7-3	James	Brakef	2760		6	4	5	245	##	14.7	1.00	1.0	88.7	X		vhdl	22	MAIS_soc	Y	yes	N	N	4G	4G				32	5	2013		use MIPS tools	register forwarding around ALU	license req'd for commercial use
mangomips32	https://github.c	stable	Ricky Tino	MIPS	32	32												1.00	1.0				verilog	25		Y	yes	N		4G	4G	Y	100		32	5	2019	2019		cache support, runs linux	very percise specs
mips_cpu_blue	https://github.com/txstat		Michael Volling	mips	32	32																	myhdl	37	cpu	Y	yes	N		4G	4G	Y			32	5		2018		simplified MIPS CPU with pipelining,	MyHDL, classic pipeline diagram	
mips_fault_tol	https://opencor	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James	Brakef	2017		6	4	6	45	##	14.7	1.00	1.0	22.5	X		vhdl	40	main	Y	yes	N		4G	4G	Y			32	5	2013	2013		arithmetic includes fault detection	no external memory port?
mips_linder	https://www.sc	paper	Michael Linder	MIPS	32	32	kintex-7-3	James	Brakef	1100		6			238	##	14.7	1.00	1.0	216.5		B	vhdl	39	a_mips	Y	yes	N		4G	4G				32		2007	2007		masters thesis	no LUT RAM, source code in PDF
mips_pipelined	https://github.c	mature	Mohammad Hossein Y	MIPS	32	32																	verilog	23	toplevelcp	Y	yes	N		4G	4G				32	5	2017	2019		course project, hazard detection as well as	forwarding, limited ISA
mips_sc_rubio	http://www.ece	untested	Victor P. Rubio	MIPS	32	32																	vhdl		mips_sc	Y	yes			4G	4G						2004	2004		MIPS RISC Processor for Comp Arch Ed, 2004, single cycle, RTL in PDF	
mips_up_vhdl	https://github.com/cm42		Chandra Mettu	mips	32	32																	vhdl	10	NYU6463	Y	yes	N		4G	4G	Y			32			2020		simple MIPS with comparison to RC5	accellerator, NYU student
mips32	https://opencor	stable	Jin Jifang	MIPS	32	32	kintex-7-3	James	Brakef	3696		6		8	192	##	v17.4	1.00	1.0	52.0	X		verilog	17	pipelinem	Y	yes			4G	4G	y			32	5	2017			vivado project	"classic MIPS"
mips32r1	https://opencor	stable	Grant Ayers	MIPS	32	32	arria-2	James	Brakef	3716		A	8		79	##	q13.1	1.00	1.0	21.3	IX		verilog	20	processor	Y	yes	N	Y	4G	4G	Y			32	5	2012	2015	https://github.cor	Harvard arch	complete software tool chain
mips789	https://opencor	stable	Li Wei	MIPS	32	32	kintex-7-3	James	Brakef	1432		6		1	171	##	14.7	1.00	1.0	119.1	IX		verilog	10	mips_core	Y	yes	N		4G	4G	Y			32	5	2007	2014		supports most MIPSI instructions	

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chai n	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe lan	start year	last revis	secondary web link	note worthy	comments
mipscpu	https://github.com/mfbsc		Matheus Souza	MIPS	32	32																	system v	24	cpu	N				4G	4G					2017	2019		MIPS like cpu, course project, VHDL verilog & system verilog	
mips-cpu	https://github.c	alpha	Jeremiah Mahler	MIPS	32	32	kintex-7-3	James	added	596		6		1	244	##	14.7	1.00	1.0	409.2	X		verilog	15	cpu	Y	yes	N		4G	4G	Y			32	5	2017	2017		Very early stage project, only implem	no outputs, missing im_data.txt
mips-cpu2	https://github.c	untested	Yash Bhutwala	MIPS	32	32																	verilog			Y	yes	N		4G	4G	Y			32		2016	2017		Pipelined CPU, course project, actual design in fibinacci or helloWorld	
mipsfpga	https://www.mi	stable	MIPS Technologies	MIPS	32	32	atrix-7-3	James	Brakef	10692		6		47	118	##	14.7	1.00	1.0	11.0	X	Y	verilog	193	mfp_syste	Y	yes	N		4G	4G	Y			32		2014	2018	https://www.yout	M14K core & mipsfpga-plus	DRAM interface, I&D caches. 8789 FF
mips-hls-vivad	https://github.c	stable	Grammatopoulos Vasi	MIPS	32	32																	cpp		cpu	Y	yes	N		4G	4G	Y			32			2019		written in cpp, no inst decode, limited ISA	
mips-lite	https://github.c	untested	Jon Craton	MIPS	32	32	kintex-7-3	James	insufficient memory			6				##	14.7	1.00	1.0				vhdl	65	cpu		asm	N							32		2009	2009			
mipsr2000	https://opencor	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James	Brakef	1971		6	4	6	71	##	14.7	1.00	1.0	36.2	X		vhdl	35	Dm	Y	yes	N		4G	4G	Y			32	5	2012	2016		supports almost all instructions of mi	course project
octagon	https://opencor	beta	Jon Pry	MIPS	32	32	kintex-7-3	James	Brakef	3021		6	4	9	333	##	14.7	1.00	1.0	110.2	X		vhdl	46	octagon		asm			4G	4G	Y			32		2015	2015	https://github.cor	8 thread barrel processor, largely MIPS	compatible
plasma	https://opencor	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James	Brakef	2462		6		3	97	##	14.7	1.00	1.0	39.5	X		vhdl	22	plasma	Y	yes	N		4G	4G	Y			32		2001	2016	http://plasmacpu.	wide outside use, opencores page has	list of related publications
plasma_fpu	https://opencor	stable	Maximilian Reuter	MIPS	32	32	kintex-7-3	James	errors			6				##	14.7	1.00	1.0				vhdl	20	plasma	Y	yes	Y		4G	4G	Y			32		2015	2015		plasma with FPU	based on Plasma by Steve Rhoads
PSX_MiSTer	https://github.c	beta	MiSTer-devel	mips	32	32																	vhdl	120	sys_top	Y	yes			4G	4G	Y			32		2021	2022	https://en.wikiped	MiSTer version of original Playstation	VHDL, verilog & system verilog RTL
r4000		errors	Michael Povlin	MIPS	32	32	kintex-7-3	James	lots of problems			6				##	14.7	1.00	1.0				verilog														1994	1995		does not implement 64-bit data	only a few insts implemented, test vehicle
sardmips	https://opencor	systemC	Igor Loi	MIPS	32	32																	systemC			Y	yes	N		4G	4G	Y			32		2006	2009		synthesizable parametric IP core	supporting full MIPS R2000 ISA
single_cyc_mip	https://www.fpga4student.com/2017/01/verilog			MIPS	16	16																	verilog	2	single_cyc_mips					64K	64K							https://www.fpga4student.com/p/verilog-project.html		
single-cyc-cpu	https://github.c	mature	Victor A Pajaro	MIPS	32	32																	vhdl	30	AlvarezPajaro_sing	N				4G	4G	Y			32			2019		nice schematic and clear description,	course work
sweet32	https://opencor	alpha	Valentin Angelovski	MIPS	32	16	kintex-7-3	James	Brakef	1050		6	1		142	##	14.7	1.00	1.0	135.1	X	B	vhdl	2	Sweet32_	Y	yes	N	N	4G	4G	Y	26		16		2014	2015		targets MACHXO2, no RAM	
sweet32	https://opencor	alpha	Valentin Angelovski	MIPS	32	16	kintex-7-3	James	Brakef	1797		6	1	2	185	##	14.7	1.00	1.0	103.1	X	Y	vhdl	28	sweet32_	Y	yes	N	N	4G	4G	Y	26		16		2014	2015		targets MACHXO2, DDR RAM	clock divider to Sweet32_v1_core
sweet32	https://opencor	alpha	Valentin Angelovski	MIPS	32	16	kintex-7-3	James	Brakef	1177		6	1		116	##	14.7	1.00	1.0	98.8	X	B	vhdl	2	Sweet32_	Y	yes	N	N	4G	4G	Y	26		16		2014	2015		targets MACHXO2, no RAM	
ucore	https://opencor	stable	Whitewill	MIPS	32	32	kintex-7-3	James	Brakef	2469		6		1	231	##	14.7	1.00	1.0	93.5	X		verilog	25	ucore	Y	yes	N		4G	4G	Y			32	6	2005	2010		MMU & caches	
vhdl-cpu2	https://github.com/lebric		Fabrice Normandin	mips	32	32																						asm	N		4G	4G	Y	29		32	5		2018		McGill Un. Course, MIPS CPU/VHDL	MIPS inst card, pipe hazard notes
yacc	https://opencor	stable	Tak Sugawara	MIPS	32	32	kintex-7-3	James	map e	2220		6	6			##	14.7	1.00	1.0		IX		verilog	10	yacc2	Y	yes	N		4G	4G	Y			32	5	2005	2009		derived from, but independent of pla	YACC Yet Another CPU CPU
yari	https://github.c	stable	Tommy Thorn	MIPS	32	32	kintex-7-3	James	Brakef	3610		6		15	189	##	14.7	1.00	1.0	52.3	X	Y	verilog	8	top					2M	2M				32		2004	2008		subset of MIPS R3000	
ztapchip	https://github.c	stable	Vuony Nguyen	MIPS	32	32	cyclone-5	James	Brakef	31331		A	43	578	100	##	q18.0	1.00	1.0	3.2	I	Y	vhdl	53	ztachip												2015	2015		multi-core with MIPS master	files no longer available, was under developme
ztapchip	https://github.c	stable	Vuony Nguyen	MIPS	32	32											q18.0	1.00	1.0		IX	Y	vhdl	53	ztachip												2015	2022		vexriscv uP, AXI crossbar	Intel & Xilinx support, runs tensor flow
m1_core	https://opencor	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	arria-2	James	Brakef	2101		A			190	##	q13.1	1.00	1.0	90.6	IX		verilog	9	m1_core		yes	N		4G	4G	Y			32		2007	2012		GCC target?	
dragonfly	http://www.leo	beta	LEOX team	MISC	16	16	kintex-7-3	James	Brakef	788		6			164	##	14.7	0.67	1.0	139.3	X		vhdl	6	dgf_core	Y		N		256	2K						2001			unusual, uses FIFOs	
fpgammix	https://github.c	stable	Tommy Thorn	MMIX	64	32	arria-2	James	Brakef	11605		A	8	10	94	##	q13.1	1.50	4.0	3.0	I		system v	3	core	Y	yes	Y	Y	16Q	16Q	Y	256		288		2006	2014	https://en.wikiped	clone of Knuth's MMIX	micro-coded
msp430_vhdl	https://opencor	beta	Peter Szabo	MSP430	16	16	kintex-7-3	James	Brakef	1735		6			127	##	14.7	0.67	2.0	24.5	IX		vhdl	9	cpu	Y	yes	N		64K	64K	Y			16		2014	2017		Comprehensive verification was not	compiles on cyclone II
neo430	https://opencor	alpha	Stephan Nolting	MSP430	16	16	virtex-6	Stephan	Nolt	402		6		2	204	##	14.7	0.67	8.0	42.5	IX		vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2021	https://github.cor	website has detailed resource utiliza	minimal configuration
neo430	https://opencor	alpha	Stephan Nolting	MSP430	16	16	artiix-7	James	chang	947		6		2	203	##	14.7	0.67	8.0	17.9	IX	Y	vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2021	https://github.cor	edit neo430_sysconfig.vhd to set opti	~8+ clocks for R-R inst
neo430	https://opencor	alpha	Stephan Nolting	MSP430	16	16	cyclone-4	Stephan	Nolt	626		6		2	117	##	14.7	0.67	8.0	15.7	IX		vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2021	https://github.cor	**website has detailed resource unt**	minimal configuration
openmsp430	https://opencor	stable	Oliver Girard	MSP430	16	16	stratix-3-4	Oliver	Girard	1147		A	1		98			0.67	2.0	28.5	IX		verilog	30	openMSP	Y	yes	N	N	64K	64K	Y			16		2009	2018		near cycle accurate	performance spreadsheet
s430	https://www.p-c	stable	Paul Taylor	MSP430	16	16	artix-7	Paul	Taylor	449		6			100			0.67	9.0	16.6			vhdl	1	s430					64K	64K	Y					2019	2019		msp430 subset with 8-bit alu	coded for size & not for speed
vhdl-msp430	https://github.c	mature	Rafael Hideo Toyomot	MSP430	16	16																	vhdl	15	processad	Y	yes	N		64K	64K	N	27		16		2018	2018		course project, inspired by msp430,	very little commentary
m32632	https://opencor	stable	Udo Moeller	N32032	32	8	kintex-7-3	James	Brakef	10167		6	19	16	83	##	14.7	1.00	1.0	8.2	IX		verilog	18	example	Y	yes	Y	Y	4G	4G	Y	200		24	3	2009	2019	http://cpu-ns32k.net/		21.97 VAX Mips at 50MHz (Cyclone IV)
nios2		proprietar	Altera	Nios II	32	32	stratix-3	Altera	consis	1020		A			290	##	q13.1	0.90	1.0	255.9	I		proprietary			Y	yes	opt		4G	4G	Y			32		2004			fltg-pt, caches & MMU options	Nios II/f: fastest version, DMIPS adj, 2.15 Core
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera	consis	584		A			420	##	q16.0	0.10	1.0	71.9	I		proprietary			Y	yes	opt		4G	4G	Y			32		2004			fltg-pt, caches & MMU options	Nios II/e: min LUTs version, DMIPS adj, 1.68 Co
niosprocessor	https://github.com/Julien		Julien Malka	Nios II	32	32																	vhdl	25	cpu	Y	yes	N		4G	4G	Y			32		2019	2019		Project for Computer Architecture co	uses much Altera source code
recon	https://github.com/jefflie		jeff lieu	Nios II	32	32																	verilog			Y	yes	opt		4G	4G	Y			32			2019	https://hackaday.c	NIOS helper files	software helper files also
softpc	https://github.com/alreac		Michael S	Nios II	32	32	cyclone-1	Micha	block	613		4		1	180		q17.1	1.00	5.0	58.9			vhdl	13	nios2ee	Y	yes	opt		4G	4G	Y			32			2019		nine variations in attempt to improve	16-bit ALU
nova-soc	https://github.com/scottl		Scott Baker	nova	16	16	**zu-3e**	James	no mem init file			6				##	v21.2	0.67	2.0			Y	vhdl	14	soc	Y	yes	N		64K	64K				7		2016	2020		Nova CPU + RAM + UART + Timer + I/O Ports, Sierra Circuit Dsgn, missing hex file	
altor32	https://opencor	stable	Ultra Embedded	OpenRISC	32	32	kintex-7-3	James	Brakef	2505		6		5	192	##	14.7	1.00	1.0	76.8	ILX		verilog	16	altor32	Y	yes	N	Y	4G	4G	Y					2012	2015	https://openrisc.io	simplified OpenRISC 1000	xilinx S3 primitives
altor32_lite	https://opencor	stable	Ultra Embedded	OpenRISC	32	32	kintex-7-3	James	Brakef	1928		6			236	##	14.7	1.00	2.0	61.3	ILX		verilog	7	altor32	Y	yes	N	Y	4G	4G	Y					2012	2014	https://openrisc.io	simplified OpenRISC 1000, no pipeline	xilinx S3 primitives
minsoc	https://opencor	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James	Brakef	4945		6	4	8	107	##	14.7	1.00	1.0	21.7	ILX	Y	verilog	88	or1200_tc	Y	yes	Y	M	4G	4G	Y			32		2009	2013	https://github.cor	minimal OR1200, vendor neutral, has	caches
mor1kx	https://github.c	stable	Julius Baxter	OpenRISC	32	32	kintex-7-3	James	Brakef	2718		6	3	3	217	##	14.7	1.00	1.0	80.0	X		verilog	48	mor1kx	Y	yes	N		4G	4G	Y			32		2012	2021	https://www.yout	lots of configuration parameters	considered best openrisc design
or1200	https://github.c	stable	Damjan Lampret	OpenRISC	32	32	kintex-7-3	James	Brakef	5231		6	4	8	118	##	14.7	1.00	1.0	22.5	X		verilog	78	or1200_tc	Y	yes	Y	M	4G	4G	Y			32		2010	2015	https://openrisc.io	best older openrisc implementation	no LUT RAM for reg file
or1200_hp	https://opencor	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauc	3 slot	5602		6			185	##		1.00	1.0	33.1	X		verilog	39	or1200_ic	Y	yes	Y	M	4G	4G	Y			32		2010	2013	https://openrisc.io	3 slot barrel version of OR1200	numbers from published paper
or1200_soc	https://opencor	beta	gaz	OpenRISC	32	32	cyclone-2	James	missing files			4				##	q11.1	0.67	2.0			Y	verilog	39	top	Y	yes	Y	M	4G	4G	Y			32		2011	2015	https://openrisc.io	OpenRISC on Terasic DE1 board	
or1200mp	https://github.c	stable	Stefan Wallentowitz	OpenRISC	32	32	kintex-7-3	James	Brakef	4960		6	4	8	111	##	14.7	1.00	1.0	22.4	X		verilog	104	or1200_tc	Y	yes	Y	M	4G	4G	Y			32		2012	2012	https://openrisc.io	multiprocessor variant, single core	
or1k	https://github.c	stable	Julius Baxter, Stefan Ky	OpenRISC	32	32	kintex-7-3	James	Brakef	3299		6	3	3	189	##	14.7	1.00	1.0	57.3	IX		verilog	39	mor1kx	Y	yes	N	M	4G	4G	Y			32		2001	2018	https://opencores	no longer supported, see mor1kx	cappuccino ALU
or1k_soc	https://opencor	mature	Xianfeng Zeng	OpenRISC	32	32	arria-2	James	syntax errors			6				##	q18.0	1.00	1.0		I	Y	verilog	194	or1k_soc_	Y	yes			4G	4G	Y			32		2009	2010	https://openrisc.io	SoC using OpenRISC 1200	huge tar file
or1k-cf	https://opencor	alpha	Kenr	OpenRISC	32	32																	confluence														2004	2009			
fpg1	https://github.com/hrvac		Hrvoje Čavrak	PDP1	18	18																Y	verilog	31	cpu	Y	yes	N		4K	4K						2019		video display of PDP-1 console, a mister	core, retro gaming
pdp1	https://opencor	alpha	Yann Vernier	PDP1	18	18	spartan-3	James	Brakef	1390		4		6	138	##	14.7	0.50	10.0	5.0	X		vhdl	15	top	Y	yes	N	N	4K	4K	Y	28				2011	2017	http://pdp-1.com/	PDP-1 descended from MIT TX-0	uses Minimal UART from opencores
ks10	http://www.tec	stable	Rob Doyle	PDP10	36	36	spartan-6	Rob	Doyle	4427		6		15	50	##	14.7	1.00	2.0	5.6	X		verilog	39	esm_ks10	Y	yes	Y	N			N					2011	2014		36-bit accum & 18-bit adrs	ucf file, most tests pass
cpu11	https://github.c	untested	1801BM1	PDP11	16	16																	verilog			Y	yes		N	64K	64K	Y	70	13	8		2014	2020		2 versions, PDP-11 uP reverse engine	USSR uP, no DEC prototype, proprietary die de
cpus-pdp11	https://github.c	untested	Brad Parker	PDP11	16	16																	verilog			Y	yes		N	64K	64K	Y			8		2006	2016		A working PDP-11 cpu with an RK11 disk	emulator which uses a IDE disk as a backing
pdp11_reduce	https://github.com/mhon		Mohamed Omran	PDP11	16	16																	vhdl	9	system	Y	yes	N	N	64K	64K		24	10	8		2021			simplified pdp11, 24 inst	no byte data size, ucode, 2-12 clocks/inst
pdp11-34verilo	www.heeltoe.co	stable	Brad Parker	PDP11	16	16	arria-2	James	Brakef	2532		A			126	##	q13.1	0.67	2.0	16.7	IX	Y	verilog	24	pdp11	Y	yes	N	N	64K	64K		70	13	8		2009			boots & runs RT-11, EIS inst & MMU	
pdp11-soc	https://github.com/scottl		Scott Baker	pdp11	16	16	**zu-3e**	James	no mem init file			6				##	v21.2	0.67	3.0			Y	vhdl	15	soc	Y	yes	N	N	64K	64K		70	13	8		2016	2020		PDP-11/20 CPU + RAM + UART + Timer + I/O Ports, Sierra Circuit Design now open so	
pdp2011	http://pdp2011.	stable	Sytse van Slooten	PDP11	16	16	kintex-7-3	James	Brakef	5060		6	1		205	##	14.7	0.67	2.0	13.6	IX	Y	vhdl	3	cpu	Y	yes	Y	N	64K	64K		70	13	8		2008	2019	http://pdp2011.sy	SoC, build files for A&X boards	complete impl including orig IO devices
pop11-40	http://www.ip-s	simulatior	Naohiko Shimizu	PDP11	16	16	ep1K	Naohiko	Shim	2687		4			20	##		0.67	2.0	2.5	I		NSL	17	top	Y	yes		N	64K	64K	Y	70	13	8		2009		www.ip-arch.jp/in	Boots UNIX	
w11	https://opencor	alpha	Walter Mueller	PDP11	16	16	kintex-7-3	James	Brakef	1760		6	1	1	147	##	14.7	0.67	2.0	28.0	X	Y	vhdl	118	pdp11_co	Y	yes	N	N	4M	4M	Y	70	13	8		2010	2022	https://github.cor	Boots UNIX, has MMU & cache, retro	PDP-11/70 CPU core and SoC
pdp6	https://github.com/Morri		Michael Morris	PDP6	36	36																	verilog	16	pdp6	Y				256K	256K						2018	2018	https://en.wikiped	ISA identical to PDP-10	PDP-10 was much more successful
cpus-pdp8	https://github.c	untested	Brad Parker	PDP8	12	12	spartan-3	James	Brakef	1557		4		1		##	14.7	0.40	2.0		X	Y	verilog	15	top	Y	yes	N	N	4K	4K						2004	2016		A working PDP-8/i cpu with an RF08	disk emulator which uses a IDE disk as a backing
pdp8	https://opencor	alpha	Joe Manojlovick, Rob	PDP8	12	12	kintex-7-3	James	Brakef	1219		6	1		183	##	14.7	0.50	2.0	37.5	X	Y	vhdl	55	cpu	Y	yes	N	N	32K	32K				8		2012	2016		PDP-8 Processor Core and System	Boots OS/8, runs apps, several variants
pdp8l	https://opencor	beta	Ian Schofield	PDP8	12	12	cyclone-3	James	Brakef	1088		4		48	63	##	q13.1	0.50	2.0	14.4	I		vhdl	11	top	Y	yes	N	N	4K	4K						2013	2013		Minimal PDP8/L implementation with	4K disk monitor system
pdp8-soc	https://github.com/scottl		Scott Baker	PDP8	12	12	**zu-3e**	James	no mem init file			6				##	v21.2	0.40	2.0			Y	vhdl	15	soc	Y	yes	N	N	4K	4K						2016	2020		Implemented for the Lattice iCE40-hx	PDP-8 CPU + RAM + UART + Timer + I/O Ports
pdp8verilog	www.heeltoe.co	stable	Brad Parker	PDP8	12	12	kintex-7-3	James	Brakef	505		6			366	##	14.7	0.50	2.0	181.3	X		verilog	18	pdp8	Y	yes	N	N	32K	32K				8		2005	2010		boots & runs TSS/8 & Basic	
pdp-8x	https://github.com/meng		Mats Engstrom	PDP8	12	12																	schematic			Y	yes	N	N	4K	4K							2019		Digital schematic, TTL	
socdp8	https://github.c	beta	Folke Will	PDP8	12	12																	vhdl	34	socdp8_p	Y	yes	N	N	32K	32K				8		2019	2019		SoC implementation of a PDP-8/I for t	includes extended ALU
synpic12		stable	Miguel Angel Ajo Pelay	PIC12	8	12	kintex-7-3	James	Brakef	474		6		1	197	##	14.7	0.33	1.0	136.8	IX		vhdl	7	synpic12	Y	yes	N	N	256	2K	Y					2011	2011	http://projects.nb	CHDL to verilog	bad weblink
altium/TSK165	http://techdocs.p	roprietar	Altium	PIC16	8	12	spartan-3	Altium		416		4			50			0.33	2.0	19.8	AILX		proprietary			Y	yes	N	Y	256	4K	Y					2004	2017	CR0140.pdf, CR01	frozen, asm, C, C++, schem, VHDL & V	default clock speed is 50MHz
cqpic	http://www002	stable	Sumio Morioka	PIC16	8	14	arria-2	James	ROM parameter errors			A				##	q13.1	0.67	1.0		I		vhdl & v	5	CQPIC	Y	yes	N	Y	256	4K	Y					1999	2004		LPM macros	
free_risc8	https://web.arc	stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James	Brakef	355		6			142	##	14.7	0.33	1.0	132.2	X		verilog	8	cpu	Y	yes	N		256	4K	Y					2002	2011	https://web.archive.org/web/20120309123835/http://www.mindspring.com/~tcoonan/index.html		
m16c5x	https://opencor	mature	Michael Morris	PIC16	8	14	spartan-3	Michael	Morr	1217		4		3	60	##		0.33	1.0	16.3	X	Y	verilog	3	m16C5x	Y	yes	N	Y	256	4K	Y					2013	2014		SOC LUT count	
m16c5x	https://github.com/Morri		Michael Morris	PIC16	8	12	kintex-7-3	James	std library problems			6				##	14.7	0.33	2.0				verilog	32	m16c5x	Y	yes	N	Y	256	4K	Y					1998	2018		pipelined and non-pipelined versions	
minirisc	https://opencor	stable	Rudolf Usselmann	PIC16	8	14	spartan-3	Rudolf	Usseln	460		4			80			0.33	1.0	57.4	X		verilog	7	risc_core	Y	yes	N	Y	256	4K	Y					2001	2012			
p16c5x	https://opencor	mature	Michael Morris	PIC16	8	14	kintex-7-3	James	Brakef	378		6			252	##	14.7	0.33	1.0	220.2	IX		verilog	3	P16C5x	Y	yes	N	Y	256	4K	Y					2013	2014			
pic_coonan		alpha	Tom Coonan	PIC16	8	14	kintex-7-3	James	Brakef	328		6		1	165	##	14.7	0.33	1.0	166.1	X		verilog	7	piccpu	Y	yes	N	Y	256	4K	Y					1999				risc8 by Tom Coonan also a PIC uP
pic-16c5x	https://tams-ww	errors	Ernesto Romani	PIC16	8	12	kintex-7-3	James	std library problems			6				##	14.7	0.33	2.0				vhdl	16	pic_core	Y	yes	N	Y	256	4K	Y					1998	2002			as part of thesis?
ppx16	https://opencor	stable	Daniel Wallner	PIC16	8	14	kintex-7-3	James	missin	409		6			238	##	14.7	0.33	1.0	192.1	X		vhdl	10	P16C55	Y	yes	N	Y	256	4K	Y					2002	2009		both 16C55 & 16F84	with fake instruction ROM

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	toolchai n	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe lan	start year	last revis	secondary web link	note worthy	comments
recore54		beta	Hans Tiggeler	PIC16	8	14	kintex-7-3	James	Cannot find <rcore_pk			6					14.7	0.33	1.0				vhdl	20	rcore54_s	Y	yes	N	Y	256	4K	Y					1999			not available at ht-lab website	www.ht-lab.com
risc16f84	https://opencor	stable	John Clayton	PIC16	8	14	kintex-7-3	James	Brakef	375		6			392	##	14.7	0.33	2.0	172.5	IX		verilog	1	risc16f84	Y	yes	N	Y	256	4K	Y					2002	2018		derived from CQPIC by Sumio Moriok	other variants with RTL
risc5x	https://opencor	stable	MikeJ	PIC16	8	14	kintex-7-3	James	RLOC constraint errors			6					14.7	0.33	1.0				vhdl	15	cpu	Y	yes	N	Y	256	4K	Y					2002	2011		makes extensive use of xilinx primitives	
risc8	https://web.arc	stable	Tom Coonan	PIC16	8	12	kintex-7-3	James	Brakef	355		6			154	##	14.7	0.33	2.0	71.5	X		verilog	8	cpu	Y	yes	N	Y	256	2K	Y					1999	1999	https://github.cor	excellent HTML doc	directory contains derivative design by anothe
ae18	https://opencor	beta	Shawn Tan	PIC18	8	16	arria-2	James	Brakef	1084		A	1		207	##	q13.1	0.33	1.0	63.1	ILX		verilog	1	ae18_core		yes	N	Y	4K	1M						2003	2009	https://hackaday.i	not 100% compatable	negative edge reset "clock"
ae18	https://opencor	beta	Shawn Tan	PIC18	8	16	**zu-3e**	James	vivado	954	501	6			208	##	v21.1	0.33	1.0	72.1	ILX		verilog	1	ae18_core		yes	N	Y	4K	1M						2003	2009	https://hackaday.i	not 100% compatable	negative edge reset "clock"
mcip_open	https://opencor	beta	Mezzah Jbrahim	PIC18	16	24	kintex-7-3	James	Brakef	881		6	1		200	##	14.7	0.67	1.0	152.1	X		vhdl	23	MCIOopen_r		yes	N	Y	4K	1M	Y					2014	2015		light version of PIC18	
copyblaze	https://opencor	stable	Abdallah Ellbrahimi	picoBlaze	8	18	kintex-7-3	James	missin	622		6			217	##	14.7	0.33	2.0	57.5	IX		vhdl	16	cp_copybl	Y	asm	N		256	2K	Y					2011	2016		wishbone extras	
dapzipi8	https://github.com/ehsan		Ehsan Ali	picoBlaze	8	18	zu-5e	Ehsan	conve	305	49	6		2	224	##	v22.1	0.33	1.0	242.4	X		vhdl	20	top	Y	asm	N		256	2K	Y						2022		Deterministic Branch Prediction for R	also zipi8 starting point, PhD thessis
nanoblaze	https://opencor	beta	Francois Corthay	picoBlaze	8	18	kintex-7-3	James	punctuation			6				##	14.7	0.33	2.0		X		vhdl	12	nanoblaze		asm			256	2K	Y					2015	2015		nanoBlaze compatable, adjustable data width	
nanoblaze	https://opencor	beta	Francois Corthay	picoBlaze	8	18	kintex-7-3	James	Brakef	247		6		1	169	##	14.7	0.33	2.0	113.2	X		vhdl	12	nanoblaze		asm			256	2K	Y					2015	2015		nanoBlaze compatable, adjustable data width	
pacoBlaze	www.bleyer.org	mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo	Kocik	177		4		1	117			0.33	2.0	109.1	X		verilog	18	pacoblaze	Y	asm	N		256	2K	Y	57		2		2006			3 versions, behavioral coding	
pauloblaze	https://github.c	mature	Paul Genssler	picoBlaze	8	18																	vhdl	7	pauloBlaz	Y	asm	N		256	2K	Y					2015	2021		LUT6 req'd, course project, slower more	LUTs than original claims easier to modify a
picoblaze	https://www.xil	stable	Ken Chapman	picoBlaze	8	18	kintex-7-3	James	Brakef	110		6		2	217	##	14.7	0.33	2.0	325.5	X		vhdl	1	kcspm6	Y	asm	N		256	2K	Y					2003		https://en.wikiped	2 clocks/inst, no prog ROM	this is the original picoBlaze author
picoblaze	https://www.xil	stable	Ken Chapman	picoBlaze	8	18	spartan-3	James	Brakef	178		4		1	182	##	14.7	0.33	2.0	168.9	X		vhdl	1	kcspm3	Y	asm	N		256	2K	Y					2003		https://en.wikiped	2 clocks/inst, no prog ROM	this is the original picoBlaze author
picoblaze	https://www.xil	stable	Ken Chapman	picoBlaze	8	18	kintex-7-3	James	Brakef	317		6		2	195	##	14.7	0.33	2.0	101.6	X	Y	vhdl	19	kc705_kcp	Y	asm	N		256	2K	Y					2003		https://en.wikiped	2 clocks/inst	this is the original picoBlaze author
riscuva1	https://opencor	stable	S. de Pablo	picoBlaze	8	14	kintex-7-3	James	Brakef	109		6			370	##	14.7	0.33	2.0	560.7	X		verilog	1	riscuva1	bme		N	Y	256	1K	Y	35				2006	2006	https://github.cor	Verilog source included in PDF file	also VHDL version by Bikash Gogoi with identic
wb4pb	https://opencor	stable	Stefan Fischer	picoBlaze	13	13	kintex-7-3	James	incomplete port to kcp			6				##	14.7	0.33	3.0			Y	vhdl or v	14	picoblaze_wb_uart				Y							2010	2013	https://en.wikiped	software addon for picoBlazeSoftwar	ported to kcpsm6
wb4pb	https://opencor	stable	Stefan Fischer	picoBlaze	13	13	spartan-3	Stefan	Fische	309		4		1	102	##	14.7	0.33	3.0	36.2	X	Y	vhdl or v	14	picoblaze_wb_uart				Y							2010	2013	https://en.wikiped	software addon for picoBlazeSoftwar	kcpsm3 only works for Spartan 3
microwatt	https://github.c	beta	anton blanchard	PPC	32	32															X		vhdl	37	toplevel	Y	yes			4G	4G	Y					2019	2022	https://openpowe	open source PPC from IBM	supports microPython, beta stage
power_a2	https://github.com/openg		IBM (open PPC)	PPC	64	32	vu3p-2		TCL files														vhdl	285		Y	yes	Y		16E	16E	Y		32		2019	2020		PPC RTL, asic gate RTL	Virtex VU3P-2 FPGA implementation (380K luts
Lutiac		custom	David Galloway, David	reg	16	NA	stratix-4	David	Gallow	140		A	4		198			0.67	1.0	947.6	I		vhdl & verilog								64	N	64		32	3		2010	Talks at Un. Toron	synthesis maps PC into ucode	no inst mem: small state machine, ~200 inst o
octavo	http://fpgacpu.c	beta	Charles LaForest	reg	16	16	stratix-4	Charles	LaFor	500		A	1		550			0.67	1.0	737.0	I		verilog	18	Octavo	Y	asm	N					14		16	10	2012	2019	https://github.cor	8 core barrel, adjustable data width	~= performance across word sizes, no call/rtn i
16bitcpu	https://github.c	simulatio	Winston Van	risc	16	16																	vhdl	19	top	Y		N		1K	1K	N	16				2020			Custom 16 bit CPU and datapath in VHDL	inspired by RISC-V
24bit_up	https://github.c	alpha	Harshal Mittal	RISC	24	24	**zu-3e**	James	area o	3535	2166	6	1		187	##	v21.1	0.80	1.0	42.2	X		verilog	17	processor			N		16M	16M	N	17		32		2019	2019		basic 24-bit RISC, course work	big Dff count, multiple writes to register file
8bit_piped_pro	https://opencor	stable	Mahesh Sukhdeo Palv	RISC	8	16	kintex-7-3	James	swapp	1049		6		1	370	##	14.7	0.33	1.0	116.4	X		verilog	28	top	Y							20		16		2013	2017	https://github.cor	uses Perl as assembler	use Perl to generate ROM file
8bit_piped_pro	https://opencor	stable	Mahesh Sukhdeo Palv	RISC	8	16	**zu-3e**	James	vivado	1500	1822	6		1	500	##	v21.1	0.33	1.0	110.0	X		verilog	28	top	Y							20		16		2013	2017	https://github.cor	uses Perl as assembler	use Perl to generate ROM file
a_tiny_up	https://www.quora.com/		Simon Moore, Frankie	RISC	32	32	arria-5	James	tiny LL	35		A				##	q18.0	0.67	1.0				system v	1	TinyComp	Y	asm	N	Y	1K	1K	N	13		128		2007	2011	https://www.cl.ca	from Thacker's version, Un Cambridge course	
a_tiny_up	https://www.qu	errors	Chuck Thacker	RISC	32	32	**zu-3e**	James	missing files			6				##	v20.1	0.67	1.0				verilog	1	TinyComp	Y	asm	N	Y	1K	1K	N	13		128		2007	2007	https://www.cl.ca	104 lines of verilog, Thacker (wikipedia)	deceased
a2z	https://hackada	errors		RISC	16	24	kintex-7-3	James	replace Altera RAM wit			6					14.7	0.67	1.0		I		verilog														2016	2018		runs on Cyclone IV	
a2z	https://hackada	errors		RISC	16	24	**zu-2e**	James	area opt			6				##	v20.1	0.67	1.0		I		verilog														2016	2018		runs on Cyclone IV	
a2z	https://hackada	stable		RISC	16	24	cyclone-4	James	Brakef	1524		4	1	12	62	##	q17.0	0.67	1.0	27.4	I		verilog		top_a2z												2016	2018			
aap	https://github.c	stable	Simon Cook	RISC	16	16	arria-2	James	Brakef	7193		A			393	##	q18.0	0.67	1.0	36.6	I		verilog	7	de0_nano	Y	yes		Y	64K	16M	Y			64		2015	2016	http://www.embe	includes Altera project	4 to 64 reg, 24-bit pc, no status reg
aap	https://github.c	stable	Simon Cook	RISC	16	16	cyclone-4	James	Brakef	10630		4			306	##	q18.0	0.67	1.0	19.3	I		verilog	7	de0_nano	Y	yes		Y	64K	16M	Y			64		2015	2016	http://www.embe	includes Altera project	4 to 64 reg, 24-bit pc, no status reg
aizup/aizup_m	instruct1.cit.cor	stable	Yamin Li, Wanming Ch	RISC	8	16	arria-2	James	Brakef	121		A			298	##	q13.1	0.17	2.0	205.4	IX		vhdl	1	cpu			N	N	64K	64K		16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
aizup/aizup_ov	instruct1.cit.cor	stable	Yamin Li, Wanming Ch	RISC	8	16	kintex-7-3	James	Brakef	138		6			318	##	14.7	0.17	3.0	128.3	IX		vhdl	1	cpu		asm	N	N	64K	64K	Y	16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
aizup/aizup_pi	instruct1.cit.cor	stable	Yamin Li, Wanming Ch	RISC	8	16	kintex-7-3	James	Brakef	198		6			375	##	14.7	0.17	2.0	157.9	IX		vhdl	1	cpu		asm	N	N	64K	64K	Y	16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
aizup/aizup_se	instruct1.cit.cor	stable	Yamin Li, Wanming Ch	RISC	8	16	kintex-7-3	James	Brakef	136		6			313	##	14.7	0.17	8.0	48.1	IX		vhdl	1	cpu		asm	N	N	64K	64K	Y	16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
altium/TSK3000	http://techdocs	proprietar	Altium	RISC	32	32	spartan-3	Altium		2426		4		4	50			1.00	1.0	20.6	AILX		proprietary				yes	N	N	4G	4G	Y					2004	2017	CR0140.pdf, http:/	frozen, asm, C, C++, schem, VHDL & V	default clock: 50MHz, opt mult/div
alwcpu	https://opencor	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James	Brakef	377		6			194	##	14.7	0.67	1.0	345.5	ILX		vhdl	7	top	bme		N	N	64K	64K	Y			16		2009	2010		lightweight CPU	maximal features
any-1	https://github.c	defined	Robert Finch	RISC	64	36	**zu-3e**	James	errors							##	v21.1	2.00	1.0		X		system v	83	any1base	Y		Y					128		64		2021	2021	http://anycpu.org	Cray-1 like with full set of vector instr	three versions with different ISAs, inst sz, reg s
artemis	https://github.c	simulatio	Sudharshan Sundaram	RISC	16	16	**zu-3e**	James	incomplete source code							##	v21.1	1.00	1.0				verilog	9	main_test	Y	asm	N				N	18		8		2018	2020	https://www.yout	simple, educational uP with decent vi	vivado project
atlas_2K	https://opencor	beta	Stephan Nolting	RISC	16	16	**zu-3e**	James	vivado	1222	1160	6	1	5	262	##	v21.1	0.80	1.0	171.4	ILX		vhdl	19	ATLAS_2K	Y	asm	N	Y	64K	64K	M	80		8		2013	2015		ARM thumb like inst set	has MMU & full SOC features
atlas_2K	https://opencor	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James	Brakef	1595		6	1	5	151	##	14.7	0.80	1.0	75.9	ILX		vhdl	19	ATLAS_2K	Y	asm	N	Y	64K	64K	M	80		8		2013	2015		ARM thumb like inst set	has MMU & full SOC features
atlas_core	https://opencor	beta	Stephan Nolting	RISC	16	16	**zu-3e**	James	vivado	611	285	6	1		333	##	v21.1	0.80	1.0	436.4	IX		vhdl	8	ATLAS_CP	Y	asm	N	Y	64K	64K	Y	80		8		2013	2015		ARM thumb like inst set	non-MMU version
atlas_core	https://opencor	beta	Stephan Nolting	RISC	16	16	kintex-7-3	James	Brakef	559		6	1		200	##	v14.1	0.80	1.0	286.2	IX		vhdl	8	ATLAS_CP	Y	asm	N	Y	64K	64K	Y	80		8		2013	2015		ARM thumb like inst set	non-MMU version
babyrisc	http://www.san	stable	John Rible	RISC	8	16	kintex-7-3	James	Brakef	468		6			141	##	14.7	0.33	2.0	49.7	X		verilog	1	qs5_mix	Y		N		64K	64K	Y	15		8		1997	1999	http://www.sandp	part of a three class course	memory rd/wt & ALU per clock
babyrisc	http://www.san	stable	John Rible	RISC	8	16	**zu-3e**	James	vivado	249		6			286	##	v21.1	0.33	2.0	189.3	X		verilog	1	qs5_mix	Y		N		64K	64K	Y	15		8		1997	1999	http://www.sandp	part of a three class course	memory rd/wt & ALU per clock
basic-cpu	https://embedd	stable	Justin Rajewski	RISC	8	16	**zu-3e**	James	syntax errors			6				##	v21.1	0.33	2.0				verilog	1									16				2018	2018		16 inst, scrapped web page, 98 lines of verilog, no call/rtn, bare core, excellent exam
basic-simd-up	https://github.com/zslwyu		Tingyuan Liang	risc	16	18																	verilog	5	cputop	Y		N	Y	1K	1K		47		8		2018	2022		simple SIMD processor in Verilog	compiled via Cadence to ASIC layout
bjx1	https://github.c	alpha	Brendan Bohannon	RISC	32	16	kintex-7-3	James	syntax errors			6				##	14.7	1.00	2.0				verilog	34	exunit	Y		Y	N	4G	4G	Y		9	16		2017	2018		128-bit memory path	based on SH-4, work suspended
bst-cpu	https://github.c	stable	Yichun Ma	RISC	32	32	kintex-7-3	James	altera primitives			6				##	14.7	1.00	1.0		I		verilog		sc_computer					4G	4G				32		2016	2016		learning, pipeline uP	
bst-cpu	https://github.c	stable	Yichun Ma	RISC	32	32	arria-2	James	Brakef	1439		A		2	58	##	q18.0	1.00	1.0	40.2	I		verilog	26	sc_computer			N		4G	4G				32		2016	2016		learning, single cycle uP	
c16too	https://www.sc	stable	Cole Design and Devel	RISC	16	16	kintex-7-3	James	Brakef	510		6			271	##	14.7	0.67	4.0	88.9	X		vhdl	1	core	Y	asm	N		64K	64K	N	20		8		2003		coledd.com/electr	graphics capability	clock/2 and six phases
cast_ba22	http://www.cas	proprietar	CAST Inc	RISC	32	16	spartan-6	CAST	Inc	1800		6		32	72			1.00	1.0	40.0	X		proprietary				yes			4G	4G				32				http://www.cast-i	Cast has uP related IP	several versions, FPGA kits
chip8	https://bitbucke	errors	Carsten Elton Sørense	RISC	8		kintex-7-3	James	missing modules							##	14.7						verilog	28	chip8	Y		N								2013	2018	https://en.wikiped	Verilog implementation of the SuperC	https://www.zophar.net/pdroms/chip8/chip-8
c-nit	http://www.c-n	stable	Sumit	RISC	16	16	spartan-3	James	xilinx l	752		4		3	100	##	14.7	0.67	2.0	44.5	X		verilog	6	soc	om	asm	N	N	64K	64K	Y	22		15		2003	2004		RISC with several load/store modes	
coen_316_cpu	https://github.c	alpha	G.K Yvann Monny	RISC	32	32	kintex-7-3	James	does r	897		6			127	##	14.7	1.00	3.0	47.0	X		vhdl	8	cpu_dp			N		32	32	N	20		32		2018	2018		MIPS based, simulation DO files, I&D	very small caches do not infer any RAM
cole_c16	https://www.sc	beta	Cole Design & Develop	RISC	16	16	spartan-6	James	Brakef	554		6			298	##	14.7	0.67	7.0	51.4	X		vhdl	1	core	Y	asm	N		64K	64K	N	20		8		2002	2012	https://blog.classy	(7) clks per inst, complete SOC	
cowgirl	https://opencor	errors	Thebeekeeper	RISC	16	16	kintex-7-3	James	incomplete source cod			6					14.7	0.67	1.0				vhdl	14	cowgirl					64K					8		2006	2009		incomplete source code	
cpu_takagi	https://github.c	untested	Masayuki Takagi	RISC	16	16																	verilog	3	cpu								16				2016	2016			
cpu-16	https://opencores.org/pr		Yvo Zoer	RISC	16	16												0.67	3.0		I		verilog	5	cpu16			N	N	64K	64K	N	32		8		2019	2021		no LUT RAM, uses block RAM	Altera register file
cpugen	https://opencor	stable	Giovanni Ferrante	RISC	32	16	kintex-7-3	James	Brakef	474		6			192	##	14.7	0.67	1.0	271.8	IX		vhdl	14	cpu	Y	asm	N	N								2003	2009		x86 .exe generates VHDL RISC uP	using 16 bit example
cpugen	https://opencor	stable	Giovanni Ferrante	RISC	32	16	kintex-7-3	James	Brakef	1597		6	8		154	##	14.7	1.00	1.0	96.3	IX		vhdl	14	cpuc	Y	asm	N	N								2003	2009		x86 .exe generates VHDL RISC uP	using 32 bit example
crisv32_axis_et	http://develope	asic	Axis Communications	RISC	32	16																Y	proprietary				yes			4G	4G	Y			16			2007	http://developer.a	embedded comm	very dated product
dcpu16	https://github.c	beta	Shawn Tan, Marcus Pe	RISC	16	16	kintex-7-3	James	Brakef	662		6	1		318	##	14.7	0.67	4.0	80.4	X		vhdl & v	5	dcpu16_c	Y	asm	N	N	64K	64K	N	37		8		2009	2012	https://en.wikiped	for the 0X10c game	4+ addressing modes, 4 & 5-bit reg /modefield
dgb16	see FISA64	stable	Robert Finch	RISC	16	16	kintex-7-3	James	Brakef	780		6			313	##	14.7	0.67	1.0	269.0	X		verilog	1	dbg16	Y		N	Y						8				https://github.cor	inside FISA64 project	debug uP for fisa64
diogenes	https://opencor	beta	Fekknhifer	RISC	16	16	kintex-7-3	James	Brakef	807		6		1	297	##	14.7	0.67	1.0	246.3	X		vhdl	11	cpu	Y	asm	N			1K						2008	2009		"student RISC system"	
dme	https://github.c	stable	ErwinM	RISC	16	16	kintex-7-3	James	Brakef	1755		6			53	##	14.7	0.67	1.0	20.4	X		verilog	49	cpu	Y	yes	N		64K	64K	Y	40		8		2016	2017		based on magic-16	computer & computer2 null dsgns: no outputs
dp32		errors	Peter Ashenden	RISC	32	32	kintex-7-3	James	errors			6				##	14.7	1.00	1.0				vhdl												32		2001	2001	book, CDROM	from The Designers Guide to VHDL	timing delays in source code
eco32	https://opencor	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James	Brakef	2339		6		1	160	##	14.7	1.00	1.5	45.5	ILX	Y	verilog	14	cpu	Y	yes	N		512M	256M	Y	61		32		2003	2014	homepages.thm.d	MIPS like, slow mul & div	
eco32	https://opencor	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James	Brakef	3367		6		5	147	##	14.7	1.00	1.5	29.1	ILX	Y	verilog	24	eco32	Y	yes	N		512M	256M	Y	61		32		2003	2014	homepages.thm.d	MIPS like, slow mul & div	
eco32f	https://github.c	stable	Stefan Kristiansson	RISC	32	32	kintex-7-3	James	Brakef	3845		6	3	4	123	##	14.7	1.00	1.0	32.1	X		verilog	12	eco32f	Y	yes	N		512M	256M	Y	61		32	6	2014	2014		pipelined version of the eco32 CPU	cache & mmu
eight_bit_uc		stable	Synplicity	RISC	8	12	kintex-7-3	James	signal/variable mixup			6					14.7	0.67	1.0				vhdl	10	eight_bit_uc						2K	Y			32		2000	2000		part of Amplify documentation	
ejrh_cpu	https://github.c	stable	Edmund Horner	RISC	16	16	kintex-7-3	James	Brakef	928		6	1	2	196	##	14.7	0.67	1.0	141.6	X		verilog	17	machine	Y									16		2015	2015		see web archive for doc	
erp	https://opencor	stable	Shahzadjk	RISC	8	16	spartan-3	James	Brakef	366		4	1	1	70	##	14.7	0.33	1.0	63.5	X		verilog	1	ERPverilog	Y							15		6		2004	2014		two report PDFs & one Verilog file	
fisa32	https://github.c	beta	Robert Finch	RISC	32	32	kintex-7-3	James	Brakef	3479		6	3	2	152	##	14.7	1.00	1.0	43.7	X		verilog	1	FISA32	Y		N	Y						32		2014	2014	https://github.com/robfinch/Cores		
fisa64	https://github.c	beta	Robert Finch	RISC	64	32	kintex-7-3	James	Brakef	10404		6	12	7	65	##	14.7	1.50	1.0	9.4	X		verilog	1	FISA64	Y		N	Y								2015	2015	https://github.com/robfinch/Cores	need to use multi-cycle on mult	
fisc	https://github.c	stable	Miguel Santos	RISC	64	32	cyclone-4	James	Brakef	5036		4		21	66	##	q18.0	2.00	1.0	26.1	I		system v	13	fisc_core	Y	yes	Y	N			Y	85	6	32	5	2018	2018	http://www.archf	Flexible Instruction Set Computer	caches, VHDL & System Verilog versions, altera
fisc	https://github.c	stable	Miguel Santos	RISC	64	32	arria-2	James	errors			A				##	q18.0	2.00	1.0				vhdl	21		Y	yes	Y	N			Y	85	6	32	5	2018	2018	http://www.archf	Flexible Instruction Set Computer	caches, VHDL & System Verilog versions, altera
fluid_core	https://opencor	alpha	Azmathmoosa	RISC	8	12	kintex-7-3	James	Brakef	956		4			381	##	14.7	0.33	1.0	131.7	X		verilog	17	FluidCore			N	Y								2015	2015		data width adj., mem sizes adj.	
fpag4_risc16_1	http://www.fpg	errors	Van Loi Le	RISC	16	16	kintex-7-3	James	degenerate design			6				##	14.7	0.66	1.0				verilog	15	Risc_16_b	Y			N	Y	64K	64K		13	4	16		2017	2017		similar to mips16_16_1cycl	incomplete Risc_16_bit module

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	toolchai n	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe line	start year	last revis	secondary web link	note worthy	comments
fpga4_mips16	http://www.fpg	stable	Van Loi Le	RISC	16	16	kintex-7-3	James Brakef		369		6			200	##	14.7	0.67	1.0	363.1	X		verilog	8	mips_16			N		65K	65K		13		8		2017	2017		educational, no block RAM inferred	same prog & data mem and alu as mips16_16
fpga4_mips16	http://www.fpg	stable	Van Loi Le	RISC	16	16	kintex-7-3	James Brakef		352		6			213	##	14.7	0.67	1.0	405.0	X		vhdl	8	mips_vhdl			N		65K	65K		8		8		2017	2017		educational, no block RAM inferred	actual prog sz=16, actual data mem sz=256
fpgacomputer	https://github.c	errors	Milan Vidakovic	RISC	16	8	arria-2	James	errors			A				##	q18.0	0.67	4.0			Y	verilog	10	computer	Y	asm	N	N	64K	64K	Y	25		8		2018	2018	https://mvidakovi	16-bit CPU, 64KB, UART (115200 bps), and VGA	
fpgacomputer	https://github.c	errors	Milan Vidakovic	RISC	16	8	kintex-7-3	James	erros			6				##	14.7	0.67	4.0			Y	verilog	10	computer	Y	asm	N	N	64K	64K	Y	25		8		2018	2018	https://mvidakovi	16-bit CPU, 64KB, UART (115200 bps), and VGA	
ft64	https://github.c	alpha	Robert Finch	RISC	64	32																	verilog		FT64v3b	Y	yes	Y		16E	16E	Y					2017	2018	https://www.ama	4th attempt at 64-bit core (raptor64,	amazon kindle book, L1 & L2 icaches & L1 dcac
gaia	https://github.com/nyuicl		Yuichi Nishiwaki	risc	32	32															X		vhdl	31	top	Y	yes	Y		4G	4G	Y					2015	https://hackaday.(	ray-tracing in OCaml, custom CPU, co	many VHDL record types
gbox16-gpu	https://github.c	ncomplet	engineersbox	risc	16	16															X		schematic		gpu												2022		Digital schematic, based on NVIDIA and AMD uarch	
gumnut	http://digitaldes	stable	Peter Ashenden	RISC	8	18	kintex-7-3	James Brakef		388		6			259	##	14.7	0.33	1.0	220.7	IX		verilog	6	gumnut-rt	Y	asm	N	Y	256	4K	Y			8		2007			see Digital Design: An Embedded Systems Approach Using VHDL	
harvard_arch_	https://github.com/omard		omarelhedaby	RISC	32	32																	vhdl	135	harvard_pro		asm	N	Y								2021			many source files
hicovec	https://opencor	beta	Harald Manske, Gunde	RISC	32	32	kintex-7-3	James	compiler errors			6					14.7	1.00	1.0				vhdl	28	cpu	Y	asm	N				Y					2008	2010		hybrid scalar & vector processor	
hpc-16	https://opencor	beta	Umair Siddiqui	RISC	16	16	kintex-7-3	James Brakef		871		6			152	##	14.7	0.67	1.0	116.6	X		vhdl	20	cpu	Y	asm	N		64K	64K				16		2005	2015			
ice_mk2	https://gitlab.co	alpha	Mario Hoffmann	RISC	16	16																	verilog	8	top	Y		N		4K	4K	N	16		16		2020	2020	https://hackaday.io/project/174049-ice-cpu-mk-ii	variant of fpga4student	
iDEA	https://github.c	alpha	Hui Yan Cheah etal	RISC	16	32	virtex-6	Liu Ch	unable	321		6	1	2	405		13.2	0.67	1.0	845.3	X		verilog	22	cpu_top	Y	yes	N	Y	64K	64K	N	24		32	9	2011	2016	The iDEA DSP Blo	uses DSP slice in barrel mode for ALU	from GitHub, rq'd NOPs lower actual results
iitb-proc	https://github.com/preet		Preetam Pinnada	RISC	16	16																	vhdl	17	iitb_proc			N									2020		course project for EE224 @EE.IITB, fo	very little doc, sizeable state machine	
iop16b	https://github.c	alpha	Doug Gilliland	RISC	8	16																Y	vhdl	51	cpu_top	Y	asm	N		4K	4K	Y	11		8		2021	2022	https://hackaday.i	I/O Processor with minimal instructio	full set of perpherals
jam	https://github.c	stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James Brakef		1396		6			159	##	14.7	1.00	1.0	113.7	X		vhdl	17	cpu_sys	Y		N	Y	128K	128K				32	5	2002	2014		serial multiply & divide	took out clock divider
jam	https://github.c	stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James Brakef		1369		6			143	##	14.7	1.00	1.0	104.2	X		vhdl	17	cpu	Y		N	Y	128K	128K				32	5	2002	2014		serial multiply & divide	
jane_nn		stable	Suresh Devanathan	RISC	4	8	kintex-7-3	James Brakef		723		6			178	##	14.7	0.33	1.0	81.4	X		vhdl	3	Processor	Y							27		16		2002			neural network microprocessor, spec	ialized registers
jca		stable	John Cronin	RISC	8	32	kintex-7-3	James	replac	3287		6	3	3	157	##	14.7	0.33	1.0	15.8	IX	Y	verilog	17	soc										16					has VGA controller, plays Pong	altera memories
jimmy	https://github.com/kuash		Eduardo Corpeño	RISC	8	8															IX		verilog	2	jimmy	Y		N	Y	256	256	Y	16		4		2020		educational, 4 regs, 8-bit adr spaces	vendor neutral source code
jpu16	https://github.c	stable	Joksan Alvarado	RISC	16	26	kintex-7-3	James	missing RAM files			6					14.7	0.67	1.0				vhdl	9	JPU16	Y	asm	N		64K	64K				16		2012			32 deep call stack, 8 addressing modes	
kgp-risc	https://github.com/kranti		Kiran & Aluru	RISC	32	32																	verilog			Y		N		4G	4G						2018	2020		only two register fields + shift amount	
klc32	https://opencor	planning	Robert Finch	RISC	32	32	kintex-7-3	James Brakef		3790		6	4	1	200	##	14.7	1.00	4.0	13.2	X		verilog	25	KLC32	Y		N		4G	4G	Y			32		2011	2012	https://github.cor	single ported block RAM register file :(	heavy use of includes
kpu	https://github.c	alpha	Andrea Corallo	RISC	32	32	kintex-7-3	James	missin	6178		6	3		19	##	14.7	1.00	1.0	3.0	X	Y	verilog	19	kpu	Y	yes	N	Y	4G	4G				32		2016	2018	http://andreacora	KPU is a minimal system on chip writte	n used as testbench for the KPU core
kraken16	https://people.e	stable	Bruce R. Land	RISC	18	18	kintex-7-3	James Brakef		281		6		1	278	##	14.7	0.67	1.0	662.3	X		verilog	1	DE2_TOP	Y	asm	N	N	256	256	N	22		16			2008	https://people.ec	Cornell course material	
latticemico8	http://www.latt	stable	Lattice Semiconductor	RISC	8	18	LFE2	Lattice	Semic	265		4		1	104			0.33	2.0	64.4	ILX		vhdl	10	isp8_core	Y	yes	N		256	4K	Y			32		2005	2010	https://en.wikipe	16 deep call stack, four configuration	tool kit: LMS for Diamond3.10
lc-3	https://github.com/Sacus		Sudhanshu Gupta	RISC	16	16																	vhdl			Y	asm	N		64K	64K	Y	16		8		2017	https://en.wikipe	from book: 978-0072467505 by Patt &	apndx has schematic
limen	https://github.com/domir		Dominik Salvet	RISC	16	16																	vhdl	12	core	Y		N	Y	64K	64K	N	20		8		2018	2021		teenager, highschool thesis	
lion	https://github.com/lliont/		Theodoulos Liontakis	RISC	16																	I	Y	vhdl	7	lionsysten	Y	yes	N		64K	64K	Y			8		2015	2019	https://hackaday.i	custom gaming CPU, mem segments	software in C#, has BASIC
lion	https://github.com/lliont/		Theodoulos Liontakis	RISC	16																	I	Y	vhdl	7	lionsysten	Y	yes	N		64K	64K	Y			8		2015	2021	http://users.sch.g	custom gaming CPU, mem segments	new directory, same RTL, Mister project
lion	https://github.com/lliont/		Theodoulos Liontakis	RISC	32																	I	Y	vhdl	7	lionsysten	Y	yes	N		1M	1M	Y			8		2015	2022	http://users.sch.g	custom gaming CPU, Altera BDF files	new 32-bit version, Mister project
lxp32	https://opencor	beta	Alex Kuznetsov	RISC	32	32	kintex-7-3	James Brakef		850		6	3	1	196	##	14.7	1.00	2.0	115.4	AIX		vhdl	20	lxp32u_to	Y	asm	N	N	4G	4G	Y	30		256	3	2016	2022	https://lxp32.gith	register file in block RAM	vendor neutral source code, no div inst
lxp32	https://opencor	beta	Alex Kuznetsov	RISC	32	32	**zu-3e**	James Brakef		948		6	4	2	250	##	v21.1	1.00	2.0	131.9	AIX		vhdl	20	lxp32u_to	Y	asm	N	N	4G	4G	Y	30		256	3	2016	2022	https://lxp32.gith	register file in block RAM	vendor neutral source code, no div inst
manik	https://www.ds	stable	Sandeeo Dytta	RISC	32	32	kintex-7-3	James	needs editing to suppo			6					14.7	0.33	1.0				vhdl	45	manik2to	Y	yes	N		4K	4K	Y			16		2002	2006	www.niktech.com	optional data & inst caches	supports Xilinx, Altera, Actel, Lattice; broken w
marca	https://opencor	stable	Wolfgang Puffitsch	RISC	16	16	arria-2	James Brakef		1763		A		22	157	##	q13.1	0.67	6.0	10.0	I		vhdl	40	marca	Y		N		8K	16K		75		16	4	2007	2009		serial multiply & divide	clks/inst is approx
mark_ii	https://github.com/Vladis		Vladislav Mlejnecký	risc	32	32															I	Y	vhdl		mark_ii	Y	yes	Y		16M	16M	N			16		2017	2018		system on chip written in VHDL	custom PCB with MAX10
mera400f	https://github.com/jakubi		jakubfi	risc	16	16																	verilog	77	mera400f	Y	yes	N		64K	64K	Y						2020		reimplementation of MERA-400 CPU,	Polish, Mera400 was TTL uP	
micro_nating	https://github.c	mature	Geoff Natin	RISC	16	16																	vhdl	56	processor_final			N	N	64K	64K	N	10		9		2016	2016		microcoded instruction set processor,	educational
minimips	https://opencor	stable	Samuel Hangouet	RISC	32	32	kintex-7-3	James Brakef		2939		6	8		118	##	14.7	1.00	1.0	40.1	X		vhdl	12	minimips	Y	yes	N	N	4G	4G				32	5	2004	2018		based on MIPS I	
minimips_supe	https://opencor	alpha	Miguel Cafruni	RISC	32	32												1.00	0.5				vhdl	18	minimips	Y	asm	N	N	4G	4G				32	5	2017	2018		based on MIPS I	dual issue to two pipes, 16-bit mulitplier
mips_16	https://opencor	stable	Doyya Doyya	RISC	16	16	kintex-7-3	James	collapsed in compile			6					14.7	1.00	1.0				verilog	12	mips_16	Y		N		64K	64K		13		8	5	2012	2013		Educational 16-bit MIPS Processor	
misoc	https://github.c	stable	M-Labs	RISC	32	32	arria_2		python source code run thru migen							##	q13.1	0.80	1.0		ILX		V*HDL			Y	yes	N		4G	4G	Y			32		2007	2019	https://m-labs.hk	Video IP for Mist & others	choice of latticemicro32 or mor1kx uP
mist1032	https://github.c	stable	Takahiro Ito	RISC	32	32	arria_2	James	altera	10801		A	4	125	98	##	q18.0	1.00	1.0	9.1			system v	50	mist32e1(	Y				4G	4G	Y			64			2014		mist32 uP: embedded version	
mist1032	https://github.c	errors	Takahiro Ito	RISC	32	32	arria_2	James	altera mem			A				##	q18.0	1.00	1.0				verilog	87	mist1032sa					4G	4G	Y			64			2014		mist32 uP: out of order version	missing cache_ram_16entry_512bit.v
mist1032	https://github.c	errors	Takahiro Ito	RISC	32	32	cyclone-1	James	altera	33251		4	4	138	32	##	q18.0	1.00	1.0	1.0			verilog	100	mist1032isa					4G	4G	Y			64			2015		mist32 uP: inorder version	high pin count
moncky	https://gitlab.com/big-bat		Kris Demuynck	RISC	16	16	artix-7	Kris Demuyn		1376		6		33	10	##	v21	0.67	1.0	4.9	X	X	schemat	36	top	Y	yes	N		64K	64K	N	32		16		2020	2021	https://hackaday.(	intended as educational, all original	iO: VGA, PS/2, SPI, SD
moncky	https://gitlab.com/big-bat		Kris Demuynck	RISC	16	16	**zu-3e**	James	no me	768	280	6			250	##	v21.1	0.67	1.0	218.1	X	X	schemat	36	Moncky3	Y	yes	N		64K	64K	N	32		16		2020	2021	https://hackaday.(	bare CPU	also has verilog
moncky	https://gitlab.com/big-bat		Kris Demuynck	RISC	16	16	**zu-3e**	James	clock (	1196	523	6		33	78	##	v21.1	0.67	1.0	43.8	X	X	schemat	36	top	Y	yes	N		64K	64K	N	32		16		2020	2021	https://hackaday.(	from 16x65K to 64KB RAM	two phase clock, ALU & mem have own phase
moxie	https://github.c	stable	Anthony Green	RISC	32	32	arria-2	James	missing module			A				##	q18.0	1.00	1.0				verilog	16	moxie					4G	4G	Y			16		2009	2017	https://github.com/atgreen/moxie-cores	four read, two write register file missing	
moxielite	https://github.c	stable	Anthony Green	RISC	32	32	kintex-7-3	James Brakef		3159		6	3		152	##	14.7	1.00	1.0	48.0	X		vhdl	11	moxielite_wb					4G	4G	Y			16		2009	2017	https://github.com/atgreen/moxie-cores		
moxielite	https://github.c	stable	Anthony Green	RISC	32	32	arria-2	James Brakef		2696		A	4		93	##	q18.0	1.00	1.0	34.6	X		vhdl	11	moxielite					4G	4G	Y			16		2009	2017	https://github.com/atgreen/moxie-cores		
mrisc32	https://github.c	alpha	Marcus Geelnard	RISC	32	32																	vhdl	36	mc1	Y	asm	Y		4G	4G	Y	68		32		2018	2021	https://www.bitsr	Mostly harmless Reduced Instruction	Cray-1 vector inst, also a1 variant, LLVM suppo
mrisc32	https://github.c	alpha	Marcus Geelnard	RISC	32	32																Y	vhdl	36	mc1	Y	asm	Y		4G	4G	Y	68		32		2018	2021	https://www.bitsr	MC1 variant web page	logic that can output a 1920×1080@60 video
multicycle_risc	https://github.c	stable	Yash Sanjay Bhalgat	RISC	16	16	kintex-7-3	James Brakef		1470		6			213	##	14.7	0.67	1.0	97.0	X		verilog	62	risc15	Y		N		64K	64K		15		8		2015	2015		multi-cycle IIT-B-RISC15 ISA	developed on Altera, course project
multi-cycle-cpu	https://github.com/Amrik		Amrik Sadhra	RISC	32	32																	vhdl	48	top_level	Y				4G	4G	Y	21		32		2016	2016	https://www.yout	nicely documented with state diagran	spreadsheet for test programs, ISE project
myproc	https://github.c	alpha	A. Raamakrishnan	RISC	32	32																	verilog					N		4G	4G				32			2017		uP for educational purposes: myproc1(single cycle), myproc2 (pipelined)	
myrisc1		stable	Muza Byte	RISC	8	8	arria-2	James Brakef		121		A		2	231	##	q13.1	0.33	1.0	628.7	I		verilog	1	myRISC1	Y		N	Y	256	256	Y	16		4		2011	2011	https://en.wikipe	Verilog source included in PDF file	AKA Mano Machine, LPM macros
myrisc1	https://github.c	stable	Susam Pal	RISC	8	8												0.33	1.0		I		vhdl	5	microproc	Y		N	Y	256	256	Y	16		4		2005	2016	https://en.wikipe	one of several implementations	AKA Mano Machine, LPM macros
natalius_8bit_	https://opencor	beta	Fabio Guzman	RISC	8	16	kintex-7-3	James Brakef		232		6		1	175	##	14.7	0.11	3.0	27.7	X		verilog	12	natalius_p	Y	asm	N	Y	256	2K	Y	29		8		2012	2012		return stack & register file	3 clocks/inst
niloofar1	http://ce.sharif.	errors	Mahdi Amiri	RISC	16	16	kintex-7-3	James	ran out of memory			6				##	14.7	0.67	1.0				verilog	3	nf1	Y													derived from risc-16	ASIC, uses Leonardo for synthesis
nocpu	https://github.c	beta	John Tzonevrakis	RISC	8	8	kintex-7-3	James Brakef		175		6			243	##	14.7	0.33	1.5	306.1	X		verilog	5	cpu	N	no	N		256	256	Y			4					minimal & complete	8 ALU inst, 3 port reg file
oberon_sdram	http://projectob	beta	Nicolae Dumitrache	RISC	32	32	kintex-7-3	James Brakef		2103		6		1	104	##	14.7	1.00	1.0	49.5	X		verilog	16	risc5	Y	yes	Y		4G	4G				16		2013	2017		minimalist Wirth, part of Project Obe	modified to use DRAM, serial mult
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	cyclone-5	James	too big	130160		A	288	462		##	q18.0	4.00	0.3		I		system v	27	CoreQuad	Y	asm	Y		4G	4G				16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	stratix-5	Dmytro Senya		32978		A	72	112	192	##	q17.1	4.00	1.0	23.3	I		system v	27	CoreOneV	Y	asm	Y		4G	4G				16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	stratix-5	Dmytro Senya		148078		A	72	122	184	##	q17.1	4.00	0.3	19.9	I		system v	27	CoreQuad	Y	asm	Y		4G	4G				16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	stratix-5	Dmytro Senya		50814		A	72	112	180	##	q17.1	4.00	1.0	14.1	I		system v	27	CoreOneV	Y	asm	Y		4G	4G				16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	cyclone-5	James	reduce	35984		A	72	112	103	##	q18.0	4.00	1.0	11.4	I		system v	27	CoreOneV	Y	asm	Y		4G	4G				16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	cyclone-5	James	slow t	50135		A	72	112	90	##	q18.0	4.00	1.0	7.2	I		system v	27	CoreOneV	Y	asm	Y		4G	4G				16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
oldland-cpu	https://jamieiles.	errors	Jamie Iles	RISC	32	32	arria-2	James	syntax errors			A				##	q18.0	1.00	1.0		I		verilog	22	oldland_c	Y		N	N	4G	4G	Y			16	5	2015	2017	https://github.cor	has caches & MMU	runs on Cyclone V
oldland-cpu	http://jamieiles.	errors	Jamie Iles	RISC	32	32	arria-2	James	syntax errors			A				##	q18.0	1.00	1.0		I	Y	verilog	32	keynsham	Y		N	N	4G	4G	Y			16	5	2015	2017	https://github.cor	has caches & MMU	runs on Cyclone V
opa	https://github.c	stable	Wesley W. Terpstra	RISC	32	32	cyclone-5	Wesle	largest	8540		A			125		q15.0	1.00	0.5	29.3	I		vhdl												32		2013	2016		An Out-of-Order Superscalar Soft CPU	tested, incomplete
opc.opc5cpu	https://github.c	stable	revaldinho	RISC	16	16	kintex-7-3	James	reduce	273		6			294	##	14.7	0.40	3.0	143.6	X		verilog	7	opc5cpu	Y	asm	N	N	64K	64K	N	15	4	16		2017	2019	https://revaldinho	OPC5 RR inst, ISA similar to OPC1	see hackaday One Page Computing Challenge
opc.opc5lscpu	https://github.c	stable	revaldinho	RISC	16	16	kintex-7-3	James Brakef		383		6			247	##	14.7	0.67	3.0	144.0	X		verilog	2	opc5lscpu	Y	asm	N	N	64K	64K	N	18	4	16		2017	2019	https://revaldinho	OPC5LS OPC5 with predicate inst	see hackaday One Page Computing Challenge
opc.opc6cpu	https://github.c	stable	revaldinho	RISC	16	16	kintex-7-3	James Brakef		450		6			222	##	14.7	0.67	2.0	165.4	X		verilog	2	opc6cpu	Y	asm	N	N	64K	64K	N	27	4	16		2017	2019	https://revaldinho	OPC6 based on OPC5LS, more inst	see hackaday One Page Computing Challenge
opc.opc7cpu	https://github.c	stable	revaldinho	RISC	32	16	kintex-7-3	James Brakef		624		6			303	##	14.7	1.00	2.0	242.8	X		verilog	2	opc7cpu	Y	asm	N	N	1M	1M	N	32	5	16		2017	2019	https://revaldinho	OPC7 32bit, based on OPC5LS, more i	see hackaday One Page Computing Challenge
opc.opc8cpu	https://github.c	beta	revaldinho	RISC	24	24	kintex-7-3	James	no tes	516		6			323	##	14.7	0.80	2.0	250.1	X		verilog	1	opc8cpu	Y	asm	N	N	16M	16M	N	32	4	16		2017	2019	https://revaldinho	OPC8 24bit, based on OPC5LS, more i	see hackaday One Page Computing Challenge
open8_urisc	https://opencor	stable	Kirk Hays, Jshamlet	RISC	8	8	kintex-7-3	James Brakef		691		6	1		263	##	14.7	0.33	1.0	125.6	X		vhdl	9	Open8	Y	yes	N		64K	64K	Y			8		2006	2021		accum & 8 regs, clone of Vautomation	uRISC processor, in use
or1k_marocch	https://github.c	stable	Andrey Bacherov	RISC	32	32																	verilog			Y	yes	Y		4G	4G	Y			32		2012	2019	https://github.cor	continous regression tests	Implements a variant of Tomasulo algorithm
pasc	https://github.c	untested	Jeff Bush	RISC	16	16																	verilog			Y		N		64K	64K	N	20	2	8		2017	2019	https://github.cor	16 RISC cores	
patmos	https://github.c	stable	Martin Schoeberl	RISC	32	32																	scala														2015	2022	http://patmos.cor	university project, ASIC tapeout	http://www.t-crest.org/
pet-on-a-chip	https://github.com/ept22		Ezra Thomas	RISC	8	16												0.67	2.0			Y	verilog	19	top	Y	asm	N	Y	64K	64K	Y	40	5	8	2	2021	2021	https://ezrasrobot	robot controller, senior design projec	cust pcb & uP, derivative of tiny_soc
piropiro	https://github.c	stable	pandora2000	RISC	32	32	kintex-7-3	James	port m	7491		6	11	1	118	##	14.7	1.00	1.0	15.7	X		vhdl	42	top			Y	N	64K	64K	Y			32		2010	2011		five variants	no doc, xilinx constraint file

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	toolchai n	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe lin	start year	last revis	secondary web link	note worthy	comments
plasma_cortex	https://github.com/Nucle		Dylan Brophy	RISC	32	16						6						1.00	1.0		X		vhdl	4	cpu	Y	yes	N		4G	4G	Y			8		2018	https://hackaday.io/project/160180-plasma-cortex-open-source-cpu-in-vhdl		
processor-core	https://github.c	untested	Steven Hua	RISC	32	32																	vhdl			Y		N	N	4G	4G		16		32		2018	2018		clean, simple, prob classwork	Quartus proj, basic RISC instructions
propeller	https://propelle	proprietar	Chip Gracey	RISC	32	32																	verilog							4G	4G				512	5	2014	2020	https://github.cor	original propeller has verilog (FPGA) s	ISA: op/ddd/sss format with predication
propeller_p8x3	https://www.pa	stable	Chip Gracey	RISC	32	32	kintex-7-3	James	Brakef	9498		6		20	160	##	14.7	1.00	0.1	134.8	X		verilog	9	top	Y	yes									2014			eight propellers, clocking from ucf file	several FPGA card build files
qnice-fpga	https://qnice-fp	stable	Bernd Ulmann	RISC	16	16																Y	vhdl	40	quince_cp	Y	yes	N	N	64K	64K	N	18	4	16		2020	https://github.cor	derived from NICE: http://www.vaxm	PDP11-like, no byte operations
qrisc32	https://opencor	alpha	Viacheslav	RISC	32	32	arria-2	James	Brakef	3075		A	4		144	##	q13.1	1.00	1.0	46.9	I		system v	8	qrisc32	Y	yes	N		4G	4G	Y			32	4	2010	2011		qrisc32 wishbone compatible risc cor	for PhD thesis
qs5-rible	http://www.san	stable	John Rible	RISC	8	16	kintex-7-3	James	Brakef	468		6			135	##	14.7	0.33	1.0	95.3	X		verilog	1	qs5_mix			N		256	32K	Y					1998	1999		used in his class, also uses eP32	
r32v2020	https://github.com/dougg		Doug Gilliland	risc																																2021			huge download, canceled
r8-core	https://github.com/vctroj		Victor O. Costa	RISC	16	16																Y	vhdl	14	r8_uc	Y	asm	N		64K	64K	N	35		16		2019		university project, doc in portuguese	expanded R8 ISA
raptor64	https://opencor	alpha	Robert Finch	RISC	64	32																	verilog	63	raptor64	Y		Y	Y	4G	4G	Y	105	2	96	9	2005	2013		16 register sets, inst & data cache, m	ISA not finished, core runs
rcpu	https://github.com/redfas		redfast00	risc	8	16															L		verilog	5	rcpu	Y	yes	N		4K	4K	Y			6		2019	https://github.cor	verilog implementation of Python emulator, six 16-bit registers	
risc_core_i	https://opencor	planning	Manuel Imhof	RISC	16	16	kintex-7-3	James	Brakef	349		6	1		526	##	14.7	0.67	3.0	336.8	X	B	vhdl	13	CPU	Y	asm	N		1K	1K				8	4	2001	2009		Havard arch, thesis project	derived clocks: estimated derating
risc0	https://sourcefo	beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James	Brakef	1186		6	4	6	110	##	14.7	0.67	1.0	61.9	X		verilog	8	RISC0	Y	yes	N		4G	4G						2011			minimalist Wirth, education tool	
risc-16	https://github.c	stable	Bruce Jacob	RISC	16	16												0.67					vhdl	12	soc	Y	yes	N		64K	64K	N	9		8		2000	2015	https://user.eng.u	single cycle, pipeline & OO variants	Little Computer (LC-896) derivative
risc16_archer	https://github.c	alpha	Alexander Archer	risc	16	16																	vhdl	7	cpu	Y		N		64K	64K	N	14		8		2019		educational	
risc5	http://www.pro	beta	Niklaus Wirth	RISC	32	32	zu-2e	James	Brakef	2001	392	6	4		177	##	v20.1	1.00	1.0	88.3	ILX		verilog	8	RISC5	Y	yes	Y		4G	4G				16		2013	2017	http://www.astro	minimalist Wirth, part of Project Obe	32x32 multiplier, wikipedia entry
risc5	http://www.pro	beta	Niklaus Wirth	RISC	32	32	zu-3e	James	Brakef	1936	392	6	4		213	##	v21.1	1.00	1.0	109.9	ILX		verilog	8	RISC5	Y	yes	Y		4G	4G				16		2013	2017	http://www.astro	minimalist Wirth, part of Project Obe	32x32 multiplier, wikipedia entry
risc5	http://www.pro	beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James	Brakef	2441		6	4	1	92	##	14.7	1.00	1.0	37.8	ILX		verilog	8	RISC5	Y	yes	Y		4G	4G				16		2013	2017	http://www.astro	minimalist Wirth, part of Project Obe	32x32 multiplier, wikipedia entry
risc5	http://www.pro	beta	Niklaus Wirth	RISC	32	32	zu-3e	James	IBUF clocking			6	4		213	##	v21.1	1.00	1.0		ILX		verilog	8	RISC5Top	Y	yes	Y		4G	4G				16		2013	2017	http://www.astro	minimalist Wirth, part of Project Obe	32x32 multiplier, wikipedia entry
risc5	http://www.pro	beta	Niklaus Wirth	RISC	32	32	atrix7-35	James	Brakef	2913		6		48	50	##	v20.1	1.00	1.0	17.2	ILX		verilog	8	RISC5Top	Y	yes	Y		4G	4G				16		2013	2017	http://www.astro	minimalist Wirth, part of Project Obe	32x32 multiplier, wikipedia entry
risc63	https://github.c	alpha	Dominik Salvet	RISC	64	16																	vhdl	16	risc63			N				Y	39		16		2021		tighlty packed 16-bit ISA	thesis in Chech
riscff		proprietar	ExpressIf	RISC	16	16																	proprietary													2004			now produce ESP8266 & ESP32	
risc-fuggit	https://github.com/itsShn		Nikhil Shah	RISC	32	32																	verilog	33	riscmain	y		N		4G	4G				32		2019		non-standard set of conditional branches, schematic conflicts with documentation o	
riscompatible	https://opencor	beta	Andre Soares	RISC	32	32	kintex-7-3	James	set IO	2167		6		1	145	##	14.7	1.00	3.0	22.3	X		vhdl	12	riscompat	Y	yes	N	Y	4G	4G	Y			16		2014			based on RISCO processor by Junqueira & Suzim 1993	
risc-processor	https://github.c	stable	Jeff Bush	RISC	32	32	kintex-7-3	James	Brakef	1445		6		6	161	##	14.7	1.00	1.0	111.6	X		verilog	22	fpga_top	Y	yes	N		4G	4G	Y	21		32		2008	2019	https://github.cor	two designs with same name	MIT course work
rise	https://opencor	beta	Jlechner etal	RISC	16	16	kintex-7-3	James	missing black boxes			6	1				14.7	0.67	1.0		X		vhdl	26	rise	Y	asm	N		64K	64K				16	5	2006	2010	en.wikiversity.org	ARM style register usage	
rj32	https://github.c	alpha	rj45	RISC	16	16																	verilog	8	top	Y	asm	N		64K	64K	Y	32		16		2013	2022	https://github.cor	Digital schematic editer	nanogo compiler, youtube videos
rois	https://opencor	alpha	James Brakefield	RISC	24	24	**zu-2e**	James	no blk	627		6			382	##	v19.2	0.83	1.0	507.1	X		vhdl	2	rois24_24min			N		16M	16M	N	30		64	1	2016	2017		single pipe stage, passes simulation	24-bit word operations only
rois	https://opencor	alpha	James Brakefield	RISC	24	24	kintex-7-3	James	Brakef	384		6		1	170	##	14.7	0.83	1.0	368.8	X		vhdl	2	rois24_24min			N		16M	16M	N	30		64	1	2016	2017		single pipe stage, passes simulation	24-bit word operations only
rois	https://opencor	alpha	James Brakefield	RISC	24	24	kintex-7-3	James	Brakef	382		6		1	120	##	14.7	0.83	1.0	261.7	X		vhdl	2	rois24_24up			N		16M	16M	Y	55		64	1	2016	2017		single pipe stage, pre simulation stag	8, 16 & 24-bit load/store
rois	https://opencor	alpha	James Brakefield	RISC	24	24	**zu-2e**	James	huge l	9000		6			150	##	v19.2	0.83	1.0	13.9	X		vhdl	2	rois24_24up			N		16M	16M	Y	55		64	1	2016	2017		single pipe stage, pre simulation stag	8, 16 & 24-bit load/store
rrisc	https://github.com/reneri		Rene Schallner	risc	8	8			Rene Schallner						100			0.33	8.0				vhdl	8	top	Y	asm	N		64K	64K	Y			8		2020	2022	https://git.sr.ht/~r	originally TTL/schematic, beginner's p	doc PDF file huge
rtf64	https://github.c	alpha	Robert Finch	RISC	64	8																	system v	3	rtf64	Y	yes	Y				Y			32		2020	2021		variable length instructions	Posit support, glossary & references
s6soc	https://opencor	stable	Dan Gisselquist	RISC	32	32	spartan-6	James	sparta	2820		6	1	10	133	##	14.7	1.00	1.0	47.3	X	Y	verilog	31	toplevel			N	N	4G	4G	N	20		16	5	2015				uses ZIP CPU
sayeh_cpu	https://github.c	untested	Armin Kazemi	RISC	16	16												0.67	1.0				vhdl		Sayeh	Y	asm	N		64K	64K				64			2017		16-bit MIPS, data flow schematic	64 word reg file?
sayeh_process	https://opencor	stable	Alireza Haghdoost, Arr	RISC	16	8	kintex-7-3	James	Brakef	479		6	1		164	##	14.7	0.67	1.0	229.7	X		verilog	13	Sayeh	Y		N		64K	64K				32		2008	2009	haghdoost.persiangig.com		simple RISC
sayuri_cpu	http://www.mo	stable	Toyoaki Sagawa	RISC	32	32	kintex-7-3	James	Brakef	1604		6			208	##	14.7	1.00	1.0	129.9	X		vhdl	13	cpu01			Y		4G	4G				32		2000	2000		dead weblink	high number of DFF
scarts	https://opencor	beta	Jlechner, Martin Walte	RISC	16	16	kintex-7-3	James	missing signal declarat			6					14.7	0.67	1.0				vhdl	18	scarts		yes	N		64K	64K		122		16	4	2011	2012		Scarts Processor	GCC compiler
schoolmips	https://github.com/MIPSf		Andrea Guerrieri	RISC	32	32																					yes			4G	4G								https://github.cor	small MIPS CPU core originally based	schoolMIPS has several versions
senior-sagn-1	https://github.c	simulatio	Niranjan Ramadas	RISC	64	32	kintex-7-3	James	way to	135009		6	32		75	##	14.7	1.00	1.0	0.6	X		verilog	28	pipeline			N	Y			Y	137		32	4-8	2012	2012	nrbramadas.appsp	university ASIC project, read PDF	64-bit data paths, superscalar, branch analysis
simplecpu	https://www-us	untested	Michael Freeman	RISC	32	32																	vhdl										8				2018	2019	https://www-user	Educational, also a version 2 with VH	both mips & riscv RTL
simple-v	https://libre-soc.org/docs		Luke Leighton	risc	64	32																	python			Y		Y				Y			32		2018	2022	https://libre-soc.o	Scalable Vectors for Power ISA	has the respect of Mitch Alsup
slurm	https://github.com/james		James Sharp	risc	16	16																Y	verilog	54	slurm16_s	Y	asm	N		64K	64K	Y	20		16		2022		SLURM16 SoC - SLightly Useful RISC M	Video console system-on-chip made for the iC
softcore-cpu	https://github.com/Ayme		Aymen Sekhri	RISC	32	16																I	vhdl	15	control_u	Y	asm	N		4G	4G	Y	32		7		2019	2020		course project, seven "x86" registers,	32-bit immediates, multi-cycle design
spartanMC	http://www.spa	stable	Falk Hassler	RISC	18	18	kintex-7-3	James	Brakef	853		6	1	2	120	##	14.7	0.67	1.0	94.6	X	Y	verilog	38	spartanmc	Y	asm										2012	2014		SPARC like register windows	
src	https://github.c	untested	Heuring & Jordan	RISC	32	32																	verilog														2018	http://www.zeepe	book by Heuring & Jordan	also Kilts cpt17 Adv FPGA dsgn
stacks-16-bit	https://github.com/rcrist/		rcrist	risc	16	16																	schemat	36													2022	https://www.instr	Digital schematic, TTL & 3 layer bread	pictures of 3 layer breadboard
supersmall	http://www.eec	stable	Michael Ritchie	RISC	32	32	stratix_3	Michael	Ritch	207		A		2+8	126	##	q9.0	1.00	16.0	38.1	I		verilog														2005	2009		2-bit serial, Mostly MIPS-I compliant	Copyright 2005,2006,2009 Jonathan Rose, and
suslik	https://opencor	alpha	Goran Dakov	RISC	32	32	kintex-7-3	James	missing file(s)			6				##	14.7	1.00	1.0				verilog	4	cpu	bm	asm										2015	2016		"arithmetic core"	has testbench & caches
swssp	https://www.ipc	patented	Othman Ahmad	RISC	8+	8+																	schematic			Y			Y						8+		2014	2021	https://groups.goo	patent, "simplest scalable" data/inst s	a template for dsgn configuration of uP
swt16	https://github.com/captai		captaindane	RISC	16	16																	verilog	10	swt16-top	Y	asm	N	Y	64K	64K	Y	31		16	5	2020		16-bit, 5-stage RISC uP. RTL description in Verilog. Includes assembler, simulator, and	
sxp	https://opencor	beta	Sam Gladstone etal	RISC	32	32			too many los														verilog	12	sxp			N		4G	4G				32		2001	2009		basic RISC	too many los
table887	https://github.c	alpha	Robert Finch	RISC	32	16	kintex-7-3	James	Brakef	643		6		2	208	##	14.7	0.67	1.0	217.1	X		verilog	2	table887	Y		N	N	64K	64K		28		8		2014	2016			included with Table888 source code
table888	https://github.c	alpha	Robert Finch	RISC	32	16	kintex-7-3	James	Brakef	5756		6	9	6	137	##	14.7	2.00	1.0	47.6	X		verilog	3	table888	bme				4G	4G	Y	130		8		2014	2016		2016 version gives same reults as 201	code for cache & mmu incomplete
tarhi	https://github.c	alpha	Dagvadorj Galbadrakh	RISC	32	32	kintex-7-3	James	everyt	396		6		1	123	##	14.7	1.00	4.0	77.9	X		verilog	4	tarhi_controller			N		16M	16M	N	11		4		2013	2013		no doc, extremely small RISC	difficulty with timing, try 7.0ns
theia_gpu	https://opencor	beta	Diego Valverde	RISC	96	64	kintex-7-3	James	huge a	934049		6				##	14.7	0.40	1.0			GPU	verilog	32	theia												2009	2012		Ray Cast Programable graphic Proces	four cores, huge LUT count, 2/3rds LUT RAM
thor	https://opencor	mature	Robert Finch	RISC	64	16	**zu-5e**	James	WIP							##	v21.1	2.00	1.0				system v	27	thor2021	Y	asm	Y		16E	16E	Y			64		2015	2021	https://github.cor	Thor-5: L1 & L2 caches, GP float & ve	plans for more features, eventually 2M LUTs
thor	https://opencor	mature	Robert Finch	RISC	32	32			Robert Finch	90000				306									verilog		thor	Y	asm	Y		4G	4G	Y			64		2015	2022	https://github.com/robfinch/Thor		variable length instructions
thor	https://opencor	mature	Robert Finch	RISC	64	32			Robert Finch	210000				306									verilog		thor2	Y	asm	Y		4G	4G	Y			64		2015	2022	https://github.cor	Thor-2: L1 & L2 caches, GP float & vec	tor regs
thor	https://opencor	mature	Robert Finch	RISC	64	16			Robert Finch	210000				306									verilog		thor5	Y	asm	Y		4G	4G	Y			64		2015	2022	https://github.cor	Thor-5: L1 & L2 caches, GP float & ve	plans for more features, eventually 2M LUTs
tigli_cpu		stable	Cleiton Juffo	RISC	16	16	kintex-7-3	James	Brakef	636		6			455	##	14.7	0.67	4.0	119.7	X		verilog	24	cpu	Y		N	Y	64K	64K		16		16		2013	2013		course project, not pipelined	no LUT RAM for reg file
tim	https://github.com/ben-n		Ben Marshall	RISC	32	8	**zu-3e**	James	degenerate synthesis			6				##	v21.1	0.33	3.0				vhdl	15	top	Y		Y		4G	4G	Y	50				2014	2015		TIM: Tiny Instruction Machine, variable	length inst
tiny_soc	https://github.com/ept22		Ezra Thomas	RISC	8	16																Y	verilog	16	top	Y	asm	N	Y	64K	64K	Y	44		16		2020	https://ezrasrobot	small cpu with VGA	includes GPU (char gen)
tiny64	https://opencor	stable	Ulrich Riedel	RISC	32	32	kintex-7-3	James	Brakef	874		6			189	##	14.7	1.00	2.0	107.9	X		vhdl	6	tinyx					64K	64K		14		8		2004	2007		data size from 32 to 64 bits	micro-coded sub-ops
tinycpu	https://opencor	alpha	Jordan Earls	RISC	8	8	arria-2	James	Brakef	136		A			384	##	q13.1	0.17	2.0	235.5	IX		vhdl	2	tinycpu		asm	N	N	1K	1K		12		4		2012	2012	directory contains	subset of 6502	MIPS/inst reduced due to few inst
tinyisa	https://github.com/dillon		Dillon Huff	RISC	32	32																	verilog	49	cpu	Y		N		4G	4G	N	13		32			2019		very small ISA with multi-cycle, pipelined & with forwarding implementations	
tiny-riscv	https://github.com/hushc		Hyounguk Shon	RISC	32	32																	verilog	35	riscv_top	Y		N		4G	4G	Y	24		32			2019		course work, reduced risc-v, 24 inst, four variations: cache, multi-cycle, pipeline & si	
totalcpu	https://opencor	alpha		RISC	12+	12	kintex-7-3	James	Brakef	229		6	1		149	##	14.7	0.33	3.0	71.7	X		verilog	10	cpu			N							16		2007	2009		data width 12 bits and up, no data memory	
tpu	https://github.c	untested	Colin Riley	RISC	16	16																	vhdl	20	tpu_top			N		64K	64K	Y			8		2016	2016	https://domipheu	Test Processing Unit. Or Terrible Proc	essing Unit. A simple 16-bit CPU in VHDL for ed
ucode_cpu	http://minnie.tu	stable	Warren Toomey	RISC	16	16	atrix-7-3	James	4K LUT	6748		6	1	1		##	14.7	0.67	2.0		I		vhdl	16	cpu			N	N	64K	64K	N			16		2012	2015			originally schematic based (Logisim)
ucpuvhdl	https://github.c	stable	Reed Foster	RISC	8	16	kintex-7-3	James	512 LU	933		6			118	##	14.7	0.33	2.0	20.8	X		vhdl	29	core	Y	asm	N		256	64K	Y	12	2	7		2016	2017	https://github.cor	six tutorials on uCPUvhdl	using muCPUv2_1 of 3 upwards compatible de
up1232	http://www.dte	stable	Santiago de Pablo	RISC	8	16	kintex-7-3	James	Brakef	220		6			244	##	14.7	0.33	3.0	122.0	X		vhdl	3	up1232a			N		64K	64K	Y	33	2	32		2000	2000		bare core, prog size 4K to 64K	description in source files
urisc		errors	Farhad Mavaddat	RISC	16	16	kintex-7-3	James	missing module			6				##	14.7	0.67	4.0				vhdl	31	urisc	Y				64K	64K	N	1				1987	2012	https://cs.uwaterl	Ultimate Reduced Inst Set Computer Un. Of Waterloo	
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16																	verilog	74	cpu	Y		N		64K	64K	N			4		2019	2019		**ten implementations of increasing so**	**missing memory & test bench RTL**
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16	**zu-3e**	James	multi-c	171		6			357	##	v21.1	0.67	1.0	1399	X		verilog	5	cpu01	Y		N	N	64K	64K	N	23		4		2019	2019		multi-driven nets	single cycle CPU that has an IPC of 1
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16	**zu-3e**	James	multi-c	288		6				##	v21.1	0.67	1.0		X		verilog	7	cpu02	Y		N	N	64K	64K	N	23		4		2019	2019		multi-driven nets	multi cycle CPU that has an IPC of 1
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16	**zu-3e**	James	multi-driven net			6				##	v21.1	0.67	1.0		X		verilog	7	cpu03	Y		N	Y	64K	64K	N	23		4	5	2019	2019		multi-driven nets	5-stage pipelined CPU, same for cpu4 thru cpu
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16	**zu-3e**	James	multi-driven net			6				##	v21.1	0.67	1.0		X		verilog	7	cpu04	Y		N	Y	64K	64K	N	23		4	5	2019	2019		multi-driven nets	Data forwarding from the ALU
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16	**zu-3e**	James	multi-driven net			6				##	v21.1	0.67	1.0		X		verilog	7	cpu05	Y		N	Y	64K	64K	N	23		4	5	2019	2019		multi-driven nets	Branch prediction with a BTB with 2-bit saturat
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16	**zu-3e**	James	multi-driven net			6				##	v21.1	0.67	1.0		X		verilog	7	cpu06	Y		N	Y	64K	64K	N	23		4	5	2019	2019		multi-driven nets	tournament branch predictor
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16	**zu-3e**	James	multi-driven net			6				##	v21.1	0.67	1.0		X		verilog	7	cpu07	Y		N	Y	64K	64K	N	23		4	5	2019	2019		multi-driven nets	Memory latency parameter
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16	**zu-3e**	James	multi-driven net			6				##	v21.1	0.67	1.0		X		verilog	8	cpu08	Y		N	Y	64K	64K	N	23		4	5	2019	2019		multi-driven nets	instruction cache and data cache

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe lin	start year	last revis	secondary web link	note worthy	comments
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16	zu-3e	James	multi-driven net			6				##	v21.1	0.67	1.0		X		verilog	9	cpu09	Y		N	Y	64K	64K	N	23		4	5	2019	2019		multi-driven nets	DMA module and its interrupt mechanism
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	RISC	16	16	zu-3e	James	multi-driven net			6				##	v21.1	0.67	1.0		X		verilog	10	cpu10	Y		N	Y	64K	64K	N	23		4	5	2019	2019		multi-driven nets	DMA interleaved with instructions that access
vespa	http://www.are	untested	David J. Lilja	RISC	32	32																	verilog			Y	asm	N		4G	4G	N	16		32		2005	2005		from book: Designing Digital Computer Systems with Verilog 0-521-82866-X, Un. Mir
vhdl-processor	https://github.com/lazyor		Anurag Saha Roy	risc	8	16			incomplete source code														vhdl	8	processor	Y				256	256				16		2019		"generic 8-bit processor"	no memory, just IO locations
vhdl-simple-up	https://github.c	untested	Pietro Lorefice	RISC	16	16	arria-2	James	ran out of memory		A					##	q18.0	0.67	1.0				vhdl	10	processor	Y		N	N	64K	64K	N			16		2014	2014		simple processor using VHDL for logic	based on Gray's xsoc
vhdl-simple-up	https://github.c	untested	Pietro Lorefice	RISC	16	16	kintex-7-3	James	ran out of memory			6				##	14.7	0.67	1.0				vhdl	10	processor	Y		N	N	64K	64K	N			16		2014	2014		simple processor using VHDL for logic	based on Gray's xsoc
vrisc	https://github.com/jayval		Jay Valentine	RISC	32	32																	vhdl	21	processor	Y		N	Y	4G	4G	Y	37	6	32			2017		little-endian Harvard architecture RIS	simple caches
wisc-sp13	https://github.c	stable	Shyamal H Anadkat	RISC	16	16																	verilog			Y		N		64K	64K	N			8		2007	2017		CS 552 term project : functional design of a microprocessor called the WISC-SP13
wisc-sp13	https://github.c	stable	Prayag Bhakar	RISC	16	16																	verilog			Y		N		64K	64K	N			8		2007	2021		CS 552 term project : functional design of a microprocessor called the WISC-SP13
x9	https://github.com/yehzh		Simon Zhang	risc	8	9																	system v	24	top_level	Y	asm	N		256	256	Y	13		16		2016	2017		9-bit processor: 4:1:4 op-code, R0, R1 fields
xgate	https://opencor	alpha	Robert Hayes	RISC	16	16	kintex-7-3	James	Brakef	2778		6			159	##	14.7	0.67	1.0	38.3	X		verilog	7	xgate_top	Y		N					42		16		2009	2013		high pin count	Freescale XGATE co-processor compatible
xr16	https://github.c	stable	Jan Gray	RISC	16	16	kintex-7-3	James	Brakef	273		6			263	##	14.7	0.67	1.0	644.8	X		verilog	4	xr16	Y		N		64K	64K				16		1999	2001		handcrafted instruction set	tool FPGA P&R, speed mode better
xr16	https://github.c	stable	Jan Gray	RISC	16	16	**zu-2e**	James	needs	346		6			282	##	v20.1	0.67	1.0	547.0	X		verilog	4	xr16	Y		N		64K	64K				16		1999	2001		handcrafted instruction set	tool FPGA P&R, speed mode better
xsoc	http://www.fpg	stable	Jan Gray	RISC	16	16	kintex-7-3	James	very sl	371		6				##	14.7	0.67	1.0		X		verilog	16	xsoc	Y	yes	N	N	64K	64K	Y	16	4	16		2000	2001		very compact, bare core	similar to xr16
xtensa	https://ip.cadenproprietar		tensilica/cadence	RISC	16	16,2	proprietary																proprietary							4G	4G				32	5,7			ch 8, Processor De	upward compatible family, sliding reg	ASIC usage, TIE tool generates RTL & software
xthundercore	http://forum.ga	alpha	majordomo	RISC	32	16	kintex-7-3	James	Brakef	793		6		2	193	##	14.7	1.00	1.0	243.7	X		vhdl	49	xtc	pm	yes	N	Y	4G	4G				16	5	2014		http://www.xthur	Gadget Factory Forum thread	in debug, no comments, mostly in simulation
xucpu	https://opencor	alpha	Jurgen Defurne	RISC	16	16	spartan-6	James	Brakef	356		6		4	187	##	14.7	1.00	1.0	524.8	X	Y	vhdl	25	system_4k					4K	4K						2015	2017		Experimental Unstable CPU	
xulalx25soc	https://opencor	mature	Dan Gisselquist	RISC	32	32	spartan-6	James	Sparta	7936		6	4	25	87	##	14.7	1.00	1.0	11.0	X	Y	verilog		toplevel			N	N	4G	4G	N	20		16	5	2015				uses ZIP CPU
yasep	https://hackada	alpha	Yann Guidon	RISC	16	32	kintex-7-3	James	reduce	632		6			215	##	I14.7	1.00	2.0	170.0	AX		vhdl	3	microYAE	s	asm	N	N	2G	2G		51		16		2005	2018	www.youtube.cor	JavaScript generated VHDL, revisions	ongoing
yfcpu	https://github.c	errors	Cory Walker	RISC	16	16	kintex-7-3	James	degen	18		6				##	14.7	0.67	1.0				verilog	2	yfcpu	Y		N	N	256	256	Y	5	1	16				Colin Mackenzie?	Educational	very simple
ygrec8	https://hackaday.io/proje		Yann Guidon	risc	8	16																	vhdl					N		256	256	Y	20		8		2017	2021	https://hackaday.i	educational uP with front panel	front panel: one button per op-code
zbasic	https://github.c	mature	Dan Gisselquist	RISC	32	32																	verilog	70	main	Y	yes	N	N	4G	4G	Y	35		16	5	2018	2020	https://github.cor	bare bones variant of zipcpu	autofpga builds complete system
zipcpu	https://github.c	stable	Dan Gisselquist	RISC	32	32	kintex-7-3	James	Brakef	1687		6		2	218	##	14.7	1.00	1.0	128.9	X		verilog	7	zipcpu	Y		N	N	4G	4G	Y	35		16	5	2015	2021	www.librecores.o	ISA has chnaged, multiple instruction	http://zipcpu.com/zipcpu/2018/01/01/zipcpu-
riscv_cpu_veri	https://github.c	simulatio	Elliot Liu	riscv	32	32	artix-7	James	Brakef	config'd for sim		6				##	v22.2	1.00	1.0				verilog	26	Risc5CPU	Y	yes	N		4G	4G	Y	45		32			2022		Five-Stage Pipe RISC-V uP	has top schematic
riscv_minimax	https://github.com/gsmec		Graeme Smecher	riscv	32	16	KU060	Graeme	Smec	423	61	6			200	##	v22.2	1.00	4.0	118.2	X		vhdl	2	minimax	Y	yes	N		4G	4G	Y			32			2022		Two port register file	most 32-bit insts microcoded, limited 16-bit IS
riscv_naxriscv	https://github.com/Spinal		Charles Papon?	riscv	32	32	artix7	Charle	AKA sp	13300		6			155			1.00	0.4	29.1			scala			Y	yes	N		4G	4G	Y			32			2022	https://spinalhdl.g	OoO execution w/reg renaming, Superscalar(2 decode, 3 execution units, 2 retire), 2	
riscv_noel	https://www.gaisler.com/		gaisler	riscv	32	32															IX		vhdl	40		Y	yes	N		4G	4G	Y			32			2022	https://www.gais	many config options	32 & 64-bit, software tools, bit files
riscv_percival	https://github.com/artecs		ArTeCS (Un Madrid)	riscv	64	32	kintex7	ArTeC	largest	57129	27996	6			50		v20.2	1.00	2.0	0.4	X		system v	~60		Y	yes	N		4G	16E	Y			32		2017	2022	https://github.cor	Open-Source Posit RISC-V Core with Quire Capability, cav6(AKA Ariane) derivative	
riscv_reonv	https://github.com/IcbcFc		Lucas Castro	riscv	32	32	spartan-6	Wajih	Yousse	3370		6			133			1.00	1.0	39.4						Y	yes	N		4G	4G	Y	45		32			2018	https://www.hind	Lightweight Cryptographic Instruction	risc-v version on Leon3 tools
darkriscv	https://github.c	alpha	Marcelo Samsoniuk	risc-v	32	32	kintex-7-3	James	Brakef	1422		6		1	167	##	14.7	1.00	1.0	117.2	X		verilog	2	darksocv	Y	yes	N		4G	4G	Y			32	2	2018	2018	https://blog.hacks	written in one night, low line count	readme is descriptive, uses cache
instant-soc	https://www.fp	stable		risc-v	32	32																	vhdl					N		4G	4G	Y			32		2020	2022	https://github.cor	converts C++ into VHDL, risc-v CPU &	perpherials, unused instructions omitted
kcp53000	https://github.c	simulatio	Samuel Falvo II	risc-v	64	32	kintex-7-3	James	trimm	2455		6			175	##	14.7	2.00	1.0	142.9	X	B	verilog	4	polaris	Y	yes	N	Y	16E	16E	Y			32		2016	2017	https://github.cor	kestrel #3, basic 64-bit RISC-V	uses state machine RTL generator
leon3	http://www.gais	stable	Jiri Gaisler, Jan Anders	risc-v	32	32						6						1.00	1.0		AILX	Y	vhdl	100s		Y	yes	Y		4G	4G	Y			64	7	2003	2021	https://en.wikiped	RTL for LEON3, LEON5 and NOEL-V for microchip & xilinx RAD hard parts	
openc	https://github.com/T-hea		T-Head Semiconducto	risc-v	32	32																	verilog			Y	yes	N		4G	4G	Y			32			2021	https://www.cnx-	Alibaba ASIC RISC-V uP: e902-e906-c906-and-c910, docs in Chinese, many many large	
reonv	https://github.c	difficult	Lucas Castro	risc-v	32	32	kintex-7-3	James	many files			6				##	14.7	1.00	1.0				vhdl			Y	yes	N		4G	4G	Y			32		2017	2018	https://strijar.live	uses Leon infrastructure with risc-v ISA	
riscv_ariane	https://github.c	untested	pulp project	risc-v	64	32												1.00	1.0							Y	yes	Y		4G	4G	Y			32	6	2018	2022	https://github.cor	single issue, in-order CPU which implements the 64-bit RISC-V ISA IMAC extensions,	
riscv_biriscv	https://opencores.org/pr		Ultra Embedded	risc-v	32	32																	verilog			Y	yes			4G	4G	Y			32		2020	2021	https://github.cor	dual issue	also single issue version
riscv_black-par	https://github.com/black-		Daniel Petrisko	risc-v	64	32																	system verilog			Y	yes	Y		16E	16E	Y			32			2021		cache-coherent, RV64GC multicore	
riscv_bonfire	https://github.c	vado proj	Thomas Hornschuh	risc-v	32	32	kintex-7	James	Brakefield			6				##	14.7	1.00	1.0				vhdl		bonfire_c	Y	yes			4G	4G	Y			32			2018	http://bonfirecpu.	vivado project, based on lxp32	comingled lxp32 & RISCv; poorly organized gith
riscv_boom	https://github.c	untested	UC Berkeley	risc-v	32	32																	scala			Y	yes	Y		4G	4G	Y	45		32				https://boom-cor	Berkeley Out-of-Order RISC-V Processor	
riscv_briscv	https://ascslab.(	untested	various	risc-v	32	32																				Y	yes	Y		4G	4G	Y	45		32		2018	2020	https://opencores	six implementations of risc-v	Boston Un. Course work
riscv_clarinet	https://github.com/HPC-L		Riya Jain etal	risc-v	32	32																	bluespec verilog			Y	yes	Y		4G	4G	Y	45		32	5		2020	https://github.cor	RISC-V with posit arithmetic, bluespec	verilog for riscv flute & (3) posit sizes
riscv_clarvi	https://github.c	stable	Robert Eady	risc-v	32	32	arria-2	James	Altera	2616		A			178	##	q18.0	1.00	1.0	68.2	I	B	system v	7	clarvi	Y	yes	N		4G	4G	Y			32	6	2016	2017	https://www.cl.ca	educational simple RISC-V implement	doesn't make use of block RAM RTL
riscv_cpu	https://github.c	untested	misha kevlishvili	risc-v	32	32												1.00	1.0				verilog			Y	yes	N		4G	4G	Y	45		32		2019	2019	https://www.yout	simple and easy to understand design	
riscv_croyde	https://github.com/ben-n		Ben Marshall	risc-v	64	32																Y	system v	35	core_top	Y	yes	N		16Q	16Q	Y			32	3	2021	2021		64-bit rv64imck ISA	small, simple yet SOC, see also his tim & vanill
riscv_dark	https://github.c	beta	Marcelo Samsoniuk	risc-v	32	32	kintex-7-3	Marcelo	Sam	1000		6			220	##	v20.1	1.00	1.0	220.0			verilog	4	darkriscv	Y	yes	N		4G	4G	Y	45		32		2018	2021	https://opencores	written in one night, low line count	builds for five fpga boards
riscv_engine-v	https://github.c	untested	Antti Lukats	risc-v	32	32				306		4						1.00	6.7		AL		verilog	11		Y	yes	N		4G	4G	Y	45		32		2018	2018	https://riscv.org/2	RISC-V contest 2nd place, 8-bit ALU	no source for xilinx, no implementation docs
riscv_femtoRV	https://github.c	stable	Bruno Levy	risc-v	32	32																	verilog	45	femtosoc	Y	yes	N		4G	4G	Y	45		32		2020	2022	https://members.	eight riscv uP, teaches FPGAs to unive	100MB of images deleted
riscv_fwrisc	https://github.c	untested	Matthew Balance	risc-v	32	32	ice40	Matthew	Bala	1653		4				##		1.00	6.7		AL		system v	8	fwrisc_fpg	Y	yes	N		4G	4G	Y	45		32		2018	2018	https://opencores	featherweight entry 2018 RISC-V cont	0.15 DMIPS/MHz
riscv_fwrisc	https://github.c	untested	Matthew Balance	risc-v	32	32	igloo2	Matthew	Bala	1060		4			20	##		1.00	6.7	2.8	AL		system v	8	fwrisc_fpg	Y	yes	N		4G	4G	Y	45		32		2018	2018	https://opencores	featherweight entry 2018 RISC-V cont	0.15 DMIPS/MHz
riscv_GRVI-pha	http://fpga.org/	beta	Jan Gray	risc-v	32	32	virtex-u-2	Jan	Gray	320		6		1	375	##	v16.4	1.00	1.0	1172	X		proprietary			Y	yes	N		4G	4G	Y	45		32	3	2015	2018	https://www.yout	hand fitted & placed	"Hoplite" router, 1680 cores in XCVU9P
riscv_harzad5	https://github.com/Wren		Luke Wren	risc-v	32	32																	verilog	18	hazard5_c	Y	yes	N		4G	4G	Y			32	5	2019	2021	https://github.cor	RISC-V processor designed for the RISCBoy games console	
riscv_hl5	https://github.c	stable	Paolo Mantovani	risc-v	32	32																	systemC	12	hl5	Y	yes	N		4G	4G	Y	45		32		2017	2020		32-bit RISC-V processor designed with HLS, coded in SystemC	
riscv_humming	https://github.c	stable		risc-v	32	32	kintex-7-3	James	too many los			6				##	14.7	1.00	1.0				verilog	141	e203_cpu	Y	yes	N		4G	4G	Y			32		2016	2018		e200 has opensource	also have a chip
riscv_humming	https://github.c	stable		risc-v	32	32	kintex-7-3	James	Brakef	14119		6		32	62	##	14.7	1.00	1.0	4.4	X		verilog	141	e203_soc	Y	yes	N		4G	4G	Y			32		2016	2018		e200 has opensource	also have a chip
riscv_humming	https://github.c	untested		risc-v	32	32																	verilog			Y	yes	N		4G	4G	Y			32		2017	2018		AKA e200, Chinese	software tools take 80MB
riscv_ibex_low	https://github.c	stable	Philipp Wagner	risc-v	32	32																	system v	27	ibex_core	Y	yes	N		4G	4G	Y			32		2020	2022	https://www.lown	AKA zero-riscy, also see pulp	several tapeouts
riscv_jive	https://github.com/fredre		Frédéric REQUIN	risc-v	32	32												1.00	20.0				verilog	19	jive_cpu_t	Y	yes	N		4G	4G	Y			32			2018		Size-Optimized Microcoded RISC-V CP	16-bit ALU
riscv_kian	https://github.com/spline		splinedrive	risc-v	32	32																	verilog	17	kianv	Y	yes	N		4G	4G	Y			32			2021		very simple riscv cpu/soc one single file implementation	
riscv_lattice	https://www.lat	stable	Lattice Semi	risc-v	32	32	machXO3	Lattice	Semic	1507		4		4	60	##		1.00	1.0	39.8	L	Y				Y	yes	N		4G	4G	Y			32	5		2021		RV32I ISA, 5 stage pipeline, configured & generated using Lattice Propel	
riscv_lowrisc	https://github.c	scala	Alex Bradbury	risc-v	32	32																Y	scala															2017	http://www.lowri	version 0.4-lowRISC with tagged memory and minion core	
riscv_microsem	https://github.c	stable	Microsemi	risc-v	32	32	polarfire	microsemi		8614		4	2	10	122		L11.8	1.00	1.0	14.2			proprietary			Y	yes	N		4G	4G	Y			32		2016	2018	https://www.micr	is encrypted IP	has caches
riscv_minerva	https://github.com/lambc		lambdaconcept	risc-v	32	32																	nmigen			Y	yes	N		4G	4G	Y			32	6		2020		microarchitecture of Minerva is largely	inspired by the LatticeMico32 processor
riscv_myth	https://github.com/kuby1		Kubiran Karakaran	risc-v	32	32																																	https://tl-x.org		
riscv_neorv32	https://github.c	stable	Stephan Nolting	risc-v	32	32	cyclone-IV	Stepha	rtl fpg	848		4			111	##	q19.1	1.00	4.0	32.7	AL	Y	vhdl	25	neorv32_t	Y	yes	N		4G	4G	Y			32		2020	2021	https://opencores	**very well documented, customiza**	**many perpherals, LUT counts for all variati**
riscv_niosv	https://www.in	proprietar	Intel	risc-v	32	32	agilex	intel	fastest	1509		A		2	566	##	q21.3	1.00	1.0	375.2	I		proprietary			Y	yes	N		4G	4G	Y			32	5		2021		free license, small inst & data mem	RV32IA spec, M20K for reg file, interrupts
riscv_niosv	https://www.in	proprietar	Intel	risc-v	32	32	stratix-10	intel	fastest	1580		A		2	362	##	q21.3	1.00	1.0	229.1	I		proprietary			Y	yes	N		4G	4G	Y			32	5		2021		free license, small inst & data mem	RV32IA spec, M20K for reg file, interrupts
riscv_niosv	https://www.in	proprietar	Intel	risc-v	32	32	arria-10	intel	fastest	1375		A		2	306	##	q21.3	1.00	1.0	222.3	I		proprietary			Y	yes	N		4G	4G	Y			32	5		2021		free license, small inst & data mem	RV32IA spec, M20K for reg file, interrupts
riscv_orca	https://github.c	beta	VectorBlox	risc-v	32	32	stratix-5	vectorblox		1082		A		?	244	##	14.7	0.98	1.0	221.0	I		vhdl	13	orca	Y	yes	N		4G	4G	Y			32		2016			*, /, fltg-pt all optional	RV32IM
riscv_paranut	https://github.com/hsa-e		Alexander Bahle	risc-v	32	32																	vhdl	~100	paranut	Y	yes	N		4G	4G	Y			32			2021	https://ees.hs-aug	SIMD vect & simul multi-threading in	Effic embed Sys group Un of Applied Sciences
riscv_piccolo	https://github.c	untested	BlueSpec	risc-v	32	32																	bluespec verilog			Y	yes	N		4G	4G	Y			32	3	2018	2018		RISC-V CPU, simple 3-stage pipeline, for low-end applications (e.g., embedded, IoT),	
riscv_picorv32	https://github.c	beta	Clifford Wolf	risc-v	32	32	xcku3p-3	Cliffor	small	761		6			769	##	v16.2	1.00	3.0	336.8	X	Y	verilog	1	picorv32	Y	yes	N		4G	4G	Y			32		2016	2020		mimimal features, soc options	designed for minimum LUTs
riscv_picorv32	https://github.c	beta	Clifford Wolf	risc-v	32	32	kintex-U-3	Cliffor	small	761		6			454	##	v16.2	1.00	3.0	198.9	X	Y	verilog	1	picorv32	Y	yes	N		4G	4G	Y			32		2016	2020		mimimal features, soc options	LUTs & Fmax for Kintex, Virtex & Ultrascale+
riscv_potato	https://github.c	beta	Kristian Skordal	risc-v	32	32	kintex-7-3	James	Brakef	2467		6			116	##	14.7	1.00	1.0	47.1	X	B	vhdl	24	pp_core	Y	yes	N	N	4G	4G	Y	30		32		2014	2020		risc-V interger only, no mult	"rocket-core" version at risc.org
riscv_pulpino	https://github.c	untested	Andreas Kurth	risc-v	32	32	arria-2	James	missing files			A				##	q18.0						system v	9		Y	yes	N		4G	4G	Y			32		2015	2020	http://www.pulp-	pulpissimo is single core "pulp" with	interest in non-riscv ISA expansion
riscv_reboot	https://github.c	pre alpha	Robert Baruch	risc-v	32	32																	python	8		Y	yes	N		4G	4G	Y	45		32			2020	https://www.yout	work in progress, has 60 minute video on design issues	
riscv_reindeer	https://github.c	untested	pulserain.com	risc-v	32	32															AL		verilog			Y	yes	N		4G	4G	Y	45		32	4	2018	2018	https://riscv.org/2	RISC-V contest prize	
riscv_riscboy	https://github.com/Wren		Luke Wren	risc-v	32	32																	verilog	54	riscboy_fp	Y	yes	N		4G	4G	Y	45		32		2018	2021		portable games console desgn, PCB dsgn, see riscv_hazard3&5	
riscv_rocket	https://github.c	scala	Andrew Waterman	risc-v	32	32																Y	scala			Y	yes	N		4G	4G	Y			32		2016	2018			
riscv_rpu	https://github.c	untested	Colin Riley	risc-v	32	32	artix-7	Colin	Riley	3291		6	12	1	100	##	14.7	1.00	1.0	30.4			vhdl	14	core	Y	yes	N		4G	4G	Y			32		2015	2020	http://labs.domip	Series of 16 tutorials on uP design, wo	RPU uP, TPU now discarded
riscv_rsd	https://github.com/rsd-de		Susumu Mashimo	risc-v	32	32	zynq	Susumu	Mash	28166		6			90			1.00	1.0	3.2			system verilog			Y	yes	N		4G	4G	Y			32			2020		RISC-V out-of-order superscalar proce	can be synthesized for small FPGAs
riscv_rtg4	https://github.c	mature	microsemi	risc-v	32	32																				Y	yes	N		4G	4G	Y			32		2018	2020	https://github.cor	risc-v for actel FPGAs, tcl files only	based on rocket chip

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe lin	start year	last revis	secondary web link	note worthy	comments
riscv_rudolv	https://github.com/bobbl		Jörg Mische	risc-v	32	32	kintex-7-3	Jörg Mische		545		6			200	##		1.00	1.0	367.0	ALMX		verilog	4	pipeline	Y	yes	N		4G	4G	Y			32	5		2021		RISC-V processor for real-time system	34 clock mult & divide
riscv_rv01_cor	https://opencor	stable	Stefano Tonello	risc-v	32	32	kintex-7-3	James Brakef		13997		6	4	62	130	##	14.7	1.00	1.0	9.3	X		vhdl	65	rv01_selft	Y	yes	N		4G	4G	Y			32		2015	2017		all files in one directory	two self test tops
riscv_rv12	https://github.c	untested	Roa Logic BV	risc-v	32	32	arria-2	James Brakefield				A				##	q18.0						system verilog			Y	yes	N		4G	4G	Y			32				https://roalogic.com		
riscv_rv3n	https://github.com/risclite		Li Xinbing	risc-v	32	32																	verilog	17		Y	yes	N		4G	4G	Y			32			2020		RV32IMC processor core, which has a new pipeline with "3+N" stages	
riscv_rvbs	https://github.com/CTSRD		Alexandre Joannou	risc-v	32	32																	bluespec	33		Y	yes	N		4G	4G	Y			32			2020		descript of the RISC-V instruction set in Bluespec, requires bluespec, no verilog code	
riscv_scarv-cpu	https://github.com/scarv/		Daniel Page	risc-v	32	32																Y	verilog	31	frv_core	Y	yes	N		4G	4G	Y			32		2019	2020	https://www.ukris	side channel hardened, no cache, branch prediction or virtual memory, research pro	
riscv_scr1	https://github.c	untested	Syntacore	risc-v	32	32	arria-2	James Brakefield				A				##	q18.0						system v	47	scr1_top	Y	yes	N		4G	4G	Y			32		2017	2018	http://syntacore.com		
riscv_scr1	https://github.c	untested	Syntacore	risc-v	32	32																	system v	47	scr1_core	Y	yes	N		4G	4G	Y			32		2017	2021	http://syntacore.com		
riscv_serv	https://github.c	untested	Olof Kindgren	risc-v	32	32	ice40					4									L		verilog	17	serv_top	Y	yes	N		4G	4G	Y	45		32		2018	2021	https://riscv.org/2	RISC-V contest prize, 1-bit ALU	https://github.com/olofk/corescore
riscv_serv	https://github.c	untested	Olof Kindgren	risc-v	32	32	vu37p	Olof Kindgren		215		6		0.5		##		1.00	32.0		X		verilog	52	serv_top	Y	yes	N		4G	4G	Y	45		32		2018	2021	https://riscv.org/2	6K cores in vu37p, reg-file in blk-RAM	https://github.com/olofk/corescore
riscv_shakti	https://github.c	untested	IIT Madras	risc-v	32	32												1.00	1.0				bluespec	25		Y	yes	N		4G	4G	Y			32	3	2014	2021	https://shakti.org/	~8 different riscv cores, Madras India	several web sites & datings
riscv_sifive	https://www.sif	asic		risc-v	32	32																	proprietary			Y	yes	N		4G	4G	Y			32				https://www.sifiv	ASIC IP house, 32-bit "freedom" core	free Artix-7 bitstream
riscv_sifive	https://www.sif	asic		risc-v	64	32																	proprietary			Y	yes	N		4G	4G	Y			32				https://www.sifiv	ASIC IP house, 64-bit "freedom" core	free Artix-7 bitstream
riscv_sodor	https://github.c	scala	UC Berkeley	risc-v	32	32																	scala			Y	yes	N		4G	4G	Y			32					1, 2, 3 and 5 stage pipe versions	
riscv_spu32	https://github.c	untested	Merten Maik	risc-v	32	32																Y	verilog		top	Y	yes	N		4G	4G	Y			32		2019	2021	https://giters.com	actively being developed	
riscv_steel	https://opencores.org/pr		Rafael Calcada	risc-v	32	32	**zu-2e**	James Brakef		1775		6			208	##	v19.2	1.00	1.0	117.4			verilog	21	steel_top	Y	yes	N		4G	4G	Y			32	3		2020	https://github.com	github version has vivado proj	under grad thesis
riscv_steel	https://opencores.org/pr		Rafael Calcada	risc-v	32	32	atrix-7-3	James Brakef		1784		6			116	##	v19.2	1.00	1.0	65.0			verilog	21	steel_top	Y	yes	N		4G	4G	Y			32	3		2020	https://github.com	github version has vivado proj	under grad thesis
riscv_swerv	https://github.c	untested	Western Digital	risc-v	32	32	ZCU102	Weste	high LU	30128		6	4	62				1.00	1.0				system verilog			Y	yes			4G	4G	Y			32		2019	2020	https://blog.weste	9 stage pipe, dual issue	risc-v SoC for fpga, riscv_swerv_eh1_fpga now
riscv_taiga	https://gitlab.co	stable	Eric Matthews	risc-v	32	32	zynq			1551				1	123			1.00	1.0	79.3	IX		system v	46		Y	yes	N		4G	4G	Y			32		2017	2022		TAIGA: A new RISC-V soft-processor f	33% smaller & 39% faster than LEON3
riscv_tinsel	https://github.com/POETS		Ghaith Tarawneh	risc-v	32	32																	bluespec verilog															https://poets-proj	message-passing architecture designed for FPGA clusters	
riscv_uriscv	https://github.com/ultrae		ultra_embedded	risc-v	32	32												1.00	2.0				verilog	7	riscv_core	Y	yes	N		4G	4G	Y			32			2021	https://opencores	Simple, small, multi-cycle 32-bit RISC-V CPU implementation	
riscv_urv-core	https://github.c	error	Tomasz Włostowski	risc-v	32	32	kintex-7-3	James	missing files							##	14.7	1.00	1.0				verilog			Y	yes	N		4G	4G	Y			32		2015	2015			
riscv_vanilla	https://github.c	verified	Ben Marshall	risc-v	32	32	artix-7	Ben Marshall		2422		6			150			1.00	2.0	31.0			verilog	26	frv_cpu_a	Y	yes	N		4G	4G	Y			32	5		2019		"toy" 5 stage RISC-V CPU, implementing the rv32imc	
riscv_vanilla	https://github.c	verified	Ben Marshall	risc-v	32	32	zu-5e	James	IO limi	2422		6				##	v21.1	1.00	2.0				verilog	26	frv_cpu_a	Y	yes	N		4G	4G	Y			32	5		2019		"toy" 5 stage RISC-V CPU, implementing the rv32imc	
riscv_vexriscv	https://github.c	beta	Charles Papon	risc-v	32	32	artix-7	Charles Papo		481		6			346			0.52	1.0	374.1	X		scala		smallest	Y	yes			4M	4M	Y						2018	https://riscv.org/2	preformance #s for 8 configurations c	"Briey" is SOC variant
riscv_vexriscv	https://github.c	scala	Charles Papon	risc-v	32	32	atrix-7-3	Charles Papo		1399		6			295			1.00	1.0	210.9	X	Y	scala		full no cac	Y	yes	N		4G	4G	Y			32			2018	https://riscv.org/2	preformance #s for 8 configurations c	"Briey" is SOC variant
riscv_vexriscv	https://github.c	beta	Charles Papon	risc-v	32	32	artix-7	Charles Papon?				6						0.52	1.0		X		vero;pg			Y	yes			4M	4M	Y						2018		verilog source	scala not needed
riscv_vhdl	https://opencor	errors	Sergey Khabarov	risc-v	64	32	kintex-7-3	James	many files, missing typ			6				##	14.7	1.00	1.0			Y	vhdl & verilog			Y	yes	N		4G	4G	Y			32		2016	2018	https://github.com	System-On-Chip based on bare Rocke	both rocket & river cores
riscv_vroom	https://github.com/Moon		Paul Campbell	risc-v	32	32																	system v	51	cpu	Y	yes	N		4G	4G	Y			32		2019	2022	https://hackaday.i	high-end RISC-V implementation	8 IPC (instructions per clock) peak, goal ~4 ave
riscv_zscale	https://github.c	scala	UC Berkeley	risc-v	32	32																	scala			Y	yes	N		4G	4G	Y			32		2015	2017		not maintained & not conformant	
rjsc5	https://github.com/rj45/r		rj45	risc-v	32	32																	schemat	6		Y	yes	N		4G	4G	Y			32			2022		Digital schematic, 16-bit data paths, micro-coded, multi-cycle	
superscaler-ris	https://github.com/risclite		Li Xinbing	risc-v	32	32																	verilog	15	ssrv_top	Y	yes	N		4G	4G	Y			32		2019	2020		Super-scalar out-of-order RV32IMC	performance: 6.4 CoreMark/MHz
verilogboy	https://hackada	alpha	Wenting Zhang	risc-v	8	8	**zu-3e**	James	vivado	872	608	6			313	##	v21.1	1.00	3.0	119.5	X		verilog	36	vbh	Y	yes	N	N	64K	64K	Y						2019	https://github.com	Game Boy in Verilog, both CPU (SM83	uses riscv_picorv32 core
vscale	https://github.c	stable	UC Berkeley	risc-v	32	32	kintex-7-3	James Brakef		3072		6			127	##	14.7	1.00	1.0	41.2	X		verilog	23	vscale_core			N							32		2016	2017		risc-v RV32IM vscale processor, depre	depreciated: not up to date (risc-v)
yarvi	https://github.c	beta	Tommy Thorn	risc-v	32	32	kintex-7-3	James Brakef		2152		6		17	122	##	14.7	1.00	2.0	28.3	X		verilog	3	yarvi_soc	Y	yes	N	N	4G	4G				32	3		2016		no multiply or divide	simple implementation of RISC-V
f32c	https://github.c	beta	marko zec, vordah, Dar	risc-v/MIPS	32	32	atrix-7-3	zec & vordah		1048		6	4	33	185	##	14.7	1.00	1.0	176.5	X		vhdl	50		Y	yes	N	Y	4G	4G	Y	30		32	5	2014	2019	http://www.nxlab	MIPS or RISC-V ISA, Arduino support	https://www.youtube.com/watch?v=55MzMH
sys_emz1001	https://github.com/zpekic		Zoltan Pekic	S2000	4	8	spartan3	Zoltan Pekic		1022	344	4				##	14.7	0.16		X	Y	vhdl	26	EMZ1001/	Y	asm	N	Y	128	4K		59				2022	https://hackaday.i	recreation of Iskra EMZ1001 4-bit mic	no block ram? Picture of original chip
jcore_aka_sh2	http://www.j-co	difficult	Jeff Dionne. Rob Landl	SH2	32	16			need to run make per README file														vhdl	136												2014	2016	https://www.yout	https://www.youtube.com/watch?v=	Americans in Japan
j-core_pi	https://github.c	stable		SH2	32	16																Y	vhdl	45	cpu	Y	yes			4G	4G	Y			16		2014	2020	https://www.cnx-	different from jcore_aka_sh2, schematic for Spartan-6 board	
fgpu	https://github.c	stable	Muhammed al Kadi	SIMT	32	32	zynq7045	Muhammed a		128K		6	192	167		##	v17.2				X		vhdl	34	fgpu	Y	yes	Y		4G	4G	Y			32		2016	2017	https://dl.acm.org	eigth cores, reviews comparable proj	vivado fltg-pt IP, benchmarks, wikipedia: GPGP
verilogboy	https://hackada	alpha	Wenting Zhang	SM83	8	8	**zu-3e**	James	vivado	2415	1601	6		4	238	##	v21.1	0.33	3.0	10.8	X	Y	verilog	22	boy	Y	yes	N	N	64K	64K	Y						2019	https://github.com	Game Boy in Verilog, both CPU (SM83	also https://github.com/neildryan/GBA
leon2	https://github.c	stable	Jiri Gaisler	SPARC	32	32	kintex-7-3	James Brakef		5992		6	1	12	133	##	14.7	1.00	1.0	22.3	X		vhdl	82	leon	Y	yes	Y		4G	4G	Y			64	5	1999	2003	https://en.wikiped	large config file, rad-hard asic version	https://www.gaisler.com/index.php/products/
leon2	https://github.c	stable	Jiri Gaisler	SPARC	32	32	cyclone-1	Klas Westerlu		7554		4		42	50	##		1.00	1.0	6.6	I		vhdl	90	leon	Y	yes	Y		4G	4G	Y			64	5	1999	2003	https://en.wikiped	LUT #s from Nios vs Leon2 compariso	https://www.gaisler.com/index.php/products/
leon3	http://www.gais	stable	Jiri Gaisler, Jan Anders	SPARC	32	32	kintex-7-3	Jiri Gaisler		2920		6			183			1.00	1.0	62.7	AILX	Y	vhdl	100s	leon3x	Y	yes	Y		4G	4G	Y			64	7	2003	2021	https://en.wikiped	**customized for ~50 FPGA boards, ,**	**xls with utilization for all targets**
openpiton	https://github.c	difficult	mmckeown	SPARC	32	32	kintex-7-3	James	too many files			6				##	14.7	1.00	1.0				verilog			Y	yes	Y	N	4G	4G	Y			64		2015	2019	http://parallel.prin	Princeton Un.	both FPGA & ASIC, very many source files
s1_core	https://opencor	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakef		52845		6	8	59	56	##	v14.1	2.00	1.0	2.1	IX		verilog	136	s1_top	Y	yes	Y	N	4G	4G	Y			32		2007	2012	https://en.wikiped	reduced version of OpenSPARC T1	Vivado run
sparc64soc	https://opencor	alpha	Dmitry Rozhdestvensk	SPARC	64	32	kintex-7-3	James	errors			6				##	14.7	2.00	1.0			Y	verilog	263	W1	N		Y									2009	2010		huge source file count	work in progress with no progress
temlib	http://temlib.or	stable		SPARC	32	32	kintex-7-3	James Brakef		2579		6		32	111	##	14.7	1.00	1.0	43.1	X		vhdl	48	mcu_simple			Y	N	4G	4G	Y			64		2013	2015		copywrite: experimental use	has caches
temlib	http://temlib.or	stable		SPARC	32	32	kintex-7-3	James Brakef		3730		6	5		111	##	14.7	1.00	1.0	29.8	X		vhdl	48	fpu_simple			Y	N	4G	4G	Y			64		2013	2015		copywrite: experimental use	options for fltg-pt, pipeline, mul & div configur
amic-0	https://github.c	stable	Alberto Moriconi	stack	32	8	**zu-3e**	James	vivado	622	357	6			250	##	v21.1	1.00	1.0	401.9			vhdl	8	processor													https://en.wikiped	based on mic-1 by Andrew Tanenbau	uCode, usually Java virtual machine
hive	https://opencor	stable	Eric Wallin	stack	32	16	arria-2	James Brakef		1420		A	8	24	283	##	q13.1	1.00	1.0	199.4	ILX		verilog		hive_core	Y		N					N	40		10	8	2013	2015		4 symetrical stacks, eight threads via	pipeline barrel
m17	http://users.ece	asic	Philip Koopman	stack																			proprietary															https://users.ece.c	chapter 4.3 in Koopman	6600 gate ASIC
minicpu	http://www.cs.h	stable	Hirotsugu Nakano	stack	16	5	kintex-7-3	James	lots of	433		6	1	1	128	##	14.7	0.33	1.0	97.7	X		verilog	7	minicpu	Y	yes	N		4K	4K	N	26				2008	2018		same as tiny-cpu	uses Flex, Bison & Perl to create gcc compiler
minicpu-s	https://github.c	stable	Michael Morris	stack	16	8	kintex-7-3	James Brakef		147		6			741	##	14.7	0.67	28.0	120.6	X		verilog	2	both	Y		N					33				2012	2013		separate source for each CPLD chip, u	fits (2) XC9500 CPLD
mproz	http://www.bitl	stable	K. Lee	stack	16	16	kintex-7-3	James	schematic			6				##	14.7	1.00	1.0				schematic			Y	asm	N			32K						1999	2007	https://groups.go	little documentation, CPLD implemen	*.1 schematics, also mproz3
pancake	https://people.e	stable	Bruce Land	stack	16	5	kintex-7-3	James	bypass	441		6	1	1	128	##	14.7	0.67	1.0	194.8	X		verilog	7	de2_minic	Y	yes	N		4K	4K		31				2010	2014	http://www.cs.hir	The Pancake Stack Machine dervied f	Cornell ECE5760
spu-mark-ii	https://github.c	WIP	Felix Queißner	stack	16	16																	vhdl	17	soc	Y		N		64K	64K	Y	34				2020	2022	https://ashet.com	micro-code ISA stack machine	ISA at doc/specs/spu-mark=ii.md
stack-cpu	https://github.com/Arlet/		Arlet Ottens	stack	16	16															X		verilog	2	cpu					64K	64K	N	23				2017		3 or 4 stacks, load/store with stack de	xilinx block RAM	
tiny_cpu	http://www.cs.h	errors	K. Nakano	stack	16		kintex-7-3	James	multiple assignments c			6				##	14.7	0.66	3.0		IX		verilog	11	DE2_TINY	Y	yes	N		4K	4K						2007	2009	http://www.cs.hir	different from tinycpu	**uses Flex, Bison & Perl to create gcc comp**
the12X_12uP		stable	James Brakefield	stack/acc	12	12	kintex-7-3	James Brakef		972		6	1	1	123	##	14.7	0.50	1.0	63.3	X		vhdl	2	the12x_12	Y		Y	N	4K	4K	N	54		64	1	2015			combo stack/accumulater design	load/store arch, not optimized
aquarius	https://opencor	stable	Thorn Aitch	SuperH-2	32	16	**zu-3e**	James	vivado	3563	1384	6	2	16	147	##	v21.1	1.00	1.0	41.2	ILX		verilog	21	top	Y	yes	N		4G	4G	Y					2003	2015	http://Opf.org/j-co	clone of Hitachi SH-2	project seems to have stalled
aquarius	https://opencor	stable	Thorn Aitch	SuperH-2	32	16	kintex-7-3	James Brakef		4071		6	2	10	97	##	14.7	1.00	1.0	23.7	ILX		verilog	21	top	Y	yes	N		4G	4G	Y					2003	2015	http://Opf.org/j-co	clone of Hitachi SH-2	project seems to have stalled
sys0800	https://github.c	stable	Zoltan Pekic	TMS0800	4	12																	vhdl	26	sys0800	Y	yes	N	Y	12	512						2019	2020	https://hackaday.i	calculator chip, both TI Datamath and	256x52 micro code
tms1000	https://opencores.org/pr		Nand Gates	TMS1000	4	8																	verilog	4	tms1000	Y		N		64	1K		54				2021	2021		Four function BCD calculator chip	used in several TI products
uTTA		stable	Hans Tiggeler	TTA	16	16	kintex-7-3	James Brakef		810		6	1		57	##	14.7	0.67	1.0	47.4	X		vhdl	23	utta_struc	N	asm	N											http://www.ht-lab	time triggered arch	bad weblink
bfcpu	http://www.cliff	stable	Clifford Wolf	Turing	8	3	kintex-7-3	James Brakef		422		6			345	##	14.7	0.01	4.0	2.0	X	B	vhdl	4	cw6671	Y	yes	N	N	64K	64K	Y	8				2003	2003	https://en.wikiped	no accum, data pointer and bracketed	current version & earlier version
bfcpu	http://www.cliff	stable	Clifford Wolf	Turing	8	3	**zu-3e**	James	vivado	303		6			500	##	v21.1	0.01	4.0	4.1	X	B	vhdl	4	cw6670	Y	yes	N	N	64K	64K	Y	8				2003	2003	https://en.wikiped	no accum, data pointer and bracketed	first implementation, no data cache
bfcpu	http://www.cliff	stable	Clifford Wolf	Turing	8	3	**zu-3e**	James	vivado	387		6			500	##	v21.1	0.02	4.0	6.5	X	B	vhdl	4	cw6671	Y	yes	N	N	64K	64K	Y	8				2003	2003	https://en.wikiped	no accum, data pointer and bracketed	internal 1-byte data cache doubles performanc
aeMB	https://opencor	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James Brakef		1018		6	3		131	##	14.7	1.00	1.0	128.5	ILX		verilog	7	aeMB_cor	Y	yes	N		4G	4G	Y					2004	2009		not 100% compatable	
aeMB	https://opencor	beta	Shawn Tan	uBlaze	32	32	**zu-3e**	James	vivado	997	434	6	3		250	##	v21.1	1.00	1.0	250.8	ILX		verilog	7	aeMB_cor	Y	yes	N		4G	4G	Y					2004	2009		not 100% compatable	
an-noc-mpsoc	https://opencor	mature	Alireza Monemi	uBlaze	32	32	**zu-3e**	James	vivado	1079		6	3	1	333	##	v21.1	1.00	1.0	308.9	X	Y	verilog	90	aeMB_top	Y	yes	N		4G	4G	Y					2014	2019		choice of lm32, aeMB, mor1kx or or1	full system has network of cores
an-noc-mpsoc	https://opencor	mature	Alireza Monemi	uBlaze	32	32	kintex-7-3	James Brakef		1164		6	3	1	192	##	i14.7	1.00	1.0	165.2	X	Y	verilog	90	aeMB	Y	yes	N		4G	4G	Y					2014	2017		choice of lm32, aeMB, mor1kx or or1	full system has network of cores
mblite	https://opencor	beta	Tamar Kranenburg	uBlaze	32	32	kintex-7-3	James Brakef		941		6		2	227	##	14.7	1.00	1.0	240.9	IX		vhdl	18	core_wb	Y	yes	N		4G	4G	Y	86		32		2009	2017		not all instructions implemented	moved everything to work library
mb-lite_plus	http://www.late	stable	Huib Arriens	uBlaze	32	32	kintex-7-3	James Brakef		244		6		2	319	##	14.7	1.00	1.0	#####	X	B	vhdl	34	tumbl	Y	yes	N		4G	4G	Y			32		2010	2012		Delft Un. Of Tech. course work	use inferred RAM
microblaze	https://www.xil	proprietar	Xilinx	uBlaze	32	32	virtex ultr	Xilinx		563		6		1	682	##		1.03	1.0	#####	X		proprietary			Y	yes	opt		4G	4G	Y	86		32	3	2002		https://en.wikiped	MicroBlaze MCS, smallest configurati	70 configuration options, MMU optional
microblaze	https://www.xil	proprietar	Xilinx	uBlaze	32	32	kintex-7	Xilinx		546		6		1	320			1.03	1.0	603.7	X		proprietary			Y	yes	opt		4G	4G	Y	86		32	3	2002			MicroBlaze MCS, smallest configurati	70 configuration options, MMU optional
mpdma	https://opencor	beta	quickwayne	uBlaze	32	32	kintex-7-3	James Brakefield				6				##	14.7	1.00	1.0			Y	perl			Y	yes	N		4G	4G	Y			32		2006	2009		Soft MultiProcessor on FPGA	Perl gens *.xmp, mhs, mss & ucf files
myblaze	https://opencor	mature	Jian Luo	uBlaze	32	32	kintex-7-3	James Brakefield				6				##	14.7	1.00	1.0				myhdl	15	top	Y	yes	N		4G	4G	Y			32		2010	2013		clone, python code generators	
myblaze	https://opencor	mature	Jian Luo	uBlaze	32	32	kintex-7-3	James Brakefield				6				##	14.7	1.00	1.0				myhdl			Y	yes	N		4G	4G	Y			32		2010	2013		clone, python code generators	
openfire_core	https://opencor	alpha	Alex Marschner, Steph	uBlaze	32	32	kintex-7-3	James	empty project file			6					14.7	0.33	1.0				verilog	12	openfire_	Y	yes	N	N	4G	4G	Y			32		2007	2009		OpenFire Processor Core	"FPGA Proven"
openfire2	https://opencor	beta	Antonio Anton	uBlaze	32	32	kintex-7-3	James Brakef		1201		6	3	2	105	##	14.7	1.00	1.0	87.4	X	Y	verilog	27	openfire_	Y	yes	N	N	4G	4G	Y			32		2007	2012		"FPGA Proven"	derived from Stephen Craven's OpenFire
openscale	http://www.lirm	stable	Lyonel Barthe	uBlaze	32	32	spartan-3	Lyonel Barthe		1563		4			91		i12.1	1.00	1.0	58.2	X	Y	vhdl	26	sb_core		yes			4G	4G	Y	86		32	5	2010	2012	www.lirmm.fr/AD	NoC secretblaze	data is for single secretblaze

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
secretblaze	http://www.lirm	beta	Lyonel Barthe	uBlaze	32	32	spartan-3	Lyonel Barthe		1563		4			91		i12.1	1.00	1.0	58.2	X		vhdl	26	sb_core		yes			4G	4G	Y	86		32	5	2010	2012	www.lirmm.fr/ADAC		
mxp	http://vectorblo	stable	VectorBlox Computing	vect	8		zynq45-7	vectorblox		39856		6	64	81	175	##	v17.2	1.00	0.1	35.1			proprietary			Y											2012	2017	http://www.ece.u	MXP Matrix Processor is a scalable so	LUT count for 8 lanes with custom inst
symphony	http://www.ece	alpha	Jason Yu	vect	32	32																	verilog	47	vpu_top												2007	2008		vector addon to NIOS	
lemberg	https://github.c	stable	Wolfgang Puffitsch	VLIW	32	32	cyclone-4	James Brakef		37459		4	25	54	43	##	q13.1	1.00	1.0	1.1	I		vhdl	57	core	Y	yes	Y		4G	2M	Y			32	4	2011		http://www2.imm	upto 4 inst/clock	LPM mem & floating point
p-vex	https://github.com/tvana		Thijs van As	VLIW	32	##	kintex-7-3	James	bypass	1660		6		1	233	##	14.7	1.00	1.0	140.1			vhdl	26	system	Y	yes	N					73		32	4	2005	2015	http://www.vliw.c	1, 2 or 4 issue VLIW, uses HP VEX too	probable degeneracy, LUT RAM for program m
spam-1	https://github.c	simulation	John Lonergan	vliw	8	48																	verilog		cpu	Y	yes	N		64K	64K	Y					2019	2022	https://hackaday.	8 Bit CPU Hardware Implementation i	TTL modules with verilog
tinyvliw8	https://opencor	alpha	Oliver Stecklina	VLIW	8	32	kintex-7-3	James	hacked	895		6			149	##	14.7	0.33	1.0	55.0	X		vhdl	19	sysarch			N	Y	256	1K	Y					2013	2020		tinyVLIW8 soft-core processor	bare core, Altera LPM for RAMs
ao486	https://opencor	beta	Aleksander Osman	x86	32	8	**zu-2e**	James Brakef	altera avalon IO			6				##	v20.1	1.00	1.0		I	Y	system v	85	ao486	Y	yes			4G	4G	Y					2014	2014	https://github.cor	complete 486, SoC configuration	non-SoC, no MMU, not superscalar
ao486	https://opencor	beta	Aleksander Osman	x86	32	8	cyclone-4	James Brakef		36094		4	4	47	46	##	q13.1	1.00	1.0	1.3	I	Y	system v	85	ao486	Y	yes			4G	4G	Y					2014	2014	https://www.stuff	complete 486, SoC configuration	Henry Wong thesis at U.Toronto, also youtube
ao486_mister	https://github.c	beta	Sorgelig	x86	32	8	**zu-3e**	James	vivado defaults			6						1.00	1.0		I	Y	system v	85	ao486	Y	yes			4G	4G	Y					2020	2021		complete 486, SoC configuration	mister version of ao486: reworked with many
cpu_basic	https://github.com/vhdlf/		vhdlf	x86	8	8	cyclone-4	vhdlf		3558			4										vhdl	7	top	Y		N		64K	64K	Y	26		16			2020		32-bit CPU with x86 inst. format	readme has screen shots, **very readable RTL**
cpu86	http://www.ht-l	beta	Hans Tiggeler	x86	8	8	kintex-7-3	James Brakef		3421		6	1		127	##	14.7	0.17	2.0	3.1	X		vhdl	23	cpu86_top	Y	yes	N	N	1M	1M	Y					2002	2018	http://www.ht-lab	8088 clone	ht-labs offers several uP cores
mcl86	https://github.c	stable	Ted Fried	x86	16	8	kintex-7-3	Ted Fried		308		6		4	180			0.67	20.0	19.6	X		verilog	3	EU	Y	yes	N	N	1M	1M	Y					2016	2021	http://www.embe	**microcoded, meets original 8088 timing@100MHz**	
next186	https://opencor	stable	Nicolae Dumitrache	x86	16	8	arria-2	James Brakef		1966		A	2		77	##	q13.1	0.67	2.0	13.1	IX		verilog	4	Next186_(	Y	yes	N	N	1M	1M	Y					2012	2013		boots DOS	
next186_soc_p	https://opencor	stable	Nicolae Dumitrache	x86	16	8	kintex-7-3	James	translate errors			6	1			##	14.7	0.67	2.0			Y	verilog	40	ddr_186	Y	yes	N	N	1M	1M	Y					2013	2019		SoC version of next186	boots DOS, does video games & sound
next186mp3	https://opencor	stable	Nicolae Dumitrache	x86	16	8	kintex-7-3					6	1			##	14.7	0.67	2.0			Y	verilog	16	ddr_186	Y	yes	N	N	1M	1M	Y					2013	2014		SoC version of next186	boots DOS, has DSP core, no x86 source
rtf8088	https://opencor	planning	Robert Finch	x86	16	8	kintex-7-3	James Brakef		4514		6	4		174	##	14.7	0.67	3.0	8.6	X		verilog	57	rtf8088	Y	yes	N	N	1M	1M	Y					2012	2013	https://github.cor	8-bit memory data, e.g. 8088	
s80186	https://github.c	stable	Jamie Iles	x86	16	8	cyclone-V	Jamie Iles		1750		A			60			0.67	2.0	11.5	I	Y	system v	50	core	Y		N		1M	1M	Y					2017	2021	https://www.jami	80186 binary compatible core	implementing the full 80186 ISA
sp-i586	https://github.c	stable	Lini Mestar	x86	32	8	kintex-7-3	James Brakef		32144		6	4	28	73	##	14.7	1.00	2.0	1.1	X		verilog	37	top_sys	Y	yes	Y		4G	4G	Y					2016	2016	http://lmeshoo.ne	gate level dsgn, vivado project also	http://img.youtube.com/vi/2W1guyhCJuE/0.jp
sub86	https://opencor	alpha	Jose Rissetto	x86	16	8	kintex-7-3	James Brakef		1916		6			172	##	14.7	0.67	3.0	20.1	X		verilog	1	sub86	Y	yes	N	N	64K	64K	Y			7		2012	2013		very small x86 subset core	no segment registers, limited op-codes
v586	https://opencor	beta	Jose Rissetto	x86	32	8	kintex-7-3	James Brakef		22282		6	12	16	102	##	14.7	1.00	2.0	2.3	X		verilog	22	v586	Y	yes	N		1M	1M	Y					2014	2016	https://github.cor	MMU & caches, branch cache	www.youtube.com/channel/UCNbm8Bah54cw
v586	https://opencor	beta	Jose Rissetto	x86	32	8	**zu-3e**	James	vivado defaults			6	12	16	102	##	v21.1	1.00	2.0		X		verilog	22	core	Y	yes	N		1M	1M	Y					2014	2016	https://github.cor	MMU & caches, branch cache	www.youtube.com/channel/UCNbm8Bah54cw
y86-64	https://github.c	early	Adithya Sunil	x86	64	8																	verilog															2021		limited set of x86-64 operations	educational
zet86	https://opencor	alpha	Zeus Marmolejo	x86	16	8	kintex-7-3	James Brakef		3642		6	1		68	##	14.7	0.67	2.0	6.2	X		verilog	32	fpga_zet_	Y	yes	N	N	1M	1M	Y					2008	2018	https://github.cor	equivalent to 80186, boots MS-DOS	Zet The x86 (IA-32) open implementation
fpz8	https://opencor	stable	Fabio Pereira	Z8	8	8	cyclone-4	James Brakef		5184		4	1	16		##	14.7	0.33	4.0		I		vhdl	4	fpz8_cpu_	Y		N	Y	2K	16K	Y					2016	2016		Zilog Z8 encore (eZ8) 8-bit core	Altera megafunctions (mem)
altium/TSK80x	http://techdocs.	proprietar	Altium	Z80	8	8	spartan-3	Altium		2558		4			50			0.33	3.0	2.2	AILX		proprietary			Y	yes	N	N	64K	64K	Y					2004	2017	CR0140.pdf, CR01	frozen, asm, C, C++, schem, VHDL & V	default clock speed is 50MHz
a-z80	https://opencor	stable	Goran Devic	Z80	8	8	spartan-6	Goran Devic		1819		6		8		##	14.7	0.33	1.0		IX		verilog	24	z80_top_d	Y	yes	N	N	64K	64K	Y					2014	2020	https://github.cor	gate level reverse eng'd Z80	Complete implementation of a Sinclair ZX Spec
a-z80	https://opencor	stable	Goran Devic	Z80	8	8	kintex-7-3	James Brakef		1186		6			24	##	14.7	0.33	1.0	6.8	IX		verilog	24	z80_top_d	Y	yes	N	N	64K	64K	Y					2014	2020	https://github.cor	gate level reverse eng'd Z80	Complete implementation of a Sinclair ZX Spec
a-z80	https://opencor	stable	Goran Devic	Z80	8	8	**zu-3e**	James	timing	1761	365	6			41	##	v21.1	0.33	1.0	7.7	IX		verilog	24	z80_top_d	Y	yes	N	N	64K	64K	Y					2014	2020	https://github.cor	gate level reverse eng'd Z80	Complete implementation of a Sinclair ZX Spec
a-z80	https://opencor	stable	Goran Devic	Z80	8	8	cyclone-2	Goran Devic		2084		4		29	19	##	q11.1	0.33	1.0	3.0	IX		verilog	24	z80_top_d	Y	yes	N	N	64K	64K	Y					2014	2020	https://github.cor	gate level reverse eng'd Z80	Complete implementation of a Sinclair ZX Spec
darfpga	https://github.com/darfp		darfpga	z80	8	8															I	Y	VHDL & Verilog			Y	yes	N	N	64K	64K	Y						2022	https://github.cor	games ported to MiSTer and DE10-lite	
nextz80	https://opencor	stable	Nicolae Dumitrache	Z80	8	8	kintex-7-3	James Brakef		854		6			119	##	14.7	0.33	1.0	46.0	X	B	verilog	3	NextZ80CI	Y	yes	N	N	64K	64K	Y					2011	2019			claim of 700 LUTs in Spartan-3 probably wrong
opengateware	https://github.com/openg		opengateware	z80	8	8																Y	vhdl & verilog			Y	yes	N		64K	64K	Y						2022	https://github.cor	compatible Congo Bongo/Tip Top arc	several others at opengateware
reverse-u16	https://github.c	stable	A.T.	Z80	8	8	cylcone-4	James Brakef		11224		4		60		##	14.7	0.33	4.0		X	Y	vhdl	29	zxpoly	Y	yes	N	N	64K	64K	Y					2015			SOC project using T80, HDMI generat	retro Z80 based on T80 by Daniel Wallner
socz80	http://sowerbut	stable	Will Sowerbutts	Z80	8	8	spartan-6	James	constr	2568		6		15	93	##	14.7	0.33	3.0	4.0	X		vhdl	25	top_level	Y	yes	N	N	64K	64K	Y					2013	2014		based on Daniel Wallner's T80, for Papillio Pro board	
t80	https://opencor	stable	Daniel Wallner	Z80	8	8	kintex-7-3	James	Z80 m	1389		6			163	##	14.7	0.33	3.0	12.9	X		vhdl	5	T80a	Y	yes	N	N	64K	64K	Y					2002	2018		Z80, 8080 & gameboy inst sets, several usages	
tv80	https://opencor	mature	Guy Hutchison, Howar	Z80	8	8	kintex-7-3	James Brakef		1207		6			182	##	14.7	0.33	3.0	16.6	IX		verilog	6	tv80n	Y	yes	N	N	64K	64K	Y					2004	2018	https://github.cor	derived from Daniel Wallner's T80, ASIC implementations	
wb_z80	https://opencor	stable	Brewster Porcella	Z80	8	8	kintex-7-3	James Brakef		2025		6			144	##	14.7	0.33	3.0	7.8	X		verilog	4	z80_core_	Y	yes	N	N	64K	64K	Y					2004	2012		derived from Guy Hutchison TV80	Wishbone High Performance Z80
y80e	https://opencor	stable	Sergey Belyashov	Z80	8	8	cycone-3	Sergey Belyas		2557		4				##	14.7	1.00	3.0				verilog	15	top_level	Y	yes	N	N	64K	64K	Y					2013	2019		Y80e - Z80/Z180 compatible processo	based on Y80 from "Microprocessor Design Us
z80control	https://opencor	alpha	Tyler Pohl	Z80	8	8	kintex-7-3	James Brakef		1483		6			189	##	14.7	0.33	3.0	14.0	X	Y	verilog	55	top_de1	Y	yes	N	N	64K	64K	Y					2010	2012		Microprocessor targeting embedded	interfaces to DRAM, based on T80 core
z80-fpga	https://github.com/Obiju		Juan Gonzalez-Gomez	Z80	8	8															L		verilog	5		Y	yes	N	N	64K	64K	Y						2020		Based on iceZ0mb1e by abnoname and TV80, with tinyBasic	
z80soc	https://opencor	stable	Ronivon Costa	Z80	8	8	**zu-3e**	James Brakefield				6				1/1(	v21.2	0.33	3.0		IX	Y	vhdl	19	top_s3e	Y	yes	N	N	64K	64K	Y					2008	2016		based on Daniel Wallner's T80	
z80soc	https://opencor	stable	Ronivon Costa	Z80	8	8	spartan-3	James Brakef		2474		4	2	19	78	##	14.7	0.33	3.0	3.4	IX	Y	vhdl	19	top_s3e	Y	yes	N	N	64K	64K	Y					2008	2016		based on Daniel Wallner's T80	directory disappeared
complete_8bit	https://www.qu	stable	Van-Lei Le		8	8	kintex-7-3	James	modifi	208		6		1	260	##	14.7	0.33	3.0	137.5	X		vhdl	6	computer	N		N		96	128	Y					2016				memory_unit uses block RAM, IO ports prunec
gpu	https://opencor	stable	Diego A. Idarraga				kintex-7-3	James	errors in source			6				##	14.7	1.00	1.0				vhdl	21	gpu			Y									2015	2015		graphic processing unit	coding errors
pycpu	https://pycpu.w	myhdl	Norbert Feurle			8																	myhdl														2013		https://pycpu.wor	python hardware processor	
reduceron	https://www.cs.	stable	Matthew Naylor/Tommy Thorm													##					IX				Reduceron												2008	2018	https://github.cor	hardware for functional programming	red-lava generates the RTL

115 # usable(beta, st 1 25 88 254 blank 559 ## 526 ## 13 426 verilog 400 non-blank 659 80

50 "B" or "X" of lim 1 940 691 a 684 vhdl 367 asm 135 Web page DMIPS p en.wikipedia.org/wiki/Instructions_per community.freesc www.eembc.org/coremark/index.php

83 zu-3e sys verilog 55 forth 10 DMIPS per clock for many microprocessors: http://en.wikipedia.org/wiki/Instructions_per_second

proprietary 36

scala 12

schematic 19

MIPS/MHz Pro-rating for data size:

1-bit	0.04	16-bit	0.67	64-bit	2.00
4-bit	0.17	24-bit	0.80	**Silicon Area equivalents**	
8-bit	0.33	32-bit	1.00	LUTS/DSP48	16:1
12-bit	0.40	48-bit	1.50	LUTS/Block RAM	32:1

Under the assumption that the core is capable of one instuction per clock

75	_paper_only
60	educational
25	_weak_start
8	_up_cores
5	in limbo
10	planning
52	simulation
573	main+sim
521	net main
644	total

353	VHDL
399	Verilog
51	System Verilog
11	Spinal/Scala
7	VHDL & Verilog
3	MyHDL
36	proprietary
13	other
4	Schematics
877	total

418 designs with FOM (KIPs/LUT) results (some duplicates due to multiple FPGA runs)

385 designs with best FOM (likely true measure of # of usable designs)

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	used to indicate best KIPS/LUT for a given design, usually using fast FPGA family
cat	main, educational, planning, simulation, paper, in limbo or weak
_uP_all_soft folder	if opencores design is their folder name, otherwise my folder name
opencores or primary link	about 200 designs in open cores, about 100 in github
status	ASIC, paper (detailed in), planning (no source), alpha, beta, stable, mature, proprietary, untested; incomplete, educational typically <16 instructions, simulation
author	First Name, Last Name or university or corporation
style / clone	part number or "forth", RISC, accumulator, etc. "asic" indicates: avail as asic & fpga, an asic netlist source or a hard core within fpga chip
data size	data register size in bits
inst size	shortest instruction size in bits
FPGA	FPGA family for compile, place, route & timing, usually using fastest part grade
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALUT	total number of LUTs, ALUTs or tiles used including route-thrus & otherwise unavailable
Dff	total number of DFFs
LUT?	4-LUT, 6-LUT, Altera ALUT, Actel Tile
mults	total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up
blk RAM	total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up
Fmax	maximum primary clock speed from compile, place & route run with best clock constraint, fastest part, best die temp
date	date of compile, place & route; serves to identify source version
tool ver	Altera (**Q**uartus), Xilinx (ISE, **V**ivado), Lattice Semiconductor(**D**iamond) or MicroSemi(**L**ibero) tool version number

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	repor ter	com ents	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	ven dor	SOC	src code	#src files	top file	doc	tool chai	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pip e len	start year	last revis	secondary web link	note worthy	comments

MIPS /inst	prorated DMIPS per instruction, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
Vendor	Vendors for which design builds: Actel: Libero, Intel(Altera): Quartus; Latticesemi: Diamond & iCEcube, Xilinx: ISE & Vivado
SOC	B: bare core (no RAM connections or memory access delay), Y: System on a Chip (has peripherals)
src code	VHDL or Verilog or System Verilog or schematic or gates or Proprietary or Scala etc
# src files	number of source files for compile, place, route & timing; includes test benches
top file	top file for compile, place, route & timing run, multiple versions of same design distinguished here
doc	is documentation provided?
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point?
Hav'd	H: separate instruction and data memory(s), 2C: # caches, M: MMU, N: von Neuman (single memory bus)
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, conditionals count as one instruction, somewhat subjective
# adr modes	abs, imm, PC rel, indexed, reg-reg indexed; stack, indir, indir++, --indir; (indir), (indir++), (--indir), (indexed), abs-short/direct page, scaled
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions or web page updates
secondary web link	secondary web address
note worthy	anything special about the design