Small soft core uP Inventory

Opencore and other soft core processors

Only cores in the "usable" category included

Most Prolific Authors (alpha or better status) ©2025 James Brakefield		main RTL	
Robert Finch (https://github.com/robfinch	any-1, butterfly, fisa32, fisa64, ft64, ftfm, minimign4v, qupls, raptor64, rtf64, rft6809, rtf8088, rtf65002, rtf65003, scarerob-v, table888, table887, thor, rf68000, rfphoenix	verilog, system	20
Scott Baker (https://sco	1802,8085,z80,6502,6800,6805,6809,6309,6811,6812,pic14,9900,9995,pdp8,pdp11,nova,msp430 (proprietary except Nova, PDP11&8)	vhdl	15
Ted Fried	8088, 8086, 8051, 6502, 68000, Risc-V, z80 (emulators for others, 8051, 6502 & 8086 open source, others not)	verilog	7
Jeff Bush	Mitecpu, RISC-Processsor, ChiselGPU, LispMicrocontroller, PASC, NyuziProcessor	verilog	6
Michael Morris	m16c5x, m65c02, m65c02a, minicpu, minicpu-s, pdp6, p16c5x	verilog, sys	6
John Kent	micro8a, micro16b, system01, system05, system09, system11, system68	vhdl	5
Daniel Wallner	ax8, ppx16 (16C55 & 16F84), t65 (6502, 65C02 & 65C816), t80 (8080 & z80)	vhdl	5
C.H. Ting	ep16, eP32, ep8080, p16b, p24e	vhdl	5
Stephan Nolting	atlas_core, fluid-core, storm_core, neo430, riscv_neorv32	vhdl	5
Jecel Mattos de Assum	mcpu, ncpu, drv16, baby8 (also Digital schematic wrappers for serv, darkriscv, picorv32 & vexriscv)	schematic	4
Shawn Tan	ae18, aeMB, k68, DCPU16, T3RAS	verilog	4
Ulrich Riedel	68hc05, 68hc08, tiny64, tiny8	vhdl	4
ensilica	eSi-1600, eSi-1650, eSi-3200, eSi-3250	verilog	4
revaldinho	(opc1cpu & opc2cpu), opc3cpu, (opc5cpu, opc5lscpu & opc6cpu), opc7cpu/opc8cpu	verilog	4
Li Xinbing	r8051, arm9, riscv_rv3n, riscv_superscalar	verilog	4
Zoltan Pekic	sys_180x, sys0800, sys9080, sys_emz1001	vhdl	4
Steve Teal	1802-pico-basic, misc16, mx65, pumpkin	vhdl	4
Jan Adelsbach	nova1bach, pdp1bach, cdc160, rca110	verilog	4
Sébastien Bourdeaudu	lm32, milkymist, navre, artiq	verilog	4
Nicolae Dumitrache	next186, nextz80, oberon_sdram	verilog	3
Samuel Falvo II	kcp53000, kestrel-2, s16x4a	verilog	3
Aleksander Osman	ao486, ao68000, aor3000	verilog	3
Martin Schoeberl	jop, leros, patmos	vhdl, scala	3
Brad Parker	cpus-caddr, cpus-pdp8, cpus-pdp11	verilog	3
Hans Tiggeler	cpu86, recore54, uTTA	vhdl	3
Tommy Thorm	fpgammix, yari, yarvi	verilog, sys	3
Jose Ruiz	ion, light52, light8080	vhdl	3
James Brakefield	lem1_9, lem4_9ptr, rois24_24, alt-risc, alt-stk/acc, alt-430, alt-11, alt-x86, alt-780, quad_isa, quad_iw, lem16_18, the12X_12uP	vhdl	3
Lazaridis Dimitris	mips_fault_tolerant, mipsr2000, mips_enhanced	vhdl	2

Most Clones	94 risc-v entries at https://riscv.org/exchange/cores-socs/, many duplicates ©2023 James Brakefield		
risc-v	f32c, kcp53000, reonv, riscv_bonfire, riscv_clarvi, riscv_GRVI, riscv_lowrisc, riscv_microsemi, riscv_orca, riscv_picorv32, riscv_potato, riscv_pulpino, riscv_rocket, riscv_rv01_core, riscv_rv12, riscr1, riscv_shakti, riscv_sifive, riscv_sodor, riscv_taiga, riscv_urv-core, riscv_vexriscv, riscv_vhdl, riscv_zscale,vexrixcv, vscale, yarvi	system verilog	138
MIPS	32-bit_MIPS, aor3000, edge, hf-risc, f32c, ion, mais, minimips, mips_fault_tolerant, mips32, mips32r1, mips789, mipsr2000, mipsfpga, oops, plasma, r4000, sweet32, ucore, yacc, yari, yellowstar, ztachip		41
6502	6502_verilog, 6502vhdl, af65k, ag_6502, apple2fpga, bc6502, c65gs, cpu6502_true_cycle, fpga-64, free6502, lattice6502, m65, m65c02, mcl65, pet_fpga, t65, t6507lp, verilog_6502		19
PIC16	altium/TSK165x, cqpic, free_risc8, jmr16f84, m16c5x, minirisc, p16c5x, pic_coonan, ppx16, recore54, risc16f84, risc5x, risc8		14
openrisc	altor32, altor32_lite, minsoc, **mor1kx**, or10, **or1200**, or1200_hp, or1200_soc, or1200mp, or1k_soc, or1k-cf, or1knd		12
x86	ao486, cpu86, mcl86, next186, next186_soc, rtf8088, s80186, sp-i586, sub86, v586, zet86		11
8051	8051, altium/TSK51x, dalton_8051, light52, mc8051, mcl51, oms8051mini, pulserain, r8051, t51, turbo8051		11
avr	avr_core, avr_hp, avt_sauerman, avr8, avrtinyx61core, ax8, cpu_lecture, navre, pavr, riscmcu		10
z80	altium/TSK80x, a-z80, nextz80, reverse=u16, socz80, t80, tv80, wb_z80, y80e, z80soc		10
68000	ao68000, aoocs, k68, mc68kods, minimig, rf68000, rtf68ksys, suska-III, tg68, v1_coldfire		10
microblaze	aeMB, an-noc-mpsoc, mblite, mb-lite-plus, microblaze, myblaze, openfire_core, openfire2, secretblaze		9
6800	hd63701, system68, system6801, 68hc05, df6805, system05, 68hc08		7
picoblaze	copyblaze, mike_pico6, nanoblaze, pacoblaze, picoblaze, riscuval, wb4pb		7
SPARC	leon, mips_enhanced, openpiton, s1_core, sparc64soc, sparcv8coprocessor, temlib		7
ARM7	amber, arm4u, oks8, storm_core, zap		5
8080	am9080, cpu8080, ep8080, light8080, t80		5
6809	6809_6309, system09, mc6809e, rtf6809		4
PDP-11	pdp11-34verilog, pdp2011, pop11-40, w11		4
PDP-8	pdp8, pdp8l, pdp8verilog		3
MSP430	msp430_vhdl, neo430, openmsp430		3
other clones	1802, 4004, 3X 68HC11, 8085, 9900, AGC, c2650, CARDIAC, COP400, Cray1, DLX, MCS-48, MMIX, N32032, NOVA, PDP-1, PDP-10, PIC12, PIC14, PIC18, Saturn HP calculator uP, 2X SH-2, Z8, EMZ1001A		26
total			218

cat	by category	1809 topics as of 9/19/2024
RISC	"https://github.com/topics/risc-v"	222
accum		80
RISC		
CISC		28
accum		
RISC		
accum		
CISC		
RISC		
RISC		
accum		
accum		
CISC		
accum		
CISC		

Most Numerous Original Processor Type ©2023 James Brakefield			
RISC	a2z, aizup, altium/TSK3000A, alwcpu, atlas_2k, atlax_core, ba22, c-nit, c0or1k, c16too, carpe, cole_c16, dcpu16, dgb16, diongenes, dlx, eco32, edu_3bus_architecture, eight_bit_uc, embedded_risc, erp, fisa32, fisa64, fluid_core, gumnut, hicovec, hpc-16, iDEA, jam, jane_nn, jpu16, klc32, kraken2, latticemicro32, lc-2, lxp32, manik, marca, microcpu, micoriscii, mips_16, mist1032isa, moxie, mproz, myrisc1, natalius_8bit_risc, ncore, niloofar1, nocpu, oberon_sdram, oldland-cpu, open8_urisc, p8x32_propeller, patmos, potoato, qrisc32, qs5-rible, raptor64, risc_16bit, risc_core_i, risc0, risc-16, risc5, riscff, riscompatible, risc-processor, rise, rois24_24, s6soc, sayeh_processor, scarts, scott_cpu, spartanMC, suslik, sxp, table888, theia_gpu, thor, tiny64, tinycpu, totalcpu, ucode_cpu, ucos, up1232, xr16, cole_c16, diogenes, dragonfly, eco32, edge, eight_bit_uc, erp, fpgammix, hicovec, hpc-16, jam, manik, marca, myrosc1, raptor64, risc0, risc5, vexriscv, vscale, xgate, xr16, xtensa, xthundercore, xucpu, xulalx25soc, yasep, zipcpu			158
accumulator	agcnorm, blue, c88, classic_HP_calculator, hmta, inst_list_processor, lem1_9, lem1_9min, lem16_18min, lem4_9, lem4_9ptr, leros, leros32, lwrisc, mano_machine, mcpu, micro8a, micro16b, morell_cpu, mycpu, nod4, popcorn, rtf65002, t180-cpu, td4, tiny8, tisc, usimplez			80
forth/stack	4stack, 8bit_chapman, b16, cpu16, dataflow_chapman, dfp, e16, eP16,ep24, ep32, eric5, f18a, f21, fc16, fefff, forth_kf532, forth-cpu, frisc-3, gullwing, ignite_ptsc, J1, J1a, J1a32, J1b, J1b_16, j1sc, jop, kestrel-2, microcore, misc_halverson, msl16, myforthprocessor, nc4016, nige_machine, nybbleForth, p16, p16b, p24e, rtx2000, sc20, sod32, ssbcc, stundurd_fmite, tf2216yafc, x32, xpu, yafc, zpu, zpuino			51
other	lutiac, c16, ensilica, octavo, lemberg, vtach, bobcat, uTTA, x32			9
total				298

Outstanding Documen	Qualificatons: great web page, build files for multiple FPGA famiilies, resource utilization & Fmax, documentation and tool chain		
leon3	Sparc, Jiri Gaisler and company, Wikipedia entry		
microblaze	xilinx.com: part of Xilinx IP, proprietary, open source variants available, Wikipedia entry		
mister	retroRGB.com & github.com/MiSTer-devel & misterfpga.org: dedicated to retro gaming on an FPGA		
neo430	MSP430, Stephan Nolting		

neorv32	Risc-V, Stephan Nolting		
nios2	was altera.com now intel: proprietary, open source variants available, Wikipedia entry		
noel-v	Risc-V, Jiri Gaisler and company		
PicoBlaze	Ken Chapman, Wikipedia entry		
risc-v	riscv.org: long list of risc-v cores in development; academic & commercial, out of Berkeley, Wikipedia entry		
https://opencores.org/	largest list of open source microprocessors, web links, quality varies		
https://github.com/jim	largest list of open source microprocessors, web links, quality varies, annual updates		

Implemented using Scala/SpinalHDL (use Scala version 2.12.n)	**https://nlnet.nl/events/20240411/index.html** ©2024 James Brakefield		
cdc160	https://github.com/jadelsbach/cdc160		
cosmacELF	https://hackaday.io/project/169486-fpga-cosmac-elf		
J1 CPU in Scala/Spinal H	https://github.com/SteffenReith/J1Sc		
lipsi	https://github.com/schoeberl/lipsi		
nop	https://github.com/NOP-Processor/NOP-Core		
opc_spinal	https://justanotherelectronicsblog.com/?p=543		
patmos	https://github.com/t-crest/patmos	proj files	
riscv_boom	https://github.com/riscv-boom/riscv-boom		
riscv_microrv32	https://github.com/agra-uni-bremen/microrv32		
riscv_naxriscv	https://github.com/SpinalHDL/NaxRiscv		
riscv_sodor	https://github.com/ucb-bar/riscv-sodor		
riscv_vexriscv	https://github.com/SpinalHDL/VexRiscv	full RISC-V implementation with Fmax, LUTs & DFFs	
riscv_vexriscv	https://github.com/SpinalHDL/SaxonSoc	multi-core SOC of vexriscv	
riscv_zscale	https://github.com/ucb-bar/zscale		
others via search on: "github scala spinalHDL cpu"			

Implemented using Digital schematic tool https://github.com/hneemann/Digital/ ©2024 James Brakefield				
baby	https://github.com/jeceljr/baby8			
ben_eater_8bit	https://github.com/hneemann/Digital/discussions/897			Digital schematic, Ben Eater uP
cbox16	https://github.com/EngineersBox/CBox16-Processor			ARMv7 / MIPS IV hybrid ISA microarchitecture
drv16/digitalcpuzoo	https://github.com/jeceljr/digitalCPUzoo	mcpu, ncpu/ncpu16, drv16		four distinct uP, also wrappers for three risc-v u
digital_up	https://github.com/hneemann/Digital/ https://github.com/hneemann/Assembler			uP implemented as schematic
drv16	https://github.com/jeceljr/digitalCPUzoo			educational, LUT count comparisons to picorv3
moncky	https://gitlab.com/big-bat/moncky			intended as educational, all original
pdp-8x	https://github.com/mengstr/PDP8-X/			Digital schematic, TTL
phinix_cpu_dsgn	https://github.com/martandrMC/cpu-design			Digital schematic editer
rj32	https://github.com/rj45/rj32			Digital schematic, 16-bit data paths, micro-code
rjsc5	https://github.com/rj45/rjsc5			originally TTL/schematic, beginner's project, no
rssb_cpu	https://gitlab.com/Houkime/rssb-cpu			Digital schematic, very minimal
simple_ttl_cpu	https://github.com/monsonite/Simple-TTL-CPU			Digital schematic, TTL & 3 layer breadboard
stacks-16-bit	https://github.com/rcrist/Stacks-16-Bit_Breadboard_Processor			Digital schematic, version of sweet-16
suite-16	https://github.com/monsonite/Suite-16			
PDF schematics				schematic of TTL parts
isetta	https://hackaday.io/project/190345-isetta-ttl-computer			
magic-1	http://www.homebrewcpu.com/architecture.htm			
swssp	https://www.ipo.gov.uk/p-ipsum/Case/ApplicationNumber/GB1420325.1			
***.1 schematics**				
mproz	http://www.bitlib.de/pub/xproz/			
osu8	https://www.pjrc.com/tech/osu8/index.html			
xproz	http://www.bitlib.de/pub/xproz/			
others via search on: "github schematic cpu"				

emulations implemented in ZIG ©2025 James Brakefield			
6502	https://github.com/timsavage/zemu6502	Tim Savage	2024
CHIP-8	https://github.com/0xdeb7ef/emu		2024
kc85 (z80 clone)	https://github.com/floooh/kc85.zig	Andre Weis	2024
lr35902 gameboy	https://github.com/tsunaminoai/game-boy	Ben Craton	2024
risc-v	https://github.com/Ronsor/riscv-zig	Ronsor	2021
risc-v	https://github.com/ringtailsoftware/zig-minirv32	Toby Jaffey	2025
sh4	https://github.com/Senryoku/Deecy	Senryoku	2025
sm83 (z80 like)	https://github.com/bartek/zigboy	Bartek Ciszl	2025
z80 & ZIG gotchas	https://github.com/floooh/chipz	Andre Weis	2025
z80	https://github.com/codersauce/zig80	CoderSauce	2024
x86	https://github.com/hchaumont/zig-8086	Hans Chaur	2024
x86 kernel (dated)	https://github.com/jzck/kernel-zig	Jack Halford	2023
Cross-compilation	https://zig.guide/build-system/cross-compilation/		

Implemented using Tang Nano 9K or 20K FPGA board ©2024 James Brakefield			
	https://github.com/yuri-panchul/basics-graphics-music https://habr.com/en/articles/823638/ music gen, misc topics		
tms9900	F18A is a gaming box, conflicts with Chuck Moore's F18A, uses Tang Nano 9K for F18a Clone processor		
riscv_n_chip8	simple RV32I on Tang Nano 9K, video shows Tang Nano & LCD doing Chip-8 games		
sbc6502	projects for cmod-a7, de10, tang9K, tang20K, tang25K; written from scratch, uses 8-digit display board		
z80 socket with SOC	https://github.com/jabadiagm/MSXgoauld_tn20k_retro MSX		
SAP	https://github.com/Fede-26/sap-1-fpga		
https://learn.lushaylabs.com/tang-nano-9k-first-processor/			

Commercial product	©2023 James Brakefield		Known For
Synopsys ARC	Targets ASIC designs, very little public information: en.wikipedia.org/wiki/ARC_(processor)		CAD tools
TSK3000A	32-bit RISC, Altium core, free with tools		CAD tools
ESi-1600, Esi-3200	Ensilica 16-bit & 32-bit , targets both FPGAs & ASICs: en.wikipedia.org/wiki/ESi-RISC		design services
Freedom E & U series	SiFive has ASIC RISC-V cores		design services
Manik	32-bit RISC, Nitech core, free source		design services

MC8051	8051 clone from Oregano Systems, source is free		design services
ZPU	opensource.Zylin, "ZPU the worlds smallest 32 bit CPU with GCC toolchain"		design services
latticemicro8 & 32	8 & 32-bit Lattice Semiconductor cores, open source		FPGA chips
MicroBlaze	32-bit Xilinx core, free with tools, clones available		FPGA chips
NIOS II	32-bit Altera core, free with tools		FPGA chips
PicoBlaze	8-bit Xilinx core, free with tools, clones available		FPGA chips
Eric-5	Entner Electronics, 9-bit Forth		FPGA design
BA21-25	32-bit RISCs by CAST Inc., targets ASICs		IP
ColdFire	68000 clone by ip-extreme, free for Altera Cyclone 3		IP
MCL86	Low LUT count (308 LUTs, 4 BlkRAM) 8088 from MicroCore Labs		IP
OpenRISC 1000	32-bit from people at Beyond Semiconductor who target ASICs with BA12-25 series		IP
S8051XC3	highest performance 8051 clone, by CAST Inc., targets ASICs		IP
LEON	SPARC clone from Aeroflex Gaisler, LEON 2 & 3 source is free		SPARC IP
ARM Cortex A53	Incorporated into Altera Stratix X and Xilinx Zynq US+		uP IP
ARM Cortex A9	Incorporated into Altera Cyclone V and Xilinx Zynq		uP IP
ARM Cortex M0	Targets FPGAs and very low cost 32-bit processors		uP IP
ARM Cortex M1	Targets FPGAs, available for Actel, Altera & Xilinx		uP IP
ARM Cortex M3	Incorporated into MicroSemi SmartFusion1 & 2		uP IP
RISC-V	several ASIC versions, atleast 50 open source soft core versions		publications

FPGA based Legacy Processor Emulation	http://en.wikipedia.org/wiki/Home_computer_remake		
	Most of the 8-bit microprocessors have RTL versions (see Most Clones), these here tend to be Retro projects		
Sun Sparc	http://en.wikipedia.org/wiki/LEON		
Cray-1 (cray1)	www.chrisfenton.com/homebrew-cray-1a/		
PDP	http://www.aracnet.com/~healyzh/pdp_fpga.html		
PDP-8	http://www.emeritus-solutions.com/pdp8onanfpga.htm		
PDP-11/70 (w11)	http://opencores.org/project,w11		
Amiga (68000)	http://en.wikipedia.org/wiki/Minimig		
MIST(minimig)	http://harbaum.org/till/mist/index.shtml		
MiSTer	https://boogermann.github.io/Bible_MiSTer/getting-started/introduction/		
m32632(N32032)	http://cpu-ns32k.net/index.html		
jcore_aka_sh2	http://j-core.org/		
SWTPC 6809	http://members.optusnet.com.au/jekent/system09/		
Color Computer	http://8littlebits.wordpress.com/category/coco3fpga/		
Commodore Pet	http://www.skibo.net/projects/pet2001fpga/		
generic	http://fpgaarcade.com/		
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Other Insights ©2023 James Brakefield

Clean template VHDL code

Scott Baker: PDP8-soc, PDP11-soc & Nova-soc: Top level port maps of periphals & memory

Steve Teal: 1802-pico-basic, pumpkin, misc16 & mx65: Top level port map decomposition

For small micro-controllers with small memory needs, some soft cores are competitive with ASIC cores

For a good figure of merit must keep LUT count low and fmax high

Floating-point will add at least 2K LUTs, except Altera now provides 32-bit floating-point in their series-10 DSP blocks

RISC-V has many implementations both FPGA & ASIC

For current status see their website (riscv.org/risc-v-cores/)

Both microBlaze and NIOS-2 have very good figure-of-merit numbers

If RAM area removed from ARM Cortex A9 ASIC, it has the highest figure of merit

GRVI-phalanx (riscv) now outperforms NIOS2 & microBlaze!

There are "wrinkles" in CAD tools:

For ISE, Quartus and Vivado: success in inferring RAM and multipliers varies across vendor families & between vendors

For ISE, Quartus and Vivado: Fmax can vary in unpredicable ways across vendor families & between vendors

The tools vary in their reporting of LUTs used for route-thrus

Non-inferred register files result in high DFF counts

Two high performance ideas that work

Multi-threading or pipeline "barrel" increase performance without adding complexity: octavo, hive, or1200_hp

State machine with program as logic for programs under 200 instructions: iDEA, Lutiac, C-to-Hardware (HLS)

No one architecture dominates in performance, size or speed

Many clone and legacy designs have relatively poor figure of merit, usually due to high LUT counts

SoC designs usually have higher LUT counts, often 2X greater

For usable original designs the numbers are RISC is 47%, stack 20%, accumulator 15%, other 11%, OpenRisc 7%

Some opencores "alpha" phase designs are system designs where core is stable and working

For those barrel designs with adjustable barrel length, intermediate barrel length gives best KIPS/LUT (sample size of 2)

Only 28nm part families in webpack tools are Cyclone V, Spartan-7, Atrix-7, Kintex-7 and Zynq-7

Only 16nm part family in webpack tools is Zynq-US+

No parts from highest performance FPGA families available in "webpack" tools (Arria X, Stratix X, Virtex-US+)

Designs with floating point			©2023 James Brakefield		
	cray1, fisc, fpgammix, odess & s1_core are 64-bit, pdp2011 & oc54x 16-bit, others are 32-bit uP		fltgpt?	LUT cnt	LUT type
ARM_Cortex_A9	ASIC, dual issue, includes fltg-pt & MMU & caches		std	4500	area equivalent
bjx1	128-bit memory path, based on SH-4		std		6LUT
cray1	homebrew Cray1, double precision		std	13463	6LUT
flexgrip	eigth cores, reviews comparable projects , vivado fltg-pt IP, benchmarks, wikipedia: GPGPU		std	128000	6LUT
fisc	Flexible Instruction Set Computer, caches, VHDL & System Verilog versions, altera dsgn		std	5036	4LUT
fpgammix	clone of Knuth's MMIX, double precision		std	11605	ALUT
ks10	36-bit accum & 18-bit adrs		std	4427	6LUT
lemberg	upto 4 inst/clock		std	37459	4LUT
leon2	dated, with FPU		opt	5992	6LUT
leon3	customized for ~50 FPGA boards, with FPU		opt	11740	6LUT
m32632	National 32032 with fltg-pt, cache & MMU		std	10167	6LUT
minsoc	minimal OR1200, vendor neutral, has caches		std	4945	6LUT
oberon_sdram	risc5 modified to use DRAM, has caches, serial multiply		std	2820	6LUT
odess	Altera proj, Multicore, P&R results at opencores, 37-bit adr, quad issue, caches, 32-64-128 fltg-pt		std	32978	ALUT
or1200_hp	1 to 4 slot barrel version of OR1200		std	5602	6LUT
or1200mp	multiprocessor variant, single core		std	4960	6LUT
pdp2011	clone of PDP11/34		std	5060	6LUT
piropiro	five variants		std	7491	6LUT

risc5	minimalist Wirth, part of Project Oberon 2013, fast multiply		std	2441	6LUT
riscv designs	RISC-V has several op-code extensions including floating-point		opt		
s1_core	reduced version of OpenSPARC T1		std	52845	6LUT
sp-i586	gate level dsgn, vivado project also		std	32144	6LUT
temlib	copywrite: experimental use, options for fltg-pt, pipeline, mul & div configuration		opt	3730	6LUT
thor	Thor-2: L1 & L2 caches, GP float & vector regs, plans for 64-bit version (Thor-II) & 2M LUTs			90000	
microblaze	Xilinx RISC, fltg-pt, cache & MMU options		opt		
nios2	Altera RISC, fltg-pt, cache & MMU options		opt		
Altera X series DSP	Arria X & Stratix X provide single precision floating-point add & multiply		std		area equivalent
Altera IP	variable exponent and mantissa size, sqrt , exp/log & trig avail, no denorm support		IP		
several	OpenCores Arithmetic cores		IP		
VHDL 2008	variable exponent and mantissa size, sqrt avail, denorms opt, rounding modes opt		IP		
Xilinx IP	variable exponent and mantissa size, sqrt & exp/log avail, no denorm support		IP		

Designs with cache(s) and/or MMU					©2023 James Brakefield	
	fisc & odess are 64-bit, w11 is 16-bit, others are 32-bit uP					
	Most 32-bit "non-educational" uP have cache & MMU support using block RAM; and support DRAM		cache	MMU	LUT cnt	LUT type
amber	ARM7, no MMU, shared cache		merged	no	6409	6LUT
aor3000	MIPS, MIPS R3000A compatible, has MMU		yes	yes	5307	6LUT
eco32f	RISC, pipelined version of the eco32 CPU		yes	yes	3845	6LUT
fisc	RISC, Flexible Instruction Set Computer		yes		5036	4LUT
latticemicro32	RISC, optional data & inst caches		optional		2166	4LUT
leon2	SPARC, large config file, rad-hard asic version		optional		5992	6LUT
leon3	SPARC, large config file, customized for ~50 FPGA boards, smallest version, no fltg-pt		optional		2920	6LUT
microblaze	xilinx uBlaze, 70 configuration options, smallest configuration		optional	optional	546	6LUT
mor1kx	OpenRISC, considered best openrisc design, lots of configuration parameters		optional	optional	2718	6LUT
nios2	Altera NIOS II, optional data & inst caches, optional MMU		optional	optional	584	ALUT
odess	Altera proj, Multicore, P&R results at opencores, 37-bit adr, quad issue, caches, 32-64-128 fltg-pt		yes	yes	32978	ALUT
oldland-cpu	RISC, has caches & MMU		yes	yes		ALUT
riscv_sifive	RISC-V, there are many RISC-V open source designs, most with caches & MMU		yes	yes	14119	6LUT
temlib	SPARC, copywrite: experimental use		yes		2579	6LUT
ucore	MIPS, MMU & caches		yes	yes	2469	6LUT
v586	x86, MMU & caches, branch cache		yes	yes	22282	6LUT
w11	PDP11, Boots UNIX, has MMU & cache, PDP11/70		yes	yes	1760	6LUT
zap	ARM7, ARMv4T & Thumbv1		yes	yes	7558	6LUT

Highly micro-coded or serial arithmetic - e.g. area over speed					©2023 James Brakefield	
			clks/ins	KIPS/LUT	LUT cnt	LUT type
fpgammix	clone of Knuth's MMIX (micro-coded & huge LUT count?)		4	3	11605	ALUT
light8080	Lightweight 8080 compatible core		9	59	154	6LUT
mcl51	MicroCore Labs AKA Ted Fried		8	24	312	6LUT
mcl65	MicroCore Labs AKA Ted Fried, cycle exact		4	50	252	6LUT
mcl86	MicroCore Labs AKA Ted Fried, matches original 8086 timing		20	20	308	6LUT
Nios2/E	serial arithmetic variant		~9	62	730	ALUT
riscv_serv	serial implementation of RISC-V					
bit-serial						

Some of the designs with ROM or RAM initialization		©2023 James Brakefield
ROM/RAM inferred, MIF or other initialization		P&R on:
altor32	automatic use of either Altera LPMs or Xilinx primitives, no initialization	A&X
amber	generic_sram_byte_en.v: inferred byte enable RAM, also spartan-6 BRAM init	A&X
ao68000	MIF microcode file, see line 2130 of ao68000.v	A2
atlas_core	case statement in BOOT_MEM.vhd	X&A
c16	bit_vector constants in mem_conten.vhd, see memory.vhd: RAM4_S1_S1	S3
classic_HP_calc	three array ROM constants	K7
cray1	cray_rom.txt: xilinx MIF, see cray_sys_top.v line 111	K7
dalton_8051	constant in i8051_rom.vhd	K7
diogenes	MIF files , see pmem.vhd line 116	K7
eco32	large case based state "microcode" machine: cpu.v, no inferred RAM for Altera	X&A-
eP16, eP8080	Lattice memory IP, with init.	X
fpgammix	initmem.data: see progmem.v	A2
gumnut	source reads *.dat files, both VHDL & Verilog	A&X
gup	gucode.mif: see gucode.vhd line 89	A2
hd63701	*.i include files contain table definitions: see HD63701_MCROM.v	S3&6
lem1_9min	lem1_9min.vhd has array constant, for Quartus to infer block RAM, must be fully registered	X&A
leros	leros_rom.vhd: case statement with others	X&A
light52	light52_ucode_pkg.vhd has microcode table generator	C2&X
light8080	light808.vhdl has signal array init (instead of constant init)	X&A-
lwrisc	init_file.mif: see ramxxx.v files	A2
m1_core	*.vh initialization file	X&A
m16c5x, p16c5x	COE files	X&A
m32632	Verilog readmemf text file	K7,C4
marca	Altera memory IP & MIF files	A2
natalius_8bit_risc	inferred, MEM file	X
nige_machine	MIF files	K7
pdp8l	MIF files	C3
plasma	INIT text	K7
risc0	INIT text	K7
risc5	MEM file	X&A
rtf68ksys	case statement in bootrom.v	S3
system68	INIT in xilinx RAMB4_S8	S3
t51	case table	K7&A2
z80soc	COE files, hex files, mif files	S3&C3