| _uP_all_soft folder | opencores or prmary link | status | author | style / clone | data size | inst size | FPGA | repor ter | com ents | LUTs ALUT | LUT? | mults | blk ram | F max | date | tool ver | MIPS /inst | clks/ inst | KIPS /LUT | ven dor | SOC | src code | #src files | top file | doc | tool chai n | fltg pt | Hav'd | max dat | max inst | byte adrs | # inst | adr mod | # reg | pip e lon | start year | last revis | secondary web link | note worthy | comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Small soft core uP Inventory** | | | **©2021 James Brakefield** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| **Opencore and other soft core processors** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| totalcpu | https://opencor | alpha | | RISC | 12+ | 12 | kintex-7-3 | James Brakef | | 229 | 6 | 1 | | 149 | ## | 14.7 | 0.33 | 3.0 | 71.7 | X | | verilog | 10 | cpu | | | N | | | | | | 16 | | 2007 | 2009 | | data width 12 bits and up, no data memory | |
| odess | https://opencor | stable | Dmytro Senyakin | RISC | 128 | 16 | stratix-5 | Dmytro Senya | | 32978 | A | 72 | 112 | 192 | ## | q17.1 | 4.00 | 1.0 | 23.3 | I | | system v | 27 | CoreOneV | Y | asm | Y | | 4G | 4G | | | 16 | | 2017 | 2017 | https://opencores | Altera proj, Multicore, P&R results at | 37-bit adr, quad issue, caches, 32-64-128 fltg-p |
| ARM_Cortex_A | https://develop | ASIC | ARM | ARM A53 | 64 | 32 | asic | Xilinx | | 6000 | A | | | 1500 | | | 2.00 | 0.5 | 1000.0 | | | asic | | | Y | yes | Y | | | | Y | | | | | https://en.wikipe | uses pro-rated LC area | dual issue, includes fltg-pt & MMU & caches |
| legv8 | https://github.c | stable | Warren Seto | AA64 | 64 | 32 | kintex-7-3 | James Brakef | | 731 | 6 | | 2 | 154 | ## | 14.7 | 1.00 | 1.0 | 210.5 | X | B | verilog | 2 | arm_cpu | Y | yes | N | | 4G | 4G | Y | 10 | | 32 | | 2018 | 2019 | | coursework, limited ISA, 3 versions | pipelined, inst: LDUR, STUR, ADD, SUB, ORR, A |
| kcp53000 | https://github.c | simulatior | Samuel Falvo II | risc-v | 64 | 32 | kintex-7-3 | James | trimm | 2455 | 6 | | | 175 | ## | 14.7 | 2.00 | 1.0 | 142.9 | X | B | vierilog | 4 | polaris | Y | yes | N | Y | 16E | 16E | Y | | | 32 | | 2016 | 2017 | https://github.cor | kestrel #3, basic 64-bit RISC-V | uses state machine RTL generator |
| cray1 | www.chrisfento | alpha | Christopher Fenton | CRAY1 | 64 | 16 | kintex-7-3 | James Brakef | | 13463 | 6 | 19 | 10 | 127 | ## | 14.7 | 6.00 | 1.0 | 56.6 | X | | verilog | 46 | cray_sys_ | Y | yes | Y | N | 4M | 4M | N | 128 | | 536 | | 2010 | 2015 | CRAY data sheets | homebrew Cray1 | 24-bit address registers |
| fisc | https://github.c | stable | Miguel Santos | RISC | 64 | 32 | cyclone-4 | James Brakef | | 5036 | 4 | | 21 | 66 | ## | q18.0 | 2.00 | 1.0 | 26.1 | I | | system v | 13 | fisc_core | Y | yes | Y | N | | | Y | 85 | 6 | 32 | 5 | 2018 | 2018 | http://www.archf | Flexible Instruction Set Computer | caches, VHDL & System Verilog versions, altera |
| fisa64 | https://github.c | beta | Robert Finch | RISC | 64 | 32 | kintex-7-3 | James Brakef | | 10404 | 6 | 12 | 7 | 65 | ## | 14.7 | 1.50 | 1.0 | 9.4 | X | | verilog | 1 | FISA64 | Y | | N | Y | | | | | | | | 2015 | 2015 | https://github.com/robfinch/Cores | need to use multi-cycle on mult | |
| fpgammix | https://github.c | stable | Tommy Thorn | MMIX | 64 | 32 | arria-2 | James Brakef | | 11605 | A | 8 | 10 | 94 | ## | q13.1 | 1.50 | 4.0 | 3.0 | I | | system v | 3 | core | Y | yes | Y | Y | 16Q | 16Q | Y | 256 | | 288 | | 2006 | 2014 | https://en.wikipe | clone of Knuth's MMIX | micro-coded |
| s1_core | https://opencor | stable | Fabrizio Fazzino etal | SPARC | 64 | 32 | kintex-7-3 | James Brakef | | 52845 | 6 | 8 | 59 | 56 | ## | v14.1 | 2.00 | 1.0 | 2.1 | IX | | verilog | 136 | s1_top | Y | yes | Y | N | 4G | 4G | Y | | | 32 | | 2007 | 2012 | https://en.wikipe | reduced version of OpenSPARC T1 | Vivado run |
| senior-sagn-1 | https://github.c | simulatior | Niranjan Ramadas | RISC | 64 | 32 | kintex-7-3 | James | way to | 135009 | 6 | 32 | | 75 | ## | 14.7 | 1.00 | 1.0 | 0.6 | X | | verilog | 28 | pipeline | | | N | Y | | | Y | 137 | | 32 | 4-8 | 2012 | 2012 | nrbramadas.appsy | university ASIC project, read PDF | 64-bit data paths, superscalar, branch analysis |
| classic_HP_cal | https://github.c | stable | Brian Nemetz | accum | 56 | 10 | kintex-7-3 | James Brakef | | 1750 | 6 | | 3 | 233 | ## | 14.7 | 0.17 | 10.0 | 2.2 | X | | vhdl | 15 | classichp_ | Y | | N | | 30 | 4K | N | 40 | | 7 | | 2012 | | | processor & ROMs for HP-55, 45 & 35 | includes LED display driver & UART, for Papilio |
| ks10 | http://www.tec | alpha | Rob Doyle | PDP10 | 36 | 36 | spartan-6-2 | Rob Doyle | | 4427 | 6 | | 15 | 50 | ## | 14.7 | 1.00 | 2.0 | 5.6 | X | | verilog | 39 | esm_ks10 | Y | yes | Y | N | | | N | | | | | 2011 | 2014 | | 36-bit accum & 18-bit adrs | ucf file, most tests pass |
| mb-lite_plus | http://www.late | stable | Huib Arriens | uBlaze | 32 | 32 | kintex-7-3 | James Brakef | | 244 | 6 | | 2 | 319 | ## | 14.7 | 1.00 | 1.0 | 1308.1 | X | B | vhdl | 34 | tumbl | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2010 | 2012 | | Delft Un. Of Tech. course work | use inferred RAM |
| microblaze | https://www.xil | proprietar | Xilinx | uBlaze | 32 | 32 | virtex ultra | Xilinx | | 563 | 6 | | 1 | 682 | ## | | 1.03 | 1.0 | 1247.7 | X | | proprietary | | | Y | yes | opt | | 4G | 4G | Y | 86 | | 32 | 3 | 2002 | | https://en.wikipe | MicroBlaze MCS, smallest configurati | 70 configuration options, MMU optional |
| riscv_GRVI-pha | http://fpga.org/ | beta | Jan Gray | risc-v | 32 | 32 | virtex-u-2 | Jan Gray | | 320 | 6 | | 1 | 375 | ## | v16.4 | 1.00 | 1.0 | 1171.9 | X | | proprietary | | | Y | yes | N | | 4G | 4G | Y | 45 | | 32 | 3 | 2015 | 2018 | https://www.yout | hand fitted & placed | "Hoplite" router, 1680 cores in XCVU9P |
| ARM_Cortex_A | https://develop | ASIC | ARM | ARM A9 | 32 | 16 | arrira V | altera | | 4500 | A | | | 1050 | | | 2.50 | 1.0 | 583.3 | | | asic | | | Y | yes | Y | | 4G | 4G | Y | 80 | | 16 | 10 | | 2012 | https://en.wikipe | uses pro-rated LC area | dual issue, includes fltg-pt & MMU & caches |
| mips-cpu | https://github.c | alpha | Jeremiah Mahler | MIPS | 32 | 32 | kintex-7-3 | James | added | 596 | 6 | | 1 | 244 | ## | 14.7 | 1.00 | 1.0 | 409.2 | X | | verilog | 15 | cpu | Y | yes | N | | 4G | 4G | Y | | | 32 | 5 | 2017 | 2017 | | Very early stage project, only implem | no outputs, missing im_data.txt |
| J1a32 | www.excamera | stable | James Bowman | forth | 32 | 16 | kintex-7-3 | James | DFF ex | 930 | 6 | | | 358 | ## | 14.7 | 1.00 | 1.0 | 384.4 | X | | verilog | 3 | j1 | Y | forth | N | | 64K | 64K | | 20 | | | 2 | 2006 | 2017 | | uCode inst, dual port block RAM | DFF used for 18 deep data & return stacks |
| riscv_vexriscv | https://github.c | beta | Charles Papon | risc-v | 32 | 32 | artix-7 | Charles Papo | | 481 | 6 | | | 346 | | | 0.52 | 1.0 | 374.1 | X | | scala | | smallest | Y | yes | | | 4M | 4M | Y | | | | | 2018 | https://riscv.org/2 | preformance #s for 8 configurations c | "Briey" is SOC variant |
| riscv_rudolv | https://github.com/bobbl | | Jörg Mische | risc-v | 32 | 32 | xcku3p-3 | Jörg Mische | | 545 | 6 | | | 200 | ## | | 1.00 | 1.0 | 367.0 | ALMX | | verilog | 4 | pipeline | Y | yes | N | | 4G | 4G | Y | | | 32 | 5 | | 2021 | | RISC-V processor for real-time system | 34 clock mult & divide |
| riscv_picorv32 | https://github.c | beta | Clifford Wolf | risc-v | 32 | 32 | xcku3p-3 | Cliffor | small | 761 | 6 | | | 769 | ## | v16.2 | 1.00 | 3.0 | 336.8 | X | Y | verilog | 1 | picorv32 | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2016 | 2020 | | mimimal features, soc options | designed for minimum LUTs |
| an-noc-mpsoc | https://opencor | mature | Alireza Monemi | uBlaze | 32 | 32 | **zu-2e** | James | area o | 968 | 6 | 3 | | 284 | ## | v20.1 | 1.00 | 1.0 | 293.5 | X | Y | verilog | 90 | aeMB_cor | Y | yes | N | | 4G | 4G | Y | | | | | 2014 | 2019 | | choice of lm32, aeMB, mor1kx or or1 | full system has network of cores |
| cpugen | https://opencor | stable | Giovanni Ferrante | RISC | 32 | 16 | kintex-7-3 | James Brakef | | 474 | 6 | | | 192 | ## | 14.7 | 0.67 | 1.0 | 271.8 | IX | | vhdl | 14 | cpu | Y | asm | N | N | | | | | | | | 2003 | 2009 | | x86 .exe generates VHDL RISC uP | using 16 bit example |
| nios2 | | proprietar | Altera | Nios II | 32 | 32 | stratix-3 | Altera | consis | 1020 | A | | | 290 | ## | q13.1 | 0.90 | 1.0 | 255.9 | I | | proprietary | | | Y | yes | opt | | 4G | 4G | Y | | | 32 | | 2004 | | | fltg-pt, caches & MMU options | Nios II/f: fastest version, DMIPS adj, 2.15 Core |
| xthundercore | http://forum.ga | alpha | majordomo | RISC | 32 | 16 | kintex-7-3 | James Brakef | | 793 | 6 | | 2 | 193 | ## | 14.7 | 1.00 | 1.0 | 243.7 | X | | vhdl | 49 | xtc | om | yes | N | Y | 4G | 4G | | | | 16 | 5 | 2014 | | http://www.xthur | Gadget Factory Forum thread | in debug, no comments, mostly in simulation |
| opc.opc7cpu | https://github.c | stable | revaldinho | RISC | 32 | 16 | kintex-7-3 | James Brakef | | 624 | 6 | | | 303 | ## | 14.7 | 1.00 | 2.0 | 242.8 | X | | verilog | 2 | opc7cpu | Y | asm | N | N | 1M | 1M | N | 32 | 5 | 16 | | 2017 | 2019 | https://revaldinho | OPC7 32bit, based on OPC5LS, more i | see hackaday One Page Computing Challenge |
| mblite | https://opencor | beta | Tamar Kranenburg | uBlaze | 32 | 32 | kintex-7-3 | James Brakef | | 941 | 6 | | 2 | 227 | ## | 14.7 | 1.00 | 1.0 | 240.9 | IX | | vhdl | 18 | core_wb | Y | yes | N | | 4G | 4G | Y | 86 | | 32 | | 2009 | 2017 | | not all instructions implemented | moved everything to work library |
| J1b_16 | www.excamera | stable | James Bowman | forth | 32 | 16 | kintex-7-3 | James | DFF ex | 1588 | 6 | | | 355 | ## | 14.7 | 1.00 | 1.0 | 223.4 | X | | verilog | 3 | j1 | Y | forth | N | | 64K | 64K | | 20 | | | 2 | 2006 | 2017 | | uCode inst, dual port block RAM | DFF used for 16 deep data & return stacks |
| riscv_orca | https://github.c | beta | VectorBlox | risc-v | 32 | 32 | stratix-5 | vectorblox | | 1082 | A | | ? | 244 | ## | 14.7 | 0.98 | 1.0 | 221.0 | I | | vhdl | 13 | orca | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2016 | | | *, /, fltg-pt all optional | RV32IM |
| riscv_dark | https://github.c | beta | Marcelo Samsoniuk | risc-v | 32 | 32 | kintex-7-3 | Marcelo Sam | | 1000 | 6 | | | 220 | ## | v20.1 | 1.00 | 1.0 | 220.0 | | | verilog | 4 | darkriscv | Y | yes | N | | 4G | 4G | Y | 45 | | 32 | | 2018 | 2021 | https://opencores | written in one night, low line count | builds for five fpga boards |
| mips_linder | https://www.sc | paper | Michael Linder | MIPS | 32 | 32 | kintex-7-3 | James Brakef | | 1100 | 6 | | | 238 | ## | 14.7 | 1.00 | 1.0 | 216.5 | | B | vhdl | 39 | a_mips | Y | yes | N | | 4G | 4G | | | | 32 | | 2007 | 2007 | | masters thesis | no LUT RAM, source code in PDF |
| riscv_vexriscv | https://github.c | scala | Charles Papon | risc-v | 32 | 32 | atrix-7-3 | Charles Papo | | 1399 | 6 | | | 295 | | | 1.00 | 1.0 | 210.9 | X | Y | scala | | full no cac | Y | yes | N | | 4G | 4G | Y | | | 32 | | | 2018 | https://riscv.org/2 | preformance #s for 8 configurations c | "Briey" is SOC variant |
| core_arm | https://opencor | beta | Konrad Eisele | ARM | 32 | 16 | kintex-7-3 | James Brakef | | 1239 | 6 | | 3 | 250 | ## | 14.7 | 1.00 | 1.0 | 201.8 | X | Y | vhdl | 151 | arm_proc | Y | yes | N | | 256M | 256M | | | | 16 | | 2004 | 2009 | http://cfw.sourcel | very large project with many unused | missing files found in sourceforge dir, very litt |
| hive | https://opencor | stable | Eric Wallin | stack | 32 | 16 | arria-2 | James Brakef | | 1420 | A | 8 | 24 | 283 | ## | q13.1 | 1.00 | 1.0 | 199.4 | ILX | | verilog | | hive_core | Y | | N | | | | N | 40 | | 10 | 8 | 2013 | 2015 | | 4 symetrical stacks, eight threads via | pipeline barrel |
| riscv_picorv32 | https://github.c | beta | Clifford Wolf | risc-v | 32 | 32 | kintex-U-3 | Cliffor | small | 761 | 6 | | | 454 | ## | v16.2 | 1.00 | 3.0 | 198.9 | X | Y | verilog | 1 | picorv32 | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2016 | 2020 | | mimimal features, soc options | LUTs & Fmax for Kintex, Virtex & Ultrascale+ |
| ensilica | http://www.ens | proprietar | ensilica.com | eSi-3200 | 32 | 16 | stratix-4 | ensilica | | 2200 | A | | | 200 | | | 2.00 | 1.0 | 181.8 | IX | | verilog | | eSi-3250 | Y | yes | | | 4G | 4G | Y | 104 | 10 | 16 | 5 | 2001 | 2016 | | verilog source included with license | room for 90 user inst, also as ASIC |
| f32c | https://github.c | beta | marko zec, vordah, Dar | risc-v/MIPS | 32 | 32 | atrix-7-3 | zec & vordah | | 1048 | 6 | 4 | 33 | 185 | ## | 14.7 | 1.00 | 1.0 | 176.5 | X | | vhdl | 50 | | Y | yes | N | Y | 4G | 4G | Y | 30 | | 32 | 5 | 2014 | 2019 | http://www.nxlab | MIPS or RISC-V ISA, Arduino support | https://www.youtube.com/watch?v=55MzMH |
| p-vex | https://github.com/tvana | | Thijs van As | VLIW | 32 | 128 | kintex-7-3 | James | bypass | 1660 | 6 | | 1 | 233 | ## | 14.7 | 1.00 | 1.0 | 140.1 | | | vhdl | 26 | system | Y | yes | N | | | | | | 73 | | 32 | 4 | 2005 | 2015 | http://www.vliw.c | 1, 2 or 4 issue VLIW, uses HP VEX too | probable degeneracy, LUT RAM for program m |
| sweet32 | https://opencor | alpha | Valentin Angelovski | MIPS | 32 | 16 | kintex-7-3 | James Brakef | | 1050 | 6 | 1 | | 142 | ## | 14.7 | 1.00 | 1.0 | 135.1 | X | B | vhdl | 2 | Sweet32_ | Y | yes | N | N | 4G | 4G | Y | 26 | | 16 | | 2014 | 2015 | | targets MACHXO2, no RAM | |
| propeller_p8x3 | https://www.pa | stable | Chip Gracey | RISC | 32 | 32 | kintex-7-3 | James Brakef | | 9498 | 6 | | 20 | 160 | ## | 14.7 | 1.00 | 0.1 | 134.8 | X | | verilog | 9 | top | Y | yes | | | | | | | | | | 2014 | | | eight propellers, clocking from ucf file | several FPGA card build files |
| sayuri_cpu | http://www.mo | stable | Toyoaki Sagawa | RISC | 32 | 32 | kintex-7-3 | James Brakef | | 1604 | 6 | | | 208 | ## | 14.7 | 1.00 | 1.0 | 129.9 | X | | vhdl | 13 | cpu01 | | | | Y | 4G | 4G | | | | 32 | | 2000 | 2000 | | dead weblink | high number of DFF |
| zipcpu | https://github.c | stable | Dan Gisselquist | RISC | 32 | 32 | kintex-7-3 | James Brakef | | 1687 | 6 | | 2 | 218 | ## | 14.7 | 1.00 | 1.0 | 128.9 | X | | verilog | 7 | zipcpu | Y | | N | N | 4G | 4G | Y | 35 | | 16 | 5 | 2015 | 2020 | www.librecores.o | ISA has chnaged, multiple instruction | http://zipcpu.com/zipcpu/2018/01/01/zipcpu- |
| aeMB | https://opencor | beta | Shawn Tan | uBlaze | 32 | 32 | kintex-7-3 | James Brakef | | 1018 | 6 | 3 | | 131 | ## | 14.7 | 1.00 | 1.0 | 128.5 | ILX | | verilog | 7 | aeMB_cor | Y | yes | N | | 4G | 4G | Y | | | | | 2004 | 2009 | | not 100% compatable | |
| mips789 | https://opencor | stable | Li Wei | MIPS | 32 | 32 | kintex-7-3 | James Brakef | | 1432 | 6 | | 1 | 171 | ## | 14.7 | 1.00 | 1.0 | 119.1 | IX | | verilog | 10 | mips_core | Y | yes | N | | 4G | 4G | Y | | | 32 | 5 | 2007 | 2014 | | supports most MIPSI instructions | |
| riscv_steel | https://opencores.org/pr | | Rafael Calcada | risc-v | 32 | 32 | **zu2-2** | James Brakef | | 1775 | 6 | | | 208 | ## | v19.2 | 1.00 | 1.0 | 117.4 | | | verilog | 21 | steel_top | Y | yes | N | | 4G | 4G | Y | | | 32 | 3 | | 2020 | https://github.cor | github version has vivado proj | under grad thesis |
| darkriscv | https://github.c | alpha | Marcelo Samsoniuk | risc-v | 32 | 32 | kintex-7-3 | James Brakef | | 1422 | 6 | | 1 | 167 | ## | 14.7 | 1.00 | 1.0 | 117.2 | X | | verilog | 2 | darksocv | Y | yes | N | | 4G | 4G | Y | | | 32 | 2 | 2018 | 2018 | https://blog.hacks | written in one night, low line count | readme is descriptive, uses cache |
| J1b | www.excamera | stable | James Bowman | forth | 32 | 16 | kintex-7-3 | James | DFF ex | 2612 | 6 | | | 302 | ## | 14.7 | 1.00 | 1.0 | 115.5 | X | | verilog | 3 | j1 | Y | forth | N | | 64K | 64K | | 20 | | | 2 | 2006 | 2017 | | uCode inst, dual port block RAM | DFF used for 32 deep data & return stacks |
| lxp32 | https://opencor | beta | Alex Kuznetsov | RISC | 32 | 32 | kintex-7-3 | James Brakef | | 850 | 6 | 3 | 1 | 196 | ## | 14.7 | 1.00 | 2.0 | 115.4 | AIX | | vhdl | 20 | lxp32u_to | Y | asm | N | N | 4G | 4G | Y | 30 | | 256 | 3 | 2016 | 2019 | https://lxp32.gith | register file in block RAM | vendor neutral source code, no div inst |
| jam | https://github.c | stable | Johan Thelin etal | RISC | 32 | 32 | kintex-7-3 | James Brakef | | 1396 | 6 | | | 159 | ## | 14.7 | 1.00 | 1.0 | 113.7 | X | | vhdl | 17 | cpu_sys | Y | | N | Y | 128K | 128K | | | | 32 | 5 | 2002 | 2014 | | serial multiply & divide | took out clock divider |
| risc-processor | https://github.c | stable | Jeff Bush | RISC | 32 | 32 | kintex-7-3 | James Brakef | | 1445 | 6 | | 6 | 161 | ## | 14.7 | 1.00 | 1.0 | 111.6 | X | | verilog | 22 | fpga_top | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2008 | 2019 | https://github.cor | two designs with same name | MIT course work? |
| octagon | https://opencor | beta | Jon Pry | MIPS | 32 | 32 | kintex-7-3 | James Brakef | | 3021 | 6 | 4 | 9 | 333 | ## | 14.7 | 1.00 | 1.0 | 110.2 | X | | vhdl | 46 | octagon | | asm | | | 4G | 4G | Y | | | 32 | | 2015 | 2015 | https://github.cor | 8 thread barrel processor, largely MIPS | compatible |
| tiny64 | https://github.c | stable | Ulrich Riedel | RISC | 32 | 32 | kintex-7-3 | James Brakef | | 874 | 6 | | | 189 | ## | 14.7 | 1.00 | 2.0 | 107.9 | X | | vhdl | 6 | tinyx | | | | | 64K | 64K | | 14 | | 8 | | 2004 | 2007 | | data size from 32 to 64 bits | micro-coded sub-ops |
| ion | https://opencor | mature | Jose Ruiz | MIPS | 32 | 32 | kintex-7-3 | James Brakef | | 1533 | 6 | | | 163 | ## | 14.7 | 1.00 | 1.0 | 106.0 | IX | | vhdl | 12 | mips_soc | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2011 | 2018 | https://github.cor | new version: moving to MIPS32r1 | new version not ready, keeping old numbers |
| ARM_Cortex_M | http://www.arm | proprietar | ARM | ARM M1 | 32 | 16 | virtex-5 | ARM | 65nm | 1900 | 6 | | | 200 | | | 1.00 | 1.0 | 105.3 | AIX | | proprietary | | | Y | yes | N | | 4G | 4G | Y | | | 16 | 3 | 2007 | | https://en.wikipe | ARM Cortex M0, M1 & M3 avail for FI | see xilinx Xcell64 |
| jam | https://github.c | stable | Johan Thelin etal | RISC | 32 | 32 | kintex-7-3 | James Brakef | | 1369 | 6 | | | 143 | ## | 14.7 | 1.00 | 1.0 | 104.2 | X | | vhdl | 17 | cpu | Y | | N | Y | 128K | 128K | | | | 32 | 5 | 2002 | 2014 | | serial multiply & divide | |
| eight32 | https://github.com/robins | | Alastair M. Robinson | accum | 32 | 8 | cyclone-4 | Alasta | appro | 1300 | 4 | | | 133 | | | 1.00 | 1.0 | 102.3 | | | vhdl | 17 | eighthirty | Y | yes | N | | 500M | 500M | Y | 28 | | 8 | | 2019 | 2020 | https://retroramb | 5-bit op-code & 3-bit reg # | full tool set, see github page for ISA descriptio |
| forth_kf532 | https://github.c | stable | Tarasov Ilia | forth | 32 | 6 | kintex-7-3 | James | no *.c | 1719 | 6 | 4 | 4 | 172 | ## | 14.7 | 1.00 | 1.0 | 100.3 | X | | vhdl | 1 | kf532 | N | | N | Y | 1K | 16K | | | | | | 2013 | 2013 | | no trace of source code on web | |
| ucore | https://opencor | stable | Whitewill | MIPS | 32 | 32 | kintex-7-3 | James Brakef | | 2469 | 6 | | 1 | 231 | ## | 14.7 | 1.00 | 1.0 | 93.5 | X | | verilog | 25 | ucore | Y | yes | N | | 4G | 4G | Y | | | 32 | 6 | 2005 | 2010 | | MMU & caches | |
| m1_core | https://opencor | beta | Fabrizo Fazzino, Albert | MIPS? | 32 | 32 | arria-2 | James Brakef | | 2101 | A | | | 190 | ## | q13.1 | 1.00 | 1.0 | 90.6 | IX | | verilog | 9 | m1_core | | yes | N | | 4G | 4G | Y | | | 32 | | 2007 | 2012 | | GCC target? | |
| mais | | stable | Rene Doss | MIPS | 32 | 32 | kintex-7-3 | James Brakef | | 2760 | 6 | 4 | 5 | 245 | ## | 14.7 | 1.00 | 1.0 | 88.7 | X | | vhdl | 22 | MAIS_soc | Y | yes | N | N | 4G | 4G | | | | 32 | 5 | 2013 | | use MIPS tools | register forwarding around ALU | license req'd for commercial use |
| risc5 | http://www.pro | beta | Niklaus Wirth | RISC | 32 | 32 | zu-2e | James Brakef | | 2001 | 6 | 4 | | 177 | ## | v20.1 | 1.00 | 1.0 | 88.3 | ILX | | verilog | 8 | RISC5 | Y | yes | Y | | 4G | 4G | | | | 16 | | 2013 | 2017 | http://www.astro | minimalist Wirth, part of Project Obe | 32x32 multiplier, wikipedia entry |
| openfire2 | https://opencor | beta | Antonio Anton | uBlaze | 32 | 32 | kintex-7-3 | James Brakef | | 1201 | 6 | 3 | 2 | 105 | ## | 14.7 | 1.00 | 1.0 | 87.4 | X | Y | verilog | 27 | openfire_s | Y | yes | N | N | 4G | 4G | Y | | | 32 | | 2007 | 2012 | | "FPGA Proven" | derived from Stephen Craven's OpenFire |
| mor1kx | https://github.c | stable | Julius Baxter | OpenRISC | 32 | 32 | kintex-7-3 | James Brakef | | 2718 | 6 | 3 | 3 | 217 | ## | 14.7 | 1.00 | 1.0 | 80.0 | X | | verilog | 48 | mor1kx | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2012 | 2018 | https://www.yout | lots of configuration parameters | considered best openrisc design |
| riscv_taiga | https://gitlab.co | stable | Eric Matthews | risc-v | 32 | 32 | zynq | | | 1551 | | | 1 | 123 | | | 1.00 | 1.0 | 79.3 | X | | system v | 46 | | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2017 | | | TAIGA: A new RISC-V soft-processor f | 33% smaller & 39% faster than LEON3 |
| hf-risc | https://opencor | stable | Sergio Johann Filho | MIPS | 32 | 32 | kintex-7-3 | James Brakef | | 1446 | 6 | | 4 | 115 | ## | 14.7 | 1.00 | 1.0 | 79.2 | X | | vhdl | 9 | spartan3e_n | Y | yes | N | N | 4G | 4G | Y | 41 | | 32 | | 2016 | | https://github.cor | MIPS I subset, no multiplier | |
| tarhi | https://github.c | alpha | Dagvadorj Galbadrakh | RISC | 32 | 32 | kintex-7-3 | James | everyt | 396 | 6 | | 1 | 123 | ## | 14.7 | 1.00 | 4.0 | 77.9 | X | | verilog | 4 | tarhi_controller | | | N | | 16M | 16M | N | 11 | | 4 | | 2013 | 2013 | | no doc, extremely small RISC | difficulty with timing, try 7.0ns |
| storm_core | https://opencor | beta | Stephan Nolting | ARM7 | 32 | 32 | kintex-7-3 | James Brakef | | 2312 | 6 | 3 | | 179 | ## | 14.7 | 1.00 | 1.0 | 77.4 | IX | | vhdl | 16 | core | Y | yes | N | | 4G | 4G | Y | | | 32 | 8 | 2011 | 2014 | | Storm Core (ARM7 compatible) | I & D caches not compiled |
| altor32 | https://opencor | stable | Ultra Embedded | OpenRISC | 32 | 32 | kintex-7-3 | James Brakef | | 2505 | 6 | | 5 | 192 | ## | 14.7 | 1.00 | 1.0 | 76.8 | ILX | | verilog | 16 | altor32 | Y | yes | N | Y | 4G | 4G | Y | | | | | 2012 | 2015 | https://opencores | simplified OpenRISC 1000 | xilinx S3 primitives |
| sc20 | http://www.for | proprietar | Brad Eckert | forth | 32 | 8 | virtex-6 | Brad Eckert | | 1977 | 6 | | | 150 | | | 1.00 | 1.0 | 75.9 | X | | proprietary | | | | | | | | | | | | | | | | PDF file, Forth Inc. | |
| myforthproces | https://opencor | stable | Gerhard Hohner | forth | 32 | 8 | SP-kintex7- | James Brakef | | 2959 | 6 | | 6 | 223 | ## | 14.7 | 1.00 | 1.0 | 75.3 | X | | vhdl | 58 | mycpu | Y | yes | N | | 64M | 64M | | 96 | | | | 2004 | 2012 | | DPANS'94 32-bit Forth, masters thesi | 25.15 Whetstones |
| aspida | https://opencor | stable | Sotiriou | DLX | 32 | 32 | kintex-7-3 | James | dated | 3586 | 6 | | | 257 | ## | 14.7 | 1.00 | 1.0 | 71.7 | X | | verilog | 10 | DLX_top | Y | yes | | | 4G | 4G | | | | | | 2002 | 2009 | | DLX | compiled sync version |
| riscv_clarvi | https://github.c | stable | Robert Eady | risc-v | 32 | 32 | arria-2 | James | Altera | 2616 | A | | | 178 | ## | q18.0 | 1.00 | 1.0 | 68.2 | I | B | system v | 7 | clarvi | Y | yes | N | | 4G | 4G | Y | | | 32 | 6 | 2016 | 2017 | https://www.cl.ca | educational simple RISC-V implement | doesn't make use of block RAM RTL |
| zpu | https://github.c | stable | Oyvind Harboe | forth | 32 | 8 | kintex-7-3 | James Brakef | | 1073 | 6 | 3 | | 283 | ## | 14.7 | 1.00 | 4.0 | 65.9 | X | | vhdl | 23 | zpu_core | Y | yes | N | | 4G | 4G | Y | 37 | | | | 2008 | 2009 | | zpu4: 16 & 32 bit versions, code size | ZPU the worlds smallest 32 bit CPU with GCC t |
| **leon3** | http://www.gai | stable | Jiri Gaisler, Jan Anders | SPARC | 32 | 32 | kintex-7-3 | Jiri Gaisler | | 2920 | 6 | | | 183 | | | 1.00 | 1.0 | 62.7 | AILX | Y | vhdl | 100s | leon3x | Y | yes | Y | | 4G | 4G | Y | | | 64 | 7 | 2003 | 2020 | https://en.wikipe | **customized for ~50 FPGA boards,** | **xls with utilization for all targets** |

| _uP_all_soft folder | opencores or prmary link | status | author | style / clone | data size | inst size | FPGA | repor ter | com ents | LUTs ALUT | LUT? | mults | blk ram | F max | date | tool ver | MIPS /inst | clks/ inst | KIPS /LUT | ven dor | SOC | src code | #src files | top file | doc | tool chai n | fltg pt | Hav'd | max dat | max inst | byte adrs | # inst | adr mod | # reg | pip e line | start year | last revis | secondary web link | note worthy | comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| risc0 | https://sourcefo | beta | Niklaus Wirth | RISC | 32 | 32 | kintex-7-3 | James | Brakef | 1186 | 6 | 4 | 6 | 110 | ## | 14.7 | 0.67 | 1.0 | 61.9 | X | | verilog | 8 | RISC0 | Y | yes | N | | 4G | 4G | | | | | 2011 | | | minimalist Wirth, education tool | |
| altor32_lite | https://opencor | stable | Ultra Embedded | OpenRISC | 32 | 32 | kintex-7-3 | James | Brakef | 1928 | 6 | | | 236 | ## | 14.7 | 1.00 | 2.0 | 61.3 | ILX | | verilog | 7 | altor32 | Y | yes | N | Y | 4G | 4G | Y | | | | 2012 | 2014 | https://openrisc.io | simplified OpenRISC 1000, no pipeline | xilinx S3 primitives |
| softpc | https://github.com/alreac | Michael S | Nios II | 32 | 32 | cyclone-10 | Micha | block | 613 | 4 | | 1 | 180 | | q17.1 | 1.00 | 5.0 | 58.9 | | | vhdl | 13 | nios2ee | Y | yes | opt | | 4G | 4G | Y | | 32 | | | 2019 | | nine variations in attempt to improve | 16-bit ALU |
| secretblaze | http://www.lirm | beta | Lyonel Barthe | uBlaze | 32 | 32 | spartan-3-4 | Lyonel | Barthe | 1563 | 4 | | | 91 | | i12.1 | 1.00 | 1.0 | 58.2 | X | | vhdl | 26 | sb_core | | yes | | | 4G | 4G | Y | 86 | | 32 | 5 | 2010 | 2012 | www.lirmm.fr/ADAC | | |
| openscale | http://www.lirm | stable | Lyonel Barthe | uBlaze | 32 | 32 | spartan-3-4 | Lyonel | Barthe | 1563 | 4 | | | 91 | | i12.1 | 1.00 | 1.0 | 58.2 | X | Y | vhdl | 26 | sb_core | | yes | | | 4G | 4G | Y | 86 | | 32 | 5 | 2010 | 2012 | www.lirmm.fr/AD | NoC secretblaze | data is for single secretblaze |
| or1k | https://opencor | stable | Julius Baxter, Stefan K | OpenRISC | 32 | 32 | kintex-7-3 | James | Brakef | 3299 | 6 | 3 | 3 | 189 | ## | 14.7 | 1.00 | 1.0 | 57.3 | IX | | verilog | 39 | mor1kx | Y | yes | N | M | 4G | 4G | Y | | | 32 | | 2001 | 2018 | https://opencores | no longer supported, see mor1kx | cappuccino ALU |
| latticemico32 | http://www.latt | stable | Yann Siommeau, Mich | LM32 | 32 | 32 | arria_2 | James | Brakef | 2166 | A | 4 | 30 | 149 | ## | q13.1 | 0.80 | 1.0 | 55.0 | LX | | verilog | 24 | lm32_cpu | Y | yes | N | Y | 4G | 4G | Y | | | 32 | 6 | 2006 | 2017 | https://en.wikiped | optional data & inst caches | Diamond3.10; see lm32 & misoc folders |
| yari | https://github.c | stable | Tommy Thorn | MIPS | 32 | 32 | kintex-7-3 | James | Brakef | 3610 | 6 | | 15 | 189 | ## | 14.7 | 1.00 | 1.0 | 52.3 | X | Y | verilog | 8 | top | | | | | 2M | 2M | | | | 32 | | 2004 | 2008 | | subset of MIPS R3000 | |
| mips32 | https://opencor | stable | Jin Jifang | MIPS | 32 | 32 | kintex-7-3 | James | Brakef | 3696 | 6 | | 8 | 192 | ## | v17.4 | 1.00 | 1.0 | 52.0 | X | | verilog | 17 | pipelinem | Y | yes | | | 4G | 4G | y | | | 32 | 5 | 2017 | | | vivado project | "classic MIPS" |
| oberon_sdram | http://projectob | beta | Nicolae Dumitrache | RISC | 32 | 32 | kintex-7-3 | James | Brakef | 2103 | 6 | | 1 | 104 | ## | 14.7 | 1.00 | 1.0 | 49.5 | X | | verilog | 16 | risc5 | Y | yes | Y | | 4G | 4G | | | | 16 | | 2013 | 2017 | | minimalist Wirth, part of Project Obe | modified to use DRAM, serial mult |
| moxielite | https://github.c | stable | Anthony Green | RISC | 32 | 32 | kintex-7-3 | James | Brakef | 3159 | 6 | 3 | | 152 | ## | 14.7 | 1.00 | 1.0 | 48.0 | X | | vhdl | 11 | moxielite_wb | | | | | 4G | 4G | Y | | | 16 | | 2009 | 2017 | https://github.com/atgreen/moxie-cores | | |
| table888 | https://github.c | alpha | Robert Finch | RISC | 32 | 16 | kintex-7-3 | James | Brakef | 5756 | 6 | 9 | 6 | 137 | ## | 14.7 | 2.00 | 1.0 | 47.6 | X | | verilog | 3 | table888 | bme | | | | 4G | 4G | Y | 130 | | 8 | | 2014 | 2016 | | 2016 version gives same reults as 201 | code for cache & mmu incomplete |
| s6soc | https://opencor | stable | Dan Gisselquist | RISC | 32 | 32 | spartan-6-3 | James | sparta | 2820 | 6 | 1 | 10 | 133 | ## | 14.7 | 1.00 | 1.0 | 47.3 | X | Y | verilog | 31 | toplevel | | | N | N | 4G | 4G | N | 20 | | 16 | 5 | 2015 | | | | uses ZIP CPU |
| riscv_potato | https://github.c | beta | Kristian Skordal | risc-v | 32 | 32 | kintex-7-3 | James | Brakef | 2467 | 6 | | | 116 | ## | 14.7 | 1.00 | 1.0 | 47.1 | X | B | vhdl | 24 | pp_core | Y | yes | N | N | 4G | 4G | Y | 30 | | 32 | | 2014 | 2020 | | risc-V interger only, no mult | "rocket-core" version at risc.org |
| coen_316_cpu | https://github.c | alpha | G.K Yvann Monny | RISC | 32 | 32 | kintex-7-3 | James | does r | 897 | 6 | | | 127 | ## | 14.7 | 1.00 | 3.0 | 47.0 | X | | vhdl | 8 | cpu_dp | | | N | | 32 | 32 | N | 20 | | 32 | | 2018 | 2018 | | MIPS based, simulation DO files, I&D | very small caches do not infer any RAM |
| qrisc32 | https://opencor | alpha | Viacheslav | RISC | 32 | 32 | arria-2 | James | Brakef | 3075 | A | 4 | | 144 | ## | q13.1 | 1.00 | 1.0 | 46.9 | I | | system v | 8 | qrisc32 | Y | yes | N | | 4G | 4G | Y | | | 32 | 4 | 2010 | 2011 | | qrisc32 wishbone compatible risc cor | for PhD thesis |
| eco32 | https://opencor | stable | Hellwing Geisse | RISC | 32 | 32 | kintex-7-3 | James | Brakef | 2339 | 6 | | 1 | 160 | ## | 14.7 | 1.00 | 1.5 | 45.5 | ILX | Y | verilog | 14 | cpu | Y | yes | N | | 512M | 256M | Y | 61 | | 32 | | 2003 | 2014 | homepages.thm.d | MIPS like, slow mul & div | |
| storm_soc | https://opencor | beta | Stephan Nolting | ARM7 | 32 | 32 | kintex-7-3 | James | Brakef | 3514 | 6 | 3 | 4 | 159 | ## | 14.7 | 1.00 | 1.0 | 45.2 | X | Y | vhdl | 40 | storm_top | Y | yes | N | | 4G | 4G | Y | | | 32 | 8 | 2012 | 2015 | | STORM SoC | cache & no peripherals |
| fisa32 | https://github.c | beta | Robert Finch | RISC | 32 | 32 | kintex-7-3 | James | Brakef | 3479 | 6 | 3 | 2 | 152 | ## | 14.7 | 1.00 | 1.0 | 43.7 | X | | verilog | 1 | FISA32 | Y | | N | Y | | | | | | 32 | | 2014 | 2014 | https://github.com/robfinch/Cores | | |
| temlib | http://temlib.or | stable | | SPARC | 32 | 32 | kintex-7-3 | James | Brakef | 2579 | 6 | | 32 | 111 | ## | 14.7 | 1.00 | 1.0 | 43.1 | X | | vhdl | 48 | mcu_simple | | | Y | N | 4G | 4G | Y | | | 64 | | 2013 | 2015 | | copywrite: experimental use | has caches |
| amber | https://opencor | stable | Conor Santifort | ARM7 | 32 | 32 | **zu-2e** | James | area o | 3145 | 6 | | 10 | 175 | ## | v20.1 | 0.75 | 1.0 | 41.8 | ILX | | verilog | 25 | a23_core | Y | yes | N | | 4G | 4G | Y | 80 | | 16 | 3 | 2010 | 2017 | https://en.wikiped | no MMU, shared cache | |
| vscale | https://github.c | stable | UC Berkeley | risc-v | 32 | 32 | kintex-7-3 | James | Brakef | 3072 | 6 | | | 127 | ## | 14.7 | 1.00 | 1.0 | 41.2 | X | | verilog | 23 | vscale_core | | | N | | | | | | | 32 | | 2016 | 2017 | | risc-v RV32IM vscale processor, depr | depreciated: not up to date (risc-v) |
| aquarius | https://opencor | stable | Thorn Aitch | SuperH-2 | 32 | 16 | **zu-2e** | James | area o | 2975 | 6 | 2 | 16 | 122 | ## | v20.1 | 1.00 | 1.0 | 41.0 | ILX | | verilog | 21 | top | Y | yes | N | | 4G | 4G | Y | | | | | 2003 | 2015 | http://0pf.org/j-c | clone of Hitachi SH-2 | project seems to have stalled |
| bst-cpu | https://github.c | stable | Yichun Ma | RISC | 32 | 32 | arria-2 | James | Brakef | 1439 | A | | 2 | 58 | ## | q18.0 | 1.00 | 1.0 | 40.2 | I | | verilog | 26 | sc_computer | | | N | | 4G | 4G | | | | 32 | | 2016 | 2016 | | learning, single cycle uP | |
| minimips | https://opencor | stable | Samuel Hangouet | RISC | 32 | 32 | kintex-7-3 | James | Brakef | 2939 | 6 | 8 | | 118 | ## | 14.7 | 1.00 | 1.0 | 40.1 | X | | vhdl | 12 | minimips | Y | yes | N | N | 4G | 4G | | | | 32 | 5 | 2004 | 2018 | | based on MIPS I | |
| cast_ba22 | http://www.cas | proprietar | CAST Inc | RISC | 32 | 16 | spartan-6 | CAST Inc | | 1800 | 6 | | 32 | 72 | | | 1.00 | 1.0 | 40.0 | X | | proprietary | | | Y | yes | | | 4G | 4G | | | | 32 | | | | http://www.cast-i | Cast has uP related IP | several versions, FPGA kits |
| riscv_lattice | https://www.lat | stable | Lattice Semi | risc-v | 32 | 32 | machXO3D | Lattice | Semic | 1507 | 4 | | 4 | 60 | ## | | 1.00 | 1.0 | 39.8 | L | Y | | | | Y | yes | N | | 4G | 4G | Y | | | 32 | 5 | | 2021 | | RV32I ISA, 5 stage pipeline, configured & generated using Lattice Propel | |
| plasma | https://opencor | stable | Steve Rhoads | MIPS | 32 | 32 | kintex-7-3 | James | Brakef | 2462 | 6 | | 3 | 97 | ## | 14.7 | 1.00 | 1.0 | 39.5 | X | | vhdl | 22 | plasma | Y | yes | N | | 4G | 4G | Y | | | 32 | 2 | 2001 | 2016 | http://plasmacpu. | wide outside use, opencores page has | list of related publications |
| aor3000 | https://opencor | beta | Aleksander Osman | MIPS | 32 | 32 | **zu-2e** | James | area o | 4259 | 6 | 4 | 8 | 167 | ## | v20.1 | 1.00 | 1.0 | 39.1 | IX | | verilog | 19 | aoR3000 | Y | yes | N | | 4G | 4G | Y | | | 32 | 5 | 2014 | 2015 | | MIPS R3000A compatible, has MMU | moved declarations forward |
| supersmall | http://www.eec | stable | Michael Ritchie | RISC | 32 | 32 | stratix_3 | Michael | Ritch | 207 | A | | 2+8 | 126 | ## | q9.0 | 1.00 | 16.0 | 38.1 | I | | verilog | | | | | | | | | | | | | | 2005 | 2009 | | 2-bit serial, Mostly MIPS-I compliant | Copyright 2005,2006,2009 Jonathan Rose, and |
| mipsr2000 | https://opencor | stable | Lazaridis Dimitris | MIPS | 32 | 32 | kintex-7-3 | James | Brakef | 1971 | 6 | 4 | 6 | 71 | ## | 14.7 | 1.00 | 1.0 | 36.2 | X | | vhdl | 35 | Dm | Y | yes | N | | 4G | 4G | Y | | | 32 | 5 | 2012 | 2016 | | supports almost all instructions of mi | course project |
| or1200_hp | https://opencor | stable | Strauch Tobias | OpenRISC | 32 | 32 | virtex-5 | Strauc | 3 slot | 5602 | 6 | | | 185 | ## | | 1.00 | 1.0 | 33.1 | X | | verilog | 39 | or1200_ic | Y | yes | Y | M | 4G | 4G | Y | | | 32 | | 2010 | 2013 | https://openrisc.io | 3 slot barrel version of OR1200 | numbers from published paper |
| **riscv_neorv32** | https://github.c | stable | Stephan Nolting | risc-v | 32 | 32 | cyclone-IV | Steph | rtl fpg | 848 | 4 | | | 111 | ## | q19.1 | 1.00 | 4.0 | 32.7 | AL | Y | vhdl | 25 | neorv32_t | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2020 | 2021 | https://opencores | **very well documented, customiza** | **many perpherals, LUT counts for all variati** |
| eco32f | https://github.c | stable | Stefan Kristiansson | RISC | 32 | 32 | kintex-7-3 | James | Brakef | 3845 | 6 | 3 | 4 | 123 | ## | 14.7 | 1.00 | 1.0 | 32.1 | X | | verilog | 12 | eco32f | Y | yes | N | | 512M | 256M | Y | 61 | | 32 | 6 | 2014 | 2014 | | pipelined version of the eco32 CPU | cache & mmu |
| dlx_chiara | https://github.c | stable | Alessandro Di Chiara | DLX | 32 | 32 | kintex-7-3 | James | Brakef | 2915 | 6 | | | 90 | ## | 14.7 | 1.00 | 1.0 | 30.9 | X | | vhdl | 32 | a-dlx | Y | yes | N | | 4G | 4G | | | | 32 | 5 | 2017 | 2017 | | Course project, no RTL comments, VHDL via instructor? | |
| arm4u | https://github.c | stable | Joanathan Masur, Xav | ARM7 | 32 | 32 | aria-2 | James | Brakef | 1668 | A | 4 | 8 | 66 | ## | q13.1 | 0.75 | 1.0 | 29.5 | I | | vhdl | 12 | cpu | Y | yes | N | | 4G | 4G | Y | 80 | | 16 | 5 | 2013 | 2014 | | university project | altera memory |
| opa | https://github.c | stable | Wesley W. Terpstra | RISC | 32 | 32 | cyclone-5 | Wesle | largest | 8540 | A | | | 125 | | q15.0 | 1.00 | 0.5 | 29.3 | I | | vhdl | | | | | | | | | | | | 32 | | 2013 | 2016 | | An Out-of-Order Superscalar Soft CPU | tested, incomplete |
| yarvi | https://github.c | beta | Tommy Thorn | risc-v | 32 | 32 | kintex-7-3 | James | Brakef | 2152 | 6 | | 17 | 122 | ## | 14.7 | 1.00 | 2.0 | 28.3 | X | | verilog | 3 | yarvi_soc | Y | yes | N | N | 4G | 4G | | | | 32 | 3 | | 2016 | | no multiply or divide | simple implementation of RISC-V |
| nige_machine | https://github.c | stable | Andrew Read | forth | 32 | 8 | kintex-7-3 | James | Brakef | 5033 | 6 | 8 | 33 | 123 | ## | 14.7 | 1.00 | 1.0 | 24.5 | X | | vhdl | 29 | Board | Y | yes | N | | 16M | 16M | | 512 | | 512 | | | 2014 | | standalone Forth system | https://www.youtube.com/watch?v=PRItE8q6 |
| btsr1arch | https://github.c | beta | Brendan Bohannon | CISC | 32 | 16 | kintex-7-3 | James | Brakef | 4762 | 6 | | 10 | 167 | ## | 14.7 | 1.00 | 1.5 | 23.3 | X | | verilog | 11 | bsrexunit | Y | yes | Y | N | 64K | 64K | Y | 64 | | 32 | | 2018 | 2021 | | is BtSR1, msp430 like, fltg-pt defined | 3 data sizes, no (R++) or (--R) modes |
| mips_fault_tol | https://opencor | stable | Lazaridis Dimitris | MIPS | 32 | 32 | kintex-7-3 | James | Brakef | 2017 | 6 | 4 | 6 | 45 | ## | 14.7 | 1.00 | 1.0 | 22.5 | X | | vhdl | 40 | main | Y | yes | N | | 4G | 4G | Y | | | 32 | 5 | 2013 | 2013 | | arithmetic includes fault detection | no external memory port? |
| or1200 | https://github.c | stable | Damjan Lampret | OpenRISC | 32 | 32 | kintex-7-3 | James | Brakef | 5231 | 6 | 4 | 8 | 118 | ## | 14.7 | 1.00 | 1.0 | 22.5 | X | | verilog | 78 | or1200_to | Y | yes | Y | M | 4G | 4G | Y | | | 32 | | 2010 | 2015 | https://openrisc.io | best older openrisc implementation | no LUT RAM for reg file |
| or1200mp | https://github.c | stable | Stefan Wallentowitz | OpenRISC | 32 | 32 | kintex-7-3 | James | Brakef | 4960 | 6 | 4 | 8 | 111 | ## | 14.7 | 1.00 | 1.0 | 22.4 | X | | verilog | 104 | or1200_to | Y | yes | Y | M | 4G | 4G | Y | | | 32 | | 2012 | 2012 | https://openrisc.io | multiprocessor variant, single core | |
| riscompatible | https://opencor | beta | Andre Soares | RISC | 32 | 32 | kintex-7-3 | James | set IO | 2167 | 6 | | 1 | 145 | ## | 14.7 | 1.00 | 3.0 | 22.3 | X | | vhdl | 12 | riscompat | Y | yes | N | Y | 4G | 4G | Y | | | 16 | | 2014 | | | based on RISCO processor by Junqueira & Suzim 1993 | |
| leon2 | https://github.c | stable | Jiri Gaisler | SPARC | 32 | 32 | kintex-7-3 | James | Brakef | 5992 | 6 | 1 | 12 | 133 | ## | 14.7 | 1.00 | 1.0 | 22.3 | X | | vhdl | 82 | leon | Y | yes | Y | | 4G | 4G | Y | | | 64 | 5 | 1999 | 2003 | https://en.wikiped | large config file, rad-hard asic version | https://www.gaisler.com/index.php/products/ |
| minsoc | https://opencor | stable | Raul Fajardo etal | OpenRISC | 32 | 32 | kintex-7-3 | James | Brakef | 4945 | 6 | 4 | 8 | 107 | ## | 14.7 | 1.00 | 1.0 | 21.7 | ILX | Y | verilog | 88 | or1200_to | Y | yes | Y | M | 4G | 4G | Y | | | 32 | | 2009 | 2013 | https://github.cor | minimal OR1200, vendor neutral, has caches | |
| mips32r1 | https://opencor | stable | Grant Ayers | MIPS | 32 | 32 | aria-2 | James | Brakef | 3716 | A | 8 | | 79 | ## | q13.1 | 1.00 | 1.0 | 21.3 | IX | | verilog | 20 | processor | Y | yes | N | Y | 4G | 4G | Y | | | 32 | 5 | 2012 | 2015 | https://github.cor | complete software tool chain | |
| altium/TSK300 | http://techdocs | proprietar | Altium | RISC | 32 | 32 | spartan-3-5 | Altium | | 2426 | 4 | | 4 | 50 | | | 1.00 | 1.0 | 20.6 | AILX | | proprietary | | | Y | yes | N | N | 4G | 4G | Y | | | | | 2004 | 2017 | CR0140.pdf, http:/ | frozen, asm, C, C++, schem, VHDL & V | default clock: 50MHz, opt mult/div |
| zap | https://opencor | alpha | Revanth Kamaraj | ARM7 | 32 | 32 | kintex-7-3 | James | Brakef | 7558 | 6 | 1 | 9 | 135 | ## | 14.7 | 1.00 | 1.0 | 17.9 | X | | verilog | 37 | zap_top | Y | yes | N | N | 4G | 4G | Y | | | 16 | | 2017 | 2018 | ddi0100e_armv1- | ARMv4T & Thumbv1 | has cache & mmu |
| minimig | https://code.go | stable | Frederic Requin | 68000 | 32 | 16 | stratix-2 | Freder | speed | 1900 | 4 | | 4 | 180 | | | 1.00 | 6.0 | 15.8 | I | | verilog | 1 | j68 | Y | yes | N | | 4G | 4G | Y | | | 16 | | 2009 | 2014 | | for use with Minimig | micro-coded on stack machine |
| piropiro | https://github.c | stable | pandora2000 | RISC | 32 | 32 | kintex-7-3 | James | port m | 7491 | 6 | 11 | 1 | 118 | ## | 14.7 | 1.00 | 1.0 | 15.7 | X | | vhdl | 42 | top | | | Y | N | 64K | 64K | Y | | | 32 | | 2010 | 2011 | | five variants | no doc, xilinx constraint file |
| riscv_microsen | https://github.c | stable | Microsemi | risc-v | 32 | 32 | polarfire | microsemi | | 8614 | 4 | 2 | 10 | 122 | | L11.8 | 1.00 | 1.0 | 14.2 | | | proprietary | | | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2016 | 2018 | https://www.micr | is encrypted IP | has caches |
| klc32 | https://opencor | planning | Robert Finch | RISC | 32 | 32 | kintex-7-3 | James | Brakef | 3790 | 6 | 4 | 1 | 200 | ## | 14.7 | 1.00 | 4.0 | 13.2 | X | | verilog | 25 | KLC32 | Y | | N | | 4G | 4G | Y | | | 32 | | 2011 | 2012 | https://github.cor | single ported block RAM register file :( | heavy use of includes |
| zpuino | http://alvie.com | alpha | Alvaro Lopes | forth | 32 | 8 | spartan-6-3 | James | Brakef | 2547 | 6 | 4 | 12 | 126 | ## | 14.7 | 1.00 | 4.0 | 12.3 | X | Y | vhdl | | papilio_pr | Y | yes | N | | 4G | 4G | Y | 37 | | | | 2008 | 2012 | | SoC version of modified ZPU | pipelined, removed ucf file |
| flexgrip | http://www.ecs | paper | Kevin Andryc | GPU | 32 | 32 | atrix-7 | James | Brakef | 72649 | 6 | 156 | 119 | 100 | ## | 14.7 | 1.00 | 0.1 | 11.0 | X | | vhdl | 46 | gpgpu_ml505_top_level | | | | | | | | | | | | 2013 | 2016 | http://www.ecs.u | eight GPU processors | requested & received source files |
| mipsfpga | https://www.m | stable | MIPS Technologies | MIPS | 32 | 32 | atrix-7-3 | James | Brakef | 10692 | 6 | | 47 | 118 | ## | 14.7 | 1.00 | 1.0 | 11.0 | X | Y | verilog | 193 | mfp_syste | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2014 | 2018 | https://www.yout | M14K core & mipsfpga-plus | DRAM interface, I&D caches. 8789 FF |
| xulalx25soc | https://opencor | mature | Dan Gisselquist | RISC | 32 | 32 | spartan-6-3 | James | Sparta | 7936 | 6 | 4 | 25 | 87 | ## | 14.7 | 1.00 | 1.0 | 11.0 | X | Y | verilog | | toplevel | Y | yes | N | N | 4G | 4G | N | 20 | | 16 | 5 | 2015 | | | | uses ZIP CPU |
| riscv_rv01_cor | https://github.c | stable | Stefano Tonello | risc-v | 32 | 32 | kintex-7-3 | James | Brakef | 13997 | 6 | 4 | 62 | 130 | ## | 14.7 | 1.00 | 1.0 | 9.3 | X | | vhdl | 65 | rv01_selfte | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2015 | 2017 | | all files in one directory | two self test tops |
| mist1032 | https://github.c | stable | Takahiro Ito | RISC | 32 | 32 | arria_2 | James | altera | 10801 | A | 4 | 125 | 98 | ## | q18.0 | 1.00 | 1.0 | 9.1 | | | system v | 50 | mist32e10 | Y | | | | 4G | 4G | Y | | | 64 | | | 2014 | | mist32 uP: embedded version | |
| m32632 | https://opencor | stable | Udo Moeller | N32032 | 32 | 8 | kintex-7-3 | James | Brakef | 10167 | 6 | 19 | 16 | 83 | ## | 14.7 | 1.00 | 1.0 | 8.2 | IX | | verilog | 18 | example | Y | yes | Y | Y | 4G | 4G | Y | 200 | | 24 | 3 | 2009 | 2019 | http://cpu-ns32k.net/ | 21.97 VAX Mips at 50MHz (Cyclone IV) | |
| leon2 | https://github.c | stable | Jiri Gaisler | SPARC | 32 | 32 | cyclone-1 | Klas | Westerlu | 7554 | 4 | | 42 | 50 | ## | | 1.00 | 1.0 | 6.6 | I | | vhdl | 90 | leon | Y | yes | Y | | 4G | 4G | Y | | | 64 | 5 | 1999 | 2003 | https://en.wikiped | LUT #s from Nios vs Leon2 compariso | https://www.gaisler.com/index.php/products/ |
| riscv_humming | https://github.c | stable | | risc-v | 32 | 32 | kintex-7-3 | James | Brakef | 14119 | 6 | | 32 | 62 | ## | 14.7 | 1.00 | 1.0 | 4.4 | X | | verilog | 141 | e203_soc | Y | yes | N | | 4G | 4G | Y | | | 32 | | 2016 | 2018 | | e200 has opensource | also have a chip |
| af65k | https://github.c | alpha | Andre Fachat | 6502 | 32 | 8 | kintex-7-3 | James | Brakef | 4424 | 6 | | | 69 | ## | 14.7 | 1.00 | 4.0 | 3.9 | X | | vhdl | 13 | gecko65k | Y | | N | N | | | | | | | | 2011 | 2019 | http://www.6502 | extended 6502 AKA 65K with 16, 32 or | 64 bit data |
| rtf65002 | https://opencor | alpha | Robert Finch | accum | 32 | 8 | kintex-7-3 | James | Brakef | 11216 | 6 | 4 | 6 | 123 | ## | v14.1 | 0.67 | 2.0 | 3.7 | X | | verilog | 10 | rtf65002d | Y | | N | | 4G | 4G | Y | | | 16 | | 2013 | 2013 | https://github.cor | 32-bit 6502 + 6502 emulation | "proven" |
| riscv_rsd | https://github.com/rsd-de | Susumu Mashimo | risc-v | 32 | 32 | zynq | Susumu | Mash | 28166 | 6 | | | 90 | | | | 1.00 | 1.0 | 3.2 | | | system verilog | | | Y | yes | N | | 4G | 4G | Y | | | 32 | | | 2020 | | RISC-V out-of-order superscalar proc | can be synthesized for small FPGAs |
| ztapchip | https://github.c | stable | Vuony Nguyen | MIPS | 32 | 32 | cyclone-5 | James | Brakef | 31331 | A | 43 | 578 | 100 | ## | q18.0 | 1.00 | 1.0 | 3.2 | I | Y | vhdl | 53 | ztachip | | | | | | | | | | | | 2015 | 2015 | | multi-core with MIPS master | files no longer available, was under developme |
| kpu | https://github.c | alpha | Andrea Corallo | RISC | 32 | 32 | kintex-7-3 | James | missin | 6178 | 6 | 3 | | 19 | ## | 14.7 | 1.00 | 1.0 | 3.0 | X | Y | verilog | 19 | kpu | Y | yes | N | Y | 4G | 4G | | | | 32 | | 2016 | 2018 | http://andreacora | KPU is a minimal system on chip writt | en used as testbench for the KPU core |
| milkymist | https://github.c | stable | Sebastien Bourdeaudu | LM32 | 32 | 32 | spartan-6 | James | failed | 13531 | 6 | 31 | 78 | 50 | ## | 14.7 | 0.80 | 1.0 | 3.0 | X | Y | verilog | 169 | system | Y | yes | N | Y | 4G | 4G | Y | | | 32 | 6 | 2007 | 2014 | | uses LM32, uses Spartan-6 IO | failed in mapper |
| riscv_fwrisc | https://github.c | untested | Matthew Balance | risc-v | 32 | 32 | igloo2 | Matthew | Bala | 1060 | 4 | | | 20 | ## | | 1.00 | 6.7 | 2.8 | AL | | system v | 8 | fwrisc_fpg | Y | yes | N | | 4G | 4G | Y | 45 | | 32 | | 2018 | 2018 | https://opencores | featherweight entry 2018 RISC-V cont | 0.15 DMIPS/MHz |
| v586 | https://opencor | beta | Jose Rissetto | x86 | 32 | 8 | kintex-7-3 | James | Brakef | 22282 | 6 | 12 | 16 | 102 | ## | 14.7 | 1.00 | 2.0 | 2.3 | X | | verilog | 22 | v586 | Y | yes | N | | 1M | 1M | Y | | | | | 2014 | | www.valptek.com | MMU & caches, branch cache | www.youtube.com/channel/UCNbm8Bah54cw |
| edge | https://opencor | alpha | Hesham ALMatary | MIPS | 32 | 32 | spartan-6-3 | James | Brakef | 5345 | 6 | 7 | 1 | 8 | ## | 14.7 | 1.00 | 1.0 | 1.5 | X | | verilog | 30 | edge_core | Y | yes | N | N | 4G | 4G | Y | | | 32 | 5 | 2014 | 2014 | | Edge Processor (MIPS) | MIPS1 clone |
| ao486 | https://opencor | beta | Aleksander Osman | x86 | 32 | 8 | cyclone-4-7 | James | Brakef | 36094 | 4 | 4 | 47 | 46 | ## | q13.1 | 1.00 | 1.0 | 1.3 | I | Y | system v | 85 | ao486 | Y | yes | | | 4G | 4G | Y | | | | | 2014 | 2014 | | complete 486, SoC configuration | non-SoC, no MMU |
| lemberg | https://github.c | stable | Wolfgang Puffitsch | VLIW | 32 | 32 | cyclone-4-6 | James | Brakef | 37459 | 4 | 25 | 54 | 43 | ## | q13.1 | 1.00 | 1.0 | 1.1 | I | | vhdl | 57 | core | Y | yes | Y | | 4G | 2M | Y | | | 32 | 4 | 2011 | | http://www2.imm | upto 4 inst/clock | LPM mem & floating point |
| sp-i586 | https://github.c | stable | Lini Mestar | x86 | 32 | 8 | kintex-7-3 | James | Brakef | 32144 | 6 | 4 | 28 | 73 | ## | 14.7 | 1.00 | 2.0 | 1.1 | X | | verilog | 37 | top_sys | Y | yes | Y | | 4G | 4G | Y | | | | | 2016 | 2016 | http://lmeshoo.ne | gate level dsgn, vivado project also | http://img.youtube.com/vi/2W1guyhCJuE/0.jp |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| rois | https://opencor | alpha | James Brakefield | RISC | 24 | 24 | **zu-2e** | James | no blk | 627 | 6 | | | 382 | ## | v19.2 | 0.83 | 1.0 | 507.1 | X | | vhdl | 2 | rois24_24min | | | N | | 16M | 16M | N | 30 | | 64 | 1 | 2016 | 2017 | | single pipe stage, passes simulation | 24-bit word operations only |
| opc.opc8cpu | https://github.c | beta | revaldinho | RISC | 24 | 24 | kintex-7-3 | James | no tes | 516 | 6 | | | 323 | ## | 14.7 | 0.80 | 2.0 | 250.1 | X | | verilog | 1 | opc8cpu | Y | asm | N | N | 16M | 16M | N | 32 | 4 | 16 | | 2017 | 2019 | https://revaldinho | OPC8 24bit, based on OPC5LS, more i | see hackaday One Page Computing Challenge |
| ep24 | | stable | C.H. Ting | forth | 24 | 6 | kintex-7-3 | James | substit | 1020 | 6 | | 3 | 167 | ## | 14.7 | 0.83 | 1.0 | 135.6 | X | | vhdl | 1 | ep24 | Y | asm | N | N | | 4K | | 27 | | | | 2002 | 2002 | | room for 37 additional op-codes | removing stack clear: 503 LUT6 & 143MHz |
| 24bit_up | https://github.c | alpha | Harshal Mittal | RISC | 24 | 24 | **zu-2e** | James | area o | 3453 | 6 | 1 | | 187 | ## | v20.1 | 0.80 | 1.0 | 43.2 | X | | verilog | 17 | processor | | | N | | 16M | 16M | N | 17 | | 32 | | 2019 | 2019 | | basic 24-bit RISC, course work | big Dff count, multiple writes to register file |
| p24e | | beta | C. H. Ting | forth | 24 | 6 | spartan_3-5 | James | Brakef | 1175 | 4 | | 16 | 51 | ## | 14.7 | 0.83 | 1.0 | 36.0 | X | | vhdl | 1 | p24c | Y | asm | N | | 2K | 2K | | 28 | | | | 2000 | | | part of eForth? | data width can be expanded |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| kraken16 | https://people.e | stable | Bruce R. Land | RISC | 18 | 18 | kintex-7-3 | James | Brakef | 281 | 6 | | 1 | 278 | ## | 14.7 | 0.67 | 1.0 | 662.3 | X | | verilog | 1 | DE2_TOP | Y | asm | N | N | 256 | 256 | N | 22 | | 16 | | | 2008 | https://people.ec | Cornell course material | |

| _uP_all_soft folder | opencores or prmary link | status | author | style / clone | data size | inst size | FPGA | reporter | comments | LUTs ALUT | LUT? | mults | blk ram | F max | date | tool ver | MIPS /inst | clks/ inst | KIPS /LUT | vendor | SOC | src code | #src files | top file | doc | toolchai n | fltgpt | Hav'd | max dat | max inst | byte adrs | # inst | adr mod | # reg | pipe len | start year | last revis | secondary web link | note worthy | comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| spartanMC | http://www.spa | stable | Falk Hassler | RISC | 18 | 18 | kintex-7-3 | James Brakef | | 853 | 6 | 1 | 2 | 120 | ## | 14.7 | 0.67 | 1.0 | 94.6 | X | Y | verilog | 38 | spartanmc | Y | asm | | | | | | | | | 2012 | 2014 | | SPARC like register windows | |
| pdp1 | https://opencor | alpha | Yann Vernier | PDP1 | 18 | 18 | spartan-3a- | James Brakef | | 1390 | 4 | | 6 | 138 | ## | 14.7 | 0.50 | 10.0 | 5.0 | X | | vhdl | 15 | top | Y | yes | N | N | 4K | 4K | | 28 | | | | 2011 | 2017 | http://pdp-1.com | PDP-1 descended from MIT TX-0 | uses Minimal UART from opencores |
| leros | https://opencor | stable | Martin Schoeberl | accum | 16 | 16 | spartan-6 | Martin Schoe | | 112 | 6 | | 1 | 182 | | | 0.67 | 1.0 | 1088.8 | IX | | vhdl | 5 | leros | Y | yes | N | Y | 256 | 64K | | | | 2 | 2 | 2008 | 2020 | https://github.cor | 256 word data RAM, PIC like | short LUT inst ROM |
| J1 | www.excamera | stable | James Bowman | forth | 16 | 16 | **zu-2e** | James | area o | 253 | 6 | | 1 | 336 | ## | v20.1 | 0.80 | 1.0 | 1061.1 | X | | vhdl | 1 | j1 | Y | forth | N | | 64K | 64K | | 20 | | | 2 | 2006 | 2015 | https://github.cor | uCode inst, dual port block RAM | 16 deep data & return stacks |
| Lutiac | | custom | David Galloway, David | reg | 16 | NA | stratix-4 | David Gallow | | 140 | A | 4 | | 198 | | | 0.67 | 1.0 | 947.6 | I | | vhdl & verilog | | | | | | | 64 | N | 64 | | 32 | 3 | | 2010 | Talks at Un. Toron | synthesis maps PC into ucode | no inst mem: small state machine, ~200 inst o |
| hamblen_scon | http://hamblen. | stable | James O. Hamblen | accum | 16 | 16 | cyclone-10 | James | altera | 80 | 4 | | 1 | 204 | ## | q18.0 | 0.67 | 2.0 | 852.7 | I | | verilog | 1 | scomp | | | N | N | 256 | 256 | N | 4 | | | | 2008 | http://hamblen.ec | from Hamblen 2008 "Rapid prototypi | tiny edu, high IO count |
| iDEA | https://github.c | alpha | Hui Yan Cheah etal | RISC | 16 | 32 | virtex-6 | Liu Ch | unable | 321 | 6 | 1 | 2 | 405 | | 13.2 | 0.67 | 1.0 | 845.3 | X | | verilog | 22 | cpu_top | Y | yes | N | Y | 64K | 64K | N | 24 | | 32 | 9 | 2011 | 2016 | The iDEA DSP Bloc | uses DSP slice in barrel mode for ALU | from GitHub, rq'd NOPs lower actual results |
| octavo | http://fpgacpu.c | beta | Charles LaForest | reg | 16 | 16 | stratix-4 | Charles LaFor | | 500 | A | 1 | | 550 | | | 0.67 | 1.0 | 737.0 | I | | verilog | 18 | Octavo | Y | asm | N | | | | | 14 | | 16 | 10 | 2012 | 2019 | https://github.cor | 8 core barrel, adjustable data width | ~= performance across word sizes, no call/rtn i |
| cpu16 | http://www.ultr | stable | C.H. Ting | forth | 16 | 5 | kintex-7-3 | James Brakef | | 347 | 6 | | | 364 | ## | 14.7 | 0.67 | 1.0 | 702.1 | X | | vhdl | 1 | cpu16 | | | N | N | 64K | 64K | N | 28 | | | | 2000 | 2000 | | P16 in VHDL | CPU24.vhd with width=16 |
| p16b | | beta | C. H. Ting | forth | 16 | 5 | kintex-7-3 | James | case c | 367 | 6 | | | 355 | ## | 14.7 | 0.67 | 1.0 | 648.1 | X | | vhdl | 1 | cpu16 | Y | asm | N | | 64K | 64K | | 28 | | | | 2000 | | | part of eForth? | data width can be expanded |
| xr16 | https://github.c | stable | Jan Gray | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 273 | 6 | | | 263 | ## | 14.7 | 0.67 | 1.0 | 644.8 | X | | verilog | 4 | xr16 | Y | | N | | 64K | 64K | | | | 16 | | 1999 | 2001 | | handcrafted instruction set | tool FPGA P&R, speed mode better |
| dspuva16 | http://www.DTE | stable | Santiago de Pablo | DSP | 16 | 16 | kintex-7-3 | James Brakef | | 332 | 6 | | | 317 | ## | 14.7 | 0.67 | 1.0 | 640.7 | X | | verilog | 1 | dspuva16 | | asm | N | Y | 256 | 4K | | 40 | | 16 | | 2001 | 2004 | www.1-core.com/ | 16 bit data memory, 24 bit regs | broken web link |
| J1a | www.excamera | stable | James Bowman | forth | 16 | 16 | kintex-7-3 | James | DFF ex | 518 | 6 | | | 412 | ## | 14.7 | 0.80 | 1.0 | 636.1 | X | | verilog | 3 | j1 | Y | forth | N | | 64K | 64K | | 20 | | | 2 | 2006 | 2017 | https://github.cor | uCode inst, dual port block RAM | DFF used for 18 deep data & return stacks |
| s16x4a | https://github.c | stable | Samuel Falvo II | forth | 16 | 4 | kintex-7-3 | James Brakef | | 514 | 6 | | | 476 | ## | 14.7 | 0.67 | 1.0 | 620.7 | X | B | verilog | 1 | s16x4a | Y | | N | N | 64K | 64K | Y | 12 | | | | 2012 | 2017 | | kestrel #2, byte & word data | derived from Myron Plichota's design (streame |
| msl16 | | beta | Philip Leong, Tsang, Le | forth | 16 | 4 | kintex-7-3 | James Brakef | | 303 | 6 | | | 256 | ## | 14.7 | 0.67 | 1.0 | 566.4 | X | | vhdl | 13 | cpu | Y | asm | N | | 256 | | | 16 | | | | 2001 | | | CPLD prototype | |
| xucpu | https://opencor | alpha | Jurgen Defurne | RISC | 16 | 16 | spartan-6-3 | James Brakef | | 356 | 6 | | 4 | 187 | ## | 14.7 | 1.00 | 1.0 | 524.8 | X | Y | vhdl | 25 | system_4k | | | | | 4K | 4K | | | | | | 2015 | 2017 | | Experimental Unstable CPU | |
| streamer16 | http://www.ultr | stable | Myron Plichota | forth | 16 | 3 | kintex-7-3 | James Brakef | | 143 | 6 | | | 417 | ## | 14.7 | 0.20 | 1.2 | 485.6 | X | | vhdl | 8 | streamer | Y | yes | N | N | 64K | 64K | N | 8 | 2 | | | 2001 | 2001 | http://www3.sym | MIPS/inst reduced | 2nd web adr non-functional |
| atlas_core | https://opencor | beta | Stephan Nolting | RISC | 16 | 16 | **zu-2e** | James | area o | 588 | 6 | 1 | | 314 | ## | v20.1 | 0.80 | 1.0 | 427.3 | IX | | vhdl | 8 | ATLAS_CP | Y | asm | N | Y | 64K | 64K | Y | 80 | | 8 | | 2013 | 2015 | | ARM thumb like inst set | non-MMU version |
| fpga4_mips16 | http://www.fpg | stable | Van Loi Le | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 352 | 6 | | | 213 | ## | 14.7 | 0.67 | 1.0 | 405.0 | X | | vhdl | 8 | mips_vhdl | | | N | | 65K | 65K | | 8 | | 8 | | 2017 | 2017 | | educational, no block RAM inferred | actual prog sz=16, actual data mem sz=256 |
| fpga4_mips16 | http://www.fpg | stable | Van Loi Le | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 369 | 6 | | | 200 | ## | 14.7 | 0.67 | 1.0 | 363.1 | X | | verilog | 8 | mips_16 | | | N | | 65K | 65K | | 13 | | 8 | | 2017 | 2017 | | educational, no block RAM inferred | same prog & data mem and alu as mips16_16 |
| micro16b | http://members | beta | John Kent | accum | 16 | 16 | kintex-7 | James Brakef | | 205 | 6 | | | 434 | ## | 14.7 | 0.33 | 2.0 | 349.0 | X | | vhdl | 1 | u16bcpu | Y | asm | N | N | 64K | 4K | Y | 8 | | | | 2002 | 2008 | http://members.c | very limited inst set | MIPS/clk adj'd, 2 clks/inst |
| alwcpu | https://opencor | alpha | Andreas Hilvarsson | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 377 | 6 | | | 194 | ## | 14.7 | 0.67 | 1.0 | 345.5 | ILX | | vhdl | 7 | top | | ome | N | N | 64K | 64K | Y | | | 16 | | 2009 | 2010 | | lightweight CPU | maximal features |
| risc_core_i | https://opencor | planning | Manuel Imhof | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 349 | 6 | 1 | | 526 | ## | 14.7 | 0.67 | 3.0 | 336.8 | X | B | vhdl | 13 | CPU | Y | asm | N | | 1K | 1K | | | | 8 | 4 | 2001 | 2009 | | Havard arch, thesis project | derived clocks: estimated derating |
| ncore | https://opencor | alpha | Stefan Istvan | accum | 16 | 8 | kintex-7-3 | James Brakef | | 223 | 6 | | | 105 | ## | 14.7 | 0.67 | 1.0 | 316.3 | X | | verilog | 3 | nCore | Y | | N | | 128K | 64K | | 16 | | 16 | | 2006 | 2018 | | This is a little-little processor core | |
| raptor16 | www.spacewire | stable | Steve Haywood | CISC | 16 | 16 | kintex-7-3 | James Brakef | | 590 | 6 | | | 319 | ## | 14.7 | 1.40 | 2.7 | 280.2 | X | | vhdl | 1 | raptor16 | Y | yes | N | N | 64K | 64K | N | | | | | 2004 | | | 8 data & 8 adr regs | no multiply, 8 adr modes |
| dgb16 | see FISA64 | stable | Robert Finch | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 780 | 6 | | | 313 | ## | 14.7 | 0.67 | 1.0 | 269.0 | X | | verilog | 1 | dbg16 | Y | | N | Y | | | | | | 8 | | | | https://github.cor | inside FISA64 project | debug uP for fisa64 |
| yafc | https://github.c | alpha | Tim Wawrzynczak | forth | 16 | | kintex-7-3 | James Brakef | | 617 | 6 | | 4 | 247 | ## | 14.7 | 0.67 | 1.0 | 268.5 | X | | vhdl | 20 | cpu | | asm | N | Y | 8K | 8K | | 26 | | | | | 2014 | | | | influenced by J1, F16 & C18 |
| diogenes | https://opencor | beta | Fekknhifer | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 807 | 6 | | 1 | 297 | ## | 14.7 | 0.67 | 1.0 | 246.3 | X | | vhdl | 11 | cpu | Y | asm | N | | | 1K | | | | | | 2008 | 2009 | | "student RISC system" | |
| sayeh_process | https://opencor | stable | Alireza Haghdoost, Arr | RISC | 16 | 8 | kintex-7-3 | James Brakef | | 479 | 6 | 1 | | 164 | ## | 14.7 | 0.67 | 1.0 | 229.7 | X | | verilog | 13 | Sayeh | Y | | N | | 64K | 64K | | | | 32 | | 2008 | 2009 | haghdoost.persiangig.com | | simple RISC |
| opc.opc3cpu | https://github.c | stable | revaldinho | accum | 16 | 16 | kintex-7-3 | James | reduce | 174 | 6 | | | 526 | ## | 14.7 | 0.30 | 4.0 | 226.9 | X | | verilog | 2 | opc3cpu | Y | asm | N | N | 64K | 64K | N | 13 | 3 | | | 2017 | 2019 | https://revaldinho | OPC3 16-bit OPC1, for XC95144 CPLD | see hackaday One Page Computing Challenge |
| table887 | https://github.c | alpha | Robert Finch | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 643 | 6 | | 2 | 208 | ## | 14.7 | 0.67 | 1.0 | 217.1 | X | | verilog | 2 | table887 | Y | | N | N | 64K | 64K | | 28 | | 8 | | 2014 | 2016 | | | included with Table888 source code |
| ep16 | https://github.c | beta | C.H. Ting | forth | 16 | 5 | kintex-7-3 | James Brakef | | 837 | 6 | | | 254 | ## | 14.7 | 0.67 | 1.0 | 203.6 | X | | vhdl | 5 | ep16.vhd | Y | yes | N | N | 32K | 32K | N | 32 | | | | 2005 | 2012 | PDF files | initialized Lattice memory blocks | 5-bit instructions |
| pancake | https://people.e | stable | Bruce Land | stack | 16 | 5 | kintex-7-3 | James | bypass | 441 | 6 | 1 | 1 | 128 | ## | 14.7 | 0.67 | 1.0 | 194.8 | X | | verilog | 7 | de2_minic | Y | yes | N | | 4K | 4K | | 31 | | | | 2010 | 2014 | http://www.cs.hir | The Pancake Stack Machine derived f | Cornell ECE5760 |
| atlas_2K | https://opencor | beta | Stephan Nolting | RISC | 16 | 16 | **zu-2e** | James | area o | 1169 | 6 | 1 | 5 | 252 | ## | v20.1 | 0.80 | 1.0 | 172.2 | ILX | | vhdl | 19 | ATLAS_2K | Y | asm | N | Y | 64K | 64K | M | 80 | | 8 | | 2013 | 2015 | | ARM thumb like inst set | has MMU & full SOC features |
| yasep | news.yaesp.org | alpha | Yann Guidon | RISC | 16 | 32 | kintex-7-3 | James | reduce | 632 | 6 | | | 215 | ## | I14.7 | 1.00 | 2.0 | 170.0 | AX | | vhdl | 3 | microYAES | Y | asm | N | N | 2G | 2G | | 51 | | 16 | | 2005 | 2018 | | JavaScript generated VHDL, revisions | YASEP talk at www.youtube.com/watch?v=bw |
| opc.opc6cpu | https://github.c | stable | revaldinho | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 450 | 6 | | | 222 | ## | 14.7 | 0.67 | 2.0 | 165.4 | X | | verilog | 2 | opc6cpu | Y | asm | N | N | 64K | 64K | N | 27 | 4 | 16 | | 2017 | 2019 | https://revaldinho | OPC6 based on OPC5LS, more inst | see hackaday One Page Computing Challenge |
| b16 | www.bernd-pay | stable | Bernd Paysan | forth | 16 | 5 | spartan-6-3 | James Brakef | | 554 | 6 | | | 134 | ## | 14.7 | 0.67 | 1.0 | 161.7 | IX | | verilog | 1 | b16 | Y | yes | N | | | | | | | | | 2002 | 2011 | | two versions: one/15 source files, derived from c18 | |
| kestrel-2 | kestrelcomputer | stable | Samuel Falvo II | forth | 16 | 16 | kintex-7-3 | James Brakef | | 735 | 6 | | 8 | 172 | ## | 14.7 | 0.67 | 1.0 | 157.2 | X | Y | verilog | 27 | M_kestrel | Y | yes | N | | 64K | 64K | | 20 | | | 2 | 2012 | 2015 | https://hackaday. | J1 with wishbone bus | M_j1a runs at 244MHz & 368 LUTs |
| mcip_open | https://opencor | beta | Mezzah Jbrahim | PIC18 | 16 | 24 | kintex-7-3 | James Brakef | | 881 | 6 | 1 | | 200 | ## | 14.7 | 0.67 | 1.0 | 152.1 | X | | vhdl | 23 | MCIOopen_r | | yes | N | Y | 4K | 1M | Y | | | | | 2014 | 2015 | | light version of PIC18 | |
| ensilica | http://www.ens | proprietar | ensilica.com | eSi-1600 | 16 | 16 | virtex-5 | ensilica | | 1100 | 6 | | | 160 | | | 1.00 | 1.0 | 145.5 | IX | | verilog | | eSi-1600 | Y | yes | | | 64K | 64K | Y | 92 | 10 | 16 | 5 | 2001 | 2016 | | verilog source included with license | room for 90 user inst, also as ASIC |
| opc.opc5lscpu | https://github.c | stable | revaldinho | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 383 | 6 | | | 247 | ## | 14.7 | 0.67 | 3.0 | 144.0 | X | | verilog | 2 | opc5lscpu | Y | asm | N | N | 64K | 64K | N | 18 | 4 | 16 | | 2017 | 2019 | https://revaldinho | OPC5LS OPC5 with predicate inst | see hackaday One Page Computing Challenge |
| opc.opc5cpu | https://github.c | stable | revaldinho | RISC | 16 | 16 | kintex-7-3 | James | reduce | 273 | 6 | | | 294 | ## | 14.7 | 0.40 | 3.0 | 143.6 | X | | verilog | 7 | opc5cpu | Y | asm | N | N | 64K | 64K | N | 15 | 4 | 16 | | 2017 | 2019 | https://revaldinho | OPC5 RR inst, ISA similar to OPC1 | see hackaday One Page Computing Challenge |
| ejrh_cpu | https://github.c | stable | Edmund Horner | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 928 | 6 | 1 | 2 | 196 | ## | 14.7 | 0.67 | 1.0 | 141.6 | X | | verilog | 17 | machine | Y | | | | | | | | | 16 | | 2015 | 2015 | | see web archive for doc | |
| dragonfly | http://www.leo | beta | LEOX team | MISC | 16 | 16 | kintex-7-3 | James Brakef | | 788 | 6 | | | 164 | ## | 14.7 | 0.67 | 1.0 | 139.3 | X | | vhdl | 6 | dgf_core | Y | | N | | 256 | 2K | | | | | | 2001 | | | unusual, uses FIFOs | |
| minicpu-s | https://github.c | stable | Michael Morris | stack | 16 | 8 | kintex-7-3 | James Brakef | | 147 | 6 | | | 741 | ## | 14.7 | 0.67 | 28.0 | 120.6 | X | | verilog | 2 | both | Y | | N | | | | | 33 | | | | 2012 | 2013 | | separate source for each CPLD chip, u | fits (2) XC9500 CPLD |
| tigli_cpu | | stable | Cleiton Juffo | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 636 | 6 | | | 455 | ## | 14.7 | 0.67 | 4.0 | 119.7 | X | | verilog | 24 | cpu | Y | | N | Y | 64K | 64K | | 16 | | 16 | | 2013 | 2013 | | course project, not pipelined | no LUT RAM for reg file |
| hpc-16 | https://opencor | beta | Umair Siddiqui | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 871 | 6 | | | 152 | ## | 14.7 | 0.67 | 1.0 | 116.6 | X | | vhdl | 20 | cpu | Y | asm | N | | 64K | 64K | | | | 16 | | 2005 | 2015 | | | |
| minicpu | http://www.cs.h | stable | Hirotsugu Nakano | stack | 16 | 5 | kintex-7-3 | James | lots of | 433 | 6 | 1 | 1 | 128 | ## | 14.7 | 0.33 | 1.0 | 97.7 | X | | verilog | 7 | minicpu | Y | yes | N | | 4K | 4K | N | 26 | | | | 2008 | 2018 | | same as tiny-cpu | uses Flex, Bison & Perl to create gcc compiler |
| lem16_18 | | alpha | James Brakefield | accum | 16 | 18 | kintex-7-3 | James Brakef | | 483 | 6 | | 1 | 294 | ## | 14.5 | 0.16 | 1.0 | 97.4 | X | | vhdl | 2 | lem16_18m | | | N | | 256 | 1K | | 77 | | | 1 | 2010 | 2018 | | variable bit-length memory read/writ | op-codes coded, untested |
| multicycle_risc | https://github.c | stable | Yash Sanjay Bhalgat | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 1470 | 6 | | | 213 | ## | 14.7 | 0.67 | 1.0 | 97.0 | X | | verilog | 62 | risc15 | Y | | N | | 64K | 64K | | 15 | | 8 | | 2015 | 2015 | | multi-cycle IIT-B-RISC15 ISA | developed on Altera, course project |
| c16too | https://www.sc | stable | Cole Design and Devel | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 510 | 6 | | | 271 | ## | 14.7 | 0.67 | 4.0 | 88.9 | X | | vhdl | 1 | core | Y | asm | N | | 64K | 64K | N | 20 | | 8 | | 2003 | | coledd.com/electr | graphics capability | clock/2 and six phases |
| dcpu16 | https://github.c | beta | Shawn Tan, Marcus Pe | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 662 | 6 | 1 | | 318 | ## | 14.7 | 0.67 | 4.0 | 80.4 | X | | vhdl & v | 5 | dcpu16_c | Y | asm | N | N | 64K | 64K | N | 37 | | 8 | | 2009 | 2012 | https://en.wikipe | for the 0X10c game | 4+ addressing modes, 4 & 5-bit reg /modefield |
| ep994a | https://github.c | stable | Erik Piehl | 9900 | 16 | 16 | kintex-7-3 | James Brakef | | 1340 | 6 | | 5 | 286 | ## | 14.7 | 0.83 | 3.0 | 59.0 | X | | vhdl | 10 | ep994a | Y | yes | N | N | 64K | 64K | Y | | | 16 | | 2016 | 2019 | https://hackaday. | TI 990 emulation | also tms9902 (uart) core by Paul Urbanus? |
| verilog-65C02 | https://github.c | alpha | Arlet Ottens | 6502 | 16 | 8 | kintex-7-3 | James | remov | 599 | 6 | | 2 | 204 | ## | 14.7 | 0.67 | 4.0 | 57.1 | | | verilog | 5 | gop16 | | yes | N | N | 4G | 4G | | | | | | 2011 | 2018 | http://forum.6502 | 16-bit data RAM "bytes" | boot ROM mapped to LUTs? |
| oc54x | https://opencor | beta | Richard Herveille | DSP | 16 | 16 | kintex-7-3 | James Brakef | | 2225 | 6 | 1 | | 180 | ## | 14.7 | 0.67 | 1.0 | 54.1 | X | | verilog | 10 | oc54_cpu | Y | yes | N | Y | 64K | 64K | | | | | | 2002 | 2009 | | 40-bit accumulator, barrel shifter | C54x clone |
| forth-cpu/h2 | https://opencor | stable | Richard Howe | forth | 16 | 16 | kintex-7-3 | James Brakef | | 1858 | 6 | | 9 | 149 | ## | 14.7 | 0.67 | 1.0 | 53.8 | X | Y | vhdl | 11 | top | | | | | 64K | 64K | | 25 | | | | 2017 | 2020 | https://github.cor | H2 Forth SoC, VHDL reads *.hex & *.b | derived from J1, hex & bin files in 2/16/2018 ta |
| cole_c16 | https://www.sc | beta | Cole Design & Develop | RISC | 16 | 16 | spartan-6-3 | James Brakef | | 554 | 6 | | | 298 | ## | 14.7 | 0.67 | 7.0 | 51.4 | X | | vhdl | 1 | core | Y | asm | N | | 64K | 64K | N | 20 | | 8 | | 2002 | 2012 | https://blog.class | (7) clks per inst, complete SOC | |
| microcore120 | http://www.pld | beta | Klaus Schleisiek | forth | 16 | 8 | kintex-7-3 | James Brakef | | 1101 | 6 | | | 168 | ## | 14.7 | 0.67 | 2.0 | 51.1 | X | | vhdl | 17 | ucore | Y | asm | N | Y | 4K | 4K | | | | | | 1999 | 2004 | | indexing into return stack, auto inc/d | no block RAM?, uses tri-state signals |
| uTTA | | stable | Hans Tiggeler | TTA | 16 | 16 | kintex-7-3 | James Brakef | | 810 | 6 | 1 | | 57 | ## | 14.7 | 0.67 | 1.0 | 47.4 | X | | vhdl | 23 | utta_struc | N | asm | N | | | | | | | | | | | http://www.ht-lat | time triggered arch | bad weblink |
| c-nit | http://www.c-n | stable | Sumit | RISC | 16 | 16 | spartan-3-5 | James | xilinx L | 752 | 4 | | 3 | 100 | ## | 14.7 | 0.67 | 2.0 | 44.5 | X | | verilog | 6 | soc | on | asm | N | N | 64K | 64K | Y | 22 | | 15 | | 2003 | 2004 | | RISC with several load/store modes | |
| bobcat | | beta | Stan Drey | DSP | 16 | 24 | kintex-7-3 | James Brakef | | 1622 | 6 | 1 | | 107 | ## | 14.7 | 0.67 | 1.0 | 44.0 | X | | vhdl | 30 | bobcat_co | Y | | N | | 64K | 64K | | | | | | 1998 | 2000 | | | dead web links |
| neo430 | https://opencor | alpha | Stephan Nolting | MSP430 | 16 | 16 | virtex-6 | Stephan Nolt | | 402 | 6 | | 2 | 204 | ## | 14.7 | 0.67 | 8.0 | 42.5 | IX | | vhdl | 19 | neo430_t | Y | yes | N | | 28K | 32K | Y | | | 16 | | 2015 | 2020 | https://github.cor | website has detailed resource untiliz | minimal configuration |
| blue | https://opencor | stable | Al Williams | accum | 16 | 16 | spartan-3-5 | James | remov | 1025 | 4 | | | 63 | ## | 14.7 | 0.67 | 1.0 | 41.1 | X | | verilog | 16 | topbox | web | | N | N | 4K | 4K | N | 16 | | 2 | | 2009 | 2010 | | derived from Caxton Foster's Blue | http://www.youtube.com/watch?v=dt4zezZP8 |
| cd16 | http://anycpu.o | stable | Brad Eckert | forth | 16 | 16 | spartan-3-5 | James Brakef | | 681 | 4 | | | 83 | ## | 14.7 | 0.67 | 2.0 | 41.0 | IX | B | vhdl | 16 | cd16 | | | N | | 128K | 8M | | | | | | 2003 | 2003 | http://web.archiv | Spartan-3 block RAM | bare core |
| xgate | https://opencor | alpha | Robert Hayes | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 2778 | 6 | | | 159 | ## | 14.7 | 0.67 | 1.0 | 38.3 | X | | verilog | 7 | xgate_top | Y | | N | | | | | 42 | | 16 | | 2009 | 2013 | | high pin count | Freescale XGATE co-processor compatible |
| aap | https://github.c | stable | Simon Cook | RISC | 16 | 16 | arria-2 | James Brakef | | 7193 | A | | | 393 | ## | q18.0 | 0.67 | 1.0 | 36.6 | I | | verilog | 7 | de0_nano | Y | yes | | Y | 64K | 16M | Y | | | 64 | | 2015 | 2016 | http://www.embe | includes Altera project | 4 to 64 reg, 24-bit pc, no status reg |
| jop | https://opencor | stable | Martin Schoeberl etal | forth | 16 | 16 | cyclone-1 | Martin Schoe | | 2000 | 4 | | | 100 | | q10.0 | 0.67 | 1.0 | 33.5 | I | | vhdl | 11 | core | Y | yes | N | | 256K | 256K | | | | | | 2004 | 2014 | | https://github.com/jop-devel/jop | java app builds some source code files |
| openmsp430 | https://opencor | stable | Oliver Girard | MSP430 | 16 | 16 | stratix-3-2 | Oliver Girard | | 1147 | A | 1 | | 98 | | | 0.67 | 2.0 | 28.5 | IX | | verilog | 30 | openMSP4 | Y | yes | N | N | 64K | 64K | Y | | | 16 | | 2009 | 2018 | | near cycle accurate | performance spreadsheet |
| w11 | https://opencor | alpha | Walter Mueller | PDP11 | 16 | 16 | kintex-7-3 | James Brakef | | 1760 | 6 | 1 | 1 | 147 | ## | 14.7 | 0.67 | 2.0 | 28.0 | X | Y | vhdl | 118 | pdp11_co | Y | yes | N | N | 4M | 4M | Y | 70 | 13 | 8 | | 2010 | 2019 | https://github.cor | Boots UNIX, has MMU & cache, retro | PDP-11/70 CPU core and SoC |
| a2z | https://hackada | stable | | RISC | 16 | 24 | cyclone-4 | James Brakef | | 1524 | 4 | 1 | 12 | 62 | ## | q17.0 | 0.67 | 1.0 | 27.4 | I | | verilog | | top_a2z | | | | | | | | | | | | 2016 | 2018 | | | |
| t180-cpu | | stable | Leonard Brandwein | accum | 16 | 8 | kintex-7-3 | James | bypass | 709 | 6 | | | 83 | ## | 14.7 | 0.67 | 3.0 | 26.2 | X | | vhdl | 23 | cpu | Y | | N | N | 64K | 64K | Y | 182 | | | | 2016 | 2016 | https://www.vtto | 8-bitter with pc, sp, a, b, c & d regs | based on Viktor Toth's 4 bit microcontroller |
| stack_machine | http://people.ec | stable | Bruce R. Land | forth | 16 | 5 | cyclone10 | James Brakef | | 5101 | 4 | 6 | 29 | 66 | ## | q18.0 | 0.67 | 0.3 | 25.9 | X | | verilog | 9 | VGA_sram | Y | asm | N | N | 64K | 4K | N | | | | | 2009 | 2011 | https://people.ec | (3) uP cores, Cornell course material | VGA output, uses Nakano's tiny_cpu |
| msp430_vhdl | https://opencor | beta | Peter Szabo | MSP430 | 16 | 16 | kintex-7-3 | James Brakef | | 1735 | 6 | | | 127 | ## | 14.7 | 0.67 | 2.0 | 24.5 | IX | | vhdl | 9 | cpu | Y | yes | N | | 64K | 64K | Y | | | 16 | | 2014 | 2017 | | Comprehensive verification was not | compiles on cyclone II |
| dme | https://github.c | stable | ErwinM | RISC | 16 | 16 | kintex-7-3 | James Brakef | | 1755 | 6 | | | 53 | ## | 14.7 | 0.67 | 1.0 | 20.4 | X | | verilog | 49 | cpu | Y | yes | N | | 64K | 64K | Y | 40 | | 8 | | 2016 | 2017 | | based on magic-16 | computer & computer2 null dsgns: no outputs |
| sub86 | https://opencor | alpha | Jose Rissetto | x86 | 16 | 8 | kintex-7-3 | James Brakef | | 1916 | 6 | | | 172 | ## | 14.7 | 0.67 | 3.0 | 20.1 | X | | verilog | 1 | sub86 | Y | yes | N | N | 64K | 64K | Y | | | 7 | | 2012 | 2013 | | very small x86 subset core | no segment registers, limited op-codes |
| **mcl86** | http://www.mic | stable | Ted Fried | x86 | 16 | 8 | kintex-7-3 | Ted Fried | | 308 | 6 | | 4 | 180 | | | 0.67 | 20.0 | 19.6 | X | | proprietary | | | Y | yes | N | N | 1M | 1M | Y | | | | | 2016 | | http://www.embe | **microcoded, meets original 8088 timing@100MHz** | |
| pdp11-34verilo | www.heeltoe.co | stable | Brad Parker | PDP11 | 16 | 16 | arria-2 | James Brakef | | 2532 | A | | | 126 | ## | q13.1 | 0.67 | 2.0 | 16.7 | IX | Y | verilog | 24 | pdp11 | Y | yes | N | N | 64K | 64K | | 70 | 13 | 8 | | 2009 | | | boots & runs RT-11, EIS inst & MMU | |
| s430 | https://www.p | stable | Paul Taylor | MSP430 | 16 | 16 | artix-7 | Paul Taylor | | 449 | 6 | | | 100 | | | 0.67 | 9.0 | 16.6 | | | vhdl | 1 | s430 | | | | | 64K | 64K | Y | | | | | 2019 | 2019 | | msp430 subset with 8-bit alu | coded for size & not for speed |
| v1_coldfire | https://www.sil | proprietar | IPextreme | 68000 | 16 | 16 | cyclone-3 | freescale | | 5000 | 4 | | | 80 | | | 0.89 | 1.0 | 14.2 | I | | verilog | | | Y | yes | N | N | 4G | 4G | Y | | | 16 | | 2008 | | https://www.silva | free for Altera | 3500 LUTs on Stratix-III |
| pdp2011 | http://pdp2011. | stable | Sytse van Slooten | PDP11 | 16 | 16 | kintex-7-3 | James Brakef | | 5060 | 6 | 1 | | 205 | ## | 14.7 | 0.67 | 2.0 | 13.6 | IX | Y | vhdl | 3 | cpu | Y | yes | Y | N | 64K | 64K | | 70 | 13 | 8 | | 2008 | 2019 | http://pdp2011.sy | SoC, build files for A&X boards | complete impl including orig IO devices |
| next186 | https://opencor | stable | Nicolae Dumitrache | x86 | 16 | 8 | arria-2 | James Brakef | | 1966 | A | 2 | | 77 | ## | q13.1 | 0.67 | 2.0 | 13.1 | IX | | verilog | 4 | Next186_( | Y | yes | N | N | 1M | 1M | Y | | | | | 2012 | 2013 | | boots DOS | |

| _uP_all_soft folder | opencores or prmary link | status | author | style / clone | data size | inst size | FPGA | repor ter | com ents | LUTs ALUT | LUT? | mults | blk ram | F max | date | tool ver | MIPS /inst | clks/ inst | KIPS /LUT | ven dor | SOC | src code | #src files | top file | doc | tool chai n | fltg pt | Hav'd | max dat | max inst | byte adrs | # inst | adr mod | # reg | pip e lea | start year | last revis | secondary web link | note worthy | comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| s80186 | https://github.c | stable | Jamie Iles | x86 | 16 | 8 | cyclone-V | Jamie Iles | | 1750 | A | | | 60 | | | 0.67 | 2.0 | 11.5 | I | Y | system v | 50 | core | Y | | N | | 1M | 1M | Y | | | | | 2017 | 2021 | https://www.jami | 80186 binary compatible core | implementing the full 80186 ISA |
| c16 | https://opencor | stable | Jsauermann | C | 16 | 8 | spartan-3-5 | James Brakef | | 1751 | 4 | | 16 | 57 | ## | 14.7 | 0.33 | 1.0 | 10.7 | X | | vhdl | 22 | Board_cp | mi | yes | N | | 64K | 64K | Y | | | 5 | | 2003 | 2012 | | 8080 derivative, optional UART, 8-bit | xilinx 4K RAM primitives |
| marca | https://opencor | stable | Wolfgang Puffitsch | RISC | 16 | 16 | arria-2 | James Brakef | | 1763 | A | | 22 | 157 | ## | q13.1 | 0.67 | 6.0 | 10.0 | I | | vhdl | 40 | marca | Y | | N | | 8K | 16K | | 75 | | 16 | 4 | 2007 | 2009 | | serial multiply & divide | clks/inst is approx |
| rtf8088 | https://opencor | planning | Robert Finch | x86 | 16 | 8 | kintex-7-3 | James Brakef | | 4514 | 6 | 4 | | 174 | ## | 14.7 | 0.67 | 3.0 | 8.6 | X | | verilog | 57 | rtf8088 | Y | yes | N | N | 1M | 1M | Y | | | | | 2012 | 2013 | https://github.cor | 8-bit memory data, e.g. 8088 | |
| ao68000 | https://opencor | beta | Aleksander Osman | 68000 | 16 | 16 | arria-2 | James Brakef | | 3479 | A | | 6 | 169 | ## | q13.1 | 0.67 | 4.0 | 8.1 | I | Y | verilog | 1 | ao68000 | bm | yes | N | | 4G | 4G | Y | | | | | 2010 | 2012 | | uses microcode, instruction prefetch | buffer |
| zet86 | https://opencor | alpha | Zeus Marmolejo | x86 | 16 | 8 | kintex-7-3 | James Brakef | | 3642 | 6 | 1 | | 68 | ## | 14.7 | 0.67 | 2.0 | 6.2 | X | | verilog | 32 | fpga_zet_ | Y | yes | N | N | 1M | 1M | Y | | | | | 2008 | 2018 | https://github.cor | equivalent to 80186, boots MS-DOS | Zet The x86 (IA-32) open implementation |
| tg68 | https://opencor | stable | Tobias Gubener | 68000 | 16 | 16 | kintex-7-3 | James Brakef | | 2331 | 6 | | | 44 | ## | 14.7 | 0.67 | 4.0 | 3.2 | X | | vhdl | 2 | TG68_fast | Y | yes | N | N | 4G | 4G | Y | | | 16 | | 2007 | 2012 | | TG68 - execute 68000 Code | for use with Minimig |
| pop11-40 | http://www.ip-s | simulation | Naohiko Shimizu | PDP11 | 16 | 16 | ep1K | Naohiko Shir | | 2687 | 4 | | | 20 | ## | | 0.67 | 2.0 | 2.5 | I | | NSL | 17 | top | Y | yes | | N | 64K | 64K | Y | 70 | 13 | 8 | | 2009 | | www.ip-arch.jp/in | Boots UNIX | various papers, no verilog or vhdl |
| k68 | https://opencor | alpha | Shawn Tan | 68000 | 16 | 16 | kintex-7-3 | James Brakef | | 2392 | 6 | | | 24 | ## | 14.7 | 0.67 | 4.0 | 1.7 | X | | verilog | 15 | k68_cpu | Y | yes | N | N | 4K | 4G | Y | | | 16 | | 2003 | 2009 | | 68K binary compatible | |
| suska-III | http://www.exp | beta | Wolfgang Forster | 68000 | 16 | 16 | arria-2 | James Brakef | | 7388 | A | | | 55 | ## | q13.1 | 0.67 | 4.0 | 1.3 | I | | vhdl | 11 | wf68k00ip | Y | yes | N | N | 4G | 4G | Y | | | 16 | | 2003 | 2013 | | for use as an Atari ST | |
| aoocs | https://github.c | beta | Aleksander Osman | 68000 | 16 | 16 | arria-2 | James Brakef | | 17852 | A | 2 | 43 | 57 | ## | q18.0 | 0.67 | 4.0 | 0.5 | I | Y | verilog | 22 | aoOCS | bm | yes | N | | 4G | 4G | Y | | | | | 2010 | 2011 | | uses ao68000 core, Amiga chip set en | Wishbone Amiga OCS SoC |
| acc | https://github.c | stable | Juan Gonzalez-Gomez | accum | 15 | 15 | kintex-7-3 | James | rom & | 88 | 6 | | 1 | 227 | ## | 14.7 | 0.67 | 2.0 | 865.2 | IX | | verilog | 1 | acc2 | Y | yes | N | | | 4K | | | | | 2016 | 2016 | https://github.cor | 26 chptr course using Apollo Comma | ??why LUT count different from agcnorm |
| agcnorm | https://opencor | beta | Dave Roberts | accum | 15 | 15 | spartan-3a | James Brakef | | 3732 | 4 | | 2 | 20 | ## | 14.7 | 0.66 | 1.0 | 3.5 | X | | vhdl | 5 | AGC | Y | | N | Y | 4K | 72K | N | 11 | | 1 | | 1962 | 2012 | http://klabs.org/h | Apollo Guidance Computer via 3-input | NOR gate emulation |
| cardiac | https://opencor | mature | Al Williams | accum | 13 | 12 | spartan-3-4 | James Brakef | | 557 | 4 | | | 71 | ## | 14.7 | 0.30 | 1.0 | 38.5 | X | | verilog | 16 | vtach | Y | asm | N | | 100 | 100 | N | 10 | | | | 2013 | 2019 | https://www.cs.di | CARDboard Illustrative Aid to Comput | 3 digit BCD arithmetic |
| wb4pb | https://opencor | stable | Stefan Fischer | picoBlaze | 13 | 13 | spartan-3 | Stefan Fische | | 309 | 4 | | 1 | 102 | ## | 14.7 | 0.33 | 3.0 | 36.2 | X | Y | vhdl or v | 14 | picoblaze_wb_uart | | | | Y | | | | | | | 2010 | 2013 | https://en.wikipe | software addon for picoBlazeSoftwar | kcpsm3 only works for Spartan 3 |
| usimplez | https://opencor | stable | Pablo Salvadeo etal | accum | 12 | 12 | stratix-2 | Pablo Salvade | | 48 | 4 | | | 134 | | q9.1 | 0.17 | 2.0 | 237.9 | I | | vhdl | 3 | usimplez_cpu | | | N | | 512 | 512 | | 8 | | | | 2011 | | http://www-gti.de | part of university course, simplez+i4 | has an index register |
| pdp8verilog | www.heeltoe.co | stable | Brad Parker | PDP8 | 12 | 12 | kintex-7-3 | James Brakef | | 505 | 6 | | | 366 | ## | 14.7 | 0.50 | 2.0 | 181.3 | X | | verilog | 18 | pdp8 | Y | yes | N | N | 32K | 32K | | | | 8 | | 2005 | 2010 | | boots & runs TSS/8 & Basic | |
| microcore110 | http://www.pld | beta | Klaus Schleisiek | forth | 12 | 8 | kintex-7-3 | James Brakef | | 399 | 6 | | 1 | 294 | ## | 14.7 | 0.40 | 2.0 | 147.4 | X | | vhdl | 30 | core | Y | asm | N | Y | 512 | 2K | | | | | | 1999 | 2004 | www.microcore.o | indexing into return stack, auto inc/d | only one block RAM? simplest core |
| the12X_12uP | | alpha | James Brakefield | stack/acc | 12 | 12 | kintex-7-3 | James Brakef | | 972 | 6 | 1 | 1 | 123 | ## | 14.7 | 0.50 | 1.0 | 63.3 | X | | vhdl | 2 | the12x_12 | Y | | | Y | N | 4K | 4K | N | 54 | | 64 | 1 | 2015 | | | combo stack/accumulater design | load/store arch, not optimized |
| pdp8 | https://opencor | alpha | Joe Manojlovick, Rob I | PDP8 | 12 | 12 | kintex-7-3 | James Brakef | | 1219 | 6 | 1 | | 183 | ## | 14.7 | 0.50 | 2.0 | 37.5 | X | Y | vhdl | 55 | cpu | Y | yes | N | N | 32K | 32K | | | | 8 | | 2012 | 2013 | | PDP-8 Processor Core and System | Boots OS/8, runs apps, several variants |
| pdp8l | https://opencor | beta | Ian Schofield | PDP8 | 12 | 12 | cyclone-3 | James Brakef | | 1088 | 4 | | 48 | 63 | ## | q13.1 | 0.50 | 2.0 | 14.4 | I | | vhdl | 11 | top | Y | yes | N | N | 4K | 4K | | | | | | 2013 | 2013 | | Minimal PDP8/L implementation with | 4K disk monitor system |
| eric5 | http://www.ent | proprietar | Thomas Entner | forth | 9 | 8 | cyclone-4-6 | entner-electr | | 110 | 4 | opt | | 60 | | | 0.42 | 1.0 | 229.1 | I | | proprietary | | | | | | | 512 | 1K | | | | 3-4 | | 2005 | 2011 | | 25 MIPS: ERIC5xs, ERIC5Q | |
| 8bit_chapman | http://www.ece | beta | Rob Chapman, Steven | forth | 8 | 8 | **zu-2e** | James | area o | 122 | 6 | | | 305 | ## | v20.1 | 0.33 | 1.0 | 824.7 | ILX | | vhdl | 10 | stack_pro | Y | | N | | 256 | 256 | Y | 24 | | | | 1998 | 1998 | | course work | |
| ssbcc | https://opencor | stable | Rodney Sinclair | forth | 8 | 9 | kintex-7 | Rodney Sincla | | 196 | 6 | | | 474 | | 14.7 | 0.33 | 1.0 | 797.9 | ILX | | verilog | 3 | core | Y | asm | N | Y | 1K | 8K | Y | 41 | | 3 | | 2012 | 2014 | https://github.cor | Python program generates the Verilo | inst after branch/call/rtn always execs |
| non-von-1 | http://www.chr | stable | Christopher Fenton | accum | 8 | 8 | kintex-7-3 | James Brakef | | 230 | 6 | | | 556 | ## | 14.7 | 0.33 | 1.0 | 797.1 | | | verilog | 1 | nonvontop | | no | N | | 64 | | Y | 30 | | | | | | | SIMID in tree structure | A & B regs, instructions broadcast |
| avr8 | https://opencor | beta | Nick Kovach | AVR | 8 | 16 | kintex-7-3 | James Brakef | | 174 | 6 | | | 418 | ## | 14.7 | 0.33 | 1.0 | 792.2 | X | | verilog | 1 | rAVR | Y | yes | N | | 64K | 64K | Y | 17 | | 4 | | 2010 | 2010 | | Reduced AVR Core for CPLD | not a full clone, doc is opencores page |
| mcpu | https://opencor | stable | Tim Boscke | accum | 8 | 8 | spartan-6-3 | James Brakef | | 41 | 6 | | | 384 | ## | 14.7 | 0.08 | 1.0 | 749.0 | X | | vhdl | 1 | tb02cpu2 | Y | asm | N | | 64 | 64 | Y | 4 | | | | 2007 | 2018 | https://github.cor | MCPU A minimal CPU for a CPLD | reduced MIPS/clk due to only 4 inst |
| mroell_cpu | https://bitbucke | stable | Matthias Roell | accum | 8 | 8 | kintex-7-3 | James | added | 185 | 6 | | | 357 | ## | 14.7 | 0.33 | 1.0 | 637.1 | X | | vhdl | 8 | cpu | Y | | | | | | | 10 | | | | 2014 | 2016 | | university course project | |
| myrisc1 | | stable | Muza Byte | RISC | 8 | 8 | arria-2 | James Brakef | | 121 | A | | 2 | 231 | ## | q13.1 | 0.33 | 1.0 | 628.7 | I | | verilog | 1 | myRISC1 | Y | | N | Y | 256 | 256 | Y | 16 | | 4 | | 2011 | 2011 | | Verilog source included in PDF file | LPM macros |
| riscuva1 | https://www.sc | stable | S. de Pablo | picoBlaze | 8 | 14 | kintex-7-3 | James Brakef | | 109 | 6 | | | 370 | ## | 14.7 | 0.33 | 2.0 | 560.7 | X | | verilog | 1 | riscuva1 | bme | | N | Y | 256 | 1K | Y | 35 | | | | 2006 | 2006 | https://github.cor | Verilog source included in PDF file | also VHDL version by Bikash Gogoi with identic |
| lwrisc | https://github.c | stable | Li Wu | accum | 8 | 12 | arria-2 | James Brakef | | 88 | A | | 1 | 230 | ## | q13.1 | 0.17 | 1.0 | 443.6 | I | | verilog | 9 | risc_core | | asm | N | Y | 1K | 2K | Y | 16 | | | | 2008 | 2009 | | ClaiRISC simplified PIC, 4 reg rtn stack | absolute addressing only, lowered MIPS/clk |
| popcorn | http://www.fpg | stable | Jeung Joon Lee | accum | 8 | 8x | kintex-7-3 | James Brakef | | 267 | 6 | | | 347 | ## | 14.7 | 0.33 | 1.0 | 428.4 | X | | verilog | 4 | pc | Y | | N | | 64K | 64K | Y | 43 | | | | 1998 | 2000 | | small 8 bit uP | |
| td4 | https://github.c | stable | cielo_ee | accum | 8 | 8 | spartan-3 | James Brakef | | 102 | | | | 200 | ## | 14.7 | 0.20 | 1.0 | 392.2 | X | | verilog | 5 | td4_top | | | | | | 16 | Y | | | | | 2012 | 2015 | | | very small uP |
| cosmac | https://github.c | beta | Eric Smith | 1802 | 8 | 8 | kintex-7-3 | James Brakef | | 244 | 6 | | | 270 | ## | 14.7 | 0.33 | 1.0 | 365.5 | X | | vhdl | 1 | cosmac | Y | asm | N | N | 64K | 64K | Y | 100 | | 16 | | 2009 | 2020 | | AKA COSMAC ELF of 1976 | Fmax is for bare core, runs CamelForth |
| mcu8 | https://opencor | alpha | Dimo Pepelyashev | accum | 8 | 8 | kintex-7-3 | James Brakef | | 274 | 6 | | | 299 | ## | 14.7 | 0.33 | 1.0 | 360.1 | X | | vhdl | 16 | processor_E | | asm | | | 256 | 256 | Y | 17 | | | | 2008 | 2009 | | asm, simulated, builds? | |
| picoblaze | https://www.xil | stable | Ken Chapman | picoBlaze | 8 | 18 | kintex-7-3 | James Brakef | | 110 | 6 | | 2 | 217 | ## | 14.7 | 0.33 | 2.0 | 325.5 | X | | vhdl | 1 | kcspm6 | Y | asm | N | | 256 | 2K | Y | | | | | 2003 | | https://en.wikipe | 2 clocks/inst, no prog ROM | this is the original picoBlaze author |
| nocpu | https://github.c | beta | John Tzonevrakis | RISC | 8 | 8 | kintex-7-3 | James Brakef | | 175 | 6 | | | 243 | ## | 14.7 | 0.33 | 1.5 | 306.1 | X | | verilog | 5 | cpu | N | no | N | | 256 | 256 | Y | | | 4 | | | | | minimal & complete | 8 ALU inst, 3 port reg file |
| ahmes | https://github.c | stable | Fabio Pereira | accum | 8 | 8 | kintex-7-3 | James Brakef | | 186 | 6 | | | 476 | ## | 14.7 | 0.33 | 3.0 | 281.6 | X | B | vhdl | 3 | ahmes | | | N | N | 256 | 256 | Y | 15 | 1 | | | 2016 | 2017 | http://embeddedsystems.io/ahmes-a-simple-8-bit-cpu-i | bare CPU with no RAM | |
| tinycpu | https://opencor | alpha | Jordan Earls | RISC | 8 | 8 | arria-2 | James Brakef | | 136 | A | | | 384 | ## | q13.1 | 0.17 | 2.0 | 235.5 | IX | | vhdl | 2 | tinycpu | | asm | N | N | 1K | 1K | | 12 | | 4 | | 2012 | 2012 | directory contains | subset of 6502 | MIPS/inst reduced due to few inst |
| parwan | | stable | Zainalabedin Navabi | accum | 8 | 8 | kintex-7-3 | James Brakef | | 157 | 6 | | | 435 | ## | 14.7 | 0.33 | 4.0 | 228.5 | X | | verilog | 16 | par_beh | Y | yes | N | N | 4K | 4K | Y | | | | | 1995 | 1997 | 2nd uP in director | from VHDL: Analysis and Modeling of | AKA cpu8, both vhdl & verilog versions |
| gumnut | http://digitaldes | stable | Peter Ashenden | RISC | 8 | 18 | kintex-7-3 | James Brakef | | 388 | 6 | | | 259 | ## | 14.7 | 0.33 | 1.0 | 220.7 | IX | | verilog | 6 | gumnut-rt | Y | asm | N | Y | 256 | 4K | Y | | | 8 | | 2007 | | | see Digital Design: An Embedded Systems Approach Using VHDL | |
| p16c5x | https://opencor | mature | Michael Morris | PIC16 | 8 | 14 | kintex-7-3 | James Brakef | | 378 | 6 | | | 252 | ## | 14.7 | 0.33 | 1.0 | 220.2 | IX | | verilog | 3 | P16C5x | Y | yes | N | Y | 256 | 4K | Y | | | | | 2013 | 2014 | | | |
| dfp | https://opencor | stable | Ron Chapman | forth | 8 | 8 | kintex-7-3 | James Brakef | | 297 | 6 | | | 192 | ## | 14.7 | 0.33 | 1.0 | 213.2 | X | | vhdl | 25 | DataFlowF | Y | | | | | | | | | | | 2003 | 2009 | | 8-bitter, generates a custom VHDL stack machine, compiler is in Forth | |
| 8bit-verilog_mcu | | stable | Josh Friend | accum | 8 | 8 | **zu-2e** | James | timing | 392 | 6 | | 1 | 500 | ## | v20.1 | 0.33 | 2.0 | 210.5 | X | | verilog | 11 | cpu | | | | | 512 | 512 | Y | 16 | | | | 2012 | 2012 | | for class project, small data stack | PB clock, students to add features |
| aizup/aizup_m | instruct1.cit.cor | stable | Yamin Li, Wanming Ch | RISC | 8 | 16 | arria-2 | James Brakef | | 298 | ## | | | | q13.1 | 0.17 | 2.0 | 205.4 | IX | | vhdl | 1 | cpu | | | N | N | 64K | 64K | | 16 | | 4 | | 1996 | 1998 | | used in Cornell EE475 course | MIPS/inst reduced due to few inst |
| **opc.opccpu** | https://github.c | stable | revaldinho | accum | 8 | 16 | kintex-7-3 | James | reduce | 101 | 6 | | | 526 | ## | 14.7 | 0.15 | 4.0 | 195.4 | X | | verilog | 2 | opccpu | Y | asm | N | N | 256 | 2K | Y | 13 | 3 | | | 2017 | 2019 | https://revaldinho | OPC1 one page computer for CPLD | **see hackaday One Page Computing Challe** |
| ppx16 | https://github.c | stable | Daniel Wallner | PIC16 | 8 | 14 | kintex-7-3 | James | missin | 409 | 6 | | | 238 | ## | 14.7 | 0.33 | 1.0 | 192.1 | X | | vhdl | 10 | P16C55 | Y | yes | N | Y | 256 | 4K | Y | | | | | 2002 | 2009 | | both 16C55 & 16F84 | with fake instruction PWM |
| opc.opc2cpu | https://github.c | stable | revaldinho | accum | 8 | 16 | kintex-7-3 | James | reduce | 117 | 6 | | | 556 | ## | 14.7 | 0.15 | 4.0 | 178.1 | X | | verilog | 2 | opc2cpu | Y | asm | N | N | 256 | 1K | Y | 12 | 3 | | | 2017 | 2019 | https://revaldinho | OPC2 revised OPC1, for XC9572 CPLD | see hackaday One Page Computing Challenge |
| risc16f84 | https://github.c | stable | John Clayton | PIC16 | 8 | 14 | kintex-7-3 | James Brakef | | 375 | 6 | | | 392 | ## | 14.7 | 0.33 | 2.0 | 172.5 | IX | | verilog | 1 | risc16f84 | Y | yes | N | Y | 256 | 4K | Y | | | | | 2002 | 2018 | | derived from CQPIC by Sumio Moriok | other variants with RTL |
| lipsi | https://github.c | stable | Martin Schoeberl | accum | 8 | 8 | cyclone4 | Martin Schoe | | 162 | 4 | | 1 | 162 | | | 0.17 | 1.0 | 167.0 | | | scala | 2 | | | Y | | N | N | 64K | 64K | Y | 9 | 3 | 16 | | 2017 | 2019 | https://github.cor | goal is 100 LUTs, program mapped to | "Lipsi, a very tiny processor" |
| pic_coonan | | alpha | Tom Coonan | PIC16 | 8 | 14 | kintex-7-3 | James Brakef | | 328 | 6 | | 1 | 165 | ## | 14.7 | 0.33 | 1.0 | 166.1 | X | | verilog | 7 | piccpu | Y | yes | N | Y | 256 | 4K | Y | | | | | 1999 | | | | risc8 by Tom Coonan also a PIC uP |
| aizup/aizup_pi | instruct1.cit.cor | stable | Yamin Li, Wanming Ch | RISC | 8 | 16 | kintex-7-3 | James Brakef | | 198 | 6 | | | 375 | ## | 14.7 | 0.17 | 2.0 | 157.9 | IX | | vhdl | 1 | cpu | | asm | N | N | 64K | 64K | Y | 16 | | 4 | | 1996 | 1998 | | used in Cornell EE475 course | MIPS/inst reduced due to few inst |
| brainfuckcpu | https://opencor | beta | Aleksander Kaminski | mem | 8 | 3 | kintex-7-3 | James Brakef | | 110 | 6 | | | 432 | ## | 14.7 | 0.08 | 2.0 | 157.2 | X | | verilog | 1 | brainfuck_cpu | | | N | Y | | | | 8 | | 0 | | 2014 | 2015 | http://www.cliffo | Touring machine like, 2ndary link is a | adj prog & data mem size, terrible name |
| classy_core_17 | https://github.com/classy | stable | Andreas Schweizer | AVR | 8 | 16 | spsrtan-3 | Andr | | 358 | 4 | | | 164 | ## | 14.7 | 0.33 | 1.0 | 151.2 | | | vhdl | 8 | top | Y | yes | N | | 64K | 128K | Y | 72 | | 32 | | | 2019 | https://blog.classy | adjust to some custom logic | Implementing a CPU in VHDL parts 1..3 |
| tisc | https://opencor | beta | Vincent Crabtree | accum | 8 | 8 | kintex-7-3 | James Brakef | | 195 | 6 | | | 87 | ## | 14.7 | 0.33 | 1.0 | 147.1 | X | | vhdl | 1 | TISC | | | N | | 256 | 1K | Y | | | 2 | | 2009 | 2009 | | Tiny Instruction Set Computer | minimal accumulator machine |
| inst_list_proce | https://opencor | planning | Mahesh Palve | accum | 8 | 15 | kintex-7-3 | James | using | 786 | 6 | | 1 | 340 | ## | 14.7 | 0.33 | 3.0 | 142.6 | X | | verilog | 34 | top | Y | | N | | 128 | 1K | | 32 | | | | 2014 | | | pipelined, state machine | UART, SPI & timer included |
| complete_8bit | https://www.qu | stable | Van-Lei Le | | 8 | 8 | kintex-7-3 | James | modifi | 208 | 6 | | 1 | 260 | ## | 14.7 | 0.33 | 3.0 | 137.5 | X | | vhdl | 6 | computer | N | | N | | 96 | 128 | Y | | | | | 2016 | | | | memory_unit uses block RAM, IO ports prunec |
| synpic12 | | stable | Miguel Angel Ajo Pelay | PIC12 | 8 | 12 | kintex-7-3 | James Brakef | | 474 | 6 | | 1 | 197 | ## | 14.7 | 0.33 | 1.0 | 136.8 | IX | | vhdl | 7 | synpic12 | Y | yes | N | N | 256 | 2K | Y | | | | | 2011 | 2011 | http://projects.nb | CHDL to verilog | bad weblink |
| free_risc8 | https://web.arc | stable | Thomas Coonan | PIC16 | 8 | 14 | kintex-7-3 | James Brakef | | 355 | 6 | | | 142 | ## | 14.7 | 0.33 | 1.0 | 132.2 | X | | verilog | 8 | cpu | Y | yes | N | | 256 | 4K | Y | | | | | 2002 | 2011 | https://web.archive.org/web/20120309123835/http://www.mindspring.com/~tcoonan/index.html | | |
| fluid_core | https://opencor | alpha | Azmathmoosa | RISC | 8 | 12 | kintex-7-3 | James Brakef | | 956 | 4 | | | 381 | ## | 14.7 | 0.33 | 1.0 | 131.7 | X | | verilog | 17 | FluidCore | | | N | Y | | | | | | 8 | | 2015 | 2015 | | data width adj., mem sizes adj. | |
| pt13 | http://www.sing | stable | Daniel Ogilvie | accum | 8 | 8 | kintex-7-3 | James Brakef | | 301 | 6 | | | 357 | ## | 14.7 | 0.33 | 3.0 | 130.5 | | | verilog | 1 | pt13 | Y | asm | N | Y | 64K | 8K | Y | 40 | 3 | | | 2011 | 2018 | https://www.edn. | PT13 is optimized to be completely e | micro-code & register updates, minimal ISA |
| bytemachine | https://github.c | mature | c0pperdragon | forth | 8 | 8 | kintex-7-3 | James Brakef | | 319 | 6 | | 1 | 250 | ## | 14.7 | 0.33 | 2.0 | 129.3 | IX | | vhdl | 7 | bytemachi | bme | | N | N | | 4K | Y | 30 | | | | 2016 | 2017 | | top is Altera schematic | results are for 2016 bare core |
| aizup/aizup_ov | instruct1.cit.cor | stable | Yamin Li, Wanming Ch | RISC | 8 | 16 | kintex-7-3 | James Brakef | | 138 | 6 | | | 318 | ## | 14.7 | 0.17 | 3.0 | 128.3 | IX | | vhdl | 1 | cpu | | asm | N | N | 64K | 64K | Y | 16 | | 4 | | 1996 | 1998 | | used in Cornell EE475 course | MIPS/inst reduced due to few inst |
| open8_urisc | https://opencor | stable | Kirk Hays, Jshamlet | RISC | 8 | 8 | kintex-7-3 | James Brakef | | 691 | 6 | 1 | | 263 | ## | 14.7 | 0.33 | 1.0 | 125.6 | X | | vhdl | 9 | Open8 | Y | yes | N | | 64K | 64K | Y | | | 8 | | 2006 | 2020 | | accum & 8 regs, clone of Vautomation | uRISC processor, in use |
| up1232 | http://www.dte | stable | Santiago de Pablo | RISC | 8 | 16 | kintex-7-3 | James Brakef | | 220 | 6 | | | 244 | ## | 14.7 | 0.33 | 3.0 | 122.0 | X | | vhdl | 3 | up1232a | | | N | | 64K | 64K | Y | 33 | 2 | 32 | | 2000 | 2000 | | bare core, prog size 4K to 64K | description in source files |
| 8bit_piped_pr | https://opencor | stable | Mahesh Sukhdeo Palve | RISC | 8 | 16 | kintex-7-3 | James | swapp | 1049 | 6 | | 1 | 370 | ## | 14.7 | 0.33 | 1.0 | 116.4 | X | | verilog | 28 | top | Y | | | | | | | 20 | | 16 | | 2013 | 2017 | https://github.cor | uses Perl as assembler | use Perl to generate ROM file |
| nanoblaze | https://opencor | beta | Francois Corthay | picoBlaze | 8 | 18 | kintex-7-3 | James Brakef | | 247 | 6 | | 1 | 169 | ## | 14.7 | 0.33 | 2.0 | 113.2 | X | | vhdl | 12 | nanoblaze | | asm | | | 256 | 2K | Y | | | | | 2015 | 2015 | | nanoBlaze compatable, adjustable data width | |
| pacoBlaze | www.bleyer.org | mature | Pablo Kocik | picoBlaze | 8 | 18 | spartan-3 | Pablo Kocik | | 177 | 4 | | 1 | 117 | | | 0.33 | 2.0 | 109.1 | X | | verilog | 18 | pacoblaze | Y | asm | N | | 256 | 2K | Y | 57 | | | 2 | | 2006 | | 3 versions, behavioral coding | |
| sap | https://opencor | stable | Ahmed Shahein | accum | 8 | 8 | kintex-7-3 | James | no LU | 48 | 6 | | | 200 | ## | 14.7 | 0.10 | 4.0 | 104.2 | X | | vhdl | 15 | mp_struct | | | N | | 16 | 16 | Y | 5 | | | | 2012 | 2017 | https://shirishkoir | Simple as Possible Computer from Ma | https://www.youtube.com/watch?v=prpvEFxZ |
| qs5-rible | http://www.san | stable | John Rible | RISC | 8 | 16 | kintex-7-3 | James Brakef | | 468 | 6 | | | 135 | ## | 14.7 | 0.33 | 1.0 | 95.3 | X | | verilog | 1 | qs5_mix | | | N | | 256 | 32K | Y | | | | | 1998 | 1999 | | used in his class, also uses eP32 | |
| tinyfpga | https://github.c | stable | Ken Jordan | accum | 8 | 8 | kintex-7-3 | James Brakef | | 185 | 6 | | 1 | 175 | ## | 14.7 | 0.33 | 3.6 | 86.9 | X | | vhdl | 12 | system | | | N | N | 16 | 16 | Y | 10 | | | | 2017 | 2017 | | educational 8-bitter with 4-bit addres | why use block RAM? |
| fpga4_8bit_up | http://www.fpg | stable | Van Loi Le | accum | 8 | 8 | kintex-7-3 | James Brakef | | 258 | 6 | | 1 | 200 | ## | 14.7 | 0.33 | 3.0 | 85.3 | X | | vhdl | 9 | computer | bme | | N | | 96 | 128 | Y | 10 | | 2 | | 2016 | 2016 | book: LaMeres Int | educational | 16 input & 16 output ports fill out 256 byte adr |
| risc8 | https://web.arc | stable | Tom Coonan | PIC16 | 8 | 12 | kintex-7-3 | James Brakef | | 355 | 6 | | | 154 | ## | 14.7 | 0.33 | 2.0 | 71.5 | X | | verilog | 8 | cpu | Y | yes | N | Y | 256 | 2K | Y | | | | | 1999 | 1999 | https://github.cor | excellent HTML doc | directory contains derivative design by anothe |
| navre | https://opencor | stable | Sebastien Bourdeaudu | AVR | 8 | 16 | kintex-7-3 | James Brakef | | 990 | 6 | | | 207 | ## | 14.7 | 0.33 | 1.0 | 69.0 | AILX | | verilog | 1 | softusb_n | Y | yes | N | | 64K | 64K | Y | 72 | | 32 | 2 | 2010 | 2013 | https://www.milk | AVR clone, part of www.milkymist.org | |
| uos | https://opencor | mature | Daniel Roggen | accum | 8 | 16 | kintex-7-3 | James Brakef | | 441 | 6 | | | 270 | ## | 14.7 | 0.33 | 3.0 | 67.4 | X | | vhdl | 14 | cpu | Y | | | | | | | | | 3 | 4 | | 2014 | 2017 | | UoS Educational Processor | inspired by x86 ISA |
| latticemico8 | http://www.latt | stable | Lattice Semiconductor | RISC | 8 | 18 | LFE2 | Lattice Semic | | 265 | 4 | | 1 | 104 | | | | 0.33 | 2.0 | 64.4 | ILX | | vhdl | 10 | isp8_core | Y | yes | N | | 256 | 4K | Y | | | 32 | | 2005 | 2010 | https://en.wikipe | 16 deep call stack, four configuration | tool kit: LMS for Diamond3.10 |
| **mcl65** | http://www.mic | stable | Ted Fried | 6502 | 8 | 8 | atrix-7-3 | Ted Fried | | 252 | 6 | | 2 | 196 | ## | 14.7 | 0.33 | 4.0 | 64.2 | X | | verilog | 1 | mcl65 | Y | yes | N | N | 64K | 64K | Y | | | | | 2017 | | | **microcoded, cycle exact** | **excellent micro-coding LUT counts** |
| erp | https://opencor | stable | Shahzadjk | RISC | 8 | 16 | spartan-3-5 | James Brakef | | 366 | 4 | 1 | 1 | 70 | ## | 14.7 | 0.33 | 1.0 | 63.5 | X | | verilog | 1 | ERPverilog | Y | | | | | | | 15 | | 6 | | 2004 | 2014 | | two report PDFs & one Verilog file | |
| ae18 | https://opencor | beta | Shawn Tan | PIC18 | 8 | 16 | arria-2 | James Brakef | | 1084 | A | 1 | | 207 | ## | q13.1 | 0.33 | 1.0 | 63.1 | ILX | | verilog | 1 | ae18_core | | yes | N | Y | 4K | 1M | | | | | | 2003 | 2009 | https://hackaday. | not 100% compatable | negative edge reset "clock" |
| ez8 | https://github.c | stable | Howard Mao | accum | 8 | 16 | kintex-7-3 | James | replac | 644 | 6 | | 2 | 233 | ## | 14.7 | 0.33 | 2.0 | 59.6 | X | | verilog | 13 | ez8_cpu | | | | | 256 | 4K | | | | | | 2014 | 2014 | http://zhehaomao.com/ | not sure inferred RAM correct? | |

| _uP_all_soft folder | opencores or prmary link | status | author | style / clone | data size | inst size | FPGA | reporter | comments | LUTs ALUT | LUT? | mults | blk ram | F max | date | tool ver | MIPS /inst | clks/ inst | KIPS /LUT | vendor | SOC | src code | #src files | top file | doc | tool chain | fltgpt | Hav'd | max dat | max inst | byte adrs | # inst | adr mod | # reg | pipe line | start year | last revis | secondary web link | note worthy | comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| light8080 | https://opencor | stable | Jose Ruiz, Moti Litoche | 8080 | 8 | 8 | kintex-7-3 | James | Brakef | 154 | 6 | | 1 | 247 | | 14.7 | 0.33 | 9.0 | 58.9 | IX | | verilog | 5 | i80soc | Y | yes | N | N | 64K | 64K | Y | | | | | 2007 | 2015 | | targeted to area, includes UART, inte | older versions have both VHDL & Verilog |
| copyblaze | https://opencor | stable | Abdallah Ellbrahimi | picoBlaze | 8 | 18 | kintex-7-3 | James | missin | 622 | 6 | | | 217 | ## | 14.7 | 0.33 | 2.0 | 57.5 | IX | | vhdl | 16 | cp_copybl | Y | asm | N | | 256 | 2K | Y | | | | | 2011 | 2016 | | wishbone extras | |
| minirisc | https://opencor | stable | Rudolf Usselmann | PIC16 | 8 | 14 | spartan-3 | Rudolf | Usseln | 460 | 4 | | | 80 | | | 0.33 | 1.0 | 57.4 | X | | verilog | 7 | risc_core_ | Y | yes | N | Y | 256 | 4K | Y | | | | | 2001 | 2012 | | | |
| tinyvliw8 | https://opencor | alpha | Oliver Stecklina | VLIW | 8 | 32 | kintex-7-3 | James | hacke | 895 | 6 | | | 149 | ## | 14.7 | 0.33 | 1.0 | 55.0 | X | | vhdl | 19 | sysarch | | | N | Y | 256 | 1K | Y | | | | | 2013 | 2020 | | tinyVLIW8 soft-core processor | bare core, Altera LPM for RAMs |
| avrtinyx61core | https://opencor | beta | Andreas Hilvarsson | AVR | 8 | 16 | kintex-7-3 | James | Brakef | 1243 | 6 | | | 194 | ## | 14.7 | 0.33 | 1.0 | 51.5 | X | | vhdl | 1 | mcu_core | | yes | N | | 64K | 128K | Y | 72 | | 32 | | 2008 | 2009 | | | |
| babyrisc | http://www.san | stable | John Rible | RISC | 8 | 16 | kintex-7-3 | James | Brakef | 468 | 6 | | | 141 | ## | 14.7 | 0.33 | 2.0 | 49.7 | X | | verilog | 1 | qs5_mix | Y | | N | | 64K | 64K | Y | 15 | | 8 | | 1997 | 1999 | http://www.sandj | part of a three class course | memory rd/wt & ALU per clock |
| 1802-pico-basi | https://github.c | beta | Steve Teal | 1802 | 8 | 8 | **zu-2e** | James | area o | 241 | 6 | | 2 | 427 | ## | v20.1 | 0.33 | 12.0 | 48.8 | LX | | vhdl | 6 | pico_basic | Y | yes | N | | 64K | 64K | Y | 52 | | 16 | | 2016 | 2016 | https://wiki.forth- | VHDL 1802 Core with TinyBASIC | tiny Basic in ROM, Interrupts & DMA not imple |
| aizup/aizup_se | instruct1.cit.cor | stable | Yamin Li, Wanming Ch | RISC | 8 | 16 | kintex-7-3 | James | Brakef | 136 | 6 | | | 313 | ## | 14.7 | 0.17 | 8.0 | 48.1 | IX | | vhdl | 1 | cpu | | asm | N | N | 64K | 64K | Y | 16 | | 4 | | 1996 | 1998 | | used in Cornell EE475 course | MIPS/inst reduced due to few inst |
| avr_hp | https://opencor | stable | Strauch Tobias | AVR | 8 | 16 | kintex-7-3 | James | 2 slot | 1554 | 6 | | | 223 | ## | 14.7 | 0.33 | 1.0 | 47.4 | X | | vhdl | 10 | avr_core_pr | | yes | N | | 64K | 128K | Y | 72 | | 32 | | 2010 | 2012 | | hyper pipelined (eg barrel) AVR | |
| nextz80 | https://opencor | stable | Nicolae Dumitrache | Z80 | 8 | 8 | kintex-7-3 | James | Brakef | 854 | 6 | | | 119 | ## | 14.7 | 0.33 | 1.0 | 46.0 | X | B | verilog | 3 | NextZ80C | Y | yes | N | N | 64K | 64K | Y | | | | | 2011 | 2019 | | | claim of 700 LUTs in Spartan-3 probably wrong |
| ax8 | https://opencor | stable | Daniel Wallner | AVR | 8 | 16 | spartan-6-3 | James | missin | 1549 | 6 | | 1 | 213 | ## | 14.7 | 0.33 | 1.0 | 45.3 | X | | vhdl | 14 | A90S1200 | | yes | N | | 64K | 128K | Y | 72 | | 32 | | 2002 | 2010 | | both A90S1200 & A90S2313 | inserted fake inst ROM |
| micro8a | http://members | beta | John Kent | accum | 8 | 16 | kintex-7 | James | Brakef | 531 | 6 | | | 204 | ## | 14.7 | 0.33 | 3.0 | 42.3 | X | | vhdl | 11 | Micro8 | Y | | N | N | 2K | 2K | Y | | | | | 2002 | 2002 | http://members.c | derived from Tim Boscke's mcpu | also micro8 and micro8b variants |
| t65 | https://opencor | stable | Daniel Wallner | 6502 | 8 | 8 | kintex-7-3 | James | Brakef | 575 | 6 | | | 291 | ## | 14.7 | 0.33 | 4.0 | 41.7 | IX | | vhdl | 7 | T65 | Y | yes | N | N | 64K | 64K | Y | | | | | 2002 | 2010 | | 6502, 65C02 & 65C816; wide use | |
| verilog-6502 | https://github.c | stable | Arlet Ottens | 6502 | 8 | 8 | kintex-7-3 | James | Brakef | 407 | 6 | | | 200 | ## | 14.7 | 0.33 | 4.0 | 40.6 | X | | verilog | 2 | cpu | | yes | N | N | 64K | 64K | Y | | | | | 2007 | 2018 | http://ladybug.xs4all.nl/arlet/fpga/6502/ | | |
| 68hc05 | https://opencor | stable | Ulrich Riedel | 6805 | 8 | 8 | **zu-2e** | James | area o | 1096 | 6 | | | 485 | ## | v20.1 | 0.33 | 4.0 | 36.5 | X | | vhdl | 1 | 6805 | | yes | N | N | 64K | 64K | Y | | | | | 2007 | 2009 | | | room for still better fmax |
| xmega_core | https://opencor | beta | Gheorghiu Iulian | AVR | 8 | 16 | kintex-7-3 | James | Brakef | 1116 | 6 | | | 120 | ## | 14.7 | 0.33 | 1.0 | 35.6 | X | | verilog | 34 | mega_cor | Y | yes | N | | 64K | 128K | Y | 72 | | 32 | | 2017 | 2018 | https://git.morgot | 8 AVR cores, 4 sets LUT counts poste | https://git.morgothdisk.com/VERILOG/VERILO |
| mxp | http://vectorblo | stable | VectorBlox Computing | vect | 8 | | zynq45-7 | vectorblox | | 39856 | 6 | 64 | 81 | 175 | ## | v17.2 | 1.00 | 0.1 | 35.1 | | | proprietary | | | Y | | | | | | | | | | 2012 | 2017 | http://www.ece.u | MXP Matrix Processor is a scalable so | LUT count for 8 lanes with custom inst |
| natalius_8bit_ | https://opencor | beta | Fabio Guzman | RISC | 8 | 16 | kintex-7-3 | James | Brakef | 232 | 6 | | 1 | 175 | ## | 14.7 | 0.11 | 3.0 | 27.7 | X | | verilog | 12 | natalius_p | Y | asm | N | Y | 256 | 2K | Y | 29 | | 8 | | 2012 | 2012 | | return stack & register file | 3 clocks/inst |
| bc6502 | http://finitron.c | beta | Robert Finch | 6502 | 8 | 8 | kintex-7-3 | James | Brakef | 619 | 6 | | | 197 | ## | 14.7 | 0.33 | 4.0 | 26.2 | X | | verilog | 18 | bc6502 | | yes | N | N | 64K | 64K | Y | | | | | 2012 | 2012 | | | bare source |
| avr_fpga | https://opencor | stable | Juergen Sauermann | AVR | 8 | 16 | kintex-7-3 | James | Brakef | 1606 | 6 | 1 | 6 | 120 | ## | 14.7 | 0.33 | 1.0 | 24.7 | X | | vhdl | 20 | cpu_core | Y | yes | N | | 64K | 128K | Y | 72 | | 32 | | 2009 | 2010 | | extended lecture on FPGA uP design | |
| free6502 | http://web.arch | stable | David Kessner | 6502 | 8 | 8 | kintex-7-3 | James | Brakef | 646 | 6 | | | 193 | ## | 14.7 | 0.33 | 4.0 | 24.6 | X | | vhdl | 5 | free6502 | Y | yes | N | N | 64K | 64K | Y | | | | | 1999 | 2000 | http://www.sprov | microcoded | |
| **mcl51** | http://www.mic | stable | Ted Fried | 8051 | 8 | 8 | artix-7-3 | Ted Fried | | 312 | 6 | | 2 | 180 | | | 0.33 | 8.0 | 23.8 | X | | proprietary | | | Y | yes | N | N | 64K | 64K | Y | | | | | 2016 | | | **micro-coded** | |
| 6809_6309 | https://opencor | beta | Alejandro Paz Schmidt | 6809 | 8 | 8 | zynq+ | James | fmax s | 1676 | 6 | | | 323 | ## | v18.2 | 0.33 | 3.0 | 21.2 | AILX | B | verilog | 5 | MC6809_c | Y | yes | N | N | 64K | 64K | Y | | | | | 2012 | 2015 | | 6309 op-codes not implemented | |
| m65c02 | https://opencor | mature | Michael Morris | 6502 | 8 | 8 | spartan-6-3 | James | Brakef | 466 | 6 | | 3 | 118 | ## | 14.7 | 0.33 | 4.0 | 20.8 | X | Y | verilog | 13 | M65C02 | Y | yes | N | N | 64K | 64K | Y | | | | | 2013 | 2020 | https://github.cor | also a m65c02a version | micro-coded via F9408 soft sequencer |
| ucpuvhdl | https://github.c | stable | Reed Foster | RISC | 8 | 16 | kintex-7-3 | James | 512 LU | 933 | 6 | | | 118 | ## | 14.7 | 0.33 | 2.0 | 20.8 | X | | vhdl | 29 | core | Y | asm | N | | 256 | 64K | Y | 12 | 2 | 7 | | 2016 | 2017 | https://github.cor | six tutorials on uCPUvhdl | using muCPUv2_1 of 3 upwards compatible de |
| system05 | https://opencor | beta | John Kent, David Burn | 6805 | 8 | 8 | kintex-7-3 | James | Brakef | 834 | 6 | | | 204 | ## | 14.7 | 0.33 | 4.0 | 20.2 | X | Y | vhdl | 10 | System05 | Y | yes | N | N | 64K | 64K | Y | | | | | 2003 | 2009 | http://members.optushome.com.au/jekent/ | | |
| altium/TSK165 | http://techdocs.proprietar | | Altium | PIC16 | 8 | 12 | spartan-3-5 | Altium | | 416 | 4 | | | 50 | | | 0.33 | 2.0 | 19.8 | AILX | | proprietary | | | Y | yes | N | Y | 256 | 4K | Y | | | | | 2004 | 2017 | CR0140.pdf, CR01 | frozen, asm, C, C++, schem, VHDL & V | default clock speed is 50MHz |
| avr_core | https://opencor | stable | Rusian Lepetenok | AVR | 8 | 16 | kintex-7-3 | James | Brakef | 2135 | 6 | | | 127 | ## | 14.7 | 0.33 | 1.0 | 19.7 | X | | verilog | 15 | avr_core | Y | yes | N | | 64K | 128K | Y | 72 | | 32 | | 2002 | 2017 | | VHDL core also | |
| pet_fpga | https://github.c | stable | Thomas Skibo | 6502 | 8 | 8 | kintex-7-3 | James | Brakef | 1052 | 6 | | | 242 | ## | 14.7 | 0.33 | 4.0 | 19.0 | X | | verilog | 1 | cpu6502 | Y | yes | N | N | 64K | 64K | Y | | | | | 2007 | 2011 | https://github.cor | for Commodore PET | |
| m65 | www.ip-arch.jp/ | stable | Naohiko Shimizu | 6502 | 8 | 8 | arria-2 | James | Brakef | 483 | A | | | 110 | ## | q13.1 | 0.33 | 4.0 | 18.8 | X | | sfl & TDF | 8 | m65cpu | Y | yes | N | N | 4K | 4K | Y | | | | | 2001 | 2002 | | | |
| ag_6502 | https://opencor | beta | Oleg Odintsov | 6502 | 8 | 8 | kintex-7-3 | James | Brakef | 824 | 6 | | | 176 | ## | 14.7 | 0.33 | 4.0 | 17.7 | ILX | | verilog | 2 | ag_6502 | | yes | N | N | 64K | 64K | Y | | | | | 2012 | 2012 | | verilog code generation, "phase level accurate" | |
| tv80 | https://opencor | mature | Guy Hutchison, Howar | Z80 | 8 | 8 | kintex-7-3 | James | Brakef | 1207 | 6 | | | 182 | ## | 14.7 | 0.33 | 3.0 | 16.6 | IX | | verilog | 6 | tv80n | Y | yes | N | N | 64K | 64K | Y | | | | | 2004 | 2018 | https://github.cor | derived from Daniel Wallner's T80, ASIC implementations | |
| pavr | https://opencor | alpha | Doru Cuturela | AVR | 8 | 16 | kintex-7-3 | James | Brakef | 2630 | 6 | | 1 | 132 | ## | 14.7 | 0.33 | 1.0 | 16.5 | X | | vhdl | 18 | pavr_cont | Y | yes | N | Y | 4K | 4M | Y | 72 | | 32 | 6 | 2003 | 2009 | | superset of AVR | |
| m16c5x | https://opencor | mature | Michael Morris | PIC16 | 8 | 14 | spartan-3-4 | Michael | Morr | 1217 | 4 | | 3 | 60 | ## | | 0.33 | 1.0 | 16.3 | X | Y | verilog | 3 | m16C5x | Y | yes | N | Y | 256 | 4K | Y | | | | | 2013 | 2014 | | SOC LUT count | core at P16C5X |
| jca | | stable | John Cronin | RISC | 8 | 32 | kintex-7-3 | James | replac | 3287 | 6 | 3 | 3 | 157 | ## | 14.7 | 0.33 | 1.0 | 15.8 | IX | Y | verilog | 17 | soc | | | | | | | | | | 16 | | | | has VGA controller, plays Pong | altera memories |
| apple2fpga | http://www.cs.c | stable | Stephen A Edwards | 6502 | 8 | 8 | **zu-2e** | James | area o | 1095 | 6 | | 8 | 195 | ## | v20.1 | 0.33 | 4.0 | 14.7 | IX | Y | vhdl | 19 | de2_top | Y | yes | N | Y | 64K | 64K | Y | | | | | 2007 | 2009 | | emulation of Apple II computer | replaced Altera PLL with stub |
| z80control | https://opencor | alpha | Tyler Pohl | Z80 | 8 | 8 | kintex-7-3 | James | Brakef | 1483 | 6 | | | 189 | ## | 14.7 | 0.33 | 3.0 | 14.0 | X | Y | verilog | 55 | top_de1 | Y | yes | N | N | 64K | 64K | Y | | | | | 2010 | 2012 | | Microprocessor targeting embedded | interfaces to DRAM, based on T80 core |
| 8051 | https://opencor | alpha | Simon Teran, Jakas | 8051 | 8 | 8 | **zu-2e** | James | area o | 1482 | 6 | | | 242 | ## | v20.1 | 0.33 | 4.0 | 13.4 | ILX | | verilog | 32 | oc8051_to | Y | yes | N | | 64K | 64K | Y | | | | | 2001 | 2016 | | 8051 core includes several on-chip peripherals, like timers and counters | |
| t80 | https://opencor | stable | Daniel Wallner | Z80 | 8 | 8 | kintex-7-3 | James | Z80 m | 1389 | 6 | | | 163 | ## | 14.7 | 0.33 | 3.0 | 12.9 | X | | vhdl | 5 | T80a | Y | yes | N | N | 64K | 64K | Y | | | | | 2002 | 2018 | | Z80, 8080 & gameboy inst sets, several usages | |
| dalton_8051 | www.cs.ucr.edu | stable | Tony Givargis | 8051 | 8 | 8 | kintex-7-3 | James | Brakef | 2725 | 6 | 1 | 1 | 105 | ## | 14.7 | 0.33 | 1.0 | 12.7 | X | | vhdl | 7 | i8051_all | Y | yes | N | N | 64K | 64K | Y | | | | | 1999 | 2003 | | ASIC | |
| gup | https://opencor | stable | Kevin Phillipson | 68HC11 | 8 | 8 | arria-2 | James | Brakef | 925 | A | 1 | 1 | 127 | ## | q13.1 | 0.33 | 4.0 | 11.3 | I | | vhdl | 25 | gator_upr | Y | yes | N | N | 64K | 64K | Y | | | | | 2008 | 2011 | https://www.mil.u | top level is schematic | |
| r8051 | https://github.c | stable | Li Xinbing | 8051 | 8 | 8 | kintex-7-3 | James | Brakef | 1031 | 6 | 1 | | 139 | ## | 14.7 | 0.33 | 4.0 | 11.1 | X | | verilog | 2 | r8051 | Y | yes | N | N | 64K | 64K | Y | | | | | 2015 | 2019 | | | |
| system11 | https://opencor | alpha | John Kent, David Burn | 68HC11 | 8 | 8 | kintex-7-3 | James | Brakef | 1218 | 6 | | | 153 | ## | 14.7 | 0.33 | 4.0 | 10.3 | X | Y | vhdl | 17 | cpu11 | Y | yes | N | N | 64K | 64K | Y | | | | | 2003 | 2009 | http://members.c | known bugs & untested instructions | |
| cpu8080 | https://opencor | stable | Scott Moore | 8080 | 8 | 8 | kintex-7-3 | James | Brakef | 1179 | 6 | | | 299 | ## | 14.7 | 0.33 | 9.0 | 9.3 | X | | verilog | 1 | m8080 | Y | yes | N | N | 64K | 64K | Y | | | | | 2006 | 2016 | | includes VGA display generator, three variants | |
| c88 | https://github.c | alpha | Daniiel Bailey | accum | 8 | 8 | kintex-7-3 | James | Brakef | 3088 | 6 | 2 | | 167 | ## | 14.7 | 0.33 | 2.0 | 8.9 | X | | vhdl | 25 | C88 | Y | asm | N | | 8 | 256 | Y | 10 | | 8 | | 2015 | 2015 | https://www.yout | only 8 memory locations | used 3658 Dff, doesn't infer block or LUT RAM |
| light52 | https://opencor | beta | Jose Ruiz | 8051 | 8 | 8 | kintex-7-3 | James | Brakef | 1022 | 6 | 1 | 1 | 154 | ## | 14.7 | 0.33 | 6.0 | 8.3 | IX | Y | vhdl | 8 | light52_m | Y | yes | N | N | 64K | 64K | Y | | | | | 2012 | 2018 | | targeted to balanced | ~ 6 clocks/inst |
| wb_z80 | https://opencor | stable | Brewster Porcella | Z80 | 8 | 8 | kintex-7-3 | James | Brakef | 2025 | 6 | | | 144 | ## | 14.7 | 0.33 | 3.0 | 7.8 | X | | verilog | 4 | z80_core_ | Y | yes | N | N | 64K | 64K | Y | | | | | 2004 | 2012 | | derived from Guy Hutchison TV80 | Wishbone High Performance Z80 |
| cpu6502_true | https://opencor | stable | Jens Gutschmidt | 6502 | 8 | 8 | kintex-7-3 | James | Brakef | 1678 | 6 | | | 159 | ## | 14.7 | 0.33 | 4.0 | 7.8 | X | | vhdl | 7 | r6502_tc | | yes | N | N | 64K | 64K | Y | | | | | 2008 | 2018 | | cycle accurate | |
| a-z80 | https://opencor | stable | Goran Devic | Z80 | 8 | 8 | kintex-7-3 | James | Brakef | 1186 | 6 | | | 24 | ## | 14.7 | 0.33 | 1.0 | 6.8 | IX | | verilog | 24 | z80_top_c | Y | yes | N | N | 64K | 64K | Y | | | | | 2014 | 2020 | https://github.cor | gate level reverse eng'd Z80 | Complete implementation of a Sinclair ZX Spec |
| t48 | https://opencor | stable | Arnim Laeuger | MCS-48 | 8 | 8 | cyclone-1 | Arnim | Laeuge | 738 | 4 | | 1 | 59 | | | 0.33 | 4.0 | 6.6 | IX | | vhdl | 70 | t48_core | Y | asm | N | | 256 | 1K | | | | | | 2004 | 2021 | | T48 uController | used in several projects |
| 68hc08 | https://opencor | stable | Ulrich Riedel | 6808 | 8 | 8 | **zu-2e** | James | area o | 1796 | 6 | | | 143 | ## | v20.1 | 0.33 | 4.0 | 6.5 | X | | vhdl | 1 | x68ur08 | | yes | N | N | 64K | 64K | Y | | | | | 2007 | 2009 | | | |
| atmega8_pong | https://fr.wikive | stable | Juergen Sauermann | AVR | 8 | 16 | spartan-3-5 | James | clock c | 2767 | 4 | 1 | 10 | 53 | ## | 14.7 | 0.33 | 1.0 | 6.3 | X | Y | vhdl | 37 | avr_fpga_ | Y | yes | N | | 64K | 64K | Y | 17 | | 4 | | 2017 | 2017 | | several projects using avr core | uses Sauermann core |
| t51 | https://opencor | stable | Andreas Voggeneder | 8051 | 8 | 8 | kintex-7-3 | James | Brakef | 1947 | 6 | 1 | | 147 | ## | 14.7 | 0.33 | 4.0 | 6.2 | IX | | vhdl | 17 | T8032 | Y | yes | N | N | 64K | 64K | Y | | | | | 2002 | 2010 | | 8052 & 8032 | 8032 SoC |
| pulserain | https://github.c | stable | PulseRain Tech LLC | 8051 | 8 | 8 | arria-2 | James | some s | 2376 | A | 2 | 41 | 130 | ## | q18.0 | 0.33 | 3.0 | 6.0 | I | | system v | 25 | FP51_fast | Y | yes | N | Y | 64K | 64K | Y | | | | | 2017 | 2018 | https://www.puls | 1 clk/inst, intended for Max10 | |
| system09 | https://opencor | stable | John Kent, David Burn | 6809 | 8 | 8 | kintex-7-3 | James | Brakef | 1631 | 6 | | 41 | 88 | ## | 14.7 | 0.33 | 3.0 | 6.0 | IX | Y | vhdl | 40 | cpu09l | Y | yes | N | N | 64K | 64K | Y | | | | | 2003 | 2021 | http://members.c | from John Kent web page | opencores download URL incorrect, use col E |
| fpga-64 | http://www.syn | stable | Peter Wendrich | 6502 | 8 | 8 | kintex-7-3 | James | Brakef | 2210 | 6 | | 2 | 156 | ## | 14.7 | 0.33 | 4.0 | 5.8 | X | Y | vhdl | 26 | fpga64_co | Y | yes | N | N | 64K | 64K | Y | | | 26 | | 2005 | 2008 | | Rendition of Commodore 64 | altera top level schematic |
| turbo8051 | https://opencor | beta | Dinesh Annayya | 8051 | 8 | 8 | kintex-7-3 | James | Brakef | 1985 | 6 | 1 | | 127 | ## | 14.7 | 0.33 | 4.0 | 5.3 | IX | | verilog | 74 | oc8051_to | Y | yes | N | N | 64K | 64K | Y | | | | | 2011 | 2016 | | includes perpherials | |
| ep8080 | https://github.c | beta | C.H. Ting | 8080 | 8 | 8 | kintex-7-3 | James | Brakef | 1276 | 6 | | | 184 | ## | 14.7 | 0.33 | 9.0 | 5.3 | X | | vhdl | 4 | ep80.vhd | Y | yes | N | N | 64K | 64K | Y | | | | | 2002 | 2016 | 8080 data sheets | initialized Lattice memory blocks | work related to eP16 |
| mycpu | http://www.my | mature | Dennis Kuschel | accum | 8 | 8 | kintex-7-3 | James | Brakef | 3428 | 6 | 1 | | 155 | ## | 14.7 | 0.33 | 3.0 | 5.0 | X | | vhdl | 28 | cpu_top | Y | | N | | 64M | 64M | Y | | | | | 2010 | | | originally in TTL | micro-coded |
| cast_8051 | http://www.cas | proprietar | CAST Inc | 8051 | 8 | 8 | virtex-6 | CAST I | 820 sli | 1800 | 6 | | 2 | 81 | ## | 12.1 | 0.33 | 3.0 | 5.0 | X | | proprietary | | | Y | yes | N | | 64K | 64K | Y | | | 32 | | | | http://www.cast-i | Cast has uP related IP | several versions, FPGA kits |
| hc11core | http://www.gm | stable | Green Mountain Comp | 68HC11 | 8 | 8 | kintex-7-3 | James | Brakef | 2190 | 6 | | | 127 | ## | 14.7 | 0.33 | 4.0 | 4.8 | X | | vhdl | 1 | hc11rtl | Y | yes | ? | N | 64K | 64K | N | 53 | | 8 | 2 | 2000 | | 6811 data sheets | restricted use license, with corrections | |
| z3 | https://opencor | stable | Charles Cole | CISC | 8 | 8 | arria-2 | James | Brakef | 3495 | A | 2 | | 141 | ## | q18.0 | 0.33 | 3.0 | 4.4 | I | | verilog | 3 | boss | Y | | | | | 128K | 128K | | | | | | 2014 | 2014 | https://en.wikipe | Infocom Z-Machine V3, youtube vide | http://inform-fiction.org/zmachine/standards/ |
| oms8051mini | https://opencor | alpha | Simon Teran, Dinesh A | 8051 | 8 | 8 | kintex-7-3 | James | Brakef | 1991 | 6 | 1 | 32 | 133 | ## | 14.7 | 0.33 | 5.0 | 4.4 | X | Y | verilog | 66 | digital_co | Y | yes | N | | 64K | 64K | Y | | | | | 2000 | 2018 | | | |
| df6805 | www.hitechglob | proprietar | Hitech Global | 6805 | 8 | 8 | stratix-1 | Hitech | Global | 1690 | 4 | | | 83 | | | 0.33 | 4.0 | 4.1 | I | | proprietary | | | Y | yes | N | N | 64K | 64K | Y | | | | | | | 6805 data sheets | | |
| socz80 | http://sowerbut | stable | Will Sowerbutts | Z80 | 8 | 8 | spartan-6-3 | James | constr | 2568 | 6 | | 15 | 93 | ## | 14.7 | 0.33 | 3.0 | 4.0 | X | | vhdl | 25 | top_level | Y | yes | N | N | 64K | 64K | Y | | | | | 2013 | 2014 | | based on Daniel Wallner's T80, for Papillio Pro board | |
| system6801 | https://opencor | stable | Michael L. Hasenfratz | 6801 | 8 | 8 | cyclone-3 | James | Brakef | 1507 | 4 | | 3 | 73 | ## | 14.7 | 0.33 | 4.0 | 4.0 | I | | vhdl | 15 | wb_cyclor | Y | yes | N | N | 64K | 64K | Y | | | | | 2003 | 2009 | http://members.c | based on John Kent's 6801 | tested on Apex20K, Cyclone & Straix boards |
| lattice6502 | https://opencor | beta | Ian Chapman | 6502 | 8 | 8 | kintex-7-3 | James | Brakef | 4942 | 6 | | | 214 | ## | 14.7 | 0.33 | 4.0 | 3.6 | X | | vhdl | 3 | ghdl_proc | Y | yes | N | N | 64K | 64K | Y | | | | | 2010 | 2010 | | targeted to LCMXO2280 | |
| z80soc | https://opencor | stable | Ronivon Costa | Z80 | 8 | 8 | spartan-3e | James | Brakef | 2474 | 4 | 2 | 19 | 78 | ## | 14.7 | 0.33 | 3.0 | 3.4 | IX | Y | vhdl | 19 | top_s3e | Y | yes | N | N | 64K | 64K | Y | | | | | 2008 | 2016 | | based on Daniel Wallner's T80 | |
| i8051 | | stable | Tony Givargis | 8051 | 8 | 8 | kintex-7-3 | James | Brakef | 2690 | 6 | 1 | 1 | 105 | ## | 14.7 | 0.33 | 4.0 | 3.2 | X | | vhdl | 9 | i8051_all | Y | yes | N | | 64K | 64K | Y | | | | | 1999 | 1999 | | author has book & course | Embedded System Design: A Unified Hardware |
| cpu86 | http://www.ht-l | beta | Hans Tiggeler | x86 | 8 | 8 | kintex-7-3 | James | Brakef | 3421 | 6 | 1 | | 127 | ## | 14.7 | 0.17 | 2.0 | 3.1 | X | | vhdl | 23 | cpu86_top | Y | yes | N | N | 1M | 1M | Y | | | | | 2002 | 2018 | http://www.ht-lat | 8088 clone | ht-labs offers several uP cores |
| mc8051 | http://www.ore | stable | Helmut Mayrhofer | 8051 | 8 | 8 | kintex-7-3 | James | Brakef | 3022 | 6 | 1 | | 83 | ## | 14.7 | 0.33 | 4.0 | 2.3 | X | | vhdl | 49 | mc8051cc | Y | yes | N | N | 256 | 64K | Y | | | | | 1999 | 2013 | www.oreganosyst | fast 8051, version available with floating-point by David Lundgren | |
| altium/TSK80x | http://techdocs.proprietar | | Altium | Z80 | 8 | 8 | spartan-3-5 | Altium | | 2558 | 4 | | | 50 | | | 0.33 | 3.0 | 2.2 | AILX | | proprietary | | | Y | yes | N | N | 64K | 64K | Y | | | | | 2004 | 2017 | CR0140.pdf, CR01 | frozen, asm, C, C++, schem, VHDL & V | default clock speed is 50MHz |
| bfcpu | http://www.cliff | stable | Clifford Wolf | Turing | 8 | 3 | kintex-7-3 | James | Brakef | 422 | 6 | | | 345 | ## | 14.7 | 0.01 | 4.0 | 2.0 | X | B | vhdl | 4 | cw6671 | Y | yes | N | N | 64K | 64K | Y | 8 | | | | 2003 | 2003 | https://en.wikipe | no accum, data pointer and bracketed | current version & earlier version |
| hd63701 | https://opencor | planning | Tsuyoshi Hasegawa | 6801 | 8 | 8 | spartan-6-3 | James | Brakef | 1412 | 6 | 1 | 3 | 31 | ## | 14.7 | 0.33 | 4.0 | 1.8 | X | | verilog | 6 | HD63701_CORE | | yes | N | N | 64K | 64K | Y | | | | | 2014 | | | Used in Atari game console, 6801 clone? | |
| system68 | https://opencor | stable | John Kent, David Burn | 6801 | 8 | 8 | spartan-3-5 | James | Brakef | 2235 | 4 | | 4 | 46 | ## | 14.7 | 0.33 | 4.0 | 1.7 | X | Y | vhdl | 21 | cpu68 | Y | yes | N | N | 64K | 64K | Y | | | | | 2003 | 2009 | http://members.optushome.com.au/jekent/ | | |
| altium/TSK51A | http://techdocs.proprietar | | Altium | 8051 | 8 | 8 | spartan-3-5 | Altium | | 1890 | 4 | | 1 | 50 | | | 0.33 | 6.0 | 1.5 | AILX | | proprietary | | | Y | yes | N | N | 64K | 64K | Y | | | | | 2004 | 2017 | CR0140.pdf, CR01 | frozen, asm, C, C++, schem, VHDL & V | default clock speed is 50MHz |
| rtf6809 | https://github.c | alpha | Robert Finch | 6809 | 8 | 8 | kintex-7-3 | James | many | 7506 | 6 | 1 | 2 | 106 | ## | 14.7 | 0.33 | 4.0 | 1.2 | X | | verilog | 4 | rtf6809 | Y | yes | N | N | 4G | 4G | Y | | | 8 | | 2012 | 2015 | http://www.finitr | 6809 with 32-bit "FAR" addressing | probably for simulation? |
| cpu65c02_true | https://opencor | stable | Jens Gutschmidt | 6502 | 8 | 8 | spartan-6-3 | James | latch v | 4794 | 6 | | | 47 | ## | 14.7 | 0.33 | 4.0 | 0.8 | X | | vhdl | 8 | core | | yes | N | N | 64K | 64K | Y | | | | | 2008 | 2021 | | cycle accurate | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| lem4_9ptr | https://opencor | beta | James Brakefield | accum | 4 | 9 | **zu-2e** | James | 1 stage | 210 | 6 | | 0 | 397 | ## | v20.1 | 0.24 | 1.0 | 453.5 | IX | | vhdl | 2 | lem1_9pt | Y | | N | Y | 512 | 2K | N | 24 | | | 1 | 2016 | | binary & BCD digit addition, speed m | 4 index registers: (ix),(--ix),(ix++),(ix+off) | |
| lem4_9ptr | https://opencor | beta | James Brakefield | accum | 4 | 9 | kintex-7-3 | James | 1 stage | 151 | 6 | | 1 | 151 | ## | 14.5 | 0.24 | 1.0 | 240.0 | IX | | vhdl | 2 | lem1_9pt | Y | | N | Y | 512 | 2K | N | 24 | | | 1 | 2016 | | binary & BCD digit addition, speed m | 4 index registers: (ix),(--ix),(ix++),(ix+off) | |
| lem4_9 | https://opencor | beta | James Brakefield | accum | 4 | 9 | kintex-7-3 | James | 1 stage | 144 | 6 | | 1 | 195 | ## | 14.5 | 0.16 | 1.0 | 216.7 | IX | | vhdl | 2 | lem1_9 | Y | | N | Y | 32 | 2K | N | 24 | | | 1 | 2016 | | binary & BCD digit addition, speed mode | | |
| jane_nn | | stable | Suresh Devanathan | RISC | 4 | 8 | kintex-7-3 | James | Brakef | 723 | 6 | | | 178 | ## | 14.7 | 0.33 | 1.0 | 81.4 | X | | vhdl | 3 | Processor | Y | | | | | | | 27 | | 16 | | 2002 | | | neural network microprocessor, specialized registers | |

| _uP_all_soft folder | opencores or prmary link | status | author | style / clone | data size | inst size | FPGA | reporter | comments | LUTs ALUT | LUT? | mults | blk ram | F max | date | tool ver | MIPS /inst | clks/ inst | KIPS /LUT | ven dor | SOC | src code | #src files | top file | doc | tool chai n | fltg pt | Hav'd | max dat | max inst | byte adrs | # inst | adr mod | # reg | pip e len | start year | last revis | secondary web link | note worthy | comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mcs-4 | https://opencor | alpha | Reece Pollack | 4004 | 4 | 4 | kintex-7-3 | James Brakef | | 228 | 6 | | | 376 | ## | 14.7 | 0.16 | 4.0 | 66.0 | X | | verilog | 7 | i4004 | | | N | | 4K | 4K | N | | | | 2012 | 2012 | | 4004 was multi-chip | 4004 CPU & MCS-4 |
| t400 | https://opencor | stable | Arnim Laeuger | COP400 | 4 | 8 | spartan-2 | Arnim Laeuge | | 643 | 3 | | 2 | 60 | | | 0.16 | 4.0 | 3.7 | IX | | vhdl | 36 | t400_core | Y | yes | N | Y | 64 | 1K | Y | | | | 2006 | 2009 | | implementation of National's 4-bit COP400 microcontroller | |
| lem1_9min | https://opencor | stable | James Brakefield | accum | 1 | 9 | kintex-7 | James | 1 stage | 63 | 6 | | 1 | 358 | ## | 14.5 | 0.04 | 1.0 | 227.2 | ILX | | vhdl | 3 | lem1_9mi | Y | asm | N | Y | 64 | 2K | N | 8 | | 64 | 1 | 2003 | 2009 | | logic emulation machine | |
| lem1_9 | https://opencor | alpha | James Brakefield | accum | 1 | 9 | kintex-7-3 | James | 1 stage | 75 | 6 | | 1 | 171 | ## | 14.5 | 0.04 | 1.0 | 91.2 | IX | | vhdl | 2 | lem1_9 | Y | | N | Y | 32 | 2K | N | 24 | | | 1 | 2016 | 2017 | | single bit at a time, absolute adrs | |
| lem1_9ptr | https://opencor | beta | James Brakefield | accum | 1 | 9 | kintex-7-3 | James | 1 stage | 147 | 6 | | 1 | 176 | ## | 14.5 | 0.06 | 1.0 | 72.0 | IX | | vhdl | 2 | lem1_9ptr | Y | | N | Y | 512 | 2K | N | 24 | | | 1 | 2016 | | | use speed opt, logic emulation machi | 4 index registers: (ix),(--ix),(ix++),(ix+off) |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 88 | # usable(beta, st | 0 | 10 | 23 | 16 | blank | | 403 | ## | | 403 | ## | 18 | | 15 | verilog | 182 | non-blank | 294 | 25 | | | | | | | | | | | | | | | | | | | | |
| 39 | "B" or "X" of lim | 0 | | 402 | 403 | a | | | | | | | | | 403 | vhdl | 180 | asm | 57 | Web page DMIPS p | en.wikipedia.org/wiki/Instructions_per | community.freesc | www.eembc.org/coremark/index.php | | | | | | | | | | | | | | | | | |
| **MIPS/MHz Pro-rating for data size:** | | | | | 18 | zu-2e | | | | | | | | | | sys verilo | 12 | forth | 5 | DMIPS per clock for many microprocessors: | | http://en.wikipedia.org/wiki/Instructions_per_second | | | | | | | | | | | | | | | |
| 1-bit | 0.04 | 16-bit | 0.67 | 64-bit | | | 2.00 | | | | | | | | | propriet | 17 | | | | | | | | | | | | | | | | | | | | | | |
| 4-bit | 0.17 | 24-bit | 0.80 | **Silicon Area equivalents** | | | | | | | | | | | | scala | 3 | | | | | | | | | | | | | | | | | | | | | | |
| 8-bit | 0.33 | 32-bit | 1.00 | LUTS/DSP48 | | | 16:1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12-bit | 0.40 | 48-bit | 1.50 | LUTS/Block RAM | | | 32:1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Under the assumption that the core is capable of one instuction per clock

| | |
|---|---|
| 74 | _paper_only |
| 58 | educational |
| 25 | _weak_start |
| 6 | _up_cores |
| 5 | in limbo |
| 11 | planning |
| 44 | simulation |
| 573 | main+sim |
| 529 | net main |
| 650 | total |

| | |
|---|---|
| 259 | VHDL |
| 277 | Verilog |
| 26 | System Verilog |
| 11 | Spinal/Scala |
| 7 | VHDL & Verilog |
| 3 | MyHDL |
| 35 | proprietary |
| 13 | other |
| 3 | Schematic |
| 634 | total |

418 designs with FOM (KIPs/LUT) results (some duplicates due to multiple FPGA runs)
385 designs with best FOM (likely true measure of # of usable designs)

| Column Titles | Details |
|---|---|
| "A" | A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original |
| "B" | used to indicate best KIPS/LUT for a given design, usually using fast FPGA family |
| cat | main, educational, planning, simulation, paper, in limbo or weak |
| _uP_all_soft folder | if opencores design is their folder name, otherwise my folder name |
| opencores or primary link | about 200 designs in open cores, about 100 in github |
| status | ASIC, paper (detailed in), planning (no source), alpha, beta, stable, mature, proprietary, untested; incomplete, educational typically <16 instructions, simulation |
| author | First Name, Last Name or university or corporation |
| style / clone | part number or "forth", RISC, accumulator, etc. "asic" indicates: avail as asic & fpga, an asic netlist source or a hard core within fpga chip |
| data size | data register size in bits |
| inst size | shortest instruction size in bits |
| FPGA | FPGA family for compile, place, route & timing, usually using fastest part grade |
| reporter | First Name, Last Name |
| comments | compile, place, route & timing problems |
| LUTs ALUT | total number of LUTs, ALUTs or tiles used including route-thrus & otherwise unavailable |
| LUT? | 4-LUT, 6-LUT, Altera ALUT, Actel Tile |
| mults | total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up |
| blk RAM | total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up |
| Fmax | maximum primary clock speed from compile, place & route run with best clock constraint, fastest part, best die temp |
| date | date of compile, place & route; serves to identify source version |
| tool ver | Altera (**Q**uartus), Xilinx (ISE, **V**ivado), Lattice Semiconductor(**D**iamond) or MicroSemi(**L**ibero) tool version number |
| MIPS /inst | prorated DMIPS per instruction, reduced for data word sizes under 32-bits, greater than one for multiple issue processors |
| clks/ inst | number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP |
| KIPS /LUT | figure of merit, does not include effects of memory capacity, floating point or instruction set quality |
| Vendor | Libero, Intel(Altera): Quartus; Latticesemi: Diamond & iCEcube, Xilinx: ISE & Vivado |
| Prog File | n, Vn, Zn; A: Mn, Arn, Cn, Stn; M: Tn, Pf, Fn; L: En, Mhn, Sbn, Xpn; n is family generation # |
| SOC | ections or memory access delay), Y: System on a Chip (has peripherals) |
| src code | System Verilog or schematic or gates or Proprietary or Scala etc |
| # src files | r of source files for compile, place, route & timing |
| top file | oute & timing run, multiple versions of same design distinguished here |
| doc | is documentation provided? |
| tool chain | re a compiler or assembler provided or available |
| fltg pt | mpile, place, route & timing run include floating point? |
| Hav'd | a memory(s), 2C: # caches, M: MMU, N: von Neuman (single memory bus) |
| max data | maximum data address |
| max inst | maximum instruction address |
| byte adrs | is byte addressing provided |
| # inst | ictions, conditionals count as one instruction, somewhat subjective |
| # adr modes | ck, indir, indir++, --indir; (indir), (indir++), (--indir), (indexed), abs-short/direct page, scaled |
| # reg | number of registers in register file |
| pipe len | number of pipeline stages |
| start year | year of first design activity |
| last revis | last year for revisions or web page updates |
| secondary web link | secondary web address |
| note worthy | anything special about the design |