Small soft core uP Inventory

Opencore and other soft core processors

Only cores in the "usable" category included

Highest KIPS per LUT or ALUT, adjusted for word size (above 200)						©2023 James Brakefield	
Work in progress: KIPS/LUT only approximate, many of the small designs will move down on the list							
Caution: these are bare cores, Fmax will probably drop with additional LUT count		**wd sz**	**# inst**	**LUT-ALUT**	**KIPS/LUT**	**Fmax**	**style**
cray1	homebrew Cray1	64	128	13463	**57**	127	RISC
fisa64	by Robert Finch	64		10404	**9**	65	RISC
fpgammix	clone of Knuth's MMIX	64	256	11605	**3**	94	RISC
s1_sparc	reduced version of OpenSPARC T1	64		52485	2	56	RISC
riscv_GRVI	Jan Gray's implementation of RISC-V RV32I	32		320	**1172**	375	RISC
microblaze	Xilinx propretary, area optimized, 70 configuration options, fltg-pt & MMU optional	32		563	**1248**	682	RISC
ARM_Cortex_A9	ASIC, LUTs number based on relative area, dual issue, includes fltg-pt & MMU & caches	32		4500	**583**	1050	RISC
nios2	Altera proprietary, speed optimized, fltg-pt, cache & MMU optional	32		895	**390**	310	RISC
microcore110	Forth machine with indexing into return stack, auto inc/dec, variable length imm	32		384	**293**	224	stack
mblite	clone of microblaze, not all instructions implemented	32	86	941	**241**	227	RISC
picorv32	version of RISC-V without mult, div or fltg-pt; advertised numbers much better	32		1276	**206**	316	RISC
hive_core	4 symetrical stacks, eight threads via pipeline barrel	32		1420	**199**	283	stack
rois24_24min	RISC with 24-bit inst, 64 registers	24	30	492	**313**	185	RISC
leros	Leros: A Tiny Microcontroller for FPGAs	16		112	**1089**	182	accum
Lutiac	Lutiac – Small Soft Processors for Small Programs (academic paper only)	16		140	**948**	198	register
iDEA	The iDEA DSP Block Based Soft Processor for FPGAs	16		321	**845**	405	RISC
octavo	Octavo: an FPGA-Centric Processor Family, eight thread barrel pipeline	16		500	**737**	550	register
p16b	16-bit forth machine, 5-bit inst	16		367	**648**	355	forth
xr16	Jan Gray's handcrafted uP auto placed & routed into Kintex-7	16		273	**645**	263	RISC
J1a	16-bit forth machine with 16-bit inst, 38% code size of microblaze	16		518	**636**	412	forth
msl16	16-bit forth machine, 4-bit inst	16		303	**566**	256	forth
micro16b	minimal	16		205	**349**	434	accum
alwcpu	small simple 16-bit RISC	16		377	**345**	194	RISC
atlas_core	ARM thumb like inst set, also MMU version	16		559	**286**	200	RISC
raptor16	16-bit CISC, 8 data & 8 adr registers	16		590	**280**	319	CISC
yafc	16-bit forth	16		617	**268**	247	forth
diogenes	student RISC system	16		807	**246**	297	RISC
sayeh_processor	simple educational RISC	16		479	**230**	164	RISC
usimplez	8 instructions, part of university course	12		48	476	134	accum
eric5	entner-electronics.com proprietary	9		110	229	60	forth
ssbcc	Python generated Verilog stack machine, 9-bit inst, memories have adj size	8		196	**798**	474	forth
avr8	not a full AVR clone, doc is opencores page	8		174	**792**	418	AVR
mcpu	fits into 32 macrocell CPLD, only 8 inst	8		41	**749**	384	accum
myrisc1	RISC with 8-bit instructions	8		121	**629**	231	RISC
lwrisc	ClaiRISC	8		88	**444**	230	accum
popcorn	small 8 bit uP	8		267	**428**	347	accum
nocpu	small 8 bit uP	8		175	**306**	243	RISC
cosmac	clone of CDP1802	8		239	**285**	206	accum
8bit_chapman	small stack processor	8		176	**245**	131	stack
gumnut	from in Peter Ashenden's Digital Design book, both VHDL & Verilog source	8		388	**221**	259	RISC
p16c5x	PIC16 clone	8		378	**220**	252	PIC16
dfp	8-bitter, generates a custom VHDL stack machine, compiler is in Forth	8		297	**213**	192	forth
lem4_9ptr	binary and BCD supported, four pointers with (x), (--x), (x++) & (x+off)	4	25	151	**240**	151	accum
lem1_9min	logic emulation machine, single stage pipe	1	11	63	227	358	accum