_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	toolchain	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
Small soft core uP Inventory			**©2025 James Brakefield**																																				
Opencore and other soft core processors																																							
totalcpu	https://opencor	alpha		RISC	12+	12	kintex-7-3	James Brakef		229		6	1		149	##	14.7	0.33	3.0	71.7	X		verilog	10	cpu			N						16		2007	2009		data width 12 bits and up, no data memory	
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	stratix-5	Dmytro Senya		32978		A	72	112	192	##	q17.1	4.00	1.0	23.3	A		system	27	CoreOneV	Y	asm	Y		4G	4G			16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	cyclone-5	James	reduce	35984		A	72	112	103	##	q18.0	4.00	1.0	11.4	A		system	27	CoreOneV	Y	asm	Y		4G	4G			16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	cyclone-5	James	slow t	50135		A	72	112	90	##	q18.0	4.00	1.0	7.2	A		system	27	CoreOneV	Y	asm	Y		4G	4G			16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	stratix-5	Dmytro Senya		50814		A	72	112	180	##	q17.1	4.00	1.0	14.1	A		system	27	CoreOneV	Y	asm	Y		4G	4G			16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	cyclone-5	James	too big	130160		A	##	462		##	q18.0	4.00	0.3		A		system	27	CoreQuad	Y	asm	Y		4G	4G			16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
odess	https://opencor	stable	Dmytro Senyakin	RISC	##	16	stratix-5	Dmytro Senya		148078		A	72	122	184	##	q17.1	4.00	0.3	19.9	A		system	27	CoreQuad	Y	asm	Y		4G	4G			16		2017	2017	https://opencores	Altera proj, Multicore, P&R results at	37-bit adr, quad issue, caches, 32-64-128 fltg-p
theia_gpu	https://opencor	beta	Diego Valverde	RISC	96	64	kintex-7-3	James	huge a	934049		6				##	14.7	0.40	1.0		GPU		verilog	32	theia											2009	2012		Ray Cast Programable graphic Proces	four cores, huge LUT count, 2/3rds LUT RAM
legv8	https://github.c	stable	Warren Seto	AA64	64	32	kintex-7-3	James Brakef		723	280	6		2	156	##	14.7	1.00	1.0	215.1	X	B	verilog	2	arm_cpu	Y	yes	N		4G	4G	Y	9		32		2018	2019		coursework, limited ISA, 3 versions	pipelined, inst: LDUR, STUR, ADD, SUB, ORR, A
legv8	https://github.c	stable	Warren Seto	AA64	64	32	kintex-7-3	James Brakef		884		6		2	137	##	14.7	1.00	1.0	155.0	X	B	verilog	2	arm_cpu	Y	yes	N		4G	4G	Y	9		32		2018	2019		coursework, limited ISA, 3 versions	inst: LDUR, STUR, ADD, SUB, ORR, AND, CBZ, B
legv8	https://github.com/mattc		Matthew Olsson	AA64	64	32	kintex-7-3	James Brakef		884		6		2	137	##	14.7	1.00	1.0	155.0			verilog			Y	yes	N		4G	4G	Y	9		32		2018	2019		another implementation	legv8 from Patterson & Hennessy 2017
risc63	https://github.com/domir		Dominik Salvet	RISC	64	16	kintex-7-3	James Brakef		2103	1080	6			240	##	14.7	2.00	1.0	227.8	X		vhdl	16	risc63	Y		N		256K	256K	Y	39		16		2020	2024		tightly packed 16-bit ISA, no mult, no	BS thesis in Chech
kcp53000	https://github.com/sam-f		Samuel Falvo II	risc-v	64	32	kintex-7-3	James	trimm	2455		6			175	##	14.7	2.00	1.0	142.9	X	B	verilog	4	polaris	Y	yes	N	Y	16E	16E	Y			32		2016	2017	https://github.cor	kestrel #3, basic 64-bit RISC-V	uses state machine RTL generator
fisc	https://github.c	stable	Miguel Santos	RISC	64	32	cyclone-4	James Brakef		5036		4		21	66	##	q18.0	2.00	1.0	26.1	A		system	13	fisc_core	Y	yes	Y	N			Y	85	6	32	5	2018	2018	http://www.archf	Flexible Instruction Set Computer	caches, VHDL & System Verilog versions, altera
ARM_Cortex_A	https://develope	ASIC	ARM	ARM A53	64	32	asic	Xilinx		6000		A			1500			2.00	0.5	1000			asic			Y	yes	Y				Y						https://en.wikipe	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
mecrisp-ice	https://sourceforge.net/p		Matthias Koch	forth	64	16	spartan7	James Brakef		6372	8860	6	16	16	63	##	v23.2	2.00	2.0	9.8	LX	Y	verilog	48	j1a	Y	forth	N		16E	16E	Y					2011	2023		64-bit data size, some comments in G	distinct j1a.v for each data size
fisa64	https://github.c	beta	Robert Finch	RISC	64	32	kintex-7-3	James Brakef		10404		6	12	7	65	##	14.7	1.50	1.0	9.4	X		verilog	1	FISA64	Y		N	Y								2015	2015	https://github.com/robfinch/Cores	need to use multi-cycle on mult	
cray1	www.chrisfento	alpha	Christopher Fenton	CRAY1	64	16	**zu-3e**	James	undefi	11510		6	15	1		##	v21.1	6.00	1.0		X		verilog	46	cray_sys_	Y	yes	Y	N	4M	4M	N	128		536		2010	2015	CRAY data sheets	homebrew Cray1	24-bit address registers
cray1	www.chrisfento	alpha	Christopher Fenton	CRAY1	64	16	spartan7	James	undefi	11554	8305	6	15	1		##	v24.1	6.00	1.0		X		verilog	46	cray_sys_	Y	yes	Y	N	4M	4M	N	128		536		2010	2015	CRAY data sheets	homebrew Cray1	24-bit address registers
fpgammix	https://github.c	stable	Tommy Thorn	MMIX	64	32	arria-2	James Brakef		11605		A	8	10	94	##	q13.1	1.50	4.0	3.0	A		system	3	core	Y	yes	Y	Y	16Q	16Q	Y	256		288		2006	2014	https://en.wikipe	clone of Knuth's MMIX	micro-coded
cray1	www.chrisfento	alpha	Christopher Fenton	CRAY1	64	16	kintex-7-3	James Brakef		13463	7358	6	19	10	127	##	14.7	6.00	1.0	56.6	X		verilog	46	cray_sys_	Y	yes	Y	N	4M	4M	N	128		536		2010	2015	https://www.chris	homebrew Cray1	24-bit address registers
forwardcom	https://github.c	stable	Agner Fog	cisc	64	32	atrix-7	Agner Fog		21121	7392	6			56	##	v20.1	2.00	1.0	5.3	X		system	18	top	Y	asm	Y		64K	32K	Y			64		2016	2023	https://www.forw	x86 like, complete ISA, MMX & vector	x86 adr modes, vector inst use width of vect re
btsr1arch	https://github.c	alpha	Brendan Bohannon	CISC	64	16	artix-7	James Brakef		29964	15823	6	26	108	58	##	v24.2	1.00	2.0	1.0	X		verilog	149	topunit	Y	yes	Y	N	256T	256T	Y	64		32		2018	2024	https://www.yout	64-bit regs, 16x inst, 48-bit VM	BJX2 is superset of BtSR1, 4 data sizes
s1_core	https://opencor	stable	Fabrizio Fazzino etal	SPARC	64	32	kintex-7-3	James Brakef		52845		6	8	59	56	##	v14.1	2.00	1.0	2.1	AX		verilog	136	s1_top	Y	yes	Y	N	4G	4G	Y			32		2007	2012	https://en.wikipe	reduced version of OpenSPARC T1	Vivado run
btsr1arch	https://github.c	alpha	Brendan Bohannon	CISC	64	16	artix-7	James Brakef		55967	23767	6	52	112	75	##	v23.2	1.00	2.0	0.7	X		verilog	149	topunit	Y	yes	Y	N	256T	256T	Y	64		32		2018	2024	https://www.yout	64-bit regs, 16x inst, 48-bit VM	BJX2 is superset of BtSR1, 4 data sizes
riscv_percival	https://github.com/artecs		ArTeCS (Un Madrid)	risc-v	64	32	kintex7	ArTeCS	larges	57129	27996	6			50		v20.2	1.00	2.0	0.4	X		system	~60		Y	yes	N		16E	16E	Y			32		2017	2022	https://github.cor	Open-Source Posit RISC-V Core with	Quire Capability, cav6(AKA Ariane) derivative
thor	https://opencor	mature	Robert Finch	RISC	64	32		Robert Finch		210000					306								verilog		thor2	Y	asm	Y		4G	4G	Y			64		2015	2023	https://github.cor	Thor-2: L1 & L2 caches, GP float & vec	96-bit registers
thor	https://opencor	mature	Robert Finch	RISC	64	16		Robert Finch		210000					306								verilog		thor5	Y	asm	Y		4G	4G	Y			64		2015	2023	https://github.cor	Thor-5: L1 & L2 caches, GP float & vec	plans for more features, eventually 2M LUTs
qupls	https://github.c	WIP	Robert Finch	risc	64	40		Robert Finch		160K											X		system	98	qupls	Y	asm	Y							64		2023	2024	http://www.finitr	Qupls (Q+): 2024 version of the Thor	variety of three operand & u-coded instruction
classic_HP_calc	https://github.c	stable	Brian Nemetz	accum	56	10	kintex-7-3	James Brakef		1750		6		3	233	##	14.7	0.17	10.0	2.2	X		vhdl	15	classichp	Y		N		30	4K	N	40		7		2012			processor & ROMs for HP-55, 45 & 35	includes LED display driver & UART, for Papilio
ks10	http://www.tec	alpha	Rob Doyle	PDP10	36	36	spartan-6	Rob Doyle		4427		6		15	50	##	14.7	1.00	2.0	5.6	X		verilog	39	esm_ks10	Y	yes	Y	N			N					2011	2014		36-bit accum & 18-bit adrs	ucf file, most tests pass
a_tiny_up	https://www.quora.com/		Simon Moore, Frankie	RISC	32	32	arria-5	James	tiny LL	35		A				##	q18.0	0.67	1.0				system	1	TinyComp	Y	asm	N	Y	1K	1K	N	13		128		2007	2011	https://www.cl.ca	from Thacker's version, Un Cambridge course	
riscv_serv	https://github.com/olofk/		Olof Kindgren	risc-v	32	32	vu37p	Olof Kindgren		125	164	6		0.5	125	##		1.00	32.0	31.3	X		verilog	63	serv_top	Y	yes	N		4G	4G	Y	45		32		2018	2023	https://riscv.org/2	6K cores in vu37p, reg-file in blk-RAM	https://github.com/olofk/corescore
riscv_serv	https://github.com/olofk/		Olof Kindgren	risc-v	32	32	ice40	Olof Kindgren		198	164	4			32	##		1.00	32.0	5.1	L		verilog	63	serv_top	Y	yes	N		4G	4G	Y	45		32		2018	2023	https://riscv.org/2	RISC-V contest prize, 1-bit ALU	https://github.com/olofk/corescore
supersmall	http://www.eec	stable	Michael Ritchie	RISC	32	32	artix_3	Michael Ritch		207		A		2+8	126	##	q9.0	1.00	16.0	38.1	A		verilog														2005	2009		2-bit serial, Mostly MIPS-I compliant	Copyright 2005,2006,2009 Jonathan Rose, and
riscv_serv	https://github.com/olofk/		Olof Kindgren	risc-v	32	32	cyclone10	Olof Kindgren		239	164	4		0.5	80	##		1.00	32.0	10.5	A		verilog	63	serv_top	Y	yes	N		4G	4G	Y	45		32		2018	2023	https://riscv.org/2	**smallest risc-v core, many boards**	https://github.com/olofk/corescore
mb-lite_plus	http://www.late	stable	Huib Arriens	uBlaze	32	32	kintex-7-3	James Brakef		244		6		2	319	##	14.7	1.00	1.0	1308	X	B	vhdl	34	tumbl	Y	yes	N		4G	4G	Y			32		2010	2012		Delft Un. Of Tech. course work	use inferred RAM
riscv_engine-v	https://github.com/micro		Antti Lukats	risc-v	32	32				306		4						1.00	6.7		AL		verilog	11		Y	yes	N		4G	4G	Y	45		32		2018	2018	https://riscv.org/2	RISC-V contest 2nd place, 8-bit ALU	no source for xilinx, no implementation docs
riscv_GRVI-pha	http://fpga.org/	beta	Jan Gray	risc-v	32	32	virtex-u-2	Jan Gray		320		6		1	375	##	v16.4	1.00	1.0	1172	X		proprietary			Y	yes	N		4G	4G	Y	45		32	3	2015	2018	https://www.yout	hand fitted & placed	"Hoplite" router, 1680 cores in XCVU9P
tarhi	https://github.c	alpha	Dagvadorj Galbadrakh	RISC	32	32	kintex-7-3	James	everyt	396		6		1	123	##	14.7	1.00	4.0	77.9	X		verilog	4	tarhi_controller			N		16M	16M	N	11		4		2013	2013		no doc, extremely small RISC	difficulty with timing, try 7.0ns
nios-v	https://www.intel.com/co		Intel	riscv	32	32	Agilex 7	Altera	compa	421		A			442	##	q24.2	1.00	1.0	1050	A		proprietary			Y	yes	opt		4G	4G	Y			32		2021	2024	https://www.intel	requires Quartus Prime Pro? Ashling	ALM mystery: off by 2X? No FF counts
riscv_minimax	https://github.com/gsmec		Graeme Smecher	risc-v	32	16	KU060	Graeme Sme		423	61	6			200	##	v22.2	1.00	4.0	118.2	X		verilog	2	minimax	Y	yes	N		4G	4G	Y			32		2022	2023		LUT count comparisons with other ris	most 32-bit insts microcoded, limited 16-bit IS
cpugen	https://opencor	stable	Giovanni Ferrante	RISC	32	16	kintex-7-3	James Brakef		474		6			192	##	14.7	0.67	1.0	271.8	AX		vhdl	14	cpu	Y	asm	N	N								2003	2009		x86 .exe generates VHDL RISC uP	using 16 bit example
riscv_vexriscv	https://github.c	beta	Charles Papon	risc-v	32	32	artix-7	Charles Papo		481		6			346			0.52	1.0	374.1	X		scala		smallest	Y	yes			4M	4M	Y					2023	https://riscv.org/2	preformance #s for 8 configurations c	"Briey" is SOC variant
riscv_rudolv	https://github.com/bobbl		Jörg Mische	risc-v	32	32	kintex-7-3	Jörg Mische		545		6			200	##		1.00	1.0	367.0	ALMX		verilog	4	pipeline	Y	yes	N		4G	4G	Y			32	5		2021		RISC-V processor for real-time system	34 clock mult & divide
microblaze	https://www.xil	proprietar	Xilinx	uBlaze	32	32	kintex-7	Xilinx		546		6		1	320			1.03	1.0	603.7	X		proprietary			Y	yes	opt	Y	4G	4G	Y	86		32	3	2002			MicroBlaze MCS, smallest configurati	70 configuration options, MMU optional
microblaze	https://www.xil	proprietar	Xilinx	uBlaze	32	32	virtex ultr	Xilinx		563		6		1	682	##		1.03	1.0	1248	X		proprietary			Y	yes	opt	Y	4G	4G	Y	86		32	3	2002		https://en.wikipe	MicroBlaze MCS, smallest configurati	70 configuration options, MMU optional
mecrisp-quintu	https://sourceforge.net/p		Matthias Koch	riscv	32	32	spartan7	James	added	572	89	6		1	100	##	v23.2	1.00	1.0	174.8	LX		verilog	24	FemtoRV32		N		N	4G	4G	Y			32		2011	2023		based on femtorv32, some comment	uls3s.v adds memory to femtorv32
nios2		proprietar	Altera	Nios II	32	32	stratix-5	Altera	consis	584		A			420	##	q16.0	1.00	1.0	719.2	A		proprietary			Y	yes	opt		4G	4G	Y			32		2004			fltg-pt, caches & MMU options	Nios II/e: min LUTs version, DMIPS adj, 1.68 Co
mips-cpu	https://github.c	alpha	Jeremiah Mahler	MIPS	32	32	kintex-7-3	James	added	596		6		1	244	##	14.7	1.00	1.0	409.2	X		verilog	15	cpu	Y	yes	N		4G	4G	Y			32	5	2017	2017		Very early stage project, only implem	no outputs, missing im_data.txt
softpc	https://github.com/alread		Michael S	Nios II	32	32	cyclone-1	Micha	block t	613		4		1	180		q17.1	1.00	5.0	58.9			vhdl	13	nios2ee	Y	yes	opt		4G	4G	Y			32			2019		nine variations in attempt to improve	16-bit ALU
amic-0	https://github.c	stable	Alberto Moriconi	stack	32	8	**zu-3e**	James	vivado	622	357	6			250	##	v21.1	1.00	6.0	67.0	X		vhdl	12	processor	Y		N		4G	4G	Y					2010	2021	https://en.wikipe	based on mic-1 by Andrew Tanenbau	36-bit uCode, usually Java virtual machine
opc.opc7cpu	https://github.c	stable	revaldinho	RISC	32	16	kintex-7-3	James Brakef		624		6			303	##	14.7	1.00	2.0	242.8	X		verilog	2	opc7cpu	Y	asm	N	N	1M	1M	N	32	5	16		2017	2021	https://revaldinho	OPC7 32bit, based on OPC5LS, more i	see hackaday One Page Computing Challenge
lxp32	https://opencor	beta	Alex Kuznetsov	RISC	32	32	**zu-3e**	James Brakef		743	844	6	3	1.5	278	##	v24.1	1.00	2.0	186.9	AIX		vhdl	20	lxp32u_to	Y	asm	N	N	4G	4G	Y	30		256	3	2016	2022	https://lxp32.gith	register file in block RAM	vendor neutral source code
riscv_picorv32	https://github.c	beta	Clifford Wolf	risc-v	32	32	xcku3p-3	Cliffor	small	761	442	6			769	##	v16.2	1.00	3.0	336.8	X		verilog	1	picorv32	Y	yes	N		4G	4G	Y			32		2016	2022	https://github.cor	mimimal features, soc options	designed for minimum LUTs
riscv_picorv32	https://github.c	beta	Clifford Wolf	risc-v	32	32	kintex-U-1	Cliffor	small	761	442	6			454	##	v16.2	1.00	3.0	198.9	X		verilog	1	picorv32	Y	yes	N		4G	4G	Y			32		2016	2022		mimimal features, soc options	LUTs & Fmax for Kintex, Virtex & Ultrascale+
xthundercore	http://forum.ga	alpha	majordomo	RISC	32	16	kintex-7-3	James Brakef		793		6		2	193	##	14.7	1.00	1.0	243.7	X		vhdl	49	xtc	on	yes	N	Y	4G	4G				16	5	2014		http://www.xthur	Gadget Factory Forum thread	in debug, no comments, mostly in simulation
lxp32	https://opencor	beta	Alex Kuznetsov	RISC	32	32	kintex-7-3	James Brakef		850	526	6	3	1	196	##	14.7	1.00	2.0	115.4	AIX		vhdl	20	lxp32u_to	Y	asm	N	N	4G	4G	Y	30		256	3	2016	2022	https://lxp32.gith	register file in block RAM	vendor neutral source code
tiny64	https://opencor	stable	Ulrich Riedel	RISC	32	32	kintex-7-3	James Brakef		874		6			189	##	14.7	1.00	2.0	107.9	X		vhdl	6	tinyx					64K	64K		14		8		2004	2007		data size from 32 to 64 bits	micro-coded sub-ops
coen_316_cpu	https://github.c	alpha	G.K Yvann Monny	RISC	32	32	kintex-7-3	James	does r	897		6			127	##	14.7	1.00	3.0	47.0	X		vhdl	8	cpu_dp			N		32	32	N	20		32		2018	2018		MIPS based, simulation DO files, I&D	very small caches do not infer any RAM
J1a32	www.excamera	stable	James Bowman	forth	32	16	kintex-7-3	James	DFF ex	930		6			358	##	14.7	1.00	1.0	384.4	X		verilog	3	j1	Y	forth	N		64K	64K		20			2	2006	2023	**https://pythonli**	uCode inst, dual port block RAM	DFF used for 18 deep data & return stacks
mblite	https://opencor	beta	Tamar Kranenburg	uBlaze	32	32	kintex-7-3	James Brakef		941		6		2	227	##	14.7	1.00	1.0	240.9	AX		vhdl	18	core_wb	Y	yes	N		4G	4G	Y	86		32		2009	2017		not all instructions implemented	moved everything to work library
simplecpucore	https://github.com/Karan		Karang	arm	32	32	kintex-7-3	James	bare c	946	309	6			100	##	v24.1	1.00	1.0	105.7	AX		vhdl	11	arm_core	Y	yes	N		4G	4G	Y			16	5		2017		CPU core for ARMv3, educational	no RTL comments, shows ASIC layout
lxp32	https://opencor	beta	Alex Kuznetsov	RISC	32	32	**zu-3e**	James Brakef		948	844	6	4	1.5	250	##	v21.1	1.00	2.0	131.9	AIX		vhdl	20	lxp32u_to	Y	asm	N	N	4G	4G	Y	30		256	3	2016	2022	https://lxp32.gith	register file in block RAM	vendor neutral source code
riscv_wildcat	https://github.com/schoe		Martin Schoeberl	risc-v	32	32	artix7	Martin Schoe		993	442	6			111			1.00	1.0	112.0	X		scala	32	singlecycl	Y	yes	N		4G	4G	Y			32	4		2025	https://arxiv.org/p	comparison of 3, 4 & 5 stage pipeline	book: Digital Design with Chisel
aeMB	https://opencor	beta	Shawn Tan	uBlaze	32	32	**zu-3e**	James Brakef		997	434	6	3		250	##	v21.1	1.00	1.0	250.8	ALX		verilog	7	aeMB_cor	Y	yes	N		4G	4G	Y					2004	2009		not 100% compatable	
riscv_dark	https://github.c	beta	Marcelo Samsoniuk	risc-v	32	32	kintex-7-3	Marcelo Sam		1000		6			220	##	v20.1	1.00	1.0	220.0	XL		verilog	4	darkriscv	Y	yes	N		4G	4G	Y	45		32	2	2018	2024	https://opencores	written in one night, low line count	ku040 overclock 400MHz, builds for 18 fpga bo
zpuflex	https://github.c	mature	Alastair M. Robinson	forth	32	8	cyclone-3	Alasta	approx	1000		4											vhdl	4	zpu_core	Y	yes	N		4G	4G	Y	37				2014	2015	https://github.cor	addditional instrucitons	
aeMB	https://opencor	beta	Shawn Tan	uBlaze	32	32	kintex-7-3	James Brakef		1018	354	6	3		131	##	14.7	1.00	1.0	128.5	ALX		verilog	7	aeMB_cor	Y	yes	N		4G	4G	Y					2004	2009		not 100% compatable	
tridora-cpu	https://gitlab.com/sleder		Sebastian Lederer	stack	32	16	artix-7	James	incom	1019	362				100	##	v24.2	1.00	4.0	24.5	X	Y	verilog	20	top	Y	yes	N		4G	4G							2024	https://hackaday.	32-bit stack machine, Wirth pascal	3-bit to 16-bit instructions, some with enables
nios2		proprietar	Altera	Nios II	32	32	stratix-3	Altera	consis	1020		A			290	##	q13.1	0.90	1.0	255.9	A		proprietary			Y	yes	opt		4G	4G	Y			32		2004			fltg-pt, caches & MMU options	Nios II/f: fastest version, DMIPS adj, 2.15 Core
f32c	https://github.c	beta	marko zec, vordah, Da	risc-v	32	32	atrix-7-3	zec & vordah		1048		6	4	33	185	##	14.7	1.00	1.0	176.5	X		vhdl	50		Y	yes	N	Y	4G	4G	Y	30		32	5	2014	2019	http://www.nxlab	MIPS or RISC-V ISA, Arduino support	https://www.youtube.com/watch?v=55MzMH
sweet32	https://opencor	alpha	Valentin Angelovski	MIPS	32	16	kintex-7-3	James Brakef		1050		6	1		142	##	14.7	1.00	1.0	135.1	X	B	vhdl	2	Sweet32_	Y	yes	N	N	4G	4G	Y	26		16		2014	2015		targets MACHXO2, no RAM	
riscv_fwrisc	https://github.com/mball		Matthew Balance	risc-v	32	32	igloo2	Matthew Bala		1060		4			20	##		1.00	6.7	2.8	AL		system	8	fwrisc_fpg	Y	yes	N		4G	4G	Y	45		32		2018	2018	https://opencores	featherweight entry 2018 RISC-V con	0.15 DMIPS/MHz
armv2a_vlsi	https://github.com/syatl/		Samy Attal	arm	32	32	**spartan7**	James	multic	1069	778	6			86	##	v23.2	1.00	1.5	53.8	X		vhdl	21	arm_core	Y	yes	N	Y	4G	4G	Y			27	3		2022		ASIC project, has vcc & vss connectio	original ARM/Acorn, external caches
zpu	https://github.c	stable	Oyvind Harboe	forth	32	8	kintex-7-3	James Brakef		1073		6	3		283	##	14.7	1.00	4.0	65.9	X		vhdl	23	zpu_core	Y	yes	N		4G	4G	Y	37				2008	2009		zpu4: 16 & 32 bit versions, code size i	ZPU the worlds smallest 32 bit CPU with GCC t
an-noc-mpsoc	https://opencor	mature	Alireza Monemi	uBlaze	32	32	**zu-3e**	James	vivado	1079		6	3	1	333	##	v21.1	1.00	1.0	308.9	X	Y	verilog	90	aeMB_top	Y	yes	N		4G	4G	Y					2014	2023		choice of lm32, aeMB, mor1kx or or1	full system has network of cores
riscv_orca	https://github.c	beta	VectorBlox	risc-v	32	32	stratix-5	vectorblox		1082		A		?	244	##	14.7	0.98	1.0	221.0	A		vhdl	13	orca	Y	yes	N		4G	4G	Y			32		2016			*, /, fltg-pt all optional	RV32IM
mips_linder	https://www.sc	paper	Michael Linder	MIPS	32	32	kintex-7-3	James Brakef		1100		6			238	##	14.7	1.00	1.0	216.5		B	vhdl	39	a_mips	Y	yes	N		4G	4G				32		2007	2007		masters thesis	no LUT RAM, source code in PDF
multi-cycle-cpu	https://github.com/Amrik		Amrik Sadhra	RISC	32	32	spartan6	James Brakef		1134	655	6			83	##	14.7	1.00	1.0	73.0	X		vhdl	48	top_level	Y				4G	4G	Y	21		32		2016	2016	https://www.yout	nicely documented with state diagrar	spreadsheet for test programs, ISE project

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	toolchai n	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
ep32	http://forth.org/	mature	C.H. Ting	forth	32	5	spartan7	James Brakef		1147	2309	6			100	##	v23.2	1.00	1.0	87.2	X		vhdl	7	ep32	Y	forth	N		4G	4G		29				2012		has eForth binary & source	now free
an-noc-mpsoc	https://opencor	mature	Alireza Monemi	uBlaze	32	32	kintex-7-3	James Brakef		1164		6	3	1	192	##	i14.7	1.00	1.0	165.2	X	Y	verilog	90	aeMB	Y	yes	N		4G	4G	Y				2014	2023		choice of lm32, aeMB, mor1kx or or1	full system has network of cores
maxicore32	https://github.c	WIP	Lawrence Manning	risc	32	32	spartan7	James Brakef		1165	209	6	2		83	##	v23.2	0.50	1.0	35.8	LX		verilog	42	maxicore32	asm	N		4G	4G		12		16	2		2024		standard risc	minimal ISA
sweet32	https://opencor	alpha	Valentin Angelovski	MIPS	32	16	kintex-7-3	James Brakef		1177		6	1		116	##	14.7	1.00	1.0	98.8	X	B	vhdl	2	Sweet32_	Y	yes	N	N	4G	4G	Y	26		16		2014	2015		targets MACHXO2, no RAM	
risc0	https://sourcefo	beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakef		1186		6	4	6	110	##	14.7	0.67	1.0	61.9	X		verilog	8	RISC0	Y	yes	N		4G	4G						2011	2018	https://people.inf	minimalist Wirth, education tool	Lola: https://people.inf.ethz.ch/wirth/Lola/ind
openfire2	https://opencor	beta	Antonio Anton	uBlaze	32	32	kintex-7-3	James Brakef		1201		6	3	2	105	##	14.7	1.00	1.0	87.4	X	Y	verilog	27	openfire_	Y	yes	N	N	4G	4G	Y			32		2007	2012		"FPGA Proven"	derived from Stephen Craven's OpenFire
riscv_neorv32	https://github.c	stable	Stephan Nolting	risc-v	32	32	cyclone-IV	Stephe	rtl fpg	1223	607	4			130	##	q19.1	1.00	2.0	53.1	ALX	Y	vhdl	25	neorv32_t	Y	yes	N		4G	4G	Y			32	2	2020	2024	https://opencores	**very well documented, customiza**	minimal configuration, minimal riscv
core_arm	https://opencor	beta	Konrad Eisele	ARM	32	16	kintex-7-3	James Brakef		1239		6		3	250	##	14.7	1.00	1.0	201.8	X	Y	vhdl	151	arm_proc	Y	yes	N		256M	256M				16		2004	2009	http://cfw.source	very large project with many unused	missing files found in sourceforge dir, very litt
eight32	https://github.com/robin:		Alastair M. Robinson	accum	32	8	cyclone-4	Alasta	approx	1300		4			133			1.00	1.0	102.3			vhdl	17	eightthirty	Y	yes	N		500M	500M	Y	28		8		2019	2023	https://retroramb	full tool set, see github page for ISA descriptior	
jam	https://github.c	stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James Brakef		1369		6			143	##	14.7	1.00	1.0	104.2	X		vhdl	17	cpu	Y		N	Y	128K	128K				32	5	2002	2014		serial multiply & divide	
riscv_niosv	https://www.int	proprietar	Intel	risc-v	32	32	arria-10	intel	fastest	1375		A		2	306	##	q21.3	1.00	1.0	222.3	A		proprietary			Y	yes	N		4G	4G	Y			32	5		2021		free license, small inst & data mem	RV32IA spec, M20K for reg file, interrupts
jam	https://github.c	stable	Johan Thelin etal	RISC	32	32	kintex-7-3	James Brakef		1396		6			159	##	14.7	1.00	1.0	113.7	X		vhdl	17	cpu_sys	Y		N	Y	128K	128K				32	5	2002	2014		serial multiply & divide	took out clock divider
riscv_vexriscv	https://github.c	scala	Charles Papon	risc-v	32	32	artix-7-3	Charles Papo		1399		6			295			1.00	1.0	210.9	X	Y	scala		full no cac	Y	yes	N		4G	4G	Y			32			2023		preformance #s for 8 configurations c	"Briey" is SOC variant
microblaze-v	https://www.adiuvoengin		adiuvo	riscv	32	32	spartan7	adiuvo	MCS v	1402	1046	6		4		##	v24.1	1.00	1.0		X					Y	yes	opt	Y	4G	4G	Y	86		32		2023	2024	https://docs.amd.	using their Embedded Sys Dev Board	tightly configured, fixed peripherals
hive	https://opencor	stable	Eric Wallin	stack	32	16	arria-2	James Brakef		1420		A	8	24	283	##	q13.1	1.00	1.0	199.4	ALX		verilog		hive_core	Y		N				N	40		10	8	2013	2015		4 symetrical stacks, eight threads via	pipeline barrel
riscv_dark	https://github.c	alpha	Marcelo Samsoniuk	risc-v	32	32	kintex-7-3	James Brakef		1422		6		1	167	##	14.7	1.00	1.0	117.2	XL		verilog	2	darksocv	Y	yes	N		4G	4G	Y	45		32	2	2018	2024	https://blog.hacks	written in one night, low line count	readme is descriptive, uses cache
kgp-risc	https://github.com/kranti		Kiran & Aluru	MIPS	32	32	spartan7	James	sparta	1428	1572	6				##	v23.2	0.33	1.0		X		verilog	25	topmodul	Y		N		4G	4G						2018	2020		only two register fields + shift amoun	need to use inferred block RAM
mips789	https://opencor	stable	Li Wei	MIPS	32	32	kintex-7-3	James Brakef		1432		6		1	171	##	14.7	1.00	1.0	119.1	AX		verilog	10	mips_core	Y	yes	N		4G	4G	Y			32	5	2007	2014		supports most MIPSI instructions	
bst-cpu	https://github.c	stable	Yichun Ma	RISC	32	32	arria-2	James Brakef		1439		A		2	58	##	q18.0	1.00	1.0	40.2	A		verilog	26	sc_computer			N		4G	4G				32		2016	2016		learning, single cycle uP	
risc-processor	https://github.c	stable	Jeff Bush	RISC	32	32	kintex-7-3	James Brakef		1445		6		6	161	##	14.7	1.00	1.0	111.6	X		verilog	22	fpga_top	Y	yes	N		4G	4G	Y	21		32		2008	2019	https://github.cor	two designs with same name	MIT course work
hf-risc	https://opencor	stable	Sergio Johann Filho	MIPS	32	32	kintex-7-3	James Brakef		1446		6		4	115	##	14.7	1.00	1.0	79.2	X		vhdl	9	spartan3e_n	yes		N	N	4G	4G	Y	41		32		2016		https://github.cor	MIPS I subset, no multiplier	
riscv_lattice	https://www.lat	stable	Lattice Semi	risc-v	32	32	machXO3	Lattice Semic		1507		4		4	60	##		1.00	1.0	39.8	L	Y	verilog			Y	yes	N		4G	4G	Y			32	5		2021		RV32I ISA, 5 stage pipeline, configured	& generated using Lattice Propel
riscv_niosv	https://www.int	proprietar	Intel	risc-v	32	32	agilex	intel	fastest	1509		A		2	566	##	q21.3	1.00	1.0	375.2	A		proprietary			Y	yes	N		4G	4G	Y			32	5		2021		free license, small inst & data mem	RV32IA spec, M20K for reg file, interrupts
ion	https://opencor	mature	Jose Ruiz	MIPS	32	32	kintex-7-3	James Brakef		1533		6			163	##	14.7	1.00	1.0	106.0	AX		vhdl	12	mips_soc	Y	yes	N		4G	4G	Y			32		2011	2018	https://github.cor	new version: moving to MIPS32r1	new version not ready, keeping old numbers
riscv_taiga	https://gitlab.co	stable	Eric Matthews	risc-v	32	32	zynq			1551				1	123			1.00	1.0	79.3	AX		system	46		Y	yes	N		4G	4G	Y			32		2017	2022		TAIGA: A new RISC-V soft-processor f	33% smaller & 39% faster than LEON3
openscale	http://www.lirm	stable	Lyonel Barthe	uBlaze	32	32	spartan-3	Lyonel Barthe		1563		4			91		i12.1	1.00	1.0	58.2	X	Y	vhdl	26	sb_core		yes			4G	4G	Y	86		32	5	2010	2012	www.lirmm.fr/AD	NoC secretblaze	data is for single secretblaze
secretblaze	http://www.lirm	beta	Lyonel Barthe	uBlaze	32	32	spartan-3	Lyonel Barthe		1563		4			91		i12.1	1.00	1.0	58.2	X		vhdl	26	sb_core		yes			4G	4G	Y	86		32	5	2010	2012	www.lirmm.fr/ADAC		
riscv_niosv	https://www.int	proprietar	Intel	risc-v	32	32	stratix-10	intel	fastest	1580		A		2	362	##	q21.3	1.00	1.0	229.1	A		proprietary			Y	yes	N		4G	4G	Y			32	5		2021		free license, small inst & data mem	RV32IA spec, M20K for reg file, interrupts
J1b_16	www.excamera	stable	James Bowman	forth	32	16	kintex-7-3	James	DFF ex	1588		6			355	##	14.7	1.00	1.0	223.4	X		verilog	3	j1	Y	forth	N		64K	64K		20			2	2006	2023		uCode inst, dual port block RAM	DFF used for 16 deep data & return stacks
cpugen	https://opencor	stable	Giovanni Ferrante	RISC	32	16	kintex-7-3	James Brakef		1597		6	8		154	##	14.7	1.00	1.0	96.3	AX		vhdl	14	cpuc	Y	asm	N	N								2003	2009		x86 .exe generates VHDL RISC uP	using 32 bit example
sayuri_cpu	http://www.mo	stable	Toyoaki Sagawa	RISC	32	32	kintex-7-3	James Brakef		1604		6			208	##	14.7	1.00	1.0	129.9	X		vhdl	13	cpu01				Y	4G	4G				32		2000	2000		dead weblink	high number of DFF
riscv_fwrisc	https://github.com/mball		Matthew Balance	risc-v	32	32	ice40	Matthew Bal		1653		4				##		1.00	6.7		AL		system	8	fwrisc_fpg	Y	yes	N		4G	4G	Y	45		32		2018	2018	https://opencores	featherweight entry 2018 RISC-V conf	0.15 DMIPS/MHz
p-vex	https://github.com/tvana		Thijs van As	VLIW	32	##	kintex-7-3	James	bypass	1660		6		1	233	##	14.7	1.00	1.0	140.1			vhdl	26	system	Y	yes	N							73		32	4	2005	2015	http://www.vliw.c	1, 2 or 4 issue VLIW, uses HP VEX too	probable degeneracy, LUT RAM for program m
zipcpu	https://github.c	stable	Dan Gisselquist	RISC	32	32	kintex-7-3	James Brakef		1687		6		2	218	##	14.7	1.00	1.0	128.9	AX		verilog	7	zipcpu	Y		N	N	4G	4G	Y	35		16	5	2015	2024	http://zipcpu.com	ISA has chnaged, multiple instruction	support for several FPGA boards
forth_kf532	https://github.c	stable	Tarasov Ilia	forth	32	6	kintex-7-3	James	no *.c	1719		6	4	4	172	##	14.7	1.00	1.0	100.3	X		vhdl	1	kf532	N		N	Y	1K	16K						2013	2013		no trace of source code on web	
riscv_wildcat	https://github.com/schoe		Martin Schoeberl	risc-v	32	32	cyclone4	Martin Schoe		1727	452	4			85			1.00	1.0	48.9	A		scala	32	singlecycl	Y	yes	N		4G	4G	Y			32	4		2025	https://arxiv.org/p	comparison of 3, 4 & 5 stage pipeline	papers show 3 & 5 stage pipelines
mips_up_vhdl	https://github.com/cm42		Chandra Mettu	mips	32	32	spartan7	James	no LUT	1744	2311	6			250	##	v23.2	1.00	1.0	143.3			vhdl	10	NYU6463	Y	yes	N		4G	4G	Y			32			2020		simple MIPS with comparison to RC5	considerable mapping of memory to logic?
riscv_steel	https://github.com/riscv-s		Rafael Calcada	risc-v	32	32	**zu-2e**	James Brakef		1775		6			208	##	v19.2	1.00	1.0	117.4			verilog	21	steel_top	Y	yes	N		4G	4G	Y			32	3	2020	2024	https://github.cor	github version has vivado proj	under grad thesis
riscv_steel	https://opencores.org/pr		Rafael Calcada	risc-v	32	32	atrix-7-3	James Brakef		1784		6			116	##	v19.2	1.00	1.0	65.0			verilog	21	steel_top	Y	yes	N		4G	4G	Y			32	3	2020	2024	https://github.cor	github version has vivado proj	under grad thesis, several web locations
riscv_rv32soc	https://github.com/tomve		tom verbeure	riscv	32	32	spartan3	James Brakef		1787	843	4	4	6	50	##	14.7	1.00	1.0	28.0	AX		verilog	18	top	Y	yes	N		4G	4G	Y			32			2018	https://tomverbe	vexriscv in verilog, VexRiscV CPU - A N	near infinite amount of configuration options
sweet32	https://opencor	alpha	Valentin Angelovski	MIPS	32	16	kintex-7-3	James Brakef		1797		6	1	2	185	##	14.7	1.00	1.0	103.1	X	Y	vhdl	28	sweet32_L	Y	yes	N	N	4G	4G	Y	26		16		2014	2015		targets MACHXO2, DDR RAM	clock divider to Sweet32_v1_core
ensilica	http://www.ens	proprietar	ensilica.com	eSi-3200	32	16	stratix-4	ensilica		1800		A			200			1.50	1.0	166.7	AX		verilog		eSi-3200	Y	yes			4G	4G	Y	104	10	16	5	2001	2016		verilog source included with license	room for 90 user inst, also as ASIC
cast_ba22	http://www.cas	proprietar	CAST Inc	RISC	32	16	spartan-6	CAST Inc		1800		6		32	72			1.00	1.0	40.0	X		proprietary			Y	yes			4G	4G				32				http://www.cast-i	Cast has uP related IP	several versions, FPGA kits
arm9-soft-cpu	https://github.com/risclit		Li Xinbing	ARM9	32	32	**zu-3e**	James Brakef		1807	736	6			357	##	v21.1	1.00	1.0	197.6			verilog	4	risclite_m	Y	yes	Y		4G	4G	Y						2020		ARMv4-compatible CPU core	no mult, interrupts or reg banks	
ARM_Cortex_M	http://www.arm	proprietar	ARM	ARM M1	32	16	virtex-5	ARM	65nm	1900		6			200			1.00	1.0	105.3	AX		proprietary			Y	yes	N		4G	4G	Y			16	3	2007		https://en.wikiped	ARM Cortex M0, M1 & M3 avail for FI	see xilinx Xcell64
j68	https://code.goo	stable	Frederic Requin	68000	32	16	stratix-2	Freder	speed	1900		4		4	180			1.00	6.0	15.8	A		verilog	1	j68	Y	yes	N		4G	4G	Y			16		2009	2014		for use with Minimig	micro-coded on stack machine
altor32_lite	https://opencor	stable	Ultra Embedded	OpenRISC	32	32	kintex-7-3	James Brakef		1928	1250	6			236	##	14.7	1.00	2.0	61.3	ALX		verilog	7	altor32	Y	yes	N	Y	4G	4G	Y					2012	2014	https://openrisc.io	simplified OpenRISC 1000, no pipelin	xilinx S3 primitives
risc5	http://www.pro	beta	Niklaus Wirth	RISC	32	32	zu-3e	James Brakef		1936	392	6	4		213	##	v21.1	1.00	1.0	109.9	ALX	Y	verilog	8	RISC5	Y	yes	Y		4G	4G				16		2013	2017	http://www.astro	minimalist Wirth, part of Project Obe	32x32 multiplier, wikipedia entry
mipsr2000	https://opencor	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James Brakef		1971		6	4	6	71	##	14.7	1.00	1.0	36.2	X		vhdl	35	Dm	Y	yes	N		4G	4G	Y			32	5	2012	2016		supports almost all instructions of mi	course project
mecrisp-ice	https://sourceforge.net/p		Matthias Koch	forth	32	16	spartan7	James Brakef		1976	2384	6	4	8	83	##	v23.2	1.00	2.0	21.1	LX	Y	verilog	48	j1a	Y	forth	N		4G	4G	Y					2011	2023		32-bit data size, some comments in G	distinct j1a.v for each data size
sc20	http://www.for	proprietar	Brad Eckert	forth	32	8	virtex-6	Brad Eckert		1977		6			150			1.00	1.0	75.9	X		proprietary														2010		PDF file, Forth Inc.	
risc5	http://www.pro	beta	Niklaus Wirth	RISC	32	32	zu-2e	James Brakef		2001	392	6	4		177	##	v20.1	1.00	1.0	88.3	ALX	Y	verilog	8	RISC5	Y	yes	Y		4G	4G				16		2013	2017	http://www.astro	minimalist Wirth, part of Project Obe	32x32 multiplier, wikipedia entry
mips_fault_tol	https://opencor	stable	Lazaridis Dimitris	MIPS	32	32	kintex-7-3	James Brakef		2017		6	4	6	45	##	14.7	1.00	1.0	22.5	X		vhdl	40	main	Y	yes	N		4G	4G	Y			32	5	2013	2013		arithmetic includes fault detection	no external memory port?
riscv_picorv32	https://github.c	beta	Clifford Wolf	risc-v	32	32	xcku3p-3	Cliffor	large	2019	1085	6			769	##	v16.2	1.00	3.0	127.0	X	Y	verilog	1	picorv32	Y	yes	N		4G	4G	Y			32		2016	2022	https://github.cor	minimal features, soc options	designed for minimum LUTs
riscv_pequeno	https://github.com/iamm		Mitu Raj	risc-v	32	32	artix7	Mitu R	16 cus	2084	1564	6			100	##		1.00	1.0	48.0	X		system	31	pqr5_core	Y	yes	N		4G	4G	Y	53		32	5	2022	2024	https://chipmunk	multi-page tutorial on uP design, peq	https://github.com/iammituraj/iammituraj
arm9-soft-cpu	https://github.com/risclit		Li Xinbing	ARM9	32	32	**zu-3e**	James Brakef		2098	778	6	4		238	##	v21.1	1.00	1.0	113.5			verilog	4	risclite_m	Y	yes	Y		4G	4G	Y						2020		ARMv4-compatible CPU core	no interrupts or reg banks	
m1_core	https://opencor	beta	Fabrizo Fazzino, Albert	MIPS?	32	32	arria-2	James Brakef		2101		A			190	##	q13.1	1.00	1.0	90.6	AX		verilog	9	m1_core		yes	N		4G	4G	Y			32		2007	2012		GCC target?	
oberon_sdram	http://projectob	beta	Nicolae Dumitrache	RISC	32	32	kintex-7-3	James Brakef		2103		6		1	104	##	14.7	1.00	1.0	49.5	X		verilog	16	risc5	Y	yes	Y		4G	4G				16		2013	2017		minimalist Wirth, part of Project Obe	modified to use DRAM, serial mult
yarvi	https://github.c	beta	Tommy Thorn	risc-v	32	32	kintex-7-3	James Brakef		2152		6		17	122	##	14.7	1.00	2.0	28.3	X		verilog	3	yarvi_soc	Y	yes	N	N	4G	4G				32	3		2016		no multiply or divide	simple implementation of RISC-V
latticemico32	http://www.latt	stable	Yann Siommeau, Mich	LM32	32	32	arria_2	James Brakef		2166		A	4	30	149	##	q13.1	0.80	1.0	55.0	LX		verilog	24	lm32_cpu	Y	yes	N	Y	4G	4G	Y			32	6	2006	2017	https://en.wikiped	optional data & inst caches	Diamond3.10; see lm32 & misoc folders
riscompatible	https://opencor	beta	Andre Soares	RISC	32	32	kintex-7-3	James	set IO	2167		6		1	145	##	14.7	1.00	3.0	22.3	X		vhdl	12	riscompat	Y	yes	N	Y	4G	4G	Y			16		2014			based on RISCO processor by Junquei	ra & Suzim 1993
ensilica	http://www.ens	proprietar	ensilica.com	eSi-3200	32	16	stratix-4	ensilica		2200		A			200			2.00	1.0	181.8	AX		verilog		eSi-3250	Y	yes			4G	4G	Y	104	10	16	5	2001	2016		verilog source included with license	room for 90 user inst, also as ASIC
microblaze-v	https://www.amd.com/en		Xilinx	riscv	32	32	Kintex Ult	Xilinx	ucontr	2201	1136	6	4		426	##	v24.1	1.00	1.0	193.5	X		proprietary			Y	yes	opt	Y	4G	4G	Y	86		32		2023	2024	https://docs.amd.	in Vivado at no extra cost	253Mhz max, numbers for 11 diff devices
yacc	https://opencor	stable	Tak Sugawara	MIPS	32	32	kintex-7-3	James	map e	2220		6	6			##	14.7	1.00	1.0		AX		verilog	10	yacc2	Y	yes	N		4G	4G	Y			32	5	2005	2009		derived from, but independent of pla	YACC Yet Another CPU CPU
cpu_32	https://github.com/aslak3		Lawrence Manning	risc	32	32	spartan7	James Brakef		2281	785	6	2		104	##	v23.2	1.00	1.0	45.7	X		vhdl	16	cpu32	Y	asm	N		64K	64K	Y	32		16			2022	https://www.yout	**uses customasm,** doc in readme.m	VGA pattern generator youtube video
storm_core	https://opencor	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakef		2312		6	3		179	##	14.7	1.00	1.0	77.4	AX		vhdl	16	core	Y	yes	N		4G	4G	Y			32	8	2011	2014		Storm Core (ARM7 compatible)	I & D caches not compiled
eco32	https://opencor	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James Brakef		2339		6		1	160	##	14.7	1.00	1.5	45.5	ALX	Y	verilog	14	cpu	Y	yes	N		512M	256M	Y	61		32		2003	2022	https://github.cor	MIPS like, slow mul & div	
arm_rusian	https://github.com/0xD5C		ruslan	arm	32	32	**zu-3e**	James	LUT RA	2360	4815	6			200	##	v21.1	1.00	1.0	84.7			system	6	ARM_Mul	Y	yes	Y		4G	4G	Y			16			2019		from "Digital design and computer ar	single cycle,
latticemico32	http://www.latt	stable	Yann Siommeau, Mich	LM32	32	32	ECP3	Lattice Semic		2370		4	4	30	115			0.80	1.0	38.8	LX		verilog	24	lm32_cpu	Y	yes	N	Y	4G	4G	Y			32	6	2006	2017	https://en.wikiped	optional data & inst caches	Diamond3.10; see lm32 & misoc folders
riscv_vanilla	https://github.c	verified	Ben Marshall	risc-v	32	32	zu-5e	James	IO limi	2422		6				##	v21.1	1.00	2.0				verilog	26	frv_cpu_a	Y	yes	N		4G	4G	Y			32	5		2019		"toy" 5 stage RISC-V CPU, implementing	the rv32imc
riscv_vanilla	https://github.c	verified	Ben Marshall	risc-v	32	32	artix-7	Ben Marshall		2422		6			150			1.00	2.0	31.0			verilog	26	frv_cpu_a	Y	yes	N		4G	4G	Y			32	5		2019		"toy" 5 stage RISC-V CPU, implementing	the rv32imc
risc5	http://www.pro	beta	Niklaus Wirth	RISC	32	32	kintex-7-3	James Brakef		2441		6	4	1	92	##	14.7	1.00	1.0	37.8	ALX	Y	verilog	8	RISC5	Y	yes	Y		4G	4G				16		2013	2017	http://www.astro	minimalist Wirth, part of Project Obe	32x32 multiplier, wikipedia entry
plasma	https://opencor	stable	Steve Rhoads	MIPS	32	32	kintex-7-3	James Brakef		2462		6		3	97	##	14.7	1.00	1.0	39.5	X		vhdl	22	plasma	Y	yes	N		4G	4G	Y			32		2001	2016	http://plasmacpu.	wide outside use, opencores page has list of related publications	
classic_mips	https://github.com/Kazaw		Xavier Yuhan Liu	mips	32	32	artix-7	Xavier	some	2463	1289	6				##	v2017	1.00	1.0		X		verilog	30	top	Y	yes	N		4G	4G	Y			32	5	2017	2024		Minisys-1 ISA, pipelined and non-pipe	English RTL, comments in Chinese
riscv_potato	https://github.c	beta	Kristian Skordal	risc-v	32	32	kintex-7-3	James Brakef		2467		6			116	##	14.7	1.00	1.0	47.1	X	B	vhdl	24	pp_core	Y	yes	N	N	4G	4G	Y	30		32		2014	2020		risc-V interger only, no mult	"rocket-core" version at risc.org
ucore	https://opencor	stable	Whitewill	MIPS	32	32	kintex-7-3	James Brakef		2469		6		1	231	##	14.7	1.00	1.0	93.5	X		verilog	25	ucore	Y	yes	N		4G	4G	Y			32	6	2005	2010		MMU & caches	
zpuino	http://alvie.com	alpha	Alvaro Lopes	forth	32	8	spartan6	James Brakef		2547	2200	6	4	11.5	126	##	14.7	1.00	4.0	12.3	X	Y	vhdl		papilio_pr	Y	yes	N		4G	4G	Y	37				2008	2018	https://github.cor	SoC version of modified ZPU	pipelined, removed ucf file
temlib	http://temlib.or	stable		SPARC	32	32	kintex-7-3	James Brakef		2579		6		32	111	##	14.7	1.00	1.0	43.1	X		vhdl	48	mcu_simple			Y	N	4G	4G	Y		64			2013	2015		copywrite: experimental use	has caches
altor32	https://opencor	stable	Ultra Embedded	OpenRISC	32	32	kintex-7-3	James Brakef		2602	1578	6		5	192	##	14.7	1.00	1.0	73.9	ALX		verilog	16	altor32	Y	yes	N	Y	4G	4G	Y					2012	2015	https://openrisc.io	simplified OpenRISC 1000	xilinx S3 primitives
J1b	www.excamera	stable	James Bowman	forth	32	16	kintex-7-3	James	DFF ex	2612		6			302	##	14.7	1.00	1.0	115.5	X		verilog	3	j1	Y	forth	N		64K	64K		20			2	2006	2023		uCode inst, dual port block RAM	DFF used for 32 deep data & return stacks
riscv_clarvi	https://github.c	stable	Robert Eady	risc-v	32	32	arria-2	James	Altera	2616		A			178	##	q18.0	1.00	1.0	68.2	A	B	system	7	clarvi	Y	yes	N		4G	4G	Y			32	6	2016	2017	https://www.cl.ca	educational simple RISC-V implement	doesn't make use of block RAM RTL
moxielite	https://github.c	stable	Anthony Green	RISC	32	32	arria-2	James Brakef		2696		A	4		93	##	q18.0	1.00	1.0	34.6	X		vhdl	11	moxielite					4G	4G	Y			16		2009	2017	https://github.com/atgreen/moxie-cores		
mor1kx	https://github.c	stable	Julius Baxter	OpenRISC	32	32	kintex-7-3	James Brakef		2718		6	3	3	217	##	14.7	1.00	1.0	80.0	X		verilog	48	mor1kx	Y	yes	N		4G	4G	Y			32		2012	2024	https://www.yout	lots of configuration parameters	considered best openrisc design
mais		stable	Rene Doss	MIPS	32	32	kintex-7-3	James Brakef		2760		6	4	5	245	##	14.7	1.00	1.0	88.7	X		vhdl	22	MAIS_soc	Y	yes	N	N	4G	4G				32	5	2013		use MIPS tools	register forwarding around ALU	license req'd for commercial use
riscv_picorv32	https://github.c	beta	Clifford Wolf	risc-v	32	32	GW1NR-9	Jean-L	small	2764	1833	4			8	##	27	##		1.00	3.0	3.3	X		verilog	1	picorv32	Y	yes	N		4G	4G	Y			32		2016	2022	https://www.cnx-	mimimal features, soc options	https://github.com/sipeed/TangNano-9K-exan
s6soc	https://opencor	stable	Dan Gisselquist	RISC	32	32	spartan-6	James	sparta	2820		6	1	10	133	##	14.7	1.00	1.0	47.3	X	Y	verilog	31	toplevel			N	N	4G	4G	N	20		16	5	2015				uses ZIP CPU

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
armv4_uarch	https://github.com/granty		Grant Wilk	ARM9	32	32	**max10**	Grant Wilk		2860		4			50	##	q18.0	1.00	1.0	17.5	A		vhdl	18		Y	yes	N		4G	4G	Y			16			2020	https://grantwilk.	custom uarch for the ARMv4 ISA on I	course work, top level is schematic
microcore	https://github.c	beta	Klaus Schleisiek	forth	32	8	XP2	Klaus Schleisi		2864		4			33	##	3.12	1.00	1.0	11.5	AILX		vhdl	38	ucore	Y	asm	N	Y	3K	8K	Y	84				1999	2023		**easy to add op-codes, fltg-pt opt., si**	**12, 16, 27 & 32 bit data sizes**
risc5	http://www.pro	beta	Niklaus Wirth	RISC	32	32	atrix7-35	James Brakef		2913		6		48	50	##	v20.1	1.00	1.0	17.2	ALX	Y	verilog	8	RISC5Top	Y	yes	Y		4G	4G				16		2013	2018	https://people.inf	minimalist Wirth, part of Project Obe	32x32 multiplier, wikipedia entry
dlx_chiara	https://github.c	stable	Alessandro Di Chiara	DLX	32	32	kintex-7-3	James Brakef		2915		6			90	##	14.7	1.00	1.0	30.9	X		vhdl	32	a-dlx	Y	yes	N		4G	4G				32	5	2017	2017		Course project, no RTL comments, VHDL via instructor?	
leon3	http://www.gais	stable	Jiri Gaisler, Jan Anders	SPARC	32	32	kintex-7-3	Jiri Gaisler		2920		6			183			1.00	1.0	62.7	AILX	Y	vhdl	100s	leon3x	Y	yes	Y		4G	4G	Y			64	7	2003	2021	https://en.wikiped	**customized for ~50 FPGA boards,**	**xls with utilization for all targets**
minimips	https://opencor	stable	Samuel Hangouet	RISC	32	32	kintex-7-3	James Brakef		2939	1886	6	8		118	##	14.7	1.00	1.0	40.1	X		vhdl	12	minimips	Y	yes	N	N	4G	4G				32	5	2004	2018		based on MIPS I	
myforthproces	https://opencor	stable	Gerhard Hohner	forth	32	8	SP-kintex	James Brakef		2959		6		6	223	##	14.7	1.00	1.0	75.3	X		vhdl	58	mycpu	Y	yes	N		64M	64M		96				2004	2012		DPANS'94 32-bit Forth, masters thesi	25.15 Whetstones
asip38	https://aaltodoc.aalto.fi/b		Lauri Isola	accum	32	38	**zu-3e**	James	xilinx I	2962	1056	6	4	35	100	##	v22.2	1.00	1.0	33.8	X	Y	vhdl	14	top	Y	asm	N	Y	16K	16K	N	31	4	4		2018	2021	http://www.kolun	Application-Specific Instruction set Pr	missing prog & data mem, missing mult
asip38	https://aaltodoc.aalto.fi/b		Lauri Isola	accum	32	38	**zu-3e**	James	xilinx I	2962	1056	6	4	35	100	##	v22.2	1.00	1.0	33.8	X	Y	vhdl	14	asip38	Y	asm	N	Y	16K	16K	N	31	4	4		2018	2021	http://www.kolun	Application-Specific Instruction set Pr	missing prog & data mem, missing mult
octagon	https://opencor	beta	Jon Pry	MIPS	32	32	kintex-7-3	James Brakef		3021		6	4	9	333	##	14.7	1.00	1.0	110.2	X		vhdl	46	octagon		asm			4G	4G	Y			32		2015	2015	https://github.cor	8 thread barrel processor, largely MIPS compatible	
vscale	https://github.c	stable	UC Berkeley	risc-v	32	32	kintex-7-3	James Brakef		3072		6			127	##	14.7	1.00	1.0	41.2	X		verilog	23	vscale_core			N							32		2016	2017		risc-v RV32IM vscale processor, depre	depreciated: not up to date (risc-v)
qrisc32	https://opencor	alpha	Viacheslav	RISC	32	32	arria-2	James Brakef		3075		A	4		144	##	q13.1	1.00	1.0	46.9	A		system	8	qrisc32	Y	yes	N		4G	4G	Y			32	4	2010	2011		qrisc32 wishbone compatible risc cor	for PhD thesis
amber	https://opencor	stable	Conor Santifort	ARM7	32	32	**zu-3e**	James	area o	3105	1857	6		10	168	##	v21.1	0.75	1.0	40.7	ALX		verilog	25	a23_core	Y	yes	N		4G	4G	Y	80		16	3	2010	2017	https://en.wikiped	no MMU, shared cache	
moxielite	https://github.c	stable	Anthony Green	RISC	32	32	kintex-7-3	James Brakef		3159		6	3		152	##	14.7	1.00	1.0	48.0	X		vhdl	11	moxielite_wb					4G	4G	Y			16		2009	2017	https://github.com/atgreen/moxie-cores		
riscv_rpu	https://github.c	untested	Colin Riley	risc-v	32	32	artix-7	Colin Riley		3291	1156	6	12	1	200	##	14.7	1.00	1.0	60.8	X	Y	vhdl	14	core	Y	yes	N		4G	4G	Y			32		2015	2020	http://labs.domip	Series of 16 tutorials on uP design, w	RPU uP, TPU now discarded
or1k	https://opencor	stable	Julius Baxter, Stefan K	OpenRISC	32	32	kintex-7-3	James Brakef		3299		6	3	3	189	##	14.7	1.00	1.0	57.3	AX		verilog	39	mor1kx	Y	yes	N	M	4G	4G	Y			32		2001	2018	https://opencores	no longer supported, see mor1kx	cappuccino ALU
altium/TSK300	http://techdocs.	proprietar	Altium	RISC	32	32	spartan-3	Altium		3326	1776	4		4	50			1.00	1.0	15.0	ALX		proprietary			Y	yes	N	N	4G	4G	Y					2004	2017	CR0140.pdf, http:/	frozen, asm, C, C++, schem, VHDL & V	clock: 50MHz, opt mult/div, #s for other fpgas
eco32	https://opencor	stable	Hellwing Geisse	RISC	32	32	kintex-7-3	James Brakef		3367		6		5	147	##	14.7	1.00	1.5	29.1	ALX	Y	verilog	24	eco32	Y	yes	N		512M	256M	Y	61		32		2003	2022	homepages.thm.d	MIPS like, slow mul & div	
ep32	https://www.an	proprietar	C.H. Ting	forth	32	6	XP2	C.H. Ting		3368		4					ispL	1.00	1.0		L		proprietary										29				2007	2018	https://wiki.forth-	kindle book & RTL available: EP32 RIS	RTL: $25 from C.H. Ting
riscv_reonv	https://github.com/lcbcFc		Lucas Castro	risc-v	32	32	spartan6	Wajih Yousse		3370		6			133			1.00	1.0	39.4						Y	yes	N		4G	4G	Y	45		32			2018	https://www.hind	Lightweight Cryptographic Instructior	risc-v version on Leon3 tools
fisa32	https://github.c	beta	Robert Finch	RISC	32	32	kintex-7-3	James Brakef		3479		6	3	2	152	##	14.7	1.00	1.0	43.7	X		verilog	1	FISA32	Y		N	Y						32		2014	2014	https://github.com/robfinch/Cores		
storm_soc	https://opencor	beta	Stephan Nolting	ARM7	32	32	kintex-7-3	James Brakef		3514		6	3	4	159	##	14.7	1.00	1.0	45.2	X	Y	vhdl	40	storm_top	Y	yes	N		4G	4G	Y			32	8	2012	2015		STORM SoC	cache & no peripherals
cpu_basic	https://github.com/vhdlf/		vhdlf	x86	32	8	cyclone-4	vhdlf		3558	715	4	4			##	q19.1				A		vhdl	7	top	Y		N		64K	64K	Y	26		16			2020		32-bit CPU with x86 inst. format	readme has screen shots, **very readable RTL**
aquarius	https://opencor	stable	Thorn Aitch	SuperH-2	32	16	**zu-3e**	James	vivado	3563	1384	6	2	16	147	##	v21.1	1.00	1.0	41.2	ALX		verilog	21	top	Y	yes	N		4G	4G	Y					2003	2015	http://0pf.org/j-co	clone of Hitachi SH-2	project seems to have stalled
arm_rusian	https://github.com/0xD5(		ruslan	arm	32	32	**zu-3e**	James	LUT R	3563		6			147	##	v21.1	1.00	1.0	41.2			system veril		ARM_Sing	Y	yes	Y		4G	4G	Y			16			2019		from "Digital design and computer ar	multi-cycle
aspida	https://opencor	stable	Sotiriou	DLX	32	32	kintex-7-3	James	dated	3586		6			257	##	14.7	1.00	1.0	71.7	X		verilog	10	DLX_top	Y	yes			4G	4G						2002	2009		DLX	compiled sync version
yari	https://github.c	stable	Tommy Thorn	MIPS	32	32	kintex-7-3	James Brakef		3610		6		15	189	##	14.7	1.00	1.0	52.3	X	Y	verilog	8	top					2M	2M				32		2004	2008		subset of MIPS R3000	
lgp30	http://www.e-b	stable	Stanley Frankel	accum	32	32	spartan6	Stanle	severa	3646	1411	6	1	15	100	##	14.7	1.00	3.0	9.1		Y	vhdl	42	LGP-30	Y	yes	N		4K	4K	N			3			2017		FPGA version of LGP30 drum computer, also LGP21, RPC4000, 65F02	
mips32	https://opencor	stable	Jin Jifang	MIPS	32	32	kintex-7-3	James Brakef		3696		6		8	192	##	v17.4	1.00	1.0	52.0	X		verilog	17	pipelinem	Y	yes			4G	4G	y	57		32	5	2017	2021		vivado project, ISA at github page	"classic MIPS"
mips32r1	https://opencor	stable	Grant Ayers	MIPS	32	32	arria-2	James Brakef		3716		A	8		79	##	q13.1	1.00	1.0	21.3	AX		verilog	20	processor	Y	yes	N	Y	4G	4G	Y			32	5	2012	2015	https://github.cor	Harvard arch	complete software tool chain
temlib	http://temlib.or	stable		SPARC	32	32	kintex-7-3	James Brakef		3730		6	5		111	##	14.7	1.00	1.0	29.8	X		vhdl	48	fpu_simple			Y	N	4G	4G	Y			64		2013	2015		copywrite: experimental use	options for fltg-pt, pipeline, mul & div configur
klc32	https://opencor	planning	Robert Finch	RISC	32	32	kintex-7-3	James Brakef		3790		6	4	1	200	##	14.7	1.00	4.0	13.2	X		verilog	25	KLC32	Y	asm	N		4G	4G	Y			32		2011	2012	https://github.cor	single ported block RAM register file :(	heavy use of includes
eco32f	https://github.c	stable	Stefan Kristiansson	RISC	32	32	kintex-7-3	James Brakef		3845		6	3	4	123	##	14.7	1.00	1.0	32.1	X		verilog	12	eco32f	Y	yes	N		512M	256M	Y	61		32	6	2014	2014		pipelined version of the eco32 CPU	cache & mmu
arm9-soft-cpu	https://github.com/risclite		Li Xinbing	ARM9	32	32	**zu-3e**	James Brakef		3914	1257	6	4		167	##	v21.1	1.00	1.0	42.6			verilog	4	arm9_con	Y	yes	Y		4G	4G	Y						2020		ARMv4-compatible CPU core	Dhrystone value: 1.2 DMIPS/MHz
aquarius	https://opencor	stable	Thorn Aitch	SuperH-2	32	16	kintex-7-3	James Brakef		4071		6	2	10	97	##	14.7	1.00	1.0	23.7	ALX		verilog	21	top	Y	yes	N		4G	4G	Y					2003	2015	http://0pf.org/j-co	clone of Hitachi SH-2	project seems to have stalled
aor3000	https://opencor	beta	Aleksander Osman	MIPS	32	32	**zu-3e**	James	high F	4199	2520	6	4	8	175	##	v21.1	1.00	1.0	41.8	AX		verilog	19	aoR3000	Y	yes	N		4G	4G	Y			32	5	2014	2015		MIPS R3000A compatible, has MMU	moved declarations forward
cpus-caddr	https://github.com/lisper/		Brad Parker	lisp	32	48	spartan6	Brad P	ran his	4223	2794	6		102	50	##	14.7	1.00	1.0	11.8	X		verilog	70	top	Y	lisp		Y	16M	16K						2011	2016	https://dspace.mi	Verilog FPGA re-implementation of M	uses 48-bit u-code, multiple clocks
af65k	https://github.c	alpha	Andre Fachat	6502	32	8	kintex-7-3	James Brakef		4424	873	6			69	##	14.7	1.00	4.0	3.9	X		vhdl	13	gecko65k	Y		N	N								2011	2019	http://www.6502.	extended 6502 AKA 65K with 16, 32 or 64 bit data	
ARM_Cortex_A	https://develope	ASIC	ARM	ARM A9	32	16	arria V	altera		4500		A			1050			2.50	1.0	583.3			asic			Y	yes	Y		4G	4G	Y	80		16	10		2012	https://en.wikiped	uses pro-rated LC area	dual issue, includes fltg-pt & MMU & caches
mc68kods	https://sites.goo	beta	Olivier De Smet	68000	32	16	kintex-7-3	James	errors	4617		6				##	14.7	1.00	8.0			Y	vhdl	10	mc68kods												2011			SOC for HP9816 computer emulation	
btsr1arch	https://github.c	beta	Brendan Bohannon	CISC	32	16	kintex-7-3	James Brakef		4762		6		10	167	##	14.7	1.00	1.5	23.3	X		verilog	11	bsrexunit	Y	yes	Y	N	64K	64K	Y	64		32		2018	2024		is BtSR1, msp430 like, fltg-pt defined	3 data sizes, no (R++) or (--R) modes
minsoc	https://opencor	stable	Raul Fajardo etal	OpenRISC	32	32	kintex-7-3	James Brakef		4945		6	4	8	107	##	14.7	1.00	1.0	21.7	ALX	Y	verilog	88	or1200_tc	Y	yes	Y	M	4G	4G	Y			32		2009	2013	https://github.cor	minimal OR1200, vendor neutral, has caches	
or1200mp	https://github.c	stable	Stefan Wallentowitz	OpenRISC	32	32	kintex-7-3	James Brakef		4960		6	4	8	111	##	14.7	1.00	1.0	22.4	X		verilog	104	or1200_tc	Y	yes	Y	M	4G	4G	Y			32		2012	2012	https://openrisc.io	multiprocessor variant, single core	
nige_machine	https://github.c	stable	Andrew Read	forth	32	8	kintex-7-3	James Brakef		5033		6	8	33	123	##	14.7	1.00	1.0	24.5	X		vhdl	29	Board	Y	yes	N		16M	16M		512		512			2014		standalone Forth system	https://www.youtube.com/watch?v=PRItE8q6
amber	https://opencor	stable	Conor Santifort	ARM7	32	32	**zu-3e**	James	area o	5066	2382	6		20	175	##	v21.1	1.05	1.0	36.4	ALX		verilog	25	a25_core	Y	yes	N		4G	4G	Y	80		16	5	2010	2017	https://en.wikiped	no MMU	
or1200	https://github.c	stable	Damjan Lampret	OpenRISC	32	32	kintex-7-3	James Brakef		5231		6	4	8	118	##	14.7	1.00	1.0	22.5	X		verilog	78	or1200_tc	Y	yes	Y	M	4G	4G	Y			32		2010	2015	https://openrisc.io	best older openrisc implementation	no LUT RAM for reg file
aor3000	https://opencor	beta	Aleksander Osman	MIPS	32	32	kintex-7-3	James Brakef		5307		6	4	9	129	##	14.7	1.00	1.0	24.2	AX		verilog	19	aoR3000	Y	yes	N		4G	4G	Y			32	5	2014	2015		MIPS R3000A compatible, has MMU	moved declarations forward
edge	https://opencor	alpha	Hesham ALMatary	MIPS	32	32	spartan-6	James Brakef		5345		6	7	1	8	##	14.7	1.00	1.0	1.5	X		verilog	30	edge_core	Y	yes	N	N	4G	4G	Y			32	5	2014	2014		Edge Processor (MIPS)	MIPS1 clone
or1200_hp	https://opencor	stable	Strauch Tobias	OpenRISC	32	32	virtex-5	Strauc	3 slot	5602		6			185	##		1.00	1.0	33.1	X		verilog	39	or1200_ic	Y	yes	Y	M	4G	4G	Y			32		2010	2013	https://openrisc.io	3 slot barrel version of OR1200	numbers from published paper
table888	https://github.c	alpha	Robert Finch	RISC	32	16	kintex-7-3	James Brakef		5756		6	9	6	137	##	14.7	2.00	1.0	47.6	X		verilog	3	table888	ome				4G	4G	Y	130		8		2014	2016		2016 version gives same reults as 201	code for cache & mmu incomplete
leon2	https://github.c	stable	Jiri Gaisler	SPARC	32	32	kintex-7-3	James Brakef		5992		6	1	12	133	##	14.7	1.00	1.0	22.3	X		vhdl	82	leon	Y	yes	Y		4G	4G	Y			64	5	1999	2003	https://en.wikiped	large config file, rad-hard asic version	https://www.gaisler.com/index.php/products/
amber	https://opencor	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakef		6103		6		18	127	##	v18.2	1.05	1.0	21.8	ALX		verilog	25	a25_core	Y	yes	N		4G	4G	Y	80		16	3	2010	2017	https://en.wikiped	no MMU	
kpu	https://github.c	alpha	Andrea Corallo	RISC	32	32	kintex-7-3	James	missin	6178		6	3		19	##	14.7	1.00	1.0	3.0	X	Y	verilog	19	kpu	Y	yes	N	Y	4G	4G				32		2016	2018	http://andreacora	KPU is a minimal system on chip written used as testbench for the KPU core	
cmips	https://github.c	mature	Roberto Hexsel	MIPS	32	32	cyclone4	Roberto Hexs		6347	2596	4		22	50	##		1.00	1.0	7.9	A	Y	vhdl	22	core	Y	yes	N	N	4G	4G	Y			32	5	2017	2019	http://www.inf.uf	5-stage pipeline, MIPS32r2 core	
amber	https://opencor	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakef		6409	2351	6		2	82	##	14.7	0.75	1.0	9.6	ALX		verilog	25	a23_core	Y	yes	N		4G	4G	Y	80		16	3	2010	2017	https://en.wikiped	no MMU, shared cache	2048 LUTs used as single port RAM
piropiro	https://github.c	stable	pandora2000	RISC	32	32	kintex-7-3	James	port m	7491		6	11	1	118	##	14.7	1.00	1.0	15.7	X		vhdl	42	top			Y	N	64K	64K	Y			32		2010	2011		five variants	no doc, xilinx constraint file
leon2	https://github.c	stable	Jiri Gaisler	SPARC	32	32	cyclone-1	Klas Westerlu		7554		4		42	50	##		1.00	1.0	6.6	A		vhdl	90	leon	Y	yes	Y		4G	4G	Y			64	5	1999	2003	https://en.wikiped	LUT #s from Nios vs Leon2 compariso	https://www.gaisler.com/index.php/products/
zap	https://opencor	alpha	Revanth Kamaraj	ARM7	32	32	kintex-7-3	James Brakef		7558		6	1	9	135	##	14.7	1.00	1.0	17.9	X		verilog	37	zap_top	Y	yes	N	N	4G	4G	Y			16		2017	2022	https://github.cor	ARMv4T & Thumbv1	has cache & mmu
mangomips32	https://github.c	stable	Ricky Tino	MIPS	32	32	spartan7	James Brakef		7923	4802	6	4		100	##	v23.2	1.00	1.0	12.6			verilog	25	mangomip	Y	yes	N		4G	4G	Y	100		32	5	2019	2023		cache support, runs linux	very percise specs, 100MHz on Artix7-2
xulalx25soc	https://opencor	mature	Dan Gisselquist	RISC	32	32	spartan6-	James	Sparta	7936		6	4	25	87	##	14.7	1.00	1.0	11.0	X	Y	verilog		toplevel			N	N	4G	4G	N	20		16	5	2015				uses ZIP CPU
opa	https://github.c	stable	Wesley W. Terpstra	RISC	32	32	cyclone-5	Wesle	largest	8540		A			125		q15.0	1.00	0.5	29.3	A		vhdl												32		2013	2016		An Out-of-Order Superscalar Soft CPU	tested, incomplete
riscv_picorv32	https://github.c	beta	Clifford Wolf	risc-v	32	32	GW1NR-9	Jean-L	large	8594	5278	4	2	32	27	##		1.00	3.0	1.0	X	Y	verilog	1	picorv32	Y	yes	N		4G	4G	Y			32		2016	2022	https://www.cnx-	mimimal features, soc options	inclueds all peripherals
riscv_microsen	https://github.c	stable	Microsemi	risc-v	32	32	polarfire	microsemi		8614		4	2	10	122		L11.8	1.00	1.0	14.2			proprietary			Y	yes	N		4G	4G	Y			32		2016	2018	https://www.micr	is encrypted IP	has caches
propeller_p8x3	https://www.pa	stable	Chip Gracey	RISC	32	32	kintex-7-3	James Brakef		9498		6		20	160	##	14.7	1.00	0.1	134.8	X		verilog	9	top	Y	yes										2014			eight propellers, clocking from ucf file	several FPGA card build files
m32632	https://opencor	stable	Udo Moeller	32032	32	8	kintex-7-3	James Brakef		10167		6	19	16	83	##	14.7	1.00	1.0	8.2	AX		verilog	18	example	Y	yes	Y	Y	4G	4G	Y	200		24	3	2009	2019	http://cpu-ns32k.net/		21.97 VAX Mips at 50MHz (Cyclone IV)
zap	https://opencor	alpha	Revanth Kamaraj	ARM7	32	32	arria-2	James	high D	10284		A	2	38	111	##	q18.0	1.00	1.0	10.8	X		verilog	37	zap_top	Y	yes	N	N	4G	4G	Y			16		2017	2022	ddi0100e_armv1-	ARMv4T & Thumbv1	has cache & mmu
mipsfpga	https://www.mi	stable	MIPS Technologies	MIPS	32	32	atrix-7-3	James Brakef		10692		6		47	118	##	14.7	1.00	1.0	11.0	X	Y	verilog	193	mfp_syste	Y	yes	N		4G	4G	Y			32		2014	2018	https://www.yout	M14K core & mipsfpga-plus	DRAM interface, I&D caches. 8789 FF
egpu	https://arxiv.org/pdf/240		Martin Langhammer	risc	32	40	agilex	Langh	no RTL	10697	26618	A	32	259	771	##	q22.4	8.00	1.0	576.6	A							Y		4G	4G		63		32			2024	https://ar5iv.labs.	800MHz in Agilex FPGA, word size and ISA configured for each task	
mist1032	https://github.c	stable	Takahiro Ito	RISC	32	32	arria_2	James	altera	10801		A	4	125	98	##	q18.0	1.00	1.0	9.1			system	50	mist32e10	Y				4G	4G	Y			64			2014		mist32 uP: embedded version	
rtf65002	https://opencor	alpha	Robert Finch	accum	32	8	kintex-7-3	James Brakef		11216		6	4	6	123	##	v14.1	0.67	2.0	3.7	X		verilog	10	rtf65002d	Y		N		4G	4G	Y			16		2013	2013	https://github.cor	32-bit 6502 + 6502 emulation	"proven"
amber	https://opencor	stable	Conor Santifort	ARM7	32	32	kintex-7-3	James Brakef		12450	3502	6		2	98	##	14.7	1.05	1.0	8.2	ALX		verilog	25	a25_core	Y	yes	N		4G	4G	Y	80		16	3	2010	2017	https://en.wikiped	no MMU	4330 LUTs used as RAM
forwardcom	https://github.c	stable	Agner Fog	cisc	32	32	atrix-7	Agner Fog		13248	4990	6			64	##	v20.1	1.00	1.0	4.8	X		system	18	top	Y	asm	Y		64K	32K	Y			64		2016	2023	https://www.forw	x86 like, complete ISA, MMX & vector	x86 adr modes, vector inst use width of vect re
riscv_naxriscv	https://github.com/Spinal		Charles Papon?	risc-v	32	32	artix7	Charle	AKA sp	13300	10300	6	4	12	155			1.00	0.4	29.1			scala			Y	yes	N		4G	4G	Y			32			2024	https://spinalhdl.g	OoO execution w/reg renaming, Superscalar(2 decode, 3 execution units, 2 retire), 2	
milkymist	https://github.c	stable	Sebastien Bourdeaudu	LM32	32	32	spartan-6	James	failed	13531		6	31	78	50	##	14.7	0.80	1.0	3.0	X	Y	verilog	169	system	Y	yes	N	Y	4G	4G	Y			32	6	2007	2014		uses LM32, uses Spartan-6 IO	failed in mapper
riscv_rv01_cor	https://opencor	stable	Stefano Tonello	risc-v	32	32	kintex-7-3	James Brakef		13997		6	4	62	130	##	14.7	1.00	1.0	9.3	X		vhdl	65	rv01_selft	Y	yes	N		4G	4G	Y			32		2015	2017		all files in one directory	two self test tops
riscv_humming	https://github.c	stable		risc-v	32	32	kintex-7-3	James Brakef		14119		6		32	62	##	14.7	1.00	1.0	4.4	X	Y	verilog	141	e203_soc_	Y	yes	N		4G	4G	Y			32		2016	2022	https://github.cor	e200 has opensource	also have a chip
v586	https://opencor	beta	Jose Rissetto	x86	32	8	kintex-7-3	James Brakef		22282		6	12	16	102	##	14.7	1.00	2.0	2.3	X		verilog	22	v586	Y	yes	N		1M	1M	Y					2014	2016	https://github.cor	MMU & caches, branch cache	www.youtube.com/channel/UCNbm8Bah54cw
ktc32	https://github.c	stable	kinpoko	risc	32	16	spartan7	James	sparta	27408	6554	6		44	125	##	v23.2	1.00	1.0	4.6	X	Y	system	15	top	Y	yes	N		4G	4G	Y	37		32		2022	2023		full basic ISA, hobby 32-bit CPU	see also zktc, xdc file, 16 & 32-bit insts
riscv_rsd	https://github.com/rsd-de		Susumu Mashimo	risc-v	32	32	zynq	Susumu Masl		28166		6			90			1.00	1.0	3.2			system verilog			Y	yes	N		4G	4G	Y			32			2020		RISC-V out-of-order superscalar proce	can be synthesized for small FPGAs
riscv_swerv	https://github.com/chipsa		Western Digital	risc-v	32	32	ZCU102	Weste	high L	30128		6	4	62	100			1.00	0.5	6.6			system	45	veer_wrap	Y	yes	N		4G	4G	Y			32	9	2019	2022	https://blog.weste	9 stage pipe, dual issue	risc-v SoC for fpga, riscv_swerv_eh1_fpga now
ztapchip	https://github.c	stable	Vuony Nguyen	MIPS	32	32	cyclone5	James Brakef		31331		A	43	578	100	##	q18.0	1.00	1.0	3.2	AX	Y	vhdl	53	ztachip												2015	2015		multi-core with MIPS master	files no longer available, was under developme
sp-i586	https://github.c	stable	Lini Mestar	x86	32	8	kintex-7-3	James Brakef		32144		6	4	28	73	##	14.7	1.00	2.0	1.1	X		verilog	37	top_sys	Y	yes	Y		4G	4G	Y					2016	2016	http://lmeshoo.ne	gate level dsgn, vivado project also	http://img.youtube.com/vi/2W1guyhCJuE/0.jp
mist1032	https://github.c	errors	Takahiro Ito	RISC	32	32	cyclone-1	James	altera	33251		4	4	138	32	##	q18.0	1.00	1.0	1.0			verilog	100	mist1032isa					4G	4G	Y			64			2015		mist32 uP: inorder version	high pin count
ao486	https://opencor	beta	Aleksander Osman	x86	32	8	cyclone-4	James Brakef		36094		4	4	47	46	##	q13.1	1.00	1.0	1.3	A	Y	system	85	ao486	Y	yes			4G	4G	Y					2014	2014	https://www.stuff	complete 486, SoC configuration	Henry Wong thesis at U.Toronto, also youtube
lemberg	https://github.c	stable	Wolfgang Puffitsch	VLIW	32	32	cyclone-4	James Brakef		37459		4	25	54	43	##	q13.1	1.00	1.0	1.1	A		vhdl	57	core	Y	yes	Y		4G	2M	Y			32	4	2011		http://www2.imm	upto 4 inst/clock	LPM mem & floating point
flexgrip	http://www.ecs	paper	Kevin Andryc	GPGPU	32	32	atrix-7	James Brakef		72649		6	##	119	100	##	14.7	1.00	0.1	11.0	X		vhdl	46	gpgpu_ml505_top_level												2013	2016	http://www.ecs.u	eight GPU processors	requested & received source files

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	repor ter	com ents	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	ven dor	SOC	src code	#src files	top file	doc	tool chai n	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
nyuzi_gpu	https://github.c	stable	Jeff Bush	GPGPU	32	32	cyclone-4	Jeff Bush		74000		4			54		q18.0	16.00	1.0	11.7	AX	Y	system	70	nyuzi	Y	yes	Y		4G	4G	Y	80		64		2015	2024	https://github.cor	32 scalar & 32 vector reg	
nyuzi_gpu	https://github.c	stable	Jeff Bush	GPGPU	32	32	artix7	James	missin	82767	38457	6	64	17	50	##	v23.2	1.00	1.0	0.6	AX	Y	system	70	nyuzi	Y	yes	Y		4G	4G	Y	80		64		2015	2024	https://github.cor	32 scalar & 32 vector reg	should run on either altera or xilinx
thor	https://opencor	mature	Robert Finch	RISC	32	32		Robert Finch		90000				306									verilog		thor	Y	asm	Y		4G	4G	Y			64		2015	2023	https://github.cor	Thor 2015, 2021-3 docs	variable length instructions
riscv_pito	https://github.com/hosse		Hossein Askari	risc-v	32	32	ZCU102	Hosse	includ	201079		6	##	###	250						X		system	31	rv32_core	Y	yes	N		4G	4G	Y			32	8	2020	2022	https://barvinn.re	RISC-V Barrel Processor for Deep Neu	has NN accelerator
fgpu	https://github.c	stable	Muhammed al Kadi	x86	32	32	zynq7045	Muhammed a		128K		6	##	167		##	v17.2				X		vhdl	34	fgpu	Y	yes	Y		4G	4G	Y			32		2016	2017	https://dl.acm.org	eigth cores, reviews comparable proj	vivado fltg-pt IP, benchmarks, wikipedia: GPGP
mimafpga	https://github.c	stable	Manuel Killinger	RISC	24	24	spartan7	James	Brakef	275	288	6			125	##	v23.2	0.80	1.0	363.6	X		vhdl	32	mimaproc	Y		N		1M	1M		19				2019	2021		Minimal Machine processor taught at	has testbench
rois	https://opencor	alpha	James Brakefield	RISC	24	24	kintex-7-3	James	Brakef	382		6		1	120	##	14.7	0.83	1.0	261.7	X		vhdl	2	rois24_24up			N		16M	16M	Y	55		64	1	2016	2017		single pipe stage, pre simulation stag	8, 16 & 24-bit load/store
rois	https://opencor	alpha	James Brakefield	RISC	24	24	kintex-7-3	James	Brakef	384		6		1	170	##	14.7	0.83	1.0	368.8	X		vhdl	2	rois24_24min			N		16M	16M	N	30		64	1	2016	2017		single pipe stage, passes simulation	24-bit word operations only
opc.opc8cpu	https://github.c	beta	revaldinho	RISC	24	24	kintex-7-3	James	no tes	516		6			323	##	14.7	0.80	2.0	250.1	X		verilog	1	opc8cpu	Y	asm	N	N	16M	16M	N	32	4	16		2017	2021	https://revaldinho	OPC8 24bit, based on OPC5LS, more i	see hackaday One Page Computing Challenge
rois	https://opencor	alpha	James Brakefield	forth	24	24	**zu-2e**	James	no blk	627		6			382	##	v19.2	0.83	1.0	507.1	X		vhdl	2	rois24_24min			N		16M	16M	N	30		64	1	2016	2017		single pipe stage, passes simulation	24-bit word operations only
ep24		stable	C.H. Ting	forth	24	6	kintex-7-3	James	substi	1020		6		3	167	##	14.7	0.83	1.0	135.6	X		vhdl	1	ep24	Y	asm	N	N		4K		27				2002	2002		room for 37 additional op-codes	removing stack clear: 503 LUT6 & 143MHz
p24e		beta	C.H. Ting	RISC	24	6	spartan_3	James	Brakef	1175		4		16	51	##	14.7	0.83	1.0	36.0	X		vhdl	1	p24c	Y	asm	N		2K	2K		28				2000			part of eForth?	data width can be expanded
24bit_up	https://github.c	alpha	Harshal Mittal	RISC	24	24	**zu-3e**	James	area o	3535	2166	6	1		187	##	v21.1	0.80	1.0	42.2	X		verilog	17	processor			N		16M	16M	N	17		32		2019	2019		basic 24-bit RISC, course work	big Dff count, multiple writes to register file
rois	https://opencor	alpha	James Brakefield	accum	24	24	**zu-2e**	James	huge !	9000		6			150	##	v19.2	0.83	1.0	13.9	X		vhdl	2	rois24_24up			N		16M	16M	Y	55		64	1	2016	2017		single pipe stage, pre simulation stag	8, 16 & 24-bit load/store
kraken16	https://people.e	stable	Bruce R. Land	RISC	18	18	kintex-7-3	James	Brakef	281		6		1	278	##	14.7	0.67	1.0	662.3	X		verilog	1	DE2_TOP	Y	asm	N	N	256	256	N	22		16			2008	https://people.ec	Cornell course material	
spartanmc	http://www.spa	stable	Falk Hassler	PDP1	18	18	kintex-7-3	James	Brakef	853		6	1	2	120	##	14.7	0.67	1.0	94.6	X	Y	verilog	38	spartanmc	Y	asm										2012	2014		SPARC like register windows	
pdp1	https://opencor	alpha	Yann Vernier	forth	18	18	spartan-3	James	Brakef	1390		4		6	138	##	14.7	0.50	10.0	5.0	X		vhdl	15	top	Y	yes	N	N	4K	4K	Y	28				2011	2017	http://pdp-1.com	PDP-1 descended from MIT TX-0	uses Minimal UART from opencores
chad	https://github.com/bradle		Brad Eckert	forth	18	16	atrix-7-3	James	option	1972		6		3	196	##	v21.1	0.80	1.0	79.5	AXML		verilog	33	mcu	Y	yes	N		64K	64K	N	23		16			2021		verilog, .f &.c code; fpga project files	min SOC, -3 speed grade
chad	https://github.com/bradle		Brad Eckert	forth	18	16	atrix-7-1	James	DFF ex	1982		6		5	127	##	v21.1	0.80	1.0	51.4	AXML		verilog	33	mcu_arty	Y	yes	N		64K	64K	N	23		16			2021		verilog, .f &.c code; fpga project files	max SOC, -1 speed grad
chad	https://github.com/bradle		Brad Eckert	forth	18	16	atrix-7-3	James	DFF ex	1995		6		5	175	##	v21.1	0.80	1.0	70.4	AXML		verilog	33	mcu_arty	Y	yes	N		64K	64K	N	23		16			2021		verilog, .f &.c code; fpga project files	max SOC, -3 speed grade
chad	https://github.com/bradle		Brad Eckert	RISC	18	16	**zu-3e**	James	Brakef	2196	2211	6		5	250	##	v21.1	0.80	1.0	91.1	AXML		verilog	33	mcu_arty	Y	yes	N		64K	64K	N	23		16			2021		verilog, .f &.c code; fpga project files	
yfcpu	https://github.c	errors	Cory Walker	accum	16	16	kintex-7-3	James	degen	18		6				##	14.7	0.67	1.0				verilog	2	yfcpu	Y		N	N	256	256	Y	5	1	16				Colin Mackenzie?	Educational	very simple
hamblen_scon	http://hamblen.	stable	James O. Hamblen	accum	16	16	cyclone-1	James	altera	80		4		1	204	##	q18.0	0.67	2.0	852.7	A		verilog	1	scomp			N	N	256	256	N	4				2008		http://hamblen.ec	from Hamblen 2008 "Rapid prototypi	tiny edu, high IO count
bit-serial	https://github.com/howe		Richard Howe	accum	16	16	spartan6	James	area o	89	66	6			100	##	14.7	0.67	51.0	14.8	X		vhdl	6	cpu	Y		N		2K	2K	N	15				2020	2024	https://hackaday.	bit serial, 16-bit uP, very simple	supports Forth
leros	https://opencor	stable	Martin Schoeberl	accum	16	16	spartan-6	Martin	Schoe	112		6		1	182			0.67	1.0	1089	AX		vhdl	5	leros	Y	yes	N	Y	256	64K				2	2	2008	2020	https://github.cor	256 word data RAM, PIC like	short LUT inst ROM
bit-serial	https://github.com/howe		Richard Howe	reg	16	16	spartan6	James	speed	137	86	6			100	##	14.7	0.67	51.0	9.6	X		vhdl	6	cpu	Y		N		2K	2K	N	15				2020	2024	https://hackaday.	bit serial, 16-bit uP, very simple	supports Forth
Lutiac		custom	David Galloway, David	forth	16	NA	stratix-4	David	Gallow	140		A	4		198			0.67	1.0	947.6	A		vhdl, verilog							64	N	64		32	3		2010	Talks at Un. Toron	synthesis maps PC into ucode	no inst mem: small state machine, ~200 inst o
streamer16	http://www.ultr	stable	Myron Plichota	stack	16	3	kintex-7-3	James	Brakef	143		6			417	##	14.7	0.20	1.2	485.6	X		vhdl	8	streamer	Y	yes	N	N	64K	64K	N	8	2			2001	2001	http://www3.sym	MIPS/inst reduced	2nd web adr non-functional
minicpu-s	https://github.c	stable	Michael Morris	RISC	16	8	kintex-7-3	James	Brakef	147		6			741	##	14.7	0.67	28.0	120.6	X		verilog	2	both	Y		N					33				2012	2013		separate source for each CPLD chip, u	fits (2) XC9500 CPLD @ 71.4 MHz
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	accum	16	16	**zu-3e**	James	multi-c	165	96	6			250	##	v21.1	0.67	1.0	1015	X		verilog	7	cpu02	Y		N	N	0	0	N	23		4		2019	2019		multi-driven nets	multi cycle CPU that has an IPC of 1
pumpkin	https://github.com/Steve		Steve Teal	RISC	16	16	**zu-3e**	James	Brakef	166	67	6			625	##	v21.2	0.67	2.0	1261			vhdl	6	hello_wor	Y	asm	N		4K	4K		14				2020			scalable, 16-bit, 16 instruction soft CP	LUT RAM inferred (small size)
verilog-harvard	https://github.com/jaywo		Jae-Won Chung	accum	16	16	kintex-7-3	James	multi-c	171		6			357	##	v21.1	0.67	1.0	1399	X		verilog	5	cpu01	Y		N	N	4K	4K	N	23		4		2019	2019		multi-driven nets	single cycle CPU that has an IPC of 1
opc.opc3cpu	https://github.c	stable	revaldinho	risc	16	16	kintex-7-3	James	reduce	174		6			526	##	14.7	0.30	4.0	226.9	X		verilog	2	opc3cpu	Y	asm	N	N	64K	64K	N	13	3			2017	2021	https://revaldinho	OPC3 16-bit OPC1, for XC95144 CPLD	see hackaday One Page Computing Challenge
mini16_cpu	https://github.com/miya4		miya	accum	16	16	kintexus	miya		186		6	1		710			0.67	1.0	2558	X		verilog	13	top										7		2024			Very small and high performance CPU	data width can be expanded
hamblen_scon	http://hamblen.	stable	James O. Hamblen	accum	16	16	cyclone-1	James	altera	196		4		1	166	##	q18.0	0.67	2.0	283.5	A		verilog	2	DE2_TOP			N	N	256	256	N	4				2008		http://hamblen.ec	from Hamblen 2008 "Rapid prototypi	tiny edu, high IO count
misc16	https://github.com/Steve		Steve Teal	accum	16	16	**zu-3e**	James	Brakef	197	78	6			500	##	v21.2	0.22	1.0	558.4	X	B	vhdl	1	misc	Y	yes	N		64K	64K	N	10				2021		https://github.cor	16-bit minimal CPU, has a single instruction 'mov' & eforth	
micro16b	http://members	beta	John Kent	accum	16	16	kintex-7-3	James	Brakef	205		6			434	##	14.7	0.33	2.0	349.0	X		vhdl	1	u16bcpu	Y	asm	N	N	64K	4K	Y	8				2002	2008	http://members.c	very limited inst set	MIPS/clk adj'd, 2 clks/inst
ncore	https://opencor	alpha	Stefan Istvan	accum	16	8	kintex-7-3	James	Brakef	223		6			105	##	14.7	0.67	1.0	316.3	X		verilog	3	nCore	Y		N		128K	64K		16		16		2006	2018		This is a little-little processor core	
bit-serial	https://github.com/howe		Richard Howe	accum	16	16	spartan6	James	area o	226	181	6		8	100	##	14.7	0.67	51.0	5.8	X		vhdl	6	top	Y		N		2K	2K	N	15				2020	2024	https://hackaday.	bit serial, 16-bit uP, very simple	supports Forth
pumpkin	https://github.com/Steve		Steve Teal	risc	16	16	**zu-3e**	James	Brakef	230	131	6		1	450	##	v21.2	0.67	2.0	656.1			vhdl	6	myco	Y	asm	N		4K	4K		14				2020			scalable, 16-bit, 16 instruction soft CP	emulates Myco, forced block RAM
troc16_16	https://github.c	WIP	James Brakefield	forth	16	16	spartan7	James	Brakef	232	50	6	1	1	74	##	v24.2	0.67	1.0	212.8	X		vhdl	5	troc16_16	Y		N		64K	64K	N	25	2	32			2025	https://events.vto	adequate 16-bit uP with op-code space	for full TROC ISA; no shift, extract or divide at
J1	www.excamera	stable	James Bowman	accum	16	16	**zu-2e**	James	area o	253		6		1	336	##	v20.1	0.80	1.0	1061	X		vhdl	1	j1	Y	forth	N		64K	64K		20			2	2006	2023	https://github.cor	uCode inst, dual port block RAM	16 deep data & return stacks
hack	https://github.com/wuha		Wu Han	RISC	16	16		Wu Han		267	152	4		4		##		0.67	2.0		L		verilog	22	hack	Y	asm	N	Y	32K	32K	N	18		2			2020	https://www.nand	CPU used to run Tetris	book: Elements of Computing Systems
xr16	https://github.c	stable	Jan Gray	RISC	16	16	kintex-7-3	James	Brakef	273		6			263	##	14.7	0.67	1.0	644.8	X		verilog	4	xr16	Y		N		64K	64K				16		1999	2001	https://github.cor	handcrafted instruction set	tool FPGA P&R, speed mode better
opc.opc5cpu	https://github.c	stable	revaldinho	risc	16	16	kintex-7-3	James	reduce	273		6			294	##	14.7	0.40	3.0	143.6	X		verilog	7	opc5cpu	Y	asm	N	N	64K	64K	N	15	4	16		2017	2021	https://revaldinho	OPC5 RR inst, ISA similar to OPC1	see hackaday One Page Computing Challenge
drv16	https://github.com/jecelj		Jecel de Assumpção	risc	16	16	gowin	Jecel de Assu		282	33	4			95	##		0.67	2.0	112.9	AGLX		schem	8	drv16.v	Y		N		64K	64K				16			2024	https://www.mdp	educational, LUT count comparisons	Digital schematic, RISC-V 16-bit ISA
troc16_16	https://github.c	WIP	James Brakefield	RISC	16	16	spartan7	James	area o	285	50	6	1	1	71	##	v24.2	0.67	1.0	167.9	X		vhdl	5	troc16_16	Y		N		64K	64K	N	25	2	32			2025	https://events.vto	adequate 16-bit uP with op-code spac	half word aligned, 4 tag bits, signed mult
alwcpu	https://opencor	alpha	Andreas Hilvarsson	forth	16	16	kintex-7-3	James	Brakef	298	78	6			194	##	14.7	0.67	1.0	437.1	ALX		vhdl	7	top	some		N	N	64K	64K	Y			8		2009	2010		lightweight CPU	minimal features, **uses generics for configur**
msl16		beta	Philip Leong, Tsang, Le	accum	16	4	kintex-7-3	James	Brakef	303		6			256	##	14.7	0.67	1.0	566.4	X		vhdl	13	cpu	Y	asm	N		256			16				2001			CPLD prototype	
c3pu	https://github.com/isovic		Ivan Sovic	x86	16	16	kintex7	James	no los	303	234	6			250	##	14.7	0.67	3.0	184.3	X		vhdl	17	Cpu_black	Y	asm	N		64K	64K		22		8		2013	2015		large state enumeration	uses internal tri-states
mcl86	https://github.c	stable	Ted Fried	RISC	16	8	kintex-7-3	Ted Fried		308		6		4	180			0.67	20.0	19.6	X		verilog	3	EU	Y	yes	N	N	1M	1M	Y					2016	2021	http://www.embe	**microcoded, meets original 8088 timing@100MHz**	
iDEA	https://github.c	alpha	Hui Yan Cheah etal	accum	16	32	virtex-6	Liu Ch	unable	321		6	1	2	405		13.2	0.67	1.0	845.3	X		verilog	22	cpu_top	Y	yes	N	Y	64K	64K	N	24		32	9	2011	2016	The iDEA DSP Blo	uses DSP slice in barrel mode for ALU	from GitHub, rq'd NOPs lower actual results
bit-serial	https://github.com/howe		Richard Howe	6502	16	16	spartan6	James	Brakef	324	210	6		8	100	##	14.7	0.67	51.0	4.1	X		vhdl	6	top	Y		N		2K	2K	N	15				2020	2024	https://hackaday.	bit serial, 16-bit uP, very simple	supports Forth
verilog-65C02	https://github.c	alpha	Arlet Ottens	DSP	16	8	**zu-3e**	James	Brakef	327	98	6			370	##	v21.1	0.33	3.0	124.6	X		verilog	26	cpu		yes	N	N	64K	64K	Y					2011	2021	https://github.cor	used in 100MHZ 6502 DIP module	rewritten for 6LUTs, spartan6 version has blac
dspuva16	http://www.DTE	stable	Santiago de Pablo	accum	16	16	kintex-7-3	James	Brakef	332		6			317	##	14.7	0.67	1.0	640.7	X		verilog	1	dspuva16		asm	N	Y	256	4K		40		16		2001	2004	www.1-core.com/	16 bit data memory, 24 bit regs	broken web link
mano-computer	https://github.com/Amin/		Amin Aliari	RISC	16	16	spartan7	James	multi-c	332	60	6			71	##	v23.2	0.67	1.0	144.1			vhdl	19	sayeh	Y		N		4K	4K	N	25				2020		https://en.wikiped	Mano uP implementation, course pro	different use of sayeh: *simple & yet enough*
limen	https://github.com/domir		Dominik Salvet	forth	16	16	spartan7	James	Brakef	333	63	6		1	250	##	v23.2	0.67	1.0	503.0	X		vhdl	12	limen_sys	Y		N	Y	256	256	N	24		8		2018	2023	https://github.cor	highschool thesis in Czech	limen_alpha is dual core version
J1	www.excamera	stable	James Bowman	RISC	16	16	kintex-7-3	James	Brakef	335		6		1	180	##	14.7	0.80	1.0	431.0	X		vhdl	1	j1	Y	forth	N		64K	64K		20			2	2006	2023	https://github.cor	uCode inst, dual port block RAM	16 deep data & return stacks
xr16	https://github.c	stable	Jan Gray	forth	16	16	**zu-2e**	James	needs	346		6			282	##	v20.1	0.67	1.0	547.0	X		verilog	4	xr16	Y		N		64K	64K				16		1999	2001		handcrafted instruction set	tool FPGA P&R, speed mode better
cpu16	http://www.ultr	stable	C.H. Ting	RISC	16	5	kintex-7-3	James	Brakef	347		6			364	##	14.7	0.67	1.0	702.1	X		vhdl	1	cpu16			N	N	64K	64K	N	28				2000	2000		P16 in VHDL	CPU24.vhd with width=16
risc_core_i	https://opencor	planning	Manuel Imhof	RISC	16	16	kintex-7-3	James	Brakef	349		6	1		526	##	14.7	0.67	3.0	336.8	X	B	vhdl	13	CPU	Y	asm	N		1K	1K				8	4	2001	2009		Havard arch, thesis project	derived clocks: estimated derating
fpga4_mips16	http://www.fpg	stable	Van Loi Le	RISC	16	16	kintex-7-3	James	Brakef	352		6			213	##	14.7	0.67	1.0	405.0	X		vhdl	8	mips_vhdl			N		65K	65K		8		8		2017	2017		educational, no block RAM inferred	actual prog sz=16, actual data mem sz=256
xucpu	https://opencor	alpha	Jurgen Defurne	accum	16	16	spartan6	James	Brakef	356		6		4	187	##	14.7	1.00	1.0	524.8	X	Y	vhdl	25	system_4k					4K	4K						2015	2017		Experimental Unstable CPU	
mano_machine	https://github.c	stable	Susam Pal	forth	16	16	kintex-7-3	James	needs	364		6				##	14.7	0.67	2.0				vhdl	5	microprod	Y		N		4K	4K	N	25				2005	2016	https://en.wikiped	course project, bidir mem data	for XC9572 CPLD, large # of latches
p16b		beta	C.H. Ting	RISC	16	5	kintex-7-3	James	case c	367		6			355	##	14.7	0.67	1.0	648.1	X		vhdl	1	cpu16	Y	asm	N		64K	64K		28				2000			part of eForth?	data width can be expanded
fpga4_mips16	http://www.fpg	stable	Van Loi Le	RISC	16	16	kintex-7-3	James	Brakef	369		6			200	##	14.7	0.67	1.0	363.1	X		verilog	8	mips_16		yes	N		65K	65K		13		8		2017	2017		educational, no block RAM inferred	same prog & data mem and alu as mips16_16_
xsoc	http://www.fpg	stable	Jan Gray	RISC	16	16	kintex-7-3	James	very sl	371		6				##	14.7	0.67	1.0		X		verilog	16	xsoc	Y	yes	N	N	64K	64K	Y	16	4	16		2000	2001	https://github.cor	very compact, bare core	similar to xr16
alwcpu	https://opencor	alpha	Andreas Hilvarsson	RISC	16	16	kintex-7-3	James	Brakef	377	77	6			194	##	14.7	0.67	1.0	345.5	ALX		vhdl	7	top	some		N	N	64K	64K	Y			16		2009	2010		lightweight CPU	maximal features (additional inst)
opc.opc5lscpu	https://github.c	stable	revaldinho	MSP430	16	16	kintex-7-3	James	Brakef	383		6			247	##	14.7	0.67	3.0	144.0	X		verilog	2	opc5lscpu	Y	asm	N	N	64K	64K	N	18	4	16		2017	2021	https://revaldinho	OPC5LS OPC5 with predicate inst	see hackaday One Page Computing Challenge
neo430	https://opencor	alpha	Stephan Nolting	stack	16	16	virtex-6	Stephan	Nolt	402		6		2	204	##	14.7	0.67	4.0	85.0	ALX	Y	vhdl	19	neo430_te	Y	yes	N		28K	32K	Y			16		2015	2021	https://github.cor	website has detailed resource utiliza	minimal configuration
minicpu	http://www.cs.h	stable	Hirotsugu Nakano	stack	16	5	kintex-7-3	James	lots of	433		6	1	1	128	##	14.7	0.33	1.0	97.7	X		verilog	7	minicpu	Y	yes	N		4K	4K	N	26				2008	2018		same as tiny-cpu	uses Flex, Bison & Perl to create gcc compiler
pancake	https://people.e	stable	Bruce Land	MSP430	16	5	kintex-7-3	James	bypass	441		6	1	1	128	##	14.7	0.67	1.0	194.8	X		verilog	7	de2_minic	Y	yes	N		4K	4K		31				2010	2014	http://www.cs.hit	The Pancake Stack Machine dervied f	Cornell ECE5760
s430	https://www.p-c	stable	Paul Taylor	RISC	16	16	artix-7	Paul Taylor		449		6			100			0.67	9.0	16.6			vhdl	1	s430					64K	64K	Y					2019	2019		msp430 subset with 8-bit alu	coded for size & not for speed
opc.opc6cpu	https://github.c	stable	revaldinho	risc	16	16	kintex-7-3	James	Brakef	450		6			222	##	14.7	0.67	2.0	165.4	X		verilog	2	opc6cpu	Y	asm	N	N	64K	64K	N	27	4	16		2017	2021	https://revaldinho	OPC6 based on OPC5LS, more inst	see hackaday One Page Computing Challenge
cpu-16-bit	https://github.com/Vedar		Vedang Asgaonkar	RISC	16	16	spartan7	James	8 latch	468	195	6			147	##	v23.2	0.67	3.0	70.2	X		vhdl	5	cpu	Y		N		64K	64K	N	17		8			2022		ld/st multiple & predication insts	trimming of inst reg
sayeh_process	https://opencor	stable	Alireza Haghdoost, Arr	accum	16	8	kintex-7-3	James	Brakef	479		6	1		164	##	14.7	0.67	1.0	229.7	X		verilog	13	Sayeh	Y		N		64K	64K				32		2008	2009	haghdoost.persian	gig.com	simple RISC
lem16_18		alpha	James Brakefield	risc	16	18	kintex-7-3	James	Brakef	483		6		1	294	##	14.5	0.16	1.0	97.4	X		vhdl	2	lem16_18m			N		256	1K		77			1	2010	2018		variable bit-length memory read/writ	op-codes coded, untested
ippro	https://github.com/fsiddi		Fahad Siddiqui	reg	16	32	virtex-7	Fahad	Siddiqu	484	447	6	1	1	372	##		0.80	1.0	614.9	X		verilog	31				asm	N	64K	64K		30		32	5	2013	2023		16-bit RISC using DSP48	image processing, several publications
octavo	http://fpgacpu.g	beta	Charles LaForest	RISC	16	16	stratix-4	Charles	LaFor	500		A	1		550			0.67	1.0	737.0	A		verilog	18	Octavo	Y	asm	N					14		16	10	2012	2019	https://github.cor	8 core barrel, adjustable data width	~= performance across word sizes, no call/rtn i
c16too	https://www.sc	stable	Cole Design and Devel	forth	16	16	kintex-7-3	James	Brakef	510		6			271	##	14.7	0.67	4.0	88.9	X		vhdl	1	core	Y	asm	N		64K	64K	N	20		8		2003		coledd.com/electr	graphics capability	clock/2 and six phases
s16x4a	https://github.c	stable	Samuel Falvo II	forth	16	4	kintex-7-3	James	Brakef	514		6			476	##	14.7	0.67	1.0	620.7	X	B	verilog	1	s16x4a	Y		N	N	64K	64K	Y	12				2012	2017		kestrel #2, byte & word data	derived from Myron Plichota's design (streame
J1a	www.excamera	stable	James Bowman	forth	16	16	kintex-7-3	James	DFF ex	518		6			412	##	14.7	0.80	1.0	636.1	X		verilog	3	j1	Y	forth	N		64K	64K		20			2	2006	2023	https://github.cor	uCode inst, dual port block RAM	DFF used for 18 deep data & return stacks
b16	www.bernd-pay	stable	Bernd Paysan	RISC	16	5	spartan-6	James	Brakef	554		6			134	##	14.7	0.67	1.0	161.7	AX		verilog	15	b16	Y	yes	N		64K	64K	N					2002	2017	https://github.cor	two versions: one/15 source files,	derived from c18
cole_c16	https://www.sc	beta	Cole Design & Develop	RISC	16	16	spartan-6	James	Brakef	554		6			298	##	14.7	0.67	7.0	51.4	X		vhdl	1	core	Y	asm	N		64K	64K	N	20		8		2002	2012	https://blog.classy	(7) clks per inst, complete SOC	

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data	sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	toolchai	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
atlas_core	https://opencor	beta	Stephan Nolting	MSP430	16	16		kintex-7-3	James Brakef		559	269	6	1		200	##	v14.1	0.80	1.0	286.2	AX		vhdl	8	ATLAS_CP	Y	asm	N	Y	64K	64K	Y	80		8		2013	2015	https://www.allat	ARM thumb like inst set	non-MMU version
neo430	https://opencor	alpha	Stephan Nolting	accum	16	16		artiix-7	Stephan Nolt		576	266	6		1	100	##	v19.2	0.67	4.0	29.1	ALX	Y	vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2024	https://github.cor	edit neo430_sysconfig.vhd to set opti	minimal configuration
c3pu	https://github.com/isovic		Ivan Sovic	CISC	16	16		spartan3	Ivan Sovic		580	268	4					14.6	0.67	3.0		X		vhdl	17	mc3pu	Y	asm	N		64K	64K		22		8		2013	2015		Spartan3: 268FF, 580 4LUT; 22 inst, 8 reg, 3clks/inst, 65K wds, asm	
raptor16	www.spacewire	stable	Steve Haywood	MSP430	16	16		kintex-7-3	James Brakef		590		6			319	##	14.7	1.40	2.7	280.2	X		vhdl	1	raptor16	Y	yes	N	N	64K	64K	N					2004			8 data & 8 adr regs	no multiply, 8 adr modes
neo430	https://opencor	alpha	Stephan Nolting	6502	16	16		cyclone4	Stephan Nolt		590	230	4		6	122	##	q17.1	0.67	4.0	34.6	ALX	Y	vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2024	https://github.cor	**website has detailed resource unt**	minimal configuration
verilog-65C02	https://github.c	alpha	Arlet Ottens	RISC	16	8		kintex-7-3	James	remov	599		6		2	204	##	14.7	0.67	4.0	57.1			verilog	5	gop16		yes	N	N	4G	4G						2011	2018	http://forum.6502	16-bit data RAM "bytes"	boot ROM mapped to LUTs?
atlas_core	https://opencor	beta	Stephan Nolting	forth	16	16		**zu-3e**	James Brakef		611	285	6	1		333	##	v21.1	0.80	1.0	436.4	AX		vhdl	8	ATLAS_CP	Y	asm	N	Y	64K	64K	Y	80		8		2013	2015		ARM thumb like inst set	non-MMU version
yafc	https://github.c	alpha	Tim Wawrzynczak	forth	16			kintex-7-3	James Brakef		617		6		4	247	##	14.7	0.67	1.0	268.5	X		vhdl	20	cpu		asm	N	Y	8K	8K		26				2014				influenced by J1, F16 & C18
cd16	http://anycpu.o	stable	Brad Eckert	RISC	16	16		spartan-3	James Brakef		618		4		7	31	##	14.7	0.67	2.0	16.9	AX	Y	vhdl	16	demosocext			N		128K	8M						2003	2003	http://web.archiv	Spartan-3 block RAM	includes stack RAMs & some inst RAM
yasep	https://hackada	alpha	Yann Guidon	RISC	16	32		kintex-7-3	James	reduce	632		6			215	##	I14.7	1.00	2.0	170.0	AX		vhdl	3	microYAE	Y	asm	N	N	2G	2G		51		16		2005	2018	www.youtube.cor	JavaScript generated VHDL, revisions ongoing	
tigli_cpu		stable	Cleiton Juffo	RISC	16	16		kintex-7-3	James Brakef		636		6			455	##	14.7	0.67	4.0	119.7	X		verilog	24	cpu	Y		N	Y	64K	64K		16		16		2013	2013		course project, not pipelined	no LUT RAM for reg file
table887	https://github.c	alpha	Robert Finch	RISC	16	16		kintex-7-3	James Brakef		643		6		2	208	##	14.7	0.67	1.0	217.1	X		verilog	2	table887_	Y		N	N	64K	64K		28		8		2014	2016			included with Table888 source code
dcpu16	https://github.c	beta	Shawn Tan, Marcus Pe	forth	16	16		kintex-7-3	James Brakef		662		6	1		318	##	14.7	0.67	4.0	80.4	X		vhdl, v	5	dcpu16_c	Y	asm	N	N	64K	64K	N	37		8		2009	2012	https://en.wikiped	for the 0X10c game	4+ addressing modes, 4 & 5-bit reg /modefield
cd16	http://anycpu.o	stable	Brad Eckert	mips	16	16		spartan-3	James Brakef		681		4			83	##	14.7	0.67	2.0	41.0	AX	B	vhdl	16	cd16			N		128K	8M						2003	2003	http://web.archiv	Spartan-3 block RAM	bare core
digital_up	https://github.com/hneer		Helmut Neemann	accum	16	16		zu-5e	James	clockir	709	310	6	1		250	##	v22.1	0.67	1.0	236.2	X		schem	46	processorHD		asm	N	Y	64K	64K		60		16		2016	2022	https://github.cor	uP implemented as schematic	has assembler and ISA pdf, 2Kx16 RAM?
t180-cpu		stable	Leonard Brandwein	mips	16	8		kintex-7-3	James	bypass	709		6			83	##	14.7	0.67	3.0	26.2	X		vhdl	23	cpu	Y		N	N	64K	64K	Y	182				2016	2016	https://www.vtto	8-bitter with pc, sp, a, b, c & d regs	based on Viktor Toth's 4 bit microcontroller
digital_up	https://github.com/hneer		Helmut Neemann	forth	16	16		spartan-7	James	clockir	716	309	6	1		182	##	v22.1	0.67	1.0	170.1	X		schem	46	processorHD		asm	N	Y	64K	64K		60		16		2016	2022	https://github.cor	uP implemented as schematic	has assembler and ISA pdf, 2Kx16 RAM?
kestrel-2	kestrelcompute	stable	Samuel Falvo II	RISC	16	16		kintex-7-3	James Brakef		735		6		8	172	##	14.7	0.67	1.0	157.2	X	Y	verilog	27	M_kestrel	Y	yes	N		64K	64K		20			2	2012	2015	https://hackaday.i	J1 with wishbone bus	M_j1a runs at 244MHz & 368 LUTs
c-nit	http://www.c-n	stable	Sumit	RISC	16	16		spartan-3	James	xilinx l	752		4		3	100	##	14.7	0.67	2.0	44.5	X		verilog	6	soc	bm	asm	N	N	64K	64K	Y	22		15		2003	2004		RISC with several load/store modes	
moncky	https://gitlab.com/big-bat	stable	Kris Demuynck	RISC	16	16		**zu-3e**	James	no me	768	280	6			250	##	v21.1	0.67	1.0	218.1	X	X	schem	36	Moncky3	Y	yes	N		64K	64K	N	32		16		2020	2021	https://hackaday.i	bare CPU	also has verilog
dgb16	see FISA64	stable	Robert Finch	forth	16	16		kintex-7-3	James Brakef		780		6			313	##	14.7	0.67	1.0	269.0	X		verilog	1	dbg16	Y		N	Y						8					https://github.cor	inside FISA64 project	debug uP for fisa64
forth-cpu	https://anycpu.org/forum		Richard Howe	RISC	16	16		spartan3	James Brakef		782	91	4	1	2	90	##	14.7	0.67	1.0	77.5	X		vhdl	10	cpu			N									2013	2024	http://www.aholn	forth uP for GPS reciever, 32-bit stack	Spartan3 block RAM & multiplier
diogenes	https://opencor	beta	Fekknhifer	TTA	16	16		kintex-7-3	James Brakef		807		6		1	297	##	14.7	0.67	1.0	246.3	X		vhdl	11	cpu	Y	asm	N				1K					2008	2009		"student RISC system"	
uTTA		stable	Hans Tiggeler	forth	16	16		kintex-7-3	James Brakef		810		6	1		57	##	14.7	0.67	1.0	47.4	X		vhdl	23	utta_struc	N	asm	N											http://www.ht-lab	time triggered arch	bad weblink
ep16	https://github.c	beta	C.H. Ting	RISC	16	5		kintex-7-3	James Brakef		837		6			254	##	14.7	0.67	1.0	203.6	X		vhdl	5	ep16	Y	yes	N	N	32K	32K	N	32				2005	2012	PDF files	initialized Lattice memory blocks	5-bit instructions
hpc-16	https://opencor	beta	Umair Siddiqui	PIC18	16	16		kintex-7-3	James Brakef		871		6			152	##	14.7	0.67	1.0	116.6	X		vhdl	20	cpu	Y	asm	N		64K	64K				16		2005	2015			
mcip_open	https://opencor	beta	Mezzah Jbrahim	RISC	16	24		kintex-7-3	James Brakef		881		6	1		200	##	14.7	0.67	1.0	152.1	X		vhdl	23	MCIOopen_r	yes		N	Y	4K	1M	Y					2014	2015		light version of PIC18	
ejrh_cpu	https://github.c	stable	Edmund Horner	accum	16	16		kintex-7-3	James Brakef		928		6	1	2	196	##	14.7	0.67	1.0	141.6	X		verilog	17	machine	Y									16		2015	2015		see web archive for doc	
EC16_on_ICE	https://github.com/Edgar		Edgar Conzen	MSP430	16	16		ice40	Edgar Conzer		940	257	4		1	20		r23.1	0.67	2.0	7.1	L	Y	vhdl	54	ec16_top	Y		N		64K	64K		50				2023	2024		designed FPGA board, Lattice Radiant	
neo430	https://opencor	alpha	Stephan Nolting	forth	16	16		artiix-7	James	chang	947	659	6		2.5	215	##	14.7	0.67	4.0	38.0	ALX	Y	vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2024	https://github.cor	edit neo430_sysconfig.vhd to set options	
mecrisp-ice	https://sourceforge.net/p		Matthias Koch	accum	16	16		spartan7	James Brakef		990	1180	6	1	4	100	##	v23.2	0.67	2.0	33.8	LX	Y	verilog	42	j1a	Y	forth	N		64K	64K	Y					2011	2023		16-bit data size, some comments in G	distinct j1a.v for each data size
blue	https://opencor	stable	Al Williams	MSP430	16	16		spartan-3	James	remov	1025		4			63	##	14.7	0.67	1.0	41.1	X	Y	verilog	16	topbox	Y		N		4K	4K	N	18		2		2009	2010		derived from Caxton Foster's Blue	http://www.youtube.com/watch?v=dt4zezZP8
neo430	https://opencor	alpha	Stephan Nolting	eSi-1600	16	16		artiix-7	Stephan Nolt		1036	1144	6		2.5	100	##	v19.2	0.67	4.0	16.2	ALX	Y	vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2024	https://github.cor	edit neo430_sysconfig.vhd to set opti	distinct j1a.v for each data size
ensilica	http://www.ens	proprietar	ensilica.com	eSi-1600	16	16		virtex-5	ensilica		1100		6			160			1.00	1.0	145.5	AX		verilog		eSi-1600	Y	yes			64K	64K	Y	92	10	16	5	2001	2016		verilog source included with license	room for 90 user inst, also as ASIC
ensilica	http://www.ens	proprietar	ensilica.com	forth	16	16		virtex-5	ensilica		1100		6			160			1.00	1.0	145.5	AX		verilog		eSi-1650	Y	yes			64K	64K	Y	92	10	16	5	2001	2016		verilog source included with license	room for 90 user inst, also as ASIC
microcore	http://www.pld	beta	Klaus Schleisiek	MSP430	16	8		kintex-7-3	James Brakef		1101	138	6			171	##	14.7	0.67	1.0	104.1	X		vhdl	17	ucore120	Y	asm	N	Y	4K	4K						1999	2023		indexing into return stack, auto inc/d	no block RAM?, uses tri-state signals
openmsp430	https://opencor	stable	Oliver Girard	RISC	16	16		stratix-3	Oliver Girard		1147			A	1	98			0.67	2.0	28.5	AX		verilog	30	openMSP	Y	yes	N	N	64K	64K	Y			16		2009	2018		near cycle accurate	performance spreadsheet
moncky	https://gitlab.com/big-bat		Kris Demuynck	RISC	16	16		**zu-3e**	James	clock c	1196	523	6		33	78	##	v21.1	0.67	1.0	43.8	X	X	schem	36	top	Y	yes	N		64K	64K	N	32		16		2020	2021	https://hackaday.i	from 16x65K to 64KB RAM	two phase clock, ALU & mem have own phase
atlas_2K	https://opencor	beta	Stephan Nolting	9900	16	16		**zu-3e**	James	40 LUT	1222	1160	6	1	4.5	262	##	v21.1	0.80	1.0	171.4	ALX		vhdl	19	ATLAS_2K	Y	asm	N	Y	64K	64K	M	80		8		2013	2015		ARM thumb like inst set	has MMU & full SOC features
ep994a	https://github.c	stable	Erik Piehl	RISC	16	16		kintex-7-3	James Brakef		1340		6		5	286	##	14.7	0.83	3.0	59.0	X		vhdl	10	ep994a	Y	yes	N	N	64K	64K	Y			16		2016	2019	https://hackaday.i	TI 990 emulation	also tms9902 (uart) core by Paul Urbanus?
basic-simd-up	https://github.c	stable	Tingyuan Liang	RISC	16	18		**spartan7**	James Brakef		1369	259	6			71	##	v23.2	0.75	1.0	39.1			verilog	5	cputop	Y		N	Y	1K	1K		47		8		2018	2022		compiled via Cadence to ASIC layout	simple SIMD processor in Verilog
moncky	https://gitlab.com/big-bat		Kris Demuynck	RISC	16	16		artix-7	Kris Demuync		1376		6		33	10	##	v21	0.67	1.0	4.9	X	X	schem	36	top	Y	yes	N		64K	64K	N	32		16		2020	2021	https://hackaday.i	intended as educational, all original	IO: VGA, PS/2, SPI, SD
multicycle_risc	https://github.c	stable	Yash Sanjay Bhalgat	RISC	16	16		kintex-7-3	James Brakef		1470		6			213	##	14.7	0.67	1.0	97.0	X		verilog	62	risc15	Y		N		64K	64K		15		8		2015	2015		multi-cycle IIT-B-RISC15 ISA	developed on Altera, course project
a2z	https://hackada	stable		RISC	16	24		cyclone-4	James Brakef		1524		4	1	12	62	##	q17.0	0.67	1.0	27.4	A		verilog		top_a2z												2016	2018			
atlas_2K	https://opencor	beta	Stephan Nolting	DSP	16	16		kintex-7-3	James	48 LUT	1595	1108	6	1	4.5	151	##	14.7	0.80	1.0	75.9	ALX		vhdl	19	ATLAS_2K	Y	asm	N	Y	64K	64K	M	80		8		2013	2015	https://www.allat	ARM thumb like inst set	has MMU & full SOC features
bobcat		beta	Stan Drey	MSP430	16	24		kintex-7-3	James Brakef		1622		6	1		107	##	14.7	0.67	1.0	44.0	X		vhdl	30	bobcat_co	Y		N		64K	64K						1998	2000		dead web links	
msp430_vhdl	https://opencor	beta	Peter Szabo	x86	16	16		kintex-7-3	James Brakef		1735		6			127	##	14.7	0.67	2.0	24.5	AX		vhdl	9	cpu	Y	yes	N		64K	64K	Y			16		2014	2017		Comprehensive verification was not	compiles on cyclone II
s80186	https://github.c	stable	Jamie Iles	accum	16	8		cyclone-V	Jamie Iles		1750		A			60			0.67	2.0	11.5	A	Y	system	50	core	Y		N		1M	1M	Y					2017	2021	https://www.jami	80186 binary compatible core	implementing the full 80186 ISA
c16	https://opencor	stable	Jsauermann	RISC	16	8		spartan-3	James Brakef		1751		4		16	57	##	14.7	0.33	1.0	10.7	X		vhdl	22	Board_cpu	mi	yes	N		64K	64K	Y			5		2003	2012		8080 derivative, optional UART, 8-bit	xilinx 4K RAM primitives
dme	https://github.c	stable	ErwinM	PDP11	16	16		kintex-7-3	James Brakef		1755		6			53	##	14.7	0.67	1.0	20.4	X		verilog	49	cpu	Y	yes	N		64K	64K	Y	40		8		2016	2017		based on magic-16	computer & computer2 null dsgns: no outputs
w11	https://github.c	alpha	Walter Mueller	RISC	16	16		kintex-7-3	James Brakef		1760		6	1	1	147	##	14.7	0.67	2.0	28.0	X	Y	vhdl	118	pdp11_co	Y	yes	N	N	4M	4M	Y	70	13	8		2010	2023	https://github.cor	Boots UNIX, has MMU & cache, retro	PDP-11/70 CPU core and SoC
marca	https://opencor	stable	Wolfgang Puffitsch	MSP430	16	16		arria-2	James Brakef		1763		A		22	157	##	q13.1	0.67	6.0	10.0	A		vhdl	40	marca	Y		N		8K	16K		75		16	4	2007	2009		serial multiply & divide	clks/inst is approx
neo430	https://opencor	stable	Stephan Nolting	forth	16	16		ice40	Stephan Nolt		1812	755	4		6	20	##	LR	0.67	4.0	1.9	ALX	Y	vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2024	https://github.cor	website has detailed resource unti	minimal configuration
forth-cpu/h2	https://opencor	stable	Richard Howe	MSP430	16	16		kintex-7-3	James Brakef		1858		6		9	149	##	14.7	0.67	1.0	53.8	X	Y	vhdl	11	top	Y		N		64K	64K		25				2017	2020	https://github.cor	H2 Forth SoC, VHDL reads *.hex & *.b	derived from J1, hex & bin files in 2/16/2018 ta
neo430	https://opencor	alpha	Stephan Nolting	68000	16	16		cyclone4	Stephan Nolt		1869	1137	4		8	121	##	q17.1	0.67	4.0	10.8	ALX	Y	vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2024	https://github.cor	website has detailed resource unti	default config, includes true RNG
j68	https://github.com/fredre		Frédéric Requin	x86	16	16		cyclone3	Frédéric Requ		1900		4		9	90			1.00	6.0	7.9			verilog	38	soc_j68		yes	N	N	64K	64K	Y			16			2018		A Size-Optimized Microcoded 68000 (	Stack based CPU with Forth-like microcode	
sub86	https://opencor	alpha	Jose Rissetto	x86	16	8		kintex-7-3	James Brakef		1916		6			172	##	14.7	0.67	3.0	20.1	X		verilog	1	sub86	Y	yes	N	N	64K	64K	Y			7		2012	2013		very small x86 subset core	no segment registers, limited op-codes
next186	https://opencor	stable	Nicolae Dumitrache	forth	16	8		arria-2	James Brakef		1966		A	2		77	##	q13.1	0.67	2.0	13.1	AX		verilog	4	Next186_	Y	yes	N	N	1M	1M	Y					2012	2013		boots DOS	
microcore	https://github.c	beta	Klaus Schleisiek	forth	16	8		XP2	Klaus Schleisi		1976		4			33	##	3.12	0.67	1.0	11.2	AILX		vhdl	38	ucore	Y	asm	N	Y	4K	8K	Y	84				1999	2023		**easy to add op-codes, fltg-pt opt., sir**	**12, 16, 27 & 32 bit data sizes**
jop	https://opencor	stable	Martin Schoeberl etal	DSP	16	16		cyclone-1	Martin Schoe		2000		4			100		q10.0	0.67	1.0	33.5	A		vhdl	11	core	Y	yes	N		256K	256K						2004	2014		https://github.com/jop-devel/jop	java app builds some source code files
oc54x	https://opencor	beta	Richard Herveille	68000	16	16		kintex-7-3	James Brakef		2225		6	1		180	##	14.7	0.67	1.0	54.1	X		verilog	10	oc54_cpu	Y	yes	N	Y	64K	64K						2002	2009		40-bit accumulator, barrel shifter	C54x clone
tg68	https://opencor	stable	Tobias Gubener	68000	16	16		kintex-7-3	James Brakef		2331		6			44	##	14.7	0.67	4.0	3.2	X		vhdl	2	TG68_fast	Y	yes	N	N	4G	4G	Y			16		2007	2012		TG68 - execute 68000 Code	for use with Minimig
k68	https://opencor	alpha	Shawn Tan	RISC	16	16		kintex-7-3	James Brakef		2392		6			24	##	14.7	0.67	4.0	1.7	X		verilog	15	k68_cpu	Y	yes	N	N	4K	4G	Y			16		2003	2009		68K binary compatible	
atlas_core	https://opencor	beta	Stephan Nolting	dsp	16	16		spartan3	Stephan Nolt		2406	1091	4	1	11	81	##	14.7	0.80	1.0	27.0	ALX		vhdl	19	ATLAS_2K	Y	asm	N	Y	64K	64K	M	80		8		2013	2015	https://www.allat	ARM thumb like inst set	has MMU & full SOC features
dsp16	https://github.com/jotege		Jose Tejada	PDP11	16	16		cyclone5	Jose Tejada		2471	612	A		12							A		verilog	12	jtdsp16	Y	asm	N	Y	64K	64K	N	29		16		2020	2021		compatible with ATT WE DSP16	
pdp11-34verilo	www.heeltoe.co	stable	Brad Parker	RISC	16	16		arria-2	James Brakef		2532		A			126	##	q13.1	0.67	2.0	16.7	AX	Y	verilog	24	pdp11	Y	yes	N	N	64K	64K		70	13	8		2009			boots & runs RT-11, EIS inst & MMU	
xgate	https://opencor	alpha	Robert Hayes	RISC	16	16		kintex-7-3	James Brakef		2778		6			159	##	14.7	0.67	1.0	38.3	X		verilog	7	xgate_top	Y		N					42		16		2009	2013		high pin count	Freescale XGATE co-processor compatible
atlas_core	https://opencor	beta	Stephan Nolting	misc	16	16		cyclone4	Stephan Nolt		2967	1364	4	1	32	99	##	q18.0	0.80	1.0	26.7	ALX		vhdl	19	ATLAS_2K	Y	asm	N	Y	64K	64K	M	80		8		2013	2015		ARM thumb like inst set	has MMU & full SOC features
sifp	https://github.c	WIP	Zoltan Pekic	68000	16	16		spartan3-	James Brakef		3157	563	4		3	123	##	14.7	1.33	2.0	25.8	X		vhdl	36	mercury	Y		N		64K	64K		30		4		2023	2024	https://hackaday.i	"Single Instruction Format Processor"	five micro-operations per inst
fx68k	http://fx68k.fxatari.com/f		Jorge Cwik	forth	16	16		spartan7	James Brakef		3162	1504	6		1	100	##	v23.2	1.00	3.0	10.5	X		system	3	fx68k	Y	yes	N		4G	4G	Y			16		2018	2021	https://github.cor	Cycle accurate, see http://atari-forum.com/viewtopic.php?f=28&t=34730#p358139	
s4pu	https://baioc.github.io/pc		Gabriel de Sant'Anna	68000	16	16		cyclone2	Gabriel de Sa		3306	1622	4		86	50	##	q13.1	0.67	1.0	10.1	A		vhdl	17	s4pu	Y	asm	N		64K	64K		32				2017	2020	https://gitlab.com/baioc/s4pu	in Portuguese	
ao68000	https://opencor	beta	Aleksander Osman	x86	16	16		arria-2	James Brakef		3479		A		6	169	##	q13.1	0.67	4.0	8.1	A	Y	verilog	1	ao68000	bm	yes	N		4G	4G	Y					2010	2012		uses microcode, instruction prefetch	buffer
zet86	https://opencor	alpha	Zeus Marmolejo	pdp11	16	8		kintex-7-3	James Brakef		3642		6	1		68	##	14.7	0.67	2.0	6.2	X		verilog	32	fpga_zet_	Y	yes	N	N	1M	1M	Y					2008	2018	https://github.cor	equivalent to 80186, boots MS-DOS	Zet The x86 (IA-32) open implementation
copro6502	https://github.c	stable	David Banks	MSP430	16	16		spatan6-9	James Brakef		3689	947	6	1	16	33	##	14.7	0.67	3.0	2.0	X	Y	vhdl, Verilog		PDP11.xis	Y	yes			64K	64K	Y	70	13	8		2014	2019	https://stardot.or	PDP11	max'd out block RAM
neo430	https://opencor	alpha	Stephan Nolting	x86	16	16		ice40	Stephan Nolt		3928	1923	4		6	20	##	LR	0.67	4.0	0.9	ALX	Y	vhdl	19	neo430_t	Y	yes	N		28K	32K	Y			16		2015	2024	https://github.cor	website has detailed resource unti	default config, includes true RNG
rtf8088	https://opencor	planning	Robert Finch	accum	16	8		kintex-7-3	James Brakef		4514		6	4		174	##	14.7	0.67	3.0	8.6	X		verilog	57	rtf8088	Y	yes	N	N	1M	1M	Y					2012	2013	https://github.cor	8-bit memory data, e.g. 8088	
hack	https://github.com/philzo		Philip Zucker	accum	16	16		spartan7	James	block I	4705	287	6			82	##	v23.2	0.67	2.0	5.8	X		verilog	22	computer	Y	yes	N	Y	32K	32K	N	18		2			2021	https://www.nand	educational formally verified version of the Nand 2 Tetris course using Coq	
hack	https://github.com/theap		Peter Clarke	pdp11	16	16		spartan7	James	block I	4803	287	6			83	##	v23.2	0.67	2.0	5.8	X		verilog	22	cpu	Y	asm	N	Y	32K	32K	N	18		2			2016	https://www.nand	CPU used to run Tetris	book: Elements of Computing Systems
copro6502	https://github.c	stable	David Banks	68000	16	16		kintex7-3	James	bare c	4978	1587	6	1		204	##	14.7	0.67	3.0	9.1	X	Y	vhdl, Verilog		pdp2011_	Y	yes			64K	64K	Y	70	13	8		2014	2019	https://stardot.or	PDP11	
v1_coldfire	https://www.sil	proprietar	IPextreme	PDP11	16	16		cyclone-3	freescale		5000		4			80			0.89	1.0	14.2	A		verilog			Y	yes	N	N	4G	4G	Y					2008		https://www.silva	free for Altera	3500 LUTs on Stratix-III
pdp2011	http://pdp2011	stable	Sytse van Slooten	forth	16	16		kintex-7-3	James Brakef		5060		6	1		205	##	14.7	0.67	2.0	13.6	AX	Y	vhdl	3	cpu	Y	yes	Y	N	64K	64K		70	13	8		2008	2019	http://pdp2011.sy	SoC, build files for A&X boards	complete impl including orig IO devices
stack_machine	http://people.ec	stable	Bruce R. Land	RISC	16	5		cyclone10	James Brakef		5101		4	6	29	66	##	q18.0	0.67	3.0	25.9	X		verilog	9	VGA_sram	Y	asm	N	N	64K	4K	N					2009	2011	https://people.ec	(3) uP cores, Cornell course material	VGA output, uses Nakano's tiny_cpu
ucode_cpu	http://minnie.tu	stable	Warren Toomey	RISC	16	16		atrix-7-3	James	4K LUT	6748		6	1	1		##	14.7	0.67	2.0			A	vhdl	16	cpu			N	N	64K	64K	N			16		2012	2015		originally schematic based (Logisim)	
aap	https://github.c	stable	Simon Cook	68000	16	16		arria-2	James Brakef		7193		A			393	##	q18.0	0.67	1.0	36.6	A		verilog	7	de0_nano	Y	yes		Y	64K	16M	Y			64		2015	2016	http://www.embe	includes Altera project	4 to 64 reg, 24-bit pc, no status reg
suska-III	http://www.exp	beta	Wolfgang Forster	RISC	16	16		arria-2	James Brakef		7388		A			55	##	q13.1	0.67	4.0	1.3	A		vhdl	11	wf68k00ip	Y	yes	N	N	4G	4G	Y			16		2003	2013		for use as an Atari ST	
aap	https://github.c	stable	Simon Cook	68000	16	16		cyclone-4	James Brakef		10630		4			306	##	q18.0	0.67	1.0	19.3	A		verilog	7	de0_nano	Y	yes		Y	64K	16M	Y			64		2015	2016	http://www.embe	includes Altera project	4 to 64 reg, 24-bit pc, no status reg

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
rtf68ksys	https://opencor	alpha	Robert Finch	68000	16	16	spartan-3	James	need t	13639		4	12	17		##	14.7	0.67	4.0		X	Y	verilog	49	rtf68kSys	Y	yes	N	N	4G	4G	Y			16		2011	2011	https://github.cor	based on Tobias Gubener's TG68	
aoocs	https://github.c	beta	Aleksander Osman	68000	16	16	arria-2	James	Brakef	17852		A	2	43	57	##	q18.0	0.67	4.0	0.5	A	Y	verilog	22	aoOCS	pn	yes	N		4G	4G	Y					2010	2011		uses ao68000 core, Amiga chip set en	Wishbone Amiga OCS SoC
aoocs	https://github.c	beta	Aleksander Osman	68000	16	16	cyclone-1	James	Brakef	26009		4	2	67	45	##	q18.0	0.67	4.0	0.3	A	Y	verilog	22	aoOCS	pn	yes	N		4G	4G	Y					2010	2011		uses ao68000 core, Amiga chip set en	Wishbone Amiga OCS SoC
aoocs	https://github.c	beta	Aleksander Osman	accum	16	16	cyclone-2	Aleksander O		26227		4	2	65		##	q10.1	0.67	4.0		A	Y	verilog	22	aoOCS	pn	yes	N		4G	4G	Y					2010	2011		uses ao68000 core, Amiga chip set en	Wishbone Amiga OCS SoC
acc	https://github.c	stable	Juan Gonzalez-Gomez	accum	15	15	kintex-7-3	James	rom &	89	96	6		1	227	##	14.7	0.67	2.0	855.5	AX		verilog	1	acc2	Y	yes	N			4K					2016	2016	https://github.cor	26 chptr course using Apollo Commar	??why LUT count different from agcnorm
agcnorm	https://opencor	beta	Dave Roberts	accum	15	15	kintex7-3	James	Brakef	2252	1110	6		2	32	##	14.7	0.66	1.0	9.3	X		vhdl	5	AGC	Y		N	Y	4K	72K	N	11		1		1962	2012	http://klabs.org/h	Apollo Guidance Computer via 3-input	NOR gate emulation
agcnorm	https://opencor	beta	Dave Roberts	picoBlaze	15	15	spartan-3	James	Brakef	3732	1115	4		2	20	##	14.7	0.66	1.0	3.5	X		vhdl	5	AGC	Y		N	Y	4K	72K	N	11		1		1962	2012	http://klabs.org/h	Apollo Guidance Computer via 3-input	NOR gate emulation
wb4pb	https://opencor	stable	Stefan Fischer	accum	13	13	spartan-3	Stefan	Fische	309		4		1	102	##	14.7	0.33	3.0	36.2	X	Y	vhdl, v	14	picoblaze_wb_uart				Y							2010	2013	https://en.wikipec	software addon for picoBlazeSoftwar	kcpsm3 only works for Spartan 3
cardiac	https://opencor	mature	Al Williams	picoBlaze	13	12	spartan-3	James	Brakef	557		4			71	##	14.7	0.30	1.0	38.5	X		verilog	16	vtach	Y	asm	N		100	100	N	10				2013	2019	https://www.cs.d	CARDboard Illustrative Aid to Comput	3 digit BCD arithmetic
wb4pb	https://opencor	stable	Stefan Fischer	accum	13	13	kintex-7-3	James	incomplete port to kcp			6				##	14.7	0.33	3.0			Y	vhdl, v	14	picoblaze_wb_uart				Y							2010	2013	https://en.wikipec	software addon for picoBlazeSoftwar	ported to kcpsm6
usimplez	https://opencor	stable	Pablo Salvadeo etal	accum	12	12	stratix-2	Pablo	Salvade	48		4			134		q9.1	0.17	2.0	237.9	A		vhdl	3	usimplez_cpu			N		512	512		8				2011		http://www-gti.de	part of university course, simplez+i4	has an index register
simplecpu12	https://github.com/jasom	Jan Sommer	PDP8	12	12	spartan6	Jan Sommer		498	212	6		6	180	##	14.7	0.50	2.0	90.4	X		vhdl	9	top_level	Y		N	Y	4K	4K	N	32	3			2020			educational, has stack pointer	looks like an accumulator dsgn
pdp8verilog	www.heeltoe.co	stable	Brad Parker	forth	12	12	kintex-7-3	James	Brakef	505		6			366	##	14.7	0.50	2.0	181.3	X		verilog	18	pdp8	Y	yes	N	N	32K	32K				8		2005	2010		boots & runs TSS/8 & Basic	
microcore	http://www.pld	beta	Klaus Schleisiek	PDP8	12	8	kintex-7-3	James	Brakef	513	75	6			336	##	14.7	0.40	1.0	261.9	X		vhdl	30	ucore110	Y	asm	N	Y	512	2K						1999	2023	www.microcore.o	indexing into return stack, auto inc/d	only one block RAM? simplest core
socdp8	https://github.c	beta	Folke Will	stack/acc	12	12	spartan7	James	Brakef	583	268	6			106	##	v24.1	0.50	3.0	30.4	X	Y	vhdl, v	34	pdp8	Y	yes	N	N	32K	32K				8		2019	2019		SoC implementation of a PDP-8/I for t	includes extended ALU
the12X_12uP		alpha	James Brakefield	PDP8	12	12	kintex-7-3	James	Brakef	972		6	1	1	123	##	14.7	0.50	1.0	63.3	X		vhdl	2	the12x_12	Y		Y	N	4K	4K	N	54		64	1	2015			combo stack/accumulater design	load/store arch, not optimized
pdp8l	https://opencor	beta	Ian Schofield	PDP8	12	12	cyclone-3	James	Brakef	1088		4		48	63	##	q13.1	0.50	2.0	14.4	A		vhdl	11	top	Y	yes	N	N	4K	4K						2013	2013		Minimal PDP8/L implementation with	4K disk monitor system
pdp8	https://opencor	alpha	Joe Manojlovick, Rob	PDP8	12	12	kintex-7-3	James	Brakef	1219		6	1		183	##	14.7	0.50	2.0	37.5	X	Y	vhdl	55	cpu	Y	yes	N	N	32K	32K				8		2012	2016		PDP-8 Processor Core and System	Boots OS/8, runs apps, several variants
cpus-pdp8	https://github.com/lisper	Brad Parker	6809	12	12	spartan3	Brad Parker		1605	481	4		1	50	##	14.7	0.40	2.0	6.2	X	Y	verilog	15	top	Y	yes	N	N	4K	4K						2004	2016		A working PDP-8/i cpu with an RF08 d	disk emulator which uses a IDE disk as a backing
rf6809	https://opencores.org/pr	Robert Finch	forth	12	12	artix-7	Robert Finch		6500		6		5	120	##	v21.2	0.50	4.0	2.3	X	Y	system	21	rf6809	Y	asm	N		64G	64G	Y	44	13	8		2022	2024	http://www.finitro	Different from rtf6809: 36-bit adrs, o	12-bit version, has inst. Cache
eric5	http://www.ent	proprietar	Thomas Entner	risc	9	8	cyclone-4	entner-electr		110		4	opt		60			0.42	1.0	229.1	A		proprietary							512	1K				3-4		2005	2011		25 MIPS: ERIC5xs, ERIC5Q	
baby8	https://github.com/jecelj	Jecel de Assumpcao Jr	risc	8	8	cyclone5	Jecel de Assu		29		A		16	58	##		0.17	4.0	84.5	AGLX		schem	17	baby8cpu	Y	asm	N		64K	64K	Y			16		2024		https://mdpi-res.c	minimal 8-bit uP with 16-bit adrs	schematic, verilog & system verilog
baby8	https://github.com/jecelj	Jecel de Assumpcao Jr	accum	8	8	spartan7	Jecel de Assu		31		6		4	58	##		0.17	4.0	79.1	AGLX		schem	17	baby8cpu	Y	asm	N		64K	64K	Y			16		2024		https://mdpi-res.c	minimal 8-bit uP with 16-bit adrs	stats for several soft uP 4 FPGA/ASIC versions
mcpu	https://opencor	stable	Tim Boscke	TMS9900	8	8	spartan-6	James	Brakef	41	30	6			384	##	14.7	0.08	1.0	749.0	X		vhdl	1	tb02cpu2	Y	asm	N		64	64	Y	4				2007	2018	https://github.cor	MCPU A minimal CPU for a CPLD	reduced MISPS/clk due to only 4 inst
core9900	https://github.com/dnotq	Matthew Hagerty	accum	8	8	kintex-7-3	James	incom	41	30	6			122	##	v23.2	0.33	5.0		X	Y	vhdl	7	top	Y	yes	N		64K	64K				16		2017			MSP 9900	LUT counts don't match those of a 8bit uP
sap	https://opencor	stable	Ahmed Shahein	accum	8	8	kintex-7-3	James	no LU	48		6			200	##	14.7	0.10	4.0	104.2	X		vhdl	15	mp_struct			N		16	16	Y	5				2012	2022	https://shirishkoir	Simple as Possible Computer from M	https://www.youtube.com/watch?v=prpyEFxZ
sap	https://github.c	stable	Federico Zotti	risc	8	8	kintex-7-3	James	no LU	48		6			200	##	14.7	0.10	4.0	104.2	G		vhdl	9	sap-1-TOP			N		16	16	Y	5				2024			Simple as Possible Computer	Gowin 9K project
baby8	https://github.com/jecelj	Jecel de Assumpcao Jr	risc	8	8	gowin	Jecel de Assu		48		4		4	58	##		0.17	4.0	51.1	AGLX		schem	17	baby8cpu	Y	asm	N		64K	64K	Y			16		2024		https://mdpi-res.c	minimal 8-bit uP with 16-bit adrs	micro-coded; mcpu has best figure of merit
drv16/mcpu16	https://github.com/jecelj	Jecel de Assumpção	risc	8	8	gowin	Jecel de Assu		69	48	4			313	##		0.17	2.0	378.8	AGLX		schematic			Y		N		256	256				16		2024		https://www.mdp	very simple accumulator based 8 bit uP	with four instructions
baby8	https://github.com/jecelj	Jecel de Assumpcao Jr	accum	8	8	ecp5	Jecel de Assu		77		4		4	58	##		0.17	4.0	31.8	AGLX		schem	17	baby8cpu	Y	asm	N		64K	64K	Y			16		2024		https://mdpi-res.c	minimal 8-bit uP with 16-bit adrs	relatively low uniform Fmax
lwrisc	https://opencor	stable	Li Wu	accum	8	12	arria-2	James	Brakef	88		4		1	230	##	q13.1	0.17	1.0	443.6	A		verilog	9	risc_core		asm	N	Y	256	2K	Y	16				2008	2009		ClaiRISC simplified PIC, 4 reg rtn stack	absolute addressing only, lowered MIPS/clk
opc.opccpu	https://github.c	stable	revaldinho	accum	8	16	kintex-7-3	James	reduce	101		6			526	##	14.7	0.15	4.0	195.4	X		verilog	2	opccpu	Y	asm	N	N	256	2K	Y	13	3			2017	2021	https://revaldinho	OPC1 one page computer for CPLD	**see hackaday One Page Computing Challe**
td4	https://github.c	stable	cielo_ee	picoBlaze	8	8	spartan-3	James	Brakef	102					200	##	14.7	0.20	1.0	392.2	X		verilog	5	td4_top						16	Y					2012	2015			very small uP
riscuva1	https://www.sc	stable	S. de Pablo	picoBlaze	8	14	kintex-7-3	James	Brakef	109		6			370	##	14.7	0.33	2.0	560.7	X		verilog	1	riscuva1	ome		N	Y	256	1K	Y	35				2006	2006	https://github.cor	Verilog source included in PDF file	also VHDL version by Bikash Gogoi with identic
picoblaze	https://www.xil	stable	Ken Chapman	mem	8	18	kintex-7-3	James	Brakef	110		6		2	217	##	14.7	0.33	2.0	325.5	X		vhdl	1	kcspm6	Y	asm	N		256	2K	Y					2003		https://en.wikipec	2 clocks/inst, no prog ROM	this is the original picoBlaze author
brainfuckcpu	https://opencor	beta	Aleksander Kaminski	accum	8	3	kintex-7-3	James	Brakef	110		6			432	##	14.7	0.08	2.0	157.2	X		verilog	1	brainfuck_cpu			N	Y				8		0		2014	2015	http://www.cliffo	Touring machine like, 2ndary link is a	adj prog & data mem size, terrible name
opc.opc2cpu	https://github.c	stable	revaldinho	RISC	8	16	kintex-7-3	James	reduce	117		6			556	##	14.7	0.15	4.0	178.1	X		verilog	2	opc2cpu	Y	asm	N	N	256	1K	Y	12	3			2017	2021	https://revaldinho	OPC2 revised OPC1, for XC9572 CPLD	see hackaday One Page Computing Challenge
myrisc1		stable	Muza Byte	RISC	8	8	arria-2	James	Brakef	121		A		2	231	##	q13.1	0.33	1.0	628.7	A		verilog	1	myRISC1	Y		N	Y	256	256	Y	16		4		2011	2011	https://en.wikipec	Verilog source included in PDF file	AKA Mano Machine, LPM macros
aizup/aizup_m	instruct1.cit.cor	stable	Yamin Li, Wanming Ch	forth	8	16	arria-2	James	Brakef	129		A			298	##	q13.1	0.17	2.0	192.6	AX		vhdl	1	cpu			N	N	64K	64K		16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
8bit_chapman	http://www.ece	beta	Rob Chapman, Steven	RISC	8	8	**zu-3e**	James	vivado	132	63	6			305	##	v21.1	0.33	1.0	762.2	ALX		vhdl	10	stack_pro	Y		N		256	256	Y	24				1998	1998		course work	
tinycpu	https://opencor	alpha	Jordan Earls	RISC	8	8	arria-2	James	Brakef	136		A			384	##	q13.1	0.17	2.0	235.5	AX		vhdl	2	tinycpu		asm	N	N	1K	1K		12		4		2012	2012	directory contains	subset of 6502	MIPS/inst reduced due to few inst
aizup/aizup_se	instruct1.cit.cor	stable	Yamin Li, Wanming Ch	RISC	8	16	kintex-7-3	James	Brakef	136	90	6			313	##	14.7	0.17	8.0	48.1	AX		vhdl	1	cpu		asm	N	N	64K	64K	Y	16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
aizup/simple_8	instruct1.cit.cor	stable	Yamin Li, Wanming Ch	RISC	8	8	kintex-7-3	James	Brakef	136	55	6			313	##	14.7	0.17	8.0	48.1	AX		vhdl	1	cpu		asm	N	N	64K	64K	Y	16		4		1996	1998		used in Cornell EE475 course	similar to mica
aizup/aizup_ov	instruct1.cit.cor	stable	Yamin Li, Wanming Ch	8080	8	16	kintex-7-3	James	Brakef	138	51	6			318	##	14.7	0.17	3.0	128.3	AX		vhdl	1	cpu		asm	N	N	64K	64K	Y	16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
light8080	https://opencor	stable	Jose Ruiz, Moti Litoche	accum	8	8	kintex-7-3	James	Brakef	154		6		1	247		14.7	0.33	9.0	58.9	AX		verilog	5	i80soc	Y	yes	N	N	64K	64K	Y					2007	2019	https://github.cor	targeted to area, includes UART, inte	older versions have both VHDL & Verilog
parwan		stable	Zainalabedin Navabi	accum	8	8	kintex-7-3	James	Brakef	157		6			435	##	14.7	0.33	4.0	228.5	X		verilog	16	par_beh	Y	yes	N	N	4K	4K	Y					1995	1997	2nd uP in director	from VHDL: Analysis and Modeling of	AKA cpu8, both vhdl & verilog versions
parwan		stable	Zainalabedin Navabi	accum	8	8	kintex-7-3	James	Brakef	161		6			76	##	14.7	0.33	4.0	38.8	X		vhdl	2	parwan	Y	yes	N	N	4K	4K	Y					1995	1997	2nd uP in director	from VHDL: Analysis and Modeling of	AKA cpu8, both vhdl & verilog versions
lipsi	https://github.c	stable	Martin Schoeberl	accum	8	8	cyclone4	Martin	Schoe	162		4		1	162			0.17	1.0	167.0	A		scala	2		Y		N	N	64K	64K	Y	9	3	16		2017	2024	https://github.cor	goal is 100 LUTs, program mapped to	"Lipsi, a very tiny processor"
ben_eater_up	https://github.com/Xarkl	Ken Jordan	AVR	8	8	spartan7-	James	Brakef	164	137	6			100	##	v23.2	0.33	2.0	100.6	X		vhdl	6	system	Y	asm	N		256	16	Y					2015	2019	https://eater.net/	Ben Eater's 8-bit breadboard computer	
avr8	https://opencor	beta	Nick Kovach	RISC	8	16	kintex-7-3	James	Brakef	174		6			418	##	14.7	0.33	1.0	792.2	X		verilog	1	rAVR	Y	yes	N		64K	64K	Y	17		4		2010	2010		Reduced AVR Core for CPLD	not a full clone, doc is opencores page
nocpu	https://github.c	beta	John Tzonevrakis	forth	8	8	kintex-7-3	James	Brakef	175		6			243	##	14.7	0.33	1.5	306.1	X		verilog	5	cpu	N	no	N		256	256	Y			4		2017			minimal & complete	8 ALU inst, 3 port reg file
8bit_chapman	http://www.ece	beta	Rob Chapman, Steven	picoBlaze	8	8	kintex-7-3	James	Brakef	176	64	6			131	##	14.7	0.33	1.0	245.5	ALX		vhdl	10	stack_pro	Y		N		256	256	Y	24				1998	1998		course work	
pacoBlaze	www.bleyer.org	mature	Pablo Kocik	picoBlaze	8	18	spartan-3	Pablo	Kocik	177		4		1	117			0.33	2.0	109.1	X		verilog	18	pacoblaze	Y	asm	N		256	2K	Y	57			2		2006		3 versions, behavioral coding	
picoblaze	https://www.xil	stable	Ken Chapman	accum	8	18	spartan-3	James	Brakef	178		4		1	182	##	14.7	0.33	2.0	168.9	X		vhdl	1	kcspm3	Y	asm	N		256	2K	Y					2003		https://en.wikipec	2 clocks/inst, no prog ROM	this is the original picoBlaze author
mroell_cpu	https://bitbucke	stable	Matthias Roell	accum	8	8	kintex-7-3	James	added	185		6			357	##	14.7	0.33	1.0	637.1	X		vhdl	8	cpu	Y							10				2014	2016		university course project	
tinyfpga	https://github.c	stable	Ken Jordan	accum	8	8	kintex-7-3	James	Brakef	185		6		1	175	##	14.7	0.33	3.6	86.9	X		vhdl	12	system			N	N	16	16	Y	10				2017	2017		educational 8-bitter with 4-bit addres	why use block RAM?
ahmes	https://github.c	stable	Fabio Pereira	accum	8	8	kintex-7-3	James	Brakef	186	100	6			476	##	14.7	0.33	3.0	281.6	X	B	vhdl	3	ahmes			N	N	256	256	Y	15	1			2016	2017	http://embeddedsystems.io/ahmes-a-simple-8-bit-cpu-i	bare CPU with no RAM	
tisc	https://opencor	beta	Vincent Crabtree	forth	8	8	kintex-7-3	James	Brakef	195		6			87	##	14.7	0.33	1.0	147.1	X		vhdl	1	TISC			N		256	1K	Y			2		2009	2009		Tiny Instruction Set Computer	minimal accumulator machine
ssbcc	https://opencor	stable	Rodney Sinclair	RISC	8	9	kintex-7	Rodney	Sincla	196		6			474		14.7	0.33	1.0	797.9	ALX		verilog	3	core	Y	asm	N	Y	1K	8K	Y	41		3		2012	2020	https://github.cor	Python program generates the Verilo	inst after branch/call/rtn always execs
aizup/aizup_pi	instruct1.cit.cor	stable	Yamin Li, Wanming Ch	accum	8	16	kintex-7-3	James	Brakef	198	52	6			375	##	14.7	0.17	2.0	157.9	AX		vhdl	1	cpu		asm	N	N	64K	64K	Y	16		4		1996	1998		used in Cornell EE475 course	MIPS/inst reduced due to few inst
vhdl_cpu	https://github.com/CGras	Charles Grassin		8	16	spartan3	Charles	Grass	203	116	4						14.7	0.20	2.0				vhdl	6	computer	Y	asm	N	N	256	256	N	14				2017	2020	http://charleslabs	educational, very simple	case statement program
complete_8bit	https://www.qu	stable	Van-Lei Le	RISC	8	8	kintex-7-3	James	modifi	208		6		1	260	##	14.7	0.33	3.0	137.5	X		vhdl	6	computer	N		N		96	128	Y					2016			memory_unit uses block RAM, IO ports prunec	
up1232	http://www.dte	stable	Santiago de Pablo	accum	8	16	kintex-7-3	James	Brakef	220		6			244	##	14.7	0.33	3.0	122.0	X		vhdl	3	up1232a			N		64K	64K	Y	33	2	32		2000	2000		bare core, prog size 4K to 64K	description in source files
non-von-1	https://www.ch	stable	Christopher Fenton	RISC	8	8	kintex-7-3	James	Brakef	230	89	6			556	##	14.7	0.33	1.0	797.1			verilog	1	nonvontop	no		N		64		Y	30				2018			SIMID in tree structure	A & B regs, instructions broadcast
natalius_8bit_r	https://opencor	beta	Fabio Guzman	1802	8	16	kintex-7-3	James	Brakef	232		6		1	175	##	14.7	0.11	3.0	27.7	X		verilog	12	natalius_p	Y	asm	N	Y	256	2K	Y	29		8		2012	2012		return stack & register file	3 clocks/inst
cosmac	https://github.c	beta	Eric Smith	picoBlaze	8	8	kintex-7-3	James	Brakef	244		6			270	##	14.7	0.33	1.0	365.5	X		vhdl	1	cosmac	Y	asm	N	N	64K	64K	Y	100		16		2009	2020		AKA COSMAC ELF of 1976	Fmax is for bare core, runs CamelForth
nanoblaze	https://opencor	beta	Francois Corthay	1802	8	18	kintex-7-3	James	Brakef	247		6		1	169	##	14.7	0.33	2.0	113.2	X		vhdl	12	nanoblaze		asm			256	2K	Y					2015	2015		nanoBlaze compatable, adjustable data width	
1802-pico-basi	https://github.c	beta	Steve Teal	RISC	8	8	**zu-3e**	James	area o	247	136	6		2	427	##	v21.1	0.33	12.0	47.6	LX		vhdl	6	pico_basic	Y	yes	N		64K	64K	Y	52		16		2016	2016	https://wiki.forth-	VHDL 1802 Core with TinyBASIC	tiny Basic in ROM, Interrupts & DMA not imple
babyrisc	http://www.san	stable	John Rible	6502	8	16	kintex-7-3	James	Brakef	249		6			286	##	v21.1	0.33	2.0	189.3	X		verilog	1	qs5_mix	Y		N		64K	64K	Y	15		8		1997	1999	http://www.sandp	part of a three class course	memory rd/wt & ALU per clock
mcl65	http://www.mic	stable	Ted Fried	accum	8	8	atrix-7-3	Ted Fried		252		6		2	196	##	14.7	0.33	4.0	64.2	X		verilog	1	mcl65	Y	yes	N	N	64K	64K	Y					2017	2021	https://github.cor	**microcoded, cycle exact**	**excellent micro-coding LUT counts**
fpga4_8bit_up	http://www.fpg	stable	Van Loi Le	risc	8	8	kintex-7-3	James	Brakef	258		6		1	200	##	14.7	0.33	3.0	85.3	X		vhdl	9	computer	ome		N		96	128	Y	10		2		2016	2016	book: LaMeres Int	educational	16 input & 16 output ports fill out 256 byte adr
drv16/ncpu	https://github.com/jecelj	Jecel de Assumpção	accum	8	8	gowin	Jecel de Assu		264	182	4			127	##		0.33	2.0	79.4	AGLX		schematic			Y		N		256	256				16		2024		https://www.mdpi.com/2674-0729/3/4/20		
kiwih	https://github.com/kiwih	Hammond Pearce	RISC	8	8	artix-7	James	has AS	265	173	6			100	##	v23.2	0.20	1.0	75.5	X		verilog	8	kiwih_tt_t	Y	asm	N		32	256	Y	20				2023		https://github.cor	uP design via chatGPT4, ASIC gate list	study using chatGPT4 for hdware synthesis
latticemico8	http://www.latt	stable	Lattice Semiconductor	accum	8	18	LFE2	Lattice	Semic	265		4		1	104			0.33	2.0	64.4	ALX		vhdl	10	isp8_core	Y	yes	N		256	4K	Y			32		2005	2010	https://en.wikipec	16 deep call stack, four configuration	tool kit: LMS for Diamond3.10
popcorn	http://www.fpg	stable	Jeung Joon Lee	RISC	8	8x	kintex-7-3	James	Brakef	267		6			347	##	14.7	0.33	1.0	428.4	X		verilog	4	pc	Y		N		64K	64K	Y	43				1998	2000		small 8 bit uP	
iop16b	https://github.c	alpha	Doug Gilliland	accum	8	16	cyclone4	Doug	Gilliland	271	76	4		2	50	##		0.33	4.0	15.2	A	Y	vhdl	51	cpu_top	Y	asm	N		4K	4K	Y	18		8		2021	2022	https://hackaday.	I/O Processor with minimal instructio	full set of perpherals, 2022 version is huge
mcu8	https://opencor	alpha	Dimo Pepelyashev	6502	8	8	kintex-7-3	James	Brakef	274		6			299	##	14.7	0.33	1.0	360.1	X		vhdl	16	processor_E	asm				256	256	Y	17				2008	2009		asm, simulated, builds?	
minicpu_morri	https://github.com/Morri	Michael Morris	risc	8	8	spartan-6	Michael	Morr	276		6			104			0.33	2.0	62.2	X		verilog	15	minicpu_d	Y		N		64K	64K	Y	31					2017		simplified 6502, see m65c02a	RE: 8-bit CPU challenge of Arlet Ottens
baby8	https://github.com/jecelj	Jecel de Assumpcao Jr	forth	8	8	ice40	Jecel de Assu		285		4			58	##		0.17	4.0	8.6	AGLX		schem	17	baby8cpu	Y	asm	N		64K	64K	Y			16		2024		https://mdpi-res.c	minimal 8-bit uP with 16-bit adrs	ASIC & FPGA stats for risc-v, baby8 & soft uP
dfp	https://opencor	stable	Ron Chapman	accum	8	8	kintex-7-3	James	Brakef	297		6			192	##	14.7	0.33	1.0	213.2	X		vhdl	25	DataFlowB	Y											2003	2009		8-bitter, generates a custom VHDL stack machine, compiler is in Forth	
pt13	http://www.sin	stable	Daniel Ogilvie	Turing	8	8	kintex-7-3	James	Brakef	301		6			357	##	14.7	0.33	3.0	130.5			verilog	1	pt13	Y	asm	N	Y	64K	8K	Y	40	3			2011	2018	https://www.edn.	PT13 is optimized to be completely e	micro-code & register updates, minimal ISA
bfcpu	http://www.cliff	stable	Clifford Wolf	picoBlaze	8	3	**zu-3e**	James	Brakef	303		6			500	##	v21.1	0.01	4.0	4.1	X	B	vhdl	4	cw6670	Y	yes	N	N	64K	64K	Y	8				2003	2003	https://en.wikipec	no accum, data pointer and bracketed	first implementation, no data cache
dapzipi8	https://github.com/ehsan	Ehsan Ali	8051	8	18	zu-5e	Ehsan	conve	305	49	6		2	224	##	v22.1	0.33	1.0	242.4	X		vhdl	20	top	Y	asm	N		256	2K	Y					2022			Deterministic Branch Prediction for R	also zipi8 starting point, PhD thessis

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	vendor	SOC	src code	#src files	top file	doc	tool chain	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
mcl51	http://www.mic	stable	Ted Fried	picoBlaze	8	8	artix-7-3	Ted Fried		312		6		2	180			0.33	8.0	23.8	X		verilog	3	mcl51_TO	Y	yes	N	N	64K	64K	Y					2016	2021	https://github.cor	**micro-coded**	
picoblaze	https://www.xil	stable	Ken Chapman	forth	8	18	kintex-7-3	James Brakef		317		6		2	195	##	14.7	0.33	2.0	101.6	X	Y	vhdl	19	kc705_kcp	Y	asm	N		256	2K	Y					2003		https://en.wikipe	2 clocks/inst	this is the original picoBlaze author
bytemachine	https://github.c	mature	c0pperdragon	6502	8	8	kintex-7-3	James Brakef		319		6		1	250	##	14.7	0.33	2.0	129.3	AX		vhdl	7	bytemach	ome	N	N		4K	Y	30				2016	2017		top is Altera schematic	results are for 2016 bare core
mcl65	http://www.mic	stable	Ted Fried	PIC16	8	8	kintex-7-3	James	inserte	326		6		2	196	##	14.7	0.33	4.0	49.6	X		verilog	1	mcl65	Y	yes	N	N	64K	64K	Y					2017	2021	http://www.micro	**microcoded, cycle exact**	**excellent micro-coding LUT counts**
pic_coonan		alpha	Tom Coonan	PIC16	8	14	kintex-7-3	James Brakef		328		6		1	165	##	14.7	0.33	1.0	166.1	X		verilog	7	piccpu	Y	yes	N	Y	256	4K	Y					1999			risc8 by Tom Coonan also a PIC uP	
free_risc8	https://web.arc	stable	Thomas Coonan	PIC16	8	14	kintex-7-3	James Brakef		355	118	6			142	##	14.7	0.33	1.0	132.2	X		verilog	8	cpu	Y	yes	N		256	4K	Y					2002	2011	https://web.archive.org/web/20120309123835/http://www.mindspring.com/~tcoonan/index.html		
risc8	https://web.arc	stable	Tom Coonan	AVR	8	12	kintex-7-3	James Brakef		355		6			154	##	14.7	0.33	2.0	71.5	X		verilog	8	cpu	Y	yes	N	Y	256	2K	Y					1999	1999	https://github.cor	excellent HTML doc	directory contains derivative design by another
classy_core_17	https://github.com/classy		Andreas Schweizer	RISC	8	16	spartan-3	Andreas Schv		358		4			164	##	14.7	0.33	1.0	151.2			vhdl	8	top	Y	yes	N		64K	128K	Y	72		32		2019		https://blog.classy	adjuct to some custom logic	Implementing a CPU in VHDL parts 1..3
erp	https://opencor	stable	Shahzadjk	PIC16	8	16	spartan-3	James Brakef		366		4	1	1	70	##	14.7	0.33	1.0	63.5	X		verilog	1	ERPverilog	Y							15		6		2004	2014		two report PDFs & one Verilog file	
risc16f84	https://opencor	stable	John Clayton	PIC16	8	14	kintex-7-3	James Brakef		375		6			392	##	14.7	0.33	2.0	172.5	AX		verilog	1	risc16f84	Y	yes	N	Y	256	4K	Y					2002	2018		derived from CQPIC by Sumio Morioka	other variants with RTL
p16c5x	https://opencor	mature	Michael Morris	RISC	8	14	kintex-7-3	James Brakef		378		6			252	##	14.7	0.33	1.0	220.2	AX		verilog	3	P16C5x	Y	yes	N	Y	256	4K	Y					2013	2014			
jimmy	https://github.com/kuash		Eduardo Corpeño	Turing	8	8	artix7	James Brakef		382	120				125	##	v23.2	0.33	1.0	108.0	AX		verilog	2	jimmy	Y		N	Y	256	256	Y	16		4		2020	2022		educational, 4 regs, 8-bit adr spaces	vendor neutral source code
bfcpu	http://www.cliff	stable	Clifford Wolf	RISC	8	3	**zu-3e**	James Brakef		387		6			500	##	v21.1	0.02	4.0	6.5	X	B	vhdl	4	cw6671	Y	yes	N	N	64K	64K	Y	8				2003	2003	https://en.wikipe	no accum, data pointer and bracketed	internal 1-byte data cache doubles performanc
gumnut	http://digitaldes	stable	Peter Ashenden	accum	8	18	kintex-7-3	James Brakef		388		6			259	##	14.7	0.33	1.0	220.7	AX		verilog	6	gumnut-rt	Y	asm	N	Y	256	4K	Y			8		2007			see Digital Design: An Embedded Systems Approach Using VHDL	
mocha	https://github.c	stable	Sanjay Gupta	accum	8	8	spartan7	James	missin	390	329	6				##	v23.2	0.33	3.0			Y	vhdl	29	processor	Y	asm	N		64K	64K	Y	31					2018		8-bit microcontroller developed at NIIT University, course materials include full RTL &
8bit-verilog_mcu		stable	Josh Friend	6502	8	8	zu-2e	James	timing	392		6		1	500	##	v20.1	0.33	2.0	210.5	x		verilog	11	cpu					512	512	Y	16				2012	2012		for class project, small data stack	PB clock, students to add features
verilog-6502	https://github.c	stable	Arlet Ottens	PIC16	8	8	kintex-7-3	James Brakef		407		6			200	##	14.7	0.33	4.0	40.6	X		verilog	2	cpu		yes	N	N	64K	64K	Y					2007	2018	http://ladybug.xs4all.nl/arlet/fpga/6502/		
ppx16	https://github.c	stable	Daniel Wallner	PIC16	8	14	kintex-7-3	James	missin	409		6			238	##	14.7	0.33	1.0	192.1	X		vhdl	10	P16C55	Y	yes	N	Y	256	4K	Y					2002	2009		both 16C55 & 16F84	with fake instruction ROM
altium/TSK16S	http://techdocs.proprietar		Altium	Turing	8	12	spartan-3	Altium		416	211	4			50			0.33	2.0	19.8	ALX		proprietary			Y	yes	N	Y	256	4K	Y					2004	2017	CR0140.pdf, CR01	frozen, asm, C, C++, schem, VHDL & V	clock is 50MHz, #s for other fpgas
bfcpu	http://www.cliff	stable	Clifford Wolf	6502	8	3	kintex-7-3	James Brakef		422		6			345	##	14.7	0.01	4.0	2.0	X	B	vhdl	4	cw6671	Y	yes	N	N	64K	64K	Y	8				2003	2003	https://en.wikipe	no accum, data pointer and bracketed	current version & earlier version
mega65	https://github.com/mega		Paul Gardner-Stephen	accum	8	8	spartan7	James	too ma	431	296	6				##	v23.2	0.67	2.0		X	Y	vhdl	114		Y	yes	N	N	64K	64K	Y					2017	2024		Enhanced c65 running in FPGA	very large SOC with many builds & tests
uos	https://opencor	mature	Daniel Roggen	PIC16	8	16	kintex-7-3	James Brakef		441		6			270	##	14.7	0.33	3.0	67.4	X		vhdl	14	cpu	Y								3	4		2014	2017		UoS Educational Processor	inspired by x86 ISA
minirisc	https://opencor	stable	Rudolf Usselmann	6502	8	14	spartan-3	Rudolf Usseln		460		4			80			0.33	1.0	57.4	X		verilog	7	risc_core	Y	yes	N	Y	256	4K	Y					2001	2012			
m65c02	https://opencor	mature	Michael Morris	RISC	8	8	spartan-6	James Brakef		466		6		3	118	##	14.7	0.33	4.0	20.8	X	Y	verilog	13	M65C02	Y	yes	N	N	64K	64K	Y					2013	2020	https://github.cor	also a m65c02a version	micro-coded via F9408 soft sequencer
qs5-rible	http://www.san	stable	John Rible	RISC	8	16	kintex-7-3	James Brakef		468		6			135	##	14.7	0.33	1.0	95.3	X		verilog	1	qs5_mix			N		256	32K	Y					1998	1999		used in his class, also uses eP32	
babyrisc	http://www.san	stable	John Rible	PIC12	8	16	kintex-7-3	James Brakef		468		6			141	##	14.7	0.33	2.0	49.7	X		verilog	1	qs5_mix	Y		N		64K	64K	Y	15		8		1997	1999	http://www.sandp	part of a three class course	memory rd/wt & ALU per clock
synpic12		stable	Miguel Angel Ajo Pelay	6502	8	12	kintex-7-3	James Brakef		474		6		1	197	##	14.7	0.33	1.0	136.8	AX		vhdl	7	synpic12	Y	yes	N	N	256	2K	Y					2011	2011	http://projects.nb	CHDL to verilog	bad weblink
verilog-6502	https://github.c	stable	Arlet Ottens	6502	8	8	**zu-3e**	James Brakef		475	112	6			333	##	v21.1	0.33	3.0	77.2	X		verilog	2	cpu		yes	N	N	64K	64K	Y					2007	2018	http://ladybug.xs4all.nl/arlet/fpga/6502/	sync memory, e.g. use block RAM	
ladybug	https://github.com/Arlet/		Arlet Ottens	6502	8	8	spartan7	James	sparta	476	111	6		4	106	##	v23.2	0.33	4.0	18.4			verilog	2	cpu		yes	N	N	64K	64K	Y						2016	http://ladybug.xs4all.nl/arlet/fpga/6502/		
m65	www.ip-arch.jp/	stable	Naohiko Shimizu	6502	8	8	arria-2	James Brakef		483		A			110	##	q13.1	0.33	4.0	18.8	X		sfl & TI	8	m65cpu	Y	yes	N	N	4K	4K	Y					2001	2002			
mx65	https://github.com/Steve		Steve Teal	6502	8	8	**zu-3e**	James Brakef		485	148	6		1.5	370	##	v21.2	0.33	4.0	63.0	X		vhdl	5	apple1	Y	yes	N		64K	64K	Y					2022	2022		cycle accurate, passes Klaus Dormann 6502 functional tests, has uart	
chip_6502	http://www.aholme.co.uk		Andrew Holme	accum	8	8	spartan7-	James Brakef		514	767	6			200	##	v23.2	0.33	4.0	32.1	X	Y	verilog	5	chip_6502	Y	yes	N		64K	64K	Y					2016		http://www.aholr	cycle accurate generated from transis	also author of two Forth TTL machines
micro8a	http://members	beta	John Kent	6502	8	16	kintex-7	James Brakef		531		6			204	##	14.7	0.33	3.0	42.3	X		vhdl	11	Micro8	Y		N	N	2K	2K	Y					2002	2002	http://members.c	derived from Tim Boscke's mcpu	also micro8 and micro8b variants
t65	https://opencor	stable	Daniel Wallner	6502	8	8	kintex-7-3	James Brakef		575		6			291	##	14.7	0.33	4.0	41.7	AX		vhdl	7	T65	Y	yes	N	N	64K	64K	Y					2002	2010		6502, 65C02 & 65C816; wide use	
bc6502	http://finitron.c	beta	Robert Finch	1802	8	8	**zu-3e**	James	vivado	583		6			286	##	v21.1	0.33	4.0	40.4	X		verilog	18	bc6502		yes	N	N	64K	64K	Y					2012	2012			bare source
cosmac	https://github.c	beta	Eric Smith	8080	8	8	kintex-7-3	James	inferre	598		6		17	87	##	14.7	0.33	1.0	48.0	X	X	vhdl	14	elf	Y	asm	N	N	64K	64K	Y	100		16		2009	2020		uses PIXIE graphics core	modified to use block RAM
vm80a	https://github.c	untested	1801BM1	6502	8	8	cortex-3			607		4			104								verilog												2014	2018		Two versions of Soviet i8080a reverse engineered from silicon die, 607 4LUTs, 104M	
bc6502	http://finitron.c	beta	Robert Finch	picoBlaze	8	8	kintex-7-3	James Brakef		619		6			197	##	14.7	0.33	4.0	26.2	X		verilog	18	bc6502		yes	N	N	64K	64K	Y					2012	2012			bare source
copyblaze	https://opencor	stable	Abdallah Ellbrahimi	6502	8	18	kintex-7-3	James	missin	622		6			217	##	14.7	0.33	2.0	57.5	AX		vhdl	16	cp_copybl	Y	asm	N		256	2K	Y					2011	2016		wishbone extras	
copro6502	https://github.c	stable	David Banks	RISC	8	8	kintex7-3	James	bare c	636	144	6			258	##	14.7	0.33	3.0	44.7	X	Y	vhdl, Verilog		T65	Y	yes			64K	64K	Y					2014	2019	https://stardot.or	65C102	
cpu_takagi	https://github.com/takagi		Masayuki Takagi	accum	8	15	spartan7	James Brakef		643	1017	6			111	##	v23.2	0.67	1.0	115.8	X		verilog	3	cpu					64K	64K	Y	16		16		2016	2016		no use of LUT RAM or block ROM	not much documentation
ez8	https://github.c	stable	Howard Mao	6502	8	16	kintex-7-3	James	replac	644		6		2	233	##	14.7	0.33	2.0	59.6	X		verilog	13	ez8_cpu					256	4K						2014	2014	http://zhehaomao.com/		not sure inferred RAM correct?
free6502	http://web.arch	stable	David Kessner	accum	8	8	kintex-7-3	James Brakef		646	144	6			193	##	14.7	0.33	4.0	24.6	X		vhdl	5	free6502	Y	yes	N	N	64K	64K	Y					1999	2000	http://www.sprov	microcoded	
reflet	https://github.com/Arkae		Maxime Bouillot	RISC	8	16	spartan7	James Brakef		688	411	6			128	##	v24.1	0.67	1.0	124.6	X		verilog	9	reflet_cpu		asm	N		64K	64K				16		2020	2024	https://github.cor	original design, data size adj	most ops between accumulator & register, risc
open8_urisc	https://opencor	stable	Kirk Hays, Jshamlet	MCS-48	8	8	kintex-7-3	James Brakef		691		6	1		263	##	14.7	0.33	1.0	125.6	X		vhdl	9	Open8	Y	yes	N		64K	64K	Y			8		2006	2023		accum & 8 regs, clone of Vautomation uRISC processor, in use	
t48	https://opencor	stable	Arnim Laeuger	accum	8	8	cyclone-1	Arnim Laeuge		738		4		1	59			0.33	4.0	6.6	AX		vhdl	70	t48_core	Y	asm	N		256	1K						2004	2022		T48 uController	used in several projects
inst_list_proce	https://opencor	planning	Mahesh Palve	MISC	8	15	kintex-7-3	James	using x	786		6		1	340	##	14.7	0.33	1.0	142.6	X		verilog	34	top	Y		N		128	1K		32				2014			pipelined, state machine	UART, SPI & timer included
dragonfly	http://www.leo	beta	LEOX team	6502	8	16	kintex-7-3	James Brakef		788		6			164	##	14.7	0.33	1.0	68.6	X		vhdl	6	dgf_core	Y	asm	N	Y	256	2K	Y	42	6	7		2001	2003		unusual, uses FIFOs	
ag_6502	https://opencor	beta	Oleg Odintsov	6805	8	8	kintex-7-3	James Brakef		824	105	6			176	##	14.7	0.33	4.0	17.7	ALX		verilog	2	ag_6502		yes	N	N	64K	64K	Y					2012	2012		verilog code generation, "phase level accurate"	
system05	https://opencor	beta	John Kent, David Burn	Z80	8	8	kintex-7-3	James Brakef		834		6			204	##	14.7	0.33	4.0	20.2	X	Y	vhdl	10	System05	Y	yes	N	N	64K	64K	Y					2003	2009	http://members.op	tushome.com.au/jekent/	
nextz80	https://github.com/RyuK	stable	Nicolae Dumitrache	6502	8	8	kintex-7-3	James Brakef		854		6			119	##	14.7	0.33	1.0	46.0	X	B	verilog	3	NextZ80C	Y	yes	N	N	64K	64K	Y					2011	2019			claim of 700 LUTs in Spartan-3 probably wrong
v6502	https://github.com/RyuKo		Ryu Kojiro	risc-v	8	8	**zu-3e**	James Brakef		868	131	6			250	##	v21.1	0.33	3.0	31.7	X		vhdl	23	v6502	Y	yes	N	N	64K	64K	Y					2019	2020	https://opencores	6502 with extras: 16-bit stack pointer	www.youtube.com/watch?v=K3jH-f_r80E
verilogboy	https://hackada	alpha	Wenting Zhang	VLIW	8	8	**zu-3e**	James Brakef		872	608	6			313	##	v21.1	1.00	3.0	119.5	X		verilog	36	vbh	Y	yes	N	N	64K	64K	Y						2019	https://github.cor	Game Boy in Verilog, both CPU (SM83	uses riscv_picorv32 core
tinyvliw8	https://opencor	alpha	Oliver Stecklina	68HC11	8	32	kintex-7-3	James	hacked	895		6			149	##	14.7	0.33	1.0	55.0	X		vhdl	19	sysarch			N	Y	256	1K	Y					2013	2020		tinyVLIW8 soft-core processor	bare core, Altera LPM for RAMs
gup	https://opencor	stable	Kevin Phillipson	RISC	8	8	arria-2	James Brakef		925		A	1	1	127	##	q13.1	0.33	4.0	11.3	A		vhdl	25	gator_upr	Y	yes	N	N	64K	64K	Y					2008	2011	https://www.mil.t	top level is schematic	
ucpuvhdl	https://github.c	stable	Reed Foster	PIC18	8	16	kintex-7-3	James	512 LU	933		6			118	##	14.7	0.33	2.0	20.8	X		vhdl	29	core	Y	asm	N		256	64K	Y	12	2	7		2016	2017	https://github.cor	six tutorials on uCPUvhdl	using muCPUv2_1 of 3 upwards compatible de
ae18	https://opencor	beta	Shawn Tan	RISC	8	16	**zu-3e**	James	vivado	954	501	6			208	##	v21.1	0.33	1.0	72.1	ALX		verilog	1	ae18_core		yes	N	Y	4K	1M						2003	2009	https://hackaday.	not 100% compatable	negative edge reset "clock"
fluid_core	https://opencor	alpha	Stephen Nolting	AVR	8	12	kintex-7-3	James Brakef		956		4			381	##	14.7	0.33	1.0	131.7	X		verilog	17	FluidCore			N	Y						8		2015	2020	https://www.allat	data width adj., mem sizes adj.	2020 version requires registration
navre	https://opencor	stable	Sebastien Bourdeaudu	8051	8	16	kintex-7-3	James Brakef		990		6			207	##	14.7	0.33	1.0	69.0	ALX		verilog	1	softusb_n	Y	yes	N		64K	64K	Y	72		32	2	2010	2013	https://www.milk	AVR clone, part of www.milkymist.org	
light52	https://opencor	beta	Jose Ruiz	8051	8	8	kintex-7-3	James Brakef		1022		6	1	1	154	##	14.7	0.33	6.0	8.3	AX	Y	vhdl	8	light52_m	Y	yes	N	N	64K	64K	Y					2012	2018		targeted to balanced	~ 6 clocks/inst
r8051	https://github.c	stable	Li Xinbing	RISC	8	8	kintex-7-3	James Brakef		1031		6	1		139	##	14.7	0.33	4.0	11.1	X		verilog	2	r8051	Y	yes	N	N	64K	64K	Y					2015	2019			
8bit_piped_pro	https://opencor	stable	Mahesh Sukhdeo Palve	6502	8	16	kintex-7-3	James	swapp	1049		6		1	370	##	14.7	0.33	1.0	116.4	X		verilog	28	top	Y								20		16		2013	2017	https://github.cor	uses Perl as assembler	use Perl to generate ROM file
pet_fpga	https://github.c	stable	Thomas Skibo	6502	8	8	kintex-7-3	James Brakef		1052		6			242	##	14.7	0.33	4.0	19.0	X		verilog	1	cpu6502	Y	yes	N	N	64K	64K	Y					2007	2011	https://github.cor	for Commodore PET	
mx65	https://github.com/Steve		Steve Teal	6502	8	8	**k7-3**	James	512 LU	1071	195	6		0.5	207	##	14.7	0.33	4.0	15.9	X		vhdl	5	apple1	Y	yes	N		64K	64K	Y					2022	2022		cycle accurate, passes Klaus Dormann 6502 functional tests, has uart	
sbc6502	https://github.com/daven		Dave Nardella	PIC18	8	8	artix7	James	was m	1074	382	6		12	42	##	v23.2	0.80	1.0	31.3	AGX	Y	verilog	19	top	Y	yes	N		256	256	Y					2024	2024	https://www.linke	linked in page has full description	web page also has soft 6502 for Gowin, Xilinx &
ae18	https://opencor	beta	Shawn Tan	6805	8	16	arria-2	James Brakef		1084		A	1		207	##	q13.1	0.33	1.0	63.1	AX		verilog	1	ae18_core		yes	N	Y	4K	1M						2003	2009	https://hackaday.	not 100% compatable	negative edge reset "clock"
68hc05	https://opencor	stable	Ulrich Riedel	6805	8	8	**zu-3e**	James	vivado	1106	117	6			485	##	v21.1	0.33	4.0	36.2	X		vhdl	1	6805		yes	N	N	64K	64K	Y					2007	2009			68c05 & 68c08 very different Fmax
68hc05	https://opencor	stable	Ulrich Riedel	AVR	8	8	kintex-7-3	James Brakef		1112		6			300	##	14.7	0.33	4.0	22.2	X		vhdl	1	6805		yes	N	N	64K	64K	Y					2007	2009			
xmega_core	https://opencor	beta	Gheorghiu Iulian	8080	8	16	kintex-7-3	James Brakef		1116		6			120	##	14.7	0.33	1.0	35.6	X		verilog	34	mega_cor	Y	yes	N		64K	128K	Y	72		32		2017	2018	https://git.morgot	8 AVR cores, 4 sets LUT counts poste	https://git.morgothdisk.com/VERILOG/VERILO
cpu8080	https://opencor	stable	Scott Moore	Z80	8	8	kintex-7-3	James Brakef		1179		6			299	##	14.7	0.33	9.0	9.3	X		verilog	1	m8080	Y	yes	N	N	64K	64K	Y					2006	2016		includes VGA display generator, three variants	
a-z80	https://opencor	stable	Goran Devic	Z80	8	8	kintex-7-3	James Brakef		1186		6			24	##	14.7	0.33	1.0	6.8	AX		verilog	24	z80_top_d	Y	yes	N	N	64K	64K	Y					2014	2020	https://github.cor	gate level reverse eng'd Z80	Complete implementation of a Sinclair ZX Spec
tv80	https://opencor	mature	Guy Hutchison, Howar	PIC16	8	8	kintex-7-3	James Brakef		1207		6			182	##	14.7	0.33	3.0	16.6	AX		verilog	6	tv80n	Y	yes	N	N	64K	64K	Y					2004	2020	https://github.cor	derived from Daniel Wallner's T80, AS	ASIC implementations
m16c5x	https://opencor	mature	Michael Morris	68HC11	8	14	spartan-3	Michael Morr		1217		4		3	60	##		0.33	1.0	16.3	X	Y	verilog	3	m16C5x	Y	yes	N	Y	256	4K	Y					2013	2014		SOC LUT count	
system11	https://opencor	alpha	John Kent, David Burn	6502	8	8	kintex-7-3	James Brakef		1218		6			153	##	14.7	0.33	4.0	10.3	X	Y	vhdl	17	cpu11	Y	yes	N	N	64K	64K	Y					2003	2009	http://members.c	known bugs & untested instructions	
apple2fpga	http://www.cs.c	stable	Stephen A Edwards	AVR	8	8	**zu-3e**	James	vivado	1238	706	6		7	195	##	v21.1	0.33	4.0	13.0	AX	Y	vhdl	19	de2_top	Y	yes	N	Y	64K	64K	Y					2007	2022		emulation of Apple II computer	replaced Altera PLL with stub
avrtinyx61core	https://opencor	beta	Andreas Hilvarsson	8080	8	16	kintex-7-3	James Brakef		1243		6			194	##	14.7	0.33	1.0	51.5	X		vhdl	1	mcu_core		yes	N		64K	128K	Y	72		32		2008	2009			
ep8080	https://github.c	beta	C.H. Ting	AVR	8	8	kintex-7-3	James Brakef		1276		6			184	##	14.7	0.33	9.0	5.3	X		vhdl	4	ep80	Y	yes	N	N	64K	64K	Y					2002	2016	8080 data sheets	initialized Lattice memory blocks	work related to eP16
attiny_atmega	https://opencor	beta	Gheorghiu Iulian	Z80	8	16	**zu-3e**	James Brakef		1366	116	6			179	##	v21.1	0.33	1.0	43.1	X	Y	verilog	9	mega_cor	Y	yes	N		64K	128K	Y	72		32		2018	2019	https://git.morgot	configurable AVR processor w/8 configurations	
t80	https://opencor	stable	Daniel Wallner	6801	8	8	kintex-7-3	James	Z80 m	1389		6			163	##	14.7	0.33	3.0	12.9	X		vhdl	5	T80a	Y	yes	N	N	64K	64K	Y					2002	2018		Z80, 8080 & gameboy inst sets, several usages	
hd63701	https://opencor	planning	Tsuyoshi Hasegawa	6502	8	8	spartan-6	James Brakef		1412		6	1	3	31	##	14.7	0.33	4.0	1.8	X		verilog	6	HD63701_CORE		N	N	N	64K	64K	Y					2014			Used in Atari game console, 6801 clone?	
apple2fpga	http://www.cs.c	stable	Stephen A Edwards	8051	8	8	kintex7-3	James Brakef		1416	654	6		8.5	159	##	14.7	0.33	4.0	9.2	AX	Y	vhdl	19	de2_top	Y	yes	N	Y	64K	64K	Y					2007	2022		emulation of Apple II computer	replaced Altera PLL with stub
8051	https://opencor	alpha	Simon Teran, Jakas	6809	8	8	**zu-3e**	James	area o	1424	645	6			242	##	v21.1	0.33	4.0	14.0	ALX		verilog	32	oc8051_to	Y	yes	N		64K	64K	Y					2001	2016		8051 core includes several on-chip peripherals, like timers and counters	
turbo9	https://github.c	WIP	Kevin Phillipson	6809	8	8	artix-7	James	no tim	1428	530	6		8	112	##	v23.2	0.33	3.0	8.6	X	Y	verilog	96	soc_top_g	Y	yes	N		64K	64K	Y	44	13	8	6		2024	https://hackaday.	Compact & Efficient Pipe'd 6809 uP IP	masters thesis, full testbench, ucoded
turbo9	https://github.c	WIP	Kevin Phillipson	Z80	8	8	artix-7	Kevin Phillips		1464	505	6		8	112	##	v22.2	0.33	3.0	8.4	X	Y	verilog	96	soc_top_g	Y	yes	N		64K	64K	Y	44	13	8	6		2024	https://www.yout	competes well against other 8-bitters	four videos, see github page
z80control	https://opencor	alpha	Tyler Pohl	RISC	8	8	kintex-7-3	James Brakef		1483		6			189	##	14.7	0.33	3.0	14.0	X	Y	verilog	6	top_de1	Y	yes	N	N	64K	64K	Y					2010	2012		Microprocessor targeting embedded	interfaces to DRAM, based on T80 core
8bit_piped_pro	https://opencor	stable	Mahesh Sukhdeo Palve	6801	8	16	**zu-3e**	James	vivado	1500	1822	6		1	500	##	v21.1	0.33	1.0	110.0	X		verilog	28	top	Y								20		16		2013	2017	https://github.cor	uses Perl as assembler	use Perl to generate ROM file

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data	sz	inst sz	FPGA	repor ter	com ents	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	ven dor	SOC	src code	#src files	top file	doc	tool chai	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
system6801	https://opencor	stable	Michael L. Hasenfratz	8080	8	8		cyclone-3	James	Brakef	1507		4		3	73	##	14.7	0.33	4.0	4.0	A		vhdl	15	wb_cyclor	Y	yes	N	N	64K	64K	Y				2003	2009	http://members.c	based on John Kent's 6801	tested on Apex20K, Cyclone & Straix boards
i8080-vhdl	https://github.com/bfenn		Brendan Fennell	6809	8	8		kintex7	James	Brakef	1508	308	6			124	##	14.7	0.33	8.0	3.4			vhdl	14	cpu8080_	Y	yes	N		64K	64K	Y					2018		implemented invaders game	
coco3fpga	https://github.c	mature	Gary Becker	AVR	8	8		spartan7	James	Kent's	1536	195	6			78	##	v23.2	0.33	3.0	5.6	X		verilog	39	cpu09l_12	Y	yes	N		64K	64K		44	13	8	2007	2015	http://www.dave	uses John Kent's 6809 & adds color c	altera project with 6809 & 6502 uPs
ax8	https://opencor	stable	Daniel Wallner	AVR	8	16		spartan-6	James	missin	1549		6		1	213	##	14.7	0.33	1.0	45.3	X		vhdl	14	A90S1200		yes	N		64K	128K	Y	72		32	2002	2010		both A90S1200 & A90S2313	inserted fake inst ROM
avr_hp	https://opencor	stable	Strauch Tobias	6809	8	16		kintex-7-3	James	2 slot	1554		6			223	##	14.7	0.33	1.0	47.4	X		vhdl	10	avr_core_bm	Y	yes	N		64K	128K	Y	72		32	2010	2012		hyper pipelined (eg barrel) AVR	
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	6809	8	8		**spartan7-**	James	vivado	1592	366	6			100	##	v23.2	0.33	3.0	6.9	ALX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y				2012	2015		6309 op-codes not implemented	does not match timing results of zynq+
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	AVR	8	8		**kintex-u3**	James	vivado	1595	367	6			200	##	v23.2	0.33	3.0	13.8	ALX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y				2012	2015		6309 op-codes not implemented	does not match timing results of zynq+
avr_fpga	https://opencor	stable	Juergen Sauermann	AVR	8	16		**zu-3e**	James	Brakef	1606		6	1	6		##	v21.1	0.33	1.0		X		vhdl	20	cpu_core	Y	yes	N		64K	128K	Y	72		32	2009	2010		extended lecture on FPGA uP design	
avr_fpga	https://opencor	stable	Juergen Sauermann	6803	8	16		kintex-7-3	James	Brakef	1606		6	1	6	120	##	14.7	0.33	1.0	24.7	X		vhdl	20	cpu_core	Y	yes	N		64K	128K	Y	72		32	2009	2010		extended lecture on FPGA uP design	
mc6803	https://opencor	stable	Dukov	AVR	8	8		spartan7	James	Brakef	1618	1223	6			83	##	v23.2	0.33	3.0	5.7	X		system	2	mc6803	Y	yes	N	N	64K	64K	Y				1999			based on System68 and System01 by	John E. Kent, translated CPU core from VHDL to
avr_core	https://opencor	stable	Rusian Lepetenok	6809	8	16		**zu-3e**	James	Brakef	1624	519	6			250	##	v21.1	0.33	1.0	50.8	X		verilog	70	avr_core	Y	yes	N		64K	128K	Y	72		32	2002	2017		VHDL core also	
system09	https://opencor	stable	John Kent, David Burn	6809	8	8		kintex-7-3	James	Brakef	1631		6		41	88	##	14.7	0.33	3.0	6.0	AX	Y	vhdl	40	cpu09l	Y	yes	N	N	64K	64K	Y	44	13	8	2003	2021	http://members.c	from John Kent web page	opencores download URL incorrect, use col E
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	6502	8	8		**kintex-u3**	James	vivado	1656	367	6			185	##	v23.2	0.33	3.0	12.3	ALX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y				2012	2015		6309 op-codes not implemented	does not match timing results of zynq+
cpu6502_true	https://opencor	stable	Jens Gutschmidt	6809	8	8		kintex-7-3	James	Brakef	1678		6			159	##	14.7	0.33	4.0	7.8	X		vhdl	7	r6502_tc		yes	N	N	64K	64K	Y				2008	2024		cycle accurate	web page update only
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	6805	8	8		arria-2	James	Brakef	1680		6		A	145	##	q18.0	0.33	3.0	9.5	ALX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y	44	13	8	2012	2015		6309 op-codes not implemented	
df6805	www.hitechglot	proprietar	Hitech Global	6502	8	8		stratix-1	Hitech	Global	1690		4			83			0.33	4.0	4.1	A		proprietary			Y	yes	N	N	64K	64K	Y						6805 data sheets		
v65c816	https://github.com/RyuKo		Valerio Venturi	8051	8	8		cyclone-IV	Valerio	Ventu	1693		4			25			0.33	3.0	1.6	A		vhdl	26	v6502	Y	yes	N	N	64K	64K	Y				2011	2023	https://opencores	6502 with extras: 16-bit stack pointer	https://www.youtube.com/watch?v=K3jH-
dp8051	https://www.dc	proprietar	Digital Core Design	6809	8	8		kintex-7-3	Digital	Core D	1699		6			200	##	14.7	0.30	1.0	35.3	ALX		proprietary			Y	yes	N		64K	64K					1999	1999		also PIC, HC11, 68000, 680x, d32pro	full system with RAM
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	6809	8	8		stratix-5	James	Brakef	1711		A			133	##	q14.0	0.33	3.0	8.6	ALX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y	44	13	8	2012	2015		6309 op-codes not implemented	
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	8051	8	8		**zu-3e**	James	vivado	1716	367	6			370	##	v21.1	0.33	3.0	23.7	ALX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y				2012	2015		6309 op-codes not implemented	does not match timing results of zynq+
8051	https://opencor	alpha	Simon Teran, Jakas	Z80	8	8		kintex-7-3	James	tunrec	1744	617	6	1		111	##	14.7	0.33	4.0	5.3	ALX		verilog	32	oc8051_to	Y	yes	N		64K	64K	Y				2001	2016		8051 core includes several on-chip	peripherals, like timers and counters
a-z80	https://opencor	stable	Goran Devic	8051	8	8		**zu-3e**	James	timing	1761	365	6			41	##	v21.1	0.33	1.0	7.7	AX		verilog	24	z80_top_(	Y	yes	N	N	64K	64K	Y				2014	2020	https://github.cor	gate level reverse eng'd Z80	Complete implementation of a Sinclair ZX Spec
cast_8051	http://www.cas	proprietar	CAST Inc	Z80	8	8		virtex-6	CAST I	820 sli	1800		6		2	81	##	12.1	0.33	3.0	5.0	X		proprietary			Y	yes	N		64K	64K	Y			32			http://www.cast-i	Cast has uP related IP	several versions, FPGA kits
a-z80	https://opencor	stable	Goran Devic	avr	8	8		spartan-6	Goran	Devic	1819		6		8		##	14.7	0.33	1.0		AX		verilog	24	z80_top_(	Y	yes	N	N	64K	64K	Y				2014	2020	https://github.cor	gate level reverse eng'd Z80	Complete implementation of a Sinclair ZX Spec
avr_cpu	https://github.com/nanar		nanamake Nanamaru	6808	8	16		**cyclone4**	nanamake	Na	1845	520	4	1		64	##	q14.0	0.33	1.0	11.4	A		verilog			Y	yes	N		64K	128K	Y	72		32		2018		quartus project & report files	2nd version with data & prog mems
68hc08	https://opencor	stable	Ulrich Riedel	AVR	8	8		**zu-3e**	James	vivado	1875	128	6			164	##	v21.1	0.33	4.0	7.2	X		vhdl	1	x68ur08		yes	N	N	64K	64K	Y				2007	2009			68c05 & 68c08 very different Fmax
avr_fpga	https://opencor	stable	Juergen Sauermann	AVR	8	16		**zu-3e**	James	Brakef	1877		6	1	6		##	v21.1	0.33	1.0		X	Y	vhdl	20	avr_fpga	Y	yes	N		64K	128K	Y	72		32	2009	2010	https://fr.wikivers	extended lecture on FPGA uP design	missing module in atmega8_pong_vga
avr_fpga	https://opencor	stable	Juergen Sauermann	8051	8	8		kintex-7-3	James	Brakef	1877		6	1	6	115	##	14.7	0.33	1.0	20.2	X	Y	vhdl	20	avr_fpga	Y	yes	N		64K	128K	Y	72		32	2009	2010	https://fr.wikivers	extended lecture on FPGA uP design	missing module in atmega8_pong_vga
altium/TSK51A	http://techdocs.p	proprietar	Altium	8051	8	8		spartan-3	Altium		1890	482	4		1	50			0.33	6.0	1.5	ALX		proprietary			Y	yes	N	N	64K	64K	Y				2004	2017	CR0140.pdf, CR01	frozen, asm, C, C++, schem, VHDL & V	clock is 50MHz, #s for other fpgas
t51	https://opencor	stable	Andreas Voggeneder	6809	8	8		kintex-7-3	James	Brakef	1942		6	1		147	##	14.7	0.33	4.0	6.2	AX		vhdl	17	T8032	Y	yes	N	N	64K	64K	Y				2002	2010		8052 & 8032	8032 SoC
copro6502	https://github.c	stable	David Banks	8051	8	8		kintex7-3	James	bare c	1958	206	6			107	##	14.7	0.33	3.0	6.0	X	Y	vhdl, Verilog		cpu09	Y	yes			64K	64K	Y				2014	2019	https://stardot.or	6809	
i8051	https://github.c	stable	Tony Givargis	8051	8	8		spartan7	James	see da	1960	1339	6		0.5	48	##	v24.1	0.33	4.0	2.0	X		vhdl	9	i8051_all	Y	yes	N		64K	64K	Y				1999	2016	https://ics.uci.edu	author has book & course	Embedded System Design: A Unified Hardware
turbo8051	https://opencor	beta	Dinesh Annayya	8051	8	8		kintex-7-3	James	Brakef	1985		6	1		127	##	14.7	0.33	4.0	5.3	AX		verilog	74	oc8051_to	Y	yes	N	N	64K	64K	Y				2011	2016		includes peripherials	
oms8051mini	https://opencor	alpha	Simon Teran, Dinesh A	6809	8	8		kintex-7-3	James	Brakef	1991		6	1	32	133	##	14.7	0.33	5.0	4.4	X	Y	verilog	66	digital_co	Y	yes	N		64K	64K	Y				2000	2018			
6809_6309	https://opencor	beta	Alejandro Paz Schmidt	Z80	8	8		kintex-7-3	James	Brakef	1996	370	6			175	##	14.7	0.33	3.0	9.7	ALX	B	verilog	5	MC6809_(	Y	yes	N	N	64K	64K	Y	44	13	8	2012	2015		6309 op-codes not implemented	
wb_z80	https://opencor	stable	Brewster Porcella	accum	8	8		kintex-7-3	James	Brakef	2025		6			144	##	14.7	0.33	3.0	7.8	X		verilog	4	z80_core_	Y	yes	N	N	64K	64K	Y				2004	2012		derived from Guy Hutchison TV80	Wishbone High Performance Z80
kiwih	https://github.com/kiwih		Hammond Pearce	Z80	8	8		arria-7	James	no LUT	2030	2167	6			90	##	v23.2	0.20	1.0	8.9	X		verilog	14	accumulat	Y	asm	N		256	256	Y	24				2023	https://efabless.c	uP design via chatGPT4, ASIC gate list	Scan (JTAG) chain of all memory & FF
a-z80	https://opencor	stable	Goran Devic	AVR	8	8		cyclone-2	Goran	Devic	2084		4		29	19	##	q11.1	0.33	1.0	3.0	AX		verilog	24	z80_top_(	Y	yes	N	N	64K	64K	Y				2014	2020	https://github.cor	gate level reverse eng'd Z80	Complete implementation of a Sinclair ZX Spec
avr_core	https://opencor	stable	Rusian Lepetenok	68HC11	8	16		kintex-7-3	James	Brakef	2135		6			127	##	14.7	0.33	1.0	19.7	X		verilog	15	avr_core	Y	yes	N		64K	128K	Y	72		32	2002	2017		VHDL core also	
hc11core	http://www.gm	stable	Green Mountain Comp	6502	8	8		kintex-7-3	James	Brakef	2190		6			127	##	14.7	0.33	4.0	4.8	X		vhdl	1	hc11rtl	Y	yes	?	N	64K	64K	N	53		8	2	2000		6811 data sheets	restricted use license, with corrections	
fpga-64	http://www.syn	stable	Peter Wendrich	6801	8	8		kintex-7-3	James	Brakef	2210		6		2	156	##	14.7	0.33	4.0	5.8	X	Y	vhdl	26	fpga64_co	Y	yes	N	N	64K	64K	Y			26		2005	2008			Rendition of Commodore 64	altera top level schematic
system68	https://opencor	stable	John Kent, David Burn	6808	8	8		spartan-3	James	Brakef	2235		4		4	46	##	14.7	0.33	4.0	1.7	X	Y	vhdl	21	cpu68	Y	yes	N	N	64K	64K	Y				2003	2009	http://members.o	ptushome.com.au/jekent/	
68hc08	https://opencor	stable	Ulrich Riedel	6809	8	8		kintex-7-3	James	Brakef	2290		6			101	##	14.7	0.33	4.0	3.6	X		vhdl	1	x68ur08		yes	N	N	64K	64K	Y				2007	2009			
jtkcpu	https://github.com/JTFPG		Jose Tejada Gomez	8051	8	8		cyclone3	Jose	Tejada G	2290		4	3		70	##	q18.0	0.33	3.0	3.4	A		verilog	12	jtkcpu	Y	yes	N	N	64K	64K	Y	44	13	8	2023	2024	https://forums.ar	gaming uP, compatible with Konami's	docs have ISA comparison 6809/6309/this
pulserain	https://github.c	stable	PulseRain Tech LLC	SM83	8	8		arria-2	James	some	2376		A	2	41	130	##	q18.0	0.33	3.0	6.0	A		system	25	FP51_fast	Y	yes	N	Y	64K	64K	Y				2017	2018	https://www.puls	1 clk/inst, intended for Max10	
verilogboy	https://hackada	alpha	Wenting Zhang	Z80	8	8		**zu-3e**	James	Brakef	2415	1601	6		4	238	##	v21.1	0.33	3.0	10.8	X	Y	verilog	22	boy	Y	yes	N	N	64K	64K	Y					2019	https://github.cor	Game Boy in Verilog, both CPU (SM83	also https://github.com/neildryan/GBA
z80soc	https://opencor	stable	Ronivon Costa	Z80	8	8		spartan3e	James	Brakef	2474		4	2	19	78	##	14.7	0.33	3.0	3.4	AX	Y	vhdl	19	top_s3e	Y	yes	N	N	64K	64K	Y				2008	2016		based on Daniel Wallner's T80	directory disappeared
y80e	https://opencor	stable	Sergey Belyashov	Z80	8	8		cycone-3	Sergey	Belyas	2557		4				##	14.7	1.00	3.0				verilog	15	top_level	Y	yes	N	N	64K	64K	Y				2013	2019		Y80e - Z80/Z180 compatible processc	based on Y80 from "Microprocessor Design Us
altium/TSK80x	http://techdocs.p	proprietar	Altium	Z80	8	8		spartan-3	Altium		2558	300	4			50			0.33	3.0	2.2	ALX		proprietary			Y	yes	N	N	64K	64K	Y				2004	2017	CR0140.pdf, CR01	frozen, asm, C, C++, schem, VHDL & V	clock is 50MHz, #s for other fpgas
socz80	http://sowerbut	stable	Will Sowerbutts	AVR	8	8		spartan-6	James	constr	2568		6		15	93	##	14.7	0.33	3.0	4.0	X		vhdl	25	top_level	Y	yes	N	N	64K	64K	Y				2013	2014		based on Daniel Wallner's T80, for Papillio Pro board	
pavr	https://opencor	alpha	Doru Cuturela	accum	8	16		kintex-7-3	James	Brakef	2630		6		1	132	##	14.7	0.33	1.0	16.5	X		vhdl	18	pavr_cont	Y	yes	N	Y	4K	4M	Y	72		32	6	2003	2009		superset of AVR	
c88	https://github.c	alpha	Daniiel Bailey	8051	8	8		spartan-3	James	Dff ge	2664		4	2		54	##	14.7	0.33	1.0	6.7	X		vhdl	25	C88	Y	asm	N		8	256	Y	10		8	2015	2015	https://www.yout	only 8 memory locations	used 3785 Dff, doesn't infer block or LUT RAM
i8051	https://github.c	stable	Tony Givargis	8051	8	8		kintex-7-3	James	see da	2690	1325	6	1	0.5	105	##	14.7	0.33	4.0	3.2	X		vhdl	9	i8051_all	Y	yes	N		64K	64K	Y				1999	2016	https://github.cor	author has book & course	Embedded System Design: A Unified Hardware
dalton_8051	www.cs.ucr.edu	stable	Tony Givargis	AVR	8	8		kintex-7-3	James	see i80	2725	1350	6	1	0.5	105	##	14.7	0.33	1.0	12.7	X		vhdl	7	i8051_all	Y	yes	N		64K	64K	Y				1999	2003	https://ics.uci.edu	ASIC	
atmega8_pong	https://fr.wikive	stable	Juergen Sauermann	AVR	8	16		spartan-3	James	clock c	2767		4	1	10	53	##	14.7	0.33	1.0	6.3	X	Y	vhdl	37	avr_fpga_	Y	yes	N		64K	64K	Y	17		4	2017	2017		several projects using avr core	uses Sauermann core
atmega8_pong	https://fr.wikive	stable	Juergen Sauermann	8051	8	16		spartan-3	James	clock c	2898		4	1	11	53	##	14.7	0.33	1.0	6.0	X	Y	vhdl	37	pacman_f	Y	yes	N		64K	64K	Y	17		4	2017	2017		several projects using avr core	uses Sauermann atmega16 core
mc8051	http://www.ore	stable	Helmut Mayrhofer	accum	8	8		kintex-7-3	James	Brakef	3022		6	1		83	##	14.7	0.33	4.0	2.3	X		vhdl	49	mc8051cc	Y	yes	N	N	256	64K	Y				1999	2013	www.oreganosyst	fast 8051, version available with floati	ng-point by David Lundgren
c88	https://github.c	alpha	Daniiel Bailey	x86	8	8		kintex-7-3	James	Brakef	3088		6	2		167	##	14.7	0.33	2.0	8.9	X		vhdl	25	C88	Y	asm	N		8	256	Y	10		8	2015	2015	https://www.yout	only 8 memory locations	used 3658 Dff, doesn't infer block or LUT RAM
i8086up	https://github.com/fallah		Ali Fallah	RISC	8	8		spartan3	Ali	Fallah	3132	529	4	1	12	98	##	14.7	0.67	4.0	5.2	X	Y	vhdl	8	processor	Y	yes	N		512	64K	Y			7		2019		simple x86 with VGA, SD, uart	case stmt, one branch per inst, xilinx IP
jca		stable	John Cronin	x86	8	32		kintex-7-3	James	replac	3287		6	3	3	157	##	14.7	0.33	1.0	15.8	AX	Y	verilog	17	soc										16					has VGA controller, plays Pong	altera memories
cpu86	http://www.ht-l	beta	Hans Tiggeler	accum	8	8		kintex-7-3	James	Brakef	3421		6	1		127	##	14.7	0.17	2.0	3.1	X		vhdl	23	cpu86_top	Y	yes	N	N	1M	1M	Y				2002	2018	http://www.ht-lat	8088 clone	ht-labs offers several uP cores
mycpu	http://www.my	mature	Dennis Kuschel	CISC	8	8		kintex-7-3	James	Brakef	3428		6	1		155	##	14.7	0.33	3.0	5.0	X		vhdl	28	cpu_top	Y		N		64M	64M	Y				2010	2023	http://mynor.org/	originally in TTL, avail. as a kit	my4th: micro-coded, bit serial, runs Forth
z3	https://opencor	stable	Charles Cole	cisc	8	8		arria-2	James	Brakef	3495		A	2		141	##	q18.0	0.33	3.0	4.4	A		verilog	3	boss	Y				128K	128K					2014	2014	https://en.wikipe	Infocom Z-Machine V3, youtube vide	http://inform-fiction.org/zmachine/standards/
m2cpu	https://github.com/ZakSN		Zakary Nafziger	6809	8	8		max10	Zakary	Nafzig	3504	1058	4		56	106	##	q22.1	0.33	6.0	1.7	A		vhdl	27	m2cpu_to	Y	asm	N		64K	64K	Y	75	4	7	2016	2018		micro-coded 8-bitter with 75 instruct	Quartus project files, vga output
rf6809	https://opencores.org/pr		Robert Finch	6809	8	8		artix-7	Robert	Finch	4200		6		4	120	##	v21.2	0.33	4.0	2.4	X	Y	system	21	rf6809	Y	yes	N		16M	16M	Y	44	13	8	2022	2024	http://www.finitr	Different from rtf6809: 24-bit adrs, o	8-bit version, has inst. Cache
mc6809	https://github.c	stable	Greg Miller	6502	8	8		spartan6	James	errors	4510	454	6				##	v23.2	0.33	3.0		X		verilog	6	demo_roo	Y	yes	N	N	64K	64K	Y	44	13	8	2016	2020	https://shop.trenz	Cycle Accurate MC6809 Core	emphasis on cycle accuracy, DIP replacement
cpu65c02_true	https://opencor	stable	Jens Gutschmidt	6502	8	8		spartan-6	James	latch v	4794		6			47	##	14.7	0.33	4.0	0.8	X		vhdl	8	core		yes	N	N	64K	64K	Y				2008	2018		cycle accurate	
lattice6502	https://opencor	beta	Ian Chapman	Z8	8	8		kintex-7-3	James	Brakef	4942		6			214	##	14.7	0.33	4.0	3.6	X		vhdl	3	ghdl_proc	Y	yes	N	N	64K	64K	Y				2010	2010		targeted to LCMXO2280	
fpz8	https://opencor	stable	Fabio Pereira	6809	8	8		cyclone-4	James	Brakef	5184		4	1	16		##	14.7	0.33	4.0		A		vhdl	4	fpz8_cpu	Y		N	Y	2K	16K	Y				2016	2016		Zilog Z8 encore (eZ8) 8-bit core	Altera megafunctions (mem)
rtf6809	https://github.c	alpha	Robert Finch	Z80	8	8		kintex-7-3	James	many	7506		6	1	2	106	##	14.7	0.33	4.0	1.2	X		verilog	4	rtf6809	Y	yes	N	N	64K	64K	Y	44	13	8	2012	2015	http://www.finitr	6809 with 32-bit "FAR" addressing	see also rf6809 variant
reverse-u16	https://github.c	stable	A.T.	vect	8	8		cylcone-4	James	Brakef	11224		4		60		##	14.7	0.33	4.0		X	Y	vhdl	29	zxpoly	Y	yes	N	N	64K	64K	Y				2015			SOC project using T80, HDMI generat	retro Z80 based on T80 by Daniel Wallner
mxp	http://vectorblo	stable	VectorBlox Computing	risc	8			zynq45-7	vectorblox		39856		6	64	81	175	##	v17.2	1.00	0.1	35.1			proprietary			Y										2012	2017	http://www.ece.u	MXP Matrix Processor is a scalable so	LUT count for 8 lanes with custom inst
nanoprocessor	https://github.com/yasan		Yasantha Niroshan	accum	4	12		artix7	James	no LUT	37	50	6			254	##	v24.1	0.10	1.0	687.2	X		vhdl	5	nanoproc	Y		N			8		4			2024			educational: 4 insts MOV, ADD, NEG & JZR	
nibblercpu	https://gist.github.com/er		erin candescent	accum	4	8		spartan7	James	Brakef	39	27	6			200	##	v23.2	0.16	2.0	410.3			vhdl	1	nibblercpu	Y		N	Y	4K	4K					2014	https://www.bign	4-bit CPU in VHDL	seondary web link has documentation
lem4_9	https://opencor	beta	James Brakefield	accum	4	9		kintex-7-3	James	1 stage	144		6		1	195	##	14.5	0.16	1.0	216.7	AX		vhdl	2	lem1_9	Y		N	Y	32	2K	N	24			1	2016			binary & BCD digit addition, speed mo	4 index registers: (ix),(--ix),(ix++),(ix+off)
lem4_9ptr	https://opencor	beta	James Brakefield	accum	4	9		kintex-7-3	James	1 stage	151		6		1	151	##	14.5	0.24	1.0	240.0	AX		vhdl	2	lem1_9pti	Y		N	Y	512	2K	N	24			1	2016			binary & BCD digit addition, speed mo	4 index registers: (ix),(--ix),(ix++),(ix+off)
lem4_9ptr	https://opencor	beta	James Brakefield	4004	4	9		**zu-2e**	James	1 stage	210		6		0	397	##	v20.1	0.24	1.0	453.5	AX		vhdl	2	lem1_9pti	Y		N	Y	512	2K	N	24			1	2016			binary & BCD digit addition, speed mo	4 index registers: (ix),(--ix),(ix++),(ix+off)
mcs-4	https://opencor	alpha	Reece Pollack	accum	4	4		kintex-7-3	James	Brakef	228		6			376	##	14.7	0.16	4.0	66.0	X		verilog	7	i4004			N		4K	4K	N				2012	2012		4004 was multi-chip	4004 CPU & MCS-4
tinycomputer	https://github.com/zpeki		Zoltan Pekic	COP400	4	8		spartan3	James	Brakef	643	286	4			100	##	14.7	0.17	1.0	26.0	X	Y	vhdl	29	tinycomp	Y					256		20		16		2017		4-bit Up via 2901 slice & micro code	no data RAM memory
t400	https://opencor	stable	Arnim Laeuger	RISC	4	8		spartan-2	Arnim	Laeuge	643		3		2	60			0.16	4.0	3.7	AX		vhdl	36	t400_core	Y	yes	N	Y	64	1K	Y				2006	2009		implementation of National's 4-bit COP400 microcontroller	
jane_nn		stable	Suresh Devanathan	S2000	4	8		kintex-7-3	James	Brakef	723		6			178	##	14.7	0.33	1.0	81.4	X		vhdl	3	Processor	Y							27		16	2002			neural network microprocessor, specialized registers	
sys_emz1001	https://github.com/zpeki		Zoltan Pekic	accum	4	8		spartan3	Zoltan	Pekic	1022	344	4				##	14.7	0.16			X	Y	vhdl	26	EMZ1001A	Y	asm	N	Y	128	4K		59			2022	https://hackaday.	recreation of Iskra EMZ1001 4-bit mic	no block ram? Picture of original chip
nibblercpu	https://github.com/bchan		Bryan Chan	accum	4	8		spartan7	James	combi	9066	84	6				##	v23.2	0.16	1.0				system	24	nibbler	Y		N	Y	4K	4K					2017	http://www.rayslo	originally a TTL project	https://www.bigmessowires.com/nibbler/
lem1_9min	https://opencor	stable	James Brakefield	accum	1	9		kintex-7	James	1 stage	63		6		1	358	##	14.5	0.04	1.0	227.2	ALX		vhdl	3	lem1_9mi	Y	asm	N	Y	64	2K	N	8		64	1	2003	2009		logic emulation machine	
lem1_9	https://opencor	alpha	James Brakefield	accum	1	9		kintex-7-3	James	1 stage	75		6		1	171	##	14.5	0.04	1.0	91.2	AX		vhdl	2	lem1_9	Y		N	Y	32	2K	N	24			1	2016	2017		single bit at a time, absolute adrs	

_uP_all_soft folder	opencores or prmary link	status	author	style / clone	data sz	inst sz	FPGA	reporter	comments	LUTs ALUT	Dff	LUT?	mults	blk ram	F max	date	tool ver	MIPS /inst	clks/ inst	KIPS /LUT	ven dor	SOC	src code	#src files	top file	doc	tool chai n	fltg pt	Hav'd	max dat	max inst	byte adrs	# inst	adr mod	# reg	pipe len	start year	last revis	secondary web link	note worthy	comments
lem1_9ptr	https://opencor	beta	James Brakefield	accum	1	9	kintex-7-3	James	1 stag	147		6		1	176	##	14.5	0.06	1.0	72.0	AX		vhdl	2	lem1_9pti	Y		N	Y	512	2K	N	24			1	2016		use speed opt, logic emulation machi	4 index registers: (ix),(--ix),(ix++),(ix+off)
up3	https://people.e	stable	Bruce Land				cyclone2	Bruce Land		186		4		1		##	q8.0						verilog	1	de2_top													Cornell ECE576	basic core is scomp, used by up3 & de2_top'
116	# usable(beta, stable or m		18	676			20	blank		677		##			634	##	42			60	verilog		300		non-blank		512	53				434	42		31					
43	"B" or "X" of limited interest						672													661	vhdl		285		asm		117	Web page DMIPS p		en.wikipedia.org/wiki/Instructions_pe		community.freesc		www.eembc.org/coremark/index.php				
MIPS/MHz Pro-rating for data size:				0.67			53	zu-3e													sys verilog		36		forth		10	DMIPS per clock for many microprocessors:				http://en.wikipedia.org/wiki/Instructions_per_second				
1-bit	0.04	16-bit		0.80			64-bit			2.00											proprietary		24																
4-bit	0.17	24-bit		1.00			**Silicon Area equivalents**			**6LUT or ALUT ~= 1.5 4LUT**											scala		6																
8-bit	0.33	32-bit		1.50			LUTS/DSP48			16:1											schematic		13																
12-bit	0.40	48-bit					LUTS/Block RAM			32:1											vhdl, verilog		8																

Under the assumption that the core is capable of one instuction per clock

421 Unique folders in this sheet

77	_paper_only
60	educational
25	_weak_start
8	_up_cores
27	in limbo
10	planning
76	simulation
573	main+sim
497	net main
644	total

417	VHDL
450	Verilog
82	System Verilog
17	Spinal/Scala
19	VHDL, Verilog
3	MyHDL
36	proprietary
14	other
29	Schematics
1067	total

https://github.com/fayalalebrun/awesome-spinalhdl (17) scala/spinal CPUs

418 designs with FOM (KIPs/LUT) results (some duplicates due to multiple FPGA runs)
385 designs with best FOM (likely true measure of # of usable designs)

Column Titles	Details
"A"	A: 1st choice clone, B: 2nd choice clone, W: 1st choice original, X: 2nd choice original
"B"	used to indicate best KIPS/LUT for a given design, usually using fast FPGA family
cat	main, educational, planning, simulation, paper, in limbo or weak
_uP_all_soft folder	if opencores design is their folder name, otherwise my folder name
opencores or primary link	about 200 designs in open cores, about 100 in github
status	ASIC, paper (detailed in), planning (no source), alpha, beta, stable, mature, proprietary, untested; incomplete, educational typically <16 instructions, simulation
author	First Name, Last Name or university or corporation
style / clone	part number or "forth", RISC, accumulator, etc. "asic" indicates: avail as asic & fpga, an asic netlist source or a hard core within fpga chip
data size	data register size in bits
inst size	shortest instruction size in bits
FPGA	FPGA family for compile, place, route & timing, usually using fastest part grade
reporter	First Name, Last Name
comments	compile, place, route & timing problems
LUTs ALUT	total number of LUTs, ALUTs or tiles used including route-thrus & otherwise unavailable
Dff	total number of DFFs
LUT?	4-LUT, 6-LUT, Altera ALUT, Actel Tile
mults	total number of multipliers/DSPs used; 9x9 multiplier counts divided by two and rounded up
blk RAM	total # of block RAMs used, Xilinx half block RAM counts divided by two and rounded up
Fmax	maximum primary clock speed from compile, place & route run with best clock constraint, fastest part, best die temp
date	date of compile, place & route; serves to identify source version
tool ver	Altera (**Q**uartus), Xilinx (ISE, **V**ivado), Lattice Semiconductor(**D**iamond) or MicroSemi(**L**ibero) tool version number
MIPS /inst	prorated DMIPS per instruction, reduced for data word sizes under 32-bits, greater than one for multiple issue processors
clks/ inst	number of clocks per instruction, typically 1.0 for modern pipelined processors, subjective for older uP
KIPS /LUT	figure of merit, does not include effects of memory capacity, floating point or instruction set quality
Vendor	Vendors for which design builds: Actel: Libero, Intel(Altera): Quartus; Latticesemi: Diamond & iCEcube, Xilinx: ISE & Vivado
SOC	B: bare core (no RAM connections or memory access delay), Y: System on a Chip (has peripherals)
src code	VHDL or Verilog or System Verilog or schematic or gates or Proprietary or Scala etc
# src files	number of source files for compile, place, route & timing; includes test benches
top file	top file for compile, place, route & timing run, multiple versions of same design distinguished here
doc	is documentation provided?
tool chain	is there a compiler or assembler provided or available
fltg pt	does the compile, place, route & timing run include floating point?
Hav'd	H: separate instruction and data memory(s), 2C: # caches, M: MMU, N: von Neuman (single memory bus)
max data	maximum data address
max inst	maximum instruction address
byte adrs	is byte addressing provided
# inst	number of unique instructions, conditionals count as one instruction, somewhat subjective
# adr modes	abs, imm, PC rel, indexed, reg-reg indexed; stack, indir, indir++, --indir; (indir), (indir++), (--indir), (indexed), abs-short/direct page, scaled
# reg	number of registers in register file
pipe len	number of pipeline stages
start year	year of first design activity
last revis	last year for revisions or web page updates
secondary web link	secondary web address
note worthy	anything special about the design