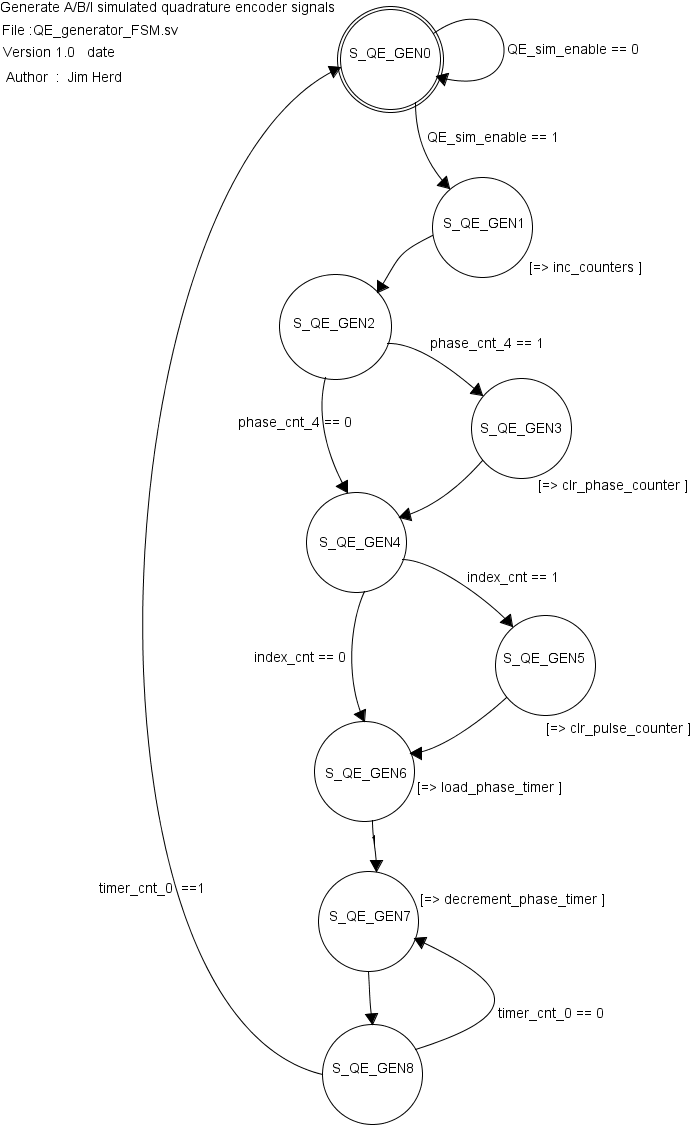
|  |  |  |  |
| --- | --- | --- | --- |
| FSM name : | QE\_generator\_FSM.sv | Date: | Feb 2021 |
| Section : | 1 of 1 | Author | Jim Herd |
| Notes : |  | | |



State Objects

|  |  |
| --- | --- |
| **States** | Notes |
| S\_QE\_GEN0 | Initial state. |
| S\_QE\_GEN1 | Increment phase counter and pulse counter |
| S\_QE\_GEN2 | Test for phase counter >3 |
| S\_QE\_GEN3 | Clear phase counter |
| S\_QE\_GEN4 | Test pulse counter |
| S\_QE\_GEN5 | Clear pulse counter |
| S\_QE\_GEN6 | Load phase timer |
| S\_QE\_GEN7 | Decrement phase timer |
| S\_QE\_GEN8 | Test phase timer |

Input objects

|  |  |  |
| --- | --- | --- |
| **Inputs** | Type | Notes |
| QE\_sim\_enable | binary | Bit 16 of PWM configuration register |
| phase\_cnt\_4 | binary |  |
| index\_cnt | binary |  |
| timer\_cnt\_0 | binary |  |

Output objects

|  |  |  |
| --- | --- | --- |
| **Outputs** | Type | Notes |
| inc\_counters | binary |  |
| clr\_phase\_counter | binary |  |
| clr\_pulse\_counter | binary |  |
| load\_phase\_timer | binary |  |
| decrement\_phase\_timer | binary |  |