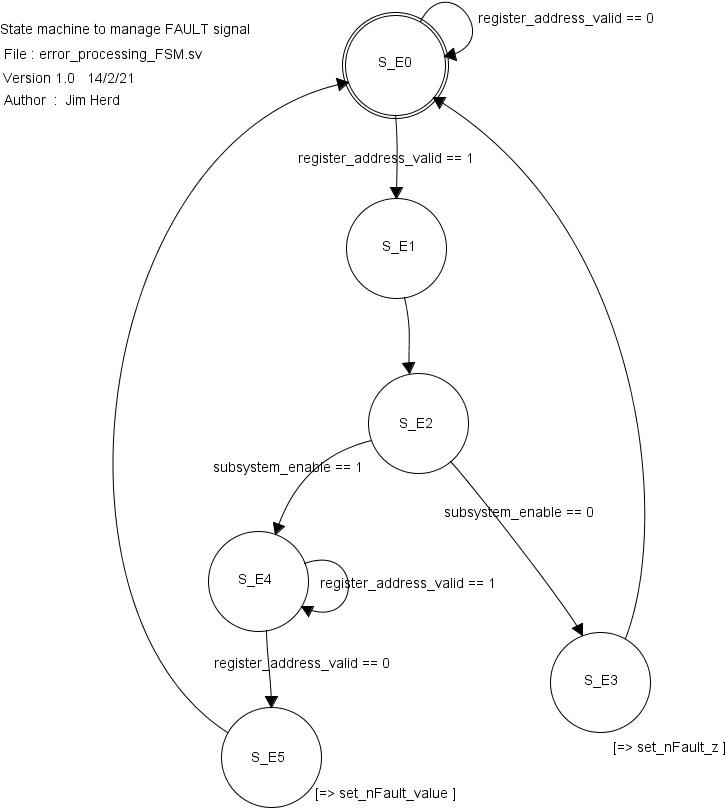
|  |  |  |  |
| --- | --- | --- | --- |
| FSM name : | Error\_processing.sv | Date: | Feb 2021 |
| Section : | 1 of 1 | Author | Jim Herd |
| Notes : | FIZZIM layout for FSM diagrams | | |



State Objects

|  |  |
| --- | --- |
| **States** | Notes |
| S\_E0 | Power-on state |
| S\_E1 | 20nS delay to allow processing of **subsystem\_enable** signal. |
| S\_E2 | Check whether subsystem has been directly addressed. |
| S\_E3 | Set **nFault** output to high impedance. **nFault** is a “tri-state” signal, although the Systemverilog compiler will implement it as an OR structure. |
| S\_E4 | Process any error conditions.  nFault == 0 🡪 error  nFault == 1 🡪 OK |

Input objects

|  |  |  |
| --- | --- | --- |
| **Inputs** | Type | Notes |
| register\_address\_valid | binary |  |
| subsystem\_enable | binary |  |

Output objects

|  |  |  |
| --- | --- | --- |
| **Outputs** | Type | Notes |
| set\_nFault\_z | binary |  |
| Set\_nFault\_value | binary |  |