Wattbot:*nt*

Technical Notes

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# 1 Introduction

This document brings together technical details relating to the design of Wattbot:*nt*.

# 2 System

## 2.1 General system overview

CANbus bus

FPGA

H-bridge

(opt)

H-bridge

(opt)

H-bridge

(opt)

H-bridge

(opt)

Encoders

RC servo

RC servo

RC servo

RC servo

RC servo

RC servo

RC servo

RC servo

Low level

Microprocessor

High speed bus

Serial comms channel

High level

Control computer

e.g. Raspi

Real-time

clock

Dynamixel

servo bus

I2C

sensors

Motion

Control

System

H-bridge

(opt)

H-bridge

(opt)

H-bridge

(opt)

H-bridge

(opt)

External

H-bridge

Internal

H-bridge

DC motors

Figure 1 General system structure

## 2.2 PORT number allocation.

When a command is sent to the FPGA it has an allocated PORT number, rather like the TCP/IP port number. This is the number that ensures that the reply is sent to the correct queue. This allows commands to come from a variety of sources e.g. PID commands from within the uP and remote commands from the High Level controller.

PORT numbers are represented by an unsigned 8-bit value with a range from 0 to 255.

Allocation is as follows

|  |  |
| --- | --- |
| PORT | Description |
| 0 | Reserved. |
| 1 | Debug process in High Level controller   * Any process within the uP can send messages to this PORT. |
| 2 🡪 19 | Used by processes in the Low Level controller (uP) |
| 20 🡪 255 | Used by processes in the High Level controller (e.g. PC, Raspbery Pi, etc) |

# 3 FPGA

## 3.1 General FPGA overview

The FPGA is structured as a peripheral system that is accessed by reading and writing to registers. There are two busses

1. An external 8-bit bi-directional bus connects the uP to the FPGA. This is a handshaked buss that run at a rate of about 100,000 transactions per second.
2. An internal 32-bit bi-directional bus that links all the peripheral subsystems to the uP.

An FPGA state machine (name…) performs all the necessary conversions between the two busses.

FSM = Finite State Machine

µP

FPGA

other functions

8-bit bus

32-bit bus

Low level

microprocessor

Digital I/O

Figure 2 General FPGA structure

The FPGA looks like a set of 256 32-bit I/O registers. For a fixed SysyemVerilog compilation, the registers will be defined. However, if the compilation parameters that define the number of subsystems are changed (eg the number of PWM units) then the register addresses will change. This is not a problem as the number of subsystems is defined in register 0 and should be the first register to be read to allow internal addresses to be pre-calculated.

Register addressing is shown in Appendix I.

# 4 Low-level control microprocessor

# 4.1 Data packets between microprocessor and FPGA.

The data interface between the low level microcontroller is an 8-bit bidirectional bus. A state machine in the FPGA converts between this 8-bit bit and the internal 32-bit bus.

The microprocessor accesses the FPGA as a set of registers. The current system has 256 available registers (0-<255). At this time, only bits 0 and 7 of the command byte are used. Bit 0 is a READ/WRITE bit and bit 7 is a RESET bit. The 6-byte microprocessor to FPGA packet is as follows (shown in C struct format for documentation purposes)

**typedef** **struct** {

**cmd\_t** command;

**uint8\_t** register\_number;

**uint32\_t** data;

} uP\_to\_FPGA\_packet\_t;

**typedef** **struct** {

**int** R\_W :1;

**int** spare :6;

**int** reset :1;

} cmd\_t;

The data returned from the FPGA can be set at compile time to be one or two 32-bit words. The first word is data and the second word is status.

However, there is very little status data that can be returned therefore this 32-bit value predominately zero, resulting in a waste of time and bandwidth on the uP/FPGA bus. The current system defaults to just sending the data. If you wish to use the status word that the FPFA and uP code must be recompiled with the appropriate compile time definitions.

**#ifdef INCLUDE\_32\_BIT\_STATUS\_RETURN**

**typedef** **struct** {

**uint32\_t** data;

**uint32\_t** status;

} FPGA\_to\_uP\_packet\_t;

**#else**

**typedef** **struct** {

**uint32\_t** data;

} FPGA\_to\_uP\_packet\_t;

**#endif**

The current code implementation allocates space for the status word but does not load it with any data.

How can status get to the uP from the FPGA when no status word is sent?

1. Each FPGA subsystem has a status register which can be read. Refer to register bit definitions.
2. There is a single digital status line connecting the FPGA to the uP. It is asserted low and can be used by a subsystem to indicate a problem.

# 4.2 Process structure of µP software : GitHub Tag V1.0

The uP runs the MBED RTOS software. The initial test structure uses the following structure with three processes (threads) and two mailbox queues.

FPGA

Com

Port

High level

controller

P3

P2

Low Level controller (µP)

P1

Queue1

Queue2

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Type** | **Program name** | **Notes** |
| **P1** | Process | read\_from\_HLcontrol\_task | * Read ASCII command string from controlling computer * Send FPGA related commands to FPGA command queue * Implement non-FPGA commands |
| **P2** | Process | write\_to\_HLcontrol\_task | * Take ASCII reply strings from reply queue and send to controlling computer |
| **P3** | Process | FPGA\_IO\_task | * Take FPGA command from FPGA command queue and Implement on the FPGA through the 8-bit bi-directional bus. |
| **Queue 1** | Mailbox | FPGA\_cmd\_queue | * FIFO queue of LLcontrol (uP) commands coded as ASCII strings |
| **Queue 2** | Mailbox | HLcontrol\_reply\_queue | * FIFO queue of binary coded FPGA register commands |

This structure provides the basic system to test and exercise the FPGA hardware. The ASCII command format allows easy access from a high level control computer e.g. PC, Raspberry Pi, etc.

Testing uses a windows laptop with a C# program (March 2021).

# 4.3 Process structure of µP software : GitHub Tag V2.0

(30/3/21 Design only)

Added process (P4) to V1.0 design that can initiate and control a sequence of FPGA commands, e.g., execute timed reading of an encoder channel as part of testing. Works by injecting FPGA commands into “Queue 1” and receiving results through “Queue 4” A specific PORT number would be assigned to this activity.

FPGA

Com

Port

High level

controller

P3

P2

Low Level controller (µP)

P1

Queue1

Queue2

P4

Queue3

Queue4

Additional objects to V1

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Type** | **Program name** | **Notes** |
| **P4** | Process | sequence\_task | * Implements sequence of FPGA commands, specifically for test purposes. |
| **Queue 3** | Mailbox | sequence\_cmd\_queue | * FIFO queue of LLcontrol (uP) sequence commands |
| **Queue 4** | Mailbox | sequence\_reply\_queue | * FIFO queue of results from executed FPGA commands |

# 5 High-level processor

# Appendices

# Appendix A :: FPGA register allocation.

|  |  |  |
| --- | --- | --- |
| **Register** | **Address** | **Notes** |
| **SYS\_INFO\_0** | 0 | Some basic information : Version, number of PWM/QE/RC subsystems |
|  |  |  |
| **PWM\_PERIOD** | PWM\_0 + 0 | Period in units of 20 nanoseconds |
| **PWM\_ON\_TIME** | PWM\_0 + 1 | PWM on-time in units of 20 nanoseconds |
| **PWM\_CONFIG** | PWM\_0 + 2 |  |
| **PWM\_STATUS** | PWM\_0 + 3 |  |
| **. . . . . . . . . . . .** |  |  |
| **PWM\_PERIOD** | PWM\_n + 0 | "n"th PWM subsystem |
| **PWM\_ON\_TIME** | PWM\_n + 1 |  |
| **PWM\_CONFIG** | PWM\_n + 2 |  |
| **PWM\_STATUS** | PWM\_n + 3 |  |
|  |  |  |
| **QE\_COUNT\_BUFFER** | QE\_0 + 0 | Count of decoded encoder pulses |
| **QE\_TURN\_BUFFER** | QE\_0 + 1 | Count of encoder index pulses |
| **QE\_SPEED\_BUFFER** | QE\_0 + 2 | Number of 20 nanosecond counts during single encoder pulse |
| **QE\_SIM\_PHASE\_TIME** | QE\_0 + 3 |  |
| **QE\_COUNTS\_PER\_REV** | QE\_0 + 4 | Number of encoder counts in a 360 degree turn |
| **QE\_CONFIG** | QE\_0 + 5 |  |
| **QE\_STATUS** | QE\_0 + 6 |  |
| **. . . . . . . . . . . .** |  |  |
| **QE\_COUNT\_BUFFER** | QE\_m + 0 | "m"th quadrature encoder subsystem |
| **QE\_TURN\_BUFFER** | QE\_m + 1 |  |
| **QE\_SPEED\_BUFFER** | QE\_m + 2 |  |
| **QE\_SIM\_PHASE\_TIME** | QE\_m + 3 |  |
| **QE\_COUNTS\_PER\_REV** | QE\_m + 4 |  |
| **QE\_CONFIG** | QE\_m + 5 |  |
| **QE\_STATUS** | QE\_m + 6 |  |
|  |  |  |
| **RC\_SERVO\_PERIOD** | RC\_0 + 0 | Period in units of 20 nanoseconds |
| **RC\_SERVO\_CONFIG** | RC\_0 + 1 |  |
| **RC\_SERVO\_STATUS** | RC\_0 + 2 |  |
| **RC\_SERVO\_ON\_TIME + 0** | RC\_0 + 3 | Servo 0 pulse on-time in units of 20 nanoseconds |
| **RC\_SERVO\_ON\_TIME +1** | RC\_0 + 4 | Servo 1 pulse on-time in units of 20 nanoseconds |
| **. . . . . . . . . . . .** | . . . . |  |
| **RC\_SERVO\_ON\_TIME + 7** | RC\_0 + 10 | Servo 7 pulse on-time in units of 20 nanoseconds |