

Figure 1: Schematic Functionality Waveforms



Figure 2: Layout Functionality waveforms

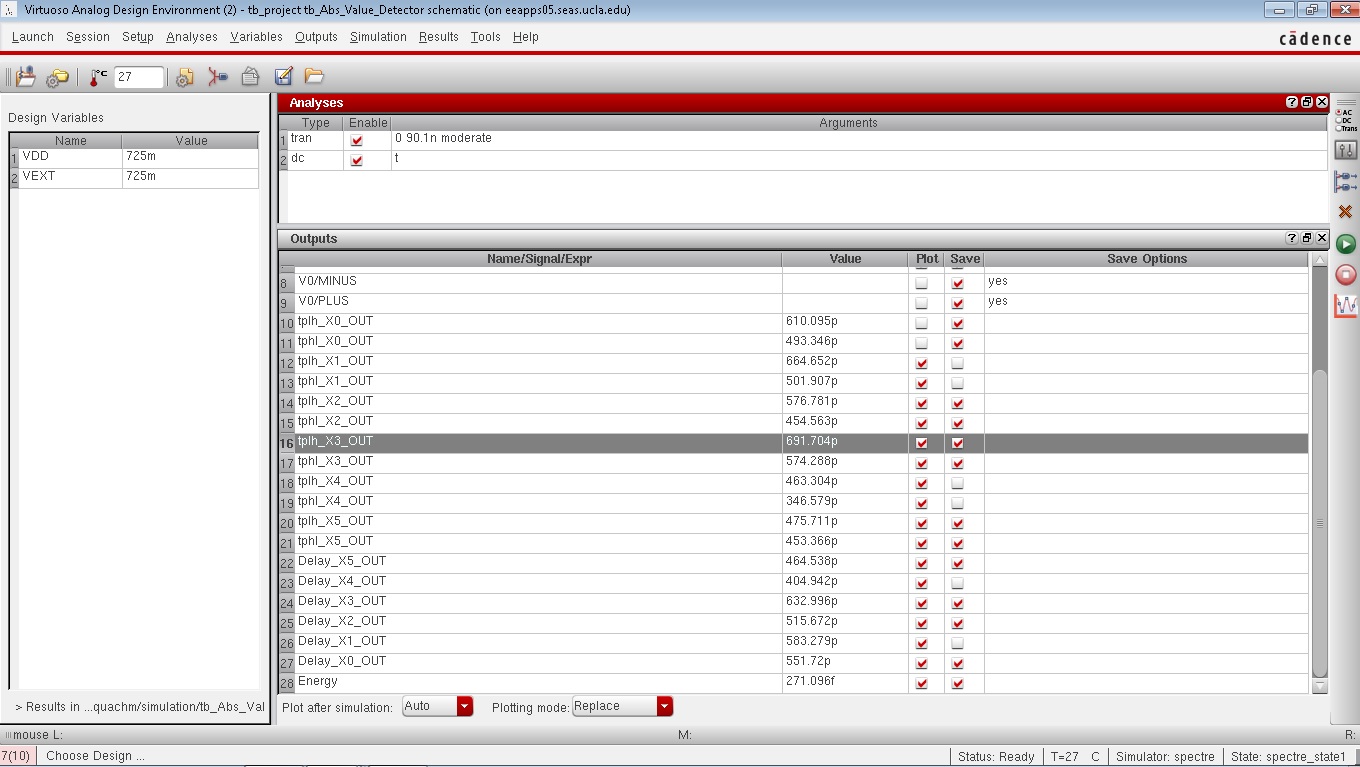


Figure 3: Schematic Delay and Energy Results

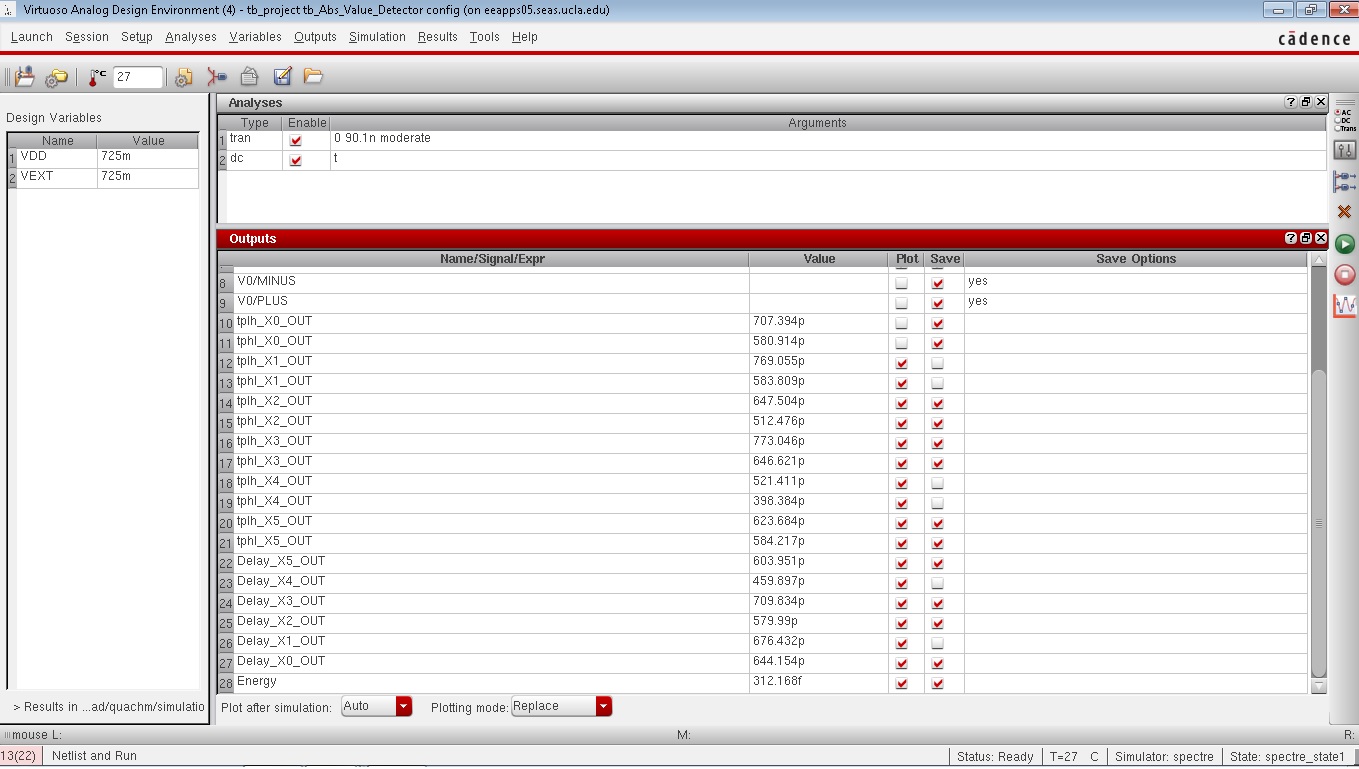


Figure 4: Layout Delay and Energy Results

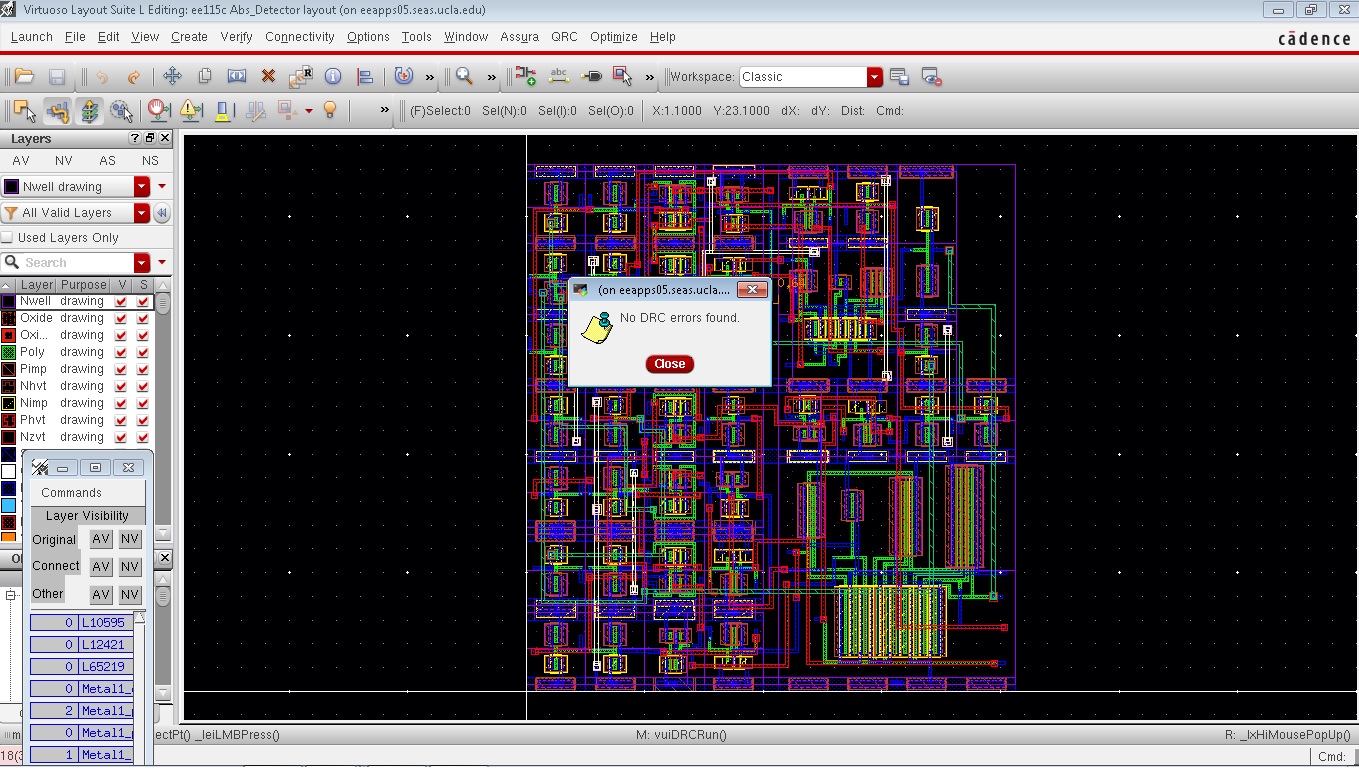


Figure 6: DRC check

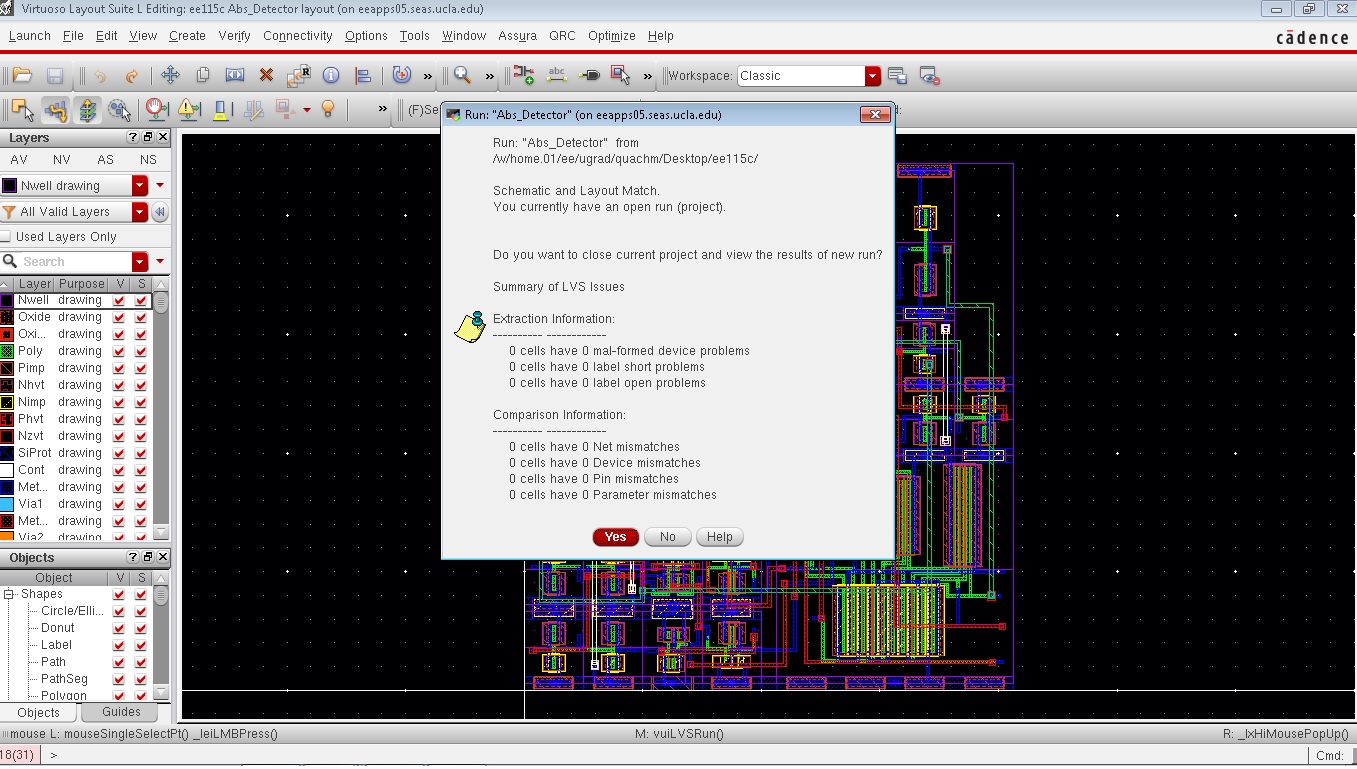


Figure 7: LVS check

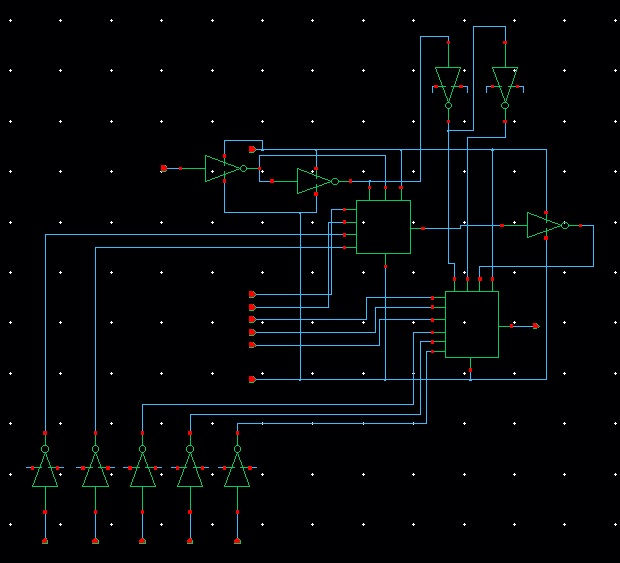


Figure 8: High level schematic

Work distribution:

This project was mostly done together, so every part of the project was worked on by both team members. The categories that each team member emphasized are as follows:

Matthew Quach: High level layout, Sizing tests

Jeffrey Jiang: Schematic Logic, Low level layout