



Automated Robust Design Optimization for Analog Circuits

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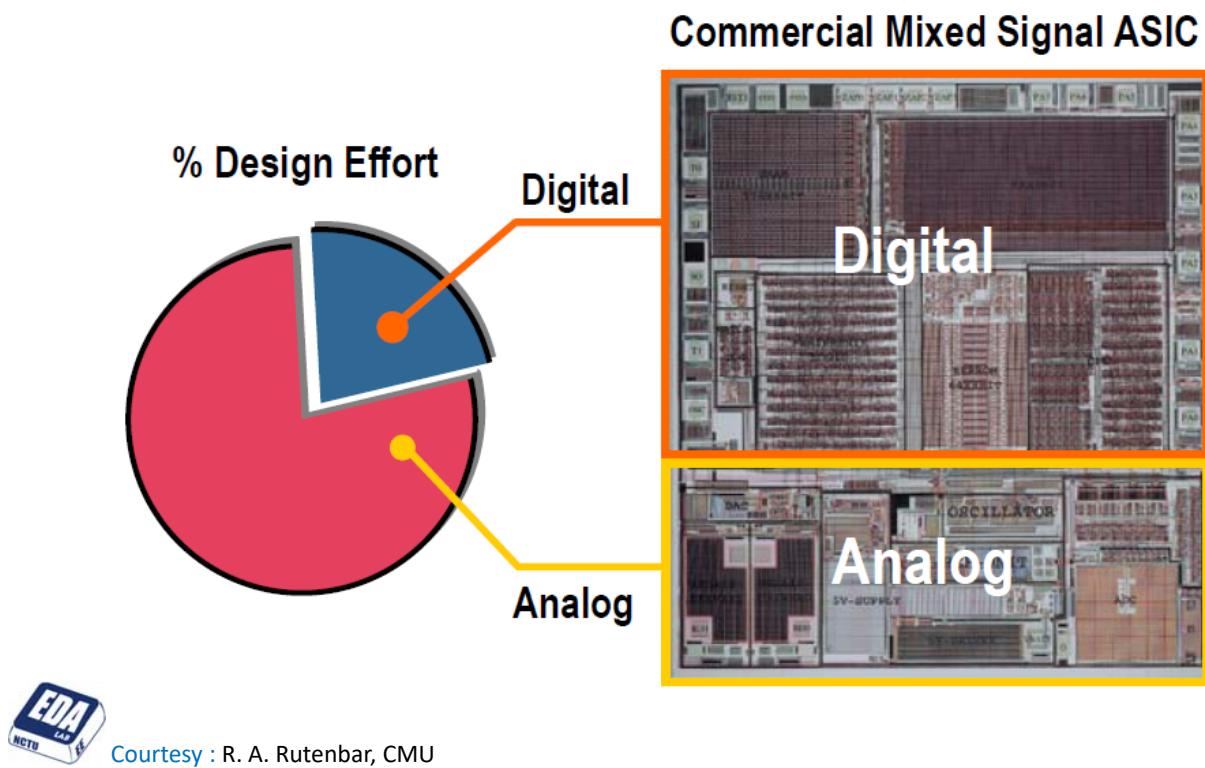
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Outline

- Motivation
- Parasitic-Aware Synthesis Approach
- Yield-Aware Synthesis Approach
- Aging-Aware Synthesis Approach



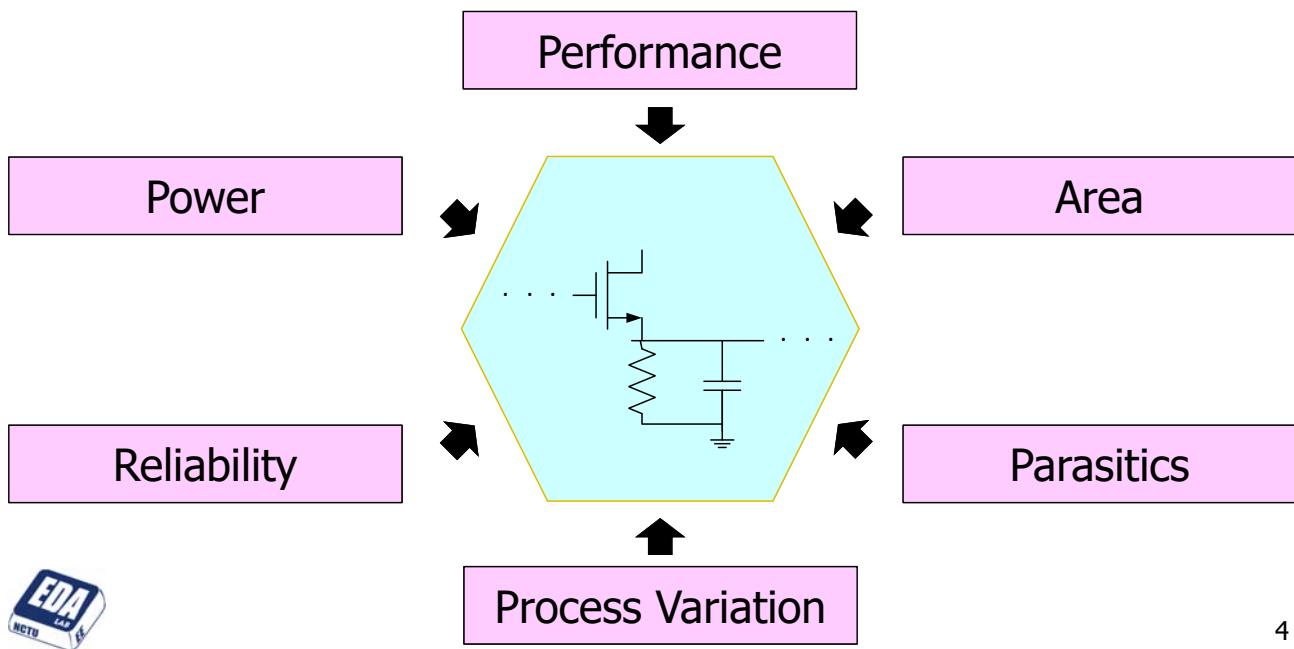
The Mixed-Signal Design Problem



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Analog Circuit Design Issues

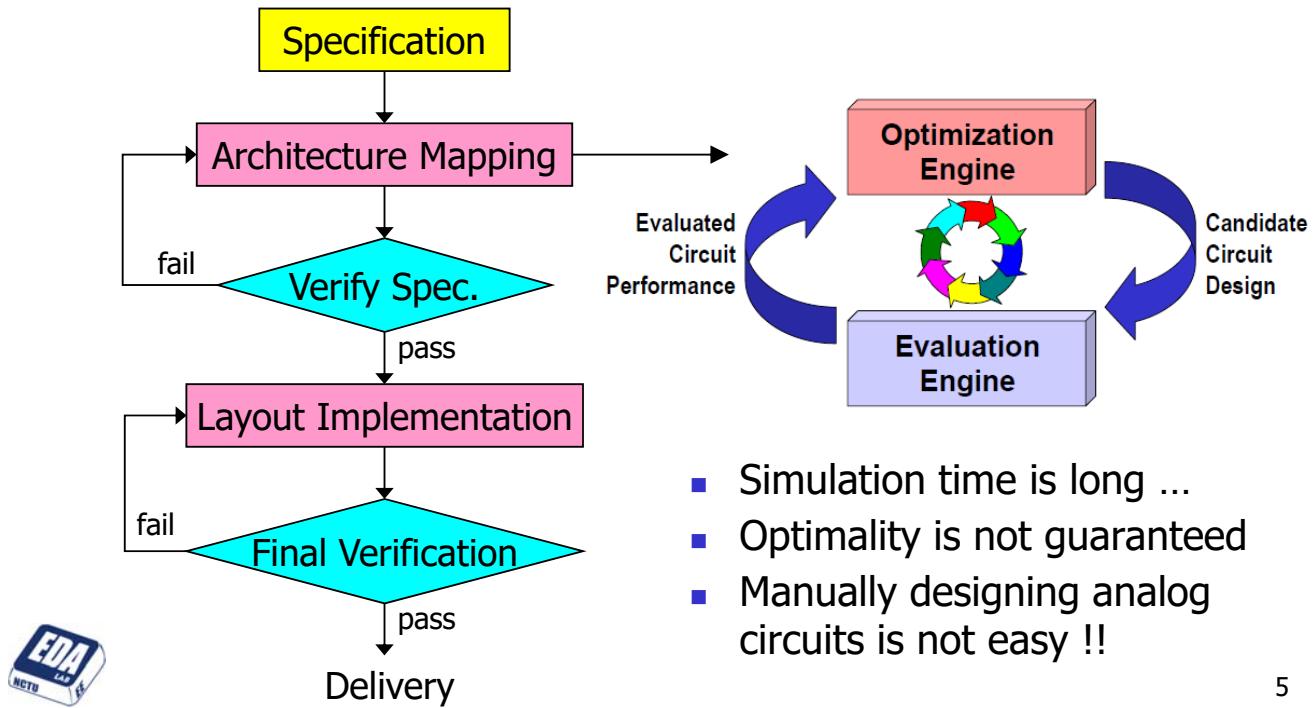
- Analog designs have to consider many issues together
 - EDA tools can help designers solve this tough problem



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Typical AMS Design Approach

- Often require **many iterations** to meet all spec.

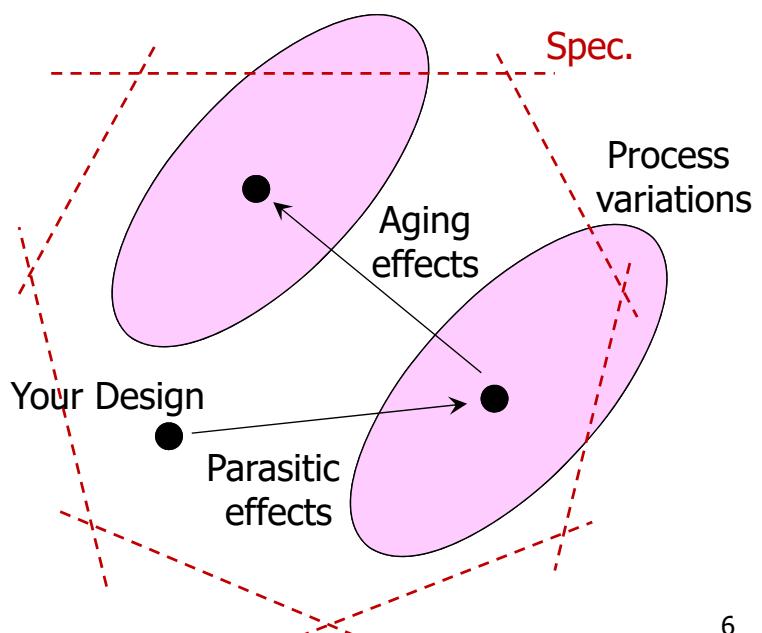


- Simulation time is long ...
- Optimality is not guaranteed
- Manually designing analog circuits is not easy !!

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Prediction ≠ Real Design

- Non-ideal effects are often not considered in traditional analog design automation algorithms
 - Parasitic effects
 - Process variations
 - Aging effects
- Real simulation results are often quite different to the prediction
 - Require many design iterations to converge

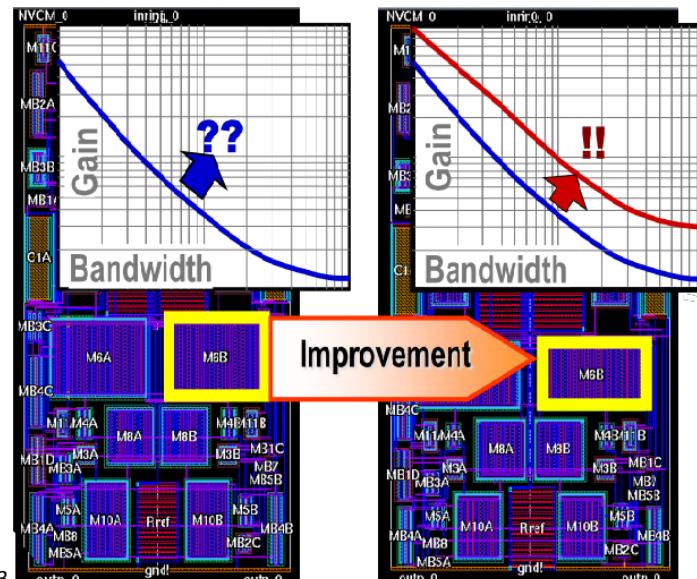


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Layout-Induced Parasitic Effects

- Analog circuit are more sensitive to the parasitic effects
- In conventional design flow, those parasitic effects can only be estimated after layout completion
 - Re-design loops are often required

Small change could have big impacts on circuit.

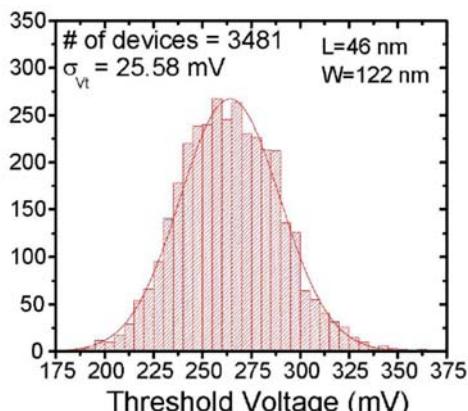


Ref: R.A Rutenbar., "Emerging Tools for Analog & Mixed-Signal: The Role of Synthesis and Analog Intellectual Property" in DATE master course, 2003

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Process Variation Effects

IBM 90nm: V_t variation

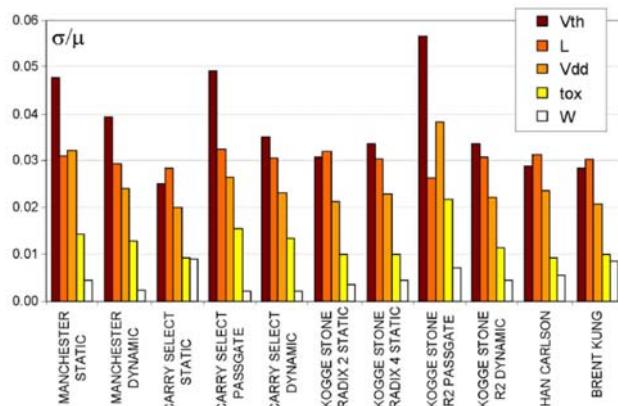


μ : mean value

σ : standard deviation



Statistical devices induce statistical performances



delay variations of different adders (90nm)

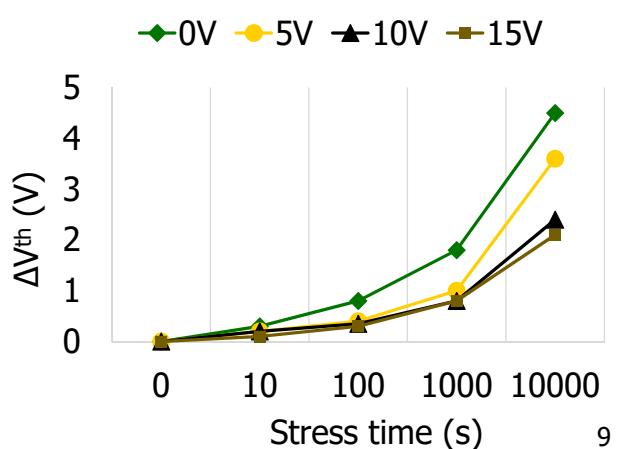


Ref: S. Nassif et. al, "High Performance CMOS Variability in the 65nm Regime and Beyond," Int. Electron Devices Meeting'07.

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Aging Effects

- Aging effects change circuit behavior with time
 - Aging effects: negative-bias temperature instability (NBTI), hot-carrier injection (HCI), ...
- Performance degrades when exposed in the ambient air or under continuous bias-stress
 - Change the V_t
 - Impact the circuit performance
 - Reduce yield and reliability significantly

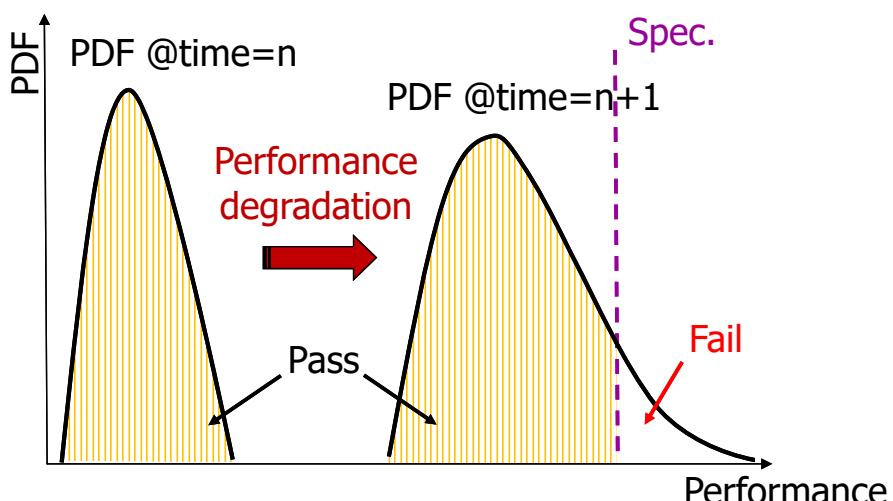


Ref: R. Shringarpure, et al., "Localization of Gate Bias Induced Threshold Voltage Degradation in a-Si:H TFTs," *IEEE EDL*, vol. 29, no. 1, pp. 93–95, Jan. 2008.



Lifetime Yield

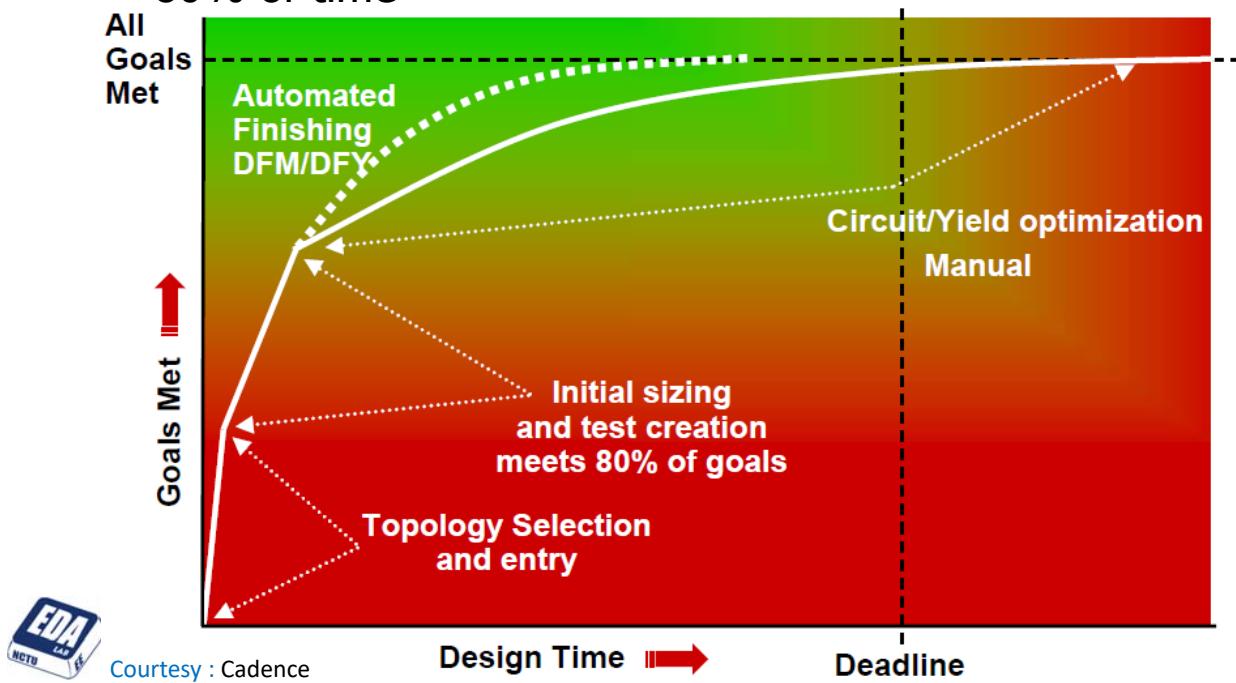
- Lifetime Yield = Process variations + Aging effects
- Analysis become more complex with one more dimension (time)



Ref: R. Shringarpure, et al., "Circuit simulation of threshold-voltage degradation in a-Si:H TFTs fabricated at 175°C," *IEEE TED*, vol. 54, no. 7, pp. 1781–1783, Jul. 2007.

DFY is not easy ...

- DFM/DFY by hand is **painful**: last 20% of design takes 80% of time



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Robust Design Optimization Flow

- Differences between prediction and simulation do exist
 - Results in many design iteration loops → not efficient
- How to consider the non-ideal effects in optimization flow?
- For parasitic effects
 - Develop a rough estimation technique before layout
 - Avoid the sizing-layout loop
- For process variations
 - Require accurate & fast analysis for variation effects
 - Avoid simulating lots of samples iteratively
- For lifetime yield
 - Simulate yield at every time step → cost is too high
 - Considered with fresh yield simultaneously



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- Yield-Aware Synthesis Approach
- Aging-Aware Synthesis Approach



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Parasitic Models

- Layout induced parasitics have 2 categories
 - Intra-module
 - Inter-module
- Intra-module (device)
 - The parasitic components within a device
 - Multi-finger, capacitors, inductors
- Inter-module (interconnect)
 - The parasitic components between devices
 - Determine by the placement and routing



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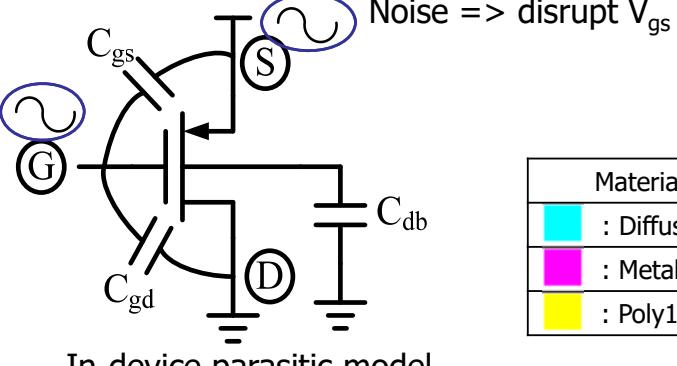
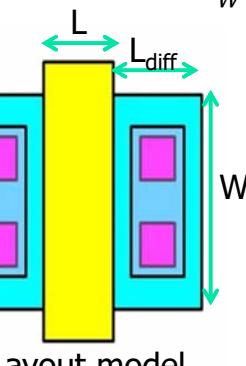
Device Parasitic Model

- In-device parasitic has large impacts on performance
 - Should be considered at circuit design stage
- Strongly dependent on layout styles
 - EX: layout parameter

$$AS = AD = W * L_{diff}$$

$$PD = PS = 2 * L_{diff} + W$$

$$NRD = NRS = \frac{L_{diff}}{W}$$

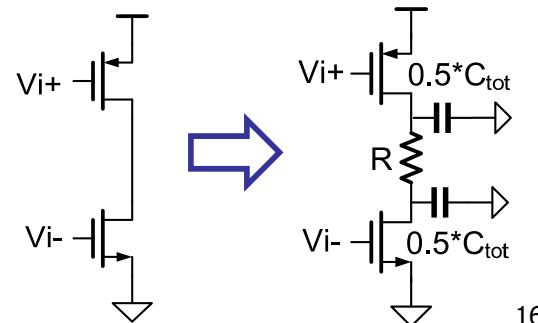


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Interconnect Parasitic Model

Resistor Model	Capacitor Model
$R = R_p * (L/W)$	$C = C_p * W * L$

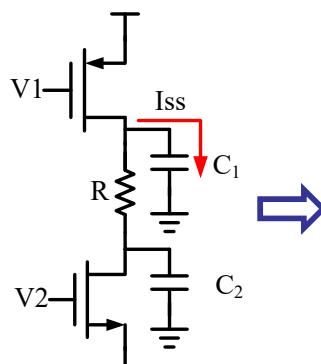
- Interconnect model (π model)
 - R_p, C_p extracted from process file



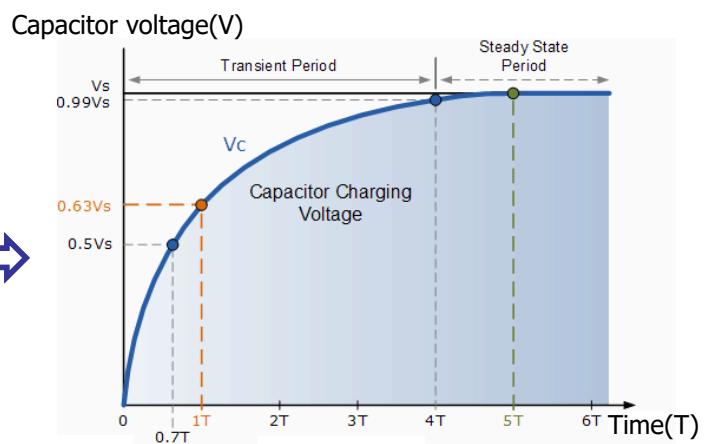
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RC Delay

- The values of resistors and capacitors determine the signal delay
- Impacts on circuit performance
 - Frequency response
 - Speed



a. Charge circuit



b. Capacitor charging timing diagram

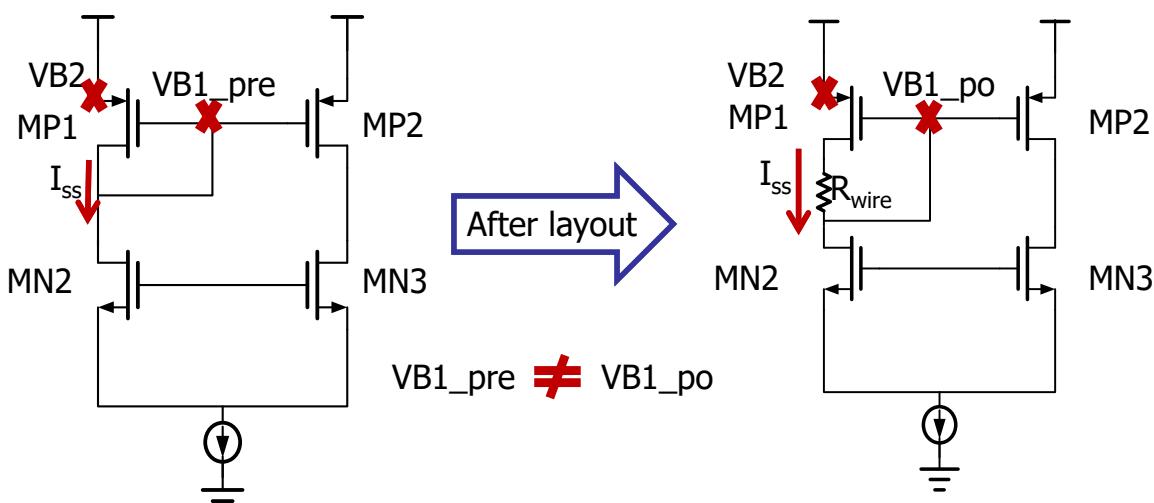


Ref: Electronics Tutorial about the RC Time Constant : RC charging circuit.
Available at: http://www.electronics-tutorials.ws/rc/rc_1.html

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IR Drop

- Interconnect parasitics may cause extra voltage drop
 - The node voltage might be different in pre-sim and po-sim
 - The current and transconductance are also changed

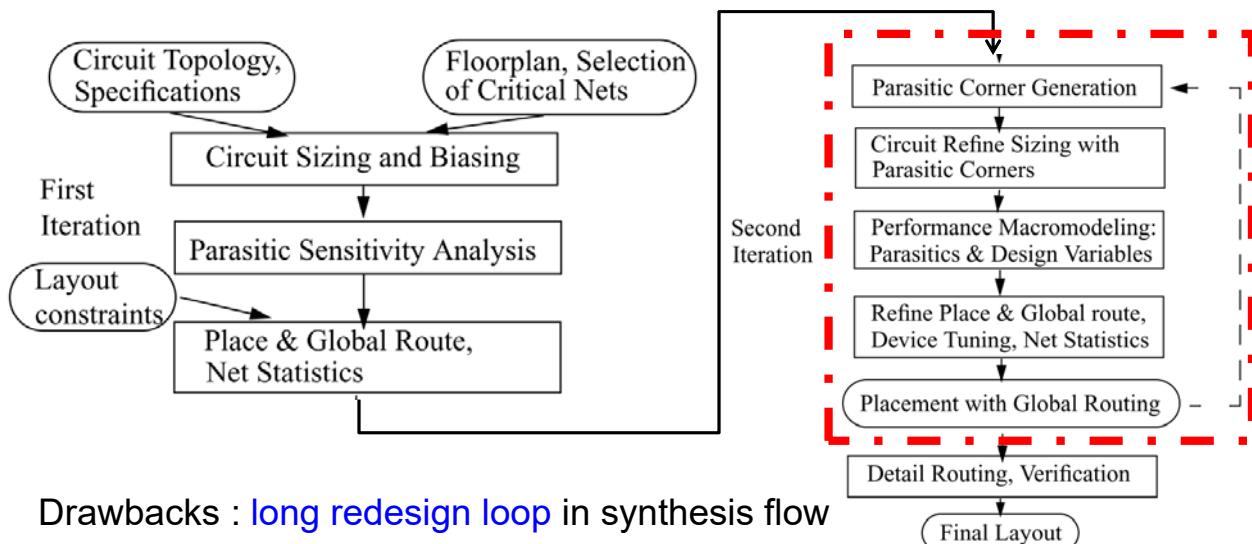


$$I_{D1_pre} = \gamma(V_{sg1_pre} - V_{tp})^2 \neq I_{D1_po} = \gamma(V_{sg1_po} - V_{tp})^2$$

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Sizing with Performance Model

- Use performance model for fast estimation during sizing
- Require rough P&R to get layout information

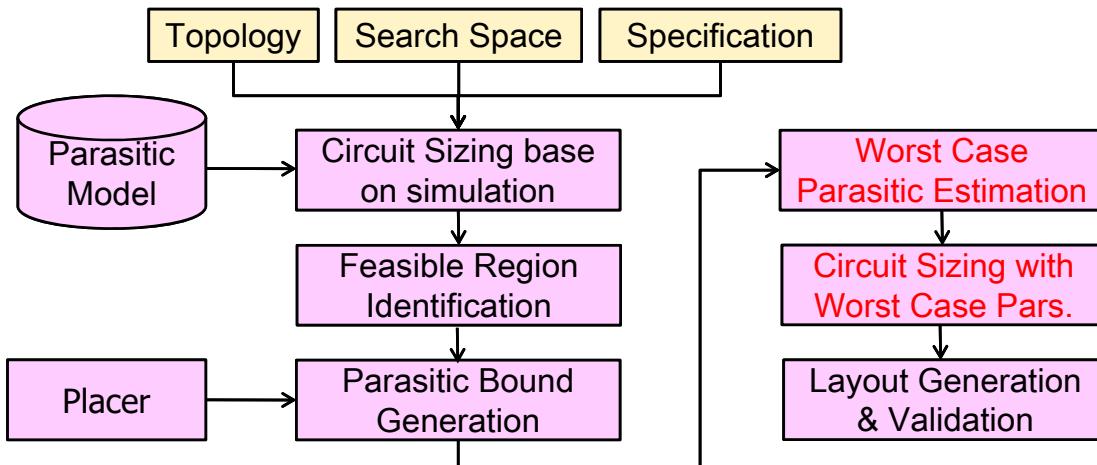


Ref: G. Zhang, A. Dengi, R. A. Rohrer, R. A. Rutenbar and L. R. Carley, “A synthesis flow toward fast parasitic closure for radio frequency integrated circuits”, in DAC 2004.

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Worst Case Parasitic Corner

- Use worst case parasitic to compensate performance



- Drawbacks: too much overdesign due to worst case parasitic and time estimation

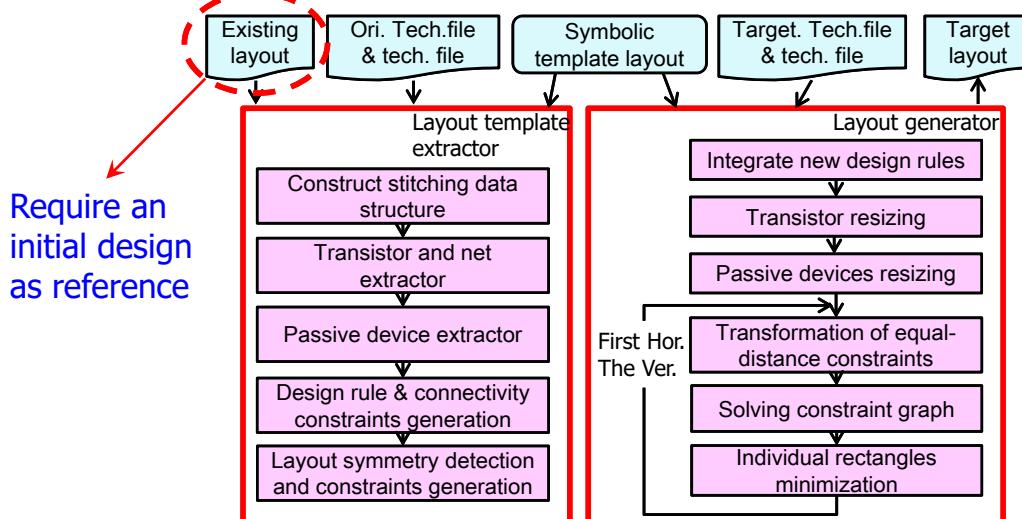


Ref: A. Agatwal, R. Vemuri, “Layout-Aware RF Circuit Synthesis Driven by Worst Case Parasitic Corners”, IEEE Int'l Conf. on Computer Design, 2005.

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Template-Based Retargeting Flow

- Extract the layout template of the original design and migrate to new technology automatically
- Parasitic information is also extracted

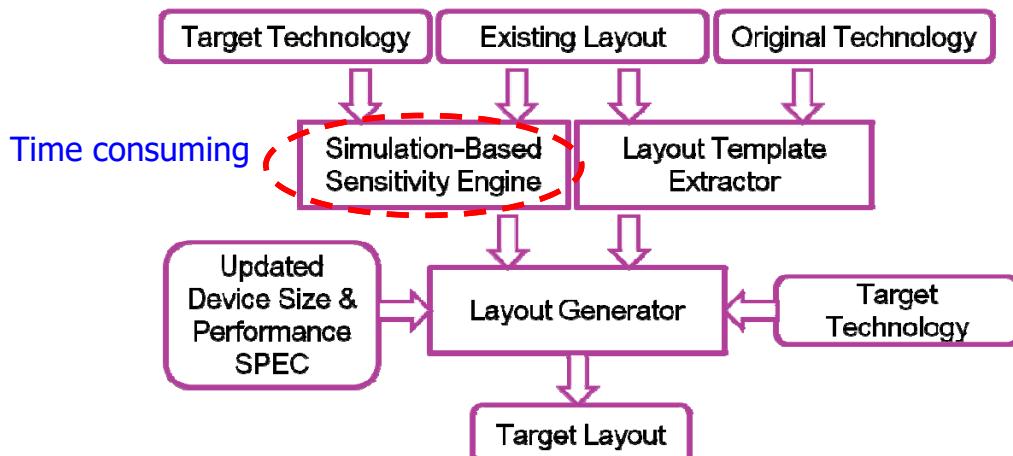


Ref: Nut. Jangkrajarng et al., "Template-Based Parasitic-Aware Optimization and Retargeting of Analog and RF Integrated Circuit Layouts", in ICCAD'2006

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Performance-Constrained Retargeting

- Calculate the performance sensitivity value based on layout template
- Adjust layout based on the sensitivity value to meet performance spec. under parasitic effect

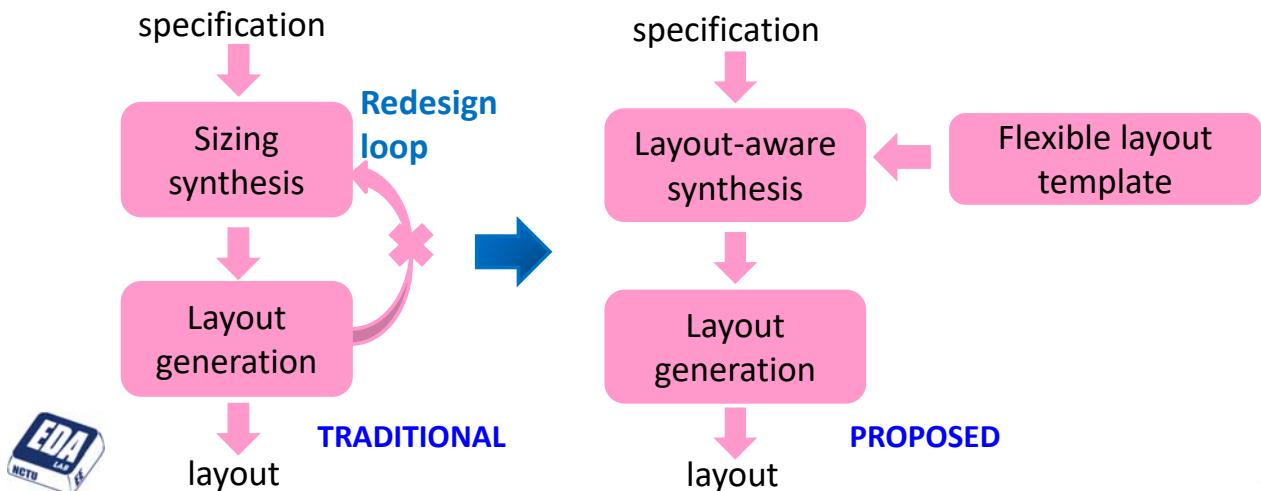


Ref: Z. Li and L. Zhang, "A Performance-Constrained Template-Based Layout Retargeting Algorithm for Analog Integrated Circuits" in ASP-DAC, 2010

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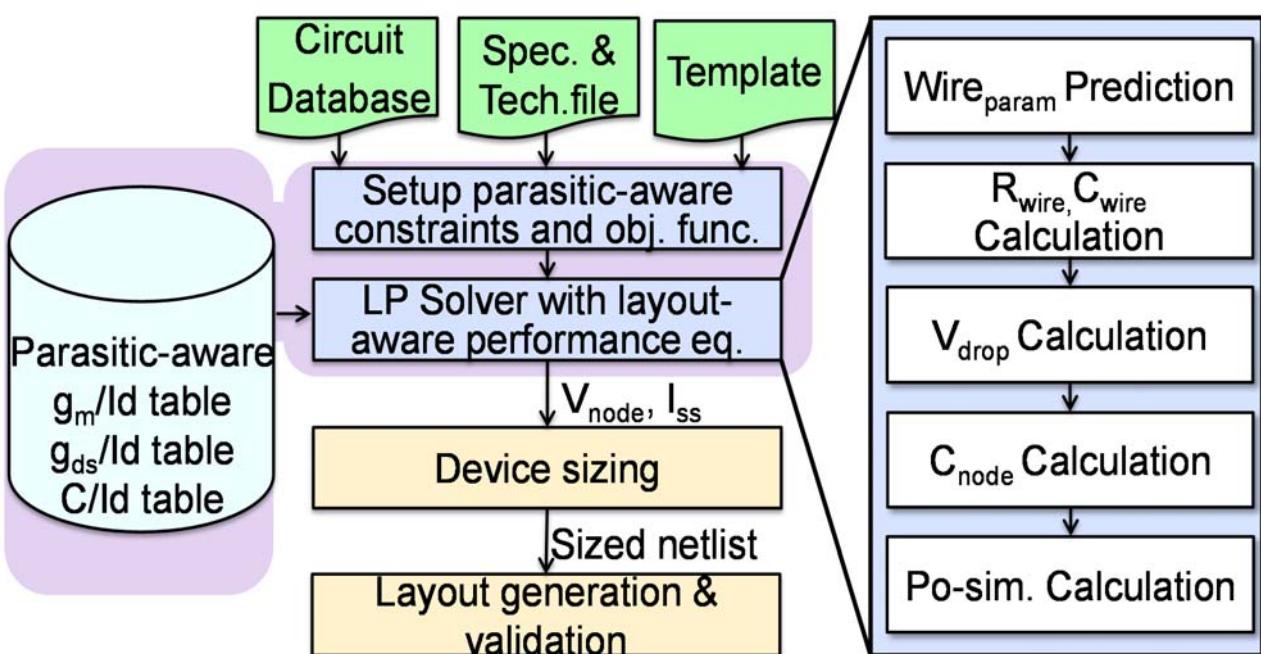
Parasitic-Aware Circuit Sizing

- Traditional flow requires redesign loops during synthesis
 - Spend a lot of time on the sizing-evaluation loops
- Proposed flow considers parasitic in early circuit sizing
 - Estimate parasitic effects from the flexible layout template
 - Avoid redesign loop in the synthesis flow



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Parasitic-Aware Synthesis Flow



Ref: Y.-L. Chen, Y.-C. Ding, Y.-C. Liao, H.-J. Chang, and C.-N. J. Liu, "A Layout-Aware Automatic Sizing Approach for Retargeting Analog Integrated Circuits", IEEE Int'l Symp. on VLSI Design, Automation, and Test , Apr. 2013

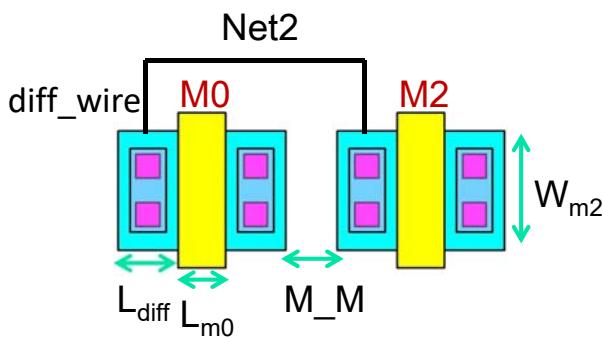
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Wire Length Estimation

- Use layout template to estimate the wire length
 - Predict routing path and its length on the layout template
 - Estimate the device width from I_d

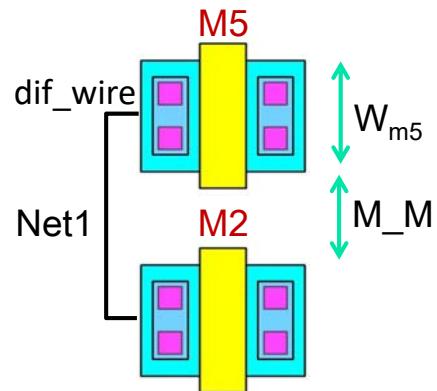
$$W = \frac{2Id * l}{u_n C_{ox} * (V_{GS} - V_t)^2}$$

Example 1



$$Wire_{net2} = 2 * L_{diff} + L_{m0} + M_M + 2 * dif_wire$$

Example 2

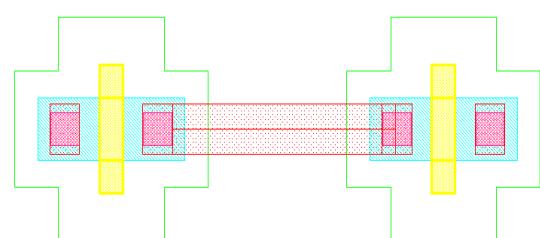


$$Wire_{net1} = (W_{m5} + W_{m2}) + M_M + 2 * dif_wire$$

R_{wire} and C_{wire} Calculation

- Calculate the values of resistance and capacitance from wire length
 - $R = R_{sh} * \left(\frac{length}{width} \right)$
 - $C = C_{sh} * length * width$

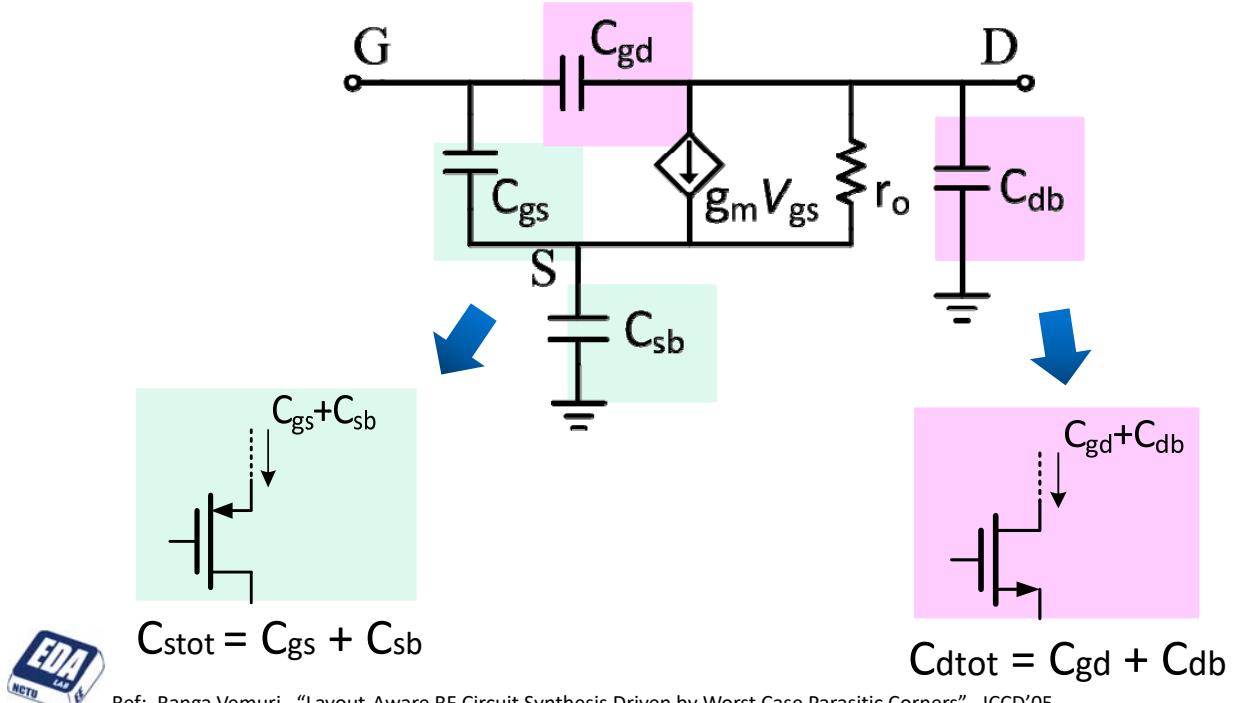
Example



Wire length : 1.625u
 Wire width : 0.23u
 Material : metal1 ($R_{sh}=0.08, C_{sh}=0.25$)
 Resistor Value : $0.08 * (1.625 / 0.23)$
 Capacitor value: $0.25 * 1.625 * 0.23$

Parasitic Capacitance

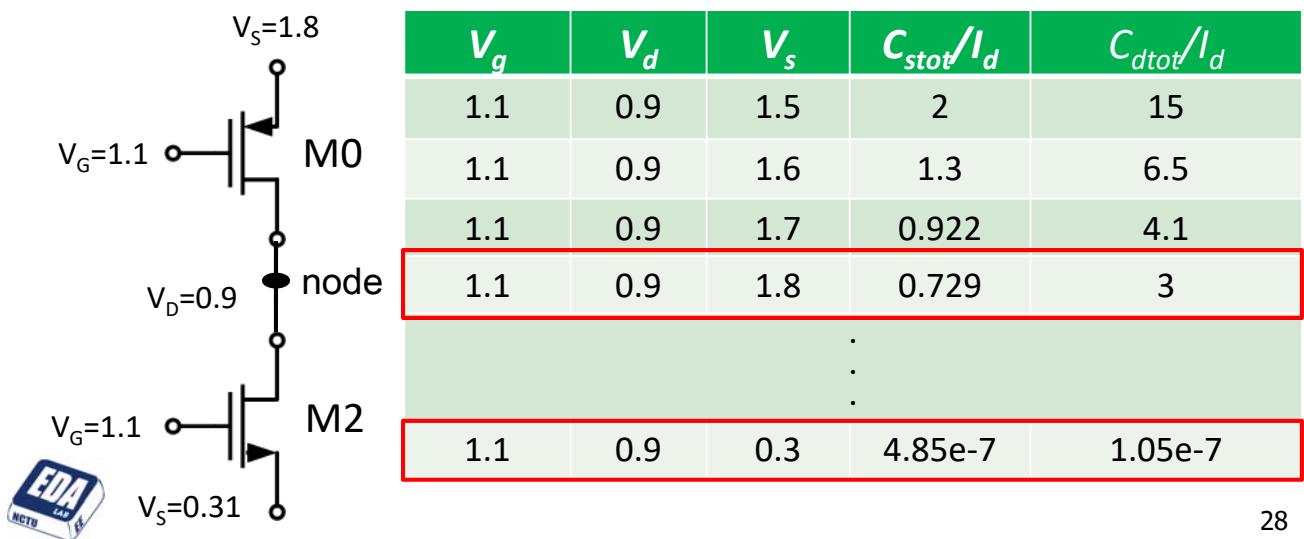
- Consider the device's parasitic into circuit synthesis



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Parasitic Capacitance Consideration

- The value of capacitance increase with current
 - C_{dtot}/I_d and C_{stot}/I_d are also independent of device's size
- Use look-up table to get C_{dtot} and C_{stot} of each device



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Parasitic-aware Lookup Table

- Parasitic capacitors in a transistor impact on the transistor behavior
 - I_D , C_s ... of a transistor are different with parasitic capacitors
- Parameter tables are constructed from the post-layout simulation
 - A unit-size transistor with parasitic effects.

Ideal transistor LUT

V_G	V_D	V_S	C_s/I_D
1.1	0.9	1.5	2.0
1.1	0.9	1.6	1.3
1.1	0.9	1.8	0.7
⋮			

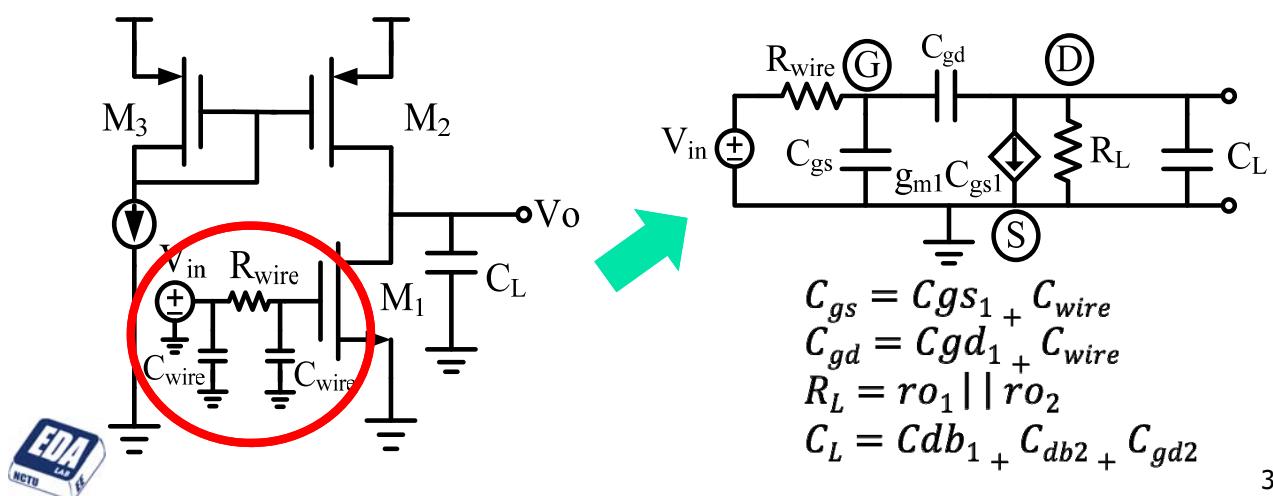
Parasitic-aware transistor LUT

V_G	V_D	V_S	C_s/I_D
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1.1	0.9	1.6	1.6
1.1	0.9	1.8	0.9
⋮			

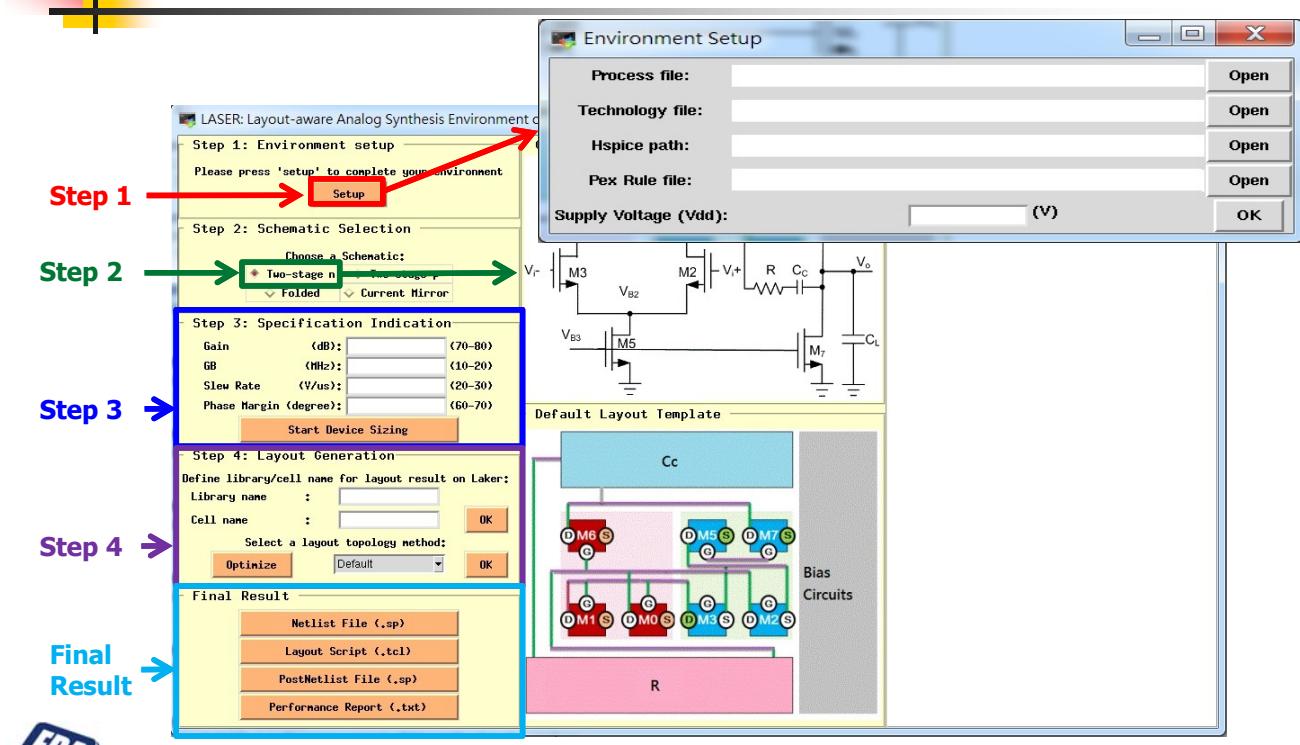
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Parasitic-Aware Performance

- Consider parasitic components in the circuit equations
 - For example, transfer function of this amplifier = $\frac{V_o(s)}{V_{in}(s)}$
- $$= \frac{g_{m1}R_L[1 - s\left(\frac{C_{gd_1}}{g_{m1}}\right)]}{1 + s[C_{gs}(R_{wire} + g_{mro_2}R_{wire} + RL) + CLRL] + s^2[(C_L + C_{gd})C_{gs} + CLC_{gd}]R_{wire}R_L}$$



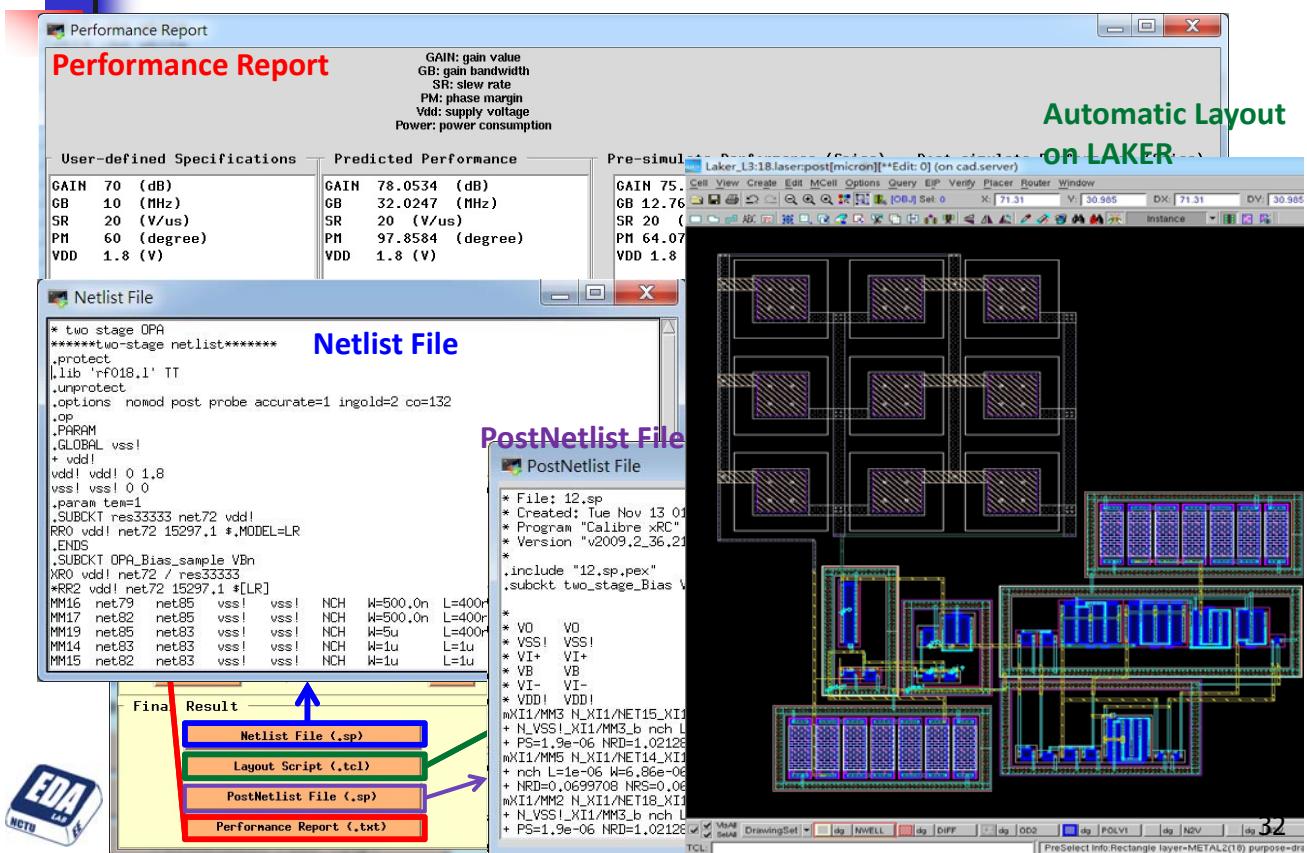
Graphical User Interface (GUI)



Ref: Y.-C Liao, Y.-L. Chen, X.-T. Cai, C.-N. J. Liu, and T.-C. Chen, "LASER - Layout-aware Analog Synthesis Environment on Laker", ACM/IEEE Great Lakes Symp. on VLSI, and Test , May 2013

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Final Results



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Experimental Results

- Test Circuit : Two-stage OPA, TSMC 0.18um process
- GB of conventional approach fails to meet spec. after layout
- Preserving design margins may incur too much overhead

Perf.	Conventional	5% margin	Parasitic-aware
Gain ≥ 75 (dB)	75.5+ 75.1++	78.9+ 78.5++	75.9+ 75.7++
GB ≥ 20 (kHz)	20.1+ 19.2++	22.5+ 21.9++	20.5+ 20.2++
SR ≥ 2 (V/ms)	2.6+ 2.2++	3.3+ 3.0++	2.8+ 2.6++
PM ≥ 60 (°)	68.5+ 67.9++	69.8+ 67.9++	68.7+ 68.3++
Power(mW)	2.17	3.54	2.18
Area (μm²)	4479	4850	3344
Time (sec.)	< 1	< 1	< 1

+: pre-sim.
++: post-sim.

Ref: Y.-C Liao, Y.-L. Chen, X.-T. Cai, C.-N. J. Liu, and T.-C. Chen, "LASER - Layout-aware Analog Synthesis Environment on Laker", ACM/IEEE Great Lakes Symp. on VLSI, and Test , May 2013

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Outline

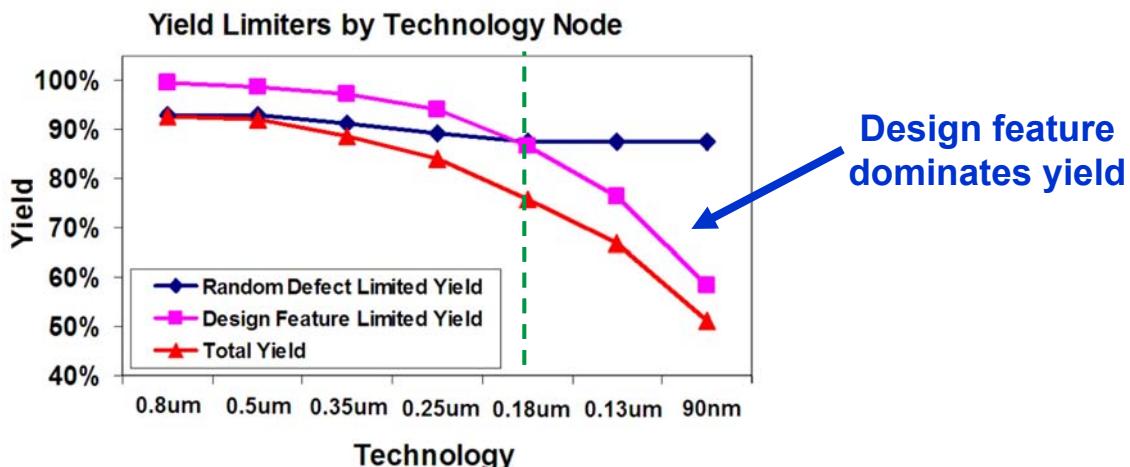
- Motivation
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- **Yield-Aware Synthesis Approach**
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Yield Loss Issues

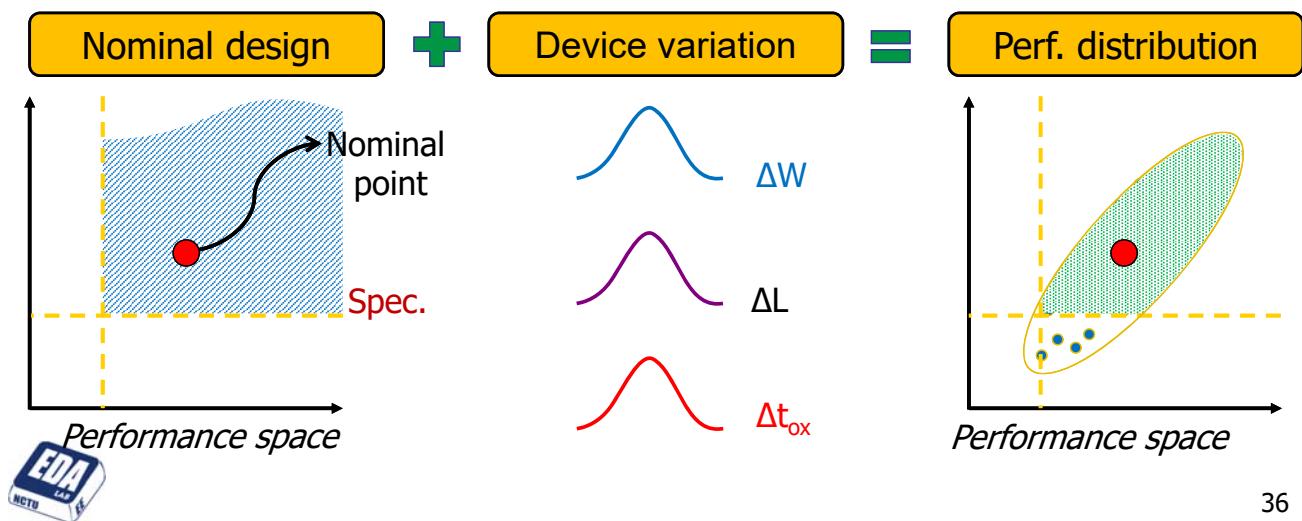
- In deep-submicron technology, **parametric variability** induce serious **yield loss** issues
- Parametric variability will dominate yield loss
- Yield affects the total cost of the products



Yield Analysis Method - Monte Carlo

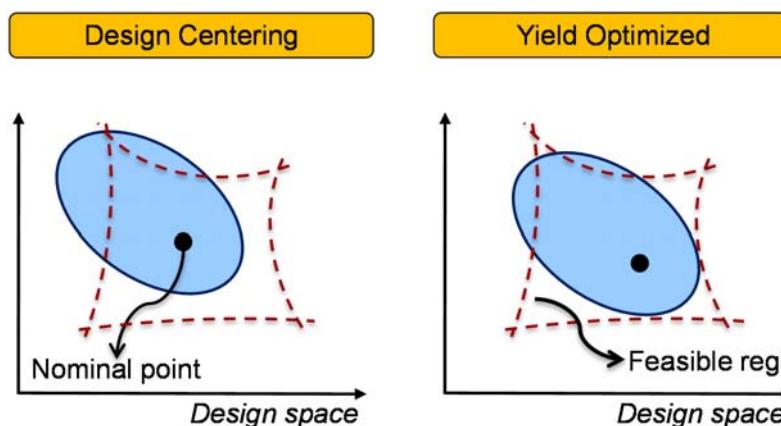
- Generate random samples to obtain performance distribution via simulation
 - High accuracy
 - High cost

$$Yield = \frac{N_{pass}}{N_{fail} + N_{pass}} \cdot 100\%$$



Yield Improvement Approaches

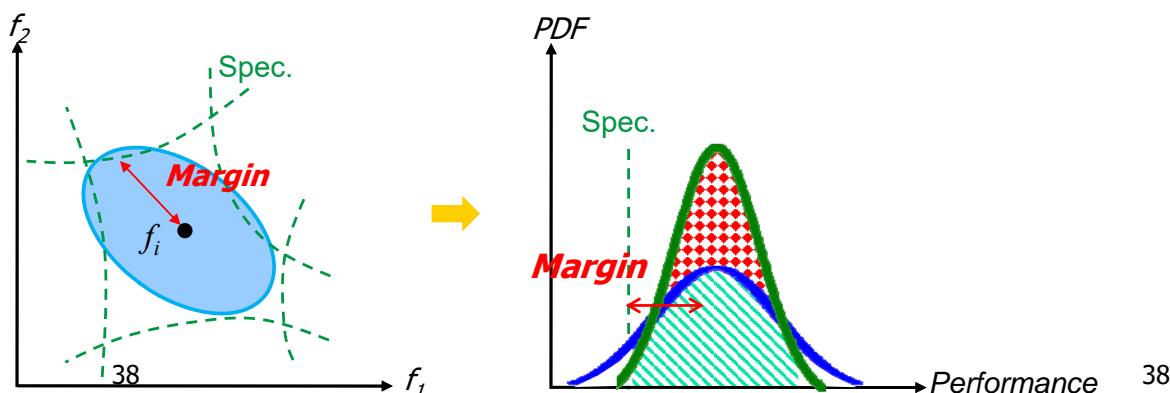
- Leaving “enough” design margin is the most popular way
 - How much is enough? → often results in too much **over design**
- Design centering** is a typical yield improvement method
 - Make the nominal design far away from performance boundary
- “Center” cannot guarantee the yield-optimized design
 - The **process sensitivity** of each performance may be different



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Design Centering

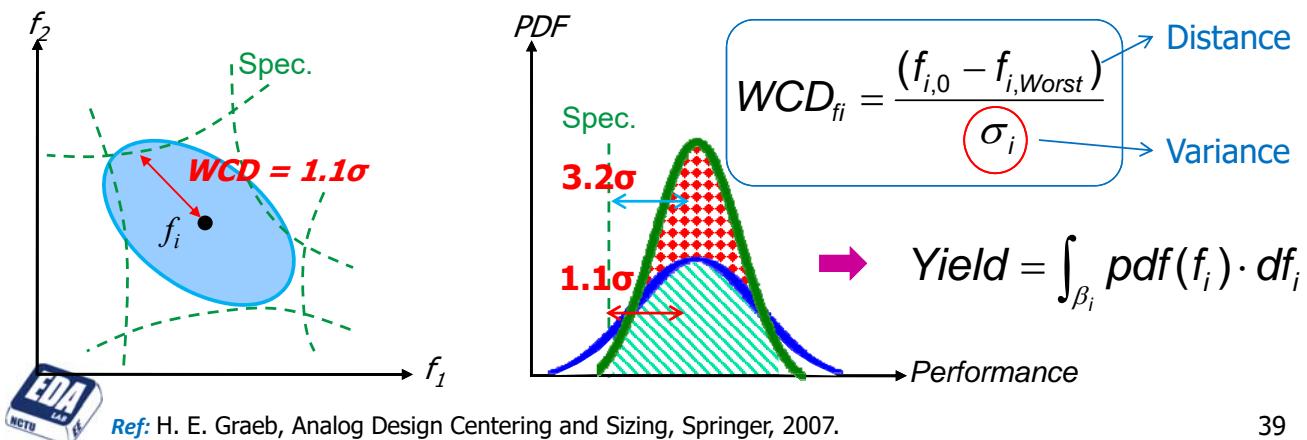
- Design centering approach is often used to improve the design-based yield
- Centered design has bigger distance to specifications
 - Performances have higher probability to locate in feasible region under process variations
- Higher distance = Higher yield ?



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Worst Case Distance (WCD) Analysis

- Corner analysis is only a conservative check
 - Cannot be used to guide yield optimization
- Simulation-based evaluation (Monte Carlo analysis) requires too much simulations → time consuming
- Equation-based worst case distance (**WCD**) is proposed
 - Both the nominal point and performance variance are considered



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Related Work – Yield-Aware Synthesis

- Simulation-based - higher accuracy, lower speed
 - Use WCD to consider variation
 - [1] – Hierarchical analysis to short run time
 - Use Pareto front to consider variation
 - [2] – Consider mismatch effect
- Equation-based - lower accuracy, higher speed
 - Design centering based approach
 - [3] – Move design to the center of feasible region
 - [4] – Move design to the center of performance space

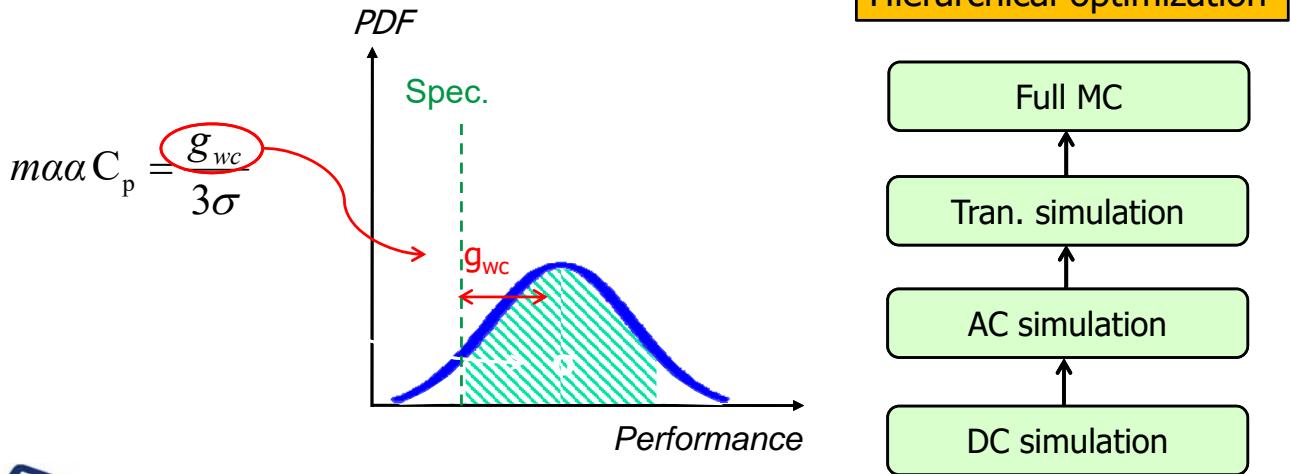
Ref:

- [1] T. McConaghy *et. al.*, "Globally Reliable Variation-Aware Sizing of Analog Integrated Circuits via Response Surfaces and Structural Homotopy," IEEE Trans. on CAD, vol. 28, no. 11, pp. 1627-1640, Nov. 2009
- [2] D. Mueller-Gritschneider *et. al.*, "Computation of Yield-Optimized Pareto Fronts for Analog Integrated Circuit Specifications," in DATE, 2010
- [3] S. Deyati *et. al.*, "An Automated Design Methodology for Yield Aware Analog Circuit Synthesis in Submicron Technology," Int'l Symp. on Quality Electronic Design, 2011
- [4] Xin Li *et. al.*, "Performance-Centering Optimization for System-Level Analog Design Exploration," in ICCAD, 2005



Simulation-Based Synthesis Using WCD

- Use process capability (C_p) to guarantee yield of circuits
 - WCD at performance space
 - High g_{wc} or low variance (σ) → Higher probability to achieve spec.
- Synthesis time is less than **overnight**

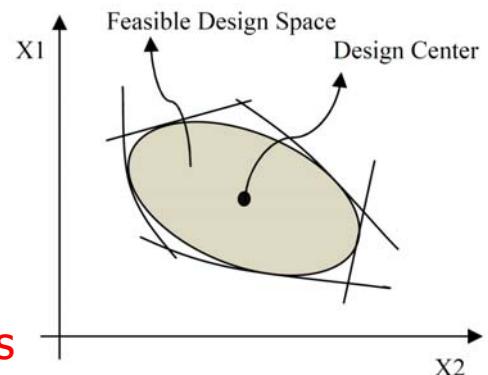


Ref: T. McConaghy *et. al*, "Globally Reliable Variation-Aware Sizing of Analog Integrated Circuits via Response Surfaces and Structural Homotopy," IEEE Trans. on CAD, vol. 28, no. 11, pp. 1627-1640, Nov. 2009

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Eq.-Based Synthesis via Centering

- Use equations to define the boundary of feasible region
 - Move the design to the center of feasible region
 - Derive equations of g_m and g_{ds} using regression
 - May overdesign too much
- Examples
 - Saturation operating constraints
 - $V_d > V_g - V_t$
 - Performance specifications
 - $gm_1 \cdot gm_2 = \text{Gain} > 70 \text{ (dB)}$
- Synthesis time is about **30 seconds**
- Neglect performance variance (σ)
 - Yield could be further improved

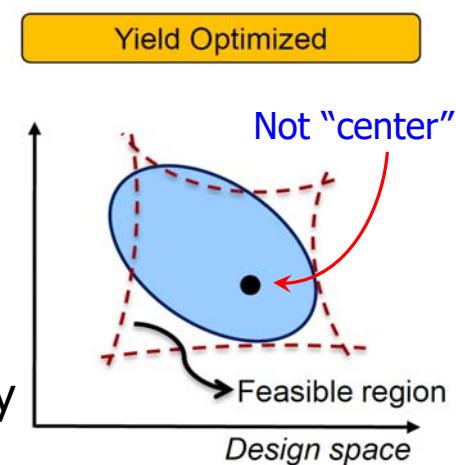


Ref: S. Deyati *et. al*, "An Automated Design Methodology for Yield Aware Analog Circuit Synthesis in Submicron Technology," Int'l Symp. on Quality Electronic Design, 2011

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Variation-Aware Synthesis Approach

- Adopt equation-based approach for fast synthesis
 - With accuracy improvement
- Using WCD concept to predict the design yield
 - Consider nominal point and performance variance simultaneously
- How to obtain the variance of performance distribution is the key
 - A hierarchical variation analysis is adopted to calculate the WCD without simulations
 - Estimate circuit yield quickly

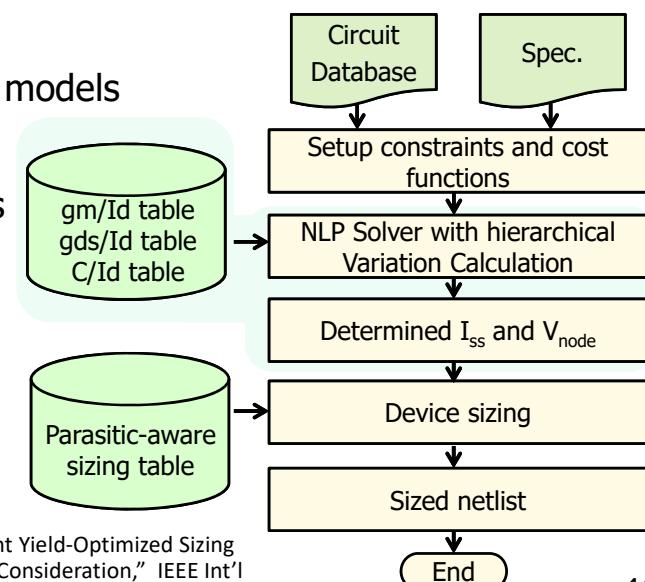


Ref: Y.-L. Chen, Y.-C. Ding, Y.-J. Lin, C.-N. J. Liu, "Efficient Yield-Optimized Sizing Approach for Analog Circuits with Accurate Variation Consideration," IEEE Int'l Workshop on Design for Manufacturability and Yield, 2012.

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Yield-Optimized Ckt. Sizing Flow

- Equation-based approach is adopted
 - Simulation-based approach is too slow → often several hours
 - Equation-based approach can be done in seconds
- Input
 - Performance spec., device models
- Output
 - Corresponding device sizes
- Objective
 - **Max** value of *WCD*
- Constraints
 - Operation range
 - Power/area bounds

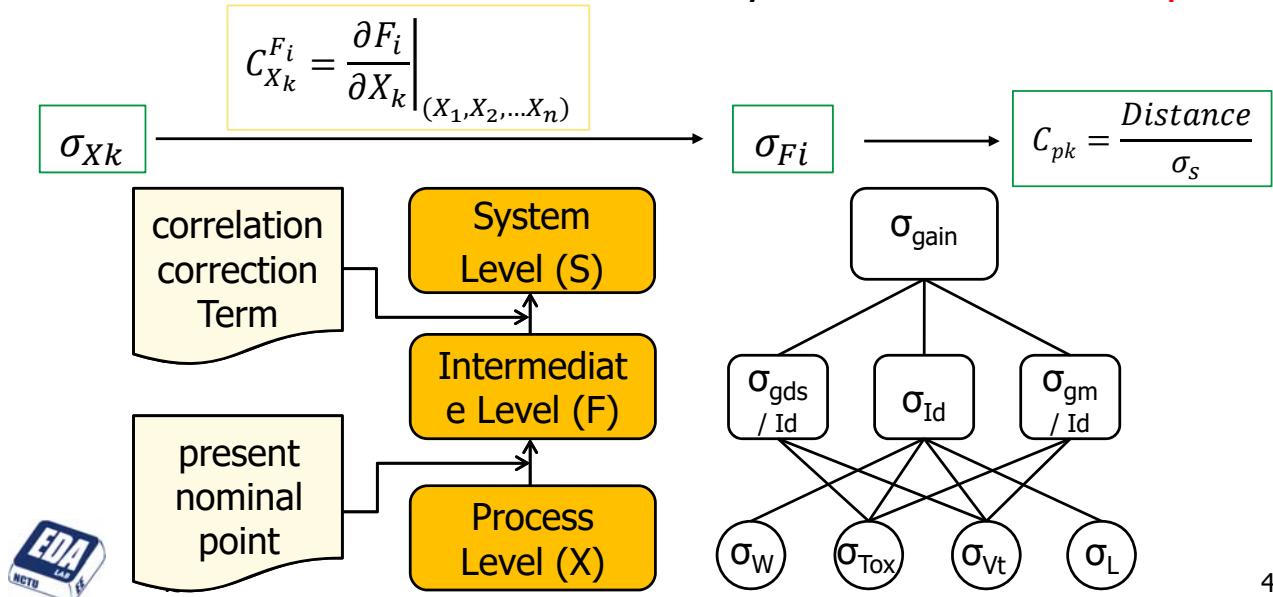


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Hierarchical Variance Analysis

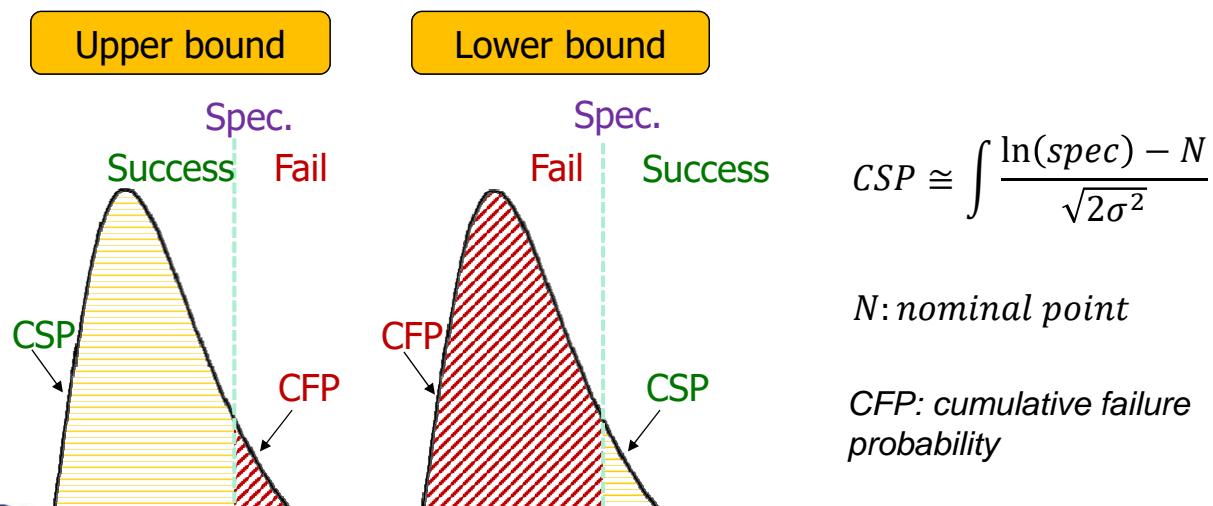
- Analyzing variance of system performances in one step is too complex
- Use hierarchical variance analysis → **faster and simpler**



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Cumulative Success Probability (CSP)

- In order to obtain better design yield, the cumulative success probability (CSP) should be maximized
- Not only limited on symmetrical distribution (ex: normal)



Ref: Y.-L. Chen, W.-R. Wu, C.-N. J. Liu, J. C.-M. Li, "Simultaneous Optimization of Analog Circuits with Reliability and Variability for the Applications on Flexible Electronics," IEEE Trans. on CAD, vol. 33, no. 1, pp. 24-35, Jan. 2014.

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Experiment Results -- OPA

- Without yield consideration, design yield is not good (**19.4%**)
- Design centering approach (**distance**) improves the yield with too much overhead (**20%**)
- With power constraints (**WCD+P**), WCD-based approach obtains higher yield (**97.2%**) and lowest overhead

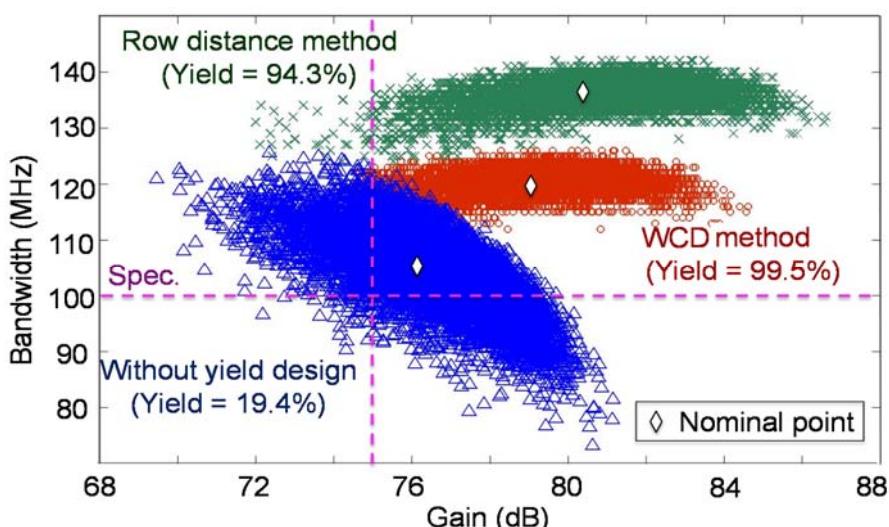


Performance	w/o yield	distance	WCD	WCD+P
Gain ($\geq 75\text{dB}$)	74.1	79.8	77.0	77.6
GB ($\geq 100\text{MHz}$)	99.3	134.9	116.9	113.0
SR ($\geq 60\text{V}/\mu\text{s}$)	61.9	72.0	66.7	64.4
PM ($\geq 55^\circ$)	50.6	57.3	60.4	61.1
Overall Results	Power(μw)	371.1	425.3	397.8
	Overhead (%)	-	14.61	7.19
	Area(μm^2)	227.7	274.8	235.7
	Overhead (%)	-	20.69	3.51
	Yield (%)	19.4	94.3	99.5
	Time (sec)	< 1	< 1	< 1

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Performance Distribution -- OPA

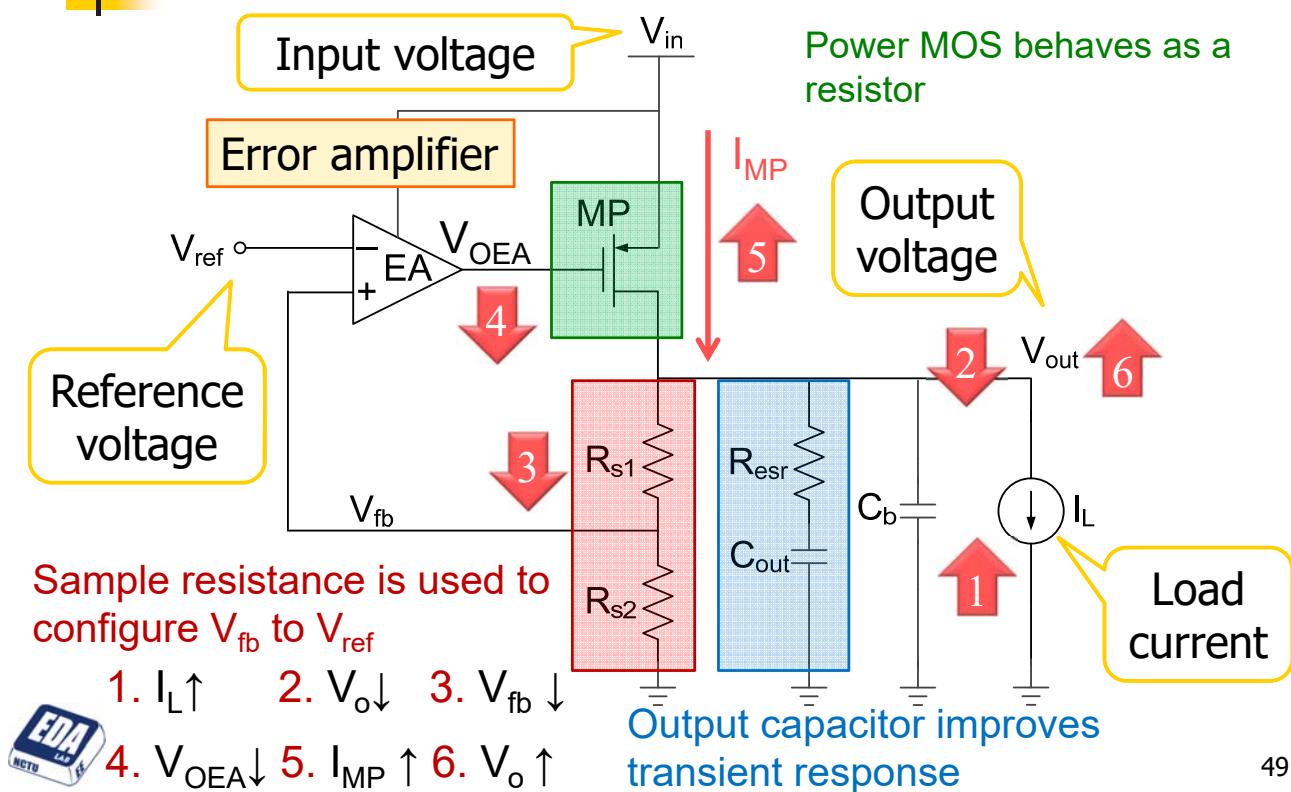
- The results of WCD-based method are more close to the performance boundary → reduce over-design
- The performance distribution is also shrunk with WCD-based approach
 - Different variance for each performance is also considered



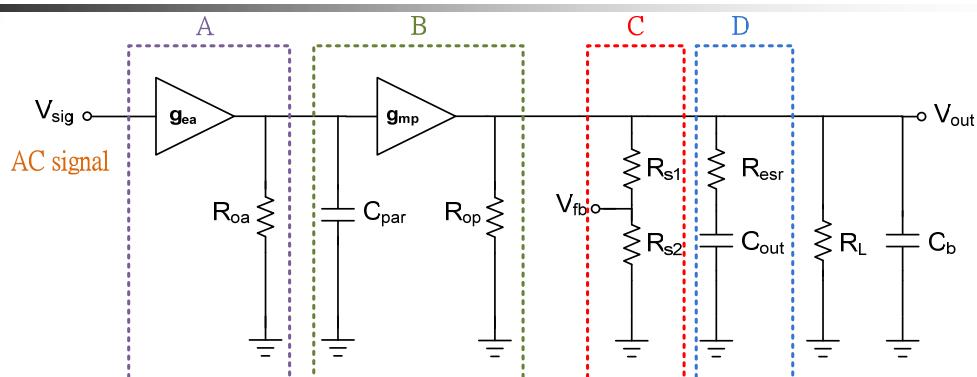
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Ex: Low Dropout Regulator (LDO)



Frequency Domain Analysis



$$Z_{out} = R_{op} \parallel (R_{s1} + R_{s2}) \parallel R_L \parallel \left(R_{esr} + \frac{1}{sC_{out}} \right) \parallel \left(\frac{1}{sC_b} \right)$$

$$P_{EA} = \frac{1}{2\pi R_p C_p}$$

$$P_{MP} = \frac{1}{2\pi R_{op} C_0}$$

$$Z_1 = \frac{1}{2\pi R_{esr} C_0}$$

$$UGF = \sqrt{\beta A_{EA} g_m R_{op}} \times (1 + (\frac{UGF}{Z_1})^2)^{\frac{1}{4}} \times \sqrt{P_{EA} P_{MP}}$$

$$PM = \tan^{-1}(\frac{UGF}{Z_1})$$



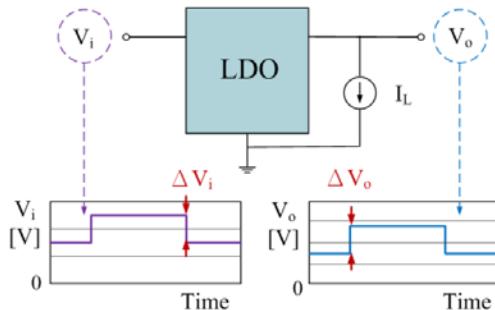
Ref: S. DasGupta, P. Mandal, "An Automated Design Approach for CMOS LDO Regulators", ASPDAC 2009.

Performance Constraints

- Line regulation: the output voltage variation arising from a specific change in input voltage

$$\text{Line regulation} = \frac{\Delta V_{out}}{\Delta V_{in}}$$

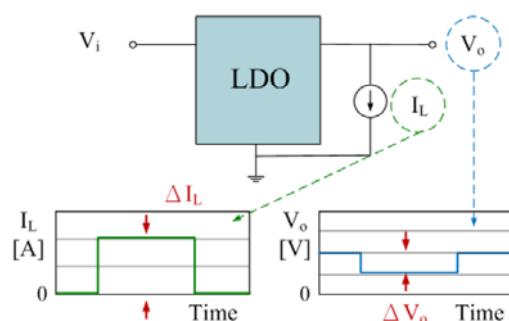
$$\approx \frac{R_{s1} + R_{s2}}{R_{s2}} \times \frac{1}{A_{EA} \times g_{mp} \times (R_{op} + R_L)}$$



- Load regulation: the change in output voltage for specific changes in load-current

$$\text{Load regulation} = \frac{\Delta V_{out}}{\Delta I_{out}}$$

$$= \frac{R_{s1} + R_{s2}}{R_{s2}} \times \frac{1}{A_{EA} \times g_{mp}}$$



Settling Time Constraints

- Settling time = $T_{ss} + T_{sl}$
 - T_{sl} : large signal settling time

$$T_{sl} \approx \frac{V_{ov} p |I_{L\max}|}{SR}$$

V_{ov}: overdrive voltage
SR: slew rate of error amplifier

- T_{sl} is determined by the slewing time required for charging up the pass transistor gate capacitance
- The slew rate of error amplifier \uparrow , $T_{sl} \downarrow$

- T_{ss} : small signal settling time

$$T_{ss} \approx \frac{1}{BW_{close-loop}}$$

$BW_{close-loop}$: close loop bandwidth of LDO

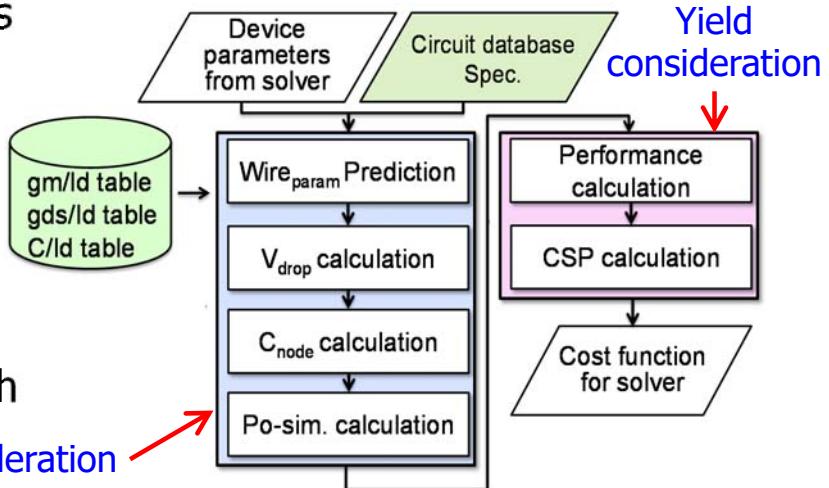
- The close loop bandwidth is equivalent to the open loop unity gain frequency.
- The open loop unity gain frequency \uparrow , $T_{ss} \downarrow$



Synthesis with Non-Idealities

- The error amplifier is not an ideal OP
 - Finite gain, finite bandwidth, ...
 - Parasitic effects change the post-layout performance
 - Process variation is getting larger
 - As mentioned in previous section
 - Those issues are considered together in the proposed approach

```
graph TD; subgraph Inputs [ ]; direction TB; A[Device parameters from solver]; B[Circuit database Spec.]; end; subgraph DB [ ]; direction TB; C[(gm/lid table  
gds/lid table  
C/lid table)]; end; A --> D[Wire_param Prediction]; B --> D; C --> D; D --> E[V_drop calculation]; E --> F[C_node calculation]; F --> G[Performance calculation]; G --> H[CSP calculation]; H --> I[Cost function for solver];
```



Ref: Y.-L. Chen, G.-M. Chu, Y.-C. Lien, C.-M. Lee, C.-N. J. Liu, "Simultaneous Optimization for Low Dropout Regulator and Its Error Amplifier with Process Variation," IEEE Int'l Symp. on VLSI Design, Automation, and Test, Apr. 2014.

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Simultaneous Optimization with EA

- The terms about EA cannot be assumed as infinite
 - Ex:

$$Load = \frac{\Delta V_o}{\Delta I_L} = \frac{R_{s1} + R_{s2}}{R_{s2}} \times \frac{1}{A_{EA} \times g_{mp}}$$
 - Replace the EA terms with real equations
 - In order to apply g_m/I_d based approach, the whole equation is rewritten as g_m/I_d form
 - Ex:

$$Load = \frac{\left(\frac{g_{d0}}{I_{ss}/2} + \frac{g_{d2}}{I_{ss}/2}\right) \cdot \left(\frac{g_{d6}}{k \cdot I_{ss}} + \frac{g_{d7}}{k \cdot I_{ss}}\right)}{\beta \cdot \frac{g_{m2,3}}{I_{ss}/2} \cdot \frac{g_{m6}}{k \cdot I_{ss}} \cdot \frac{g_{mp}}{I_{mp}}}$$
 - Optimize with the new performance equations automatically considers both LDO and EA



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Experimental Results -- LDO

- Reach all specifications with the consideration of the *error amplifier, parasitic effects* and *process variation*

Perf.	Spec.	Mandal [1]	Nominal	Layout	DFY	Unified
t_{settle} (μ s)	< 0.50	0.52	0.47+ 0.52*	0.45+ 0.49*	0.22+ 0.35*	0.37+ 0.42*
Line (mV/V)	< 0.05	0.039	0.041+ 0.049*	0.044+ 0.049*	0.027+ 0.039*	0.030+ 0.035*
Load (mV/A)	< 0.10	0.084	0.095+ 0.131*	0.054+ 0.057*	0.052+ 0.071*	0.081+ 0.084*
Power (μ W)	-	64.7	60.5	61.3	70.0	65.1
Area (μ m ²)	-	738.8	469.3	472.7	477.5	478.2
#Fail corner	-	-	3+ 4*	2+ 2*	0+ 1*	0+ 0*
Yield (%)	-	-	47.3+ 23.5*	76.5+ 53.3*	100.0+ 93.4*	100.0+ 100.0*

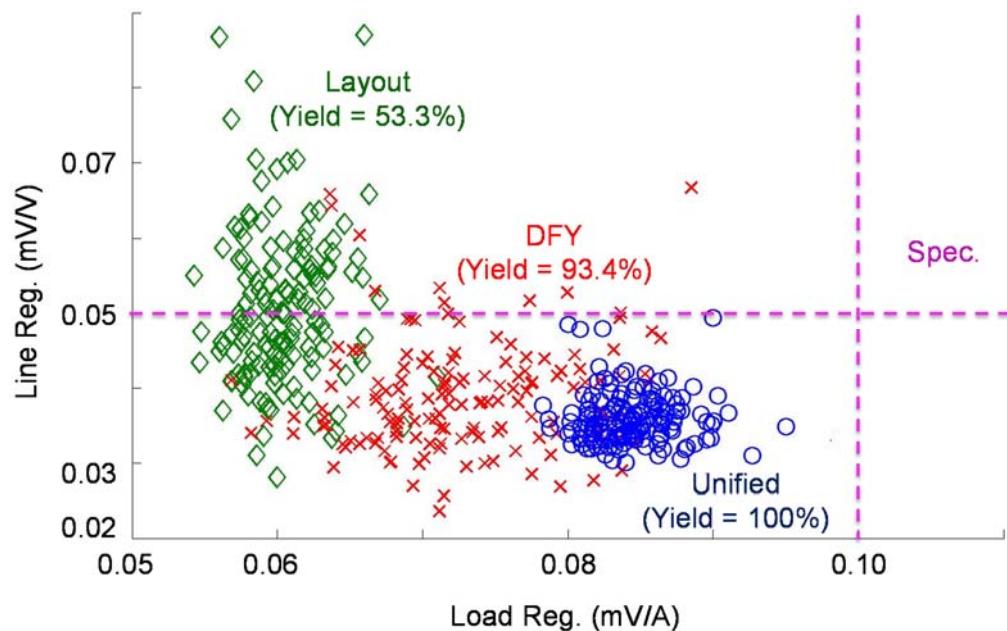
⁺: pre-sim.
^{*}: post-sim.

[1] S. DasGupta, and P. Mandal, "An Automated Design Approach for CMOS LDO Regulators", in Proc. Asia and South Pacific Design Automation Conf., pp. 510-515, 2009.

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Performance Distribution -- LDO

- The performance distribution meets all spec. even in post-layout simulations !!



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Outline

- Motivation
- Parasitic-Aware Synthesis Approach
- Yield-Aware Synthesis Approach
- Aging-Aware Synthesis Approach



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Flexible Electronics

- Large area, flexible and printed electronics
 - Flexible thin-film transistor (TFT)
- Advantages
 - Low manufacturing cost
 - Short manufacturing time
 - Lightweight
 - Flexibility
- Applications
 - Flexible display
 - e-paper, e-skin
 - Wearable computing
 - ...



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Comparison of CMOS & Flexible TFT

		Device technology			
Technology parameter	CMOS	Amorphous Si TFT	Amorphous IGZO TFT	SAM organic TFT	Ink-jetted organic TFT
Process temperature	1,000C	250C	<100C	<100C	Room temperature
Process technology	Lithography	Lithography	Roll-to-roll lithography	Shadow mask	Ink-jet printing
Substrate	Wafer	Glass or plastics	Glass or plastics	Wafer or plastics	Glass or plastics
Device type	Complementary	N-type only	N-type only	Complementary	P-type only
Mobility (cm ² /Vs)	1,500	1	10	0.01 or 0.5 (n- or p-type)	0.01
Cost/Area	High	Medium	Low	Low	Low
Lifetime	Very good	Good	Good	Medium	Poor

Ref: T. Huang, et al., "Robust circuit design for flexible electronics," IEEE Design & Test of Computers, Nov. 2011. 59

Design Issues with Flexible TFTs

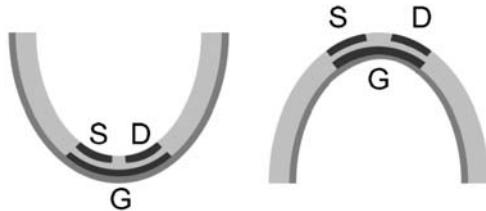
- Process variation & bending effects
 - Critical parameter variations [1]
- Aging effects
 - Short lifetime [2]
- Only mono-type devices
- Low carrier mobility
 - Slow operation speed
- High supply voltage
 - High power consumption

[1] H. Gleskova, et al., "Electrical response of amorphous silicon thin-film transistors under mechanical strain," Journal of Applied Physics, vol.92, no.10, pp.6224-6229, Nov. 2002.

[2] R. Shringarpure, et al., "Circuit simulation of threshold-voltage degradation in a-Si: H TFTs fabricated at 175°C," IEEE Transactions on Electron Devices, vol.54, no. 7, pp. 1781-1783, Jul. 2007.

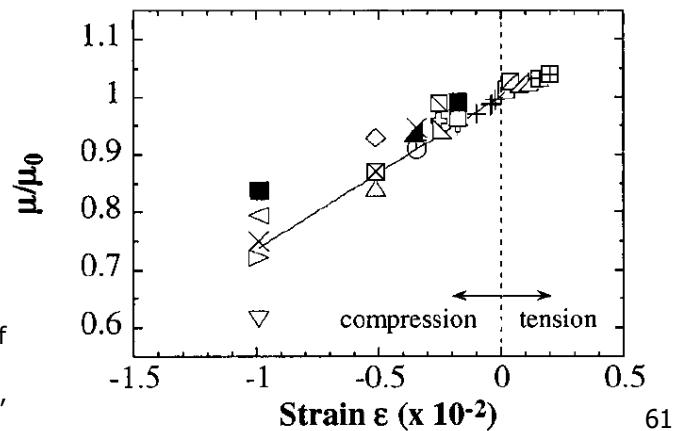
Bending Effects

- Compressive strain & tensile strain



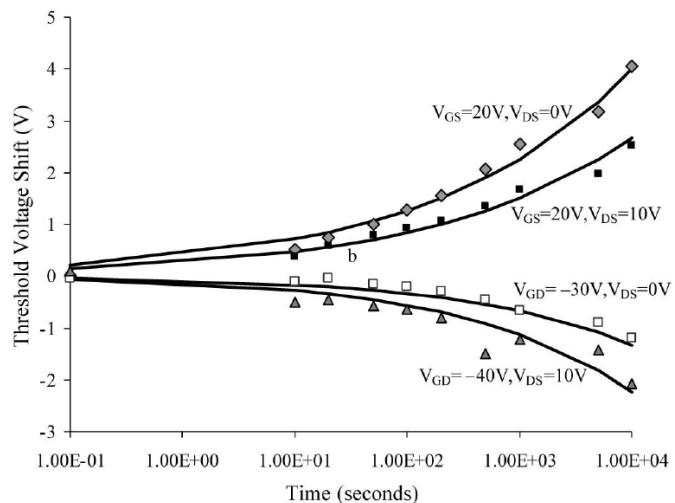
- Serious mobility change under bending

- Max decreasing -26%
- Max increasing 7.6%



Aging Effects

- Change of transistor parameters (V_t , r_o) over time
- Performance degrades when exposed in the ambient air or under continuous bias-stress
- Significantly reduce yield and reliability



Ref: R. Shringarpure, et al., "Circuit simulation of threshold-voltage degradation in a-Si: H TFTs fabricated at 175°C," IEEE Trans. on Electron Devices, vol.54, no. 7, pp. 1781-1783, Jul. 2007.



Simulation-Based Aging Analysis

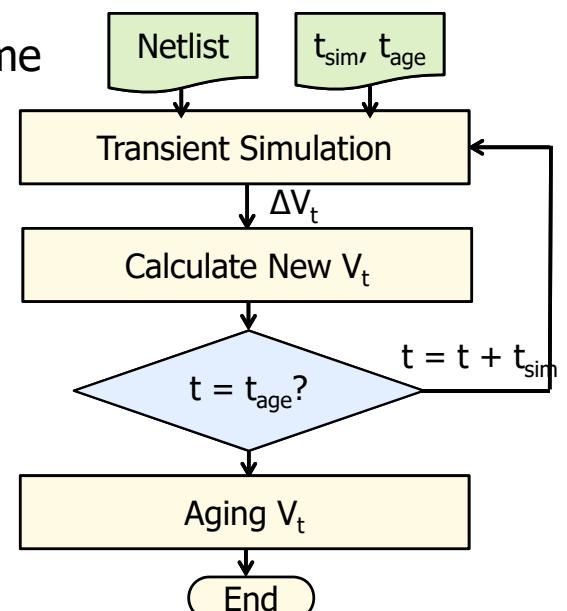
- Incrementally calculate the degradation that each transistor suffers
- Often require long simulation time

$$\Delta Age(\Delta t_i) = \int_{t_{i-1}}^{t_i} \left(A^{-\beta} \exp\left(\frac{-E_A}{\beta kT}\right) (V_{GS} - \eta V_{DS} - V_t)^{\frac{\eta}{\beta}} \right) dt$$

$$Age(t_{sim}) = \sum_{i=0}^N \Delta Age(\Delta t_i)$$

$$Age(t_{age}) = \frac{t_{age}}{t_{sim}} Age(t_{sim})$$

$$\Delta V_t(t_{age}) = [Age(t_{age})]^{\beta}$$

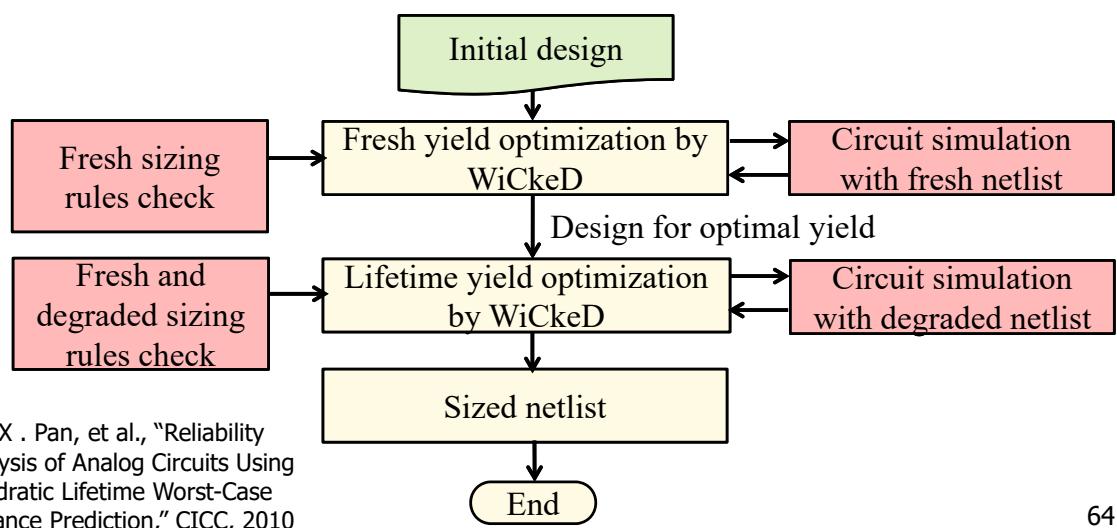


Ref: R. Shringarpure, et al., "Circuit simulation of threshold-voltage degradation in a-Si:H TFTs fabricated at 175°C," IEEE Trans. on Electron Devices, vol.54, no. 7, pp. 1781-1783, Jul. 2007.

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2-Stage Design-for-Reliability Flow

- Only the **fresh yield** is considered in the first stage
- Only the **lifetime yield** is considered in the second stage
 - The optimal point of stage 1 will be changed
 - The fresh yield may no longer be the best value



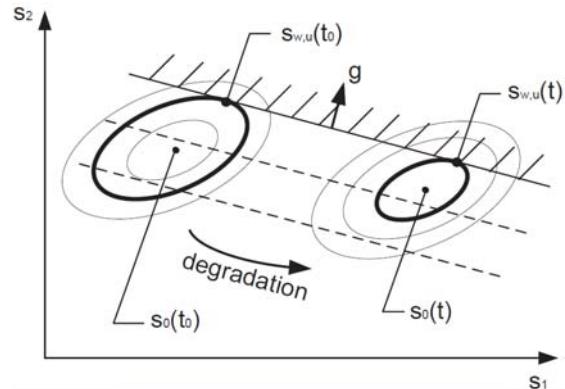
Ref: X . Pan, et al., "Reliability Analysis of Analog Circuits Using Quadratic Lifetime Worst-Case Distance Prediction," CICC, 2010

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Linear Performance Model for CMOS

- Assume that the sensitivity of performance over statistical parameters keeps constant

$$\beta_{w,u}(t) = \beta_{w,u}(t_0) + \frac{d\beta_{w,u}(t)}{dt} \Big|_{t_0} \cdot (t - t_0)$$



- Cannot be applied on flexible electronics directly
 - Aging effects are much more significant in flexible TFT

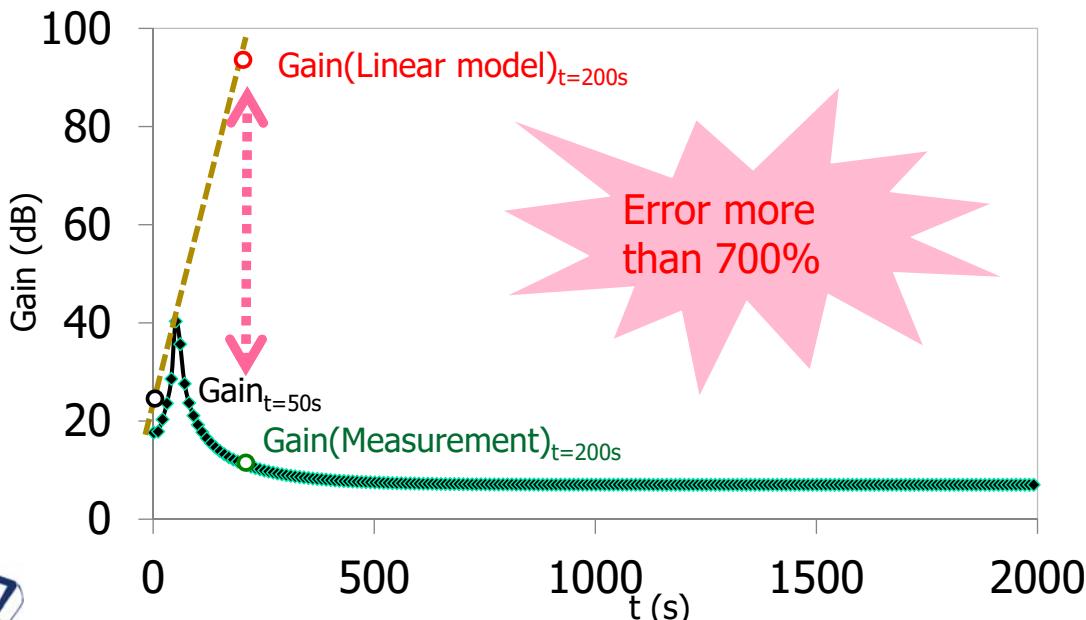


Ref: X. Pan, et al., "Lifetime yield optimization of analog circuits considering process variations and parameter degradations," Advances in Analog Circuits, InTech, Feb. 2011.

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Errors of Linear Model

- Aging variations on flexible TFT's parameters are much greater than the variations on CMOS.



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DFR Flow for Flexible Electronics

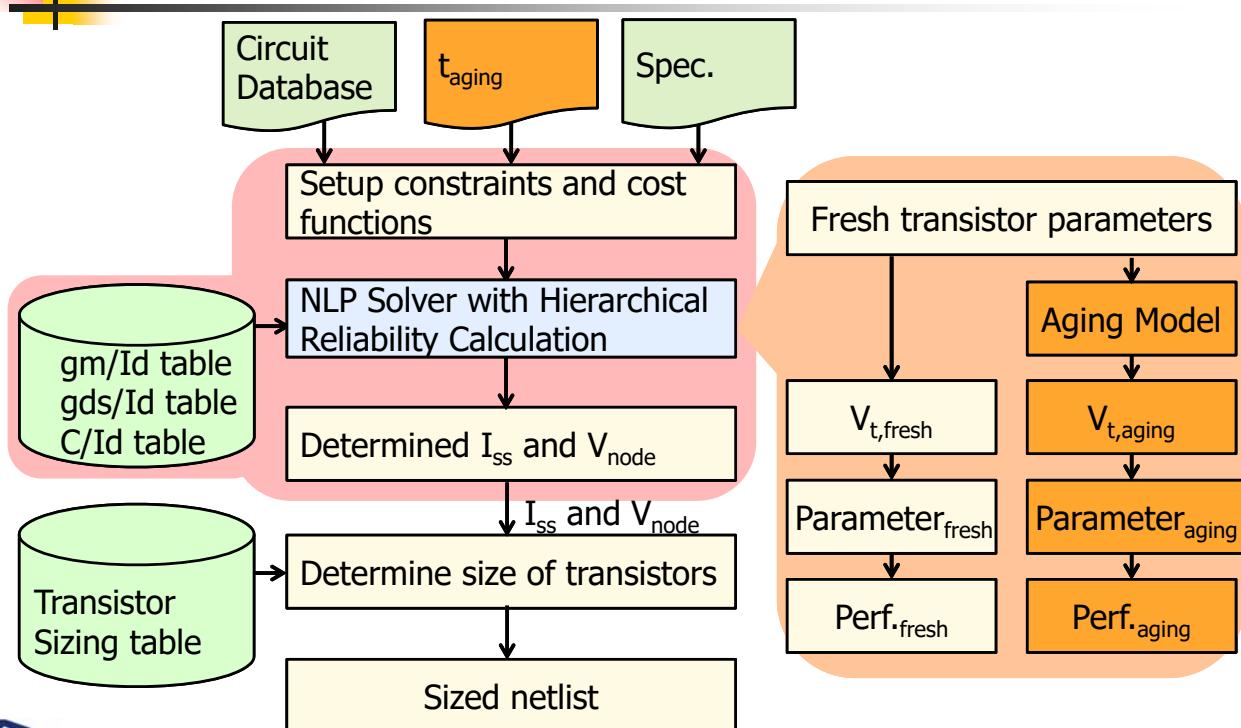
- Design yield of flexible circuit is reduced significantly
 - Product cost ↑
- Mobility changes significantly when bended
 - $\Delta\mu$ is 26% under bending [1]
- V_t increases significantly when operated
 - ΔV_t is 4~5V when operated 10,000s [2]
- It is difficult for designers to consider so many effects when designing flexible TFT circuits
- An **automatic synthesis methodology** considering **yield and reliability** is required for flexible TFTs

[1] H. Gleskova, et al., "Electrical response of amorphous silicon thin-film transistors under mechanical strain," Journal of Applied Physics, vol.92, no.10, pp.6224-6229, Nov. 2002.

[2] R. Shringarpure, et al., "Circuit simulation of threshold-voltage degradation in a-Si:H TFTs fabricated at 175°C," IEEE Transactions on Electron Devices, vol.54, no. 7, pp. 1781-1783, Jul. 2007.

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Aging-Aware Circuit Sizing Flow



Ref: Y.-L. Chen, W.-R. Wu, C.-N. J. Liu, J. C.-M. Li, "Simultaneous Optimization of Analog Circuits with Reliability and Variability for the Applications on Flexible Electronics," IEEE Trans. on CAD, vol. 33, no. 1, pp. 24-35, Jan. 2014.

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Exponential Aging Model

- Estimate the threshold voltage shift in a-Si TFT
- Evaluate the circuit performance after a given time period
- Assume only V_t is changed over time
 - The assumption of most previous works

$$\Delta V_t = (V_{GS} - V_t) \times \left\{ 1 - \exp \left[-\left(\frac{t}{\tau} \right)^{\beta} \right] \right\}$$

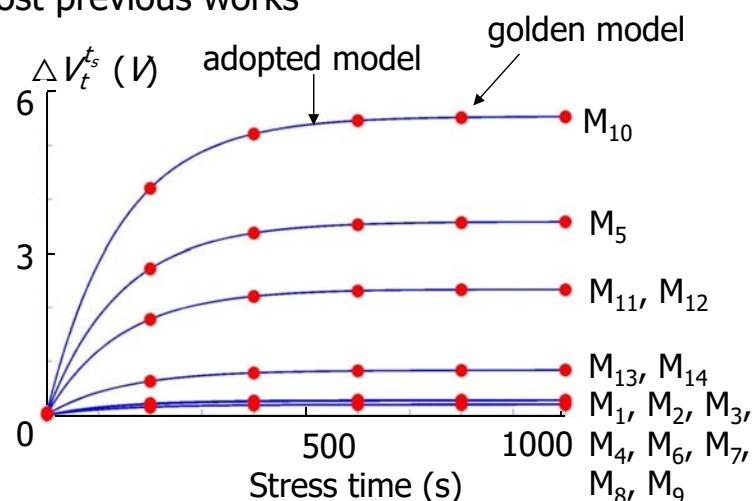
$$\tau = k(V_{GS} - V_t)^{\frac{1-\alpha}{\beta}}$$

ΔV_t : the threshold voltage shift

t : aging time

$k: 4.7 \times 10^4$

α, β : process parameter



Ref: S.-E. Liu, et al., "Estimate threshold voltage shift in a-Si:H TFTs under increasing bias stress," IEEE Transactions on Electron Devices, vol. 56, no. 1, pp. 56-59, Dec. 2009.

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Predict Aging g_m/I_D & g_{ds}/I_D

- Threshold voltage at t_{aging}

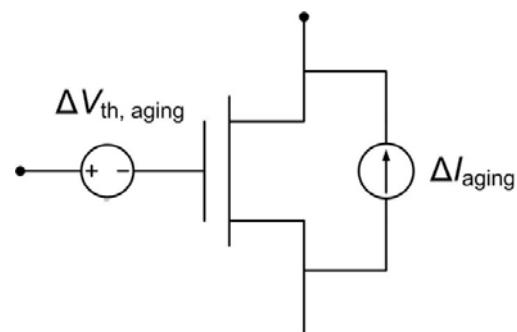
$$V_{t,aging} = V_{t,fresh} + \Delta V_t$$

- Fresh transistor parameters

$$\frac{g_{m,fresh}}{I_{D,fresh}} = \frac{2}{(V_{gs} - V_{t,fresh})}$$

- Aging transistor parameters

$$\frac{g_{m,aging}}{I_{D,aging}} = \frac{2}{(V_{gs} - V_{t,aging})} = \frac{2}{(V_{gs} - (V_{t,fresh} + \Delta V_t))} = \frac{2}{((V_{gs} - \Delta V_t) - V_{t,fresh})}$$



- Advantage

- Reuse the lookup table built with $V_{t,fresh}$
- Get the aging g_m and g_{ds} efficiently



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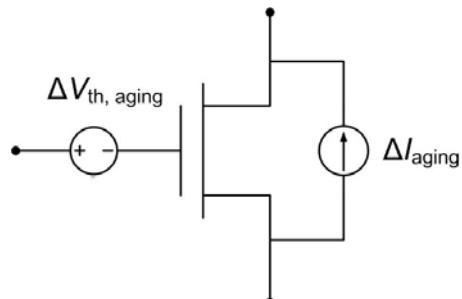
Modify Current and Constraints

- Assume that the node voltages are similar with degradation

$$\frac{I_{D,fresh}}{I_{D,aging}} = \left(\frac{V_{GS} - V_{t,fresh}}{V_{GS} - V_{t,aging}} \right)^\gamma$$

$$I_{D,aging} = I_{D,fresh} \times \left(\frac{V_{GS} - V_{t,aging}}{V_{GS} - V_{t,fresh}} \right)^\gamma$$

γ : process parameter



- Make sure all the transistors are still in right operation region after aging
 - For example, saturation region:

$$V_{GS,i} > V_{t,i,aging}$$

$$V_{GD,i} < V_{t,i,aging}$$



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Experimental Environment

- The experiments are performed on PC with Intel 4-core 2.66GHz CPU and 2GB memory
- ITRI 8μm a-Si TFT process
- Parameters variations
 - μ : -25% ~ 10%
 - V_t : ±20%
 - W and L: ± 3%
 - Aging time: 10000s
- NLP Solver: IBM CPLEX
- Yield verification
 - 1000-run Monte Carlo analysis with HSPICE simulator

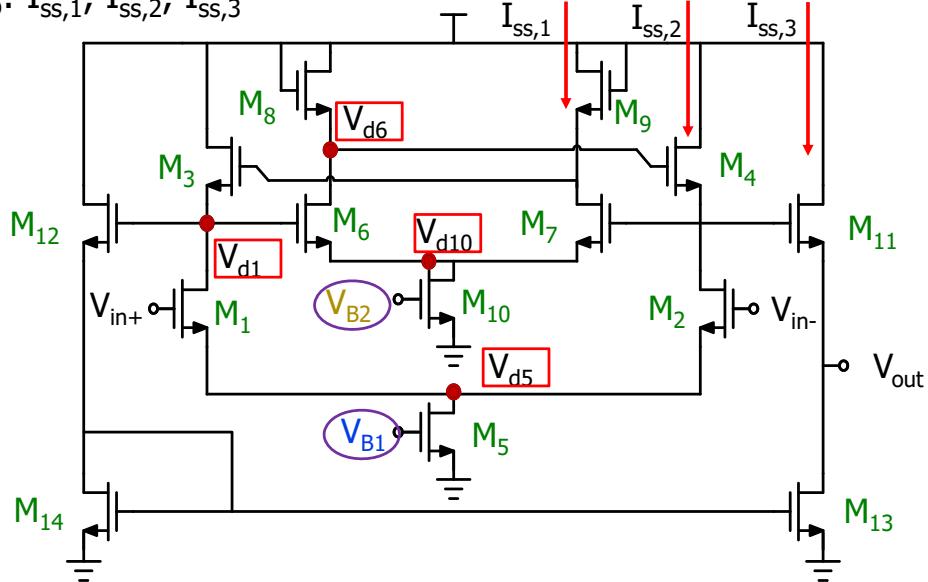


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Experimental Circuit: OPA

- Variables

- Node voltages: $V_{B1}, V_{B2}, V_{d1}, V_{d5}, V_{d6}, V_{d10}$
- I_D : $I_{ss,1}, I_{ss,2}, I_{ss,3}$



Ref: Y.-C. Tarn, et al., "An amorphous silicon operational amplifier and its application to 4 bit digital to analog converter," Journal of Solid-State Circuits, vol. 45, no. 5, pp. 1028-1035, May 2010.

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Experimental Results -- OPA

- Lifetime yield of WCD_{fresh} decays to 0% at $t_s=1000s$
- WCD_{quad} reaches 97.4% fresh yield with 28.9% area overhead
- Proposed method reaches 100% yield with 2.8% area overhead

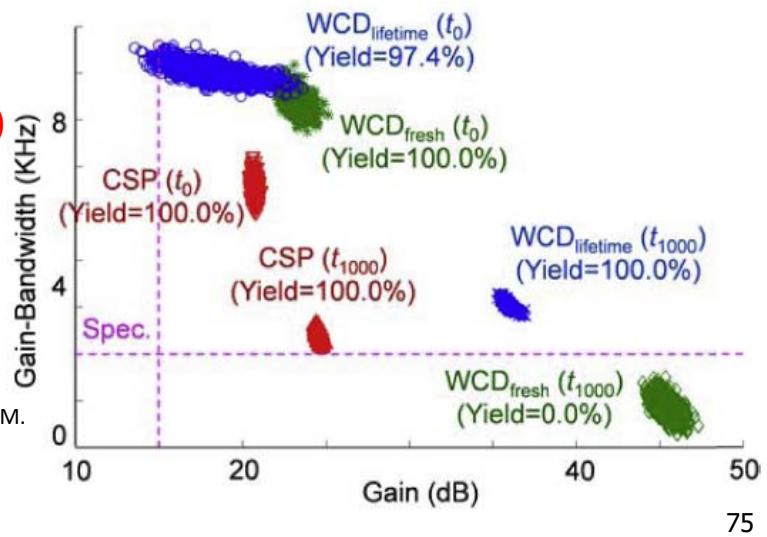
Performance	WCD_{fresh}		WCD_{quad} [1]		Proposed	
	t_0	t_{1000}	t_0	t_{1000}	t_0	t_{1000}
Gain	≥ 15 (dB)	23.7	45.3	18.2	36.2	20.7
GBW	≥ 2 (kHz)	7.4	0.8	8.2	2.8	5.6
SR	≥ 6 (V/ms)	16.7	6.5	17.9	14.0	14.5
PM	≥ 60 ($^{\circ}$)	84.1	43.5	75.6	73.1	72.0
Overall results	Power (mW)	18.7		22.8		21.0
	Overhead (%)	-		21.8		12.3
	Area (μm^2)	2940.2		3789.3		3021.8
	Overhead (%)	-		28.9		2.8
	Yield (%)	100.0	0.0	97.4	100.0	100.0
	Run Time (s.)	< 1		< 1		< 1

[1] X . Pan, et al., "Reliability Analysis of Analog Circuits Using Quadratic Lifetime Worst-Case Distance Prediction", CICC 2010.

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Performance Distribution -- OPA

- Lifetime yield of WCD_{fresh} becomes 0% with transistor degradation at $t_s=1000$
- The fresh yield of WCD_{quad} ($WCD_{lifetime}(t_0)$) is not optimal
 - Due to the two-stage optimization approach
- Proposed flow (CSP) reaches highest fresh & lifetime yield (100%)



Ref: Y.-L. Chen, W.-R. Wu, C.-N. J. Liu, J. C.-M. Li, "Simultaneous Optimization of Analog Circuits with Reliability and Variability for the Applications on Flexible Electronics," IEEE Trans. on CAD, pp. 24-35, Jan. 2014.

