



BL0910

Ten-phase AC power metering chip

Data Sheet

V1.01



Table of contents

Version information Error! Bookmark not defined.

Contents.....2

1. Product Description.....5

2. Basic features.....6

2.1 Main features.....	6
2.2 System Block Diagram.....	7
2.3 Pin Arrangement (LQFP48)	9
2.4 Performance Indicators.....	10
2.4.1 Electrical parameter performance.....	10
indicators 2.4.2 Limit range.....	11

3. Working Principle.....12

3.0 Current and Voltage Mode Selection.....	12
3.1 Principle of current and voltage waveform generation.....	12
3.1.1 Phase compensation.....	13
3.1.2 Channel offset correction	14
3.1.3 Channel gain correction	14
3.1.4 Current and voltage waveform output.....	15
3.2 Active Power Calculation Principles.....	16
3.2.1 Active power output	16
3.2.2 Active power calibration.....	17
3.2.3 Active power anti-creep 3.2.4	18
Active power small signal compensation.....	18
3.3 Principle of Active Energy Measurement.....	19
3.3.1 Active energy output	19
3.3.2 Active energy output selection.....	20
3.3.3 Active energy output ratio	20
3.4 Principle of Calculation of Effective Value of Current and Voltage.....	21
3.4.1 Effective value output	21
3.4.2 Current and voltage effective value	22
calibration 3.4.3 Effective value anti-creep.....	23
3.5 Fast Leakage/Overcurrent Detection Principle.....	23
3.5.1 Fast RMS output 3.5.2	23
Fast RMS cumulative time and threshold 3.5.3	24
Fast RMS save before reading 3.5.4	24
Overcurrent indication	25
3.5.5 Relay control	26
3.6 Reactive Power Calculation.....	26
3.6.1 Reactive power calculation input	27
selection 3.6.2 Phase compensation.....	27



3.6.3 Reactive power output27
3.6.4 Reactive power calibration.....	.28
3.6.5 Anti-creep of reactive power28
3.6.6 Reactive power small signal28
compensation 3.6.7 Reactive energy output.....	.29
3.7 Apparent and Power Factor Calculations.....	.29
3.7.1 Apparent Power and Energy29
Output 3.7.2 Apparent Power30
Calibration 3.7.3 Power Factor.....	.30
3.8 Temperature Measurement.....	.30
3.9 Electrical Parameter Measurement.....	.31
3.9.1 Line cycle measurement.....	.31
3.9.2 Line frequency31
measurement 3.9.3 Phase.....	.32
angle calculation 3.9.4 Power sign-bit.....	.32
3.10 Fault Detection.....	.33
3.10.1 Zero-crossing33
detection 3.10.2 Peak value33
exceeding the limit 3.10.3 Line34
voltage drop 3.10.4 Zero-.....	.35
crossing timeout 3.10.5 Power supply indication.....	.36
3.10.6 ADC shutdown.....	.37
4. Internal Registers.....	.37
4.1 Electrical Parameter Registers.....	.37
4.2 Calibration Register (External Write)41
4.3 Calibration Register (Writable)45
4.4 Mode Register.....	.47
4.4.1 Mode Register (MODE)47
4.5 Interrupt Status Register (STATUS1/STATUS2).....	.48
4.5.1 STATUS1 register 4.5.2.....	.48
STATUS3 register49
4.6 Detailed description of calibration registers.....	.50
4.6.1 Channel PGA gain adjustment register50
4.6.2 Phase correction register50
4.6.3 Effective value gain adjustment51
register 4.6.4 Effective value offset52
correction register 4.6.5 Active small signal52
compensation register 4.6.6 Reactive small.....	.53
signal compensation register 4.6.753
Anti-creep threshold register 4.6.8 Fast effective54
value related setting register55
4.6.9 Overcurrent alarm and56
control 4.6.10 ADC enable control 4.6.11 Energy read clear setting register.....	.57



4.6.12 User Write Protection Setting Register.....	57
4.6.13 Soft Reset Register	57
4.6.14 Channel Gain Adjustment Register.....	57
4.6.15 Channel Offset Adjustment Register.....	58
4.6.16 Active Power Gain Adjustment Register	59
4.6.17 Active Power Offset Adjustment Register.....	59
4.6.18 Reactive/Apparent Power Gain Adjustment	60
Register 4.6.19 Reactive/Apparent Power Offset	60
Scaling Ratio Register 4.6.20.....	60
4.7 Detailed description of electrical parameter registers.....	61
4.7.1 Waveform register.....	61
4.7.2 Effective value	62
register 4.7.3 Fast effective value.....	62
register 4.7.4 Active power	63
register 4.7.5 Reactive power	63
register 4.7.6 Apparent power	64
register 4.7.7 Energy pulse count	64
register 4.7.8 Waveform angle.....	64
register 4.7.9 Fast effective value	65
holding register 4.7.10 Power	66
factor register 4.7.11 Line voltage frequency register.....	66
5. Communication interface.....	67
5.1 SPI	67
5.1.1 Overview	67
5.1.2 Working Mode	67
5.1.3 Frame Structure.....	67
5.1.4 Read Operation Timing	68
5.1.5 Write Operation Timing	69
Mechanism 5.1.6 SPI Interface Fault Tolerance.....	69
5.2 UART	70
5.2.1 Overview.....	70
5.2.2 Byte Format 5.2.3	70
Read Timing 5.2.4	70
Write Timing 5.2.5	71
UART Interface Protection Mechanism.....	71
6. Typical application diagram.....	72
7. Packaging Information.....	73
7.1 Order Information.....	73
7.2 Packaging.....	73
7.3 Package Appearance.....	73



1. Product Description

BL0910 is a multi-channel calibration-free energy metering chip with built-in clock, which can achieve up to 10-phase AC energy metering. It can be used in multi-channel electric bicycle charging piles, multi-channel smart sockets/strips, Dali2.0 smart lighting and other multi-channel single-phase electricity metering and fault detection fields, with high cost performance.

BL0910 integrates 11 high-precision Sigma-Delta ADCs and can measure 11 channels simultaneously. Signal (current or voltage).

You can choose the 1U10I mode, which is a 10-way energy metering mode. It shares 1 voltage channel and uses it with 10 current channels to generate 10 energy meters. You can also choose the 5U5I mode, which uses 5 voltage channels and 5 current channels to generate 5 energy meters. You can also choose the 3U6I mode.

Mode, this mode uses 3 voltages Ua/Ub/Uc, which are divided into Ia/Ib/Ic and Ia'/Ib'/Ic' and multiplied to generate 6-way energy measurement.

BL0910 can measure current, voltage RMS, active power, active electric energy and other parameters. It can output fast current effective value (for leakage monitoring, overcurrent protection and other fault detection), as well as temperature detection, waveform output and other functions. It can output data through UART or high-speed SPI interface, which can fully meet the needs of multi-channel charging piles and multi-channel power consumption data collection and monitoring of IoT devices. demand.

The BL0910 factory channel measurement gain deviation is calibrated to <1%. When the whole machine is not calibrated, if a high-precision sampling resistor is used externally, the whole machine measurement error is less than 2%. If you need to meet high-precision measurement requirements (whole machine error <0.3%), external calibration is required.



2. Basic characteristics

2.1 Main features

1U10I mode, this mode shares 1 voltage with 10 currents to generate 10 electric energies

Measurement

Configurable 5U5I mode, which uses 5 voltages and 5 currents to generate 5-way energy measurement

Configurable 3U6I mode, which uses 3 voltages and 6 currents (each 1 voltage with 2 currents) to generate 6-way energy measurement

Dynamic range of

active energy measurement (5000:1) Can detect the

effective value of voltage and current Batch

factory gain deviation is less than 1% Built

-in waveform register, which can be used for waveform

analysis Leakage monitoring function, can measure leakage above 1mA, with the fastest response time of 10mS, leakage monitoring

Threshold and response time can be set Each

overcurrent output indication, overcurrent threshold can be set, response time can be set Built - in temperature sensor,

measurement range -40 degrees ~ 85 degrees, measurement accuracy ± 2 degrees, to meet the product's own over-temperature monitoring, room temperature

measurement and other needs Built - in active power, energy,

current/voltage effective value and other registers UART / SPI output Anti - creep design to ensure that

noise signals are removed when there is

no current Power failure monitoring, when the working power is lower than 2.7V (typical value), the

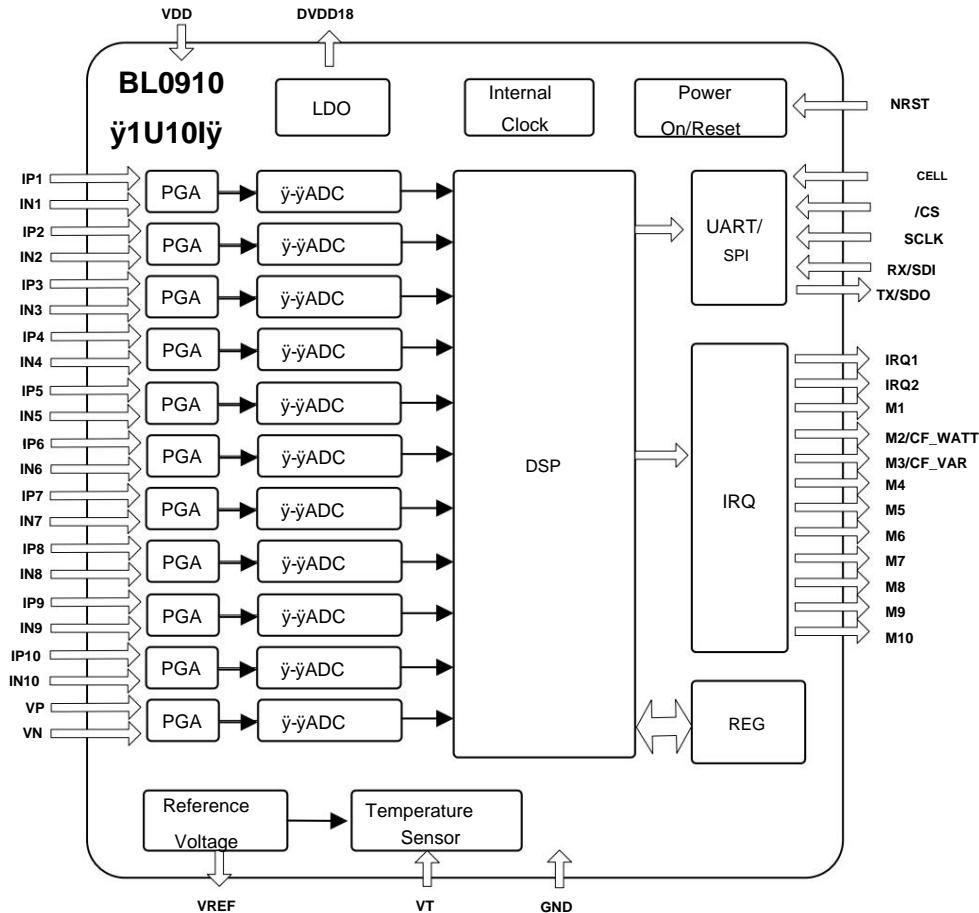
chip is reset Built - in 1.097V reference voltage source (typical value) Built - in oscillation circuit, clock about 8MHz Single working power

supply 3.3V, low power consumption 40mW (typical value) LQFP48 package



2.2 System Block Diagram

Working mode 1: 1U10I mode



BL0910 integrates 11 high-precision Sigma-Delta ADCs, which can measure 11 signals (current

or voltage). It has built-in crystal oscillator, reference voltage, temperature measurement and other analog parts, while the DSP part is based on different

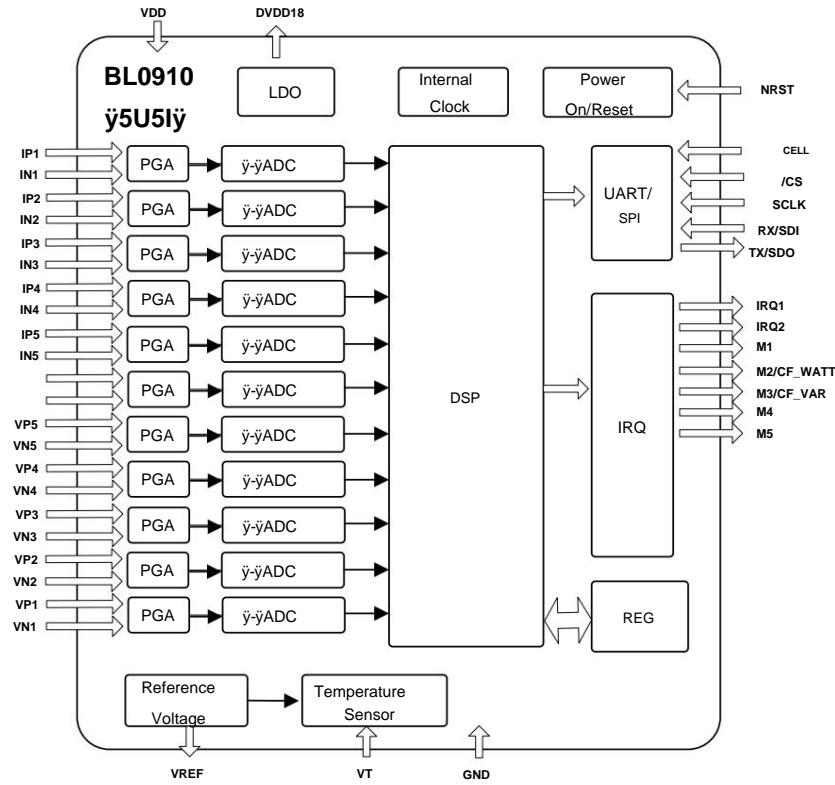
Mode configuration internal signal processing, storing power and energy in registers, the digital part also includes optional UART

Or SPI, interrupt and various indication outputs.

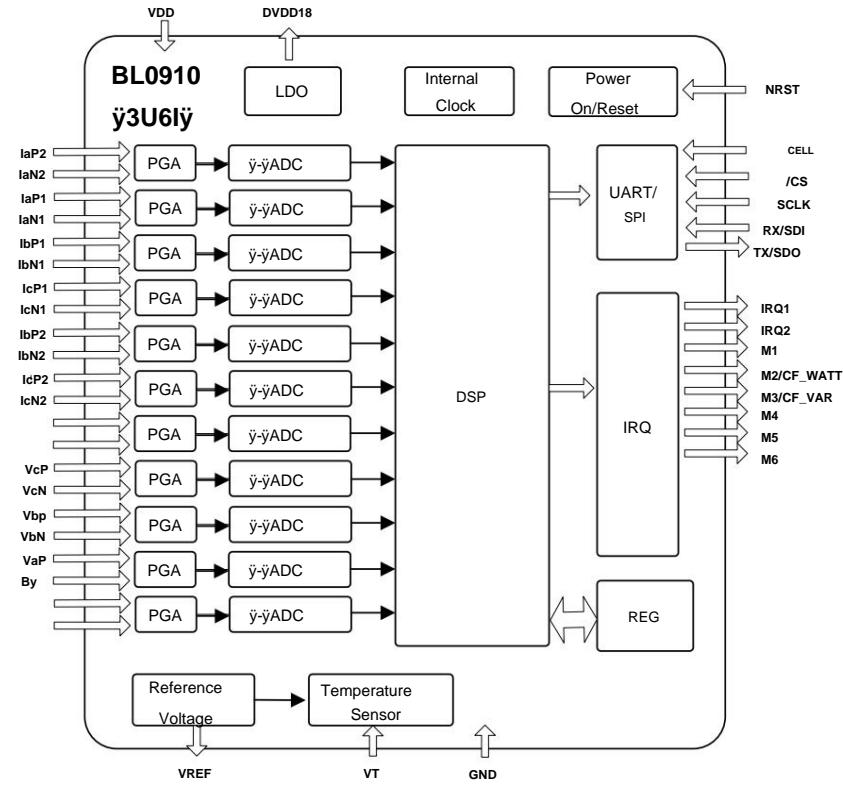


BL0910 ten-phase AC power metering chip

Working mode 2: 5U5I mode



Working mode 3: 3U6I mode





2.3 Pin Arrangement (LQFP48)

Pin Name	I/O	Pin Description
1	VT	I Temperature detection terminal.
2	VREF I/O	Reference voltage input and output terminal. External 0.1uF filter capacitor
3	IN6	I #6_Current channel negative input. Analog input, gain x1, x2, x4, x16 Adjustable. The maximum differential voltage per pin pair is ±700mV.
4	IP6	I #6_Current channel positive input. Same as Pin3.
5	IN7	I #7_Current channel negative input. Same as Pin3.
6	IP7	I #7_Current channel positive input. Same as Pin3.
7	IN8	I #8_Negative input of current channel. Same as Pin3.
8	IP8	I #8_Current channel positive input. Same as Pin3.
9	IN9	I #9_Negative input of current channel. Same as Pin3.
10	IP9	I #9_Current channel positive input. Same as Pin3.
11	IN10	I #10_Current channel negative input. Same as Pin3.
12	IP10	I #10_Current channel positive input. Same as Pin3.
13	VN	I #11_Voltage channel negative input, maximum differential voltage ±700mV.
14	VP	I #11_Positive input of voltage channel, maximum differential voltage ±700mV.
15	NRST	I Reset pin, low level is valid.
16	AGND	I Analog ground.
17	DGND	I Digital ground.
18	CS	I SPI chip select signal/Uart rate selection.
19 TX SDO	O SPI/UART	O communication, send.
20 RX SDI	I SPI UART	I communication, receiving.
21	SCLK	I SPI communication clock/Uart rate selection
22 _IRQ1		O Interrupt output 1, configurable output
23 _IRQ2		O Interrupt output 2, output voltage zero crossing signal
24	VPP	I Reserved, can be left floating.
25	M1	O Channel 1 overcurrent output.
26	M2	O Channel 2 overcurrent output.
27	M3	O Channel 3 overcurrent output.
28	M4	O Channel 4 overcurrent output.
29	M5	O Channel 5 overcurrent output.
30	M6	O Channel 6 overcurrent output.
31	M7	O Channel 7 overcurrent output.
32	M8	O Channel 8 overcurrent output.
33	M9	O Channel 9 overcurrent output.



BL0910 ten-phase AC power metering chip

34	M10	O Channel 10 overcurrent output.
35 DVDD18	O Digital 1.8V voltage, external 0.1uF filter capacitor.	
36 CELL	I Sel default internal pull-down, leave it unconnected to select UART, Sel=1 to select SPI	
37 DVDD	I Digital power input, 3.3V.	
38 AVDD	I Analog power input, 3.3V.	
39 IN1	I #1_Current channel negative input. Same as Pin3.	
40 IP1	I #1_Current channel positive input. Same as Pin3.	
41 IN2	I #2_Current channel negative input. Same as Pin3.	
42 IP2	I #2_Current channel positive input. Same as Pin3.	
43 IN3	I #3_Current channel negative input. Same as Pin3.	
44 IP3	I #3_Current channel positive input. Same as Pin3.	
45 IN4	I #4_Negative input of current channel. Same as Pin3.	
46 IP4	I #4_Current channel positive input. Same as Pin3.	
47 IN5	I #5_Negative input of current channel. Same as Pin3.	
48 IP5	I #5_Current channel positive input. Same as Pin3.	

2.4 Performance Indicators

2.4.1 Electrical parameter performance indicators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active power measurement error Difference	WATTERR	5000:1 input DR		0.1		%
Reactive power measurement error Difference	VARERR	5000:1 input DR		0.1		%
The phase angle between channels causes Measurement error (PF=0.8 capacitive) (PF=0.5 perceptual)	PF08CERR PF05LERR	Phase advance 37° Phase lag 60°		0.15		%
AC Power Rejection (Output frequency amplitude changes change) DC Power Supply Rejection (Output frequency amplitude changes change)	ACPSRR DCPSRR	10-channel current input pin IP\IN@100mV, voltage Channel input pin VP\VN=100mV		0.01		%
Voltage RMS measurement Accuracy, relative error	VRMSERR	2500:1 input DR		0.2		%
Current RMS measurement Accuracy, relative error	IRMSERR	2500:1 input DR		0.2		%
Analog Input Input level (peak) input resistance		Differential input		370	700 mV	kΩ



BL0910 ten-phase AC power metering chip

Bandwidth (-3dB)			14		kHz	
Gain Error		External 1.1 reference voltage	0.5		%	
Phase gain matching error Difference		External 1.1 reference voltage	3		%	
Internal voltage reference	Vref		1.097		IN	
Benchmark Deviation	VrefERR		5		mV	
Temperature Coefficient	TempCoef		20		ppm/°C	
Logic Input NRST/RESET/SDI SCLK/Clock Input high level Input low level		DVDD=3.3V±2.5%	2.6		IN IN	
Logic Output TX/SDO/M1-M10 /IRQ1/IRQ2 Output high level Output low level		DVDD=3.3V±2.5%	2.6	0.8	IN IN	
power supply AVDD/DVDD DVDD18 OAT DID	VAVDD VDVDD18 IAVDD IDVDD	DVDD18=1.8V AVDD=3.3 DVDD=3.3	3 1.6 5 6	3.3 1.8 8 10	3.6 2 8 10	IN mA mA

2.4.2 Limit range

T = 25 °C

project	symbol	extremum	unit
Power supply voltage	AVDD/DVDD	-0.3 ~ +4	IN
VDD Power supply voltage	DVDD18	-0.3 ~ +2.5	IN
DVDD18 Analog input voltage (relative to GND)	IN1-IN10/VN/IP1-IP10 VP/VT	-1 ~ +AVDD	IN
Analog output voltage (relative to GND)	VREF	-0.3 ~ +AVDD	IN
Digital input voltage (relative to GND)	SEL/NRST/RESET/SDI/SCLK /CS	-0.3 ~ DVDD+0.3	IN
Digital output voltage (relative to GND)	M1-M10/TX/SDO/IRQ1 /IRQ2	-0.3 ~ DVDD+0.3	IN
Working temperature	Topr	-40 ~ +85	°C
Storage temperature	Tstr	-55 ~ +150	°C
Power consumption (LQFP48)	P	200	mW



3. Working principle

3.0 Current and Voltage Mode Selection

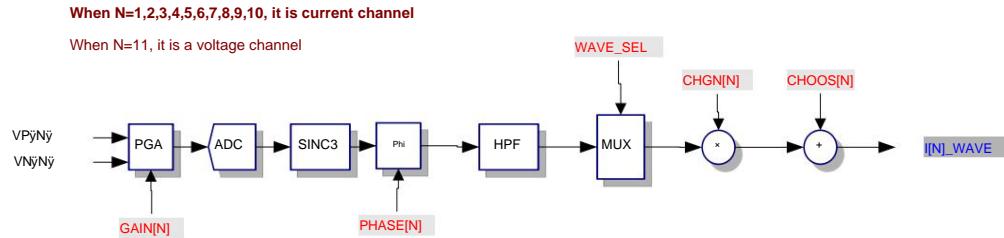
There are 11 high-precision ADCs with the same structure, using double-ended differential signal input. Depending on the mode,

Each channel can be used for current input or voltage input, see the table below for details.

Line Description.

1U10I mode 5U5I mode		3U6I Mode			Output			
Current	Voltage	Current	Voltage	RMS	Power	Indicator		
1	11	1	11			rms01	watt01	m1
2	11	2	10	2	10	rms02	watt02	m2
3	11	3	9	3	9	rms03	watt03	m3
4	11	4	8	4	8	rms04	watt04	m4
5	11	5	7			rms05	watt05	m5
6	11					rms06	watt06	m6
7	11			1	10	rms07	watt07	m7
8	11			5	9	rms08	watts08	m8
9	11			6	8	rms09	watt09	m9
10	11					rms10	watt10	m10

3.1 Principle of current and voltage waveform generation



11 waveform outputs, including 10 current and 1 voltage.

In the channel (same circuit structure for current and voltage), the input signal passes through the analog module amplifier

The 1-bit PDM code is transmitted to the digital module through the PGA and high-precision analog-to-digital conversion (ADC).



After phase calibration, downsampling filter (SINC3), high-pass filter (HPF), gain and offset correction, etc.

Module to obtain the required current waveform data and voltage waveform data (I[N]_WAVE, V_WAVE).

11 Channel PGA gain is adjustable. The data format of channel PGA gain adjustment registers GAIN1 and GAIN2 is

The formula is as follows: (every 4 bits control one channel, 0000=1; 0001=2; 0010=8; 0011=16).

Address	Name	Bit Width	Default Value	Description
60	GAIN1	24	0x000000	Channel PGA gain adjustment register [3:0]: Voltage channel [7:4]: Current 1 channel [11:8]: Current 2 channel [15:12]: Current 3 channel [19:16]: Current 4 channels [23:20]: Current 5 channel
61	GAIN2	20	0x000000	Channel PGA gain adjustment register [3:0]: Current 6 channels [7:4]: Current 7 channel [11:8]: Current 8 channels [15:12]: Current 9 channel [19:16]: Current 10 channel

3.1.1 Phase compensation

At the ADC output, a method is provided to digitally calibrate small phase errors.

The time delay or advance of the signal is introduced into the signal processing circuit to compensate for small phase errors.

The compensation must be timely, so this method is only applicable to small phase errors in the range of <0.6°.

Positive phase errors will introduce significant phase errors in higher harmonics.

11 Channel phase compensation is adjustable. For details of the phase calibration register, see the register description.

Address	Name	Bit width	Default value	Description
64	PHASE[1]/PHASE[2] 16		0x0000	[15:8]: 1 channel phase compensation [7:0]: 2-channel phase compensation
65	PHASE[3]/PHASE[4] 16		0x0000	[15:8]: 3-channel phase compensation [7:0]: 4-channel phase compensation
66	PHASE[5]/PHASE[6] 16		0x0000	[15:8]: 5-channel phase compensation [7:0]: 6-channel phase compensation



BL0910 ten-phase AC power metering chip

67	PHASE[7]/PHASE[8] 16		0x0000	[15:8]: 7-channel phase compensation [7:0]: 8-channel phase compensation
68	PHASE[9]/PHASE[10] 16		0x0000	[15:8]: 9-channel phase compensation [7:0]: 10-channel phase compensation
69	PHASE[11]	8	0x00	[7:0]: 11-channel phase compensation

3.1.2 Channel offset correction

Contains 11 16-bit channel offset calibration registers CHOS[N], with the default value being 0x0000.

These registers can be used for digital calibration or factory error pre-calibration.

They use 2's complement data to eliminate the analog-to-digital conversion of the current channel and the voltage channel.

Deviation. The deviation here may be caused by the offset generated by the input and the analog-to-digital conversion circuit itself. Deviation

The correction can make the waveform offset 0 under no-load condition.

See register detailed description.

Address Name		Bit width	default value	description
AB	FOOT[1]	16	0x0000	1 channel channel offset adjustment register, two's complement
AC	FOOT [2]	16	0x0000	2-channel channel offset adjustment register, two's complement
AD	FOOT[3]	16	0x0000	3-channel channel offset adjustment register, two's complement
BUT	FOOT[4]	16	0x0000	4-channel channel offset adjustment register, two's complement
OF	FOOT[5]	16	0x0000	5-channel channel offset adjustment register, two's complement
B0	FOOT[6]	16	0x0000	6-channel channel offset adjustment register, two's complement
B1	FOOT[7]	16	0x0000	7-channel channel offset adjustment register, two's complement
B2	FOOT[8]	16	0x0000	8-channel channel offset adjustment register, two's complement
B3	FOOT[9]	16	0x0000	9-channel channel offset adjustment register, two's complement
B4	FOOT[10]	16	0x0000	10-channel channel offset adjustment register, two's complement
B5	FOOT [11]	16	0x0000	11-channel channel offset adjustment register, two's complement

3.1.3 Channel gain calibration

Contains 11 16-bit channel gain calibration registers CHGN[N], with the default value being 0x0000.

These registers can be used for digital calibration or factory error pre-calibration.

They use 2's complement data to adjust the gain of the current channel and voltage channel analog-to-digital conversion.

Error. The error here may be caused by the input and the analog-to-digital conversion circuit itself. Gain correction can



Adjust within the range of plus or minus 50%. For the channel gain adjustment register correction formula, see the register detailed description.

Address Name		Bit width	Default value	Description
A0	CHGN[1]	16	0x0000	1-channel channel gain adjustment register, two's complement
A1	CHGN[2]	16	0x0000	2-channel channel gain adjustment register, two's complement
A2	CHGN[3]	16	0x0000	3-channel channel gain adjustment register, two's complement
A3	CHGN[4]	16	0x0000	4-channel channel gain adjustment register, two's complement
A4	CHGN[5]	16	0x0000	5-channel channel gain adjustment register, two's complement
A5	CHGN[6]	16	0x0000	6-channel channel gain adjustment register, two's complement
A6	CHGN[7]	16	0x0000	7-channel channel gain adjustment register, two's complement
A7	CHGN[8]	16	0x0000	8-channel channel gain adjustment register, two's complement
A8	CHGN[9]	16	0x0000	9-channel channel gain adjustment register, two's complement
A9	CHGN[10]	16	0x0000	10-channel channel gain adjustment register, two's complement
AA	CHGN[11]	16	0x0000	11-channel channel gain adjustment register, two's complement

3.1.4 Current and voltage waveform output

It can collect the current load current and voltage waveform data, sampling current and voltage at a speed of 15.625ksps.

The sampling rate is updated, and 312.5 points can be sampled per cycle. Each sampling data is a 24-bit signed number and is stored in

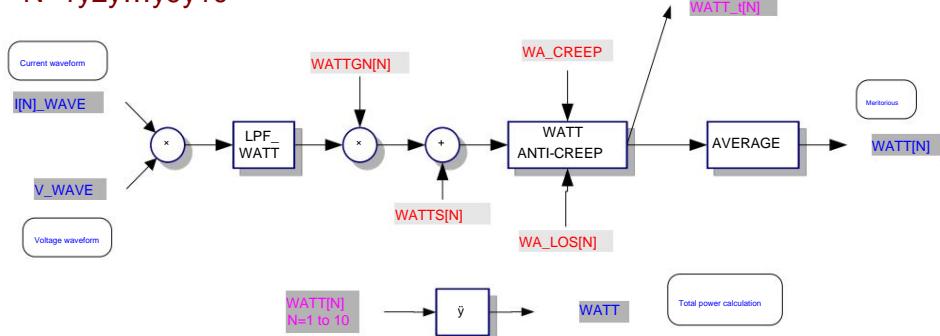
Waveform register (WAVE[N]). The SPI rate is less than 1.5Mbps, and the waveform values of multiple channels can be read continuously.

Address	Name	Bit Width	Default Value	Description
1	WAVE[1]	24	0x000000	1 Channel waveform register
2	WAVE[2]	24	0x000000	2 Channel Waveform Register
3	WAVE[3]	24	0x000000	3 Channel Waveform Register
4	WAVE[4]	24	0x000000	4-channel waveform register
5	WAVE[5]	24	0x000000	5 Channel Waveform Register
6	WAVE[6]	24	0x000000	6-channel waveform register
7	WAVE[7]	24	0x000000	7 Channel waveform register
8	WAVE[8]	24	0x000000	8-channel waveform register
9	WAVE[9]	24	0x000000	9-channel waveform register
A	WAVE[10]	24	0x000000	10 Channel waveform register
B	WAVE[11]	24	0x000000	11 Channel waveform register



3.2 Active power calculation principle

$N=1 \dots 9 \dots 10$



The current and voltage waveforms are digitally multiplied and then pass through a low-pass filter, gain, and offset correction in sequence.

The power signal can be obtained after accurate, anti-creep judgment and averaging processing.

3.2.1 Active power output

10 power signals WATT[N]. The active power register is a 24-bit signed number (complement code), Bit[23]

It is the sign bit, indicating positive work/negative work. For the active power calculation formula, please refer to the register detailed description.

Address	Name	Bit width	default value	description
22	WATT[1]	24	0x000000	Channel 1 active power register
23	WATT[2]	24	0x000000	Channel 2 active power register
24	WATT[3]	24	0x000000	Channel 3 active power register
25	WATT[4]	24	0x000000	Channel 4 active power register
26	WATT[5]	24	0x000000	Channel 5 active power register
27	WATT[6]	24	0x000000	Channel 6 Active Power Register
28	WATT[7]	24	0x000000	Channel 7 Active Power Register
29	WATT[8]	24	0x000000	Channel 8 Active Power Register
2A	WATT[9]	24	0x000000	Channel 9 Active Power Register
2B	WATT[10]	24	0x000000	Channel 10 Active Power Register
2C	WATT	24	0x000000	Total active power register

The add_sel register can be used to set the active power sum to be absolute value addition or algebraic sum addition.

0x98	MODE	Working Mode Register	
No.	name	default	description
[8]	add_sel	1'b0	Watt sum addition method: 0- absolute value addition; 1- algebraic sum addition.



BL0910 ten-phase AC power metering chip

3.2.2 Active power calibration

Contains 10 16-bit active power offset correction registers WATTOS[N] and 10 16-bit active power offset correction registers

Active power gain correction register WATTGN[N], the default value is 0x0000.

These registers can be used for digital calibration or factory error pre-calibration.

WATTOS is used to eliminate DC deviations in active power calculations, and WATTGN is used to eliminate DC deviations in active power calculations.

The gain deviation in the power calculation may be caused by the gain difference between the PCB board and the integrated circuit in the power calculation.

The crosstalk between the two channels generated by the circuit itself may also be the gain deviation of the ADC channel itself.

Deviation correction can make the value in the active power register close to 0 under no-load conditions.

For details on how to set the adjustment register, see the register detailed description.

Address	Name	Bit Width	Default Value	Description
B6	WATTGN[1]	16	0x0000	Channel 1 active power gain adjustment register, two's complement
B7	WATTGN[2]	16	0x0000	Channel 2 active power gain adjustment register, two's complement
B8	WATTGN[3]	16	0x0000	Channel 3 active power gain adjustment register, two's complement
B9	WATTGN[4]	16	0x0000	Channel 4 active power gain adjustment register, two's complement
NOT	WATTGN[5]	16	0x0000	Channel 5 active power gain adjustment register, two's complement
BB	WATTGN[6]	16	0x0000	Channel 6 active power gain adjustment register, two's complement
BC	WATTGN[7]	16	0x0000	Channel 7 active power gain adjustment register, two's complement
BD	WATTGN[8]	16	0x0000	Channel 8 active power gain adjustment register, two's complement
BE	WATTGN[9]	16	0x0000	Channel 9 active power gain adjustment register, two's complement
BF	WATTGN[10]	16	0x0000	Channel 10 active power gain adjustment register, two's complement
C0	WATTS[1]	16	0x0000	Channel 1 active power bias adjustment register, two's complement
C1	WATTS[2]	16	0x0000	Channel 2 active power bias adjustment register, two's complement
C2	WATTS[3]	16	0x0000	Channel 3 active power bias adjustment register, two's complement
C3	WATTS[4]	16	0x0000	Channel 4 active power bias adjustment register, two's complement
C4	WATTS[5]	16	0x0000	Channel 5 active power bias adjustment register, two's complement
C5	WATTS[6]	16	0x0000	Channel 6 active power bias adjustment register, two's complement
C6	WATTS[7]	16	0x0000	Channel 7 active power bias adjustment register, two's complement
C7	WATTS[8]	16	0x0000	Channel 8 active power bias adjustment register, two's complement
C8	WATTS[9]	16	0x0000	Channel 9 active power bias adjustment register, two's complement
C9	WATTS[10]	16	0x0000	Channel 10 active power bias adjustment register, two's complement



3.2.3 Active power anti-creep

Built-in patented power anti-submarine function module to ensure that the power output is 0 when there is no current input.

Active power anti-creep threshold register (WA_CREEP) is a 12-bit unsigned number, with a default value of 0x04C.

This value is compared with the absolute value of the instantaneous active power measured internally. When the absolute value of the instantaneous active power is less than this value,

When the output active power is set to zero, this allows the output to be

The value output to the active power register is 0.

Address	Name	Bit Width	Default Value	Description
88	VAR_CREEP/ WA_CREEP	24	0x04C04C	[11:0] is the active anti-creep power threshold register WA_CREEP; [23:12] is the reactive power protection threshold register VAR_CREEP
89	WA_CREEP2	12	0x000 [11:0]	Total active power anti-creep threshold register

WA_CREEP can be set according to the power register WATT value. The default anti-creep value is roughly the full power scale.

20 millionths.

When a channel is in the anti-submarine state, the instantaneous power of the channel below the threshold does not participate in the energy accumulation.

3.2.4 Active power small signal compensation

For active power calculation, in order to reduce the noise error in the small signal segment, the small signal compensation register can be used.

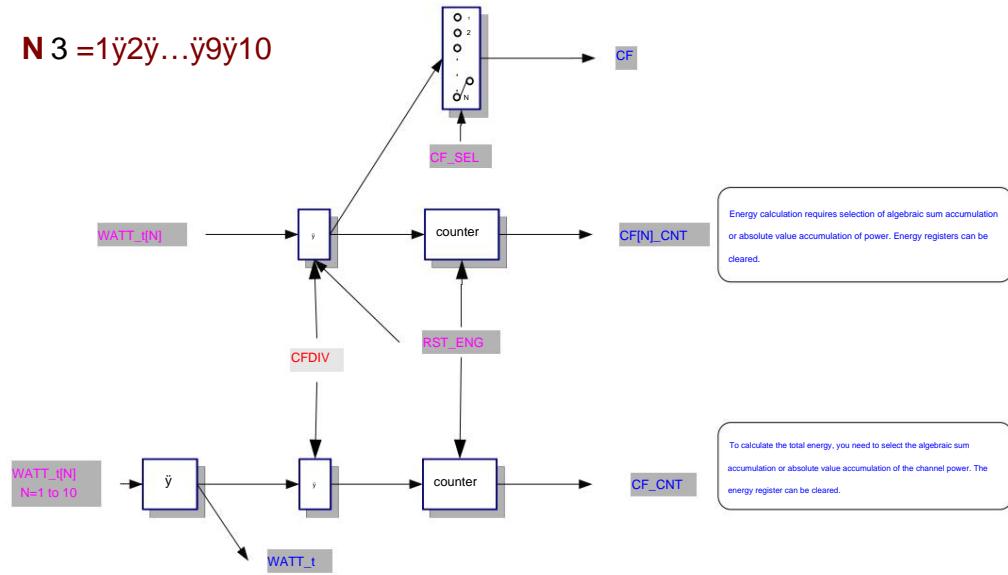
The active small signal compensation register (WA_LOS) is 12 bits.

Two's complement, the default value is 0x000.

Address	Name	Bit Width	Default Value	Description
82	WA_LOS[1]/ WA_LOS[2]	24	0x000000	[23:12]: Channel 1 active power small signal compensation register [11:0]: Channel 2 active power small signal compensation register
83	WA_LOS[3]/ WA_LOS[4]	24	0x000000	[23:12]: Channel 3 active power small signal compensation register [11:0]: Channel 4 active power small signal compensation register
84	WA_LOS[5]/ WA_LOS[6]	24	0x000000	[23:12]: Channel 5 active power small signal compensation register [11:0]: Channel 6 active power small signal compensation register
85	WA_LOS[7]/ WA_LOS[8]	24	0x000000	[23:12]: Channel 7 active power small signal compensation register [11:0]: Channel 8 active power small signal compensation register
86	WA_LOS[9]/ WA_LOS[10]	24	0x000000	[23:12]: Channel 9 active power small signal compensation register [11:0]: Channel 10 active power small signal compensation register



3.3 Principle of Active Energy Measurement



Provides 10 channels of energy pulse accumulation. The principle is that the active power of each channel is accumulated over a period of time.

By integrating, the active energy during this period can be obtained, and the energy can be further converted into the corresponding frequency calibration pulse CF.

The more electricity is used, the faster the CF frequency is; the less electricity is used, the slower the CF frequency is.

3.3.1 Active energy output

The energy (power consumption) can be obtained by counting the CF pulses and stored in the Nth phase energy accumulation register.

CF[N]_CNT. The total energy of the ten phases is stored in the total energy register CF_CNT, as shown in the figure below.

Address	Name	Bit width	default value	description
2F	CF[1]_CNT	24	0x000000	Channel 1 active pulse count, unsigned
30	CF[2]_CNT	24	0x000000	Channel 2 active pulse count, unsigned
31	CF[3]_CNT	24	0x000000	Channel 3 active pulse count, unsigned
32	CF[4]_CNT	24	0x000000	Channel 4 active pulse count, unsigned
33	CF[5]_CNT	24	0x000000	Channel 5 active pulse count, unsigned
34	CF[6]_CNT	24	0x000000	Channel 6 Active pulse count, unsigned
35	CF[7]_CNT	24	0x000000	Channel 7 active pulse count, unsigned
36	CF[8]_CNT	24	0x000000	Channel 8 active pulse count, unsigned
37	CF[9]_CNT	24	0x000000	Channel 9 active pulse count, unsigned
38	CF[10]_CNT	24	0x000000	Channel 10 active pulse count, unsigned
39	CF_CNT	24	0x000000	Total active pulse count, unsigned



3.3.2 Active energy output selection

0x98		MODE	Working Mode Register	
No.	name	default	description	
[9]	cf_enable	1'b0	0-cf disable, default; 1-cf enable	
[13:10]	CF_SEL	4'b0000	Channel CF_WATT output selection: 0000, CF is turned off by default; 0001, power CF of channel 1; 0010, power CF of channel 2; 0011, power CF of channel 3; 0100, power CF of channel 4; 0101, power CF of channel 5; 0110, power CF of channel 6; 0111, power CF of channel 7; 1000, power CF of channel 8; 1001, power CF of channel 9; 1010, power CF of channel 10; 1011, total active power CF; 1100, reactive power CF (channel can be optional); 1101, apparent power CF (channel optional); 1110, 1111, turn off CF; In addition, CF_VAR is always the reactive power CF (channel optional) and remains unchanged.	
[15]	cf_add_sel	1'b0	Watt and var energy addition method: 0-absolute value addition; 1-algebraic sum addition (separate and combined)	

First, set MODE[9]=1 to configure M2 and M3 to output CF_WATT pulse and CF_VAR pulse respectively.

Then set CF_SEL to select the calibration pulse output of any channel for calibration. The period of CF is less than 180ms

When it is 50% duty cycle pulse, when it is greater than or equal to 180ms, the high level pulse width is fixed at 90ms.

CF_add_sel can be used to set how the total energy is added, the algebraic sum of each phase or the absolute value addition.

The counting results of CF pulses are stored in the CF[N]_CNT register. The power conversion corresponding to 1 CF

For the formula, see the register detailed description.

3.3.3 Active energy output ratio

During energy accumulation, the speed of energy accumulation can be set through the CF_DIV register, with a 2-fold relationship for each level.

There are 12 levels in total. Used for coarse adjustment.

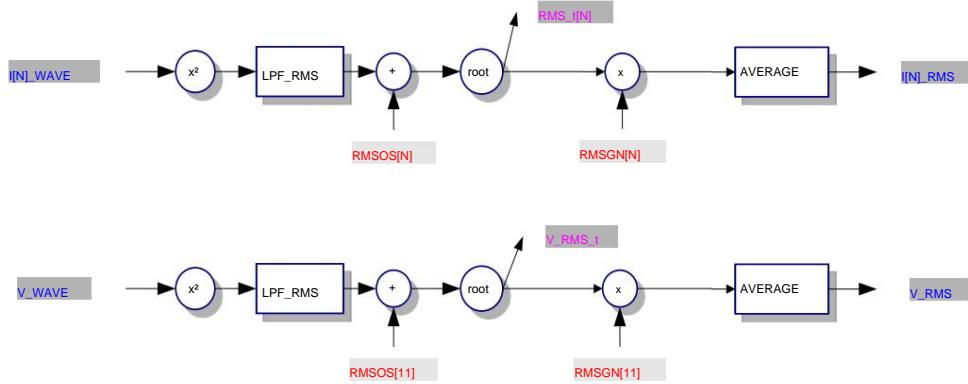
These registers can be used for digital calibration or factory error pre-calibration.

Address	Name	Bit width	default value	description
THIS	CFDIV	12	0x010	CF Scaling ratio register



3.4 Principle of current and voltage effective value calculation

$$N=1 \dots 9 \dots 10$$



The principle of effective value of each channel is shown in the figure. The original waveform of each channel is squared (X^2) and effective

The value is low-pass filter (LPF_RMS), root opening circuit (ROOT), and the instantaneous value of the effective value RMS_t is obtained.

The average value RMS[N] of each channel is obtained by averaging.

3.4.1 Effective value output

The effective value calculation result is output to 11 registers, which are 24-bit unsigned numbers.

In the anti-submarine state, the effective value of the channel is not measured. For the effective value conversion formula, please refer to the register detailed description.

Address	Name	Bit width	default value	description
c	RMS[1]	24	0x000000	1 channel effective value register, unsigned
D	RMS[2]	24	0x000000	2-channel effective value register, unsigned
AND	RMS[3]	24	0x000000	3-channel effective value register, unsigned
F	RMS[4]	24	0x000000	4-channel effective value register, unsigned
10	RMS[5]	24	0x000000	5-channel effective value register, unsigned
11	RMS[6]	24	0x000000	6-channel effective value register, unsigned
12	RMS[7]	24	0x000000	7 Channel effective value register, unsigned
13	RMS[8]	24	0x000000	8-channel effective value register, unsigned
14	RMS[9]	24	0x000000	9-channel effective value register, unsigned
15	RMS[10]	24	0x000000	10-channel effective value register, unsigned
16	RMS[11]	24	0x000000	11 Channel effective value register, unsigned



3.4.2 Current and voltage RMS calibration

Contains 11 24-bit RMS offset correction registers RMSOS[N] and 11 16-bit RMS

Gain correction register RMSGN[N], the default value is 0x0000.

They use data in 2's complement format to correct for errors in effective value calculations. This error may

It comes from input noise. Because there is a square operation in the calculation of the effective value, this may introduce noise.

Gain and offset correction can make the value in the rms register close to

0. For details about the channel effective value gain adjustment register, see the register detailed description.

Address Name		Bit width	default value	description
6C	RMSGN[1]	16	0x0000	1 Channel RMS gain adjustment register
6D	RMSGN[2]	16	0x0000	2-channel effective value gain adjustment register
6E	RMSGN[3]	16	0x0000	3-channel effective value gain adjustment register
6F	RMSGN[4]	16	0x0000	4-channel RMS gain adjustment register
70	RMSGN[5]	16	0x0000	5-channel effective value gain adjustment register
71	RMSGN[6]	16	0x0000	6-channel RMS gain adjustment register
72	RMSGN[7]	16	0x0000	7-channel effective value gain adjustment register
73	RMSGN[8]	16	0x0000	8-channel RMS gain adjustment register
74	RMSGN[9]	16	0x0000	9-channel effective value gain adjustment register
75	RMSGN[10]	16	0x0000	10-channel RMS gain adjustment register
76	RMSGN[11]	16	0x0000	11 Channel RMS gain adjustment register
77	RMSOS[1]	24	0x000000	1 Channel RMS offset correction register
78	RMSOS[2]	24	0x000000	2-channel RMS offset correction register
79	RMSOS[3]	24	0x000000	3-channel RMS offset correction register
7A	RMSOS[4]	24	0x000000	4-channel RMS offset correction register
7B	RMSOS[5]	24	0x000000	5-channel RMS offset correction register
7C	RMSOS[6]	24	0x000000	6-channel RMS offset correction register
7D	RMSOS[7]	24	0x000000	7-channel RMS offset correction register
7E	RMSOS[8]	24	0x000000	8-channel RMS offset correction register
7F	RMSOS[9]	24	0x000000	9-channel RMS offset correction register
80	RMSOS[10]	24	0x000000	10 Channel RMS offset correction register
81	RMSOS[11]	24	0x000000	10 Channel RMS offset correction register



3.4.3 Effective value anti-creep

It has a patented RMS anti-submarine function to ensure that the RMS output is 0 when there is no current input.

The effective value anti-creep threshold register (RMS_CREEP) is a 12-bit unsigned number, and the default value is 0x200.

This value is internally expanded by 2 times and compared with the absolute value of the input effective value signal.

When the value is set, the output effective value is set to zero. This allows the output to be

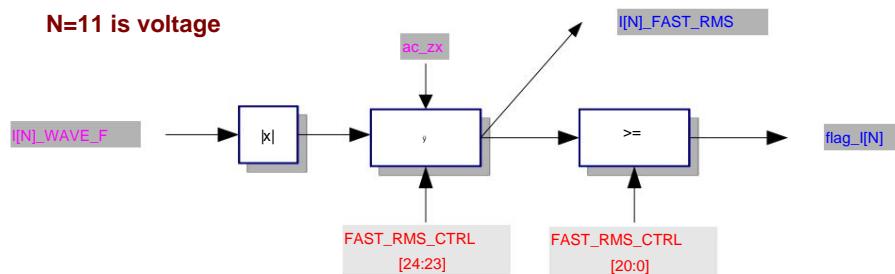
The value output to the valid value register is 0.

Address	Name	Bit width	default value	description
8A	RMS_CREEP	12	0x200	Effective value small signal threshold register

3.5 Fast leakage/overcurrent detection principle

N=1, 2, ..., 9, 10 is the current

N=11 is voltage



The fast effective value calculation principle is shown in the figure. All 11 channels have fast effective value registers, which can detect half-cycle

Or cycle effective value. This function can be used for leakage or overcurrent detection.

The input waveform is taken by taking the absolute value and then integrating it within a specified time to obtain a fast effective value.

I[N]_FAST_RMS[23:3] is compared with the preset threshold FAST_RMS_CTRL[20:0]. If it exceeds

A flag may be given.

Note: When measuring AC signals, you need to set Bit [22] of register 0x96 (MODE1) = 1.

Through high pass, filter out DC bias.

3.5.1 Fast RMS output

The fast effective value output register of 11 channels is shown in the figure below. This register is a 24-bit unsigned number.

Address	Name	Bit width	default value	description
17	FAST_RMS[1]	24	0x00000001	Channel fast (leakage current) effective value register, unsigned
18	FAST_RMS[2]	24	0x00000002	channel fast (leakage current) effective value register, unsigned
19	FAST_RMS[3]	24	0x00000003	3-channel fast (leakage current) RMS register, unsigned
1A	FAST_RMS[4]	24	0x00000004	4-channel fast (leakage current) RMS register, unsigned



1B	FAST_RMS[5] 24 0x000000 5-channel fast (leakage current) RMS register, unsigned			
1C	FAST_RMS[6] 24 0x000000 6-channel fast (leakage current) RMS register, unsigned			
1D	FAST_RMS[7] 24 0x000000 7-channel fast (leakage current) RMS register, unsigned			
1E	FAST_RMS[8] 24 0x000000 8-channel fast (leakage current) RMS register, unsigned			
1F	FAST_RMS[9] 24 0x000000 9-channel fast (leakage current) RMS register, unsigned			
20	FAST_RMS[10] 24 0x000000 10 Channel fast (leakage current) RMS register, unsigned			
21	FAST_RMS[11] 24 0x000000 11 Channel fast (leakage current) RMS register, unsigned			

3.5.2 Fast RMS Accumulation Time and Threshold

To calculate the fast effective value, first take the absolute value, and then integrate it according to the set cumulative time.

Frequency, integer multiple of frequency time.

Address	Name	Bit width	default value	description
8B	FAST_RMS_CTRL 24		0x20FFFF	[23:21] Channel fast effective value register refresh time, can be selected half cycle and N cycle, the default is cycle; [20:0] Channel fast effective value threshold register

The accumulation time is selected by FAST_RMS_CTRL[23:21], 000-10ms, 001-20ms, 010-40ms,

There are six types: 011-80ms, 100-160ms, 101-320ms. The default selection is half-cycle cumulative response time 20ms.

The longer the accumulated time, the smaller the jump.

FAST_RMS_CTRL[20:0] is used to set the fast RMS value exceeding the limit threshold.

When the effective value exceeds the threshold, the output flag flag[N] is 1. The flag bit connection output (M1~M10) can be directly

Pull the leakage/overcurrent output indication pin high. Can be used in conjunction with the overcurrent indication control register.

3.5.3 Fast effective value save before reading

In order to record the fast overload signal, the fast effective value exceeding the threshold has a saving function and will not be read before reading.

The specific registers are shown in the table below:

Address	Name	Bit width	default value	description
46	FAST_RMS_H [1] 24 0x000000 1 Channel fast (leakage current) effective value storage register			
47	FAST_RMS_H [2] 24 0x000000 2 Channel fast (leakage current) effective value storage register			
48	FAST_RMS_H [3] 24 0x000000 3 Channel fast (leakage current) effective value storage register			
49	FAST_RMS_H [4] 24 0x000000 4-channel fast (leakage current) effective value storage register			
57	FAST_RMS_H [5] 24 0x000000 5 Channel fast (leakage current) effective value storage register			



BL0910 ten-phase AC power metering chip

58	FAST_RMS_H [6] 24 0x000000	6 Channel fast (leakage current) effective value storage register
59	FAST_RMS_H [7] 24 0x000000	7 Channel fast (leakage current) effective value storage register
5A	FAST_RMS_H [8] 24 0x000000	8-channel fast (leakage current) effective value storage register
5B	FAST_RMS_H [9] 24 0x000000	9-channel fast (leakage current) effective value storage register
5C	FAST_RMS_H [10] 24 0x000000	10 Channel fast (leakage current) effective value storage register

3.5.4 Overcurrent indication

Overcurrent indication (M1~M10) can be controlled by the following registers:

Address	Name	Bit Width	Default Value	Description
91	flag_ctrl1	24	0x000000	<p>Overcurrent indication control register 1.</p> <p>[23:10] Disconnection delay timing, 0.1ms/lsb;</p> <p>[9:0] Indication control, M1-M6: 0-output real-time interrupt; 1-input</p> <p>Output delay control</p> <p>[0]: 1 channel;</p> <p>[1]: 2 channels;</p> <p>[2]: 3 channels;</p> <p>[3]: 4 channels;</p> <p>[4]: 5 channels;</p> <p>[5]: 6 channels;</p> <p>[6]: 7 channels;</p> <p>[7]: 8 channels;</p> <p>[8]: 9 channels;</p> <p>[9]: 10 channels</p>
92	flag_ctrl2	24	0x000000	<p>Overcurrent indication control register 2.</p> <p>[23:10] Close delay timing, 0.1ms/lsb;</p> <p>[9:0] Close control, M1-M6: 0-close, 1-open</p> <p>Output delay control</p> <p>[0]: 1 channel;</p> <p>[1]: 2 channels;</p> <p>[2]: 3 channels;</p> <p>[3]: 4 channels;</p> <p>[4]: 5 channels;</p> <p>[5]: 6 channels;</p> <p>[6]: 7 channels;</p>



BL0910 ten-phase AC power metering chip

				[7]~8 channels; [8]~9 channels; [9]~10 channels
--	--	--	--	---

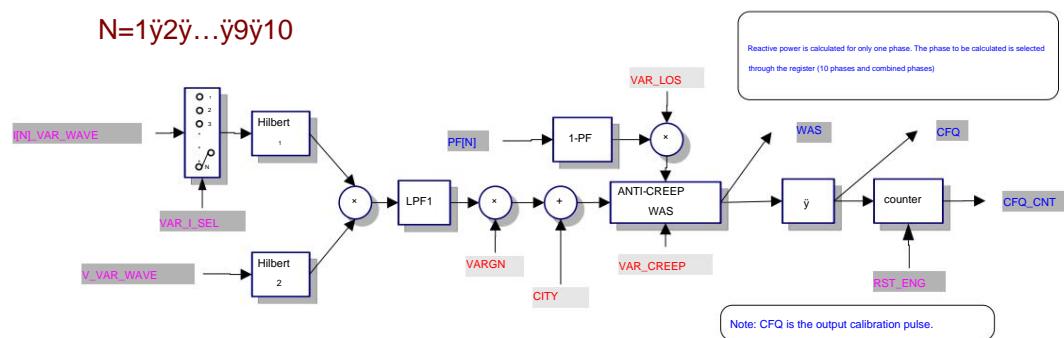
3.5.5 Relay control

You can also directly control the output level of M1~M10 pins by writing register flag_ctrl directly.

For relay control:

Address	Name	Bit Width	Default Value	Description
90	flag_ctrl	24	0x000000	The master controller directly controls the output level of M10~M1 [21:12] is the priority of M10~M1 output [0]: 1 channel; [1]~2 channels; [2]~3 channels; [3]~4 channels; [4]~5 channels; [5]~6 channels; [6]~7 channels; [7]~8 channels; [8]~9 channels; [9]~10 channels

3.6 Reactive Power Calculation



The reactive power calculation principle is shown in the figure. The current and voltage waveforms pass through the Hilbert filter and then are digitally

Multiplication, and then in sequence through low-pass filter, gain and offset calibration, anti-creep judgment and averaging processing



Reactive power signal can be obtained. After integration, reactive energy pulse accumulation can be obtained.

3.6.1 Reactive power calculation input selection

The input can select one of 10 currents to be multiplied by voltage through the VAR_I_SEL register

0x98		MODE		Working Mode Register			
No.	name	default	description				
[3:0] VAR_I_SEL		4'b000	Select reactive current measurement channel, select 1 from 10, default is 0000 0000ÿchannel 1 0001ÿchannel 2 0010ÿchannel 3 0011ÿchannel 4 0100ÿchannel 5 0101ÿchannel 6 0110ÿchannel 7 0111ÿchannel 8 1000ÿchannel 9 1001ÿchannel 10				

3.6.2 Phase Compensation

The phase compensation of the current and voltage channels for calculating reactive power is adjustable, the phase calibration register VAR_PHCAL_I

The data format of VAR_PHCAL_V is as follows (reactive phase correction (fine-tuning): [3:0] is fine-tuning, [3] is

Enable bit, the minimum adjustable delay time is 500ns, corresponding to 0.009 degrees/1LSB, and the maximum adjustable delay time is ±0.072 degrees.

Reactive phase correction (coarse adjustment): [12] is coarse adjustment, when it is 1, the reactive delay of this channel is 64us):

Address	Name	Bit width	Default value	Description
6A	VAR_PHCAL_I	5	0000H	Current channel reactive phase correction
6B	VAR_PHCAL_V	5	0000H	Voltage channel reactive phase correction

3.6.3 Reactive power output

Output only 1 phase reactive power, fundamental reactive power

Address	Name	Bit Width	Default Value	Description
2D	FVAR	24	0x000000	Optional channel reactive power register (fundamental wave)



3.6.4 Reactive power calibration

Contains a 16-bit reactive bias correction register VAROS and a 16-bit reactive gain correction register

Register VARGN, the default value is 0x0000.

These registers can be used for digital calibration or factory error pre-calibration.

They use data in 2's complement format to correct for errors in reactive power calculation. This error may come from

Originated from input noise or phase difference, this may introduce DC offset and gain errors caused by noise.

The reactive power measurement curve can be corrected by the deviation correction. For the correction of reactive power, please refer to the register detailed description.

Address Name	Bit Width	Default Value	Description	
THAT	VARGN	16	0x0000 Corresponding channel reactive power gain adjustment register, complement code	
CB	CITY	16	0x0000 Corresponding channel reactive power bias adjustment register, complement code	

3.6.5 Anti-creeping of reactive power

It has a patented power anti-submarine function to ensure that the power output is 0 when there is no current input.

The reactive power anti-creep threshold register (VAR_CREEP) is a 12-bit unsigned number, and the default value is 0x04C.

This value is internally expanded by 1 times and compared with the absolute value of the input reactive power signal.

When the value is less than this value, the output reactive power is set to zero. This can make it possible to measure reactive power even if there is a small

The noise signal is output to the reactive power register and the value is 0.

Address	Name	Bit width	Default value	Description
88	VAR_CREEP/ WA_CREEP	24	0x04C04C	[11:0] is the active anti-creep power threshold register Register WA_CREEP; [23:12] is the reactive power protection threshold register VAR_CREEP;

VAR_CREEP can be set according to the power register VAR value. Their corresponding relationship is generally

Take the reactive power range from 20 to 200 millionths of the full scale.

When a channel is in the anti-submarine state, the power of the channel below the threshold does not participate in energy accumulation.

3.6.6 Reactive power small signal compensation

For reactive power calculation, in order to reduce the noise error in the small signal segment, the small signal compensation parasitic



Address	Name	Bit width	default value	description
87	FVAR_LOS	24	0x000000	[11:0] Reserved [23:12] Corresponding reactive (fundamental wave) small signal compensation Register, two's complement.

3.6.7 Reactive energy output

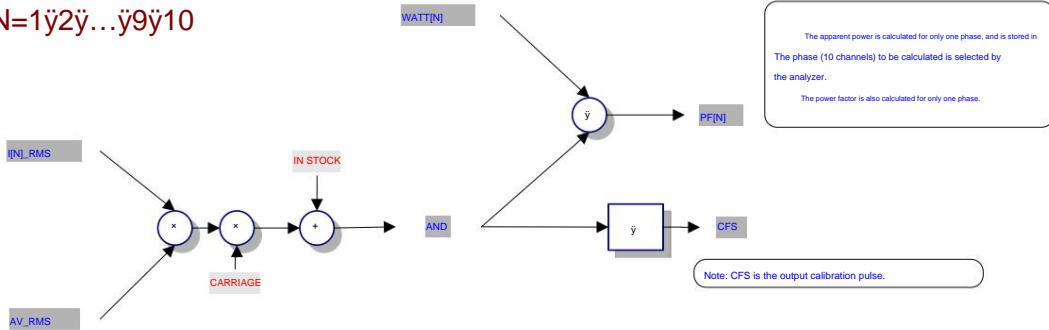
The reactive energy can be obtained by counting the reactive CF pulses and stored in the reactive energy accumulation register.

CFQ_CNT_y

Address	Name	Bit width	default value	description
3A	CFQ_CNT	24	0x000000	Optional channel reactive pulse count, unsigned

3.7 Apparent and Power Factor Calculation

$$N=1\ddot{\circ}2\ddot{\circ}\dots\ddot{\circ}9\ddot{\circ}10$$



The apparent calculation principle is shown in the figure. The current and voltage effective values are digitally multiplied and then pass through the gain in sequence.

The apparent power signal can be obtained by calibrating the deviation. After integration, the apparent energy pulse accumulation can be obtained.

The power factor is obtained by dividing the power by the apparent power.

3.7.1 Apparent power and energy output

The output is only 1 phase apparent power and energy, which is selected by the VAR_I_SEL register, that is, which phase is reactive.

channels, and it depends on which channel is selected.

Address	Name	Default value	of bit width	describe
2E	AND	24	0x000000	Optional channel apparent power register
3B	CFS_CNT	24	0x000000	Optional channel apparent pulse count, unsigned



3.7.2 Apparent Power Calibration

Contains a 16-bit apparent offset correction register VAOS and a 16-bit apparent gain correction register

Register VAGN, the default value is 0x0000.

These registers can be used for digital calibration or factory error pre-calibration.

They use data in 2's complement format to correct for errors in apparent calculations. This error may come from

This may introduce offset and gain errors. Gain and offset correction can correct the apparent measurement curve.

For the calibration of apparent power, please refer to the register detailed description.

Address	Name	Bit Width	Default Value	Description
CC	CARRIAGE	16	0x0000	corresponds to the channel apparent power gain adjustment register, complement code
CD	IN STOCK	16	0x0000	corresponds to the channel apparent power offset adjustment register, complement code

3.7.3 Power Factor

The output has only 1 phase power factor, which needs to be selected by the VAR_I_SEL register, that is, reactive power selection

Which channel, the power factor also chooses which channel.

Address	Name	bit width	default value	describe
4A	PF	24	0x000000	Optional channel power factor register

3.8 Temperature measurement

Provides internal temperature measurement and external temperature measurement.

The external and internal temperature readings are stored in the TPS1 and TPS2 registers respectively.

Address	Name	Bit width	default value	description
5E	TPS1	10	0x000000	Internal temperature value register
5F	TPS2	10	0x000000	AD measurement value of external temperature

Internal temperature measurement formula: internal temperature = $(TPS1-64) * 12.5/59-40 (\circ\text{C})$

External temperature measurement VT pin, detects the voltage of VT pin, TPS2 is the corresponding AD measurement value, full

The sampling voltage corresponding to 0x3FF is 0.55*VDD.

Address	Name	Bit width	default value	description



BL0910 ten-phase AC power metering chip

94	TPS_CTRL	16	0x07FF	<p>[15] Switch: 1-off, 0-on, default;</p> <p>[14] External temperature alarm release switch: 1-alarm off, 0-alarm on, default;</p> <p>[13:12] Temperature measurement selection: 00, 01 - Automatic temperature measurement, default 10- Select internal temperature measurement, 11-Select external temperature measurement;</p> <p>[11:10] Temperature measurement start time interval selection: 00-50ms 01-100ms, default 10-200ms 11-400ms</p> <p>[9:0] External temperature alarm threshold setting, default 0x3ff</p>
95	TPS2_A/ TPS2_B	24	0x0000	External temperature sensor coefficient A correction register/ External temperature sensor coefficient B correction register

3.9 Electrical parameter measurement

3.9.1 Line cycle measurement

It has a line cycle energy accumulation calculator, including active and reactive power.

Address Name		Bit width	default value	description
4B	LINE_WATTHR	24	0	Line cycle accumulated active energy register
4C	LINE_VARHR	24	0	Line cycle accumulated reactive energy register

The number of line cycles can be selected via the LINECYC register:

Address Name		Bit width	default value	description
8F	SAGLVL/ LINECYC	24	0x100009	[11:0] Line energy accumulation cycle number register LINECYC, default value is 009H, representing 10 cycles.

3.9.2 Line frequency measurement

For grid frequency testing, measure on the voltage input channel.



The PERIOD register contains the count of line cycles. If the input signal deviates from 50Hz/60Hz, the corresponding count

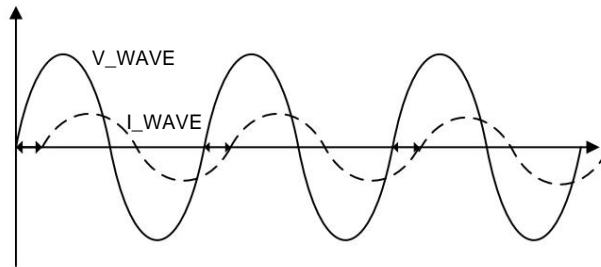
The value will change.

Address	Name	Bit Width	Default Value	Description
4E	PERIOD	20	0x000000	Line voltage frequency period register

Note: Frequency detection is related to ZX and nSAG signals.

It is valid only when the instantaneous effective value of voltage [23:12]>SAGLVL.

3.9.3 Phase angle calculation



The principle of phase angle measurement is shown in the figure. The phase is obtained by calculating the time difference between the positive zero crossing of current and voltage.

The corresponding time value is updated to the register ANGLE[N], each register is a 16-bit unsigned number.

For the calculation formula, please refer to the detailed description of registers.

Address	Name	Bit width	default value	Description
3C	ANGLE[1]	16	0x0000	Channel 1 current and voltage waveform angle register
3D	ANGLE[2]	16	0x0000	Channel 2 current and voltage waveform angle register
3E	ANGLE[3]	16	0x0000	Channel 3 current and voltage waveform angle register
3F	ANGLE[4]	16	0x0000	Channel 4 current and voltage waveform angle register
40	ANGLE[5]	16	0x0000	Channel 5 current and voltage waveform angle register
41	ANGLE[6]	16	0x0000	Channel 6 current and voltage waveform angle register
42	ANGLE[7]	16	0x0000	Channel 7 current and voltage waveform angle register
43	ANGLE[8]	16	0x0000	Channel 8 current and voltage waveform angle register
44	ANGLE[9]	16	0x0000	Channel 9 current and voltage waveform angle register
45	ANGLE[10]	16	0x0000	Channel 10 current and voltage waveform angle register

3.9.4 Power Sign Bit

For each channel power pulse CF output, there is a sign bit register to indicate the direction of each CF.

Direction indicates the direction of the corresponding accumulated energy (power consumption or power supply) from the previous CF to the current CF pulse.



BL0910 ten-phase AC power metering chip

Address	Name	Bit width	default value	description
4D	SIGN	24	0x000000	<p>Power sign bit. Corresponds to the sign of the current energy pulse count.</p> <p>The signal bit is refreshed when the CF pulse is output.</p> <p>[0]: 1 channel is active; [1]: 2 channels are active;</p> <p>[2]: 3 channels are active; [3]: 4 channels are active;</p> <p>[4]: 5 channels are active; [5]: 6 channels are active;</p> <p>[6]: 7 channels active; [7]: 8 channels active;</p> <p>[8]: 9 channels are active; [9]: 10 channels are active;</p> <p>[10]: combined active power; [11]: optional reactive power;</p>

3.10 Fault Detection

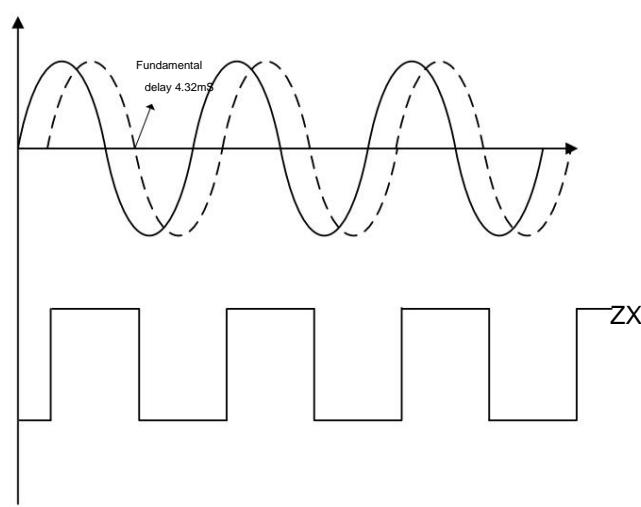
3.10.1 Zero Crossing Detection

Provides voltage and current zero-crossing detection, and can be configured to output zero-crossing signals through pin IRQ1.

The fundamental wave zero crossing is measured, which needs to pass through the fundamental wave filter internally, and the time delay with the actual input signal is 4.32ms.

right

The output zero-crossing signal mainly assists in shutting off the relay at the zero-crossing point to reduce the relay sticking phenomenon.



Note: To prevent the uncertainty caused by stray signals in the background noise or small signals, the current zero

The threshold is 70000, and the voltage zero-crossing threshold is 200000. If the instantaneous effective value is smaller than the threshold, there is no ZX signal.

The IRQ2 pin does not need to be configured and outputs the zero-crossing signal of the voltage channel.

3.10.2 Peak value exceeded

The current and voltage peak thresholds can be set programmatically by using the peak threshold registers



(I_PKLVL, V_PKLVL) settings.

Address	Name	Bit Width	Default Value	Description
8C	I_PKLVL/ V_PKLVL	24	0xFFFFFFF	[23:12] Current peak threshold register I_PKLVL; [11:0] Voltage peak threshold register V_PKLVL

For example, when the peak current of channel 1 is greater than the threshold set by the current peak threshold register (I_PKLVL),

The current overload indication PK01 is given if the corresponding PK01 enable bit in the interrupt mask register (MASK1) is

When set to logic 0, the /IRQ logic output becomes active low.

Similarly, when the current peak of channels 2 to 10 is greater than the threshold set by the current peak threshold register (I_PKLVL),

When the value is set, the current overload indication PK02~PK10 is given. If the corresponding

When any enable bit of PK02~PK10 is set to logic 0, the /IRQ logic output becomes active low.

Similarly, when the voltage peak is greater than the threshold set by the voltage peak threshold register (V_PKLVL),

Output voltage overload indication, if the corresponding PKV enable bit in the interrupt mask register (MASK1) is logic

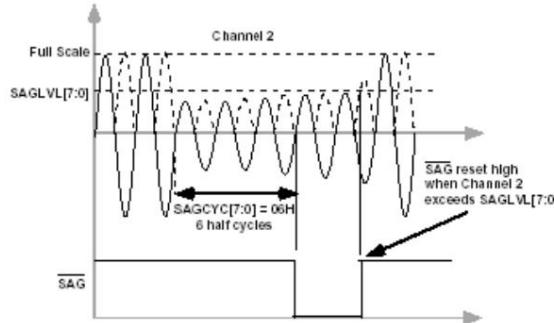
0, the /IRQ logic output becomes active low.

0x54	STATUS1		
Position interrupt flag		default value	describe
13	pk01	0	1 channel peak value exceeding limit signal
14	pk02	0	2 channels of peak over-limit signal
15	pk03	0	3-channel peak over-limit signal
16	pk04	0	4-channel peak over-limit signal
17	pk05	0	5-channel peak over-limit signal
18	pk06	0	6-channel peak over-limit signal
19	pk07	0	7-channel peak over-limit signal
20	pk08	0	8-channel peak over-limit signal
21	pk09	0	9-channel peak over-limit signal
22	pk10	0	10-channel peak over-limit signal
23	pkv		11 channels peak value exceeding limit signal

3.10.3 Line voltage drop

It can be programmed to indicate when the line voltage RMS value is lower than a certain peak value for more than a certain period of time.

When the number of half cycles reaches the limit, a line voltage drop indication is given.



As shown in the figure above, when the voltage RMS value is less than the threshold set in the Dropout Voltage Threshold Register (SAGLVL),

The drop time exceeds the set time in the drop line cycle register (SAGCYC) (the figure shows that it exceeds the

After 6 half cycles, SAGCYC[11:0]=0x06), the line voltage drop event is detected by setting the interrupt status

The SAG flag in the STATUS1 register is used to record this.

0x96	STATUS1		
Location	Interrupt flag	default value	describe
0	sag	0	Line voltage drop

If the corresponding SAG enable bit in the interrupt mask register (MASK1) is logic 0, the /IRQ logic

The edit output becomes active low.

The number of drop cycles and the threshold value of the drop voltage can be set. The drop voltage threshold register (SAGLVL)

Can be written or read by the user, the initial value is 0x100, the drop line cycle register (SAGCYC) can also

Written or read by the user, the initial value is 0x04.

Address	Name	Bit Width	Default Value	Description
8E	SAGCYC/ ZXTOUT	24	0x04FFFF [23:16]	Falling line period register SAGCYC, default value is 0x04.
8F	SAGLVL/ LINECYC	24	0x100009	[23:12] Dropout voltage threshold register SAGLVL, voltage channel The input value is lower than this register value for more than SAGCYC. The line voltage drop interrupt will be generated at the time of Approximately 1/16 full-scale voltage input.

3.10.4 Zero Crossing Timeout

The zero-crossing detection circuit is also connected to a register ZXTOUT that detects the zero-crossing signal timeout.

When there is a zero-crossing signal on the pressure channel, ZXTOUT is set to the initial value. If there is no zero-crossing signal, it decreases.

If there is no zero-crossing signal output for a long time, the value in this register will become 0.



The corresponding bit ZXTO is set to 1. If the corresponding enable bit ZXTO in the interrupt mask register is 0, then

The zero-crossing signal timeout event is also reflected on the interrupt pin/IRQ.

Whether the enable bit is set or not, the ZXTO flag in the interrupt status register (STATUS1) is always in the ZXTOUT

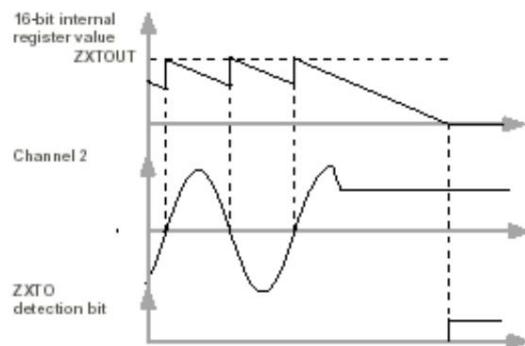
The register is set to valid 1 when it decrements to 0.

Address	Name	Bit Width	Default Value	Description
8E	SAGCYC/ ZXTOUT	24	0x04FFFF	[15:0] Zero crossing timeout register ZXTOUT. If there is no zero-crossing signal within the time indicated by the register, a zero-crossing signal will be generated. Timeout interrupt, default value is 0xFFFF.

The zero crossing timeout register ZXTOUT can be written or read by the user, and the initial value is 0xFFFF.

The resolution of the device is 70.5us/LSB, so the maximum delay time of an interrupt is limited to 4.369s.

The following figure shows the mechanism of detecting zero-crossing timeout when the line voltage is always a fixed DC signal:



3.10.5 Power supply indication

Contains an on-chip power supply monitoring circuit that continuously monitors the analog power supply (AVDD).

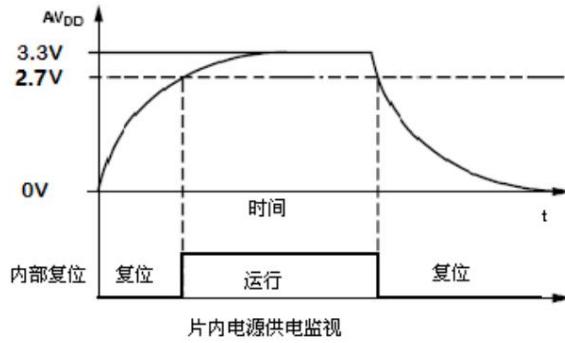
If the power supply voltage is less than $2.7V \pm 5\%$, the entire circuit will not be activated (will not work).

This ensures that the device maintains correct operation during power-on and power-off.

This power monitoring circuit has hysteresis and filtering mechanisms, which can largely eliminate errors caused by noise.

In general, the decoupling part of the power supply should ensure that the ripple on AVDD does not exceed

$3.3V \pm 5\%$



3.10.6 ADC shutdown

Address	Name	Bit Width	Default Value	Description
93	ADC_PD	11	0x000	11 channel ADC enable control: [0]-11 channels; [1] -1 channel; [2] - 2 channels; [3]-3 channels; [4] - 4 channels; [5]-5 channels; [6]-6 channels; [7]-7 channels; [8]-8 channels; [9]-9 channels; [10]-10 channels

This function can be used to shut down channels that do not need to work and reduce power consumption.

4. Internal registers

4.1 Electrical parameter registers

Address	Name	Bit width	default value	description
1	WAVE[1]	24	0x000000	1 channel waveform register
2	WAVE[2]	24	0x000000	2-channel waveform register (
3	WAVE[3]	24	0x000000	3-channel waveform register
4	WAVE[4]	24	0x000000	4-channel waveform register



BL0910 ten-phase AC power metering chip

5	WAVE[5]	24	0x000000	5-channel waveform register
6	WAVE[6]	24	0x000000	6-channel waveform register
7	WAVE[7]	24	0x000000	7-channel waveform register
8	WAVE[8]	24	0x000000	8-channel waveform registers
9	WAVE[9]	24	0x000000	9-channel waveform registers
A	WAVE[10]	24	0x000000	10-channel waveform register
B	WAVE[11]	24	0x000000	11 channels waveform registers
C	RMS[1]	24	0x000000	1 channel effective value register, unsigned
D	RMS[2]	24	0x000000	2-channel effective value register, unsigned
AND	RMS[3]	24	0x000000	3-channel effective value register, unsigned
F	RMS[4]	24	0x000000	4 Channel effective value register, unsigned
10	RMS[5]	24	0x000000	5-channel effective value register, unsigned
11	RMS[6]	24	0x000000	6-channel effective value register, unsigned
12	RMS[7]	24	0x000000	7 Channel effective value register, unsigned
13	RMS[8]	24	0x000000	8-channel effective value register, unsigned
14	RMS[9]	24	0x000000	9-channel effective value register, unsigned
15	RMS[10]	24	0x000000	10-channel effective value register, unsigned
16	RMS[11]	24	0x000000	11 Channel effective value register, unsigned
17	FAST_RMS[1]	24	0x000000	1 channel fast (leakage current) effective value register,
18	FAST_RMS[2]	24	0x000000	2-channel fast (leakage current) effective value register,
19	FAST_RMS[3]	24	0x000000	3-channel fast (leakage current) RMS register,
1A	FAST_RMS[4]	24	0x000000	4-channel fast (leakage current) effective value register,
1B	FAST_RMS[5]	24	0x000000	5-channel fast (leakage current) effective value register,
1C	FAST_RMS[6]	24	0x000000	6-channel fast (leakage current) RMS register,
1D	FAST_RMS[7]	24	0x000000	7-channel fast (leakage current) effective value register,
1E	FAST_RMS[8]	24	0x000000	8-channel fast (leakage current) RMS registers,
1F	FAST_RMS[9]	24	0x000000	9-channel fast (leakage current) RMS register,
20	FAST_RMS[10]	24	0x000000	10-channel fast (leakage current) RMS register,
21	FAST_RMS[11]	24	0x000000	11-channel fast (leakage current) effective value register,
22	WATT[1]	24	0x000000	Channel 1 active power register
23	WATT[2]	24	0x000000	Channel 2 active power register
24	WATT[3]	24	0x000000	Channel 3 active power register
25	WATT[4]	24	0x000000	Channel 4 active power register



BL0910 ten-phase AC power metering chip

26	WATT[5]	24	0x000000 Channel 5 active power register
27	WATT[6]	24	0x000000 Channel 6 Active Power Register
28	WATT[7]	24	0x000000 Channel 7 Active Power Register
29	WATT[8]	24	0x000000 Channel 8 Active Power Register
2A	WATT[9]	24	0x000000 Channel 9 Active Power Register
2B	WATT[10]	24	0x000000 Channel 10 Active Power Register
2C	WATT	24	0x000000 Total active power register
2D	FVAR	24	0x000000 Optional channel reactive power register
2E	AND	24	0x000000 Optional channel apparent power register
2F	CF[1]_CNT	24	0x000000 Channel 1 active pulse count, unsigned
30	CF[2]_CNT	24	0x000000 Channel 2 active pulse count, unsigned
31	CF[3]_CNT	24	0x000000 Channel 3 active pulse count, unsigned
32	CF[4]_CNT	24	0x000000 Channel 4 active pulse count, unsigned
33	CF[5]_CNT	24	0x000000 Channel 5 active pulse count, unsigned
34	CF[6]_CNT	24	0x000000 Channel 6 Active pulse count, unsigned
35	CF[7]_CNT	24	0x000000 Channel 7 active pulse count, unsigned
36	CF[8]_CNT	24	0x000000 Channel 8 active pulse count, unsigned
37	CF[9]_CNT	24	0x000000 Channel 9 active pulse count, unsigned
38	CF[10]_CNT	24	0x000000 Channel 10 active pulse count, unsigned
39	CF_CNT	24	0x000000 Total active pulse count, unsigned
3A	CFQ_CNT	24	0x000000 Optional channel reactive pulse count, unsigned
3B	CFS_CNT	24	0x000000 Optional channel apparent pulse count, unsigned
3C	ANGLE[1]	16	0x000000 Channel 1 Current and voltage waveform angle register
3D	ANGLE[2]	16	0x000000 Channel 2 Current and Voltage Waveform Angle Register
3E	ANGLE[3]	16	0x000000 Channel 3 Current and voltage waveform angle register
3F	ANGLE[4]	16	0x000000 Channel 4 Current and voltage waveform angle register
40	ANGLE[5]	16	0x000000 Channel 5 Current and voltage waveform angle register
41	ANGLE[6]	16	0x000000 Channel 6 Current and voltage waveform angle register
42	ANGLE[7]	16	0x000000 Channel 7 Current and voltage waveform angle register
43	ANGLE[8]	16	0x000000 Channel 8 Current and voltage waveform angle register
44	ANGLE[9]	16	0x000000 Channel 9 Current and voltage waveform angle register
45	ANGLE[10]	16	0x000000 Channel 10 Current and voltage waveform angle register
46	FAST_RMS_H[1]	24	0x000000 1 Channel fast (leakage current) effective value storage register



BL0910 ten-phase AC power metering chip

				Memory
47	FAST_RMS_H [2] 24		0x000000	2-channel fast (leakage current) effective value storage register Memory
48	FAST_RMS_H [3] 24		0x000000	3-channel fast (leakage current) effective value storage register Memory
49	FAST_RMS_H [4] 24		0x000000	4-channel fast (leakage current) effective value storage register Memory
4A	PF	24	0x000000	Optional channel power factor register
4B	LINE_WATTHR	24	0	Line cycle accumulated active energy register
4C	LINE_VARHR	24	0	Line cycle accumulated reactive energy register
4D	SIGN	24	0x000000	Power sign bit. Corresponding to the current energy pulse count The sign bit is refreshed when the CF pulse is output.
4E	PERIOD	20	0x000000	Line voltage frequency period register (optional channel), To extract from the voltage fundamental
4F Reserved				
50 Reserved				
51 Reserved				
52 Reserved				
53 Reserved				
54	STATUS1	24	0x000000	Interrupt status register 1
55 Reserved				
56	STATUS3	10	0x000	M Status Register
57	FAST_RMS_H [5] 24		0x000000	5-channel fast (leakage current) effective value storage register Memory
58	FAST_RMS_H [6] 24		0x000000	6-channel fast (leakage current) effective value storage register Memory
59	FAST_RMS_H [7] 24		0x000000	7 Channel fast (leakage current) effective value storage register Memory
5A	FAST_RMS_H [8] 24		0x000000	8-channel fast (leakage current) effective value storage register Memory
5B	FAST_RMS_H [9] 24		0x000000	9-channel fast (leakage current) effective value storage register Memory
5C	FAST_RMS_H [10] 24		0x000000	10-channel fast (leakage current) effective value storage register Memory



BL0910 ten-phase AC power metering chip

5D Reserved				
5E	TPS1	10	0x000000 Internal temperature value register	
5F	TPS2	10	0x000000 External temperature value register	

4.2 Calibration register (external write)

Address	Name	Bit width	default value	description
60	GAIN1	24	0x000000	Channel PGA gain adjustment register [3:0]: Voltage channel [7:4]: 1 channel [11:8]: 2 channels [15:12]: 3 channels [19:16]: 4 channels [23:20]: 5 channels
61	GAIN2	20	0x00000	Channel PGA gain adjustment register [3:0]: 6 channels [7:4]: 7 channels [11:8]: 8 channels [15:12]: 9 channels [19:16]: 10 channels
62	Reserved			
63	Reserved			
64	PHASE[1]/ PHASE[2]	16	0x1010	[15:8]: 1 channel phase compensation [7:0]: 2-channel phase compensation
65	PHASE[3]/ PHASE[4]	16	0x1010	[15:8]: 3-channel phase compensation [7:0]: 4-channel phase compensation
66	PHASE[5]/ PHASE[6]	16	0x1010	[15:8]: 5-channel phase compensation [7:0]: 6-channel phase compensation
67	PHASE[7]/ PHASE[8]	16	0x1010	[15:8]: 7-channel phase compensation [7:0]: 8-channel phase compensation
68	PHASE[9]/ PHASE[10]	16	0x1010	[15:8]: 9-channel phase compensation [7:0]: 10-channel phase compensation
69	PHASE[11]	8	0x10	[7:0]: 11-channel phase compensation
6A	VAR_PHCAL_I	5	0000H	Current channel reactive phase correction



BL0910 ten-phase AC power metering chip

6B	VAR_PHCAL_V	5	0000H Voltage	channel reactive phase correction
6C	RMSGN[1]	16 0x0000		1 Channel RMS gain adjustment register
6D	RMSGN[2]	16 0x0000	2 Channel RMS	gain adjustment register
6E	RMSGN[3]	16 0x0000	3 Channel RMS	gain adjustment register
6F	RMSGN[4]	16 0x0000	4 Channel RMS	gain adjustment register
70	RMSGN[5]	16 0x0000	5 Channel RMS	gain adjustment register
71	RMSGN[6]	16 0x0000	6 Channel RMS	gain adjustment register
72	RMSGN[7]	16 0x0000	7 Channel RMS	gain adjustment register
73	RMSGN[8]	16 0x0000	8-channel effective value	gain adjustment register
74	RMSGN[9]	16 0x0000	9 Channel RMS	gain adjustment register
75	RMSGN[10]	16 0x0000		10-channel RMS gain adjustment register
76	RMSGN[11]	16 0x0000		11 Channel RMS gain adjustment register
77	RMSOS[1]	24 0x000000	1 Channel RMS	offset correction register
78	RMSOS[2]	24 0x000000	2 Channel RMS	offset correction register
79	RMSOS[3]	24 0x000000	3 Channel RMS	offset correction register
7A	RMSOS[4]	24 0x000000	4 Channel RMS	offset correction register
7B	RMSOS[5]	24 0x000000	5 Channel RMS	offset correction register
7C	RMSOS[6]	24 0x000000	6 Channel RMS	offset correction register
7D	RMSOS[7]	24 0x000000	7 Channel RMS	offset correction register
7E	RMSOS[8]	24 0x000000	8-channel RMS	offset correction register
7F	RMSOS[9]	24 0x000000	9 Channel RMS	offset correction register
80	RMSOS[10]	24 0x000000	10 Channel RMS	offset correction register
81	RMSOS[11]	24 0x000000	10 Channel RMS	offset correction register
82	WA_LOS[1]/ WA_LOS[2]	24 0x000000		[23:12]: Channel 1 active power small signal compensation register Device [11:0]: Channel 2 active power small signal compensation register
83	WA_LOS[3]/ WA_LOS[4]	24 0x000000		[23:12]: Channel 3 active power small signal compensation register Device [11:0]: Channel 4 active power small signal compensation register
84	WA_LOS[5]/ WA_LOS[6]	24 0x000000		[23:12]: Channel 5 active power small signal compensation register Device [11:0]: Channel 6 active power small signal compensation register
85	WA_LOS[7]/	24 0x000000	[23:12]: Char	nel 7 active power small signal compensation register



BL0910 ten-phase AC power metering chip

	WA_LOS[8]			Device [11:0]: Channel 8 active power small signal compensation register
86	WA_LOS[9]/ WA_LOS[10]	24 0x000000		[23:12]: Channel 9 active power small signal compensation register Device [11:0]: Channel 10 active power small signal compensation register Device
87	FVAR_LOS/	24 0x000000		[11:0] Reserved [23:12] Corresponding reactive (fundamental wave) small signal compensation register Device, complement.
88	VAR_CREEP/ WA_CREEP	24 0x04C04C		[11:0] is the active anti-creep power threshold register WA_CREEP [23:12] is the reactive power protection threshold register VAR_CREEP
89	WA_CREEP2	12	0x000 [11:0]	Total active power anti-creep threshold register
8A	RMS_CREEP	12	0x200	Effective value small signal threshold register
8B	FAST_RMS_CTRL	24 0x20FFFF		[23:21] Channel fast effective value register refresh time, You can choose between half cycle and N cycle, the default is cycle; [20:0] Channel fast effective value threshold register
8C	I_PKLV/L/ V_PKLV	24 0xFFFFFFF		[23:12] Current peak threshold register I_PKLV; [11:0] Voltage peak threshold register V_PKLV
8D	Reserved			
8E	SAGCYC/ ZXTOUT	24 0x04FFFF		[23:16] Drop line cycle register SAGCYC, default 0x04 [15:0] Zero crossing timeout register ZXTOUT, if If there is no zero crossing signal within the time indicated by the register, a Zero-crossing timeout interrupt, default value is 0xFFFF.
8F	SAGLVL/ LINECYC	24 0x100009		[23:12] Falling voltage threshold register SAGLVL, voltage The channel input is continuously lower than the value of this register for more than The time in SAGCYC will cause a line voltage drop interruption. The default is 0x100, which is approximately 1/16 of the full-scale voltage input. [11:0] Line energy accumulation cycle number register LINECYC, The default value is 0x009, which means 10 cycles.
90	flag_ctrl	24 0x000000		The master controller directly controls the output level of M10~M1 [21:12] is the priority of M10~M1 output



BL0910 ten-phase AC power metering chip

				[0]: 1 channel; [1]: 2 channels; [2]: 3 channels; [3]: 4 channels; [4]: 5 channels; [5]: 6 channels; [6]: 7 channels; [7]: 8 channels; [8]: 9 channels; [9]: 10 channels
91	flag_ctrl1	24	0x00000000	Overcurrent indication control register 1. [23:10] Disconnection delay timing, 0.1ms/lsb; [9:0] Indication control, M1-M6: 0-output real-time interrupt; 1-Output delay control [0]: 1 channel; [1]: 2 channels; [2]: 3 channels; [3]: 4 channels; [4]: 5 channels; [5]: 6 channels; [6]: 7 channels; [7]: 8 channels; [8]: 9 channels; [9]: 10 channels
92	flag_ctrl2	24	0x00000000	Overcurrent indication control register 2. [23:10] Close delay timing, 0.1ms/lsb; [9:0] Close control, M1-M6: 0-close, 1-open [0]: 1 channel; [1]: 2 channels; [2]: 3 channels; [3]: 4 channels; [4]: 5 channels; [5]: 6 channels; [6]: 7 channels; [7]: 8 channels; [8]: 9 channels; [9]: 10 channels
93	ADC_PD	11	0x000	11 channel ADC enable control: [0] - 11 channels; [1] - 1 channel; [2]-2 channel; [3]-3 channel; [4]-4 channels; [5]-5 channels; [6]-6 channel; [7]-7 channel; [8]-8 channel; [9]-9 channel; [10]-10 channels
94	TPS_CTRL	16	0x07FF	[15] Switch: 1-off, 0-on, default; [14] External temperature alarm release switch: 1-alarm off, 0-alarm on, default; [13:12] Temperature measurement selection: 00, 02- Automatic temperature measurement, default



BL0910 ten-phase AC power metering chip

				10- Select internal temperature measurement, 11-Select external temperature measurement; [11:10] Temperature measurement start time interval selection: 00-50ms 01-100ms, default 10-200ms 11-400ms [9:0] External temperature alarm threshold setting, default value is 0x3ff
95	TPS2_A/ TPS2_B	24 0x0000		External temperature sensor coefficient A correction register/external temperature Sensor coefficient B correction register
96	MODE1	24 0x000000	User mode selection register	
97 Reserved				
98	MODE	24 0x000000	User mode selection register	
99 Reserved				
9A	MASK1	24 0x000000		Interrupt mask register, controls whether an interrupt generates an A valid IRQ1 output is associated with the STATUS1 register. Bit description corresponds to
9B Reserved				
9C Reserved				
9D	RST_ENG	24 0x000000		Energy reset setting register, see "Energy reset setting register" for details. Register Description
9E	USR_WRPRT	16 0x00		User write protection setting register, when writing 5555H, table The operable user register pairs reg60 to reg9d are shown. rega0 to d0
9F	SOFT_RESET	24 0x000000		When the input is 5A5A5A, the system resets - only resets State machines and registers for the digital part! When the input is 55AA55, the user read and write register is reset —Reset: reg60 to reg9f, rega0 to regd0

4.3 Calibration register (writable)

Address	Name	Bit width	default value	description
A0	CHGN[1]	16	0x0000	1 Channel gain adjustment register, two's complement
A1	CHGN[2]	16	0x0000	2 Channel gain adjustment register, two's complement



BL0910 ten-phase AC power metering chip

A2	CHGN[3]	16	0x0000 3 Channel gain adjustment register, two's complement
A3	CHGN[4]	16	0x0000 4-channel channel gain adjustment register, two's complement
A4	CHGN[5]	16	0x0000 5 Channel gain adjustment register, two's complement
A5	CHGN[6]	16	0x0000 6-channel channel gain adjustment register, two's complement
A6	CHGN[7]	16	0x0000 7 Channel gain adjustment register, two's complement
A7	CHGN[8]	16	0x0000 8-channel channel gain adjustment register, two's complement
A8	CHGN[9]	16	0x0000 9-channel channel gain adjustment register, two's complement
A9	CHGN[10]	16	0x0000 10 Channel gain adjustment register, two's complement
AA	CHGN[11]	16	0x0000 11 Channel gain adjustment register, two's complement
AB	FOOT[1]	16	0x0000 1 Channel offset adjustment register, two's complement
AC	FOOT [2]	16	0x0000 2 Channel offset adjustment register, two's complement
AD	FOOT[3]	16	0x0000 3 Channel offset adjustment register, two's complement
BUT	FOOT[4]	16	0x0000 4-channel channel offset adjustment register, two's complement
OF	FOOT[5]	16	0x0000 5 Channel offset adjustment register, two's complement
B0	FOOT[6]	16	0x0000 6-channel channel offset adjustment register, two's complement
B1	FOOT[7]	16	0x0000 7 Channel offset adjustment register, two's complement
B2	FOOT[8]	16	0x0000 8-channel channel offset adjustment register, two's complement
B3	FOOT[9]	16	0x0000 9-channel channel offset adjustment register, two's complement
B4	FOOT[10]	16	0x0000 10 Channel offset adjustment register, two's complement
B5	FOOT [11]	16	0x0000 11 Channel offset adjustment register, two's complement
B6	WATTGN[1]	16	0x0000 Channel 1 active power gain adjustment register, two's complement
B7	WATTGN[2]	16	0x0000 Channel 2 active power gain adjustment register, two's complement
B8	WATTGN[3]	16	0x0000 Channel 3 active power gain adjustment register, two's complement
B9	WATTGN[4]	16	0x0000 Channel 4 active power gain adjustment register, two's complement
NOT	WATTGN[5]	16	0x0000 Channel 5 active power gain adjustment register, two's complement
BB	WATTGN[6]	16	0x0000 Channel 6 active power gain adjustment register, two's complement
BC	WATTGN[7]	16	0x0000 Channel 7 active power gain adjustment register, two's complement
BD	WATTGN[8]	16	0x0000 Channel 8 active power gain adjustment register, two's complement
BE	WATTGN[9]	16	0x0000 Channel 9 active power gain adjustment register, two's complement
BF	WATTGN[10]	16	0x0000 Channel 10 active power gain adjustment register, two's complement
C0	WATTS[1]	16	0x0000 Channel 1 active power bias adjustment register, two's complement
C1	WATTS[2]	16	0x0000 Channel 2 active power bias adjustment register, two's complement
C2	WATTS[3]	16	0x0000 Channel 3 active power bias adjustment register, two's complement



BL0910 ten-phase AC power metering chip

C3	WATTS[4]	16	0x0000 Channel 4 active power bias adjustment register, two's complement
C4	WATTS[5]	16	0x0000 Channel 5 active power bias adjustment register, two's complement
C5	WATTS[6]	16	0x0000 Channel 6 active power bias adjustment register, two's complement
C6	WATTS[7]	16	0x0000 Channel 7 active power bias adjustment register, two's complement
C7	WATTS[8]	16	0x0000 Channel 8 active power bias adjustment register, two's complement
C8	WATTS[9]	16	0x0000 Channel 9 active power bias adjustment register, two's complement
C9	WATTS[10]	16	0x0000 Channel 10 active power bias adjustment register, two's complement
THAT	VARGN	16	0x0000 Corresponding channel reactive power gain adjustment register, complement code
CB	CITY	16	0x0000 Corresponding channel reactive power bias adjustment register, complement code
CC WAGON		16	0x0000 corresponds to the channel apparent power gain adjustment register, complement code
VAOS CD		16	0x0000 corresponds to the channel apparent power offset adjustment register, complement code
THIS	CFDIV	12	CF Scaling Factor Register
CF Sky			reserve
D0	OTP checksum1 16		Checksum1 of the calibration register has a problem and is restored to 0 to rega0 to regd0

4.4 Mode Register

4.4.1 Mode Register (MODE)

0x96	MODE1	Working mode register 1	
No.	name	default value	description
[21:0] Reserved			
[22]	FAST_RMS_F	1'b0	0, fast effective value but high pass 1. Rapid effective value over high pass
[23] Reserved			

0x98	MODE	Working Mode Register	
No.	name	default value	description
[3:0] VAR_I_SEL		4'b000	Select reactive current measurement channel, select 1 from 10, default is 0000 0000;channel 1;0001;channel 2 0010;channel 3;0011;channel 4; 0100;channel 5;0101;channel 6; 0110;channel 7;0111;channel 8;



BL0910 ten-phase AC power metering chip

			1000-channel 9;1001-channel 10;
[8]	add_sel	1'b0	Watt total addition method: 0-absolute value addition; 1-algebraic sum addition
[9]	cf_enable	1'b0	0-cf disable, default; 1-cf enable
[13:10]	CF_SEL	4'b0000	<p>Channel CF_WATT output selection:</p> <p>0000, CF is turned off by default;</p> <p>0001, power CF of channel 1;</p> <p>0010, power CF of channel 2;</p> <p>0011, power CF of channel 3;</p> <p>0100, power CF of channel 4;</p> <p>0101, power CF of channel 5;</p> <p>0110, power CF of channel 6;</p> <p>0111, power CF of channel 7;</p> <p>1000, power CF of channel 8;</p> <p>1001, power CF of channel 9;</p> <p>1010, power CF of channel 10;</p> <p>1011, total active power CF;</p> <p>1100, reactive power CF (channel optional);</p> <p>1101, apparent power CF (channel optional);</p> <p>1110, 1111, turn off CF;</p> <p>In addition, CF_VAR is always the reactive power CF (channel optional).</p> <p>constant</p>
[14]	Reserved		
[15]	cf_add_sel	1'b0	<p>Watt and var energy addition method:</p> <p>0-absolute value addition; 1-algebraic sum addition (separate and combined)</p>
[16]	var_sel	1'b0	var energy selection: 0-base wave; 1-full wave
[19]	mode_sel	1'b0	0=1U10I mode 1=3U6I/5U5Imode

4.5 Interrupt Status Register (STATUS1/STATUS3)

4.5.1 STATUS1 register

Position interrupt	flag	default value	describe
0	sag	0	11 Channel line voltage drop
1	zxto	0	11 Channel zero crossing timeout
2	zx01	0	1 channel zero crossing signal



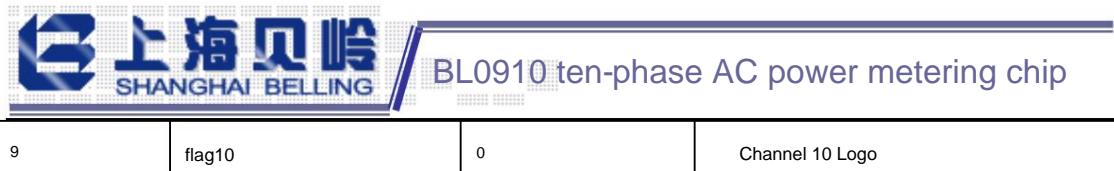
BL0910 ten-phase AC power metering chip

3	zx02	0	2-channel zero-crossing signal
4	zx03	0	3-channel zero-crossing signal
5	zx04	0	4-channel zero-crossing signal
6	zx05	0	5-channel zero-crossing signal
7	zx06	0	6-channel zero-crossing signal
8	zx07	0	7-channel zero-crossing signal
9	zx08	0	8-channel zero-crossing signal
10	zx09	0	9-channel zero-crossing signal
11	zx10	0	10-channel zero-crossing signal
12	zx11	0	11-channel zero-crossing signal
13	pk01	0	1 channel peak value exceeding limit signal
14	pk02	0	2 channels of peak over-limit signal
15	pk03	0	3-channel peak over-limit signal
16	pk04	0	4-channel peak over-limit signal
17	pk05	0	5-channel peak over-limit signal
18	pk06	0	6-channel peak over-limit signal
19	pk07	0	7-channel peak over-limit signal
20	pk08	0	8-channel peak over-limit signal
21	pk09	0	9-channel peak over-limit signal
22	pk10	0	10-channel peak over-limit signal
23	pkv		11 channels peak value exceeding limit signal

The output event status of the IRQ1 pin corresponds to the STATUS1 and MASK1 register bits.

4.5.2 STATUS3 register

Location	interrupt flag	default value	describe
0	flag01	0	Channel 1 Logo
1	flag02	0	Channel 2 Logo
2	flag03	0	Channel 3 Logo
3	flag04	0	Channel 4 Logo
4	flag05	0	Channel 5 logo
5	flag06	0	Channel 6 Logo
6	flag07	0	Channel 7 Logo
7	flag08	0	Channel 8 Logo
8	flag09	0	Channel 9 Logo



Fast RMS value exceeding threshold flag of corresponding channel

4.6 Detailed description of calibration registers

4.6.1 Channel PGA gain adjustment register

11 Channel PGA gain is adjustable. The data format of channel PGA gain adjustment registers GAIN1 and GAIN2 is

The formula is as follows: (Every 4 bits controls one channel, 0000=1; 0001=2; 0010=8; 0011=16).

Please note that after setting the gain of the corresponding channel, the maximum allowable input signal of the channel should also be reduced accordingly!

Address	Name	Bit Width	Default Value	Description
60	GAIN1	24	0x000000	Channel PGA gain adjustment register [3:0]: voltage channel; [7:4]: Current 1 channel [11:8]: Current 2 channel; [15:12]: Current 3 channel; [19:16]: Current 4 channels; [23:20]: Current 5 channel;
61	GAIN2	20	0x000000	Channel PGA gain adjustment register [3:0]: Current 6 channels [7:4]: Current 7 channel [11:8]: Current 8 channels [15:12]: Current 9 channel [19:16]: Current 10 channel

4.6.2 Phase Correction Register

11 Channel phase compensation is adjustable. The data format of the phase calibration register PHASE[N] is as follows:

Calibrate one channel, [7] is reserved, and the minimum adjustment delay time of [6:0] is 250ns, corresponding to 0.0045 degrees

/1LSB, corresponding error $\approx 1.732 \times \sin(0.0045^\circ) = 0.0136\%$, maximum adjustable ± 0.574 degrees, maximum

The maximum adjustment error is approximately 1.734%.

Address	Name	Bit width	default value	Description
64	PHASE[1]/PHASE[2] 16		0x0000	[15:8]: 1 channel phase compensation [7:0]: 2-channel phase compensation
65	PHASE[3]/PHASE[4] 16		0x0000	[15:8]: 3-channel phase compensation



BL0910 ten-phase AC power metering chip

				[7:0]: 4-channel phase compensation
66	PHASE[5]/PHASE[6] 16		0x0000	[15:8]: 5-channel phase compensation [7:0]: 6-channel phase compensation
67	PHASE[7]/PHASE[8] 16		0x0000	[15:8]: 7-channel phase compensation [7:0]: 8-channel phase compensation
68	PHASE[9]/PHASE[10] 16		0x0000	[15:8]: 9-channel phase compensation [7:0]: 10-channel phase compensation
69	PHASE[11]	8	0x00	[7:0]: 11-channel phase compensation

The phase compensation of the current and voltage channels for calculating reactive power is adjustable, the phase calibration register VAR_PHCAL_I

The data format of VAR_PHCAL_V is as follows: Reactive phase correction (fine-tuning): [3:0] is fine-tuning, [3] is

The minimum adjustment delay time is 500ns, corresponding to 0.009 degrees/1LSB, and the corresponding error is ±0.0245%.

The maximum adjustable value is ±0.072 degrees. Reactive phase correction (coarse adjustment): [12] is coarse adjustment. When it is 1, this channel has no

Power delay 64us.

Address	Name	Bit width	Default value	Description
6A	VAR_PHCAL_I	5	0x00	Current channel reactive phase correction
6B	VAR_PHCAL_V	5	0x00	Voltage channel reactive phase correction

4.6.3 Effective value gain adjustment register

Address	Name	Bit width	Default value	Description
6C	RMSGN[1]	16	0x0000	1 Channel RMS gain adjustment register
6D	RMSGN[2]	16	0x0000	2-channel effective value gain adjustment register
6E	RMSGN[3]	16	0x0000	3-channel effective value gain adjustment register
6F	RMSGN[4]	16	0x0000	4-channel RMS gain adjustment register
70	RMSGN[5]	16	0x0000	5-channel effective value gain adjustment register
71	RMSGN[6]	16	0x0000	6-channel RMS gain adjustment register
72	RMSGN[7]	16	0x0000	7-channel effective value gain adjustment register
73	RMSGN[8]	16	0x0000	8-channel RMS gain adjustment register
74	RMSGN[9]	16	0x0000	9-channel effective value gain adjustment register
75	RMSGN[10]	16	0x0000	10-channel RMS gain adjustment register
76	RMSGN[11]	16	0x0000	11 Channel RMS gain adjustment register

Channel effective value gain adjustment register, 16-bit complement code, the highest bit is the sign bit, used for effective value gain adjustment

Gain correction, adjustment range ±50%



$$[]_ = []_- \quad 0 \ddot{y} (1 + \frac{[]}{2^{16}})$$

Where $I[N]_{RMS0}$ is the measured value of the Nth channel, $RMSGN[N]$ is the gain correction value, and $I[N]_{RMS}$ is

The corresponding calibration output value.

4.6.4 RMS offset correction register

Address	Name	Bit width	Default value	Description
77	RMSOS[1]	24	0x000000	1 Channel RMS offset correction register
78	RMSOS[2]	24	0x000000	2-channel RMS offset correction register
79	RMSOS[3]	24	0x000000	3-channel RMS offset correction register
7A	RMSOS[4]	24	0x000000	4-channel RMS offset correction register
7B	RMSOS[5]	24	0x000000	5-channel RMS offset correction register
7C	RMSOS[6]	24	0x000000	6-channel RMS offset correction register
7D	RMSOS[7]	24	0x000000	7-channel RMS offset correction register
7E	RMSOS[8]	24	0x000000	8-channel RMS offset correction register
7F	RMSOS[9]	24	0x000000	9-channel RMS offset correction register
80	RMSOS[10]	24	0x000000	10 Channel RMS offset correction register
81	RMSOS[11]	24	0x000000	10 Channel RMS offset correction register

Channel effective value offset correction register, 24-bit complement code, the highest bit is the sign bit. Used to eliminate effective value

The deviation in the calculation due to input noise can make the effective value register value close to

0 \ddot{y}

$$[]_ = \ddot{y} []_- \quad 0 \dot{2} + [] \ddot{y} 256$$

Where $I[N]_{RMS0}$ is the measured value of the Nth channel, $RMSOS[N]$ is the gain correction value, and $I[N]_{RMS}$ is

The corresponding calibration output value.

4.6.5 Active small signal compensation register

Address	Name	Bit Width	Default Value	Description
82	WA_LOS[1]/ WA_LOS[2]	24	0x000000	[23:12]: Channel 1 active power small signal compensation register [11:0]: Channel 2 active power small signal compensation register



83	WA_LOS[3]/ WA_LOS[4]	24	0x000000	[23:12]: Channel 3 active power small signal compensation register [11:0]: Channel 4 active power small signal compensation register
84	WA_LOS[5]/ WA_LOS[6]	24	0x000000	[23:12]: Channel 5 active power small signal compensation register [11:0]: Channel 6 active power small signal compensation register
85	WA_LOS[7]/ WA_LOS[8]	24	0x000000	[23:12]: Channel 7 active power small signal compensation register [11:0]: Channel 8 active power small signal compensation register
86	WA_LOS[9]/ WA_LOS[10]	24	0x000000	[23:12]: Channel 9 active power small signal compensation register [11:0]: Channel 10 active power small signal compensation register

The active power small signal compensation register is used to compensate for the active power small signal deviation caused by DC bias.

$$[\cdot] = \text{WATT0[N]} + \text{WA_LOS[N]} - \text{VAR} \times 2^{12}$$

Where WATT0[N] is the measured value of the Nth channel, WA_LOS[N] is the offset correction value, and WATT[N] is the

The calibration output value of the corresponding channel.

Note that WA_LOS[N] is a signed number, two's complement, which can correct the active power register within the range of ± 4094 .

4.6.6 Reactive small signal compensation register

Address	Name	Bit width	Default value	Description
87	FVAR_LOS	24	0x000000	[11:0] Reserved [23:12] corresponds to the reactive small signal compensation register, code.

FVAR_LOS formula:

$$= \text{VAR0} + \text{FVAR_LOS} - \text{VAR} \times 2^{12}$$

Where VAR0 is the reactive power measurement value, FVAR_LOS is the offset correction value, and VAR is the calibration output value.

Note that FVAR_LOS is a signed number, two's complement, which can correct the reactive power register within the range of ± 4094 .

4.6.7 Anti-creep Threshold Register

Address	Name	Bit Width	Default Value	Description
88	VAR_CREEP	24	0x04C04C	[11:0] is the active anti-creep power threshold register WA_CREEP;



	WA_CREEP			[23:12] is the reactive power protection threshold register VAR_CREEPy
89	WA_CREEP2 12		0x000 [11:0]	Total active power anti-creep threshold register

The anti-creep power threshold register is used to set the active power/reactive power anti-creep setting for each channel.

When a channel is in the anti-submarine state, the power of the channel below the threshold does not participate in the energy accumulation.

When the absolute value of the instantaneous power signal is less than this value, the output power register value is set to zero.

In the no-load condition, even with a small noise signal, the value output to the active power register is 0.

$$\text{value} = \frac{\text{Corresponding power register value}}{2}$$

10 channels of total active power anti-creep threshold setting, if set Reg88 register, this register

This parameter can be left unset.

$$2 = \frac{\text{Register Value}}{2}$$

Address	Name	Bit width	default value	description
8A	RMS_CREEP	12	0x200	Effective value small signal threshold register

It can make the value output to the effective value register remain unchanged even with a small noise signal under no load condition.

is 0.

$$- = []_-$$

4.6.8 Fast effective value related setting register

Address	Name	Bit width	default value	description
8B	FAST_RMS_CTRL 24		0x20FFFF	[23:21] Channel fast effective value register refresh time, can be Select half cycle and N cycle, the default is cycle; [20:0] Channel fast effective value threshold register

The accumulation time is selected by FAST_RMS_CTRL[23:21], which is 10ms (000), 20ms (001), and 40ms.

There are six types: (010), 80ms (011), 160ms (100), and 320ms (101). The default (001) is the selected cycle.

The wave accumulation response time is 20ms. The longer the accumulation time is, the smaller the jump is.

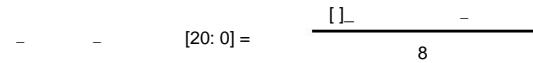
FAST_RMS_CTRL[20:0] is used to set the fast RMS value over-limit threshold. Once exceeded, the output flag



BL0910 ten-phase AC power metering chip

flag[N] is 1. The flag bit is connected to the output (M1~M10), which can directly output the leakage/overcurrent indication pin

Pull high. Can be used with the overcurrent indication control register.



4.6.9 Overcurrent alarm and control

Address	Name	Bit Width	Default Value	Description
90	flag_ctrl	22	0x000	<p>The master controller directly controls the output level of M10~M1</p> <p>[21:12] is the priority of M10~M1 output</p> <p>[0]: 1 channel; [1]: 2 channels;</p> <p>[2]: 3 channels; [3]: 4 channels;</p> <p>[4]: 5 channels; [5]: 6 channels;</p> <p>[6]: 7 channels; [7]: 8 channels;</p> <p>[8]: 9 channels; [9]: 10 channels</p>
91	flag_ctrl1	24	0x000000	<p>Overcurrent indication control register 1.</p> <p>[23:10] Disconnection delay timing, 0.1ms/lsb;</p> <p>[9:0] Indication control, M1-M6: 0-output real-time</p> <p>Off; 1-Output delay control</p> <p>[0]: 1 channel; [1]: 2 channels;</p> <p>[2]: 3 channels; [3]: 4 channels;</p> <p>[4]: 5 channels; [5]: 6 channels;</p> <p>[6]: 7 channels; [7]: 8 channels;</p> <p>[8]: 9 channels; [9]: 10 channels</p>
92	flag_ctrl2	24	0x000000	<p>Overcurrent indication control register 2.</p> <p>[23:10] Close delay timing, 0.1ms/lsb;</p> <p>[9:0] Closed control, M1-M6: 0- Closed, 1-</p> <p>disconnect</p> <p>[0]: 1 channel; [1]: 2 channels;</p> <p>[2]: 3 channels; [3]: 4 channels;</p> <p>[4]: 5 channels; [5]: 6 channels;</p> <p>[6]: 7 channels; [7]: 8 channels;</p> <p>[8]: 9 channels; [9]: 10 channels</p>

Flag_ctrl register, Bit[9:0] is the level control of M10~M1 output;



Bit[21:12] is the control priority of M10~M1 output. When the corresponding position is 1, it can be controlled by Bit[9:0]

The corresponding bit state directly controls the output level of M10~M1. It has priority over flag_ctrl1 and flagg_ctrl2.

Higher level.

Channel 10		9	8	7	6	5	4	3	2	1
Bit 21		20	19	18	17	16	15	14	13	12
When Bit[21:12]=1, M10~M1 pins output signals according to Bit[9:0]										
Bit 9		8	7	6	5	4	3	2	1	0
When Bit[9:0]=0, the corresponding channel outputs low level; =1, outputs high level										

Real-time alarm output

Output the alarm high level of the corresponding channel in real time through the M10~M1 pins.

Value register Reg8B (FAST_RMS_CTRL), fast effective value refresh time/fast effective value threshold;

Logic description of delay control 1)

Set Reg8B register, fast effective value refresh time/fast effective value threshold;

2) Set the Reg91 register, Bit[23:10] delays the output high level time T1, Bit[9:0] turns on

Delay control of the corresponding channel;

3) Set the Reg92 register, Bit[23:10] delays the output low level time T2, Bit[9:0]=0;

-----Run the process-----

4) If a fast RMS over-limit event occurs on channel N, the I[N]_FAST_RMS_HOLD register is retained.

The fast effective value when the limit is exceeded; then T1 seconds later, the corresponding M[N] pin is pulled high, and the Reg56 register

The corresponding indication status bit is 1;

-----After the quick effective value over-limit fault is eliminated-----

5) MCU writes the delay output low level time T2 to the Reg92 register, the corresponding channel of Bit[9:0]

[N] position is 1; M[N] pin is pulled low after T2 delay, and Reg56 status is cleared;

6) MCU writes to Reg92 register, Bit[23:10] = T2 delay time, the corresponding pass of Bit[9:0]

Set the channel [N] position to 0 and clear the corresponding I[N]_FAST_RMSHOLD register value.

4.6.10 ADC Enable Control

Address	Name	Bit Width	Default	Value Description
93	ADC_PD	11	0x000	11 channel ADC enable control: [0] - 11 channels; [1] - 1 channel; [2]-2 channel; [3]-3 channel; [4]-4 channels; [5]-5 channels; [6]-6 channel; [7]-7 channel; [8]-8 channel; [9]-9 channel;



You can reduce power consumption by turning off unused channels.

ADC of the road.

4.6.11 Energy Read Clear Setting Register

Address	Name	Bit Width	Default Value	Description				
9D	RST_ENG	13	0x0000	Energy pulse count register cleared after reading				

When Bit[12:0] is set to 1, the energy-related registers Reg3B~2F are set to clear after reading.

set up.

Bit	12	11	99	2	1	0
Energy pulse register value address (0x) 3B		3A	99	31	30	2F

4.6.12 User write protection setting register

Address	Name	Bit Width	Default Value	Description			
9E	USR_WRPROT	16	0x0000	User write protection setting register, when writing 0x5555, indicates the operable user register pair reg60 to reg9d, rega0 to d0			

BL0910 has a strict protection mechanism for register writing. You must first write to the write protection setting register.

0x5555 can be used to write to other registers.

4.6.13 Soft Reset Register

Address	Name	Bit Width	Default Value	Description			
9F	SOFT_RESET	24	0x000000	When the input is 5A5A5A, the system resets - only resets State machines and registers for the digital part! When the input is 55AA55, the user read and write register is reset —Reset: reg60 to reg9f, rega0 to regd0			

4.6.14 Channel gain adjustment register

Address	Name	Bit width	Default value	Description			



BL0910 ten-phase AC power metering chip

A0	CHGN[1]	16	0x0000	1 channel channel gain adjustment register, two's complement
A1	CHGN[2]	16	0x0000	2-channel channel gain adjustment register, two's complement
A2	CHGN[3]	16	0x0000	3-channel channel gain adjustment register, two's complement
A3	CHGN[4]	16	0x0000	4-channel channel gain adjustment register, two's complement
A4	CHGN[5]	16	0x0000	5-channel channel gain adjustment register, two's complement
A5	CHGN[6]	16	0x0000	6-channel channel gain adjustment register, two's complement
A6	CHGN[7]	16	0x0000	7-channel channel gain adjustment register, two's complement
A7	CHGN[8]	16	0x0000	8-channel channel gain adjustment register, two's complement
A8	CHGN[9]	16	0x0000	9-channel channel gain adjustment register, two's complement
A9	CHGN[10]	16	0x0000	10-channel channel gain adjustment register, two's complement
AA	CHGN[11]	16	0x0000	11-channel channel gain adjustment register, two's complement

Channel gain adjustment register, 16-bit signed number, adjusts the AD of the corresponding channel in 2's complement form

The gain of the sampling waveform can be adjusted within the range of $\pm 50\%$

$$[\] = 0[\] \times (1 + \frac{[\]}{2^{16}})$$

Where WAVE0[N] is the measured value of channel N, CHGN[N] is the gain calibration value, and WAVE[N] is the calibration value.

output value.

4.6.15 Channel offset adjustment register

Address Name		Bit width	default value	description
AB	FOOT[1]	16	0x0000	1 channel channel offset adjustment register, two's complement
AC	FOOT [2]	16	0x0000	2-channel channel offset adjustment register, two's complement
AD	FOOT[3]	16	0x0000	3-channel channel offset adjustment register, two's complement
BUT	FOOT[4]	16	0x0000	4-channel channel offset adjustment register, two's complement
OF	FOOT[5]	16	0x0000	5-channel channel offset adjustment register, two's complement
B0	FOOT[6]	16	0x0000	6-channel channel offset adjustment register, two's complement
B1	FOOT[7]	16	0x0000	7-channel channel offset adjustment register, two's complement
B2	FOOT[8]	16	0x0000	8-channel channel offset adjustment register, two's complement
B3	FOOT[9]	16	0x0000	9-channel channel offset adjustment register, two's complement
B4	FOOT[10]	16	0x0000	10-channel channel offset adjustment register, two's complement
B5	FOOT [11]	16	0x0000	11-channel channel offset adjustment register, two's complement

The channel offset adjustment register uses 2's complement data to eliminate the current channel and voltage channel respectively.



The deviation here may be caused by the input and the analog-to-digital conversion circuit itself.

Deviation correction can make the waveform offset to 0 under no-load condition.

$$\text{WAVE}[N] = \text{WAVE}0[N] + \text{CHOS}[N]*2$$

Where $\text{WAVE}0[N]$ is the measured value of channel N, $\text{CHOS}[N]$ is the calibration value, and $\text{WAVE}[N]$ is the calibrated value.

output value.

4.6.16 Active power gain adjustment register

Address	Name	Bit Width	Default Value	Description
B6	WATTGN[1]	16	0x0000	Channel 1 active power gain adjustment register, two's complement
B7	WATTGN[2]	16	0x0000	Channel 2 active power gain adjustment register, two's complement
B8	WATTGN[3]	16	0x0000	Channel 3 active power gain adjustment register, two's complement
B9	WATTGN[4]	16	0x0000	Channel 4 active power gain adjustment register, two's complement
NOT	WATTGN[5]	16	0x0000	Channel 5 active power gain adjustment register, two's complement
BB	WATTGN[6]	16	0x0000	Channel 6 active power gain adjustment register, two's complement
BC	WATTGN[7]	16	0x0000	Channel 7 active power gain adjustment register, two's complement
BD	WATTGN[8]	16	0x0000	Channel 8 active power gain adjustment register, two's complement
BE	WATTGN[9]	16	0x0000	Channel 9 active power gain adjustment register, two's complement
BF	WATTGN[10]	16	0x0000	Channel 10 active power gain adjustment register, two's complement

Active power gain adjustment register, 16-bit signed number, adjusts the corresponding channel power in 2's complement form.

Rate gain:

$$\text{WATT}[N] = \text{WATTO}[N] \times (1 + \frac{[]}{2^{16}})$$

$\text{WATT}[N]$ is the active power after the Nth channel is calibrated, and $\text{WATTO}[N]$ is the active power before the Nth channel is calibrated.

Active power. Adjustment range $\pm 50\%$.

4.6.17 Active Power Bias Adjustment Register

Address	Name	Bit Width	Default Value	Description
C0	WATTS[1]	16	0x0000	Channel 1 active power bias adjustment register, two's complement
C1	WATTS[2]	16	0x0000	Channel 2 active power bias adjustment register, two's complement



BL0910 ten-phase AC power metering chip

C2	WATTS[3]	16	0x0000 Channel 3 active power bias adjustment register, two's complement
C3	WATTS[4]	16	0x0000 Channel 4 active power bias adjustment register, two's complement
C4	WATTS[5]	16	0x0000 Channel 5 active power bias adjustment register, two's complement
C5	WATTS[6]	16	0x0000 Channel 6 active power bias adjustment register, two's complement
C6	WATTS[7]	16	0x0000 Channel 7 active power bias adjustment register, two's complement
C7	WATTS[8]	16	0x0000 Channel 8 active power bias adjustment register, two's complement
C8	WATTS[9]	16	0x0000 Channel 9 active power bias adjustment register, two's complement
C9	WATTS[10]	16	0x0000 Channel 10 active power bias adjustment register, two's complement

Active power bias adjustment register, two's complement, highest bit is the sign bit. Used to eliminate board-level noise.

Active power deviation.

$$[] = \frac{WATT0[N] + WATTOS[N]}{2}$$

Where WATT0[N] is the measured value of the Nth channel, WATTOS[N] is the offset correction value, and WATT[N] is the

The corresponding calibration output value.

4.6.18 Reactive/apparent power gain adjustment register

Address Name	Bit Width	Default Value	Description		
THAT	VARGN	16	0x0000 Corresponding channel reactive power gain adjustment register, complement code		
CC	CARRIAGE	16	0x0000 corresponds to the channel apparent power offset adjustment register, complement code		

The adjustment formula is similar to the active power gain adjustment.

4.6.19 Reactive/apparent power bias adjustment register

Address Name	Bit Width	Default Value	Description		
CB	CITY	16	0x0000 Corresponding channel reactive power bias adjustment register, complement code		
CD	IN STOCK	16	0x0000 corresponds to the channel apparent power offset adjustment register, complement code		

The adjustment formula is similar to the active power bias adjustment.

4.6.20 CF Scaling Ratio Register

Used to control the accumulation speed of energy pulse counting. The default setting of BL0910 is 0x10.

Address Name	Bit width	Default value	Description		



BL0910 ten-phase AC power metering chip

THIS	CFDIV	12	0x010 CF Scaling ratio register
------	-------	----	---------------------------------

The frequency of energy pulse counting when CFDIV=0x10 is used as the standard frequency.

The multiples of the punch count are as follows:

CFDIV	Counting rate
0x00	0.03125
0x01	0.0625
0x02	0.125
0x04	0.25
0x08	0.5
0x10	1
0x20	2
0x40	4
0x80	8
0x100	16
0x200	32
0x400	64
0x800	256
Other values	1

4.7 Detailed description of electrical parameter registers

4.7.1 Waveform Register

Address	Name	Bit Width	Default Value	Description
1	WAVE[1]	24	0x000000	1 Channel waveform register
2	WAVE[2]	24	0x000000	2 Channel Waveform Register
3	WAVE[3]	24	0x000000	3 Channel Waveform Register
4	WAVE[4]	24	0x000000	4-channel waveform register
5	WAVE[5]	24	0x000000	5 Channel Waveform Register
6	WAVE[6]	24	0x000000	6-channel waveform register
7	WAVE[7]	24	0x000000	7 Channel waveform register
8	WAVE[8]	24	0x000000	8-channel waveform register
9	WAVE[9]	24	0x000000	9-channel waveform register
A	WAVE[10]	24	0x000000	10 Channel waveform register



B	WAVE[11] 24		0x000000 11 Channel waveform register
---	-------------	--	---------------------------------------

Waveform data of real-time sampling points, sampling clock 4MHz, 4MHz/256/50=312.5, each cycle is about 312 sampling points.

4.7.2 Effective value register

Address	Name	Bit width default	value description	
C	RMS[1]	24	0x000000	1 channel effective value register, unsigned
D	RMS[2]	24	0x000000	2-channel effective value register, unsigned
AND	RMS[3]	24	0x000000	3-channel effective value register, unsigned
F	RMS[4]	24	0x000000	4-channel effective value register, unsigned
10	RMS[5]	24	0x000000	5-channel effective value register, unsigned
11	RMS[6]	24	0x000000	6-channel effective value register, unsigned
12	RMS[7]	24	0x000000	7 Channel effective value register, unsigned
13	RMS[8]	24	0x000000	8-channel effective value register, unsigned
14	RMS[9]	24	0x000000	9-channel effective value register, unsigned
15	RMS[10]	24	0x000000	10-channel effective value register, unsigned
16	RMS[11]	24	0x000000	11 Channel effective value register, unsigned

4.7.3 Fast RMS Register

Address	Name	Bit width	default value	description
17	FAST_RMS[1]	24	0x000000	1 Channel fast (leakage current) RMS register
18	FAST_RMS[2]	24	0x000000	2 Channel fast (leakage current) RMS register
19	FAST_RMS[3]	24	0x000000	3 Channel fast (leakage current) RMS register
1A	FAST_RMS[4]	24	0x000000	4-channel fast (leakage current) RMS register
1B	FAST_RMS[5]	24	0x000000	5-channel fast (leakage current) RMS register
1C	FAST_RMS[6]	24	0x000000	6-channel fast (leakage current) RMS register
1D	FAST_RMS[7]	24	0x000000	7 Channel fast (leakage current) RMS register
1E	FAST_RMS[8]	24	0x000000	8-channel fast (leakage current) RMS register
1F	FAST_RMS[9]	24	0x000000	9-channel fast (leakage current) RMS register
20	FAST_RMS[10]	24	0x000000	10 Channel fast (leakage current) RMS register
21	FAST_RMS[11]	24	0x000000	11 Channel fast (leakage current) RMS register



Used for over-current or leakage detection, the detection period can be set by the FAST_RMS_CTRL register.

Note that the smaller the detection period, the greater the fluctuation of the register value.

[]_ - Ÿ []_ Ÿ 0.55

4.7.4 Active Power Register

Address	Name	Bit width	Default value	Description
22	WATT[1]	24	0x000000	Channel 1 active power register
23	WATT[2]	24	0x000000	Channel 2 active power register
24	WATT[3]	24	0x000000	Channel 3 active power register
25	WATT[4]	24	0x000000	Channel 4 active power register
26	WATT[5]	24	0x000000	Channel 5 active power register
27	WATT[6]	24	0x000000	Channel 6 Active Power Register
28	WATT[7]	24	0x000000	Channel 7 Active Power Register
29	WATT[8]	24	0x000000	Channel 8 Active Power Register
2A	WATT[9]	24	0x000000	Channel 9 Active Power Register
2B	WATT[10]	24	0x000000	Channel 10 Active Power Register
2C	WATT	24	0x000000	Total active power register

The active power register is a 24-bit data with a sign, two's complement. The highest bit is the sign bit, Bit[23]=1,

Indicates that the current power is negative;

$$= \frac{([])}{16}$$

4.7.5 Reactive Power Register

Address	Name	Bit Width	Default Value	Description
2D	FVAR	24	0x000000	Optional channel reactive power register (fundamental wave)

Signed 24-bit data, two's complement. Bit[23] is the sign bit, 1 means the current power is negative;

MODE[3:0] is used to select the reactive power measurement channel.



4.7.6 Apparent Power Register

Address	Name	Bit width	Default value	Description
2E	AND	24	0x000000	Optional channel apparent power register

4.7.7 Energy Pulse Count Register

Address	Name	Bit width	Default value	Description
2F	CF[1]_CNT	24	0x000000	Channel 1 active pulse count, unsigned
30	CF[2]_CNT	24	0x000000	Channel 2 active pulse count, unsigned
31	CF[3]_CNT	24	0x000000	Channel 3 active pulse count, unsigned
32	CF[4]_CNT	24	0x000000	Channel 4 active pulse count, unsigned
33	CF[5]_CNT	24	0x000000	Channel 5 active pulse count, unsigned
34	CF[6]_CNT	24	0x000000	Channel 6 active pulse count, unsigned
35	CF[7]_CNT	24	0x000000	Channel 7 active pulse count, unsigned
36	CF[8]_CNT	24	0x000000	Channel 8 active pulse count, unsigned
37	CF[9]_CNT	24	0x000000	Channel 9 active pulse count, unsigned
38	CF[10]_CNT	24	0x000000	Channel 10 active pulse count, unsigned
39	CF_CNT	24	0x000000	Total active pulse count, unsigned
3A	CFQ_CNT	24	0x000000	Optional channel reactive pulse count, unsigned
3B	CFS_CNT	24	0x000000	Optional channel apparent pulse count, unsigned

Energy pulse count is related to CFDIV register. The larger the CFDIV register setting value, the higher the pulse count.

Sooner.

MODE[15] is used to set the energy pulse counting accumulation mode: algebraic sum/absolute value mode;

The RST_ENG register is used to set whether the energy pulse counting register is cleared after reading;

$$= \frac{\ddot{y}}{16} []$$

4.7.8 Waveform Angle Register

Address	Name	Bit width	Default value	Description
3C	ANGLE[1]	16	0x0000	Channel 1 current and voltage waveform angle register
3D	ANGLE[2]	16	0x0000	Channel 2 current and voltage waveform angle register



BL0910 ten-phase AC power metering chip

3E	ANGLE[3]	16	0x0000 Channel 3 Current and voltage waveform angle register
3F	ANGLE[4]	16	0x0000 Channel 4 Current and voltage waveform angle register
40	ANGLE[5]	16	0x0000 Channel 5 current and voltage waveform angle register
41	ANGLE[6]	16	0x0000 Channel 6 Current and voltage waveform angle register
42	ANGLE[7]	16	0x0000 Channel 7 Current and voltage waveform angle register
43	ANGLE[8]	16	0x0000 Channel 8 Current and voltage waveform angle register
44	ANGLE[9]	16	0x0000 Channel 9 Current and voltage waveform angle register
45	ANGLE[10]	16	0x0000 Channel 10 Current and voltage waveform angle register

It should be noted that when the current is less than a certain value, the angle register stops working.

$$\text{Angle } (\quad) = \frac{360 \cdot \ddot{\gamma}}{[500000]} \quad [^\circ]$$

fc is the measurement frequency of the AC signal source, the default is 50Hz

4.7.9 Fast RMS Value Holding Register

Address	Name	Bit width	default value	description
46	FAST_RMS_H[1]	24	0x000000	1 Channel fast (leakage current) effective value storage register
47	FAST_RMS_H[2]	24	0x000000	2 Channel fast (leakage current) effective value storage register
48	FAST_RMS_H[3]	24	0x000000	3 Channel fast (leakage current) effective value storage register
49	FAST_RMS_H[4]	24	0x000000	4-channel fast (leakage current) effective value storage register
57	FAST_RMS_H[5]	24	0x000000	5 Channel fast (leakage current) effective value storage register
58	FAST_RMS_H[6]	24	0x000000	6 Channel fast (leakage current) effective value storage register
59	FAST_RMS_H[7]	24	0x000000	7 Channel fast (leakage current) effective value storage register
5A	FAST_RMS_H[8]	24	0x000000	8-channel fast (leakage current) effective value storage register
5B	FAST_RMS_H[9]	24	0x000000	9-channel fast (leakage current) effective value storage register
5C	FAST_RMS_H[10]	24	0x000000	10 Channel fast (leakage current) effective value storage register

Data exceeding the fast RMS threshold is stored in the corresponding I[x]_FAST_RMS_HOLD register.

It can be cleared after setting operation.

- 1) The corresponding bit of flag_ctrl2[9:0] is set to 1;
- 2) Set the corresponding bit of flag_ctrl2[9:0] to 0; clear the corresponding FAST_RMS_HOLD register value;



4.7.10 Power Factor Register

Address	Name	bit width	default value		describe
4A	PF	24	0x000000		Optional channel power factor register

The VAR_I_SEL register selects which channel is selected for reactive power and which channel is also selected for power factor.

24-bit signed number, two's complement. Bit[23] is the sign bit.

$$\text{Power Factor} = \frac{\text{Value}}{2^{23}}$$

4.7.11 Line Voltage Frequency Register

Address	Name	Bit Width	Default Value	Description	
4E	PERIOD	20	0x000000	Line voltage frequency period register	

Measure the frequency of the sine wave signal of the voltage channel.

$$\text{Line voltage frequency} = \frac{10000000}{\text{Value}} \text{ Hz}$$



5. Communication interface

Register data is sent as 3 bytes (24 bits). Register data less than 3 bytes is not used.

Fill the bits with 0 to make up 3 bytes to be sent.

Select by pin SEL, when SEL=1 it is SPI, when SEL=0 it is UART

5.1 SPI

5.1.1 Overview

Slave mode, half-duplex communication, maximum communication rate 1.5M

8-bit data transmission, MSB first, LSB last

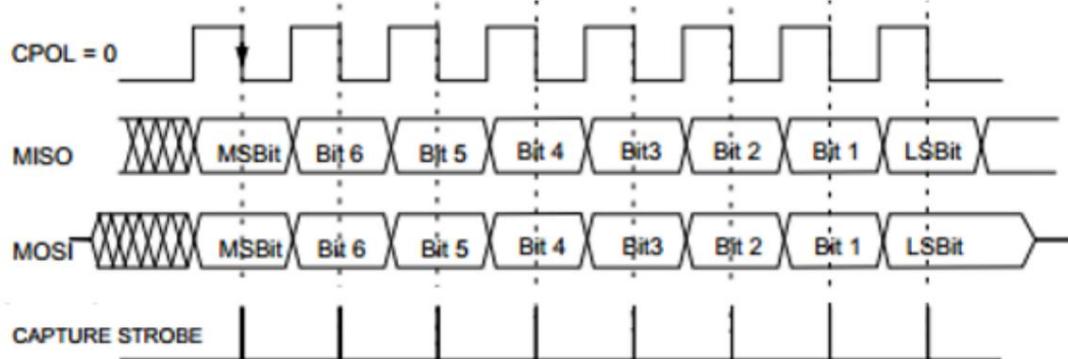
Fixed clock polarity/phase (CPOL=0, CPHA=1)

5.1.2 Working Mode

The master device works in Mode 1: CPOL=0, CPHA=1, that is, in idle state, SCLK is at low level, and the data

Data is sent on the first edge, that is, when SCLK changes from low level to high level, so data sampling

The sample is on the falling edge and the data is sent on the rising edge.



5.1.3 Frame structure

In communication mode, first send 8-bit identification byte (0x81) or (0x82), (0x82) is the read identification byte

Section, (0x81) is to write the identification byte, and then send the register address byte to determine the address of the register to be accessed

(See BL0910 register list.) The following diagrams show the data transfer sequence for read and write operations respectively.

After a frame of data is transmitted, BL0910 re-enters the communication mode. The SCLK required for each read/write operation is

The number of pulses is 48 bits.



There are two frame structures, which are described as follows:

1. Write register

Cmd: {0x81}+ Addr+Data_H+Data_M+Data_L+SUM

{0x81} is the frame identification byte for the write operation;

Addr is the internal register address of BL0910 corresponding to the write operation;

The checksum byte CHECKSUM is (({0x81}+ADDR+DATA_H+DATA_M+DATA_L) & 0xFF)

Then negate the bit.

Write operation frame 0x81	ADDR[7:0]	DATA_H[7:0] DATA_M[7:0] DATA_L[7:0]	CHECKSUM[7:0]	
----------------------------	-----------	-------------------------------------	---------------	--

2. Read register

Cmd:{0x82}+Addr

Return: Data_H+Data_M+Data_L+SUM

{0x82} is the frame identification byte for the read operation;

Addr is the internal register address of BL0910 corresponding to the read operation (0x00-0xff);

The checksum byte CHECKSUM is (({0x82}+ADDR+DATA_H+DATA_M+DATA_L) & 0xFF)

Then negate the bit.

Read command frame	0x82	ADDR[7:0]
--------------------	------	-----------

Reading Data Frame	DATA_H[7:0] DATA_M[7:0] DATA_L[7:0]	CHECKSUM[7:0]	
--------------------	-------------------------------------	---------------	--

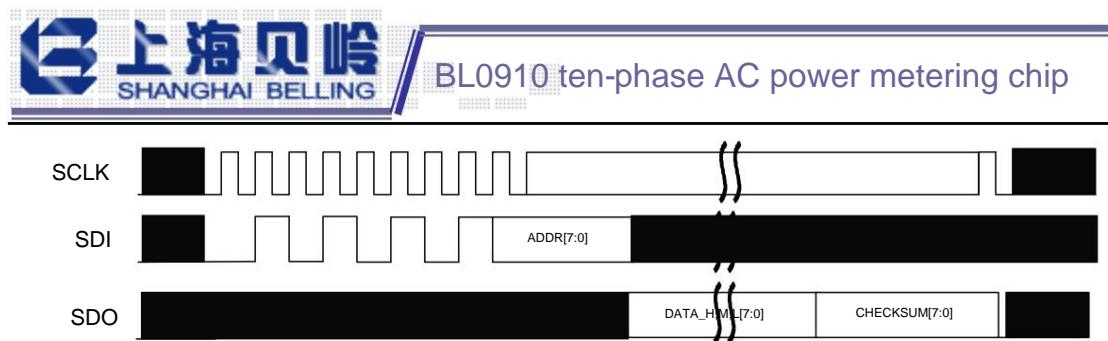
5.1.4 Read Operation Timing

During the data read operation of BL0910, at the rising edge of SCLK, BL0910 will

The data is shifted out to the DOUT logic output pin. During the next time when SCLK is 1, the DOUT value remains at

The value of DOUT remains unchanged, that is, at the next falling edge, the external device can sample the value of DOUT.

The operation is the same, the MCU must send the identification byte and address byte before the data read operation.



When BL0910 is in communication mode, the frame identification byte {0x82} indicates the next data transmission operation

The following byte is the address of the target register to be read. BL0910 is on the rising edge of SCLK

All remaining bits of the register data are shifted out on subsequent SCLK rising edges.

Therefore, on the falling edge, the external device can sample the SPI output data.

After the operation is completed, the serial interface re-enters the communication mode. At this time, the DOUT logic output is at the last SCLK

The falling edge of the signal enters the high impedance state.

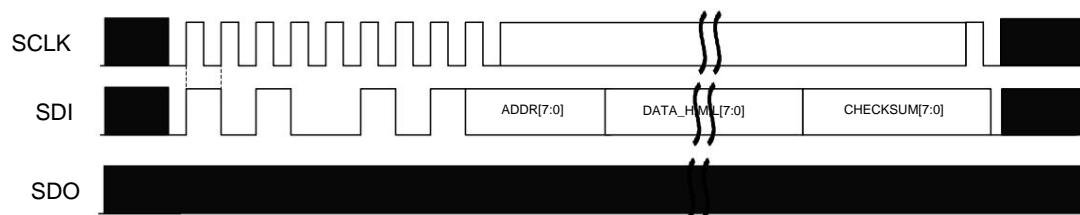
5.1.5 Write Operation Timing

The serial write sequence is as follows. The frame identification byte {0x81} indicates that the data is written during the data transmission operation.

The MCU prepares the data bits to be written into BL0910 before the falling edge of SCLK.

The falling edge of the SCLK starts shifting in the register data. All remaining bits of the register data are also shifted in on the falling edge of the SCLK.

Perform a left shift operation.



5.1.6 SPI interface fault tolerance mechanism

1) If the frame identification byte is wrong or the SUM byte is wrong, the frame data is discarded.

2) SPI module reset: send 6 bytes of 0xFF through the SPI interface.

Perform a reset;

3) _CS is pulled high to reset.



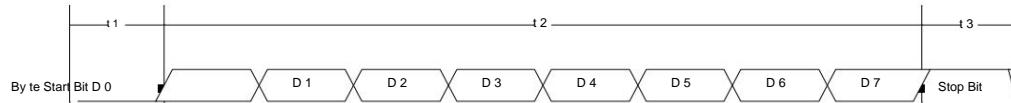
5.2 UART

5.2.1 Overview

- ÿSelect through pin UART_SEL, when SEL=1 it is SPI, when SEL=0 it is UART
- ÿCommunication baud rate is 4800bps/9600bps/19200bps/38400bps/, no parity, stop bit 1;
- ÿ In UART mode, CS and SCLK pins are used as baud rate setting pins.

Baud rate setting 4800 9600		19200	38400
CS pin 0	0	1	1
SCLK pin 0	1	0	1

5.2.2 Each byte format

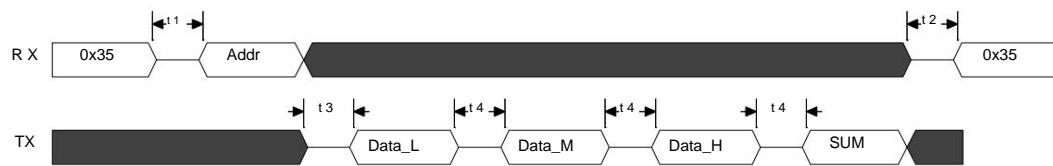


Start bit low level duration $t_1 = 208\mu s$ (4800bps);

The effective data bit duration is $t_2 = 208 \times 8 = 1664\mu s$ (4800bps);

Stop bit high level duration $t_3 = 1 \times 208\mu s$ (4800bps);

5.2.3 Reading Timing



The host UART read data timing is shown in the figure below. The host first sends the command byte (0x35), and then sends

The address byte (ADDR) to be read, followed by the data bytes sent by BL0910, and finally the checksum byte

Festival.

{0x35} is the frame identification byte for the read operation;

Addr is the internal register address of BL0910 corresponding to the read operation (0x00-0xff);

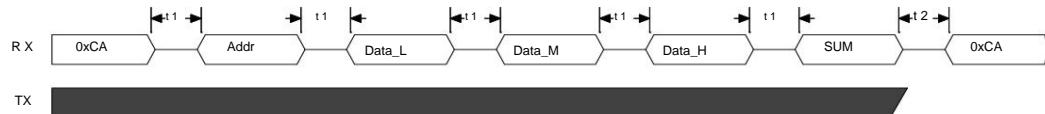
The SUM byte is (Addr+Data_L+Data_M+Data_H)&0xFF inverted;

	illustrate	Min	Type	Max	Unit	
t1	The interval time between bytes sent by MCU	0		20	mS	
t2	Frame interval time	0.5			uS	
t3:	The time from when MCU finishes sending the register address to when BL050 sends the byte during the read operation.		110		uS	



	Interval				
t4	BL0910 Interval time between sending bytes		1		bit

5.2.4 Write Timing



The host UART write data timing is shown in the figure below. The host first sends the command byte (0xCA), followed by the write address byte (ADDR) is followed by the data bytes and finally the checksum byte.

{0xCA} is the frame identification byte for the write operation;

Addr is the internal register address of BL0910 corresponding to the write operation;

The CHECKSUM byte is ((ADDR+Data_L+Data_M+Data_H) & 0xFF) and then bitwise inverted.

5.2.5 UART interface protection mechanism

BL0910's UART communication provides a timeout protection mechanism. If the interval between bytes exceeds 18.5mS, the UART interface will automatically reset.

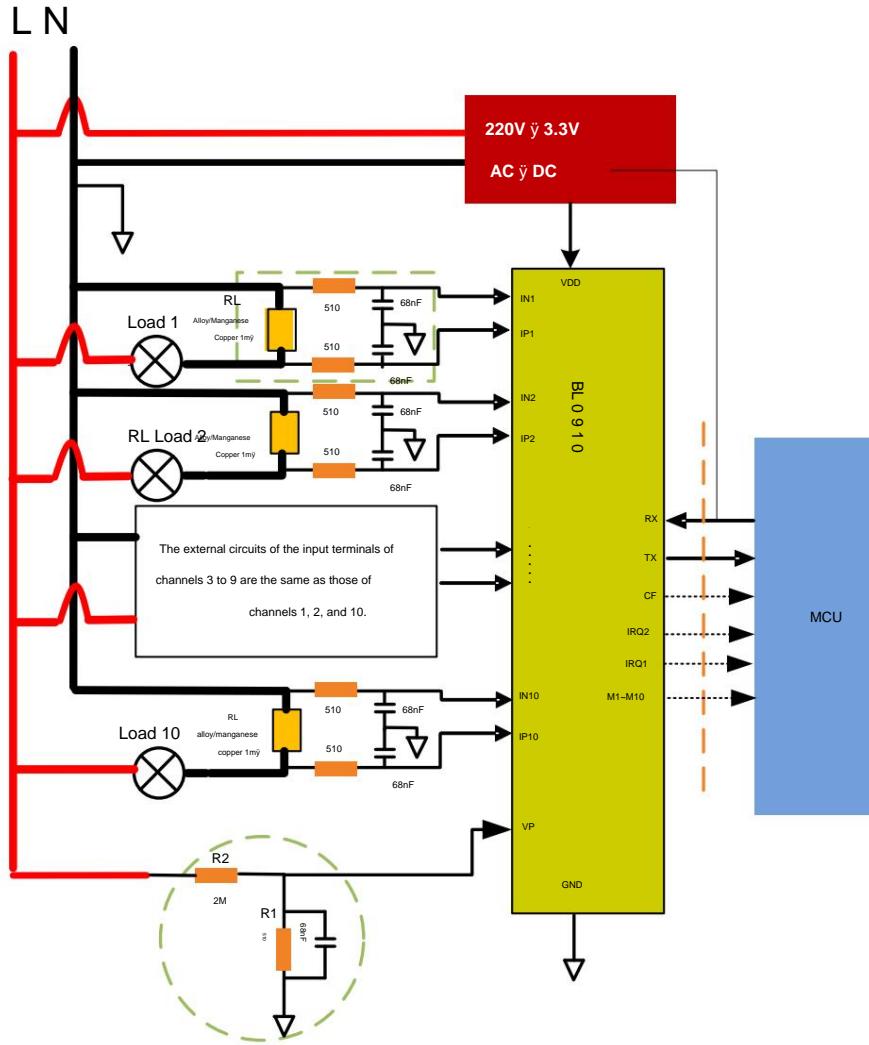
If the frame identification byte is wrong or the CHECKSUM byte is wrong, the frame data is discarded.

UART module reset: pull the RX pin low level after more than 32 bps (6.67ms at 4800bps)

High, the UART module is reset.



6. Typical application diagram



For 1U10I applications, the external circuit diagram for each current channel is the same, and the voltage channel requires signal voltage division.



BL0910 ten-phase AC power metering chip

7. Packaging information

7.1 Order Information

BL0910 LQFP48 package

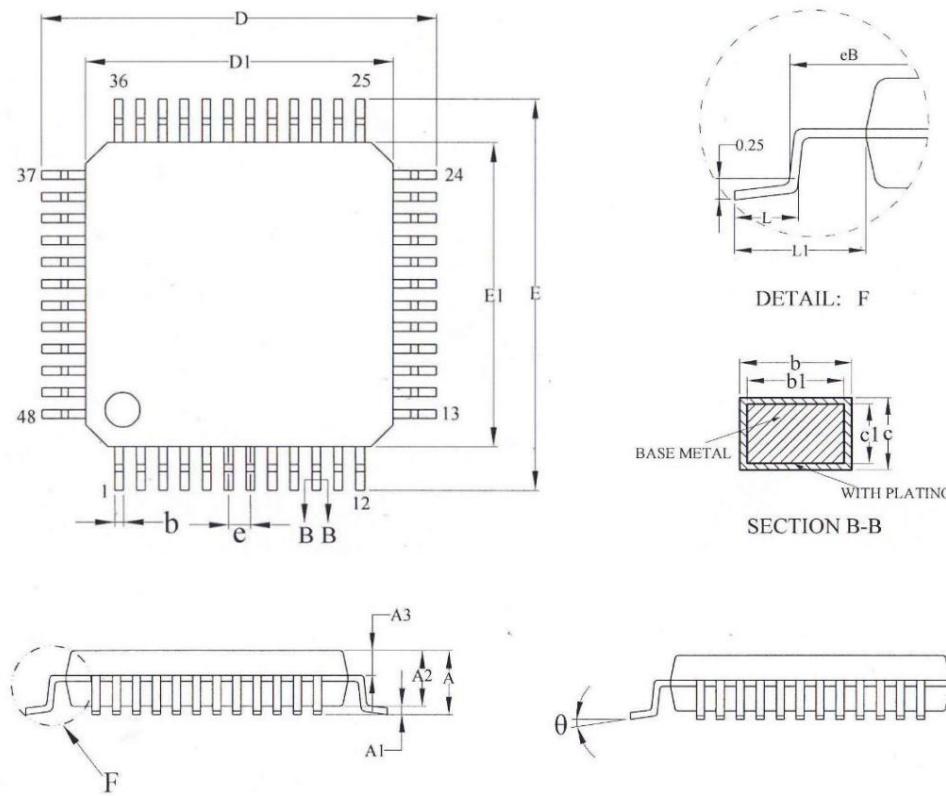
7.2 Encapsulation

Moisture sensitivity level MSL 3

Two-year warranty

Packing method: Tray

7.3 Package Appearance





BL0910 ten-phase AC power metering chip

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.50BSC		
L	0.40	—	0.65
L1	1.00REF		
θ	0	—	7°