COVER SHEET

FOR VOLUNTEER CORE COURSE APPROVAL

To Submit: To submit a proposal, please complete the following application and save it as a single PDF file that also contains your syllabus and a sample of at least one **significant assignment** for the course. Save your PDF file by the course name and category (e.g. engl101WC).

The PDF should be uploaded using this link - http://tiny.utk.edu/VolCoreProposalDrop AND emailed to gened@utk.edu.

If you are submitting a revision, please also include a brief written "Response to Reviewers" detailing how the requested revisions have been addressed. This "Response to Reviewers" should be included in your single PDF file and the file should be save by course name, category, and the revision and date (e.g. engl101WCrevision050120).

Date Submitting Proposal: October 7, 2021

Is this a revised proposal? _____ Yes __X__ No

If yes, what dates were previous versions submitted _____

Contact Information (please print or type):

Name: Garrett S. Rose

Department: Min H. Kao Department of Electrical Engineering & Computer Science

Email: garose@utk.edu

Phone: 865-974-3132

Course information:
Provide full catalog entry for the course including course subject, number, suffix (if any), course title, credit hours, course description, prerequisites/corequisites, credit restrictions, etc.

NOTES:

- *Courses in WC category **must** have the following prerequisite:*
  (RE) Prerequisite(s): English 102, 132, 290, or 298 *(plus any others for this course)*
- *Courses in AOC category:* We **strongly encourage** the oral communication general education requirement used in your program serve as a prerequisite for this course (e.g., CMST 210, 240; CE 205; Phil 244)
- Courses may apply for either OC or AOC but not both categories.

Catalog entry for course: Include an indication of any Honors version of this course or other equivalent courses (e.g., cross listed courses, S, N, or R designated courses) to be included with this proposal.

Course Number: ECE 351
Course Title: Digital Systems Design
Credit Hours: 3
Course Description: Introduction to techniques and strategies for designing digital systems using hardware description languages and industry-standard design tools. Topics include simulation and synthesis of high-level designs, finite state-machine design, digital memory systems, arithmetic circuit design, circuit delay estimation, timing, and power analysis. Laboratory and project activities include the implementation of digital systems using field-programmable gate arrays (FPGAs).

(RE) Prerequisite(s): ECE 255 with a grade of C or better.

Frequency of Course Offering (e.g., fall only, spring only): Fall only

Course Capacity per Semester *(per course & total if multiple sections):* 30

Course format (e.g., lecture, discussion, lab): Lecture by faculty, hands-on labs as homework, group project

How is this class to be staffed (i.e., instructor, GTAs, graders etc.): Instructor, 1 GTA

Please check all that apply:

	Volunteer Core areas in which this course is already approved	**Applying for inclusion in these categories for Volunteer Core**
Written Communication (WC)		
Verbal Communication (OC)		
Applied Oral Communication (AOC)		
Arts & Humanities (AH)		
Applied Arts and Humanities (AAH)		
Natural Sciences (NS) – Lab		
Natural Sciences (NS) – Non-lab		
Quantitative Reasoning (QR)		
Social Sciences (SS)		
Global Citizenship-International (GCI)		
Global Citizenship-US (GCUS)		
Engaged Inquiries (EI)		X

ENGAGED INQUIRIES

PROPOSAL FOR VOLUNTEER CORE COURSE APPROVAL

Course subject, number, suffix (S [service], R [research], N [internship]**) and title.** Include an indication of any Honors version of this course or other equivalent courses (e.g., cross listed courses, S, N, or R designated courses) to be included with this proposal.

ECE 351 – Digital Systems Design

NOTE: Courses with an S (service), R (research), or N (internship) designation will be equivalent to their base course for the Effective Communication and Expanded Perspectives Volunteer Core categories. The base course and suffix courses will be considered as different courses for Engaged Inquiries.

Engaged Inquiries

Truly well-educated citizens should be ready to lead and solve problems, building on their chosen fields of study and personal interests and strengths. Students will benefit from experiences that broaden, extend, apply, and integrate prior learning and promote effective collaboration and self-awareness.

In all Engaged Inquiries courses, students will produce significant **investigative, creative, or practical work(s) relevant to the course topic.**

Learning Areas and Learning Outcomes
In addition, El courses must demonstrate that they produce learning outcomes from **at least two** of the following Learning Areas:

1. **Applied Learning**
   In applied learning courses, students will engage in a process of proposing, implementing, and assessing the success of strategies, plans, or approaches to addressing questions in applied contexts. Courses in this domain are expected to achieve the following outcome for students:
   Students will apply skills and knowledge from the classroom in hands-on situations, real-world settings, or in independent/directed research or creative projects.

2. **Collaborative Learning**
   During the semester, students will engage in a process of sharing ideas, making useful contributions, communicating effectively, understanding their roles, planning and implementing the plan to completion. Courses in this domain are expected to achieve the following outcome for students:
   Students will demonstrate the ability to engage effectively in a group to complete an investigative, creative, or practical work.
3. **Reflective Learning**
   Students will engage in reflective activities such as journal entries, reflective response papers or creative exercises on a regular basis in this course. Students should grapple not only with the major ideas and content of the course, but with the question of what these ideas mean to them within a larger context. Courses in this domain are expected to produce the following outcome for students:
   Students will reflect on their own thinking, learning, understanding, and competencies, to draw connections between the subject matter of the course and the students' own experiences within a larger social or global context.
4. **Integrative or Multidisciplinary Learning**
   Courses that address this domain may include team-taught interdisciplinary courses; exploration into adjacent fields; courses on pre-defined interdisciplinary subjects. Courses in this domain are expected to achieve the following outcome for students:
   Students will demonstrate the ability to draw on theories, knowledge, tools, and/or methods from at least two fields of study to investigate relevant issues.

ENGAGED INQUIRIES

PROPOSAL FOR VOLUNTEER CORE COURSE APPROVAL

Answer all questions below with respect to the description and learning outcomes given above.

Questions:

I. Relevant Work: What is the "investigative, creative, or practical work(s) relevant to the course topic" that students will produce? How will students typically complete this relevant work? Demonstrate how this will account for a minimum of 35% of the course grade.

The primary practical work for this course is the final group project which itself accounts for 35% of the total grade. For the group project, student groups propose their own digital system design project, often building on examples of smaller systems explored through individual lab assignments. Individual lab and homework assignments account for 15% of the total grade for the course. For the final group projects, the total project grade (35% of course) is broken into four components: proposal (typically 5% of project grade), design review (typically 20% of project grade), final presentation (typically 30% of project grade), and final report (typically 45% of project grade).

II. EI courses must demonstrate that they produce learning outcomes from **at least two** of the following areas, as described above. **Select TWO of the FOUR** Engaged Inquiries Learning Areas:

__X__ Applied learning

__X__ Collaborative Learning

_____ Reflective Learning

_____ Integrative or Multidisciplinary Learning

For each of the TWO LEARNING AREAS indicated above, answer the following questions:

APPLIED LEARNING: Students will apply skills and knowledge from the classroom in hands-on situations, real-world settings, or in independent/directed research or creative projects.

a. How does the course meet this learning outcome?

Lectures emphasize the design and implementation of digital systems through the use of a hardware description language, such as VHDL. Throughout the semester, students leverage skills learned in the classroom through several individual lab/homework assignments where they implement small design problems on field-programmable gate arrays (FPGAs) distributed at the beginning of the semester for hands-on learning. The second half of the semester includes a group project, where small student groups work together on the implementation of digital system, again using their FPGAs. For their projects, students are required to identify an application of interest, propose how they will design a digital system for that application, and work together on the final implementation.

b. For the course itself, how are students evaluated regarding this learning outcome? (Provide information on course grading and examples of evaluation criteria, grading rubrics, scorecards, feedback given to students, or other relevant information.)

For each individual lab assignment, students submit reports detailing how they approached the problem, evidence of their solution (e.g. VHDL code snippets), simulations alongside expected results, and conclusions detailing what was learned from the assignment. They must also demonstrate their working system on the FPGA with the GTA or instructor. Group projects consist of four major graded components:

project proposal, mid-project presentation or design review, final project presentation, and final report. As part of the final project presentation, student groups will demonstrate their working design. These four items contribute to a total project grade, with the report and final presentation accounting for most weight while proposal accounts for the least.

COLLABORATIVE LEARNING: Students will demonstrate the ability to engage effectively in a group to complete an investigative, creative, or practical work

a. How does the course meet this learning outcome?

The group project requires students to work together toward a proposed digital system application that they then implement as a team. Student groups must also present their project work to the class twice during the semester: once as part of a mid-project design review and then for the final project presentation where they demonstrate their working system. As part of the design effort, students are encouraged to take a divide and conquer approach, where the system is partitioned as evenly as possible for each team member to focus on specific design elements. They must then work as a team integrating these design elements into the full system implementation. Finally, students work as a team to write a project report detailing their application, design decisions made along the way, and their final results.

b. For the course itself, how are students evaluated regarding this learning outcome? (Provide information on course grading and examples of evaluation criteria, grading rubrics, scorecards, feedback given to students, **peer-assessment, and/or** other relevant information.) **Note that this kind of feedback (not necessarily grading) on collaborative learning is different than simply grading the collaborative project or assignment.**

As part of their project proposals, students describe how they plan on partitioning their designs and how they will collaborate on the implementation of their system. This early planning is expected to evolve and is considered when students present their mid-project design reviews and again when they present their final projects. For both presentations, the evolution of design strategies are presented, including how group members work together to accomplish specific design goals. Further detail of design partitioning and final system integration, including how team members interact, is provided in the final report.

REFLECTIVE LEARNING: Students will reflect on their own thinking, learning, understanding, and competencies, to draw connections between the subject matter of the course and the students' own experiences within a larger social or global context.

a. How does the course meet this learning outcome?

b. For the course itself, how are students evaluated regarding this learning outcome? (Provide information on course grading and examples of evaluation criteria, grading rubrics, scorecards, feedback given to students, or other relevant information.)

INTEGRATIVE OR MULTIDISCIPLINARY LEARNING: Students will demonstrate the ability to draw on theories, knowledge, tools, and/or methods from at least two fields of study to investigate relevant issues.
a. How does the course meet this learning outcome?
b. For the course itself, how are students evaluated regarding this learning outcome? (Provide information on course grading and examples of evaluation criteria, grading rubrics, scorecards, feedback given to students, or other relevant information.)

III. What process is used to monitor/oversee that each section of this course is meeting the learning outcomes if multiple sections are taught to ensure consistency semester to semester?

IV. Course Assessment

Provide a short description of how this course will be assessed for the Volunteer Core outcomes. According to the revised General Education guidelines, all approved Volunteer Core courses must be assessed according to the guidelines and timeline set by the General Education Committee. For the review, this course will need to provide quantifiable data and results regarding how successful the students were in mastering the learning outcomes chosen above. With that in mind, please be as specific as possible in your plan to measure both of the chosen learning outcomes*. (You can refer to the Volunteer Core assessment document and rubrics on the Volunteer Core website.)

Assessment plans for EI courses should feature direct assessment of student learning using the IE Course Rubric to answer the following:

First Learning Area: (please check one)

__X__ Applied learning

_____ Collaborative Learning

_____ Reflective Learning

_____ Integrative or Multidisciplinary Learning

a. Provide a description of the (most likely one example of) student work that will be used to assess the learning outcome required by the EI designation in this course.

Students will provide reports for their lab assignments that detail how they considered a specific digital design problem and implemented a solution using a hardware description language, such as VHDL. The report will also provide evidence of their work in implementing their design on an FPGA. It is worth noting, that this course must also satisfy ABET outcomes for computer engineering. Thus, the EECS assessment committee regularly collects assessment data to ensure that the course is providing for the necessary learning outcomes for ABET. A process similar to the collection of data for ABET will be used to collect data for the EI learning outcomes. When the course is complete, samples of lab and project reports will be used for assessment by the EECS assessment committee.

b. Provide a description of how you will obtain the sample of student work.

Students are required to submit lab and project reports on specified due dates throughout the semester. These are required assignments that will be graded and returned to the students with constructive feedback from the instructor.

Second Learning Area: (please check one)

_____ Applied learning

__X__ Collaborative Learning

_____ Reflective Learning

_____ Integrative or Multidisciplinary Learning

a. Provide a description of the (most likely one example of) student work that will be used to assess the learning outcome required by the EI designation in this course.

Final project reports will include a methodology section that details how the project groups complete the design as a team. The final project report itself is collected for final grading and assessment. For assessment purposes for this particular outcome, the sections detailing design methodology and student engagement will be specifically assessed by the instructor in consultation with the EECS assessment committee. It is worth noting, that this course must also satisfy ABET outcomes for computer engineering. Thus, the EECS assessment committee regularly collects assessment data to ensure that the course is providing for the necessary learning outcomes for ABET. A process similar to the collection of data for ABET will be used to collect data for the EI learning outcomes. When the course is complete, samples of lab and project reports will be used for assessment by the EECS assessment committee.

b. Provide a description of how you will obtain the sample of student work.

Students are required to submit lab and project reports on specified due dates throughout the semester. These are required assignments that will be graded and returned to the students with constructive feedback from the instructor.

*****The answer to the assessment question should include:

1. A **description of the student work** that will be used to assess each learning objective. The student work may be an exam, an essay, a lab report, a reaction paper, a set of homework problems, a short-answer response provided on a mid-term exam, selected multiple-choice questions from a quiz, etc. More than one learning outcome can be assessed by the same student work. The assignment/ exam/paper/etc. does not have to be made specifically for the purpose of this assessment. In fact, it is *preferable* that the student work be an assignment or test that is a normal part of the course.

2. **The sampling method to be used for the assessment**. If it is expected that there will be multiple sections of the course, you may choose to sample 20% of the sections of the course or 20% of the students in each section. This 20% should be at least 50 students. If the course is expected to have one section or a total of 50 students or less, you should collect work from all students.

ADDITIONAL MATERIALS

Please include:

- a representative **course syllabus** (including a clear indication that the course is a Volunteer Core course and course objectives that include the Volunteer Core student learning outcomes) and
- a sample of at least one **significant assignment** for the course.

Department of Electrical Engineering and Computer Science, The University of Tennessee
ECE 351 – Digital System Design, Fall 202X

Digital systems have become ubiquitous in nature and even appear in critical applications ranging from military defense systems to medical devices. Thus, it is necessary for digital system designers to design systems that are reliable in their functionality and also efficient in their performance.

Introduction to techniques and strategies for designing digital systems using hardware description languages and industry-standard design tools. Topics include simulation and synthesis of high-level designs, finite state-machine design, digital memory systems, arithmetic circuit design, circuit delay estimation, timing, and power analysis. Laboratory and project activities include the implementation of digital systems using field-programmable gate arrays (FPGAs).

Teaching Staff
Professor: Garrett S. Rose: garose@utk.edu, 865-974-3132, **MK319**
GTA: TBD

Schedule
Lecture: MWF 9:15 am – 10:05 am **MK405**
Labs: FPGA configuration & verification during TA office hours in **MK224**

Office Hours
Professor Rose: Tuesday and Thursday 11:00 am – 12:30 pm
GTA: TBD

Required Text

Ricardo Jackson, *Effective Coding with VHDL: Principles and Best Practices*, The MIT Press, 2016.

Additional Reading (not required)

Volnei A. Pedroni, *Circuit Design and Simulation with VHDL*, Second Edition, The MIT Press, 2010.

Peter J. Ashenden, *The Designer's Guide to VHDL*, 3rd edition, Morgan Kaufmann, 2008.

David Money Harris & Sarah L. Harris, *Digital Design and Computer Architectures*, 2nd Edition, Morgan Kaufmann, 2013.

Grading

Labs/Homework:	15%
Quizzes/Participation:	10%
Mid-Term:	20%
Final Project:	35%
Final Exam:	20%

Assignment Policy
Lab assignments and homework are individual assignments to be completed on your own time – TA and Professor will be available to help. Completed lab assignments must be verified and reports signed by the TA *before* the due date. All homework and lab assignments are to be handed in at beginning of class on due date unless told otherwise. ***If there is a reasonable excuse, you will get one week after original due date to submit only if you notify the professor first***. One week after due date solutions will be posted on Canvas and no excuses will be accepted for late assignments. In *extreme* situations, you may be accommodated by other substitute assignments (alternate homework, extra credit, etc.).

Academic Integrity
All homework and lab assignments to be turned in for credit must be each student's own work. Students can discuss problems and general ideas but any code or other deliverable must be written independently by each student.

Pop quizzes and in-class activities may be given from time to time during the class lecture period. Some in-class activities may allow for or even require collaboration with other students. Quizzes and in-class activities will be graded as part of "Quizzes/Participation." ***Quizzes and both exams will be closed-book with no discussion allowed***. Any violations can result in a zero on the given quiz or exam.

Electronic Devices
Laptops, smartphones, tablets and other electronic devices are allowed during lectures in as much as such devices are used with discretion and proper respect is given to the professor and other students. If the use of any electronic device is found to be a distraction then said device must be turned off and put away immediately.

A major component of this course consists of learning to code with VHDL. As such, some in-class activities may benefit from the use of a laptop or tablet. However, no activity will be given which requires the use of such devices.

Project Expectations
A major component of this course is a group project where students will implement a design of their choice. As part of the learning experience, students will discuss ideas, devise a plan, and divide up the work as a team consisting of 2-3 members. Toward the end of class, project presentations will be delivered by each team. It is recommended that students begin forming teams and considering potential projects as soon as possible.

Disability Statement
Any student requiring an accommodation based on the impact of a disability should contact the Office of Disability Services at 865-974-6087 to coordinate reasonable accommodations for documented disabilities.

Prerequisites
ECE 255 with a grade of C or better.

Topics Covered
- Introduction: Motivation for Digital Systems
- Review of Digital Logic Concepts: Combinational Logic
- Review of Digital Logic Concepts: Sequential Logic
- Introduction to Top-Down Design Approach with VHDL
- VHDL Behavioral Design
- VHDL Structural Design
- Combinational Design with VHDL
- Sequential Design with VHDL
- Synchronous and Asynchronous Design
- CAD Design Software and Emulation Testbeds
- Testbench Development
- FPGA Timing Analysis and FPGA Power Analysis
- Optimizing FPGA-based Designs
- Applications of FPGAs in Practical Digital Systems

ECE351 Digital Systems Design, Spring 202X
Lab 3

Arithmetic Logic Unit (ALU) Design

In this lab you will design and implement an arithmetic logic unit using the BASYS3 FPGA board. An ALU is controlled by an operational code (op code) used to select one of several possible arithmetic or logical operations for computation. Your ALU will operate on at most 2 8-bit, signed integer inputs which must be stored in registers A0 and B0. *The two registers are to be explicitly implemented in your VHDL code*. Single input operations (e.g. shift) will operate on the contents of register A0, returning the result to register A0.

Operations to be implemented:

- Addition: A0 ← A0 + B0
- Subtraction: A0 ← A0 – B0
- Multiplication: A0,B0 ← A0 * B0
- Logical AND: A0 ← A0 and B0
- Logical OR: A0 ← A0 or B0
- Logical XOR: A0 ← A0 xor B0
- Logical NOT: A0 ← ~A0
- Logical Shift Left: A0 ← A0 lsl B0 ; B0 stores number of positions to shift
- Logical Shift Right: A0 ← A0 lsr B0 ; B0 stores number of positions to shift
- Arithmetic Shift Right: A0 ← A0 lsr B0 ; B0 stores number of positions to shift
- Rotate Shift Left: A0 ← A0 rsl B0 ; B0 stores number of positions to shift
- Rotate Shift Right: A0 ← A0 rsr B0 ; B0 stores number of positions to shift

NOTE: For multiplication, A0,B0 acts as single 16-bit register with A0 storing the most significant digit (bits 15 – 8) of the result and B0 the lower digit.

In addition to the ALU operations above, include the following operations for loading and reading the registers:

- Load Register A0: A0 ← (contents of switches 7 – 0)
- Load Register B0: B0 ← (contents of switches 7 – 0)
- Read Register A0: (lower 2 7-seg displays) ← A0
- Read Register B0: (lower 2 7-seg displays) ← B0
- Read Register A0,B0: (upper 2 7-seg displays) ← A0, (lower 2 7-seg displays) ← B0

NOTE: Since the numbers being read are signed, use LED15 to display the sign bits for the three read operations. The MSB of (switch 7) inputs will be the sign bits for load operations.

Task 1*:** Use operators and type cast functions available in the NUMERIC_STD package to implement the ALU operations. ***After synthesis, save the schematic view of the ALU and the resulting multiplier as an image to be included in your report. Be sure to simulate each operation using 4 test cases each. Simulation results are also to be included in your report. (60%)
***Task 2*:** Repeat the same work as in Task1 but now use structural VHDL to implement the addition and subtraction logic as a structured 8-bit carry-ripple adder. Simulate using same 4 test cases as in Task 1 and compare results. (40%)

NOTE: You should develop sub-entities for register, XOR, AND, OR, NOT, and FULL_ADD (full adder operation).

Be sure to include clear block diagram describing your resulting ALU design. Also document design decisions, including selection logic used and details for the chosen op codes used to select the different operations.

NOTE (both tasks): you will likely want to use a button (BTNC) to capture 8-bit inputs from switches 7 – 0. The other switches (15 – 8) should be used as needed to implement the op code inputs to control your ALU. How op codes are assigned is entirely up to the designer.