Fully-Addressable Varactor-Based Reflecting Metasurface with Dual-Linear Polarisation for Low Power Reconfigurable Intelligent Surfaces

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***Abstract*—This work explores the performance of a 1-bit dual-linear polarised varactor-based metasurface design at sub-6 GHz. A modified particle swarm optimisation algorithm was utilised to determine the element geometry resulting in minimum reflection loss and phase error, and maximum cross-polarisation isolation. Unit cells may be individually addressed and with independent polarisation control over 3.3 to 3.7 GHz. A prototype consisting of an arrangement 48 x 16 unit cells has been fabricated for deployment in a reconfigurable intelligent surface-aided wireless communication channel sounding campaign.**

***Index Terms*—metasurfaces, varactors, reconfigurable intelligent surface, intelligent reflecting surface.**

I. Introduction

Future wireless communication systems may not only compensate for the highly variable wireless channel at the transmitter and receiver, but also within the wireless propagation environment itself. This involves transforming an uncontrollable wireless channel into a smart radio environment [1]. This idea has seen significant recent research interest and devices known as reconfigurable intelligent surfaces (RISs) may facilitate this transformation [2][3][4]. RISs are essentially reflecting-type metasurfaces whose scattering properties can be programmed to meet a desired communication or sensing goal.

Dual-linear polarised RISs enable manipulation of both transverse components of incident electromagnetic waves. This is important since base stations in mobile networks typically operate with dual-polarised antenna arrays in order to mitigate random scattering in the radio environment and cater for the unknown orientation of mobile handsets. Several recent works have introduced dual-polarised programmable metasurfaces [5][6][7]. Positive-intrinsic-negative (PIN) diode-based RIS designs are popular due to their simple, scalable biasing mechanism, at the expense of a higher power consumption when compared to varactor-based designs [8]. Varactor-based programmable metasurfaces do not suffer the requirement of a constant bias current to operate. Additionally, varactor-based designs enjoy the flexibility of a continuously tunable surface reactance. This is at the expense of less conventional bias voltage requirements that are not typically met by off-the-shelf digital components. Zhang et al. recently introduced a dual-polarised varactor-based reflecting metasurface operating at 6 GHz [6]. The design utilised a rotationally-symmetric unit cell topology, with 4 varactor diodes per element. Metasurface-based XOR logic gate and dual-beam scanning applications were successfully demonstrated. While metasurface designs such as [6] and [7] utilise 4 varactor diodes per unit cell to maintain symmetry and keep cross-polarisation low, Ke et al. introduced a dual-polarised varactor-based programmable metasurface operating at 2.6 GHz and utilising the minimal 2 varactors per unit cell [5]. This reduces fabrication cost due to halving the tuning component count, as well as aiding scalability of the design to high frequencies with associated smaller unit cell dimensions. However, compared to [6], the unit cell addressability in their implementation is limited to a column-wise scheme. The authors introduced a time-domain digital coding scheme for linear and non-linear polarisation synthesis, demonstrating arbitrary polarisation conversion at fundamental and harmonic frequencies. In this work, we introduce a varactor-based reflecting metasurface with dual-linear polarisation operating within the 5G sub-6 GHz band. The design employs the minimal 2 tuning components per element. All elements are individually programmable, with separate control over both linear polarisations.

II. Metasurface Design

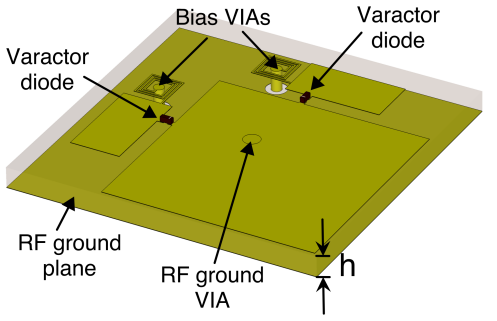
A. Unit Cell Design

The unit cell is composed of a single square microstrip patch and two parasitic rectangular patches positioned with mirror symmetry about the diagonal, as shown in Fig. 1. These are etched onto an F4B220 substrate with $\epsilon_r = 2.2$ and $tan\delta = 0.001$ backed by a copper ground plane. A VIA connects the square patch to the ground plane. Two Skyworks SMV1408 varactor diodes, one for each linear polarisation, connect the parasitic patches to the square patch and provide a voltage-tunable series capacitance. These are arranged such that the cathode is connected to the square patch. In order to tune the varactor diodes, a fixed high voltage is applied to the square patch through the ground plane and a lower switchable voltage is applied to the parasitic patches. The switchable voltage connections are isolated from the radio frequency (RF)

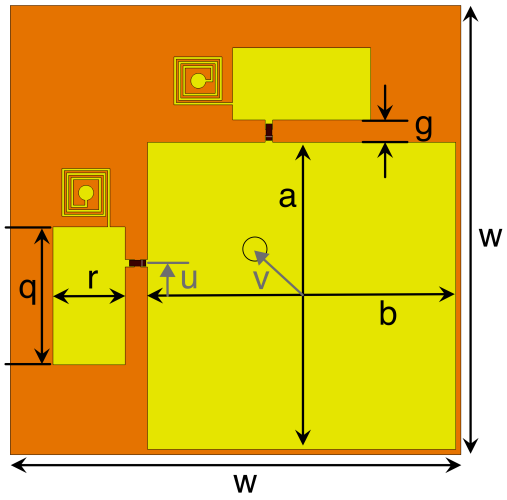
TABLE I
UNIT CELL DIMENSIONS

Parameter	Length (mm)	Parameter	Length (mm)
w	30	h	2
g	1.5	a, b	20.5, 20.5
q, r	9.2, 4.8	u, v	1.9, 2.8

portion of the device through planar spiral inductors tuned and positioned to act as RF chokes at 3.5 GHz. Dimensions are provided in Table I. This asymmetric design enables use of the minimum number of two discrete components per unit cell without introducing disruptively large linear-linear polarisation conversion.



(a)



(b)

Fig. 1. Perspective view (a) and top view (b) of the unit cell design. Dimensions are given in Table I. A square microstrip patch printed on an F4B220 dielectric substrate is connected to two parasitic patches through varactor diodes. The square patch is set to the upper varactor voltage whilst the respective parasitic patches are driven by a switchable voltage through the bias VIAs, providing a 1-bit response at both linear polarisations.

The unit cell geometry was optimised utilising a particle swarm optimisation algorithm similar to that employed in [9]. The parameters subject to optimisation were the square patch width, a, parasitic patch respective lengths and widths, q and r, the parasitic patch spacing, g, the unit cell periodicity, w,

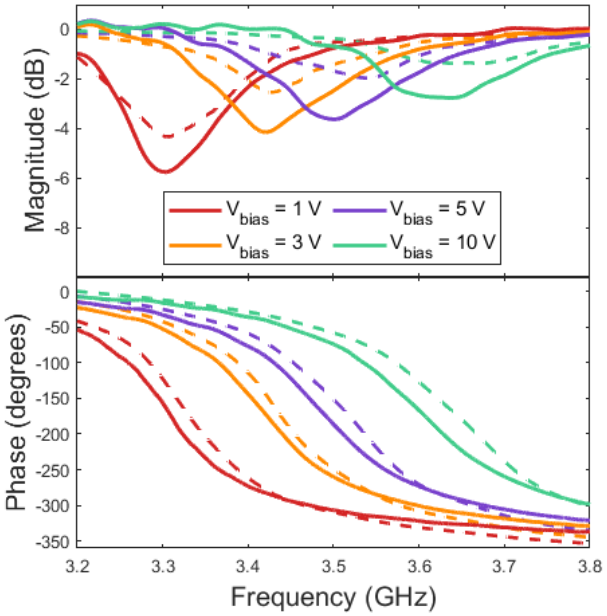


Fig. 2. Global reflection response for co-polar varactor voltages of $V_1 = 1, 3, 5$, and 10 V, with the cross-polar varactors held at $V_2 = 0$ V. Full-wave simulation results are given by the dashed curves and measured results given by the solid curves.

and the offsets, u and v. The substrate thickness, h, was kept at 2 mm to reduce fabrication costs. The unit cell was simulated in CST Studio Suite with the frequency domain solver and periodic boundary conditions. Two orthogonal Floquet ports were employed broadside to the surface to capture the co- and cross-polar reflection performance. The varactor diodes were simulated as discrete ports and the bias VIAs and inductors were omitted to reduce complexity during optimisation.

During each iteration, 80 particles were simulated, with the initial population normally distributed throughout the search space. Each particle was scored based on it's best possible 1-bit performance given the set of available capacitances from the varactor diodes. The cost function was defined as:

$$f_{cost} = \alpha_1(1 - |S_{11}(C_1, C_2)|) + \alpha_2|S_{21}(C_1, C_2)| + \alpha_3\varepsilon(C_1, C_2) \quad (1)$$

Where α_1 to α_3 are the respective weighting coefficients, S_{11} is the co-polar reflection coefficient, S_{21} is the cross-polar transmission coefficient, and ε is the phase error in radians. C_1 and C_2 are the two capacitance values selected as follows. After a given particle (i.e., set of parameters) is simulated, post-processing is performed in which the discrete port is replaced by an equivalent load of that of the SMV1408 varactor. The load is simulated at voltage levels 0 - 20 V at 0.5 V intervals. The pair of voltage levels resulting in minimising (1) determine the capacitances C_1 and C_2 used scoring for that particle. This flexibility in the selection of bias voltage

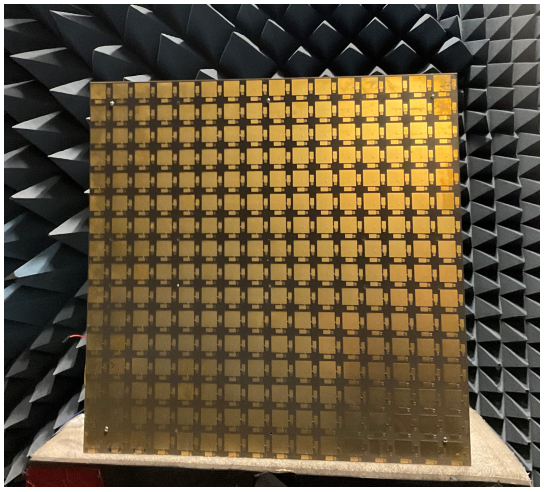


Fig. 3. Front view of one of the fabricated metasurface tiles with an arrangement of 16×16 unit cells. Control circuitry is arranged on the back side of the metasurface.

levels is due to the control circuit topology employed here, as detailed in the next section. The weighting coefficients, α_1, α_2, and α_3 were set to 0.2, 0.1, and 5, respectively.

The resulting simulated co-polar reflection performance is shown by the dashed curves in Fig. 2, subject to vertically-polarised plane wave incidence. These were generated by utilising the S2P data available for the SMV1408 varactors at the respective voltages. The reverse-bias voltage for the horizontally-arranged varactor is held fixed at 0 V, whilst the voltage levels for the vertically arranged varactor are set to 1, 3, 5, and 10 V. At 3.5 GHz there is a 248° phase variation between 1 and 10 V, which is more than sufficient for 1-bit operation. The simulated magnitude remains above approximately 1.4 dB at the center frequency, with the losses attributed mostly to the forward resistance of the varactor diodes.

B. Control Circuitry

While previous varactor-based reconfigurable metasurface designs limit the biasing control to groupings of unit cells [6][5], this design offers two-level voltage control to each individual varactor diode. The control circuit topology is centred around high voltage shift registers with 32 push-pull outputs each. Each shift register can provide 1-bit control of the varactor diodes of 16 unit cells, providing a switchable voltage level determined by the logic voltage V_{DD}. With a DC voltage $V_S \geq V_{DD}$ applied to the square patches, the reverse bias voltages for the 0 and 1 logic states become V_S and $V_S - V_{DD}$, respectively. Metasurface tiles of dimensions 480 mm $\times$ 480 mm were fabricated, each consisting of an arrangement of 16×16 unit cells, one of which is shown in Fig. 3. Each metasurface tile contains 16 high voltage shift registers, each with 32 output pins, providing bias signals to 512 varactors. For a set configuration, the control circuitry consumes a quiescent power of approximately 60 mW due largely to the minimum quiescent current of the shift registers, with the varactor diodes drawing negligible current. By comparison, driving a similar number of PIN diodes with a typical 1 mA bias current with off-the-shelf logic circuitry would result in an average power consumption in the region of 1 W. The metasurface is connected to a Raspberry Pi single-board computer, providing digital signals to program the shift registers and a WiFi interface for remote control.

III. Measurements

The measurement setup is depicted in Fig. 4. Two standard gain horn antennas and a metasurface tile were placed in an anechoic chamber at a distance of 1.5 m from the chamber floor. The chamber has dimensions $8m \times 4m \times 4m$. The horn antennas were positioned 6 m from the center of the tile, with an inter-antenna spacing of 0.5 m. The antennas were connected by 5m coaxial cables to an Agilent 8720ET vector network analyser (VNA). Initially, both antennas were arranged in a vertical polarisation and the tile was replaced by a copper plate of similar dimensions. The system was calibrated in the S21 setting by normalising the transmission via the copper plate. This was followed by measuring the S21 to ascertain the co-polar metasurface reflection for the voltage range 0-18 V. The cross-polar performance was then ascertained by a similar procedure, with one of the horn antennas oriented in a horizontal polarisation. The co-polar reflection behaviour versus bias voltage for several frequency points is plotted in Fig. 5. It can be seen that a 1-bit response can be achieved at all noted frequency points from 3.3 to 3.7 GHz, although the associated magnitude can vary as much as 6.5 dB. To broaden the bandwidth over which the phase differences between two fixed voltage levels remains within $180 \pm 20^\circ$, bias voltage levels which result in a peak phase difference of 200° at the center frequency of 3.5 GHz have been found as 2.5 V and 10 V. This is highlighted by the vertical dashed lines. The associated co-polar magnitudes, phases (solid curves), phase difference (dashed curves), and cross-polar magnitudes (dotted curves) have been plotted in Fig. 6. With these settings, the metasurface can be seen to exhibit a 1-bit bandwidth of approximately 160 MHz, a cross-polar isolation of 20 dB, and a maximum reflection loss of 4.2 dB at the lower band edge.

IV. Conclusion

This work has introduced a dual-polarised reflecting metasurface based on binary control of varactor diodes for low power RIS applications. The metasurface offers independent control of horizontally- and vertically-polarised wave components. The element geometry has been optimised through a modified particle swarm optimisation algorithm to minimise reflection loss and phase error, and maximise cross-polarisation isolation. The fabricated metasurface is capable of binary control of each constituent tunable component and the center operating frequency can be set through global tuning of two voltage levels. The global reflection performance of a 16×16 metasurface tile has been investigated, with measurements in agreement with full-wave simulations utilising manufacturer

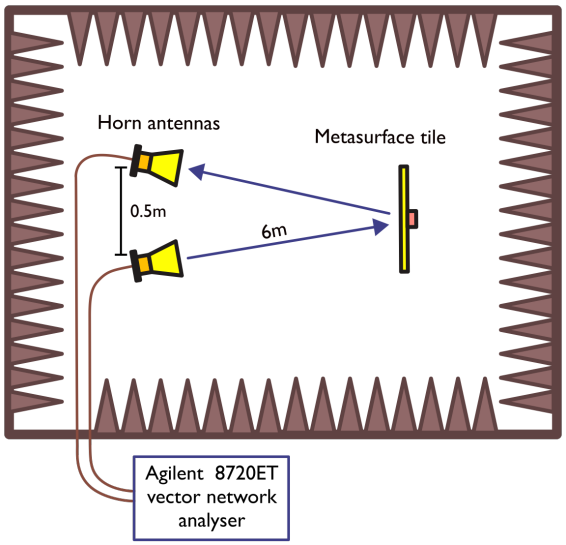


Fig. 4. Measurement setup for ascertaining global reflection coefficients. The metasurface tile sample and two standard gain horn antennas were placed in an $8m \times 4m \times 4m$ anechoic chamber. The horn antennas were directed at the prototype at a distance of 6 m, with 0.5 m spacing between the antennas. S21 measurements were ascertained with an Agilent 8720ET vector network analyser after calibration by replacing the metasurface tile with a copper plate of similar dimensions.

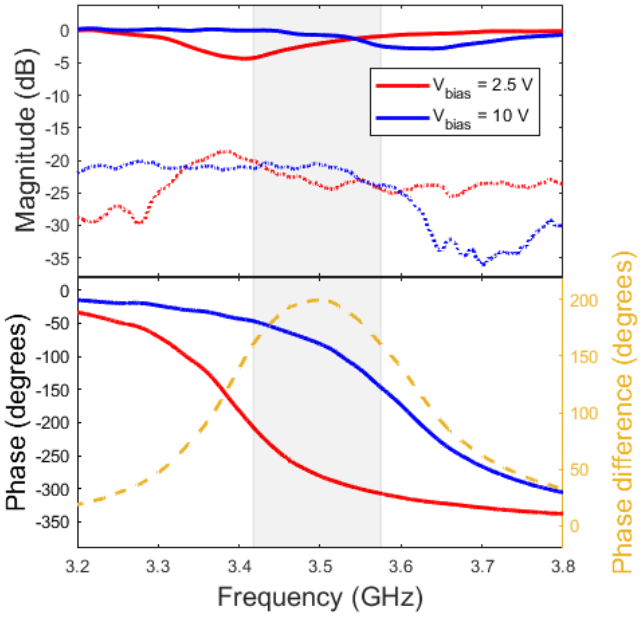


Fig. 6. Measured reflection response for metasurface biased for 1-bit operation for 3.42 to 3.58 GHz. These values correspond to $V_{DD} = 7.5V$ and $V_S = 10V$, resulting in reverse-bias voltages of $2.5V$ and $10V$ for the 1 and 0 states, respectively. The co- and cross-polar reflection magnitude is given by the solid and dotted curves in the top plot, respectively. The phase difference between the two bias states is highlighted as the dashed curve in the bottom plot. The operating region, where $\Delta\phi = 180 \pm 20°$, is highlighted by the shaded region.

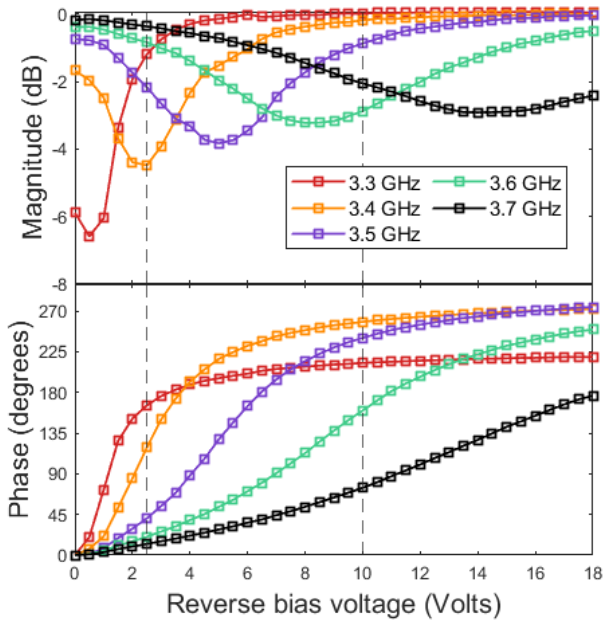


Fig. 5. Measured reflection phase and magnitude versus voltage for 3.3, 3.4, 3.5, 3.6, and 3.7 GHz. Vertical dashed lines highlight the operating points, 2.5 V and 10 V, utilised for 1-bit operation centered at 3.5 GHz, as detailed in Fig. 6.

S2P data. Three metasurface tiles have been fabricated for deployment in a channel sounding campaign of RIS-aided wireless communication networks in order to ascertain the suitability of RISs for wireless coverage enhancement. This work will be detailed in an extension of this paper.

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