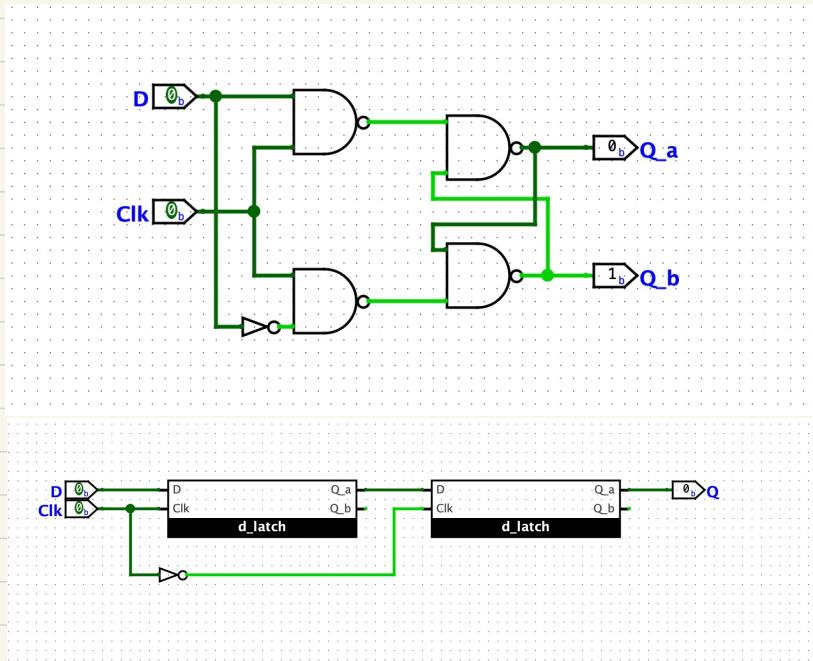


CSC LAB 4

Chenyue Li 1004767558

Part I



3. We should not be the first test when $\text{Clk} = 0$.
Since the state of Q could be either 0 or 1.

Part II

2. a) Oscillation apparent

It forms a infinite loop which the output will infinite operate function.

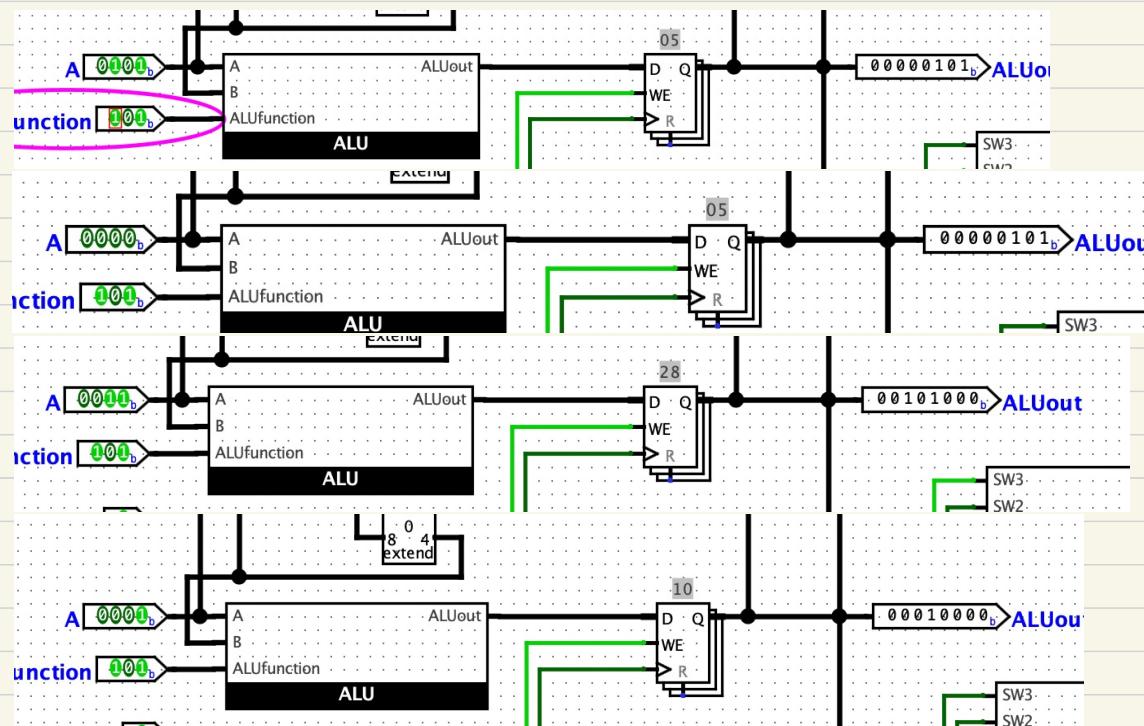
b) 21

	A	ALUout
Function 0:	0000	0000 0001
	0010	0000 0011
	0010	0000 0011
Function 1/2:	0000	0000 0000
	0001	0000 0001
	0010	0000 0011
	0100	0000 0111
	0111	0000 1110

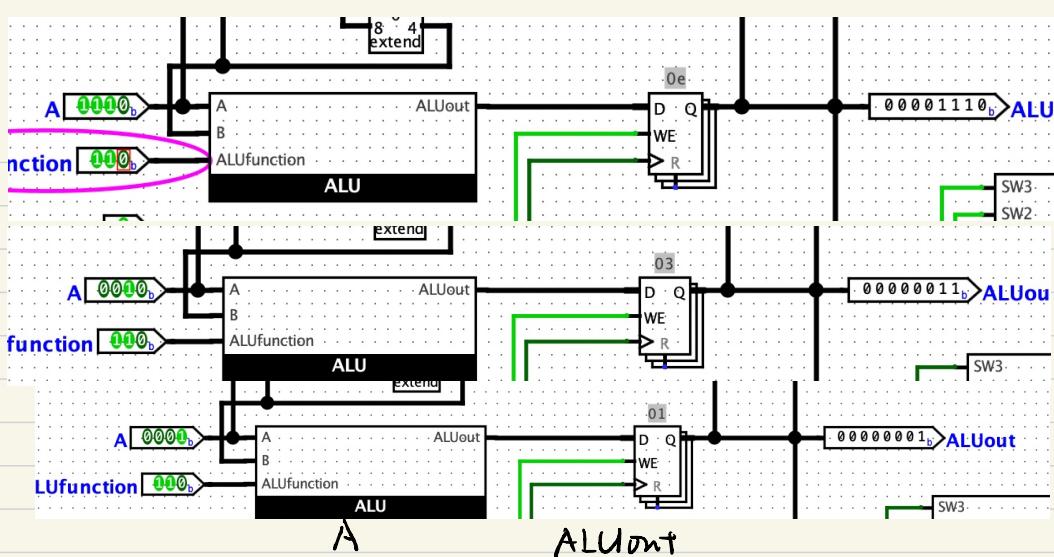
A	ALUout
Function 3: 0000	0000 0000
1010	1010 1010
1010	1010 0000
1111	1111 1111
1111	1111 0000

A	ALUout
Function 4: 0 0 0 0	0000 0000
0 0 0 1	0 0 0 0 001
0 0 0 0	0 0 0 0 001
1 1 1 1	0 0 0 0 001

A	ALUout
Function 5: set B to	00000101
0 0 0 0	0 0 0 0 0101
0 0 1 1	0 0 1 0 1000
0 0 0 1	0 0 0 1 0000

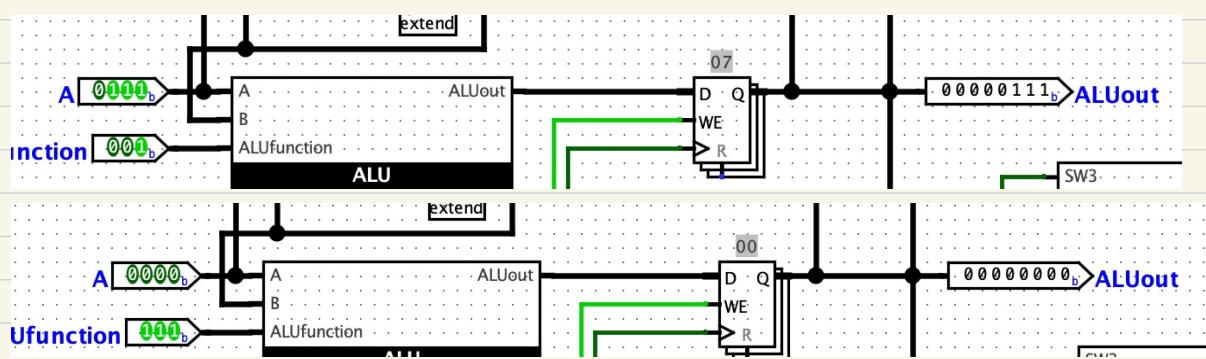
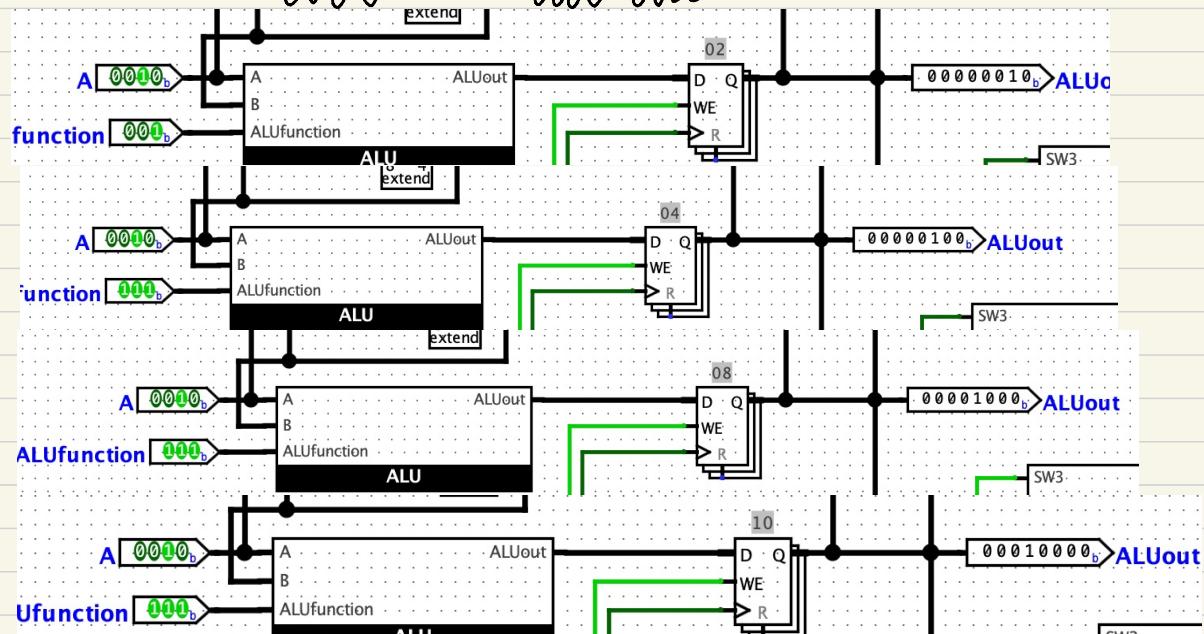


A	ALUout
Function 6: set B to	00001110
0010	0000 0011
0001	0000 0001



Function 7 :

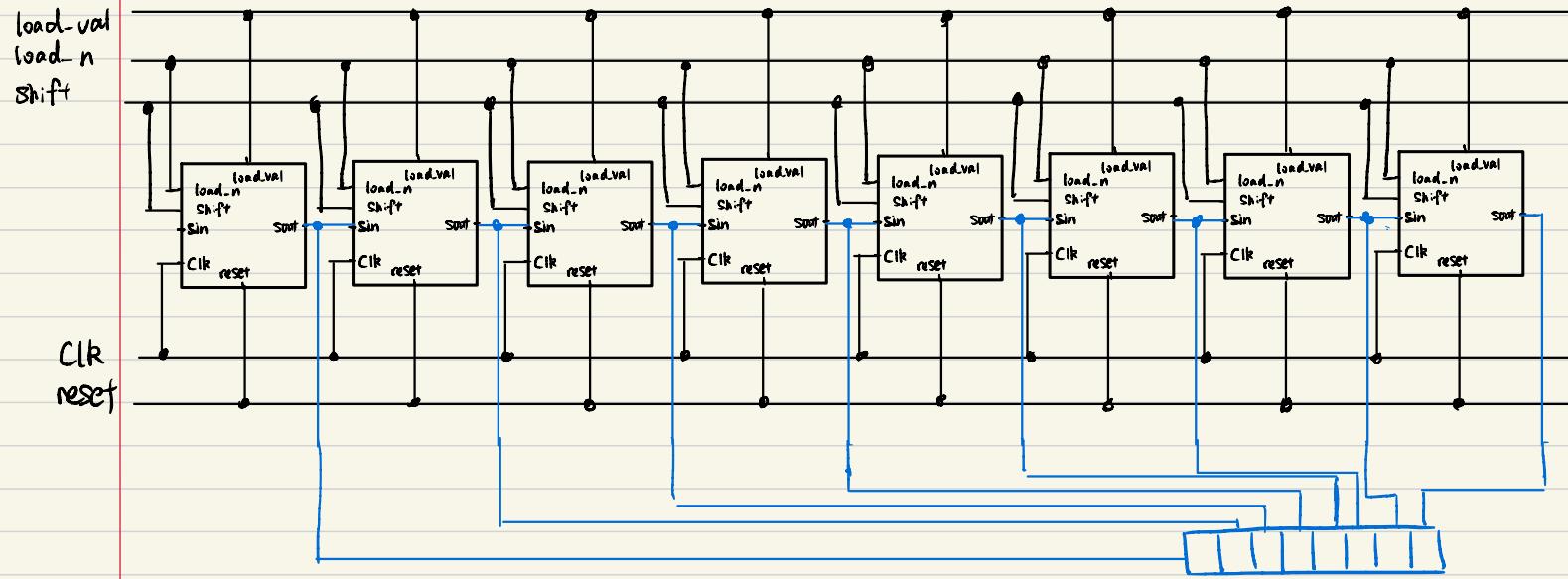
Set B to	0010
	0010
	0010
	0010
Set B to	0000
	0000



Part III

1. The output does not change on every positive clock edge.

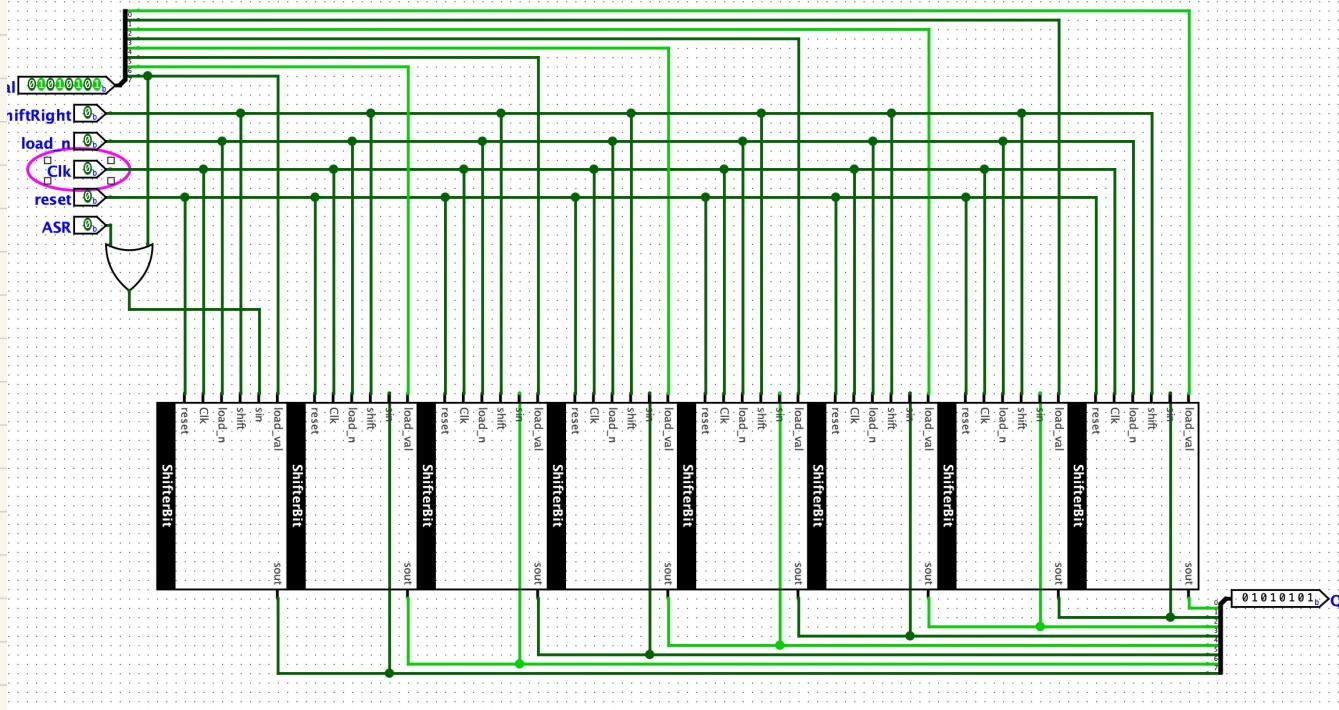
2. Schematic



5. Simulation

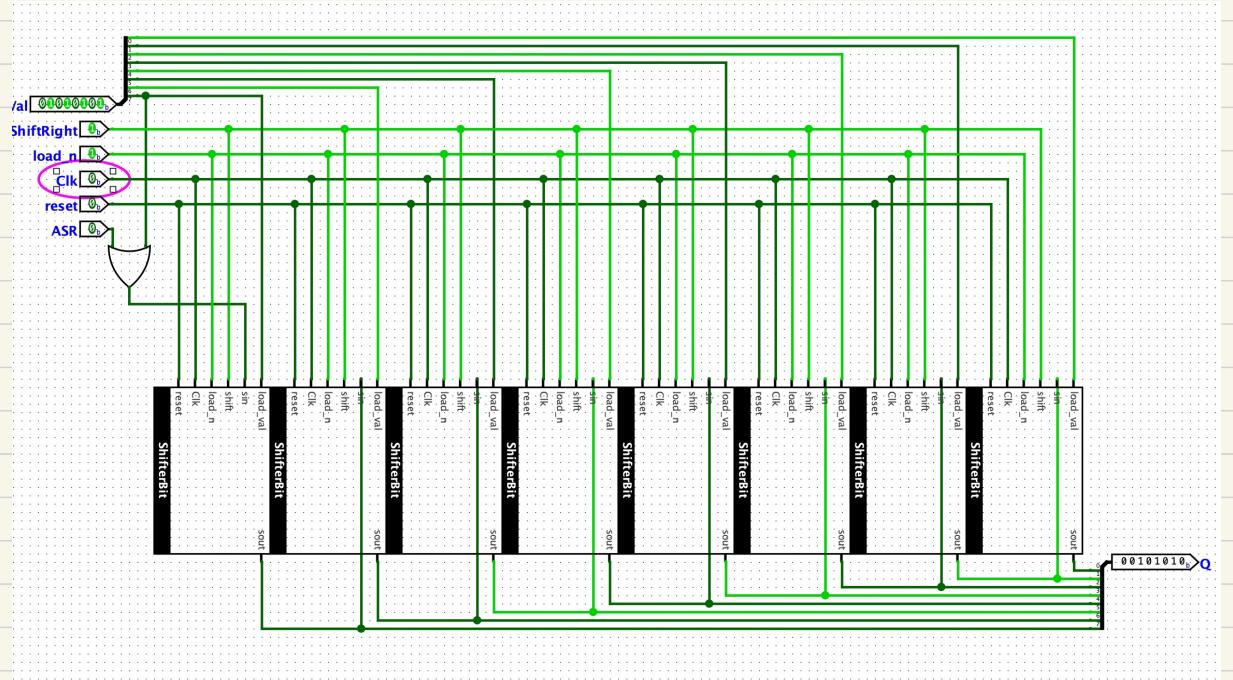
Load-n = 0 ASR = 0

Cycle 0 = load data

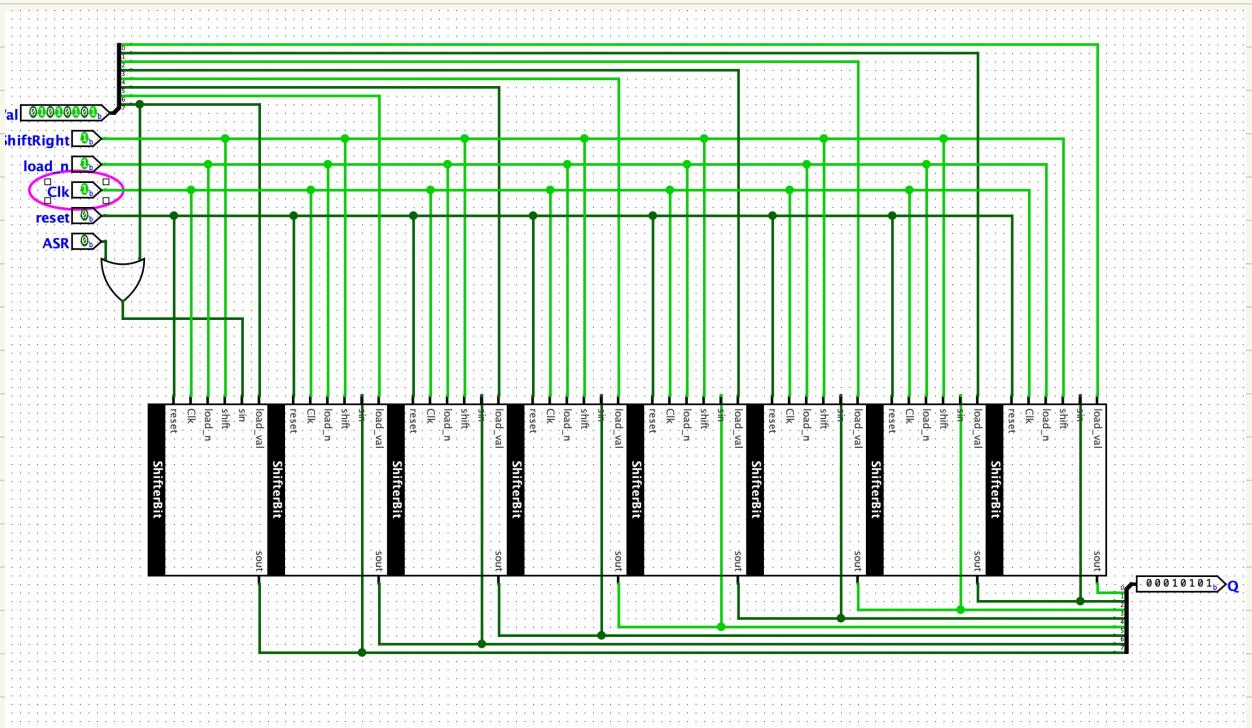


$\text{load_n} = 1$ $\text{ASR} = 0$ $\text{ShiftRight} = 1$

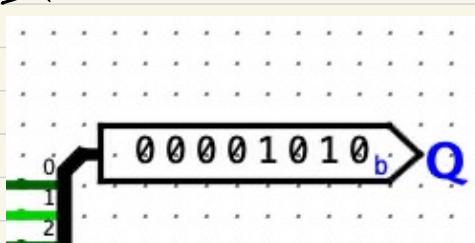
Cycle 1 :



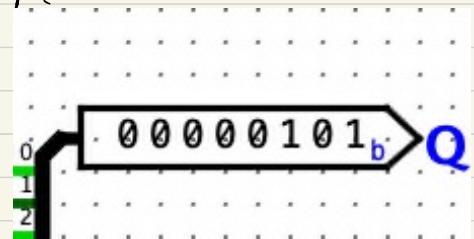
Cycle 2 :



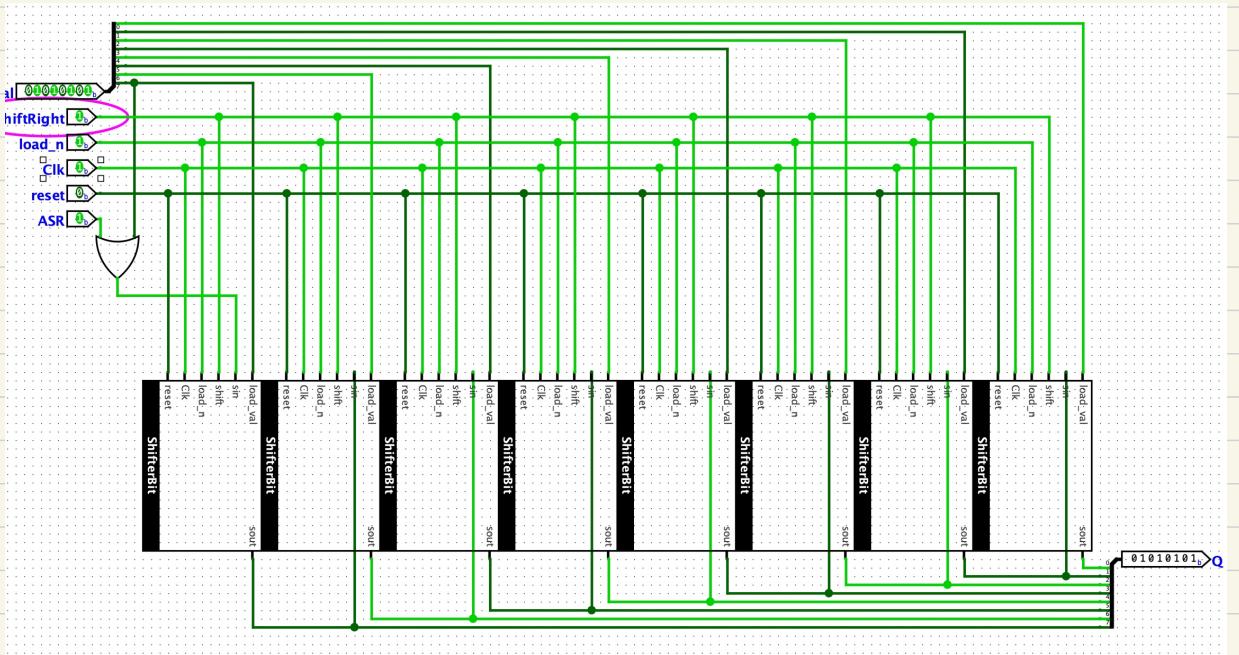
Cycle 3 :



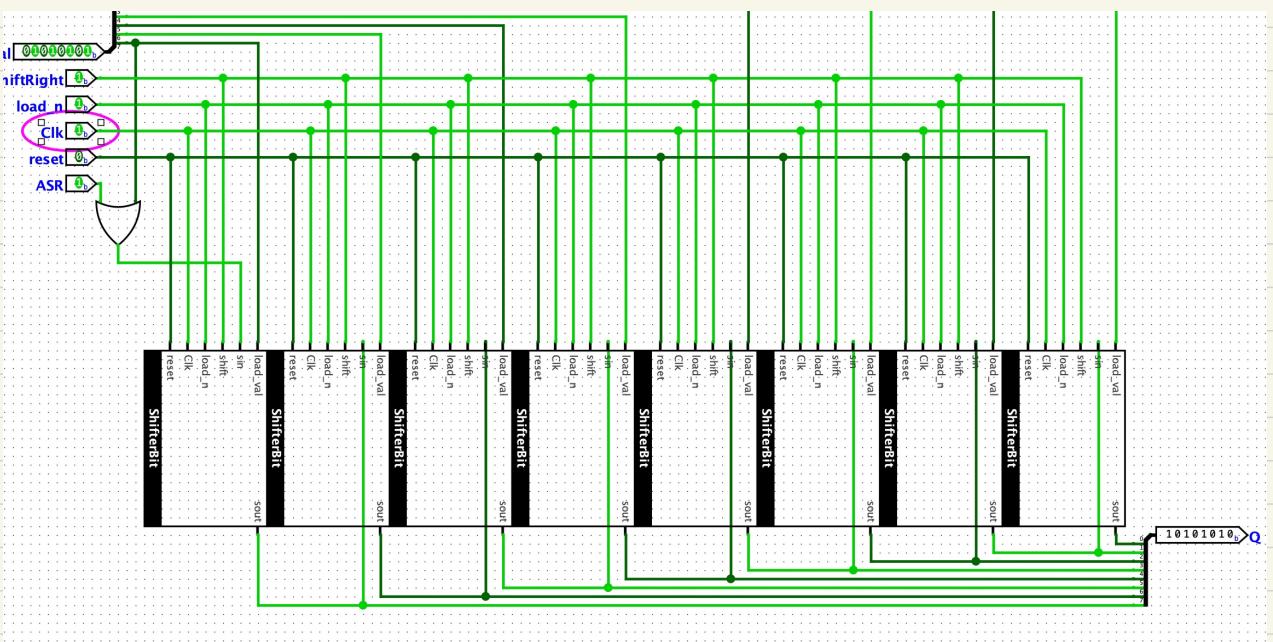
Cycle 4 :



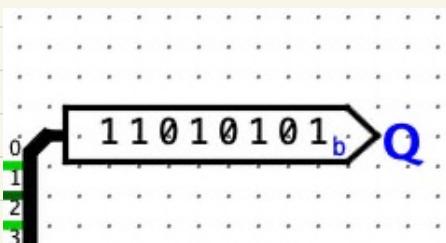
$ASR = 1$
Cycle 0:



Cycle 1:



Cycle 2:



Cycle 3:

