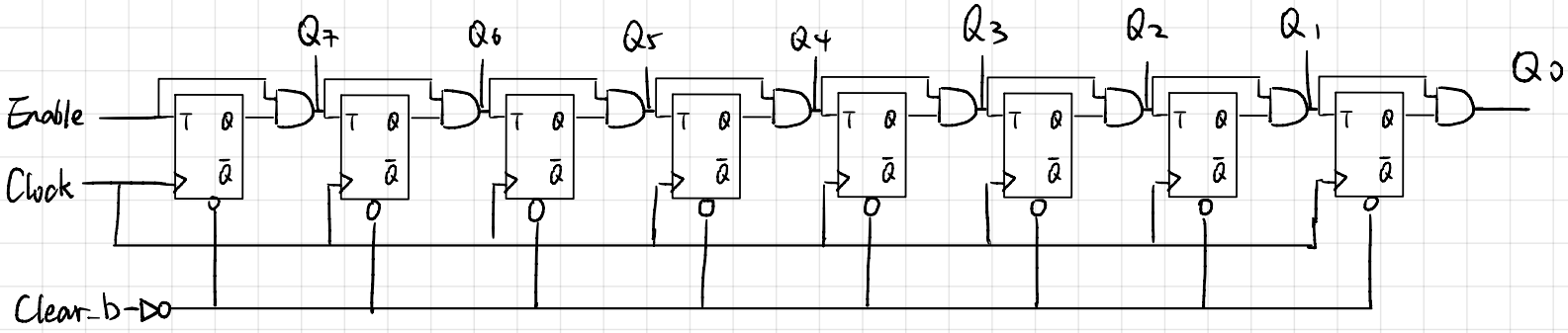
CSC 258 LAB 5

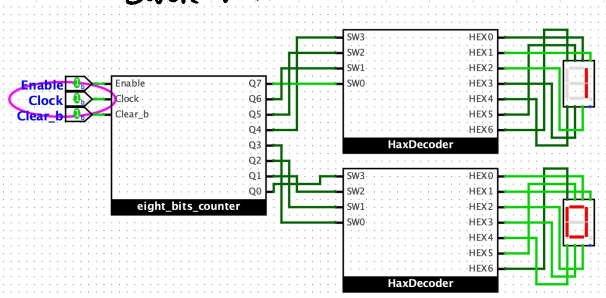
lichen 65 1004767558

Part 1

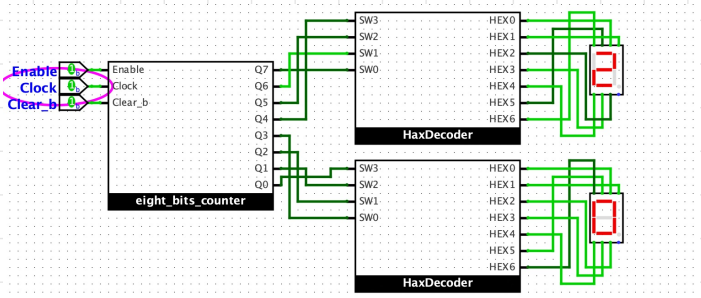
1.2.



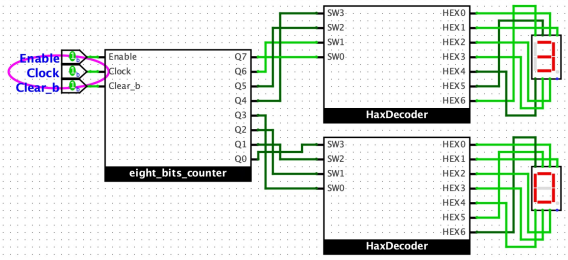
5. Clock 1 time



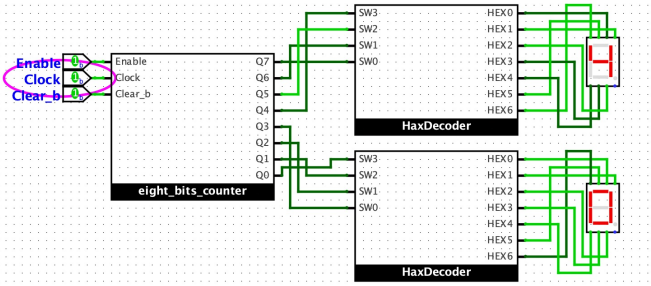
2 times



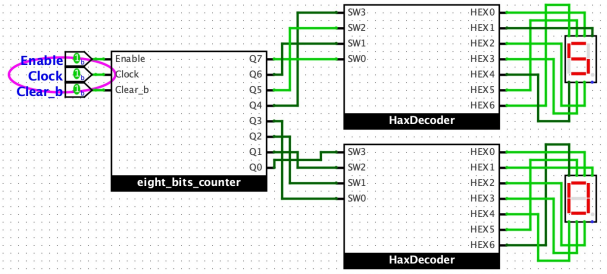
3 times



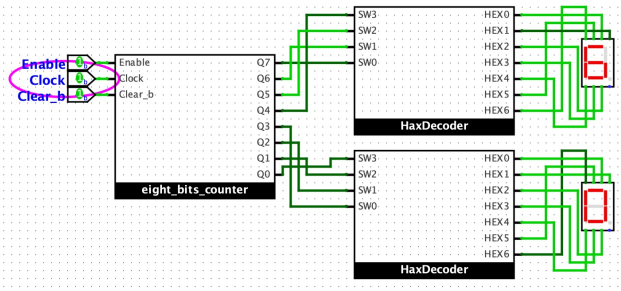
4:



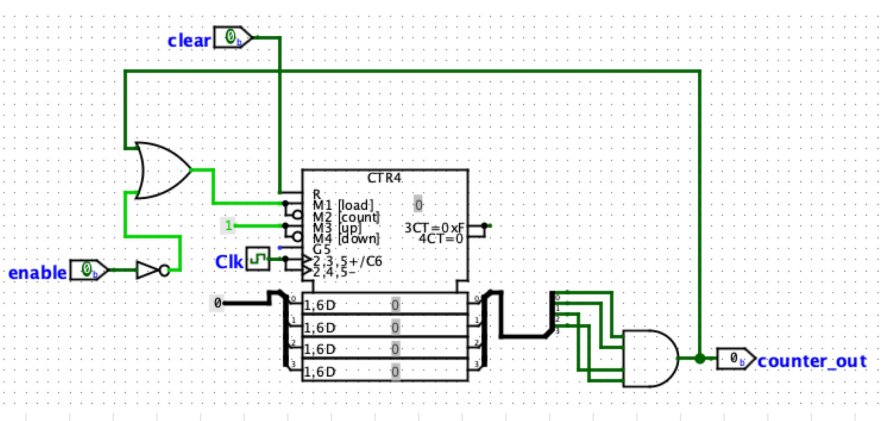
5:



6:



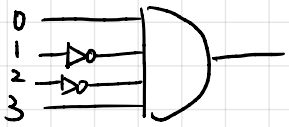
Part 2



1. The check for the maximum value is not necessary in the example above. Explain why in your prelab report **(PRELAB)**
2. If you wanted this 4-bit counter to count from 0-9, how would you adjust the circuit above? **(PRELAB)**
3. In *Properties* there is a setting called *Action On Overflow*. Explain how each value for this setting responds to overflow by experimenting with this setting and describing the results. **(PRELAB)**

1. For educational purpose, the max value part explicitly shows how reloads work when reaches the max value.

2. We can change the right part from detect 1111 to 1001:

e.g. 

Then the circuit will reload when counter count to 9.

3. Wrap Around:
the next value is 0 if incrementing and max value if decrementing

Stay at value: remains at max / 0

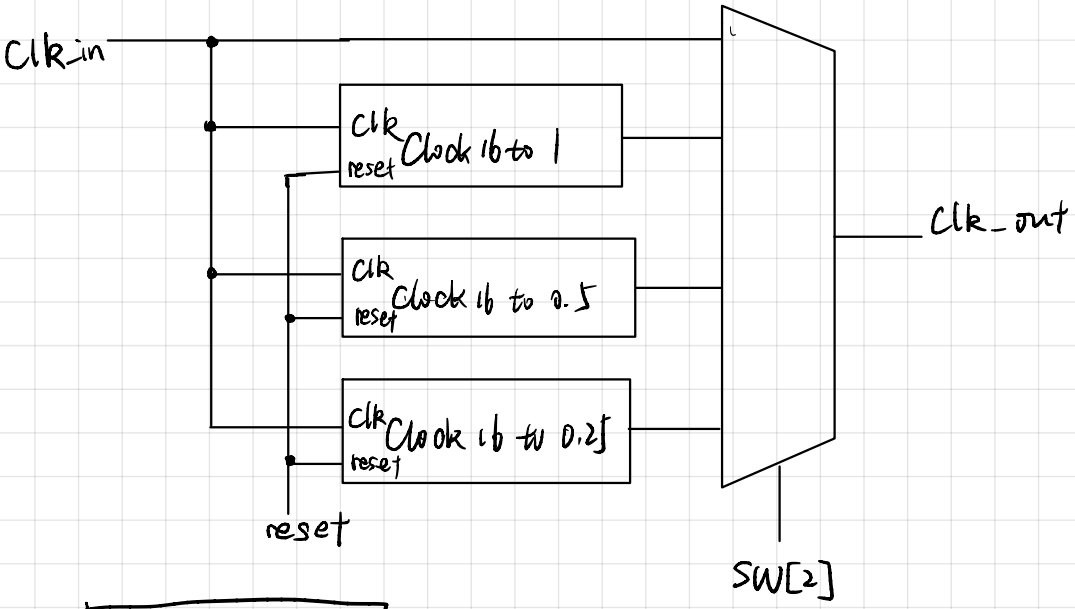
Continue counting: continue incrementing / de

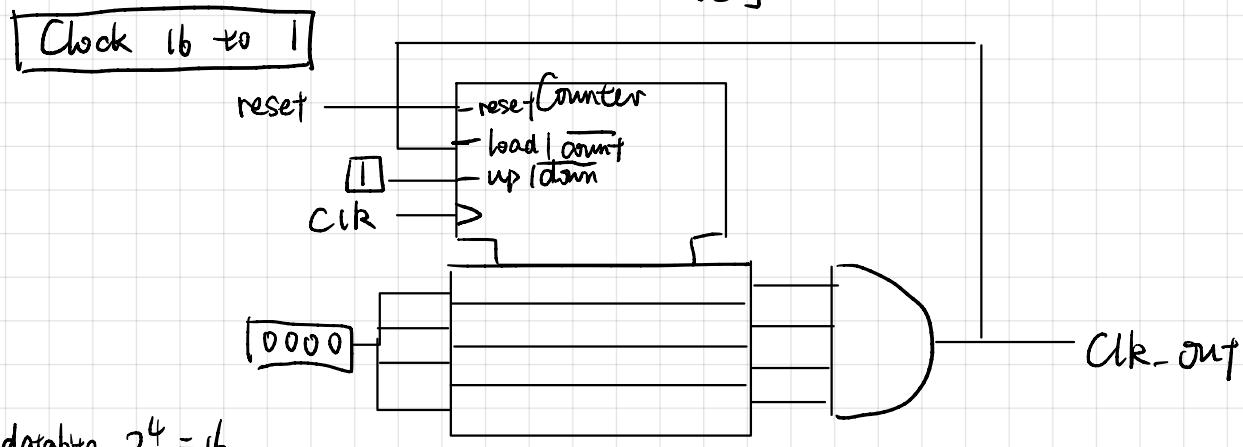
load next value: the next value is loaded from input.

In your prelab report, calculate how large a counter would be required to count 50 million clock cycles, as illustrated by Figure 3. How many binary bits would that counter need to represent such a value? **(PRELAB)**

$\lceil \log_2 50,000,000 \rceil = 26$

1. Draw Schematic





4 databits $2^4 = 16$

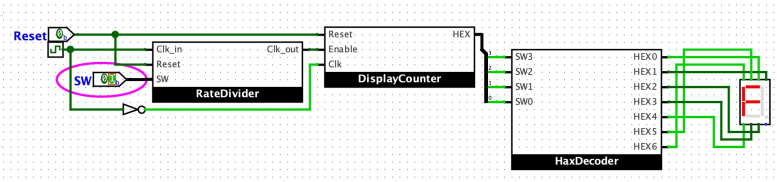
3 databits $2^3 = 8$

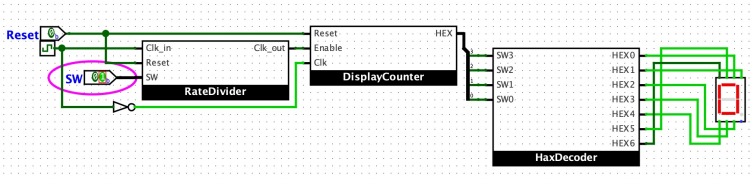
5 databits $2^5 = 32 \rightarrow 16/32 = 0.5$ Hz.

3. Test Cases :

		(16 Hz = 16 ticks per second) Duration of Clk_out	(16 cycles per second) Duration of Clk_out.
When SW = 00	16 Hz	1/8	1/16
SW = 01	1 Hz	2	1
SW = 10	0.5 Hz	4	2
SW = 11	0.25 Hz	8	4

After F is 0 :



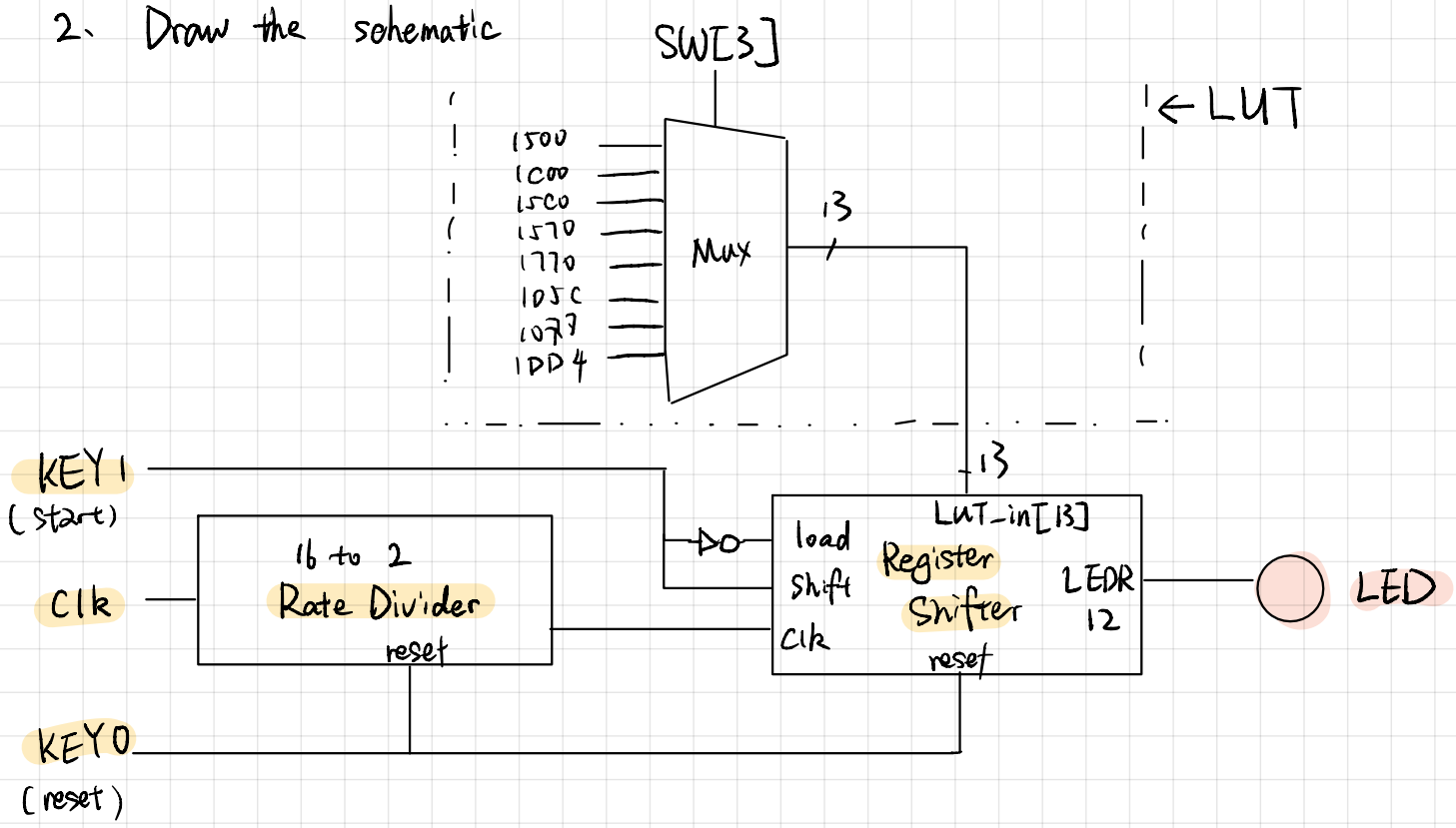


Part 3

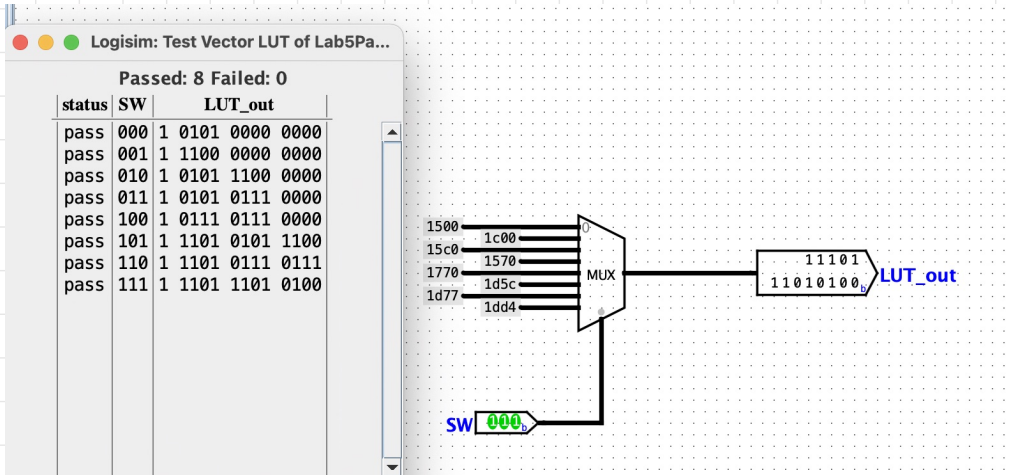
LUT

	Letter	Morse Code	Pattern Representation (sequence length is 13 bits)	Hex:
000	S	• • •	1010 1000 0000 0	1500
001	T	—	1110 0000 0000 0	1C00
010	U	• • —	1010 1110 0000 0	15C0
011	V	• • • —	1010 1011 1000 0	1570
100	W	• — —	1011 1011 1000 0	1770
101	X	— • • —	1110 1010 1110 0	1D5C
110	Y	— • — —	1110 1011 1011 1	1D77
111	Z	— — • •	1110 1110 1010 0	1DD4

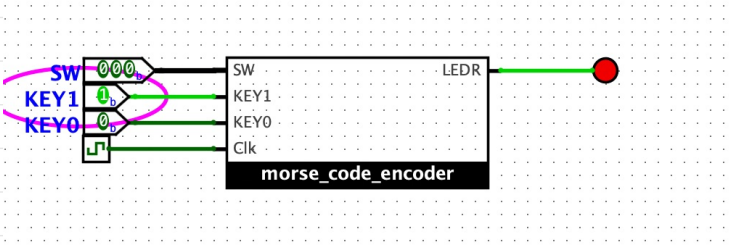
2. Draw the schematic



4. Test Vector

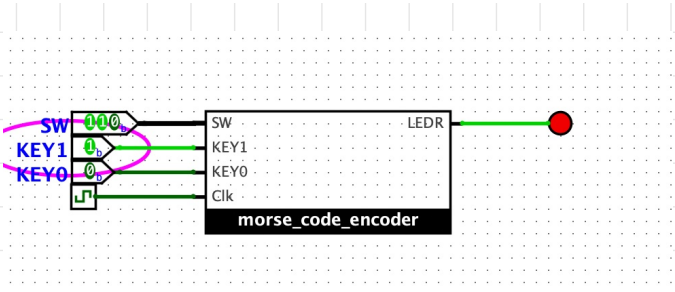


Test cases:



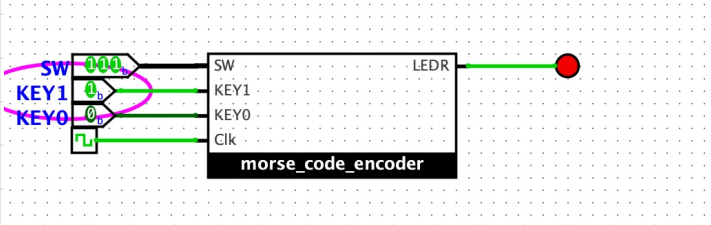
000:

three shorts



110:

long short long long



111:

long long short short