CoSP/CSP Network Solutions accelerated by Intel E810 DDP

Legal Disclaimer

General Disclaimer:

Technology Disclaimer:

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Performance Disclaimers:

Results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.

Agenda

- Overview
- CoSP Successful Use Cases
- CSP Successful Use Cases

Overview

E810 DDP Key Advantage

- Programmability
  - Programmable Packet Process Pipeline
    -- A single hardware for different workload acceleration.

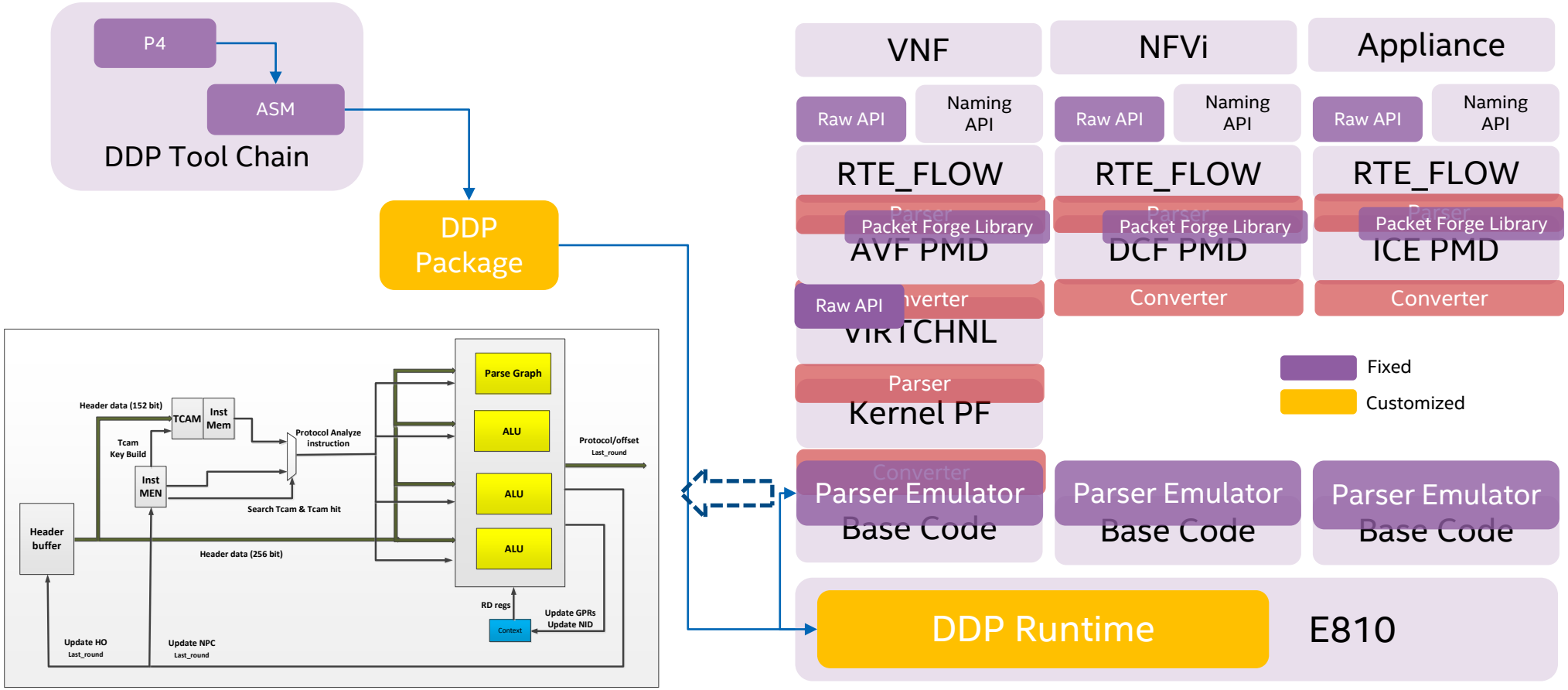
- Observability
  - Learning Driver
    -- A single software driver for different hardware customizations.

E810 DDP DPDK Enabling Summary

400+ RTE_FLOW Rule Types in DPDK 21.11!

DDP Features	v19.11			v20.05			v20.08			v20.11			v21.02			v21.05			v21.08		
	PF mode	VF mode	DCF Mode	PF mode	VF mode	DCF Mode	PF mode	VF mode	DCF Mode	PF mode	VF mode	DCF Mode	PF mode	VF mode	DCF Mode	PF mode	VF mode	DCF Mode	PF mode	VF mode	DCF Mode
RTE-FLOW API																					
Flow Priority																					
VxLAN/GRE																					
GTPU (EH)																					
PPPOE																					
PFCP																					
ESP/AH																					
L2TPv3																					
eCPRI																					
QinQ Filter																					
GTPU (5 tuple hash)																					
GTPU (w/o EH)																					
GTPU TEID filter																					
Symmetric Hash																					
Separate configure for outer IPv4/IPv6 GTPU																					
IPv6 prefix hash																					
Metadata Extraction to mbuf																					

Learning Driver



Testpmd Example

```
Create a filter base on inner l3 of a GTPU uplink flow in testpmd


#flow create 0 ingress pattern raw pattern
spec 00000000000000000000000008004500004200010000040117ca87f0000017f0000010
8680868002eba0d34ff001e000000000000085011000004500001600010000040007ce5000
000100000001 pattern mask
     00000000000000000000000000000000000000000000000000000000000000000000
00000000000000000000000000000000000000000000000000000000000000000000ffff
ffffffffffff / end actions queue index 3 / end
```

Parse

Offset	Protocol
0	MAC_DEPTH0
12	ETYPE_DEPTH0
14	IPV4_DEPTH0
34	UDP_DEPTH0
58	IPV4_DEPTH1

Profile

Protocol	Offset	Mask
IPV4_DEPTH1	12	0xffff
IPV4_DEPTH1	14	0xffff
IPV4_DEPTH1	16	0xffff
IPV4_DEPTH1	18	0xffff

New Features in Planning

- Protocol Agnostic Flow Offloading on AVF
- Package forging from **rte_flow_item_xxx** to training packet
- Support **rte_flow_item_flex**

CoSP Successful Use Cases

Intel 5G Wireless Core Work Scope

Breakthrough 5G Core Performance

TCO and power optimized

intel XEON

intel ETHERNET

5G UPF

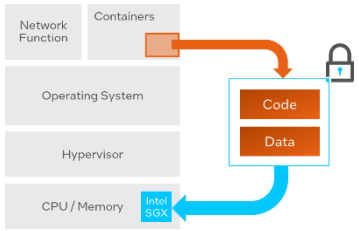
42%* Performance improvement

Breakthrough ecosystem performance for 5G UPF

640 Gbps[1]

Comprehensive Edge-to-Core Security

Hardened capability with **smallest attack surface for new 5G security threats**



intel SGX Tool

IPSEC **1.8x*** Performance improvement

Leading with Cloud Native

Automation

Acceleration

Kubernetes* Networking

Resource Management

Ease of deployment

End-to-end reference architecture and experience kits

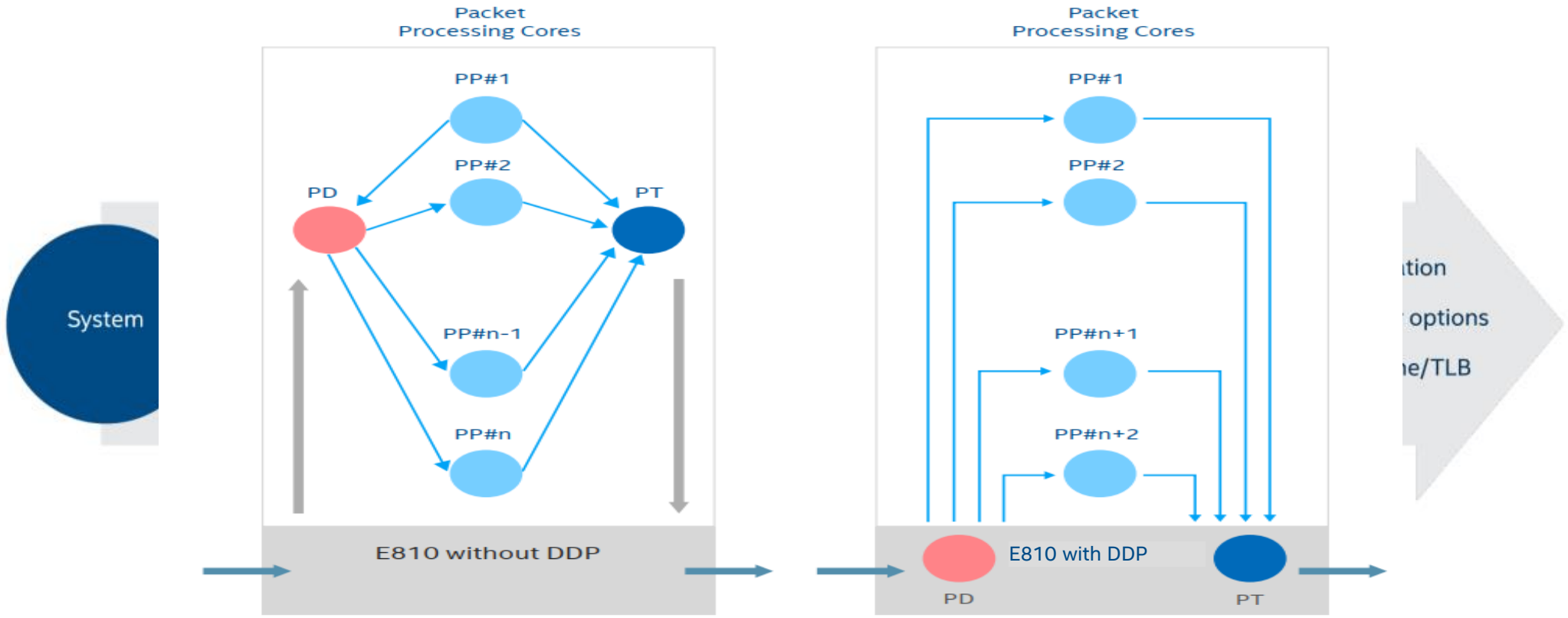
The Full Promise of 5G Begins with the 5G SA Core

1. NEC's High Performance 5G UPF on 3rd Gen Xeon SP
2. * Performance varies by use, configuration and other factors at www.intel.com/3gen-xeon-config

GTPU IPv4/IPv6 Combinations and Variants

		Tunnel Info													UE Info				
		MAC header		Eth Type	IPv4 Packet			UDP		GTP Header					IPv4 Packet			TCP / UDP	
ipv4+ipv4	x	DMAC	SMAC	0x0800 0x86DD	Dst-IP	Src-IP	Protocol	Src-Port	Dst-Port	Msg Type	Length	TEID	Seq #	ExtHdr	Dst-IP	Src-IP	Protocol	Src-Port	Dst-Port
		MAC header		Eth Type	IPv6 Packet			UDP		GTP Header					IPv6 Packet			TCP / UDP	
ipv6+ipv6	x	DMAC	SMAC	0x0800 0x86DD	Dst-IP	Src-IP	Protocol	Src-Port	Dst-Port	Msg Type	Length	TEID	Seq #	ExtHdr	Dst-IP	Src-IP	Protocol	Src-Port	Dst-Port
		MAC header		Eth Type	IPv4 Packet			UDP		GTP Header					IPv6 Packet			TCP / UDP	
ipv4+ipv6	x	DMAC	SMAC	0x0800 0x86DD	Dst-IP	Src-IP	Protocol	Src-Port	Dst-Port	Msg Type	Length	TEID	Seq #	ExtHdr	Dst-IP	Src-IP	Protocol	Src-Port	Dst-Port
		MAC header		Eth Type	IPv6 Packet			UDP		GTP Header					IPv4 Packet			TCP / UDP	
ipv6+ipv4	x	DMAC	SMAC	0x0800 0x86DD	Dst-IP	Src-IP	Protocol	Src-Port	Dst-Port	Msg Type	Length	TEID	Seq #	ExtHdr	Dst-IP	Src-IP	Protocol	Src-Port	Dst-Port

Samsung NGCore Performance Enhancement



Better NGCore Performance through Samsung-Intel Collaboration

Samsung : Throughput And Latency Improvements

	HP Server
CPU	Intel® Xeon® Platinum 8280 Processor
Number of CPUs	2
Memory	384GB DDR4
Network Adapter	2 x Dual-port 100Gb Intel® Ethernet Network Adapter E810-CQDA2

White Paper

intel | SAMSUNG

Executive Summary

Samsung Achieves 305 Gbps on 5G UPF Core Utilizing Intel® Architecture

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Executive Summary

5G is creating a ripple effect of innovations and developments that will enrich our daily lives. 5G commercial services have begun in 2019 and operators have been continuing to enhance their services with the latest network technologies.

As part of an ongoing partnership, Samsung and Intel have collaborated on performance and latency optimizations of Samsungs 5G Cloud Native UPF, which resulted in a significant performance breakthrough of data throughput measuring 305 Gbps. This was achieved by utilizing software optimizations on Intel® Xeon® Platinum 8280 processor and Intel® Ethernet Network Adapter E810-CQDA2 platforms. This performance and efficiency enables operators to deliver higher quality end user experiences at a lower total cost of ownership.

1. Introduction

We have already had a taste of what 5G will deliver over the next decade from the upgraded 5G New Radio (NR) devices and networks being deployed around the world, providing access to new spectrum and bandwidth. However, the majority of deployments are 5G Non Stand-Alone (NSA) network configurations, which retains much of the 4G core network to support the 5G NR base stations.

To fully unleash the potential of 5G, and to support the new, exciting use cases like Ultra Reliable Low Latency Communication (URLLC), Industrial Control and Fixed Wireless Access (FWA), the entire network will need to be upgraded to 5G Stand Alone (SA). This involves all the 4G network infrastructure being upgraded to a brand-new Service Based Architecture (SBA).

We cannot underestimate the impact 5G will bring to our industry and to our lives, but there is also an evolution happening at the platform level which is having an equally important effect. The shift to 5G SA requires platforms that are providing increases in performance and throughput which are critical to improving the effiiciency, scalability and flexibility of the 5G network.

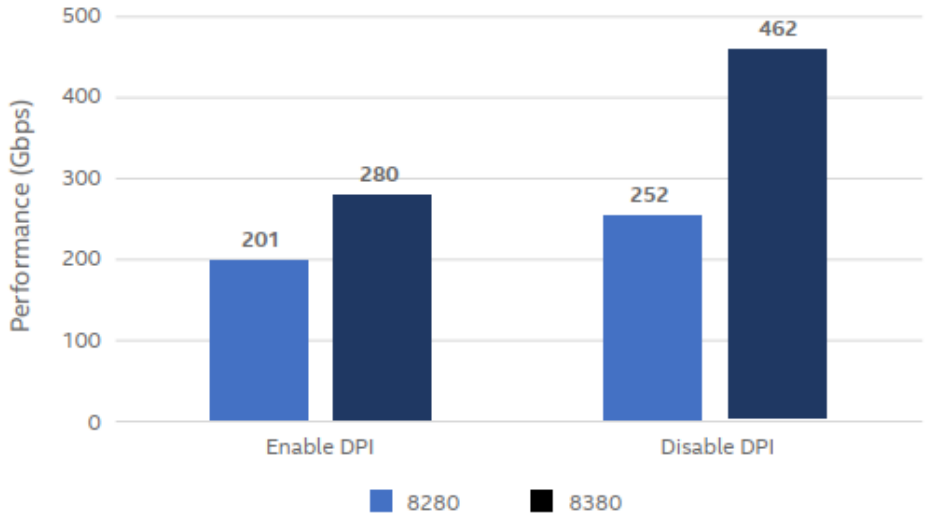
ZTE : Throughput And Latency

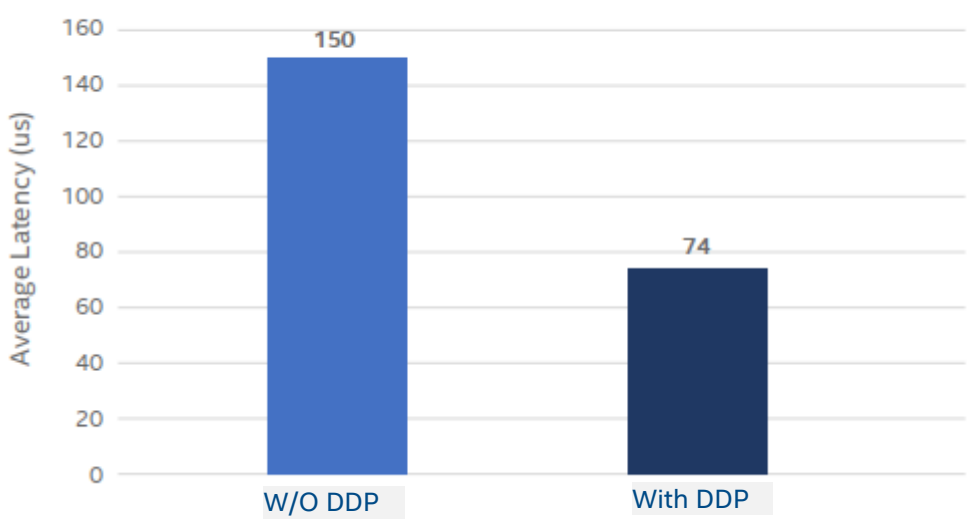
White Paper

5G Core

intel

ZTE's High Performance 5G Core Network UPF Implementation Based on 3rd Generation Intel® Xeon® Scalable Processors





Server	
Ucode	
CPU	
Number	
Memory	512G DDR4@2666MHZ
Network Adapter	4x Dual-port 100Gb Intel® Ethernet Network Adapter E810-CQDA2 on 6330N server 6x Dual-port 100Gb Intel® Ethernet Network Adapter

Table of Contents

without any additional hardware acceleration.

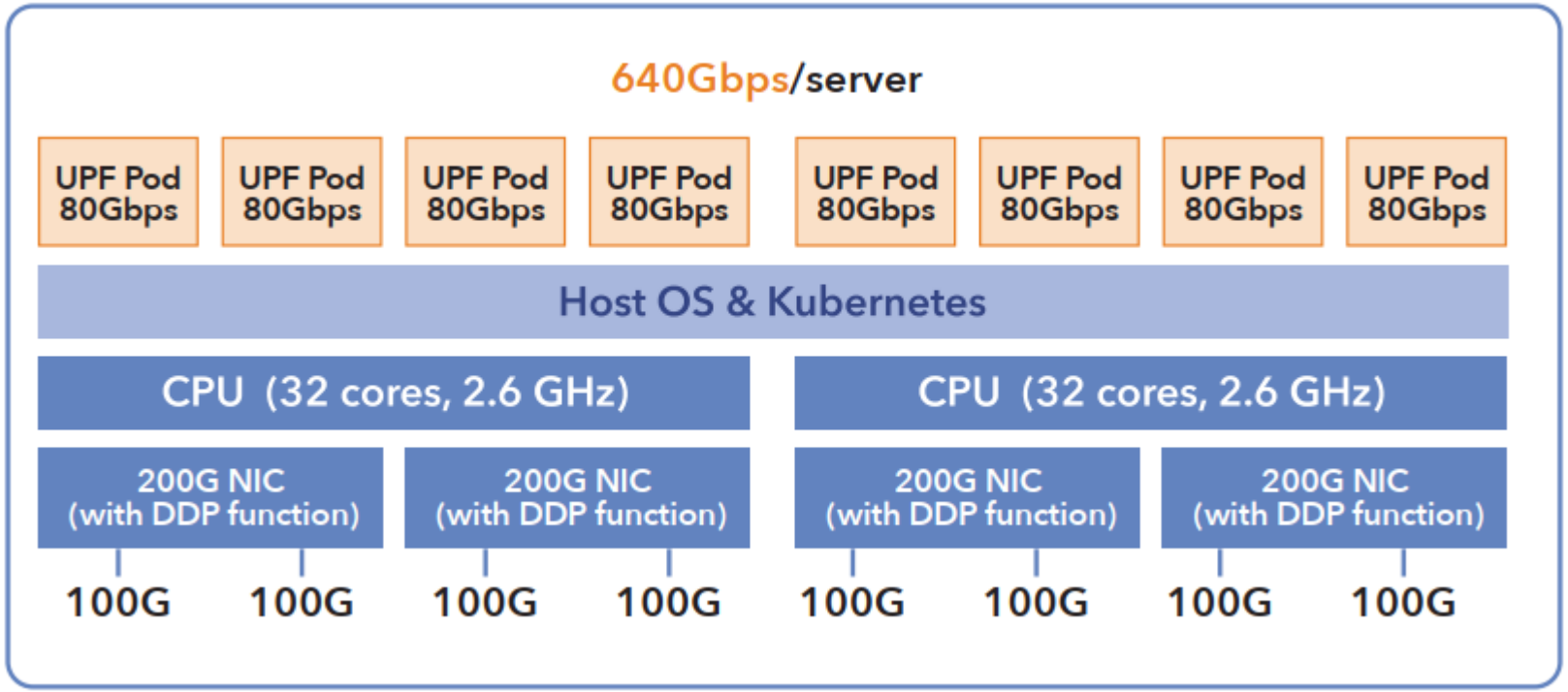
This test was completed by ZTE on March 30th, 2021. See the System Test Environment section for specific test configurations.

1. ZTE 5G Virtualized and Cloud Native UPF Solution

1.1. ZTE 5G Common Core Introduction

5G capabilities will help enable continuous wide area coverage, low power consumption, low latency, and high reliability connectivity. It will meet the diversified service requirements of eMBB, mMTC, uRLLC and other application scenarios.

NEC : Throughput And Latency Improveme



CPU	Intel® Xeon® Platinum 8358 2.60 GHz, 32 c
Memory	DDR4-2933 DI
NIC	Intel® Ethern E810-2CQDA2
Host OS	CentOS Linux 8
Host OS kernel	4.18.0-193.28.1.el8_2.x86_64
Kubernetes	Ver. 1.19.3
DPDK	Ver. 20.08

: based on DSCP

:ching)
dvanced

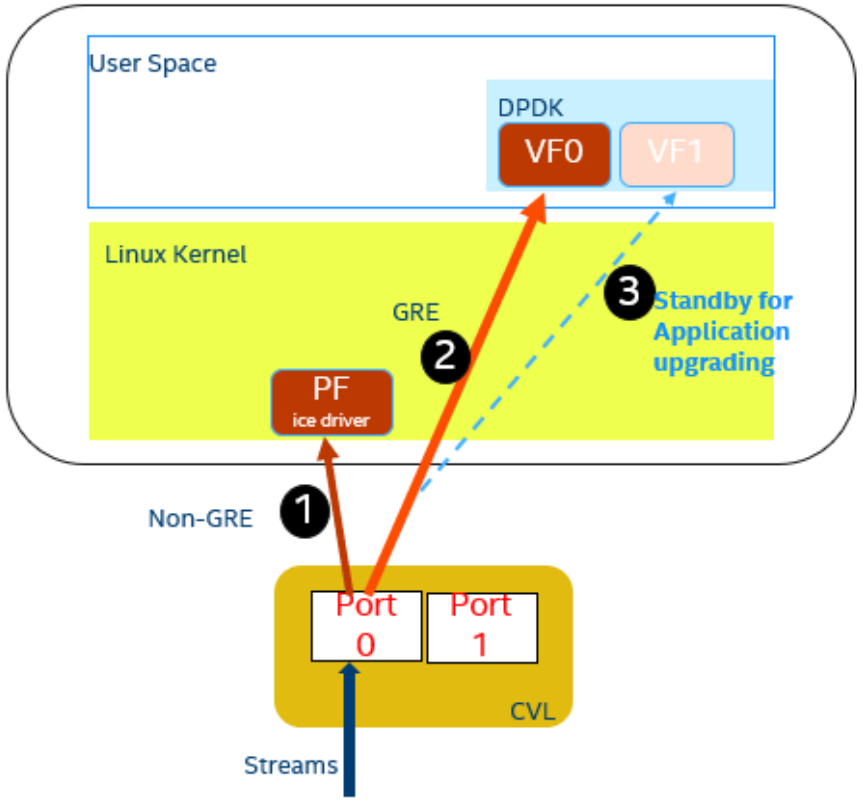
nments)

edge of 5G coverage areas, reducing latency and increasing capacity.
As a result, service providers can offer C-plane

designed in a cloud-native architecture to meet these requirements. NEC's strong track record and technical capabilities and expertise in both mobile

CSP Successful Use Cases

CSP Gateway with custom GRE



Data Plane

Packet Filtering

- IPv4 case only (both outer and inner)
- Steering GRE (proto = 0x2f) packet to specific VF
- DST MAC address is same as PF's
- Cover fragmented packet (both outer and inner).

RSS for workload distribution

- Be applied on GRE packet on VF
- For non fragmented packet, take inner L3 / L4 as input se
- For inner fragmented packet, take inner L3 as input set
- For outer fragmented packet, take outer L3 as input set

Control Plane

- VF based configuration including global data plane steering and VF0/VF1 hot swap.
- Single DPDK port for data path and control path (rte_flow)

Solution

1. DDP profile to support Custom GRE

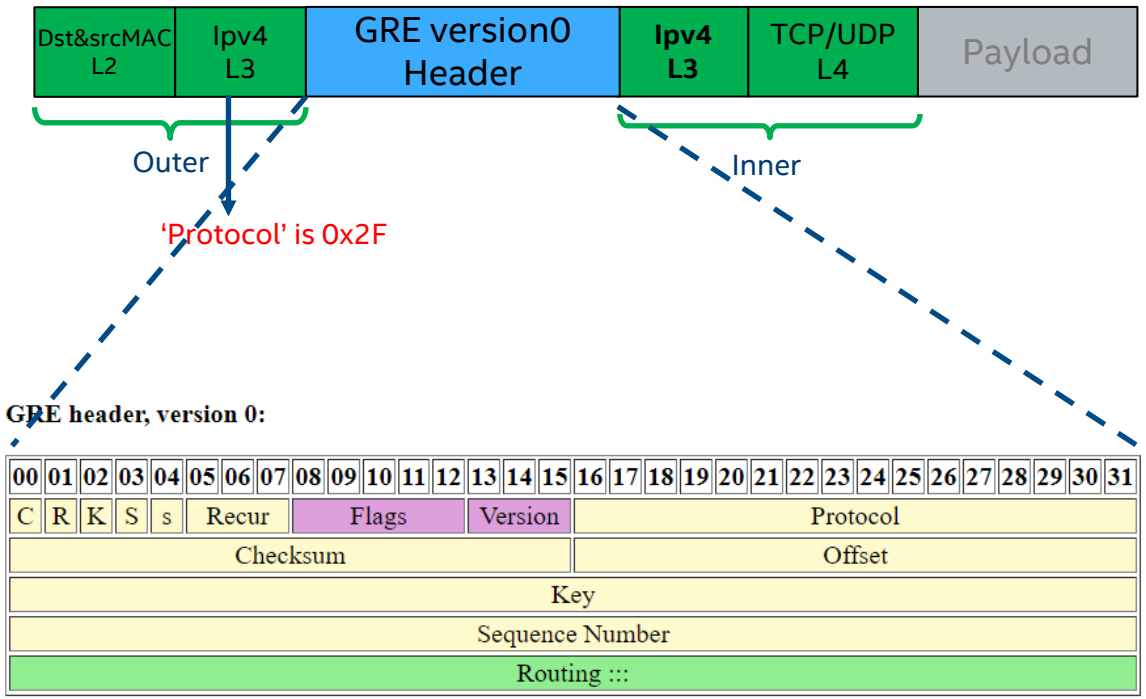
2. Custom DPDK-DCF (Device Config. Function) for CVL VF: remove DCF VF0, enable DCF capability to VF1/2 and transition. Add Datapath to DCF capability

3. Kernel PF driver with patches to support DPDK-DCF RTE_FLOW

DDP for Custom GRE

GRE Packet Formats

GRE tunneling packet basic format

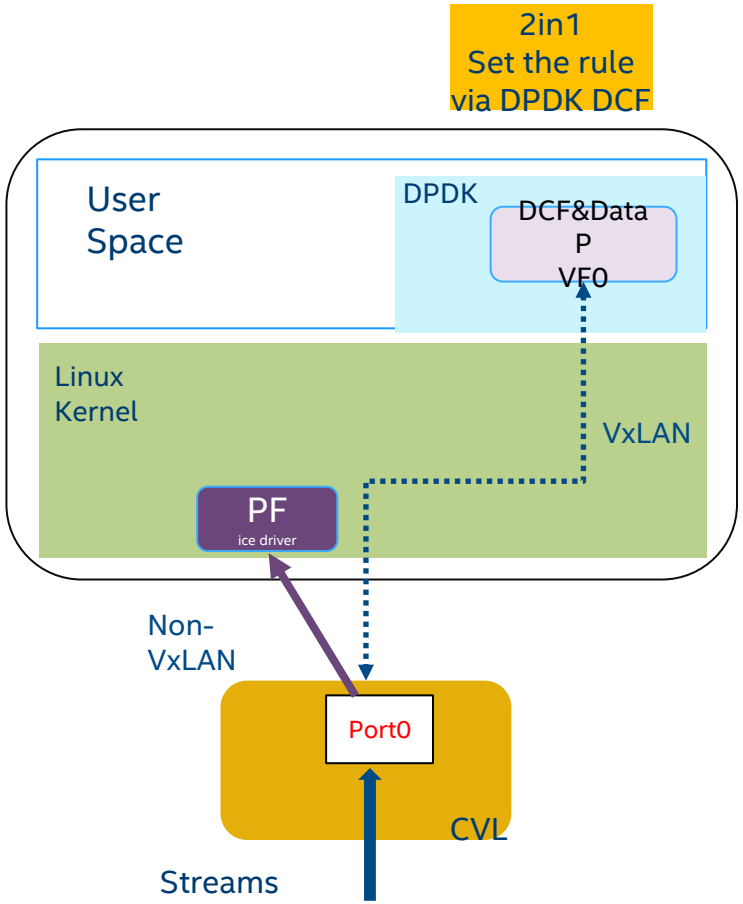


- Based on different business application, the length of GRE header is scalable. Defined as below:
  - ✓ GRE Header size is 4 Byte, when C,R,K,S = 0'bit;
  - ✓ GRE Header size is 8 Byte, when K=1;
  - ✓ GRE Header size is 12 Byte, when K=1 & S=1;
  - ✓ GRE Header size is 16 Byte, when K=1 & S=1 & C=1.

- The Value in GRE Version Field
  - ✓ Version = 0;
  - ✓ Version = 1;

Reference: http://www.networksorcery.com/enp/protocol/gre.htm

CSP Cloud with custom VxLAN



VF0 takes DCF & iAVF 2in1

- **Control Plane: RTE_FLOW in VF0, DPDK-DCF.**
- **Data Plane: Steer Vxlan pkt to specific VF,**

  non-Vxlan to PF

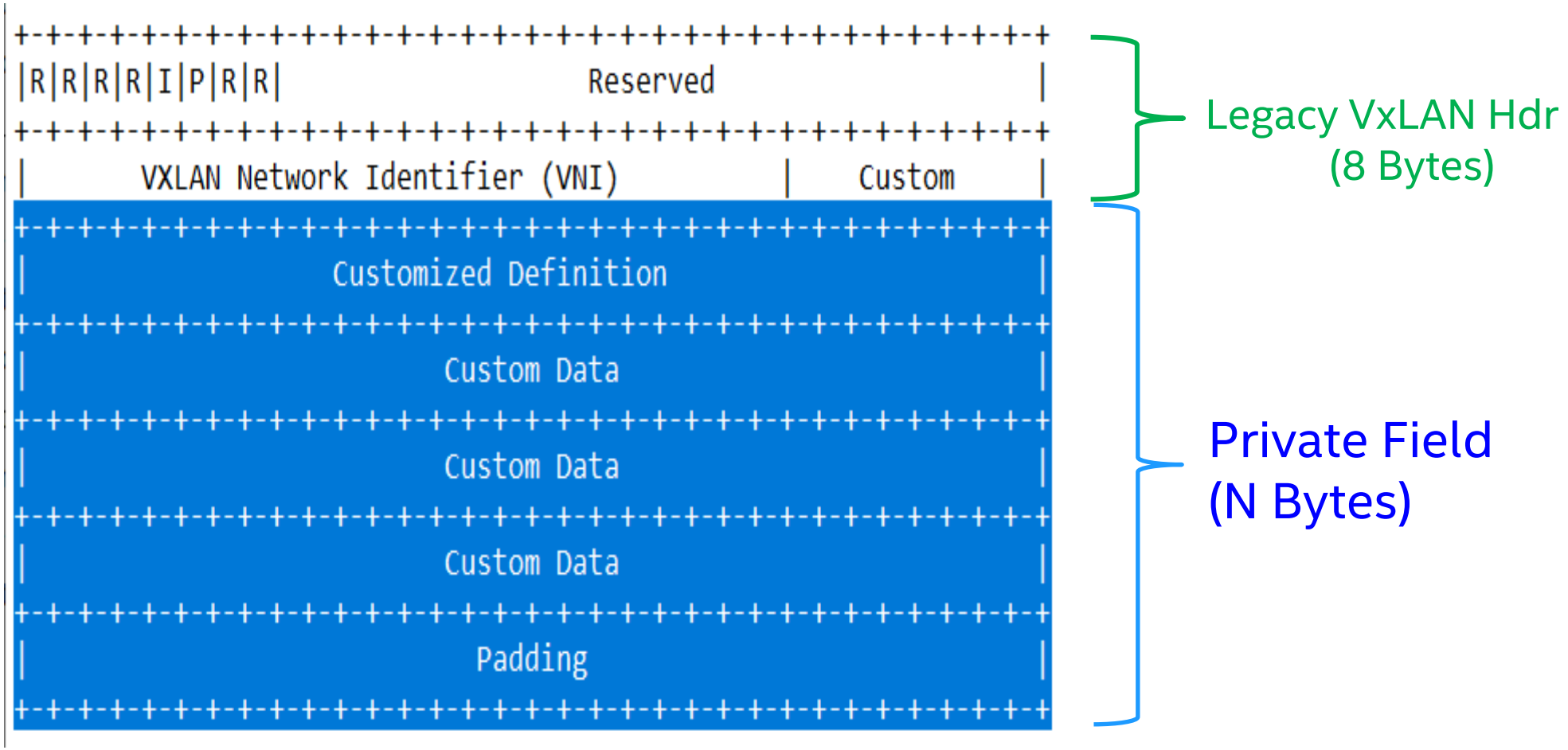
TSO HW Offloading

- **Requirement:**

  Standard VXLAN inner TSO is needed

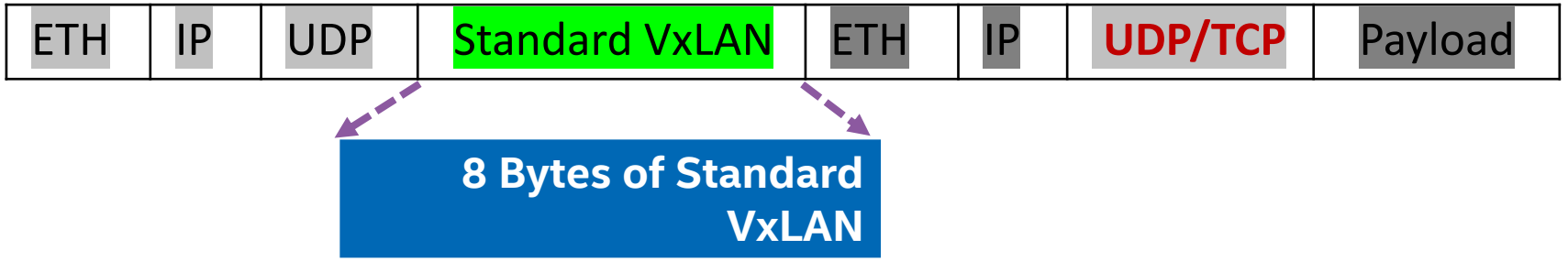
  RSS Hash

DDP for Custom VxLAN

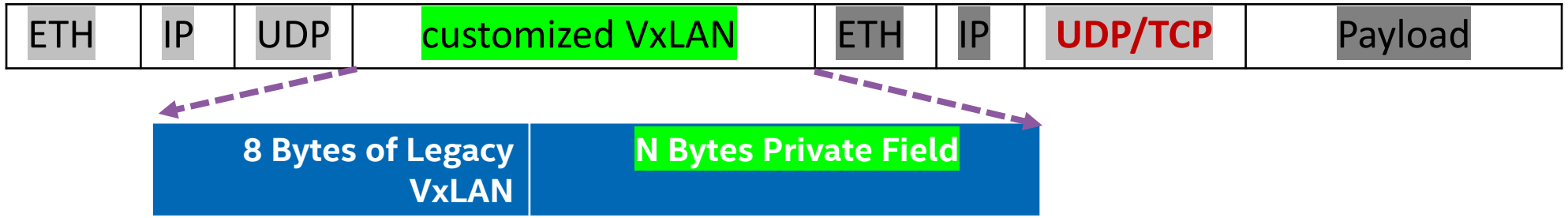


Custom VxLAN Solution

Standard VxLAN pkt:



Custom VxLAN pkt:



- TSO for VxLAN* inner-TCP segmentation
- RSS Input set for VxLAN*: **outer-L3**: IPv4 dstIP+srcIP + **outer-L4**:dstP+srcP
- RSS Input set for VxLAN*: **inner-L3**: IPv4 dstIP+srcIP + **inner-L4**: dstP+srcP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