



INTEL® NETWORK TECHNOLOGY WORKSHOP

OPENING REMARKS

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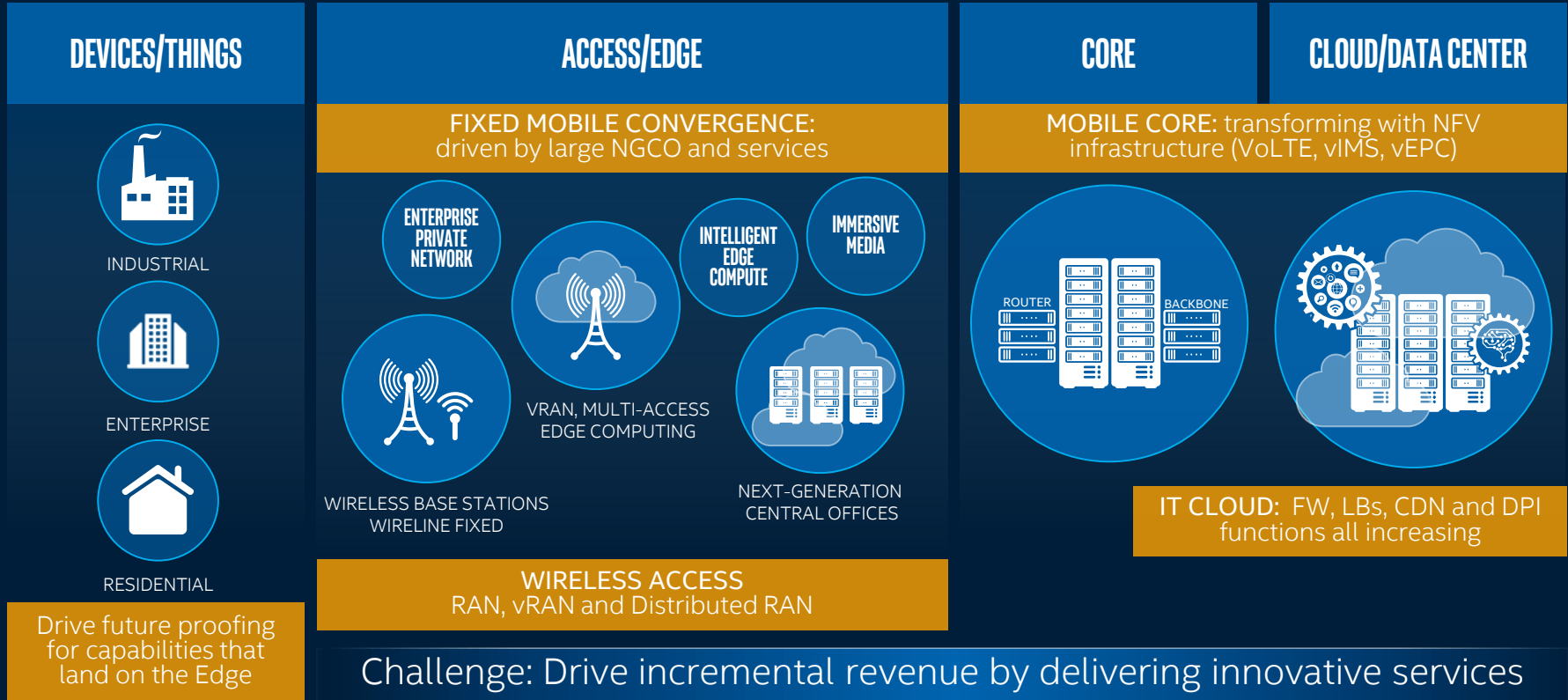
Data Explosion Driving Network Transformation

**BILLIONS OF DEVICES WILL
GET CONNECTED**

VIDEO STREAMING IS EXPLODING

**ULTRA-LOW LATENCY MACHINE TO
MACHINE COMMUNICATIONS**

Network Infrastructure Opportunities



Challenge: Drive incremental revenue by delivering innovative services

Network Transformation

– Moving The Network At Cloud Pace



CLOUD-READY:
**POOLED COMPUTE, NETWORK
& STORAGE**

Standardized, Commercial-
Grade Solutions



FLEXIBLE:
**SOFTWARE-DEFINED, DYNAMIC
NETWORKS**

Next-Generation
Network Architectures



DISTRIBUTED:
SERVICES DELIVERY & AGILITY
Business Process
Transformation

2nd Gen Intel® Xeon® Scalable Platform

– World-class Infrastructure For Transformed Networks

MICRO-ARCHITECTURE & ACCELERATION

- Integrated Intel® **Advanced Vector Extensions 512**
- Intel® **Optane™ DC persistent memory**
- Intel® **Deep Learning** Boost for inference
- Available with Intel® **QuickAssist Technology**

INTEL® INFRASTRUCTURE MANAGEMENT TECHNOLOGIES

- Industry-leading Intel® **Virtualization Technology**
 - Seamless VM migration for over 5 generations
- Enhanced Intel® **Resource Director Technology**
 - New Intel resource orchestration software
- INTEL® **Speed Select Technology**
 - Prioritize workload performance

INTEL® ETHERNET 800 SERIES

- New with **Application Device Queues (ADQ)** and **Dynamic Device Personalization (DDP)** along with DPDK and Kernel networking advancements



Broadest selection of SKUs for customers unique and evolving needs to improve TCO

Unlocking Platform Performance with Software



Hyperscan is a high-performance multiple regex matching library available as open source with a C API.



The Data Plane Development Kit is a set of software libraries for accelerating packet processing workloads on COTS hardware platforms.



The Universal Data plane relentlessly focused on data IO speed and efficiency for more flexible and scalable networks and storage.

SCALABLE PLATFORMS



INTEL® XEON®
PROCESSORS



INTEL ATOM®
PROCESSORS



INTEL® CORE™
PROCESSORS



VPU



INTEL® FPGA



INTEL® OPTANE® DC
SOLID STATE DRIVE



INTEL® ETHERNET
CONTROLLER

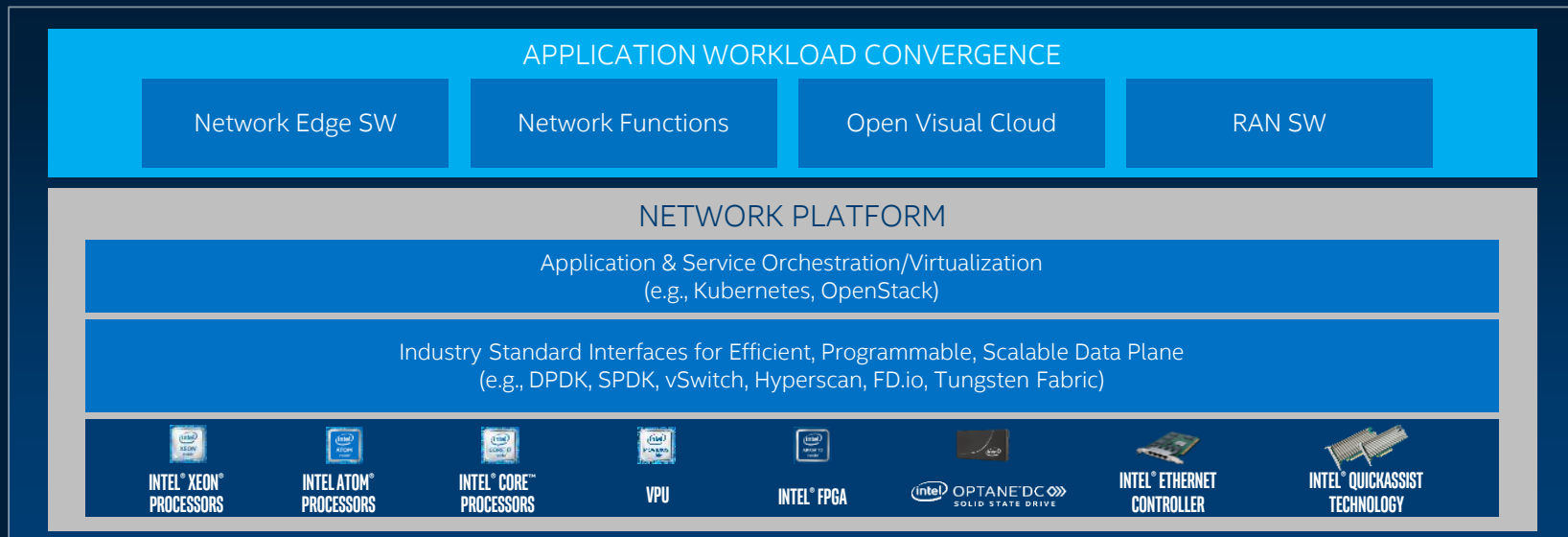


INTEL® QUICKASSIST
TECHNOLOGY

Converge The Workloads

Services (IoT Verticals, Comms, Cloud, Enterprises)

Developer Edge Frameworks (e.g., AWS, Azure, Baidu, Alibaba)



Use rich and flexible software frameworks for faster customer solution readiness and deployments

Partnerships: Winning With The Ecosystem

INVEST

OPEN SOURCE AND STANDARDS



INDUSTRY COLLABORATION

INTEL® NETWORK BUILDERS &
INTEL® DEVELOPER ZONE

350+

Members

35+

Comms SPs

100+

POCs/Trials/Deployments
Based on Member Solutions

13,000+

Developers Trained
Worldwide

12,000+

Network Builder
University Program
Members

50+

Network Edge
Ecosystem Program
Members

251,480+

IDZ Page Views



NFVI

NETWORK FUNCTIONS
VIRTUALIZATION
INFRASTRUCTURE



Lenovo

NOKIA



UCPE

UNIVERSAL CUSTOMER
PREMISES EQUIPMENT

ADVANTECH

CASWELL

Lanner

PREMIER

Silicom
Community Solutions

SUPERMICR



Intel® Select Solutions for Visual Cloud available Q2'19

Use industry-leading ecosystem programs
to drive edge transformation and enable developers

Continuous Innovation Driving Business

Intel, Baidu sign 3-year deal to collaborate in cloud, AI, 5G

Intel and Baidu on Thursday [announced](#) a new, three-year agreement to collaborate on technology related to Baidu's core businesses -- namely, cloud, AI, autonomous driving, 5G and edge technologies. Building on 10 years of partnership, the deal revolves around Intel optimizing its platforms and products for the Chinese tech giant.

Researchers mine cache of Intel processors to speed up data packet processing

Developed with Ericsson Research, the slice-aware memory-management scheme allows frequently used data to be accessed more quickly via the last-level cache of memory (LLC) of an Intel Xeon CPU. By establishing a key-value store and allocating memory in a way that it maps to the most appropriate LLC slice, they demonstrated both high-speed packet processing and improved performance of a key-value store. The team used the proposed scheme to implement a tool called CacheDirector, which makes Data Direct I/O (DDIO) slice-aware and published a conference paper, Make the Most out of Last Level Cache in Intel Processors, which was presented at EuroSys 2019 in the spring.

Lanner Electronics upgrades processors in flagship network appliance line

Lanner Electronics' four flagship network appliances, the NCA-6210, NCA-5710, NCA-5520, and FX-3230 models, are being upgraded to the 2nd generation Intel Xeon Scalable Family Processors, that feature up to 28 cores per processor, Intel AVX-512 instructions, and Intel QuickAssist technology.

Nokia Puts a Physical Box at the Edge to Support Cloud, 5G

Inside that box is a commoditized x86 architecture running an Intel processor. The chassis can support up to five servers, with those servers upgradeable to a Nokia chipset for more capacity.

Ericsson, Intel Team Up on 5G Software-Defined Infrastructure

Ericsson and Intel are jointly developing a hardware management platform for service providers targeting 5G, NFV, and distributed [cloud](#).

Call For Action

PARTNER with the ecosystem

INNOVATE continuously

WIN together

Focus here, multitask elsewhere

- Presentations & discussion
- Demo during breaks

