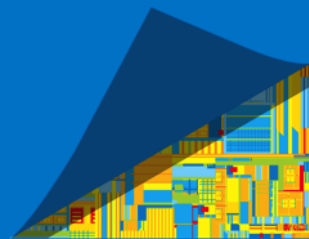




IA Based Acceleration In 5G UPF

Steve Liang, Jianwei Ma, Feng Yang

7th Sep. 2019



Legal Disclaimer

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or go to: <http://www.intel.com/design/literature.htm> Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, visit Intel Performance Benchmark Limitations

All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice.

, Intel, Intel logo, Intel Core, Intel Inside, Intel Inside logo, Intel Ethernet, Intel QuickAssist, Intel Flow Director, Intel Solid State Drives, Intel Intelligent Storage Acceleration Library, Itanium, Xeon, and Xeon Inside are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

64-bit computing on Intel architecture requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel® 64 architecture. Performance will vary depending on your hardware and software configurations. Consult with your system vendor for more information.

No computer system can provide absolute security under all conditions. Intel® Trusted Execution Technology is a security technology under development by Intel and requires for operation a computer system with Intel® Virtualization Technology, an Intel Trusted Execution Technology-enabled processor, chipset, BIOS, Authenticated Code Modules, and an Intel or other compatible measured virtual machine monitor. In addition, Intel Trusted Execution Technology requires the system to contain a TPMv1.2 as defined by the Trusted Computing Group and specific software for some uses. See <http://www.intel.com/technology/security/> for more information.

Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and, for some uses, certain platform software enabled for it. Functionality, performance or other benefits will vary depending on hardware and software configurations and may require a BIOS update. Software applications may not be compatible with all operating systems. Please check with your application vendor.

* Other names and brands may be claimed as the property of others.

Other vendors are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice. Copyright © 2015, Intel Corporation. All rights reserved.

INTEL'S NETWORK & EDGE EVOLUTION ENABLEMENT

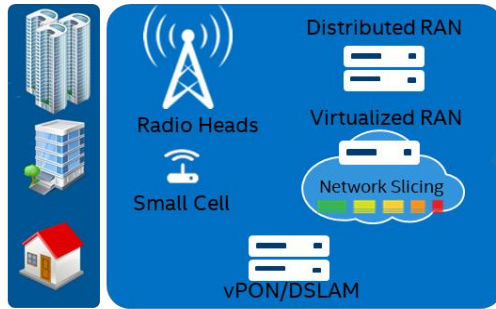
On Prem
Edge

Far Edge / Access

Near Edge

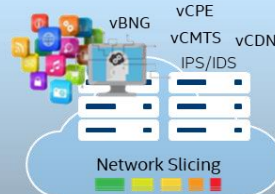
Core

Cloud / Data Center



Demand for Broad Range of Deployments

Next Generation Central Office



vEPC/5GCN

Router

Backbone

Network Slicing

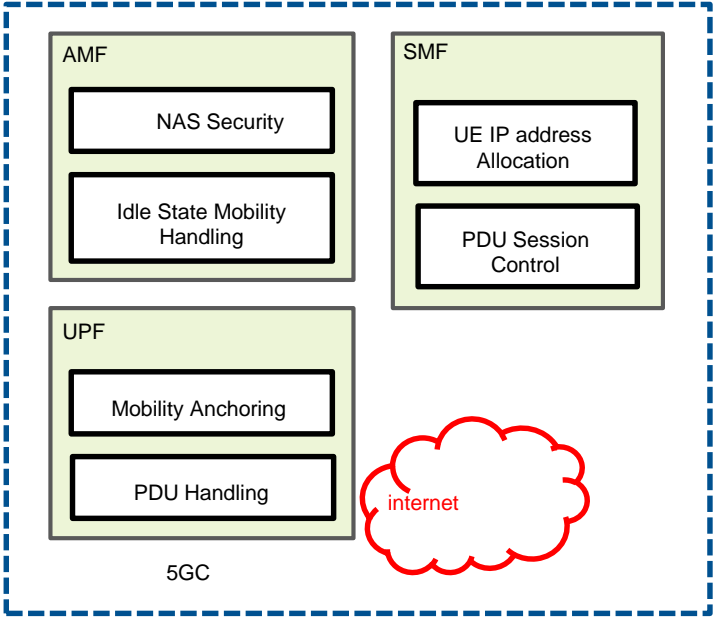
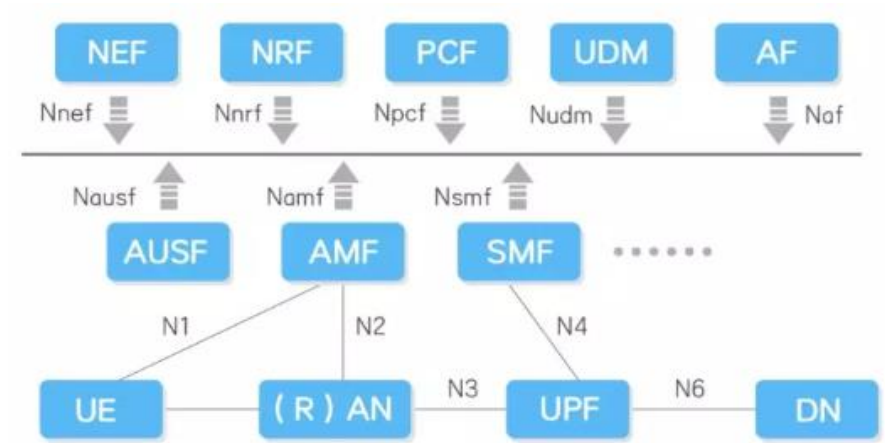
Demand for Cloud-Like Innovation



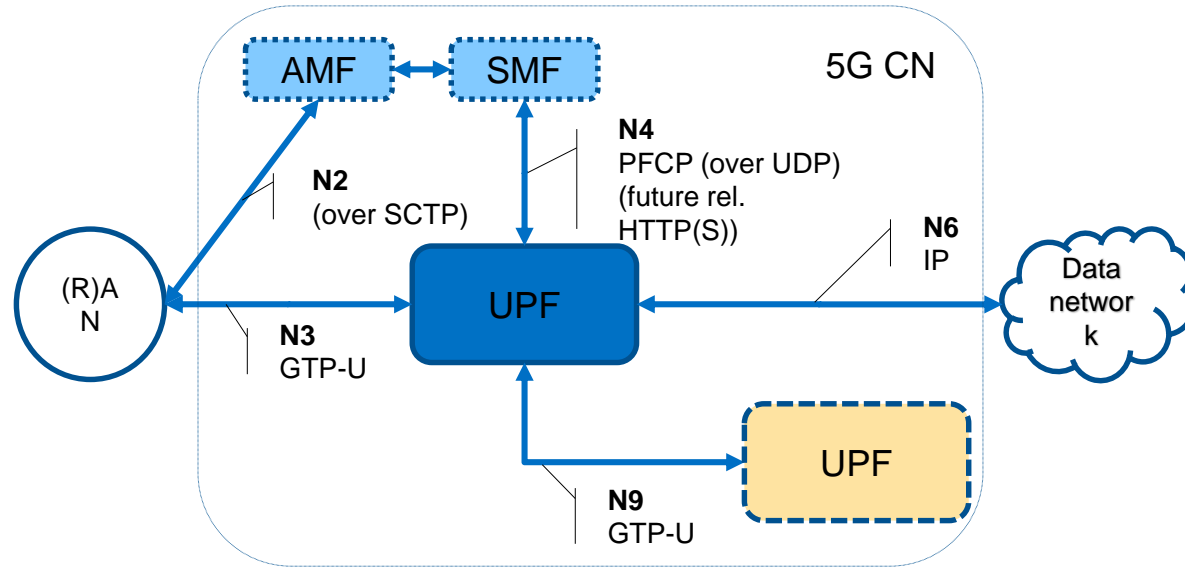
- Continued 4G & 5G traffic growth require significant increase in RAN & core capacity – maximize leverage of existing investments
- Virtualization of the 5G Core vs fixed function 5G Core appliances will be greater than 90% NFV
- Evolution to Cloud Platforms provide opportunity for cloud-like innovation: flexibility, scale & new revenue models

Intel brings together the products, ecosystem & influence to enable next generation Edge(s)

5G CN: ARCHITECTURE OVERVIEW



5G CN: UPF interfaces

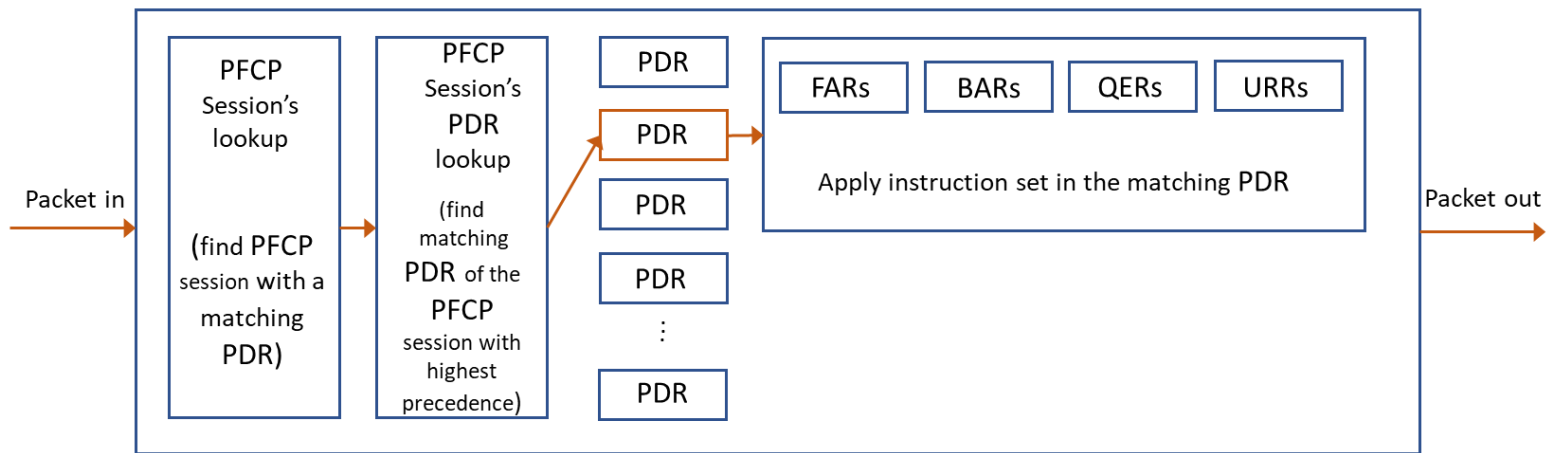


For N9 reference point: traffic received as GTP-U could have UL or DL encapsulated.

DL vs UL can be classified by **PDU Type** field of the **PDU SESSION INFORMATION** carried in GTP-U extension header of **PDU Session Container** type.

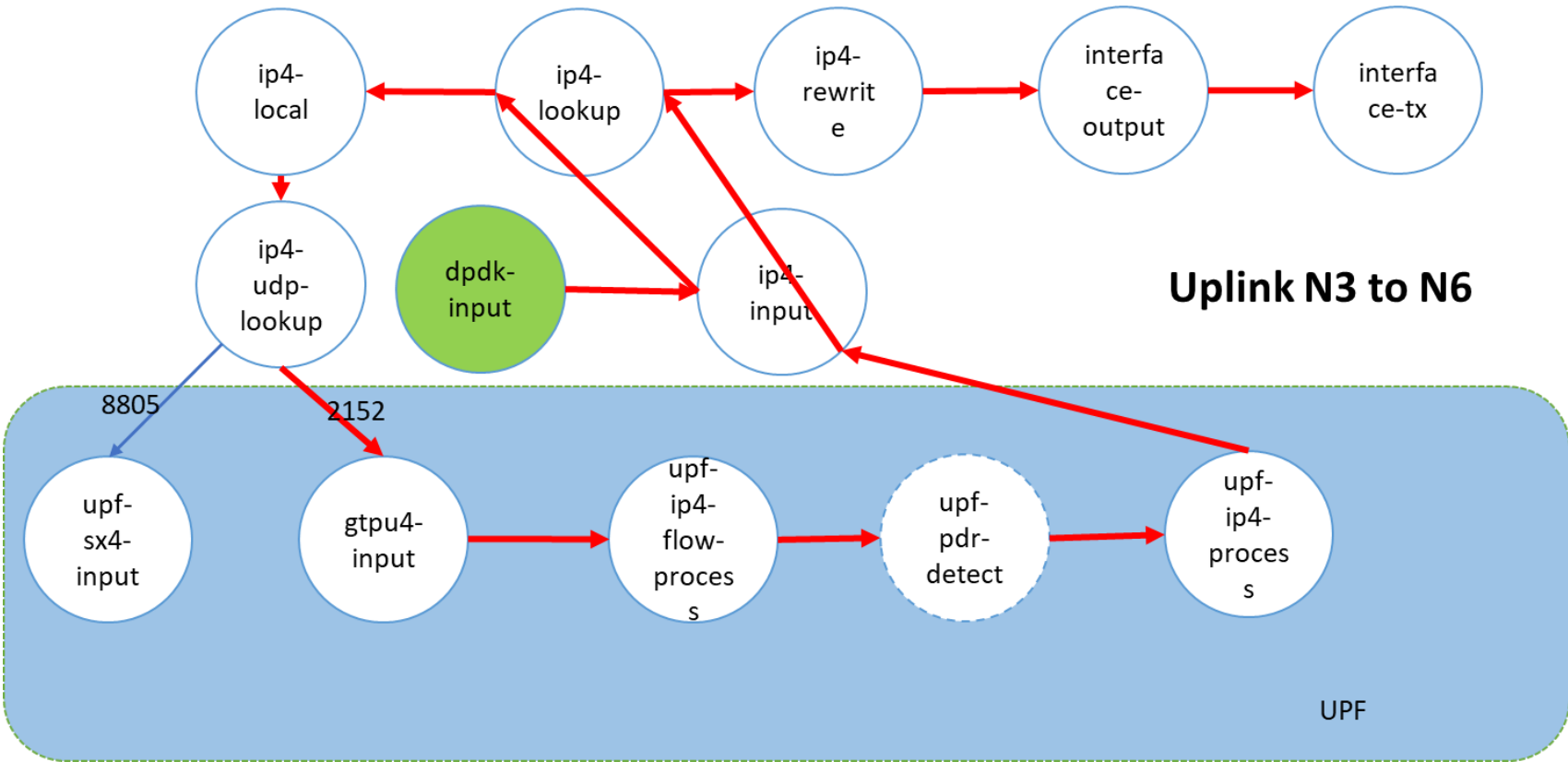
Need an ability to configure different inset (for RSS) for UL and DL packets

WHAT IS THE 5G USER PLANE FUNCTION (UPF)

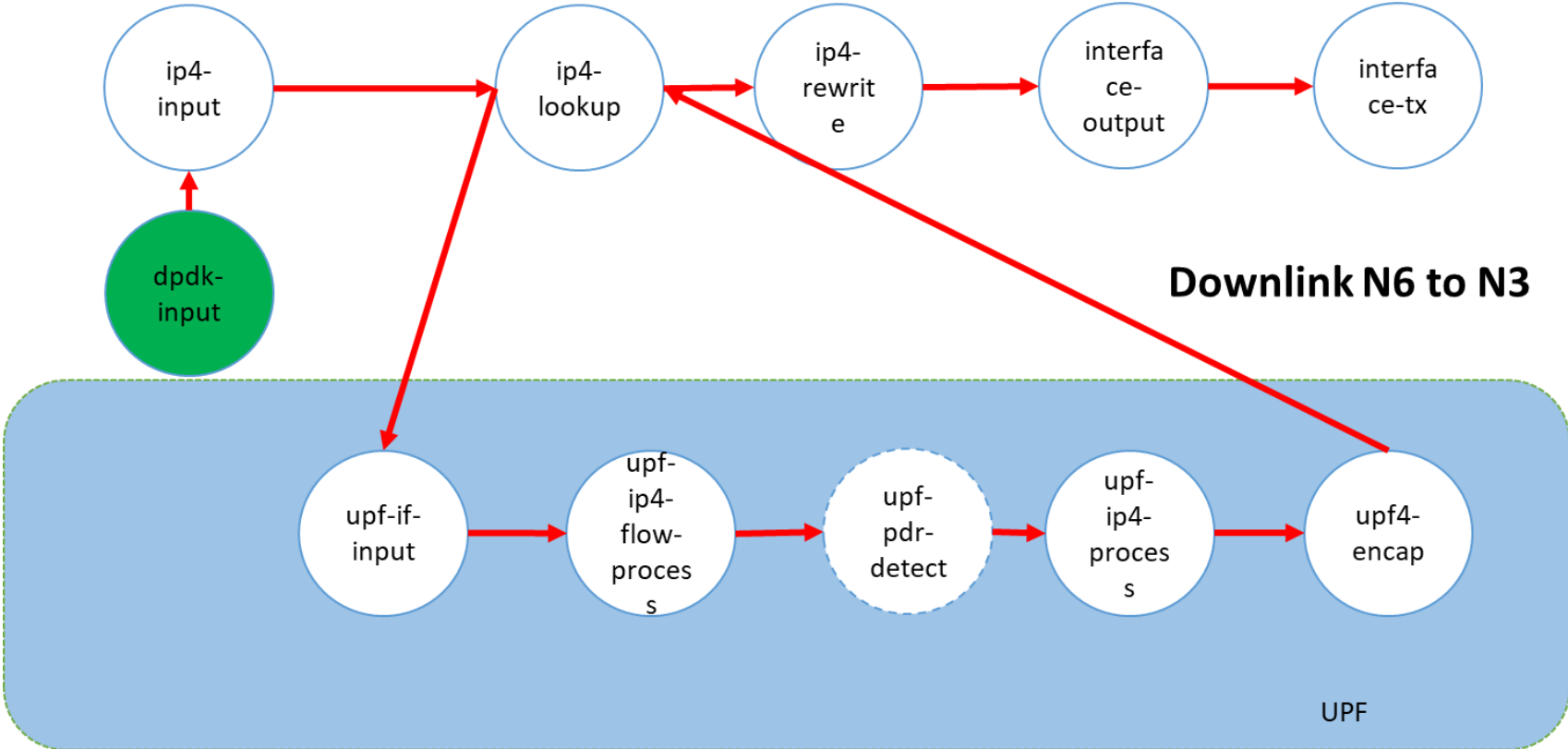


Packet processing flow in the User Plane Function (per 3GPP TS29.244)

UPLINK PIPELINE (VPP BASED RA)



DOWNLINK PIPELINE(VPP BASED RA)



IP Flows In Mobile Network

❑ Industry data <https://www.forbes.com/sites/forbestechcouncil/2019/02/28/what-are-elephant-flows-and-why-are-they-driving-up-mobile-network-costs/#2920b318407e>

- 3-min YouTube stream takes 20,000X more bandwidth than 3-min consuming Twitter
- 50% of all video will be consumed on mobile devices by 2020
- 3% of data sessions account for 70% of all traffic on mobile networks

❑ Data collected from real Packet Gateway on mobile network indicates

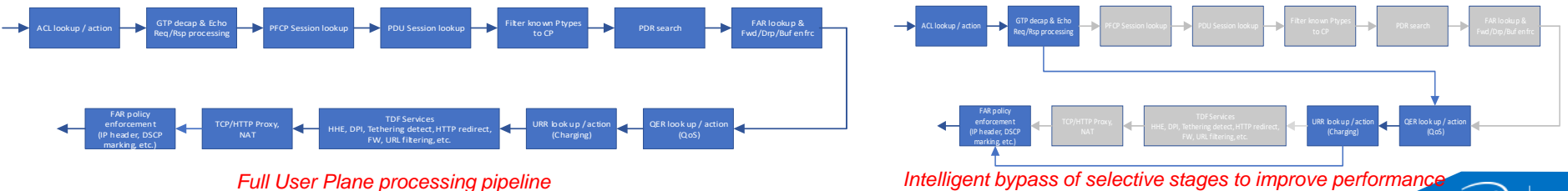
- More than 60% of IP flows have few # of packets in them (i.e. short durations flows)
- More than 70% of data carried over relatively smaller number, but longer duration IP flows

❑ Longer duration flows (that carry most data volume) need relatively lower processing overall

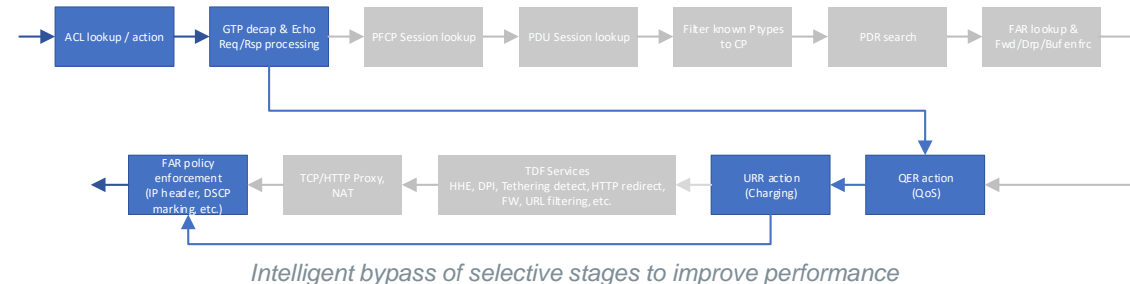
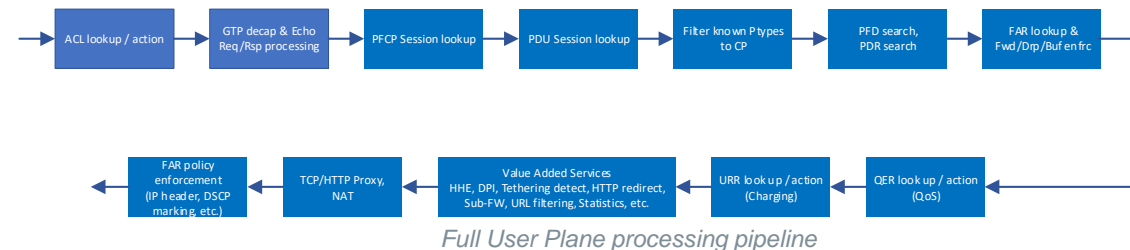
- Initial packets need full processing (e.g. DPI, security, etc.), subsequent packets of the flow can bypass most of the stages of User Plane processing – can be done effectively in software!
 - *Functionally implemented in Intel's internal 5G UPF stack, perf. testing 2H' 2019*

❑ Advantages

- No architectural challenges with packet ordering, Session-AMBR, QoS Flows – simplifies overall System Architecture while improving performance for IP flows that really dominate overall traffic



IP Flow processing – Flow Cache



- All IP flows start with full UPF processing in SW/VNF
- Long duration flows, as well as flows that have been validated (even short duration flows) can bypass full UPF processing stages, for faster processing of UP traffic
- SW/VNF maintains 5-tuple flow and its' policies in exact match table
- Every ingress packet (on N3,N4, N6, N9) is first looked up in this flow table to check the IP flow has been validated
- If IP flow has been fully validated (in prior packets of the flow), SW steers packets to stages that are only required for the IP flow (i.e. SW acceleration)
 - Includes flow aging for auto-removal, or re-insertion into flow table
- Implementation exercised in 5G UPF stack

5G UPF VNF Acceleration assists being defined & developed

❑ HW based traffic separation (GTP-U, PFCP, L2/everything else)

- Steer packets intelligently to different queues, minimize software exception path processing

❑ GTP-U Load distribution to cores based SW selectable approach

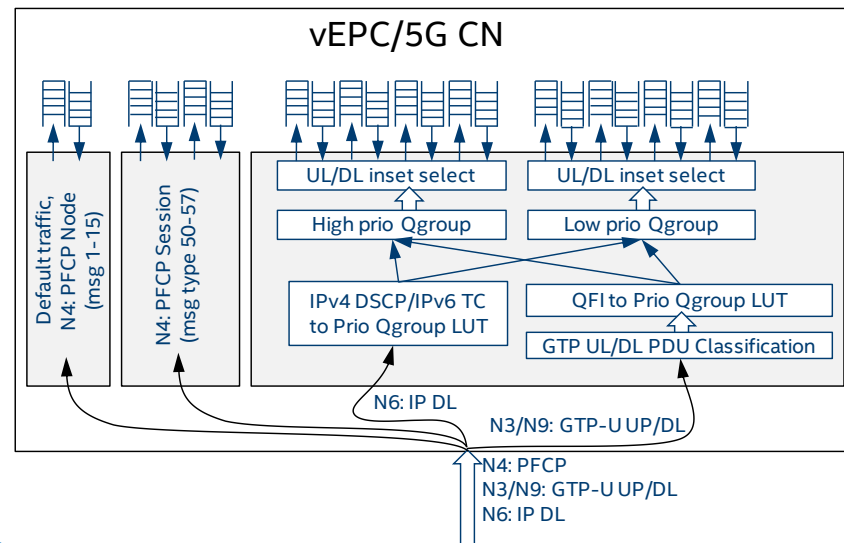
- Pin UEs to cores, or pin Flows to cores, steer packets of UE/Flows based on QoS parameters to different queues (URLLC, Video, VoLTE traffic separation)

❑ Control plane load distribution (in UPF)

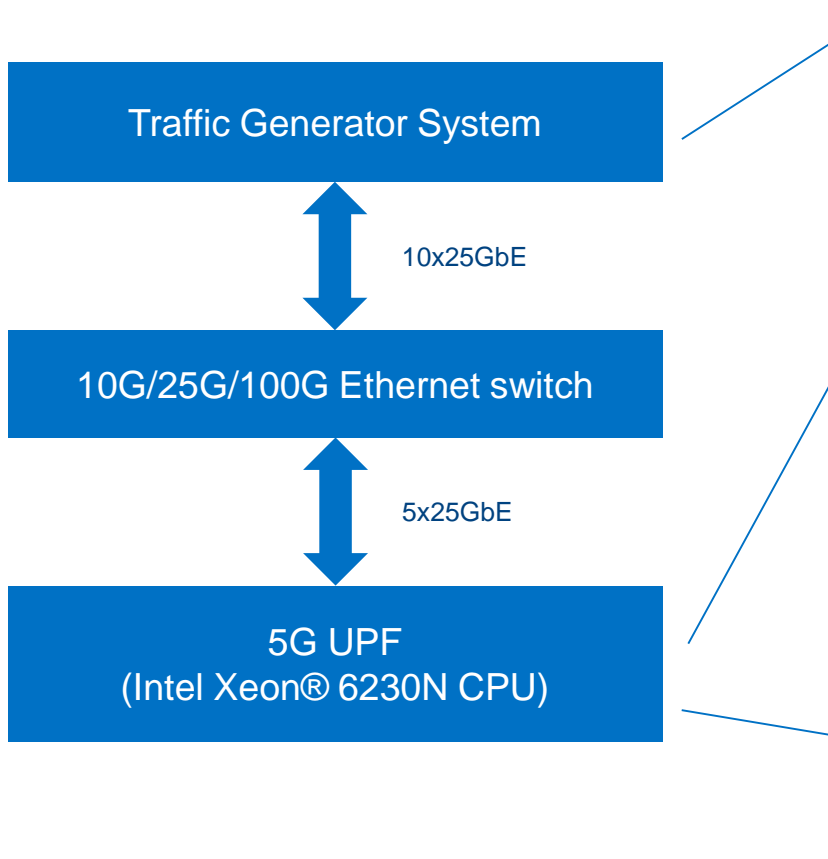
- Session Messages distribution, Node Messages to default queue

❑ HW based classification of packet types, for SW acceleration

- Provide SW with packet types detected in HW (e.g. IP→TCP, IP→UDP→GTP→IP→TCP, etc.)



Test Infrastructure & Performance



- Traffic generator for both UL and DL
- Includes emulation of gNB, 5G NR Ues
- Concurrent traffic in UL and DL, along with latency and jitter measurements

- 5G UPF on single CPU socket with 20 cores at 2.3 GHz
- 5x25GbE FVL ports with GTP-U DDP profile to steer UP data directly to worker cores
- 5G NR sessions setup into UPF without CP interaction for performance test measurements (same performance validated with CP interactions using SMF simulator)

Measured Performance:

- Throughput: 100 Gbps
- One-way packet latency: less 100 us.

VPP Runtime Info

```
root@ue28:/home/PRC-DEMO/UPF-VPP-1907-5UPF-1# ./vppctlx 1 show interface rx-placement
```

```
Thread 1 (vpp_wk_0):
```

```
node dpdk-input:
```

```
TwentyFiveGigabitEthernet86/0/0 queue 0 (polling)
```

```
Thread 2 (vpp_wk_1):
```

```
node dpdk-input:
```

```
TwentyFiveGigabitEthernet86/0/0 queue 1 (polling)
```

```
Thread 3 (vpp_wk_2):
```

```
node dpdk-input:
```

```
TwentyFiveGigabitEthernet86/0/0 queue 2 (polling)
```

```
Thread 4 (vpp_wk_3):
```

```
node dpdk-input:
```

```
TwentyFiveGigabitEthernet86/0/0 queue 3 (polling)
```

```
Thread 5 (vpp_wk_4):
```

```
node dpdk-input:
```

```
TwentyFiveGigabitEthernet86/0/0 queue 4 (polling)
```

```
Thread 6 (vpp_wk_5):
```

```
node dpdk-input:
```

```
TwentyFiveGigabitEthernet86/0/0 queue 5 (polling)
```

```
Thread 7 (vpp_wk_6):
```

```
node dpdk-input:
```

```
TwentyFiveGigabitEthernet86/0/0 queue 6 (polling)
```

```
Thread 8 (vpp_wk_7):
```

```
node dpdk-input:
```

```
TwentyFiveGigabitEthernet86/0/0 queue 7 (polling)
```

```
root@ue28:/home/PRC-DEMO/UPF-VPP-1907-5UPF-1# ./vppctlx 1 show runtime | grep dpdk-input
```

dpdk-input	polling	25028647382	20502925940	0	4.85e2
dpdk-input	polling	25826962852	20507088926	0	4.93e2
dpdk-input	polling	25674271125	20566726574	0	4.88e2
dpdk-input	polling	25724936841	20490050768	0	4.93e2
dpdk-input	polling	25043555592	20502838796	0	4.87e2
dpdk-input	polling	25610765155	20523222316	0	4.88e2
dpdk-input	polling	25774168228	20506635008	0	4.90e2
dpdk-input	polling	25515072566	20506328792	0	4.93e2

Trex Latency Measurement

Latency Statistics (usec)

PG ID	11	21	31	41	51
TX pkts	28790582	28790582	28790582	28790582	28790588
RX pkts	20775301	19435620	20611268	20164305	16504834
Max latency	302	249	293	334	283
Avg latency	140	145	136	139	126
-- Window --					
Last max	191	192	185	181	164
Last-1	199	206	192	203	180
Last-2	183	213	175	191	166
Last-3	189	190	180	182	176
Last-4	190	190	181	188	177
Last-5	192	194	173	200	243
Last-6	192	188	182	182	173
Last-7	181	201	183	195	178
Last-8	184	210	187	190	169
Last-9	195	199	183	189	283
Last-10	195	199	183	189	283
Last-11	197	200	188	197	168
Last-12	192	205	212	190	167
Last-13	200	192	181	195	166

Jitter	7	17	5	7	7

Trex Throughput Measurement

Port Statistics

port	0	1	2	3	total
owner	root	root	root	root	
link	UP	UP	UP	UP	
state	TRANSMITTING	TRANSMITTING	TRANSMITTING	TRANSMITTING	
speed	25 Gb/s	25 Gb/s	25 Gb/s	25 Gb/s	
CPU util.	36.8%	36.8%	37.1%	37.1%	
--					
Tx bps L2	5.51 Gbps	5.50 Gbps	5.50 Gbps	5.51 Gbps	22.02 Gbps
Tx bps L1	5.68 Gbps	5.68 Gbps	5.67 Gbps	5.68 Gbps	22.71 Gbps
Tx pps	1.08 Mpps	1.08 Mpps	1.07 Mpps	1.08 Mpps	4.30 Mpps
Line Util.	22.71 %	22.70 %	22.70 %	22.71 %	

Rx bps	16.51 Gbps	16.50 Gbps	16.50 Gbps	16.51 Gbps	66.02 Gbps
Rx pps	3.22 Mpps	3.22 Mpps	3.22 Mpps	3.22 Mpps	12.89 Mpps

opackets	13414761217	13392180858	13373143017	13373660030	53553745122
ipackets	38121254249	38041545237	38005205868	38003901454	152171906808
obytes	8584398954200	8569948843092	8557765888884	8558097405536	34270211091712
ibytes	24396607764584	24345611939270	24322327159256	24321496143926	97386043007036
opackets	13.41 Gpkts	13.39 Gpkts	13.37 Gpkts	13.37 Gpkts	53.55 Gpkts
ipackets	38.12 Gpkts	38.04 Gpkts	38.01 Gpkts	38.00 Gpkts	152.17 Gpkts
obytes	8.58 TB	8.57 TB	8.56 TB	8.56 TB	34.27 TB
ibytes	24.40 TB	24.35 TB	24.32 TB	24.32 TB	97.39 TB

oerrors	0	0	0	0	0
ierrors	0	0	0	0	0

5G UPF Performance (Reference Only)

- 5G UPF implemented as graph nodes over VPP infrastructure
- Includes all functionalities
 - IP, UDP, GTP (with encap/decap), PFCP (CP interfaces), PDR detection, FAR, QER, URR based policy enforcements
 - Features under development includes DPI, URLLC, etc.
- Intel Xeon® 6230N CPU (single socket) performance measurements for following scenario:

• Number of 5G NR subscribers:	50K
• Number of PDU Sessions per subscribers:	1
• Uplink to Downlink TPT ratio:	1:3
• Average packet size:	~600 Bytes
• Total packet rate:	~20 MPPS
• Aggregate Throughput:	100 Gbps
• Average Latency:	150 us

