P4和Tofino可编程交换芯片引领网络创新

intel®

Developer Ecosystem

- **Packet Headers**

```
header ethernet_h {
    bit<48>     dstAddr;
    bit<48>     srcAddr;
    bit<16>     etherType;
}
```

- **Match-Action Table**

```
table dmac {
    key = {
        ingress_metadata.bd : exact;
        ethernet.dstAddr    : exact;
    }
    actions = {
        dmac_hit;
        dmac_miss;
        dmac_redirect_to_cpu;
    }
    default_action = dmac_miss;
    size = 131072;
}
```

- **Actions**

```
action dmac_hit(bit<9> egress_port) {
     ig_intr_md_for_tm.ucast_egress_port = egress_port;
     l2_metadata.same_if_check =
             ig_intr_md.ingress_port ^ egress_port;
}
```

P4 Features

- Open Spec, Compiler, Test Frameworks, and more
- Protocol Independent
- Target Independent

Strong community

- 4000+ developers trained and growing
- 100+ member organizations
- Expanding across the globe

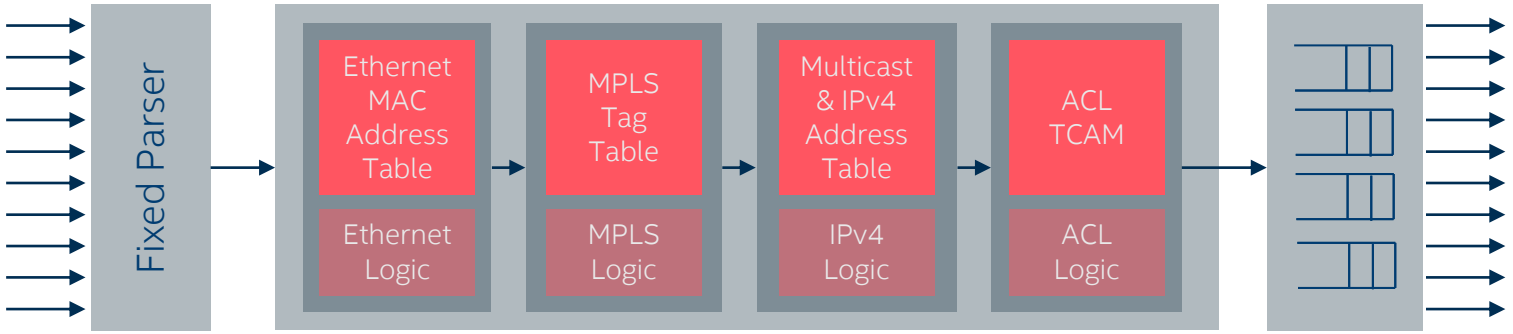
Accelerating adoption

- Expanding adoption by new vendors
- Switches, NICs, FPGA, Software Data Planes

P4: Programming Protocol-independent Packet Processors

https://p4.org/

P4可编程芯片流水线调整的价值



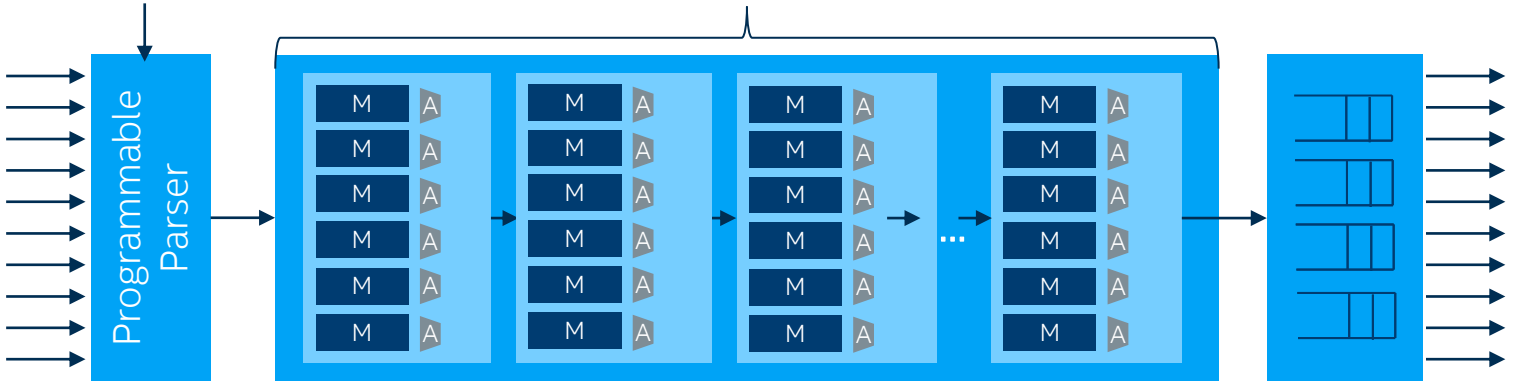
功能固化

− 处理流程不可改变
− 难以网络可视化

传统芯片功能和表格规格固化，无法优化并使用低效

用户定义报文格式

用户通过P4代码指定表和大小需求以及数据包处理功能



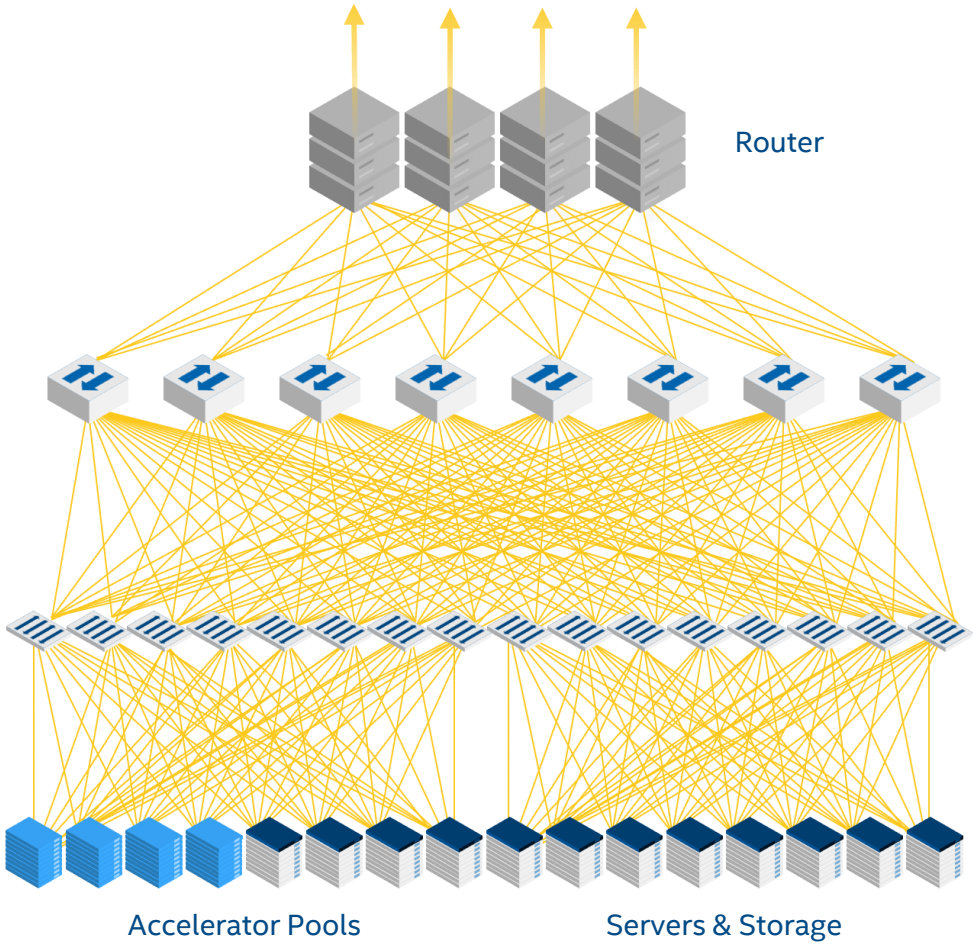
可编程

+ 处理流程基于用户需要优化
+ 实时网络可视化
+ 按需随应用场景调整

流水线完全根据应用场景优化

Data Center Fabric Strategy

Unleashing the performance of compute at scale through innovations in end-to-end networking



intel. Si PHOTONICS

intel. TOFINO

intel. IPU

intel. ETHERNET

intel. XEON

intel. AGILEX

intel. STRATIX

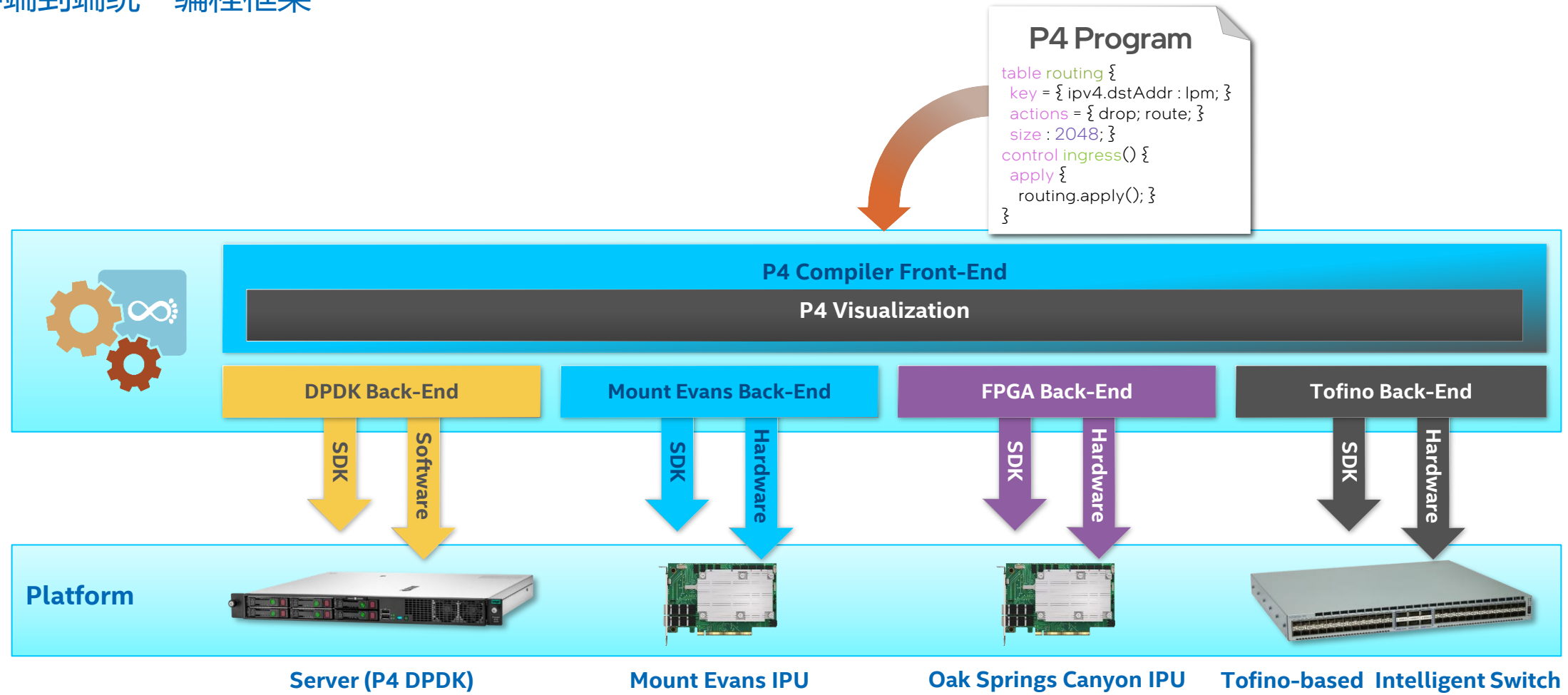
intel. eASIC

habana

Xe

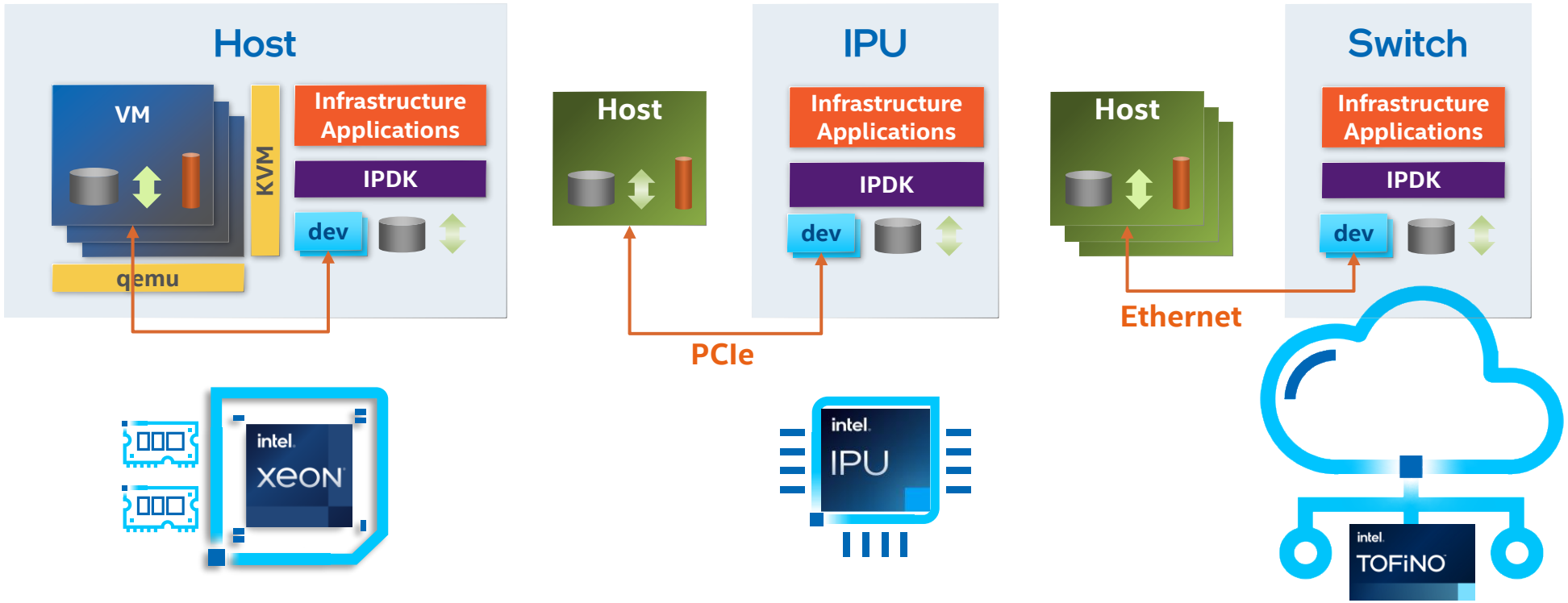
IPDK: Infrastructure Programmer Development Kit

P4端到端统一编程框架



IPDK.io

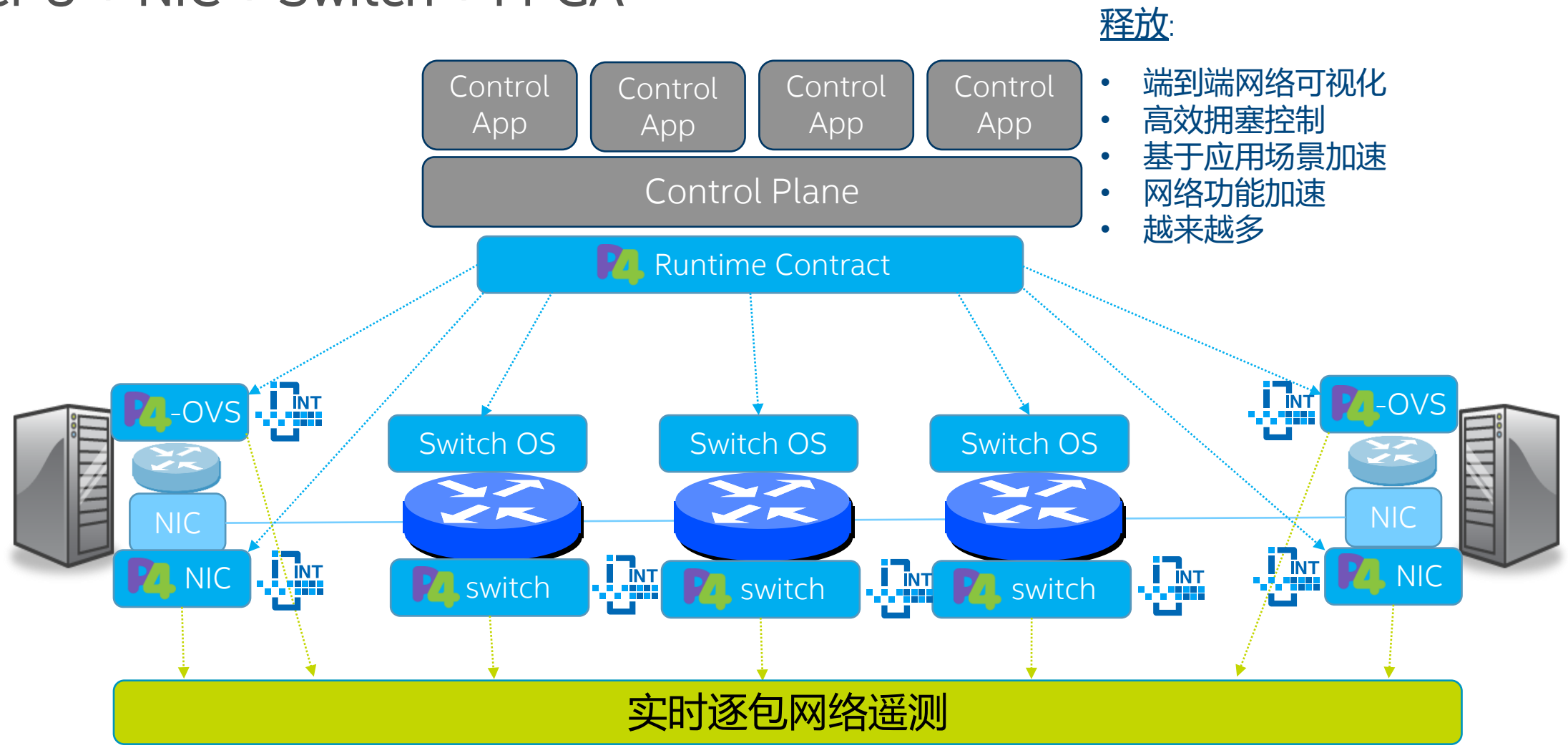
ipdk Infrastructure Programmer Development Kit



https://ipdk.io/

端到端P4可编程

CPU + NIC + Switch + FPGA

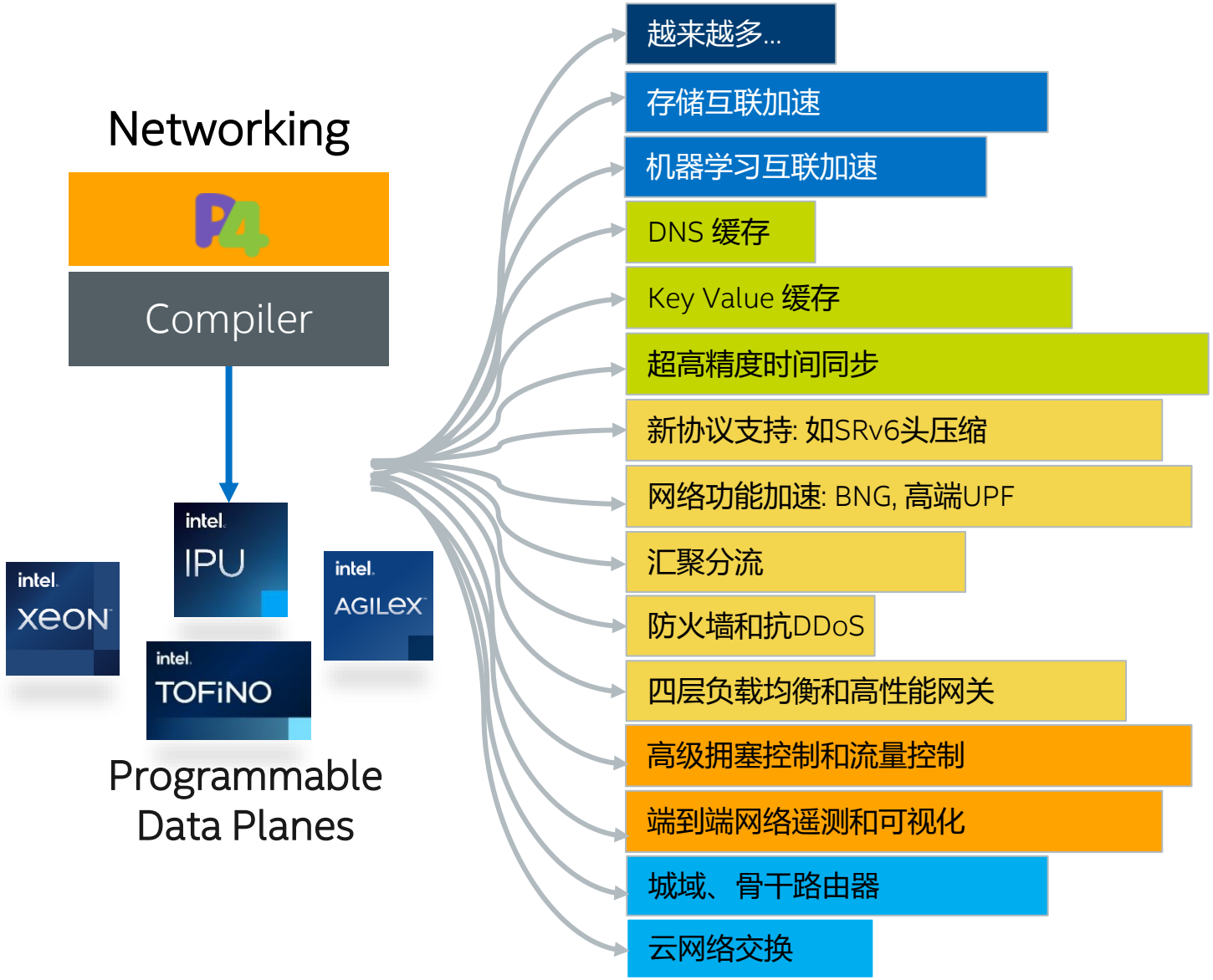


释放:

- 端到端网络可视化
- 高效拥塞控制
- 基于应用场景加速
- 网络功能加速
- 越来越多

跨 CPUs, NICs, Switches, and FPGAs赋能P4可编程

P4可编程 = 被优化的应用场景爆发式增长



Tofino Switching Silicon Family

Tofino

Programmable Ethernet
Switch ASIC w/ **28Gbps** SerDes

16nm Process Node

Optimized for
100GbE / 50GbE / 40GbE / 25GbE / 10GbE

compute connectivity
6.4 Tbps

1.8 Tbps

2.0 Tbps

3.2 Tbps

Tofino 2

Programmable Ethernet
Switch ASIC w/ **56Gbps** SerDes

7nm Process Node

Optimized for
400GbE / 200GbE / 100GbE / 50GbE / 25GbE / 10GbE

compute connectivity
12.8 Tbps

6.4 Tbps

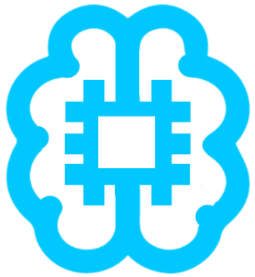
8.0 Tbps

intel innovation

Announcing

Intel® Tofino™ 3

Intelligent Fabric Processor



Intelligence

P4 programmable
AI/ML acceleration
Highly secure solution

Performance

Up to 25.6 Tbps
112G/56G SerDes
Power-optimized use cases

Visibility & Control

Edge-to-cloud real-time telemetry
Enhanced congestion control
Self-healing network capabilities

Features subject to change

Opening Tofino's P4 Target Architecture

Unleashing the power of network programmability by making Tofino the first open, programmable Ethernet switch ASIC

End users can now openly publish the data plane and control plane code for Tofino!

Accelerating innovation in the networking industry

Enabling network owners and operators to customize and build new applications for their network infrastructures

Encouraging collaboration among developers and researchers to foster the growth of the P4 ecosystem

https://github.com/barefootnetworks/Open-Tofino

How Is Programmability Used?

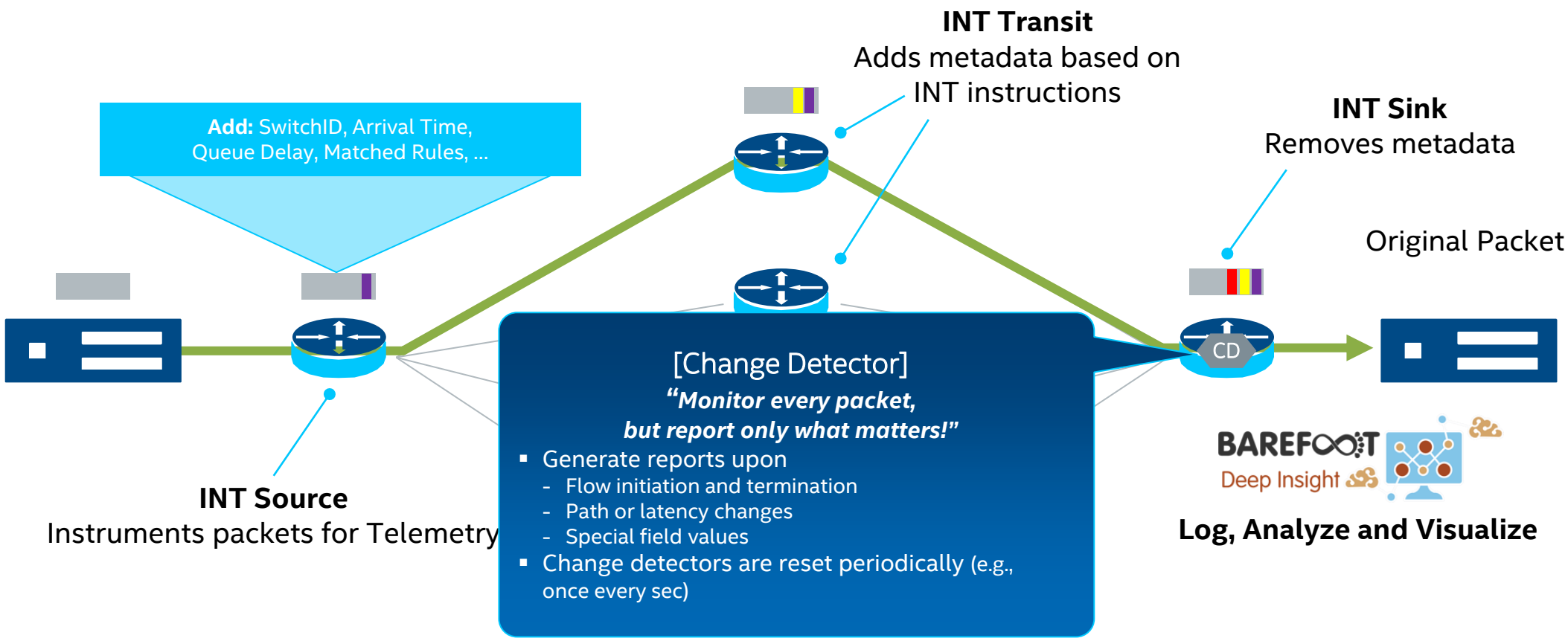
Data-plane Telemetry and Real-time Control

The Network Should Answer These Questions

1. “Which path did my packet take?”
2. “Which rules did my packet follow?”
3. “How long did it queue at each switch?”
4. “Who did it share the queues with?”

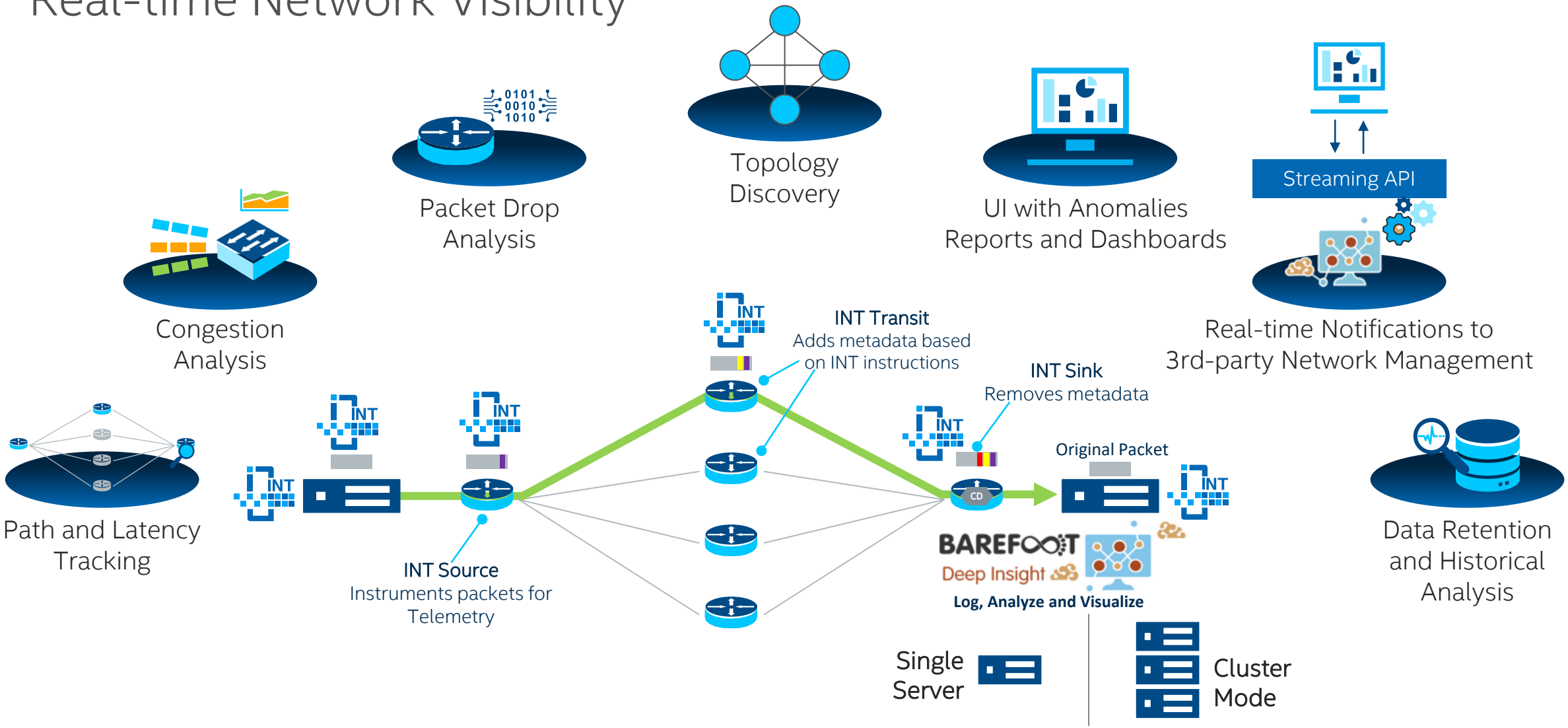
Tofino™ + Deep Insight™ can answer all four questions.
At full line rate. Without generating any additional packets!

Flow Reporting: INT-MD Mode



In-band Network Telemetry (INT) & Deep Insight (DI)

Real-time Network Visibility

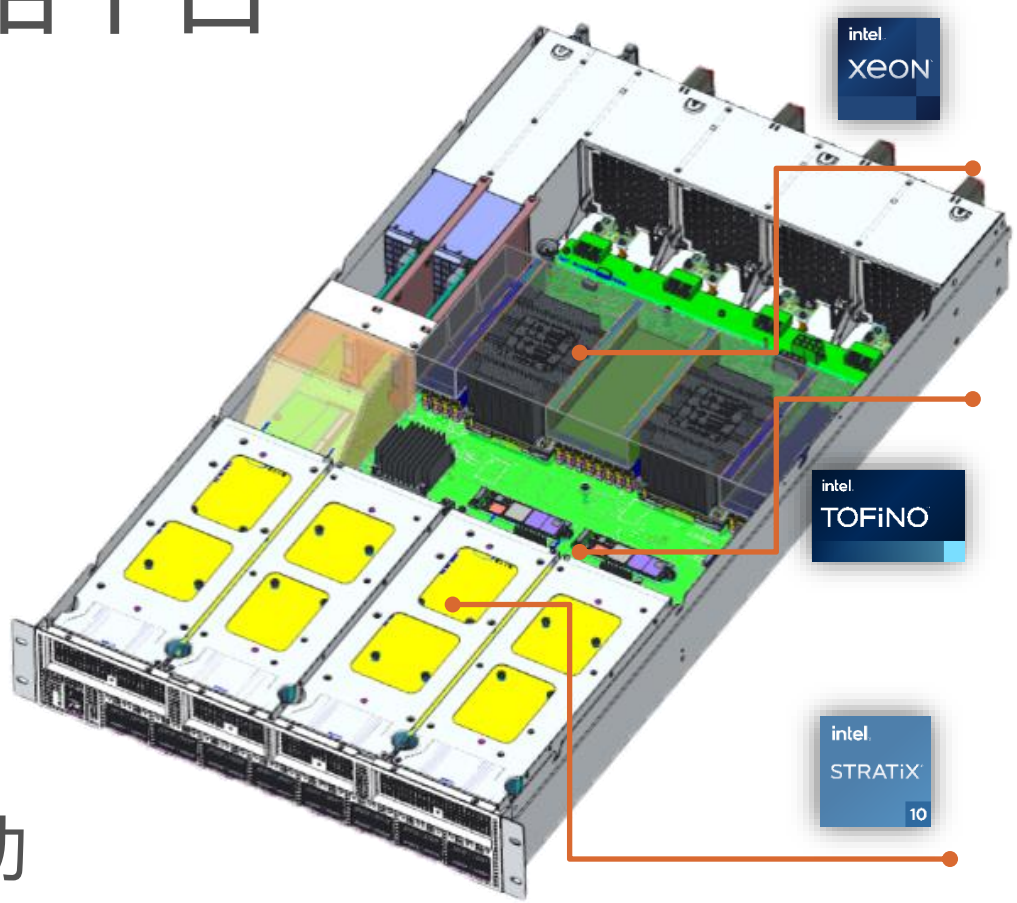


How Is Programmability Used?

超融合可编程网络平台

超融合可编程网络平台

- 组成
  - 服务器级双路至强CPU
  - Tofino交换芯片
  - 可选配FPGA模块
- 亮点
  - 全可编程架构
  - 大表项、大缓存
  - 高性能、低延时、低抖动
  - 云网融合、边缘计算、算网融合
    - ToR, Gateway, vRouter, L4 LB, Security, etc.



CPU Module
- 2x Intel Xeon SP
- DDR Memory

Switch Module
- 1x Tofino
- 32x 100GE (External)
- 32x 100GE (to FPGA)

FPGA Module
- 4x Stratix 10
- HBM
- DDR Memory

Intel's Commitment
to Network Developer Community

Leadership Hardware

intel. TOFiNO

intel. Si PHOTONiCS

intel. IPU

intel. ETHERNET

Partner to Create Industry Standards

SPDK

P4

DPDK

SONiC

ipdk Infrastructure Programmer Development Kit

OPENFABRICS ALLIANCE

Engage with Developers

Thank You!