Course Name: Analog Electronics

Course Number and Section: **14:332:463:01**

Project: Analog Electronics Course Project

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Abstract:

This project focuses on designing and analyzing a two-stage CMOS operational amplifier (op-amp) catering to the specific requirements of low-power applications. The op-amp is a critical component in many electronic systems, and our goal is to meet critical design specifications:

- Architecture: two-stage op-amp
- Low-frequency voltage gain > 60 dB
- Slew rate > 100 V/μs.
- Unity-gain bandwidth (GB) > 50 MHz
- VDD = 1.8 V
- ICMR: 0.7 V to 1.4 V
- Load capacitance (C_L) = 1 pF

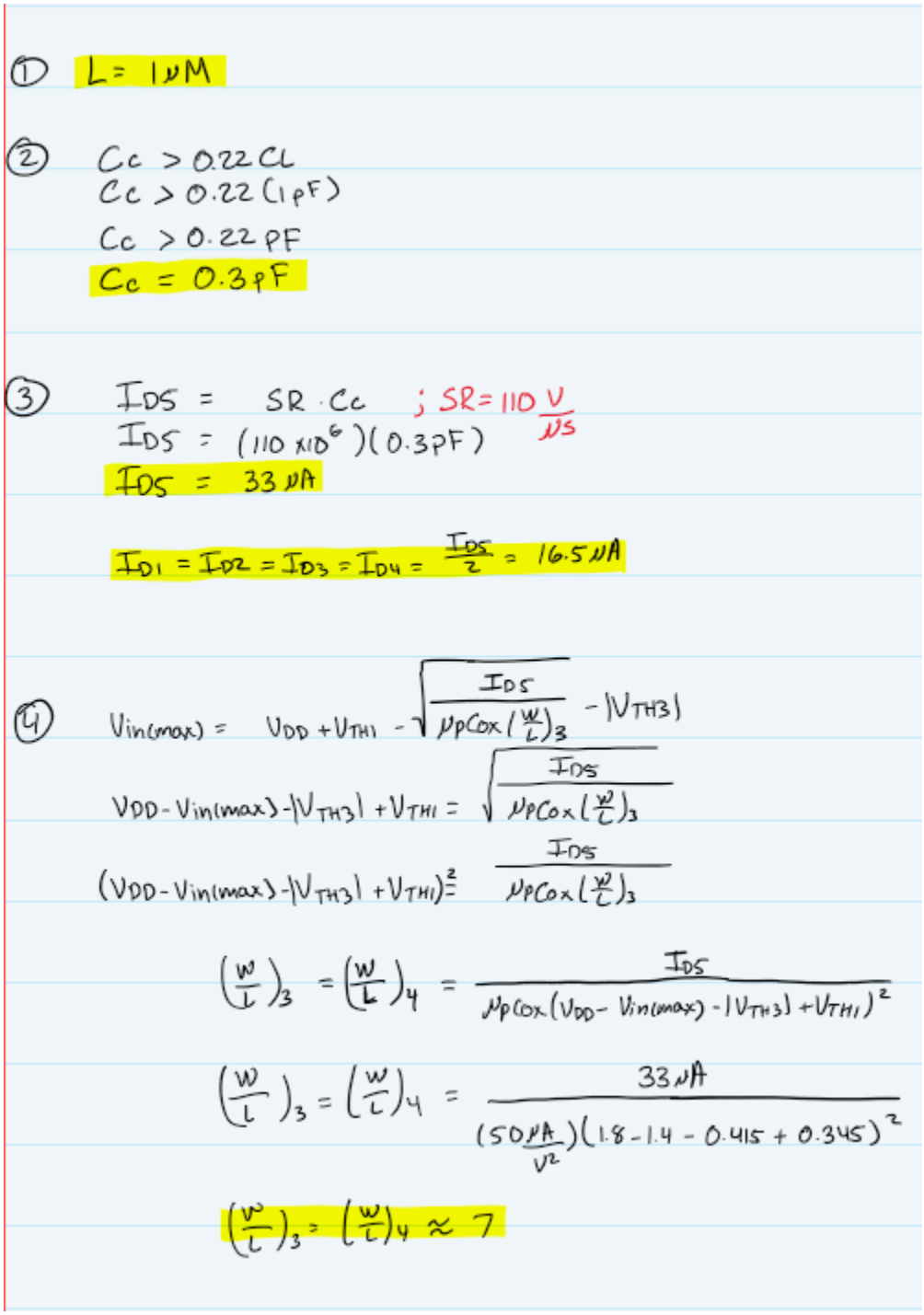
Introduction:

Operational amplifiers are pivotal in electronic circuits, serving as the cornerstone for various applications such as signal processing and amplification. In this project, we design a two-stage CMOS op-amp tailored for low power consumption, aiming to balance performance and energy efficiency.

In our pursuit of an optimized two-stage amplifier, we employ a set of meticulously crafted equations to derive the width/length ratios of the transistors, crucial parameters that underpin the design criteria. These equations are the blueprint for achieving the desired performance characteristics, ensuring a harmonious balance between various factors influencing the operational amplifier's functionality.

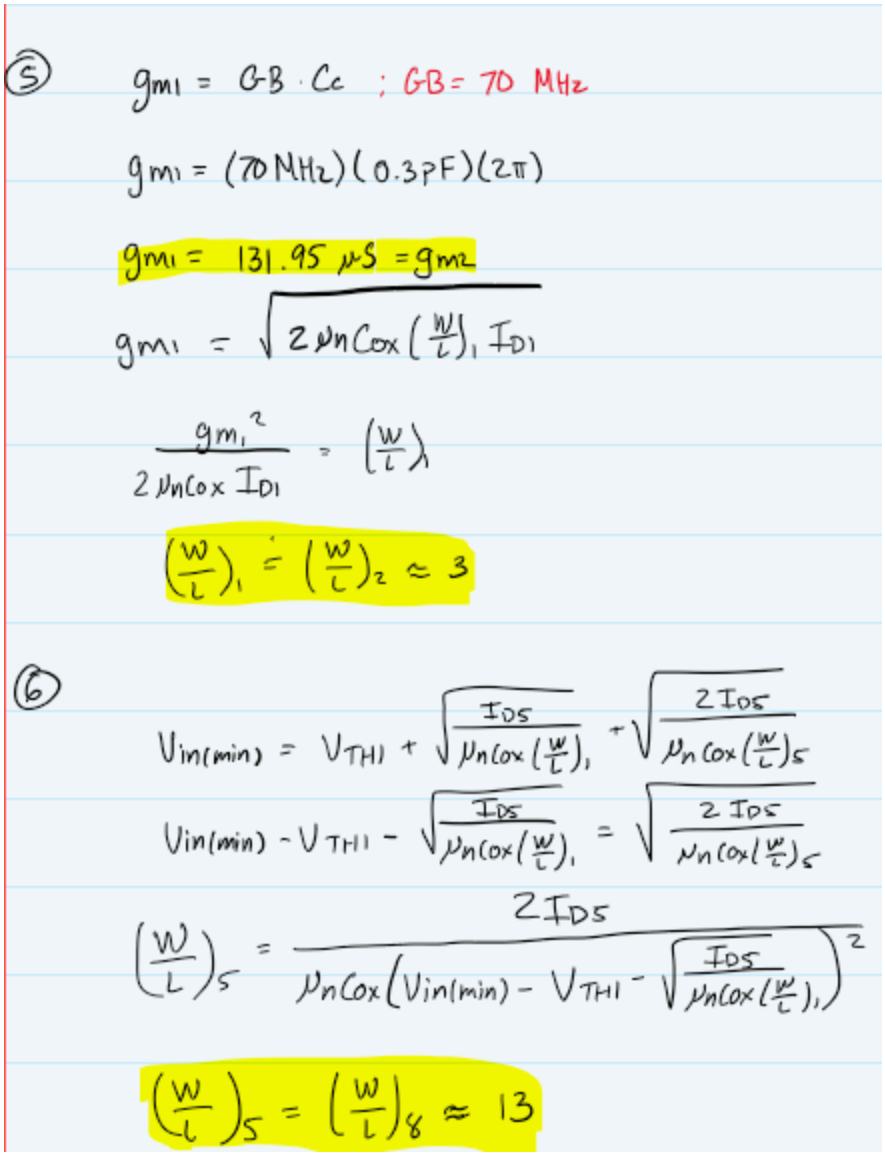
Width-to-length (W/L) ratios in the context of transistor design in integrated circuits, such as CMOS (Complementary Metal-Oxide-Semiconductor) technology, are crucial parameters that define the physical dimensions of the transistors. The W/L ratio refers to the transistor's channel width (W) ratio to its channel length (L). These dimensions play a pivotal role in determining the electrical characteristics and performance of the transistor.

Hand Calculations:

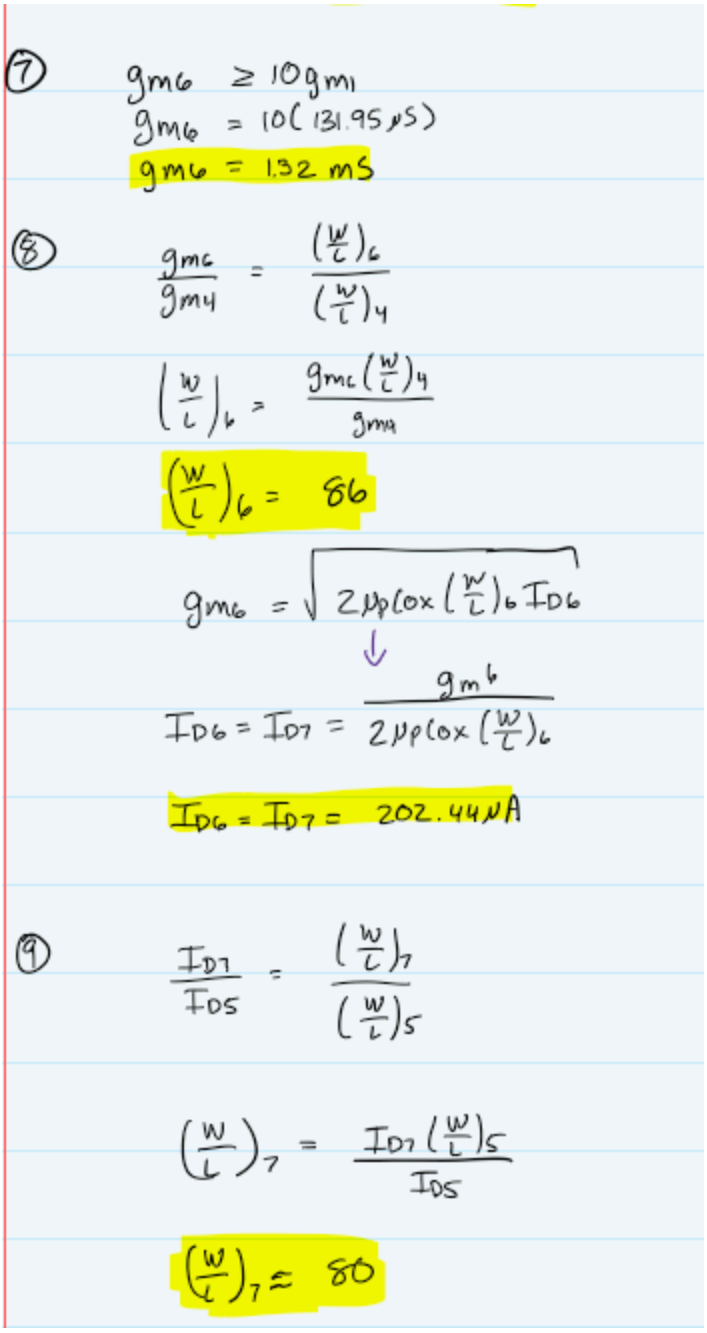


Notice that we are going with L = 1uM for our channel length. Initially, we went with 180nM, the default value in simulations. However, when we did our AC analysis, we found that this restricted the maximum Low-Frequency gain we could achieve. After experimenting with fine-tuning parameters, we found that increasing channel length increased our gain from 41 dB

to > 60 dB. In addition, notice MOSFET 3 and 4 are current mirrors; hence, their ratios will be the same.



Notice that ID5 is the current flowing through MOSFET 1 and 2 combined. In addition, Since MOSFETs 1, 2, 3, and 4 form a differential amplifier, MOSFET 1 and 2 will have the same ratios. In addition, notice that MOSFETs 5 and 8 form a current mirror where ID5 is the current that needs to be replicated, hence why IREF = ID5. Also, notice that M6 and M7 form a gain stage. This is responsible for amplifying the gain.



Note: It's important to note that the (W/L) ratios are rounded. Initially, when we used exact numbers to solve for ratios, we discovered that our (W/L) ratio for 5 blew up to >100 digits. This is likely because if the (W/L) ratio of 1 is small, close to 1, it will blow up to large numbers. However, if it's greater than 1, it will give us desirable numbers.

In addition, to avoid tedious work from repeatedly trying different Slew rate values, gain bandwidth values, and Cc values, we wrote a MATLAB script that solves W/L ratios for us.

MATLAB:

```
upcox = 50 * 10^-6;
uncox = 250 * 10^-6;
vth1 = 0.345;
vth3 = 0.415;
vdd = 1.8;
vss = 0;
vinmax = 1.4;
vinmin = 0.7;
Cl = 1*10^-12;
SR = 110 / 10^-6;
GB = 70 * 10^6;
%1
Cc = 0.3 * 10^-12;
%2
ID5 = SR * Cc;
%3
ratio3 = ID5/(upcox*(vdd-vth3-vinmax+vth1)^2);
ratio3 = ceil(ratio3);
ratio4 = ratio3;
%4
gm1 = GB * 2 * pi * Cc;
ratio1 = (gm1)^2/(uncox*ID5);
ratio1 = ceil(ratio1);
ratio2 = ratio1;
%5
VDS5 = vinmin - vss - sqrt(ID5/(uncox*ratio1)) - vth1;
ratio5 = ceil((2*ID5)/(uncox*(VDS5)^2));
ratio8 = ratio5;
%6
gm6 = 10 * gm1;
gm4 = sqrt(2*(ID5/2)*upcox*ratio4);
ratio6 = ratio4*(gm6/gm4);
ratio6 = ceil(ratio6);
%7
ID6 = (gm6)^2/(2*upcox*ratio6);
ID7 = ID6;
%8
ratio7 = (ID7/ID5) * ratio5;
ratio7 = ceil(ratio7);
%9
VDS7 = sqrt((2*ID7)/(uncox*ratio7)) %output swing
Voutmin = VDS7 + vss
Voutmax = vdd - sqrt((2*ID6)/upcox*ratio6)
%10
pdiss = (vdd+vss)*(ID6+ID5);
```

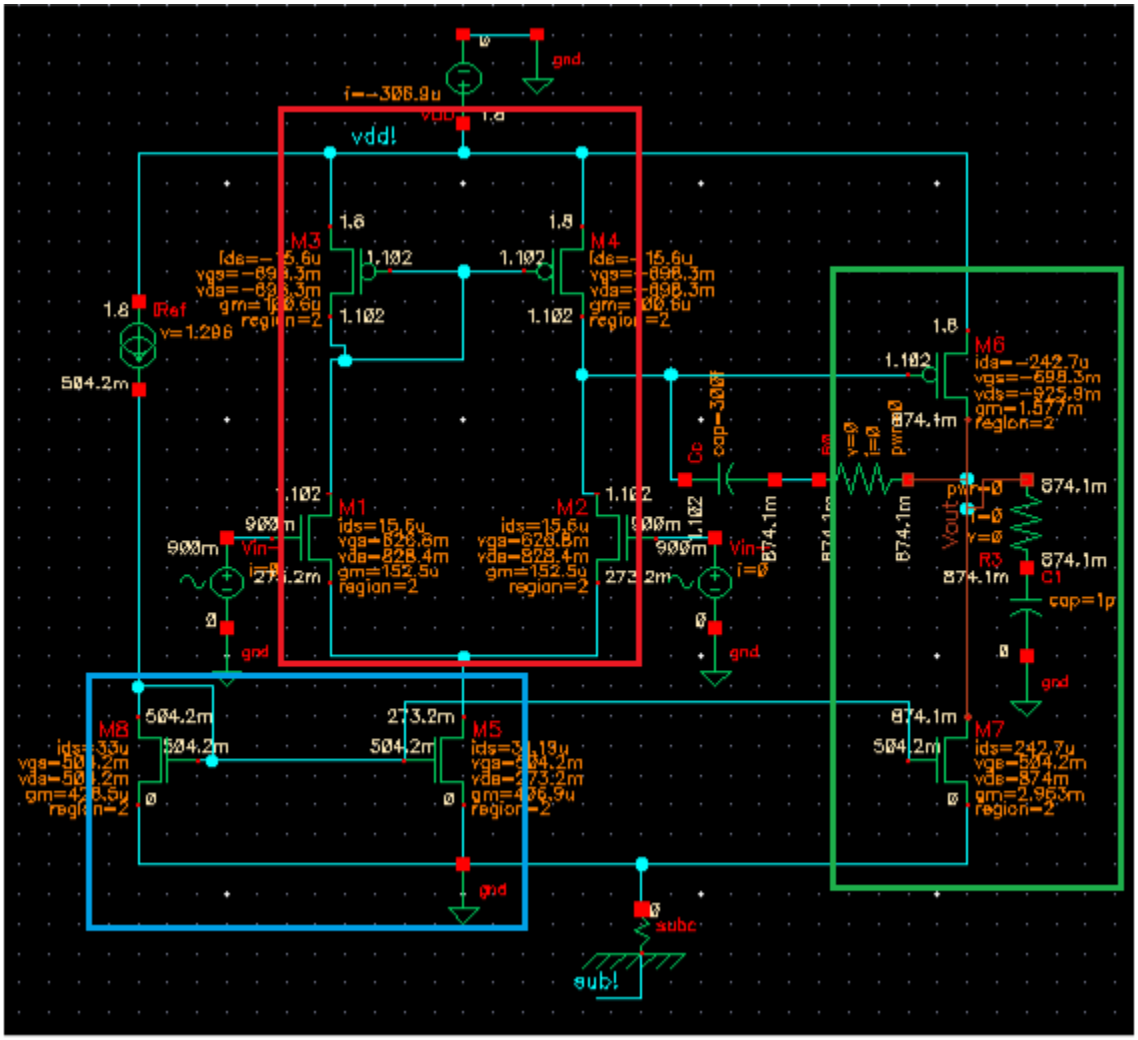
```
%11
Av = 2*gm1*gm6 * (1/(ID5*(0.04+0.05))) * (1/(ID6*(0.05+0.04)))
transistors = ["M1", "M2", "M3", "M4", "M5", "M6", "M7", "M8]';
ratios = [ratio1, ratio2, ratio3, ratio4, ratio5, ratio6, ratio7, ratio8]';
results = table(transistors, ratios)
disp("ID5: ")
disp(ID5)
disp("Cc: ")
disp(Cc)
```

The hand calculations and MATLAB script result in the following results:

```
  8×2 table

    transistors    ratios
    ___________    ______

       "M1"           3
       "M2"           3
       "M3"           7
       "M4"           7
       "M5"          13
       "M6"          86
       "M7"          80
       "M8"          13

ID5:
    33.0000e-006

Cc:
   300.0000e-015
```

Note that M6 is modified to 105. This is because when we were doing the simulation, putting exact values from our calculations resulted in a very low output node voltage of around 100-300 mV. In contrast, simulation 1 asks that we achieve an output voltage 0.9V. Hence, increasing the M7 ratio gave us a much higher voltage of approximately 0.9V. This will be explained in much more detail in the following sections.

Here is an overview of parts of this amplifier:



A two-stage operational amplifier (op amp) typically consists of three main building blocks: a differential amplifier, a current mirror, and a gain stage. Each component aims to achieve the op-amp's overall amplification and performance goals. Let's break down the responsibilities of each:

1. Differential Amplifier (RED):

Purpose: The differential amplifier is the first stage of the op-amp and is responsible for handling the input signals.
Operation: It amplifies the voltage difference between its input terminals (inverting and non-inverting) and helps reject common-mode signals (signals common to both inputs). The differential amplifier establishes the basic gain and provides a degree of noise rejection.

2. Current Mirror (BLUE):

Purpose: The current mirror is often employed between the op-amp's first (differential) and second (gain) stages.
Operation: It ensures a consistent and accurate current replication from the differential amplifier. The current mirror helps maintain a stable biasing current, improving the op-amp's overall linearity and common-mode rejection. Mirroring the current provides a reliable and matched source for the subsequent gain stage.

3. Gain Stage(GREEN):

Purpose: The gain stage is the second amplification stage of the op-amp.
Operation: It further amplifies the signal from the current mirror. The gain stage is designed to provide the desired voltage gain for the op-amp, contributing to the overall amplification of the input signal. The gain stage is crucial for achieving the op-amp's specified voltage gain, bandwidth, and other performance characteristics.

Transistor Label	W/L Ratio
M1	3
M2	3
M3	7
M4	7
M5	13
M6	105
M7	80
M8	13

Capacitor Name	Capacitance Values
C_C	0.3 pF
C_L	1.0 pF

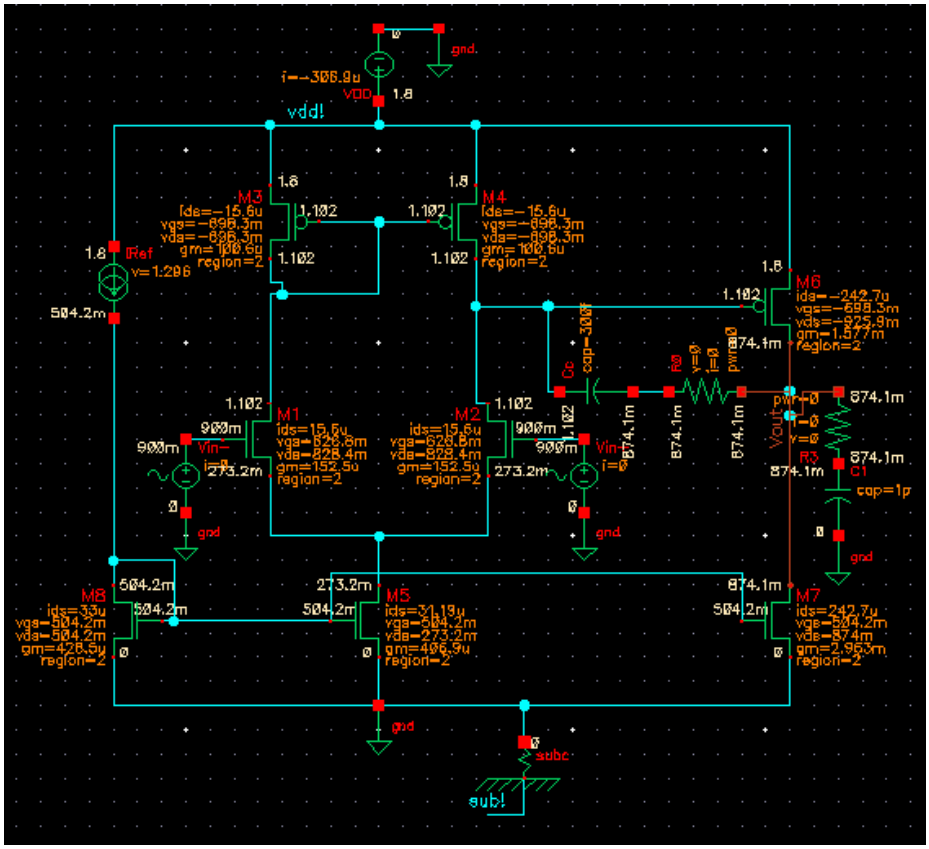
Resistor Label	Resistance

R_C	6.2 k Ohms
R_L	1.5 k Ohms

Simulation Results:

For DC analysis, we are to set the op-amp in an open-loop configuration, which means we apply a 0.9V DC voltage to the negative and positive terminals. Ideally, we should see an output node voltage of 0.9V. Initially, we got something in a range of 100-300mV using exact calculation values for our (W/L) ratios. To get 0.9V, we had to fine-tune our design. The first thing we did was increase the W/L ratio for MOSFET 6.

Increasing the PFET 6 W/L ratio to 105 gave us a desirable ~0.9V. Here is a figure of the simulation with all MOSFET operating in the saturation region (indicated by region = 2).

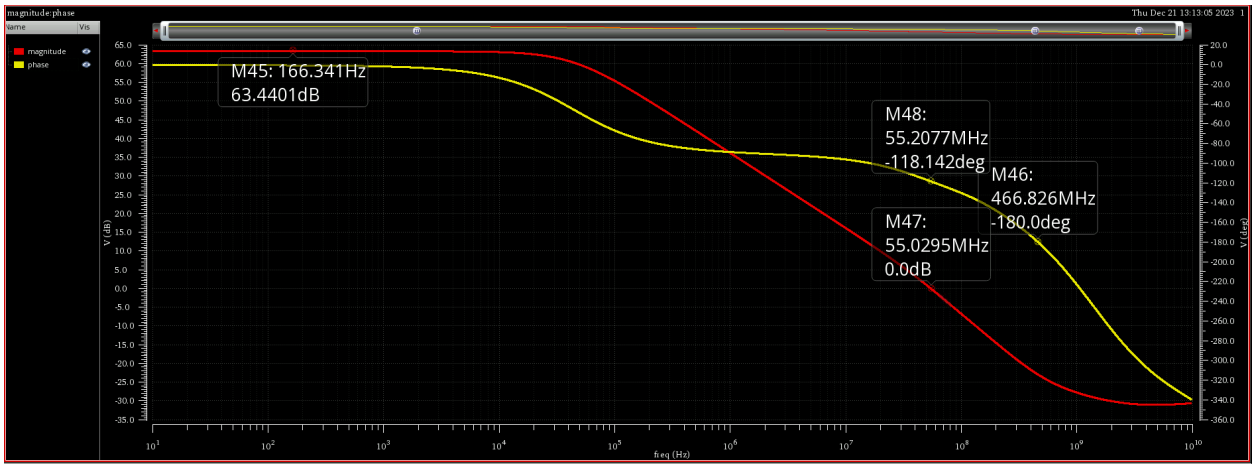


Notice the output voltage is 874mV, which is close to 0.9V.

AC analysis:

To check if our two-stage op-amp meets the requirements, we must find the op-amp's low-frequency gain, unity gain bandwidth, and phase margin. This is where AC analysis comes into play. To perform AC analysis, we have to see the op-amp in an open-loop configuration by applying a DC voltage source of 0.9V at the negative terminal and an AC voltage source at the positive terminal with an AC magnitude of 1V and a DC voltage of 0.9V. Then, we can perform an AC simulation and sweep the frequency from 10 Hz to 1 GHz. Initially, we encountered an issue where our low-frequency gain and unity-gain bandwidth would match the requirements, but the phase margin didn't. The phase margin was always less than 60 degrees. To fix this, we added a resistor in series with the compensation capacitor and a resistor in series with the load resistor. This allowed us to shift the high-frequency pole closer to the origin. The compensation resistor value was calculated by: $R = 1/(2\pi * GB * Cc)$, and we got a resistor of 6.2k. We fine-tuned the load resistor until the phase margin was at least 60 degrees.

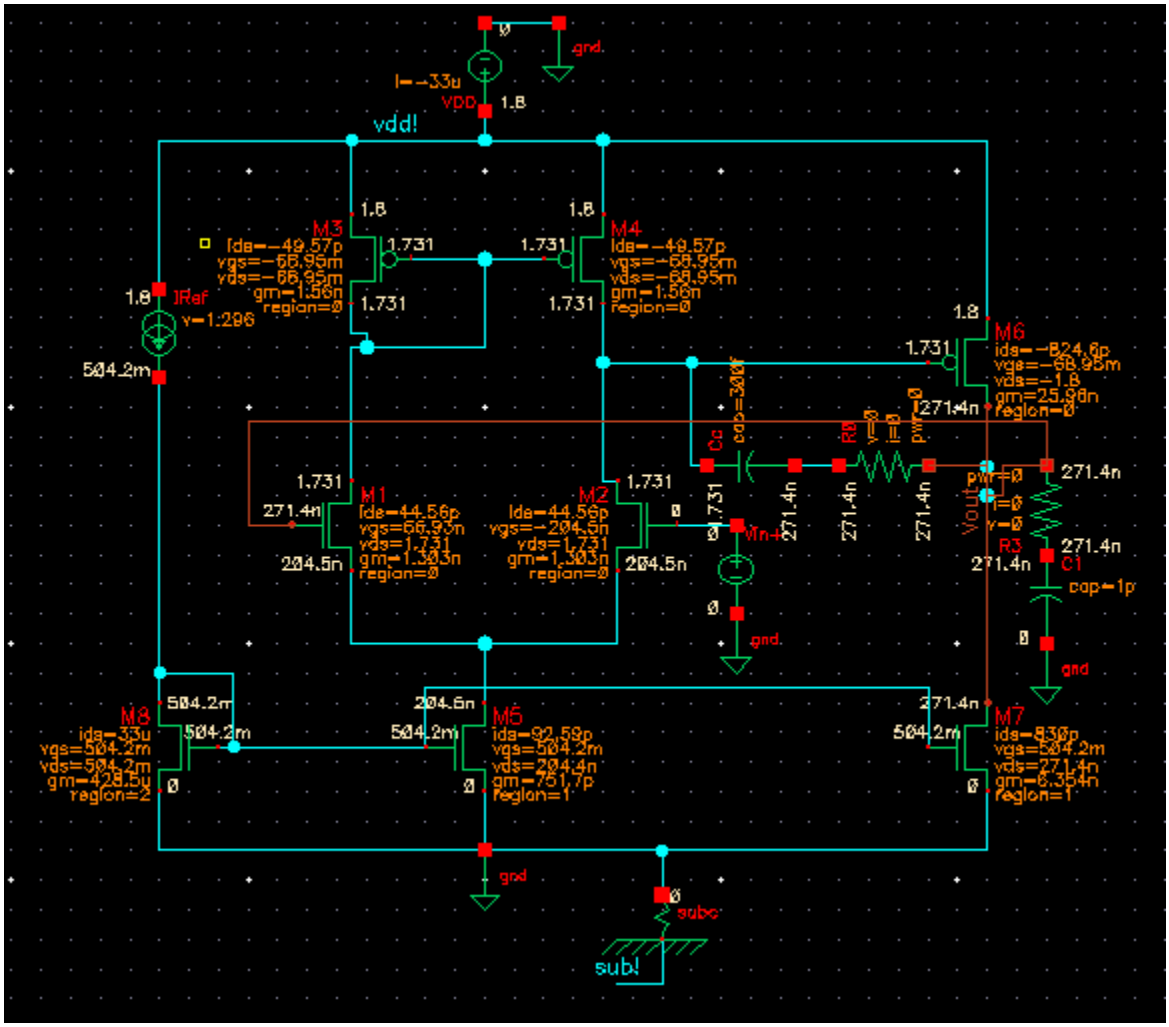
Here is the magnitude and phase response of our op-amp.



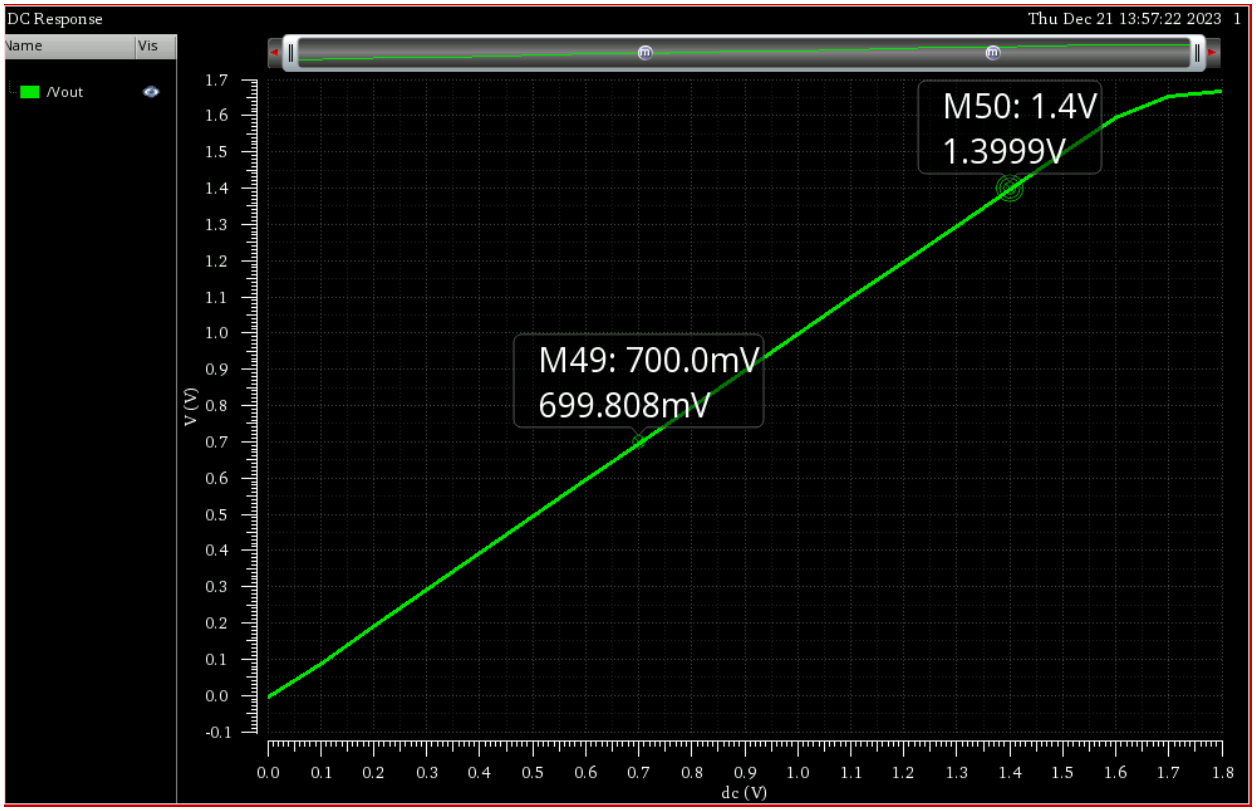
As we can see, our low-frequency gain is approximately 63 dB. Unity gain bandwidth is approximately 55Mhz. Note that Unity-gain bandwidth is where the gain is 0 dB. Given where the unity-gain bandwidth occurs, we can use the frequency to trace onto the phase margin and see an angle of -118 degrees. To calculate the Phase margin, we must use the phase margin equation given by: $PM = 180 + \omega_{Gx}$, where ω_{Gx} is -118 degrees. This gave us a phase margin of 62 degrees, which matches the design requirements. This phase margin provides excellent stability in the amplifier.

Measure the input common-mode range:

The Input Common Mode Range (ICMR) of a two-stage CMOS operational amplifier (op-amp) defines the range of common-mode input voltages over which the op-amp operates linearly. This range is critical for ensuring the op-amp's linearity, specifying the common-mode input voltage values within which the op-amp provides expected linear behavior. To measure the ICMR of our op-amp, we must configure the op-amp as a unity-gain buffer. This is where we remove the DC voltage connected to the negative input and connect the negative input to the output. Then, we apply a DC voltage source to the positive terminal as shown:



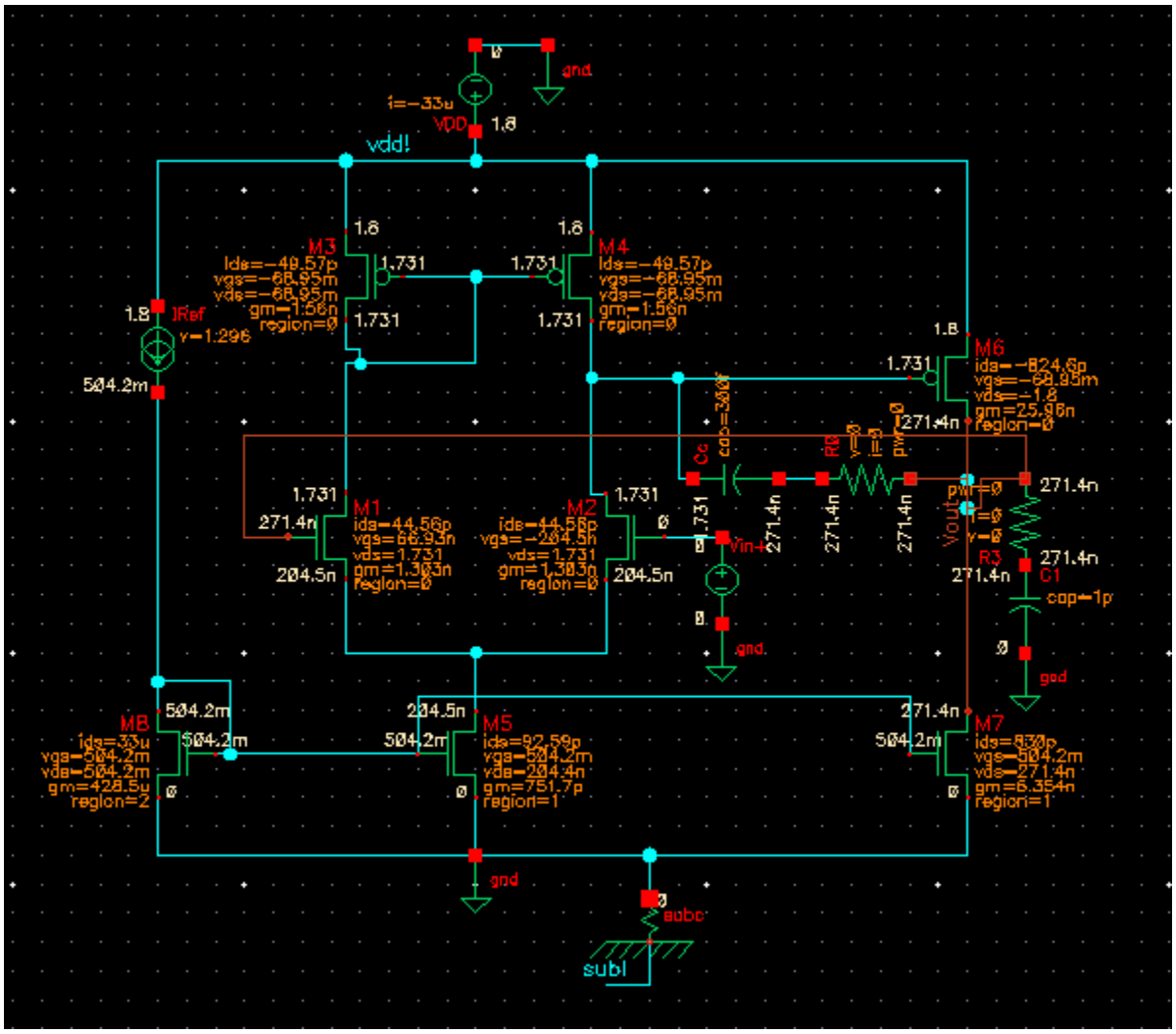
We get the following plot by running a DC simulation and sweeping the DC voltage at the positive terminal from 0 to 1.8V.



We can see a linear relationship between Vout and Vin from 0V to approximately 1.6V. After 1.6V, it seems to be non-linear. As the design requirement stated, our op-amp must have an ICMR from 0.7V to 1.4V, which fits the range. Hence, we can say that our ICMR is from 0 to 1.6V and will also operate from 0.7V to 1.4V.

Power Dissipation:

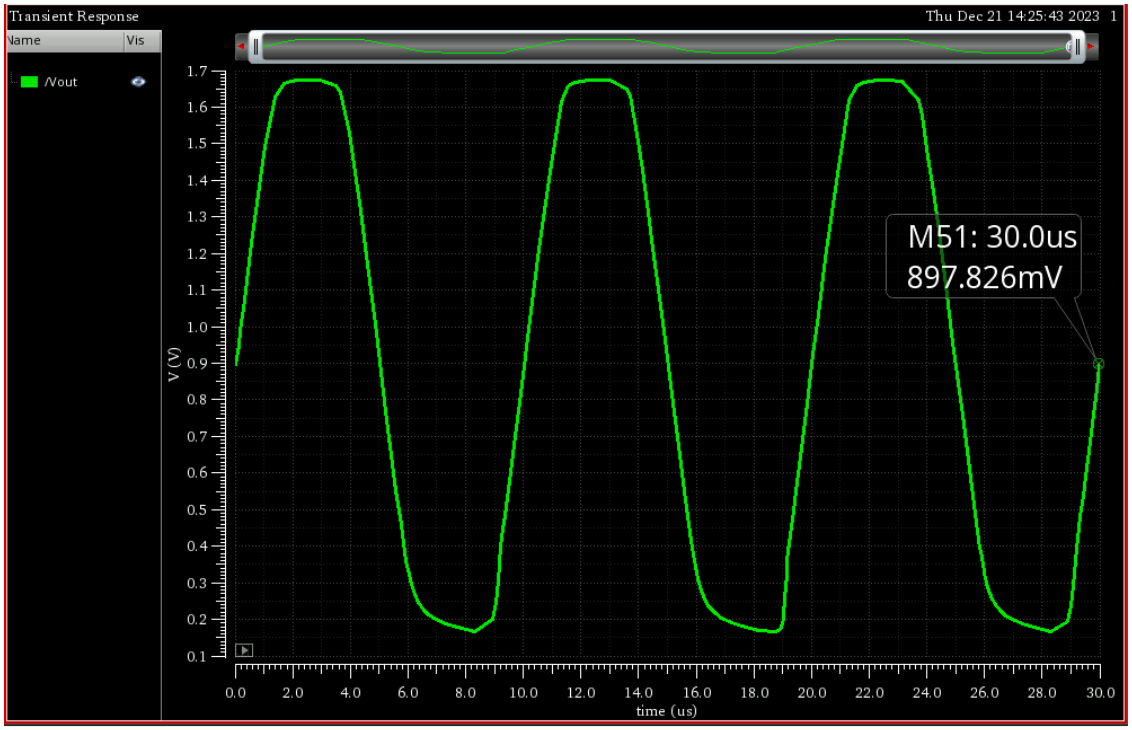
Power dissipation is vital in a two-stage op-amp as it affects efficiency and component reliability. Efficient power management is crucial for minimizing energy consumption, especially in battery-powered applications. To measure the power dissipation of our op amp, we can configure the op-amp as a unity-gain buffer and then run a DC simulation. The power dissipation equation is given by VDD x IDD, where VDD is the DC voltage source, and IDD is the total current coming from VDD.



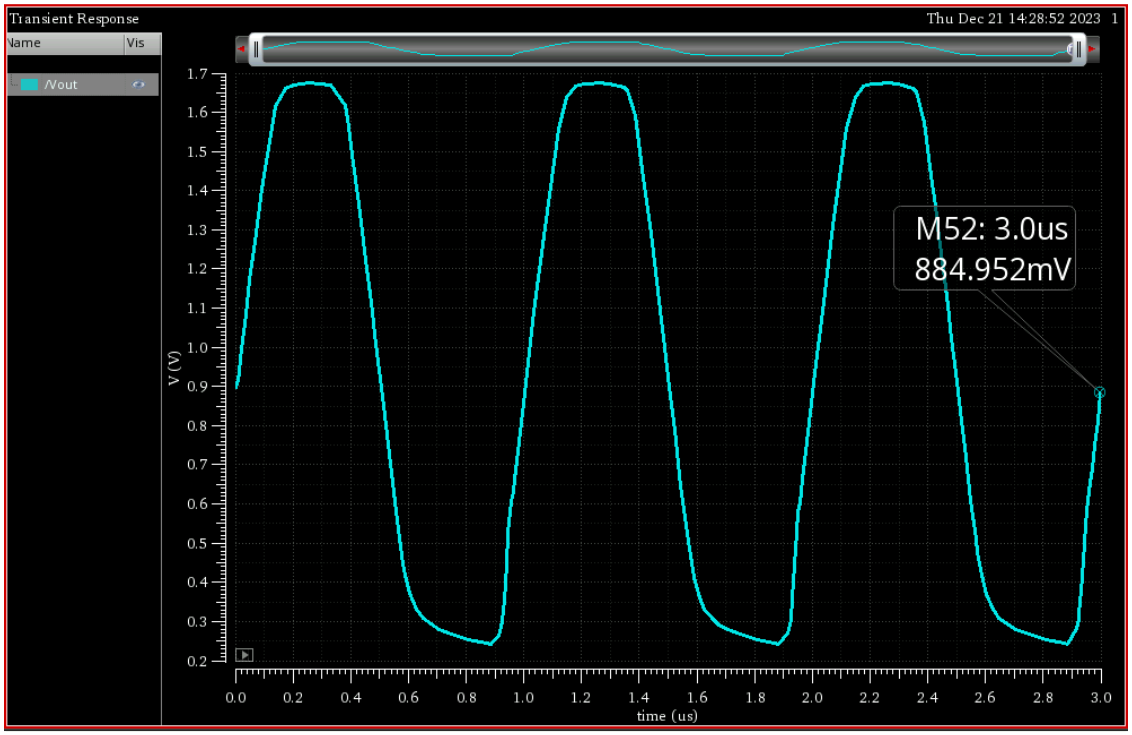
From the simulation, we can see that our VDD is 1.8V and IDD = -33uA. Taking the product of these values gives us a power dissipation of 59.4mW. We are omitting the negative sign.

Transient Simulation:

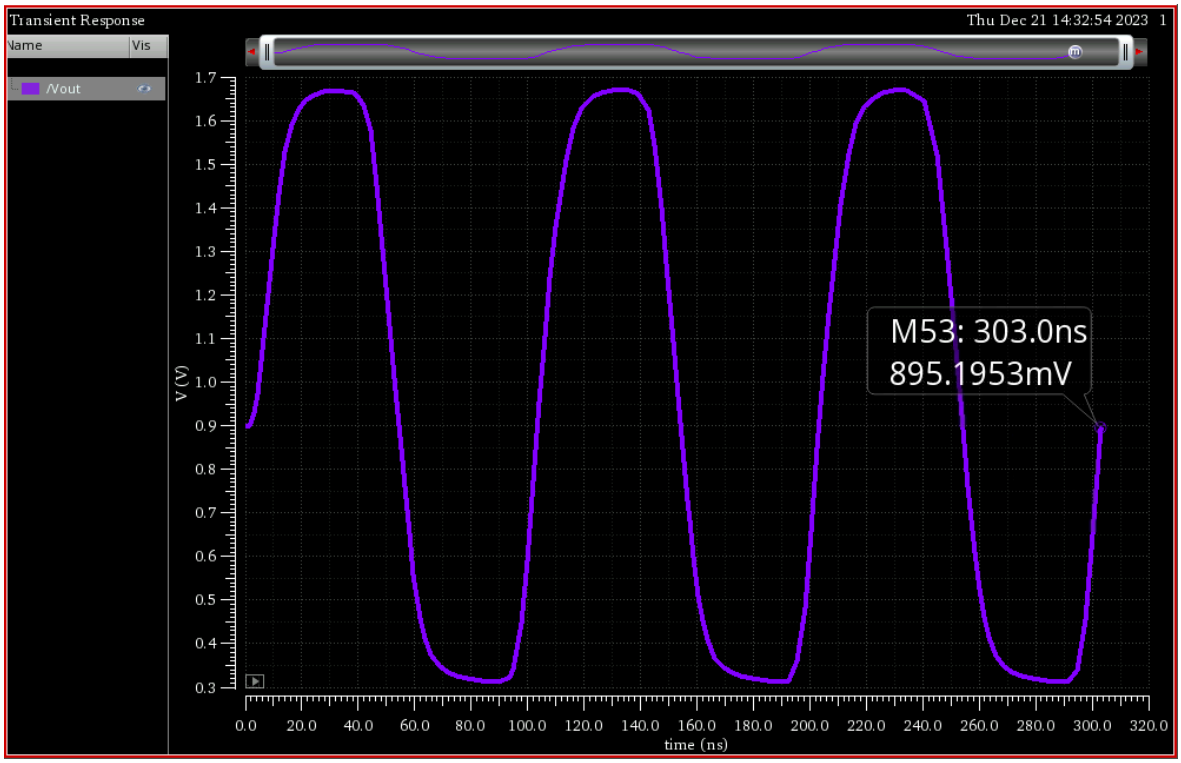
100kHz



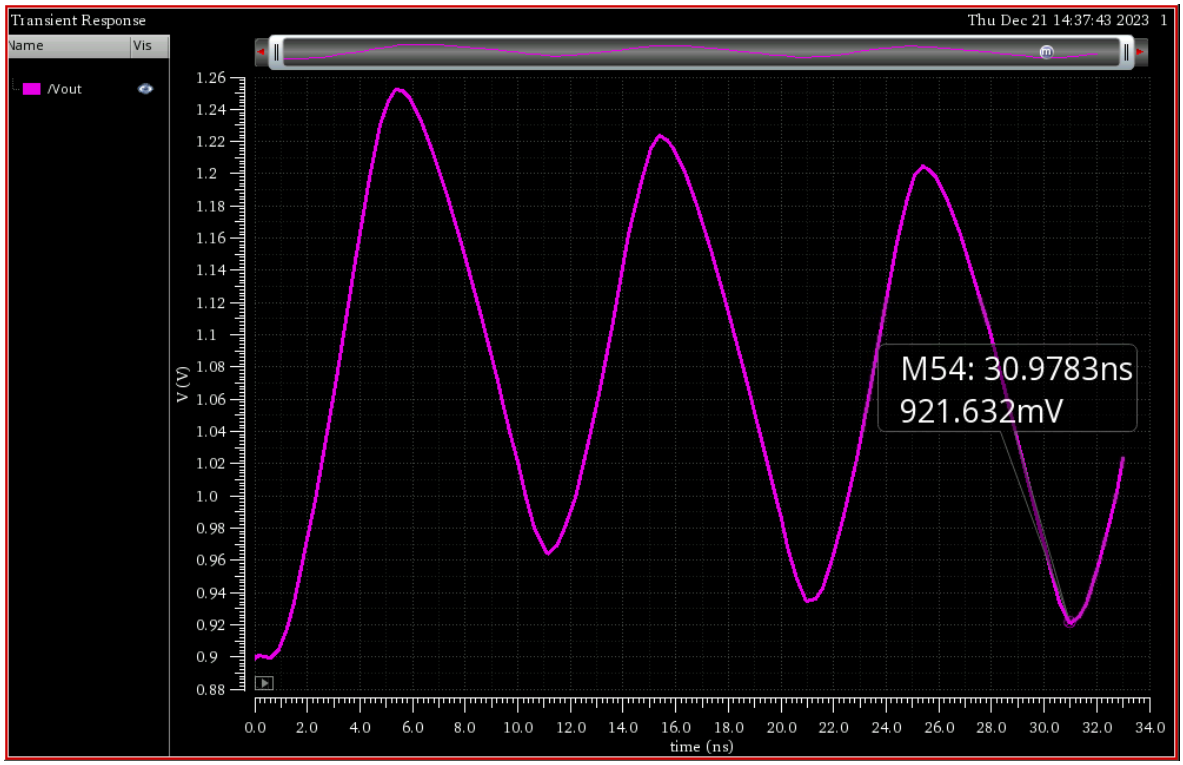
1Mhz



10Mhz



100Mhz:



The main difference we can observe on these plots is that the time scale for each cycle becomes smaller and smaller as the AC frequency is scaled up. This is due to the simple fact that frequency is inversely related to the cycle period. At lower frequencies, the plots look more "rounded." At 100 MHz, the plot looks much more "sharp" and has many more pointed edges. This is because at higher frequencies, the voltage changes more rapidly, and this increased speed of change leads to a faster sampling period. The number of points included in the visualization of the response is drastically increased, providing a more accurate version of the amplifier's behavior. More data points lead to a more accurate visualization of the amplifier's behavior.

Here is a table summarizing the specifications of our stand-alone op-amp.

Specification	Value
Low-Frequency Gain	~63 dB
Gain.Bandwidth (GB)	~55 Mhz
Input Common Mode Range (ICMR)	0V - 1.6V (includes 0.7V to 1.4V)
Phase Margin	~62 degrees
Power Dissipation	59.4mW

To conclude, a minimum MOSFET channel length of around 1 micron was necessary to achieve a low-frequency gain of 60 dB. The M6 mosfet needed a higher W/L ratio than expected because it needed to generate more current, which is directly proportional to the W/L ratio of an FET. Adding a load capacitance significantly increased the phase margin, but adding a small resistor in series with this capacitance allowed us to achieve a phase margin of ~62 degrees. Finally, a C_C of 0.3 pF was necessary because the minimum capacitance allowed us to achieve the gain parameters of the amplifier.

This project was very interesting because we explored Cadence intimately and directly observed the effects of changing parameters on the overall circuitry. It has given us a new appreciation for the intricacies of transistor circuit design and all the thought and methodology that goes into designing these devices to be reliable, robust, and stable.