# 263-2300-00: How To Write Fast Numerical Code

## Assignment 1: 100 points

**Submitted by Jinank Jain**

**Solution 1**

**Part a**
Processor Manufacturer: Intel
Processor Name: i7
Processor Number: 3632QM

**Part b**
CPU Logical Cores: 8
CPU Physical Cores: 4

**Part c**
CPU Core frequency: 2.2 GHz

**Part d**
CPU Maximum Frequency: 3.2 GHz.
Yes it does support Intel Turbo Boost Technology (2.0)

**Part e**
Tick since my processor belongs to the family of Ivy Bridge Processor.

**Part f-i**

| OpType | Latency | Throughput | Gap |
|---|---|---|---|
| Addition | 3 | 1 | 1 |
| Multiplication | 5 | 2 | 0.5 |
| rcp | 7 | 0.5 | 2 |
| FMA | NA | NA | NA |

Table 1: Latency/Throughput/Gap for various operations

**Part j**
Peak performance: 32 flops/cycle and 102.4 Gflops/sec

**Solution 2**

**Part a**
Appropriate cost function would involve cost of multiplication, additions and divisions individually. One such example could be following:

$$C(n) = C_{add} * N_{add} + C_{mul} * N_{mul} + C_{div} * N_{div} + C_{typecast} * N_{typecast}$$

## Part b

$$C(n) = C_{add} * (4(n-1)+1) + C_{mul} * (6(n-1)+2) + C_{div} * (2(n-1)+2) + C_{typecast} * (2(n-1)+2)$$
$$C(n) = C_{add} * (4n-3) + C_{mul} * (6n-4) + C_{div} * (2n) + C_{typecast} * (2n)$$
$$C(n) = flops(n) = 14\text{n - } 7$$

## Solution 3

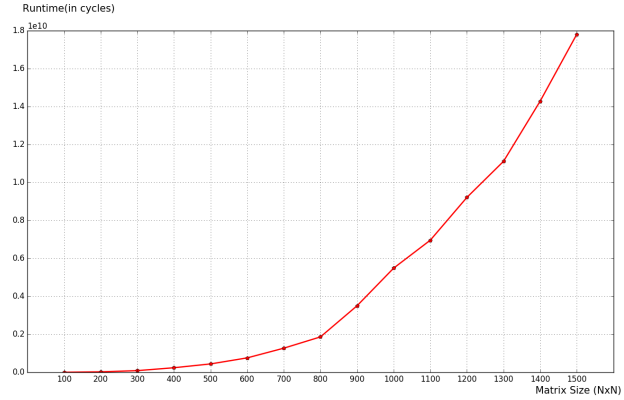


Figure 1: Flow Fairness v/s Per-user fairness

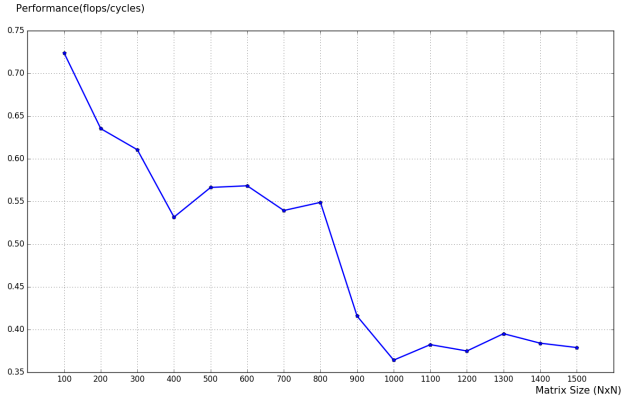


Figure 2: Flow Fairness v/s Per-user fairness

## Solution 4

For example if we look at the paper from Facebook we could find a couple a example due to which traffic would not be rack local:

- Cache Leader servers won't have rack local traffic as they are achieve cache coherency and in order to do that they need to talk to servers within datacenter or outside datacenter.
- Cache Follower servers won't have rack local traffic as they are providing data from cache to other servers in the datacenter and that's what was evident from the paper.

### Solution 5

#### Part a

- `artcomp1`: N flops
- `artcomp2`: N flops
- `artcomp3`: N flops

#### Part b

- `artcomp1`:
  - Flops = N
  - Memory Transfers (floats) $\geq$ 2N
  - Read (bytes) $\geq$ 8N
  - Operational Intensity I(N) $\leq \frac{1}{8}$
- `artcomp2`:
  - Flops = N
  - Memory Transfers (floats) $\geq$ 2N
  - Read (bytes) $\geq$ 8N
  - Operational Intensity I(N) $\leq \frac{1}{8}$
- `artcomp3`:
  - Flops = N
  - Memory Transfers (floats) $\geq$ 3N
  - Read (bytes) $\geq$ 12N
  - Operational Intensity I(N) $\leq \frac{1}{12}$

#### Part c
#### i

- `artcomp1`: N/2
- `artcomp2`: N/2

- `artcomp3`: N/2

**ii**

- `artcomp1`: N/4, N/4, N/2
- `artcomp2`: N/4, N/4, N/2
- `artcomp3`: N/4, 5N/12, 5N/6