Block Diagram

```
class System
vector<Chip*> chips;
```

```
class Chip
System* system;
vector<Node*> node_mesh;
```

```
class Node
Chip* chip;
NodeID id;
int x, y;
Buffer* xneg_in_buffer;
Buffer* xpos_in_buffer;
Buffer* yneg_in_buffer;
Buffer* ypos_in_buffer;
Buffer* xneg_link_buffer;
Buffer* xpos_link_buffer;
Buffer* yneg_link_buffer;
Buffer* ypos_link_buffer;
```

```
vector<IF> IF_Ring;
```

Simulation Engine

```
Message* genMes();
void routing(Message& s);
     void Core_to_Core(Message& s);
     void IF_to_IF(Message& s);
     void IF_to_Core(Message& s);
     void Core_to_IF(Message& s);
void vc_allocate(Message& s);
void switch_allocate(Message& s);
void update(Message& s);
void run(vector<Message*>&
  all_messages, System*& system){
    // Update all messages per cycle
};
```

```
vector<Message*> all_messages;
class Message{
    NodeID source;
    NodeID destination;
    FlitInfo* routpath; // Position of flits, routpath[0]: head flit
    vector<FlitInfo> candidate_channels;
    ····· // Multiple flags
};
```

Configuration File

- Internal Buffer Size
- Interface Buffer Size
- VC Number
- Packet Size
- Flit Width
- On-Chip Bandwidth
- Off-Chip Bandwidth
- Off-Chip Delay
- System Topology
- Routing Algorithm
- Traffic Pattern
- NoC Scale
- System Scale
- Pipeline Cycles
- Interleaving

Monitor

- Latency
- Arrived Packets
- Queued Packets
- Accept Rate
- Hop Number
- Energy