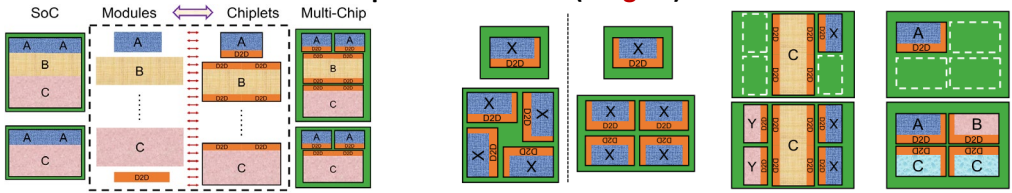
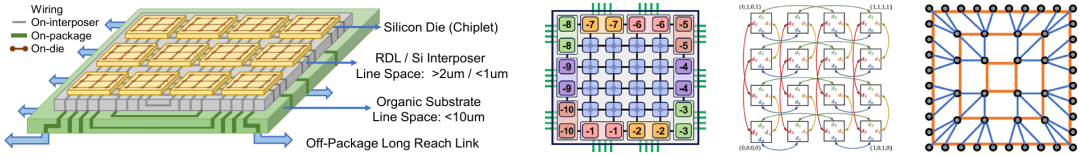
Chiplet-Based High-Performance Interconnection Network Architecture

Chiplet Architecture (Insights)



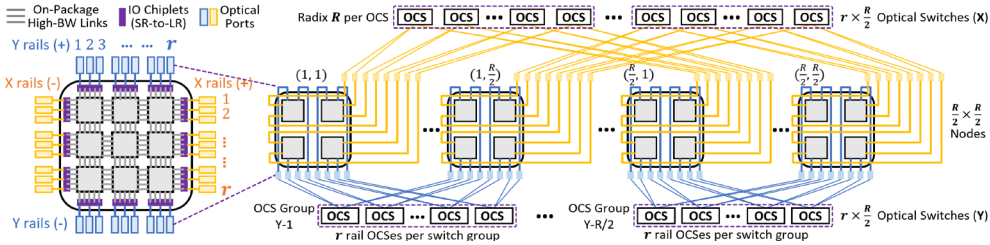
- **CH3:** Chiplet Actuary: Quantitative Cost Model and Multi-Chiplet Architecture Exploration **[DAC 2022]**

Chiplet-Level Network Architecture (Methods and Techniques)



- **CH4:** Scalable Methodology for Designing Efficient Interconnection Network of Chiplets **[HPCA 2023]**
- **CH5:** Heterogeneous Die-to-Die Interfaces: Enabling More Flexible Chiplet Networks **[MICRO 2023]**
- **CH6:** Chiplet Network Simulator: Enabling Efficient Large-Scale Chiplet Network Simulation **[ATC 2024]**
- **CH7:** Ring Road: On-Chiplet Network Architecture Fixing Limitations of Chiplet Networks **[MICRO 2024]**

Chiplet-based System-Level Network Architecture (Solutions)



- **CH8:** Switch-Less Dragonfly on Wafers: A Scalable Network Architecture for Supercomputing **[SC 2024]**
- **CH9:** RailX: A Scalable and Low-Cost Network Architecture for Hyper-Scale LLM Training