Summary

In my program, there are 3 functions. The “instruction\_find” function the “data\_find” function and the “instruction\_find\_previous\_edition” simulates how the computer find the instruction or data using virtual address.

In the main function, I initialized program counter (PC) with a random 32-bit virtual address as the input of “instruction\_find” function. Every time after each instruction found, the PC will be incremented by 16, except for branch instruction in which the PC will get the address contained in the instruction. After “instruction\_find” function is done, I assume we have already get the instruction, so I generate a random instruction which format is:

2-bit opcode + 32-bit address + 6-bit opcount/branch condition

The 2-bit opcode has range [0,3]. The opcount/branch is [1,4]. Besides, all the 3 numbers are randomly generated but within their own range. Then they make up one 40-bit instruction. So after executing the “instruction\_find” function, I made a subloop to realize fetch two (a pair) instructions at the same time.

Cache and TLB:

I defined a class “CacheBlock” to simulate Cache and TLB. When it’s a cache, the member tag is block tag. When TLB, the tag is actually a combination of TLB tag and real page number. A typical cache looks like this:

L1\_I [index\_L1\_I]

It’s a list. L1\_I is the name, means it’s level 1 instruction cache. index\_L1\_I is the cache index. When it equals to 0, that means L1\_I is a fully associative cache (just one set). The size of each list must less than ways. For example, if it’s a 4-way associative cache, L1\_I [index\_L1\_I] <=4. For each index, it’s a linked list. So we use the pointer to traverse/search the list from L1\_I[index\_L1\_I].begin() to L1\_I[index\_L1\_I].end(). If there’s a hit, we get the value using the pointer. We also update cache/TLB using pop/push by LRU policy.

Write back policy:

Blocks are written out to the next level, when they are swapped. When we need to delete data in full set of L1 Cache, we need put the data in L2 if L2 doesn’t contain it. This simulation is achieved.

LRU policy:

I use LRU policy to update the cache and TLB. The back of the list means highest priority (most recently accessed) and the front of the list means the lowest priority (lease recently accessed). So when there’s a hit, we still need to update the list because of LRU. We erase the accessed data, and then push it to the list. So the accessed data will transfer from somewhere in the list to the back of list which means highest priority. Of course when it’s a miss, we pop the most front data(lease recently accessed) in the list and push the new data to the back of the list.

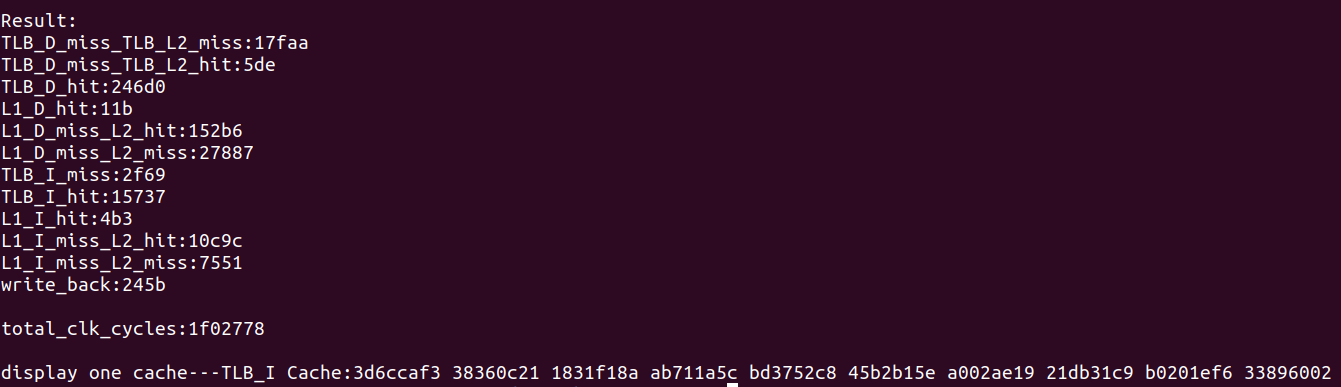
Page fault:

For the page fault simulation, because page fault means there’s a miss when searching memory level page table. In the function “instruction\_find\_previous\_edition”, I simulated update TLB using MPT (memory level page table) or DPT (disk level page table). When there’s a MPT miss, that mean a page fault. But we have to have correspond DPT before running the program. The DPT can’t be just randomly generated. So I use an external file called trace3.din which contains the virtual address and trace4.din which has DPT. To execute this function, we should have these two files as our input. Because the professor said we can just randomly generate the real page number when there’s a instruction/data TLB miss. So there’s no need to apply MPT and DPT. The only goal of this function is page fault simulation.

Statistic and performance gathering system:

The system will show a trace of each step executed for each instruction. In the trace, we can find exactly how the virtual address transferred to physical address and how we find cache and TLBs using these addresses. Also, the system collect how many times of each cache or TLB hit or miss. Also the write back times is also collected. So if we know the miss penalty and hit time for each cache or TLB or write back, the total execution time could be calculated. Besides, we can check contents of any cache or TLB if we want.

Result: (if execute 100001 loops)



These numbers are hex numbers.

Trace (one loop from 100001 loops):

/\*command: make \*/ to compile

/\*command: ./find\_test \*/ to execute

loop: 18690

program counter = 3389b4f0

execute instruction find

virtual address:3389b4f0

block.tag virtual page number:3389TLB\_I hit

get physical address from TLB\_I:6002b4f0

index\_L1\_I:d3

block.tag:1800a

L1\_I miss

L1\_I this set is full, execute write back policy

index\_L2:2d3

block.tag:6002

L1 miss, L2 hit

sub-loop:0

instruction fetched: 13a9e6b501

opcode:0

decode the instruction---load/store

execute data find

instruction:13a9e6b501

virtual address:4ea79ad4

block\_tag:4ea7

TLB\_D miss

TLB\_D this set is full

index\_TLB\_L2:27

block.tag:9d

TLB\_D miss, TLB\_L2 miss

TLB\_L2 this set is full

get real\_page\_num:9d0f

push this 9+16 bit number to TLB\_L2:9d9d0f

push this 16+16 bit number to TLB\_D:4ea79d0f

get physical address from MPT/DPT:9d0f9ad4

physical address for cache find:9d0f9ad4

index\_L1\_D and block.tag6b 4e87c

L1\_D miss

L1\_D this set is full, execute write back policy

index\_L2:26b

block.tag L2:9d0f

L1 miss, L2 miss

cache L2 this set is full

sub-loop:1

instruction fetched: 1975c92484

opcode:0

decode the instruction---load/store

execute data find

instruction:1975c92484

virtual address:65d72492

block\_tag:65d7

TLB\_D miss

TLB\_D this set is full

index\_TLB\_L2:57

block.tag:cb

TLB\_D miss, TLB\_L2 miss

TLB\_L2 this set is full

get real\_page\_num:dfcc

push this 9+16 bit number to TLB\_L2:cbdfcc

push this 16+16 bit number to TLB\_D:65d7dfcc

get physical address from MPT/DPT:dfcc2492

physical address for cache find:dfcc2492

index\_L1\_D and block.tag12 6fe61

L1\_D miss

L1\_D this set is full, execute write back policy

index\_L2:92

block.tag L2:dfcc

L1 miss, L2 miss

cache L2 this set is full

execute data find

instruction:1975c92884

virtual address:65d724a2

block\_tag:65d7

TLB\_D hit

get physical address from TLB\_D:dfcc24a2

physical address for cache find:dfcc24a2

index\_L1\_D and block.tag12 6fe61

L1\_D miss

L1\_D this set is full, execute write back policy

index\_L2:92

block.tag L2:dfcc

L1 miss, L2 hit

execute data find

instruction:1975c93084

virtual address:65d724c2

block\_tag:65d7

TLB\_D hit

get physical address from TLB\_D:dfcc24c2

physical address for cache find:dfcc24c2

index\_L1\_D and block.tag13 6fe61

L1\_D miss

L1\_D this set is full, execute write back policy

index\_L2:93

block.tag L2:dfcc

L1 miss, L2 miss

cache L2 this set is full

execute data find

instruction:1975c93c84

virtual address:65d724f2

block\_tag:65d7

TLB\_D hit

get physical address from TLB\_D:dfcc24f2

physical address for cache find:dfcc24f2

index\_L1\_D and block.tag13 6fe61

L1\_D miss

L1\_D this set is full, execute write back policy

index\_L2:93

block.tag L2:dfcc

L1 miss, L2 hit

Trace (execute find instruction previous edition)

/\*command: ./find\_test ./input\_file/trace3.din ./input\_file/trace4.din\*/ to execute

execute instruction find previous edition

virtual\_address 0:123a6666

TLB\_I miss

Page fault-MPT miss

real page number from DPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I miss

index\_L2:199

block.tag:8888

L1\_I miss, L2 miss

virtual\_address 1:123b6666

TLB\_I miss

Page fault-MPT miss

real page number from DPT:4561

physical address:45616666

index\_L1\_I:99

block.tag:11585

L1\_I miss

index\_L2:199

block.tag:4561

L1\_I miss, L2 miss

virtual\_address 2:123c6666

TLB\_I miss

Page fault-MPT miss

real page number from DPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address 3:123d6666

TLB\_I miss

Page fault-MPT miss

real page number from DPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address 4:123e6666

TLB\_I miss

Page fault-MPT miss

real page number from DPT:2385

physical address:23856666

index\_L1\_I:99

block.tag:8e15

L1\_I miss

L1\_I this set is full

index\_L2:199

block.tag:2385

L1\_I miss, L2 miss

virtual\_address 5:123f6666

TLB\_I miss

Page fault-MPT miss

real page number from DPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address 6:12aa6666

TLB\_I miss

Page fault-MPT miss

real page number from DPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address 7:12ab6666

TLB\_I miss

Page fault-MPT miss

real page number from DPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address 8:12ac6666

TLB\_I miss

Page fault-MPT miss

real page number from DPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address 9:12ad6666

TLB\_I miss

TLB\_I this set is full

Page fault-MPT miss

real page number from DPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address a:12ae6666

TLB\_I miss

TLB\_I this set is full

Page fault-MPT miss

real page number from DPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address b:12af6666

TLB\_I miss

TLB\_I this set is full

Page fault-MPT miss

real page number from DPT:6666

physical address:66666666

index\_L1\_I:99

block.tag:19999

L1\_I miss

L1\_I this set is full

index\_L2:199

block.tag:6666

L1\_I miss, L2 miss

virtual\_address c:12ba6666

TLB\_I miss

TLB\_I this set is full

Page fault-MPT miss

real page number from DPT:6666

physical address:66666666

index\_L1\_I:99

block.tag:19999

L1\_I hit

virtual\_address d:12bb6666

TLB\_I miss

TLB\_I this set is full

Page fault-MPT miss

real page number from DPT:6666

physical address:66666666

index\_L1\_I:99

block.tag:19999

L1\_I hit

virtual\_address e:123a6666

TLB\_I miss

TLB\_I this set is full

TLB\_I miss, MPT hit

real page number from MPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address f:123b6666

TLB\_I miss

TLB\_I this set is full

TLB\_I miss, MPT hit

real page number from MPT:4561

physical address:45616666

index\_L1\_I:99

block.tag:11585

L1\_I miss

L1\_I this set is full

index\_L2:199

block.tag:4561

L1 miss, L2 hit

virtual\_address 10:123c6666

TLB\_I miss

TLB\_I this set is full

TLB\_I miss, MPT hit

real page number from MPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address 11:123d6666

TLB\_I miss

TLB\_I this set is full

TLB\_I miss, MPT hit

real page number from MPT:8888

physical address:88886666

index\_L1\_I:99

block.tag:22221

L1\_I hit

virtual\_address 12:123e6666

TLB\_I miss

TLB\_I this set is full

TLB\_I miss, MPT hit

real page number from MPT:2385

physical address:23856666

index\_L1\_I:99

block.tag:8e15

L1\_I miss

L1\_I this set is full

index\_L2:199

block.tag:2385

L1 miss, L2 hit