RAM and U-Bus
Due: October 1, 2019 at 23:55 on MyCourses

Tutorials A, B and C will be helpful for this assignment. Tutorial A explores truth-tables. Tutorial B and C explores LOGISIM and memory. Become familiar with using LOGISIM before starting this assignment.

QUESTION

Using LOGISIM, build a working 4-nibble RAM. See class lectures and the textbook. Your RAM must have the following elements: 4 nibbles, addressing circuits, the address register, the data register, the mode register (bit), a u-bus, and a clock. Your RAM must be able to read and write nibbles.

You will run your circuit manually by setting the address, mode and data registers, then you will start the clock. The desired action will take place. For example: if you plug in an address into the address register, and a 1 in the mode register, and a nibble in the data register, and you turn on the clock, then the nibble must be copied into the RAM nibble at the desired address.

Since you have a 4-nibble RAM then you will only have addresses 00, 01, 10, and 11. Mode register set to 1 is for write and 0 is for read.

You will need to implement a u-bus to properly handle read and write operations between the data register and the 4-nibbles of RAM.

WHAT TO HAND IN

The LOGISIM circuit file. The TA must be able to load and execute your circuit.

HOW IT WILL BE GRADED

4 nibbles exist : 2 points	Total points = 20
Address circuit : 3 points	Each question is graded proportionally
Address register: 1 point	compared with the official solution.
Mode register : 1 point	
Data register : 1 point	-5% per day late.
U-Bus exists : 3 points	After 2 late days, the assignment is not accepted.
Clock exists : 1 point	
Reads correctly : 4 points	
Writes correctly : 4 points	