

# JINGYAO ZHANG

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## EDUCATION

### University of California, Riverside

Ph.D. student in Computer Science; GPA: 3.71/4.00

Advisor: *Prof. Elaheh Sadredini*

Riverside, USA

Sep 2021 – Present

### Xidian University

M.E. in Electronic and Telecommunications Engineering; Outstanding Thesis Award

Xi'an, China

Sep 2018 – Jun 2021

### Xidian University

B.E. in Telecommunications Engineering; Pilot Class (Top 5% of 800+)

Xi'an, China

Sep 2014 – Jun 2018

## PUBLICATIONS

1. **Jingyao Zhang**, Mohsen Imani, and Elaheh Sadredini. "BP-NTT: Fast and Compact in-SRAM Number Theoretic Transform with Bit-Parallel Modular Multiplication." *In Proc. of the 60th Design Automation Conference (DAC)*. July 2023 (to appear). (acceptance rate: 23%) [[paper](#)]
2. **Jingyao Zhang**, and Elaheh Sadredini. "Inhale: Enabling High-Performance and Energy-Efficient In-SRAM Cryptographic Hash for IoT." *In Proc. of the 41th International Conference on Computer-Aided Design (ICCAD)*. November 2022. (acceptance rate: 22.5%) [[paper](#)] [[doi](#)]
3. **Jingyao Zhang**, Hoda Naghibijouybari, and Elaheh Sadredini. "Sealer: In-SRAM AES for High-Performance and Low-Overhead Memory Encryption." *In Proc. of the 22th International Symposium on Low Power Electronics and Design (ISLPED)*. August 2022. (acceptance rate: 25%) [[paper](#)] [[doi](#)]
4. **Jingyao Zhang**, Huaxi Gu, Li Zhang, Bing Li, and Ulf Schlichtmann. "Hardware-Software Codesign of Weight Reshaping and Systolic Array Multiplexing for Efficient CNNs." *In Proc. of the 24th Design, Automation and Test in Europe (DATE)*. February 2021. (acceptance rate: 24%) [[paper](#)] [[doi](#)]

## RESEARCH EXPERIENCE

### AREA Lab, University of California, Riverside

Graduate Research Assistant

Advisor: *Prof. Elaheh Sadredini*

Sep 2021 – Present

- Currently developing a framework to seamlessly integrate in-SRAM computing into existing computer systems for efficient and secure on-chip processing of pre- and post-quantum cryptography.
- Developed a bit-parallel modular multiplication algorithm with implicit shifting technology for efficient and secure in-SRAM computing of the NTT, optimizing performance on a low-overhead SRAM array.
- Designed a secure in-SRAM architecture for on-chip acceleration of the SHA-3 algorithm using lane-wise data alignment and in-place read/write strategy, achieving high energy and area efficiency with high throughput.
- Designed a secure in-SRAM architecture for on-chip acceleration of the AES algorithm using row-wise data alignment and SubBytes/ShiftRows stage fusion, achieving high energy and area efficiency.

### Advanced Networking Technology Lab, Xidian University

Graduate Research Student

Advisor: *Prof. Huaxi Gu*

Sep 2018 – Jun 2021

- Developed a hardware-software co-design framework for efficient CNNs, leveraging weight reshaping and systolic array multiplexing with genetic algorithms for optimal hardware performance.
- Built a distributed inference system for accelerating CNNs using systolic array on FPGAs, with HLS for low-level hardware description and Aurora/Ethernet protocols for inter-board communication.
- Designed a flexible and compact  $N \times N$  plasmonic switch topology with a dedicated configuration algorithm that ensures re-arrangeable non-blocking, making it ideal for managing mixed traffic in data centers.
- Designed a low-loss compact plasmonic router for mesh networks in optical Network-on-Chip, exhibiting lower insertion loss and a smaller footprint compared to other structures.

## TEACHING EXPERIENCE

### CS 213 Multiprocessor Architecture and Programming

Teaching Assistant

Instructor: *Prof. Elaheh Sadredini*

Sep 2022 – Dec 2022

- Led two discussion sessions of students' presentations.
- Held weekly office hours to answer students' questions.
- Graded homework and programming assignments.

## OTHER EXPERIENCE

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### gem5 Boot Camp

Davis, USA

Participant

Jul 2022 – Jul 2022

- Simulated and analyzed the performance of computer architectures, and studied the behavior of different workloads and benchmark suites on various computer architectures.
- Evaluated the impact of different design choices on system performance, such as varying cache sizes or using different interconnect topologies, and explored the effects of different microarchitectural features.

### Xilinx Summer Camp

Online

Participant & Team Leader

Jul 2020 – Aug 2020

- Developed an FPGA-based distributed platform for acceleration over Ethernet, with the mother board sending a file to a watched folder on the child board for immediate program execution. [[source](#)]

### Microsoft Innovation Center

Xi'an, China

Intern

Jul 2017 – Aug 2017

- Explored the advancements and challenges in the evolution of cellular networks across generations, starting from the early analog systems to the 5G technology.

## PRESENTATIONS

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1. **Jingyao Zhang.** "Inhale: Enabling High-Performance and Energy-Efficient In-SRAM Cryptographic Hash for IoT." *In Proc. of the 41th International Conference on Computer-Aided Design (ICCAD). San Diego, CA.* [[slides](#)] [[video](#)] Nov 2022
2. **Jingyao Zhang.** "Sealer: In-SRAM AES for High-Performance and Low-Overhead Memory Encryption." *In Proc. of the 22th International Symposium on Low Power Electronics and Design (ISLPED). Boston, MA.* [[slides](#)] [[video](#)] Aug 2022
4. **Jingyao Zhang.** "Hardware-Software Codesign of Weight Reshaping and Systolic Array Multiplexing for Efficient CNNs." *In Proc. of the 24th Design, Automation and Test in Europe (DATE). Online.* [[slides](#)] [[video](#)] Feb 2021

## AWARDS & ACHIEVEMENTS

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<b>Dean's Distinguished Fellowship Award</b> , University of California, Riverside	2021
<b>Outstanding Thesis Award</b> , Xidian University	2021
<b>First-class Scholarship</b> , Xidian University (Top 14% of 560+)	2018, 2019
<b>Outstanding Student Award</b> , Xidian University	2018, 2019

## SKILLS

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**Programming:** C, C++, Python, Verilog

**Technologies:** gem5, Sniper, HSpice, PyTorch, Xilinx Vivado, Omnet++

**Languages:** Chinese (Native), English (Professional), Korean (Elementary)