

For the main control block I used the bellow table for the signals :

| opcode | RegDEs | Branch | Memread | Memtoreg | Aluop | Memwrite | Alusrc | Regwrite | J | Jal | Bne |
|--------|--------|--------|---------|----------|-------|----------|--------|----------|---|-----|-----|
| 000000 | 1      | 0      | 0       | 0        | 010   | 0        | 0      | 1        | 0 | 0   | 0   |
| 000010 | 0      | 0      | 0       | 0        | x     | 0        | 0      | 0        | 1 | 0   | 0   |
| 000011 | 0      | 0      | 0       | 0        | x     | 0        | 0      | 0        | 0 | 1   | 0   |
| 000100 | x      | 1      | 0       | x        | 001   | 0        | 0      | 0        | 0 | 0   | 0   |
| 000101 | x      | 0      | 0       | x        | 001   | 0        | 0      | 0        | 0 | 0   | 1   |
| 001101 | 0      | 0      | 0       | 0        | 100   | 0        | 1      | 1        | 0 | 0   | 0   |
| 100011 | 0      | 0      | 1       | 1        | 000   | 0        | 1      | 1        | 0 | 0   | 0   |
| 101011 | x      | 0      | 0       | x        | 000   | 1        | 1      | 0        | 0 | 0   | 0   |
| 001111 | 0      | 0      | 0       | 0        | 011   | 0        | 1      | 1        | 0 | 0   | 0   |

For the Alu control :

| AluOP | Funct field | Alu control | Operation |
|-------|-------------|-------------|-----------|
| 000   | Xxxxxx      | 010         | Add       |
| 001   | Xxxxxx      | 110         | Sub       |
| 010   | 100000      | 010         | Add       |
| 010   | 100010      | 110         | Sub       |
| 010   | 100100      | 000         | And       |
| 010   | 100101      | 001         | Or        |
| 011   | Xxxxxx      | 011         | Lui       |
| 100   | Xxxxxx      | 001         | Ori       |
| 010   | 100110      | 111         | xor       |

**The comparator module** gets the alu result and the opcode as input ,

The output is the alu result id the instruction is ori or lui ,

Otherwise the comparator checks If the result is less ,greater or equal to zero and produce the output .

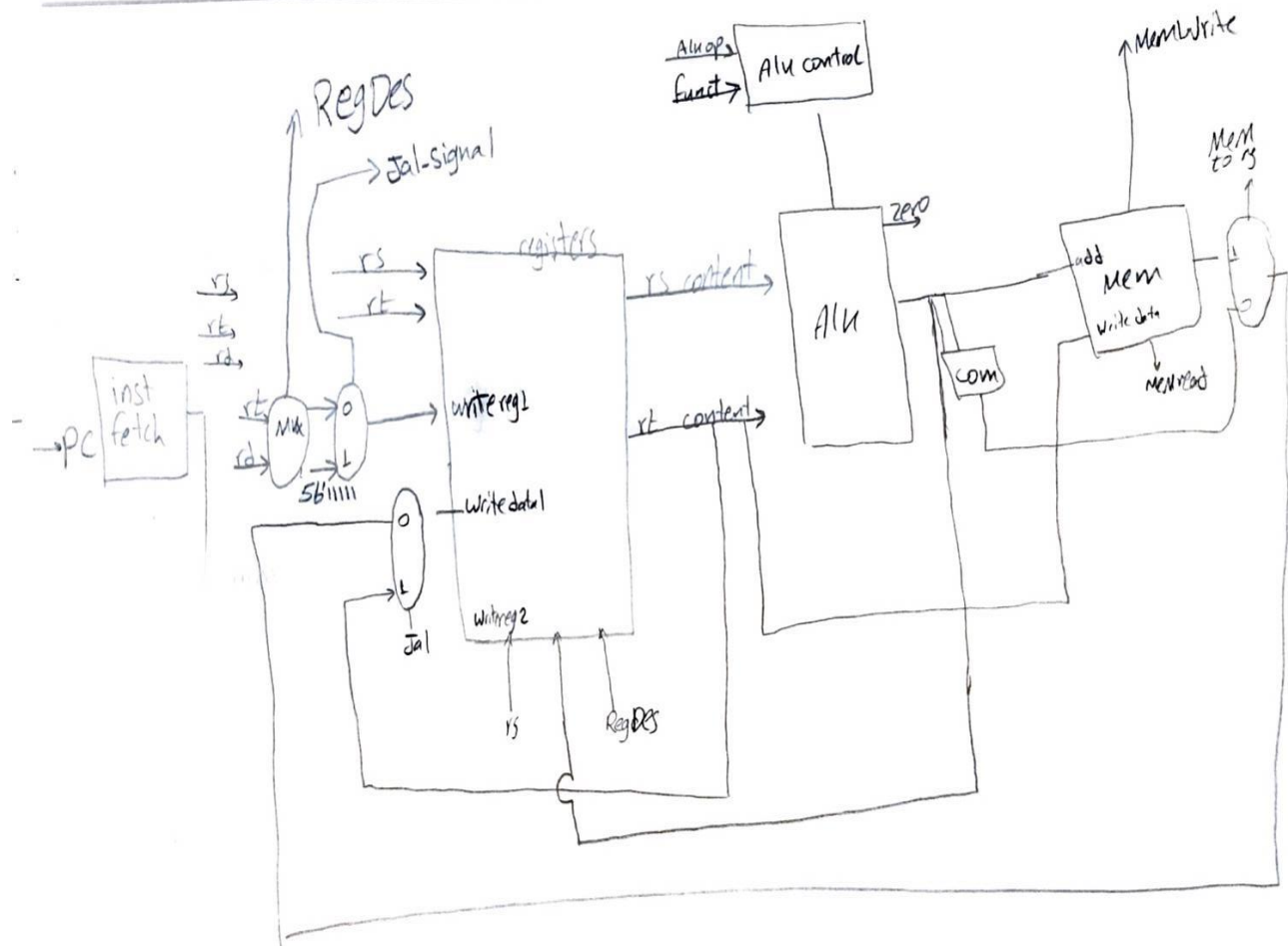
**Registers module** : outputs the content of RS and RT registers ,

And writes into two different registers ,(RT , RD or \$31 ( in case of jal )) and writes into RS register in case of R type instructions

**PC module** : computes the next pc depending on the input signlas

Jal, jump, (beq and zero) , (bne and not zero ) and jump register ,or it adds one to the current pc .

All the modules have testbench to check if it is working well ,



All the signals come from the control unit in the above picture

Some test cases :

