CS3211 Project 1

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Part 1

Hardware

Machines	Number of cores	Clock Speed (GHz)	Total Memory (GB)	L1 cache (kB)	L2 cache (kB)	L3 cache (kB)
CS3211 Lab Intel i7-2600	8	3.4	16	64	256	8192
Tembusu Cluster Intel Xeon E5-2620	24	2.4	64	64	256	15260

Table 1: Hardware specifications

Lab1: Speedup

Task 3

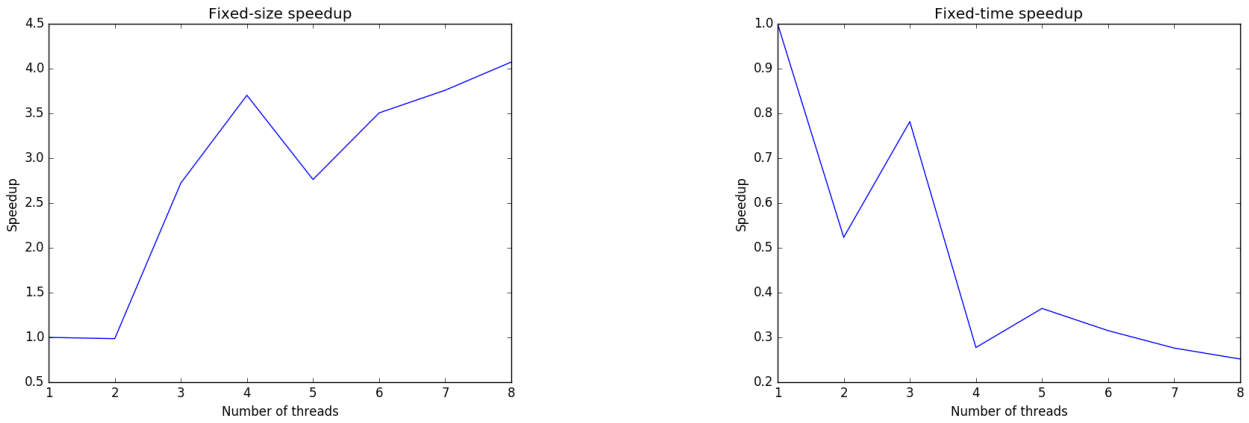

Figure 1: Comparing Fixed-size speedup and Fixed-time speedup

Task 4

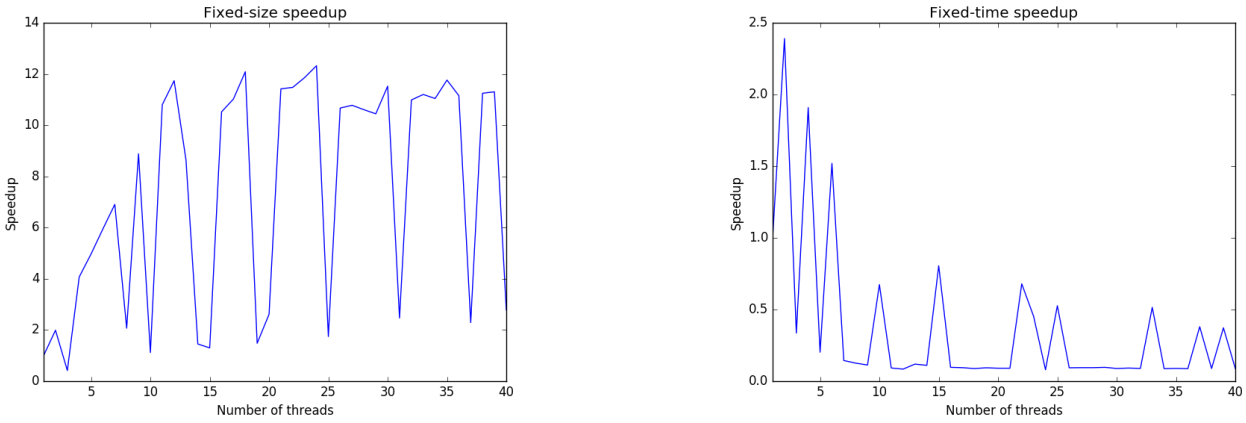

Figure 2: Comparing Fixed-size speedup and Fixed-time speedup

Lab1: Memory effects

Task 6

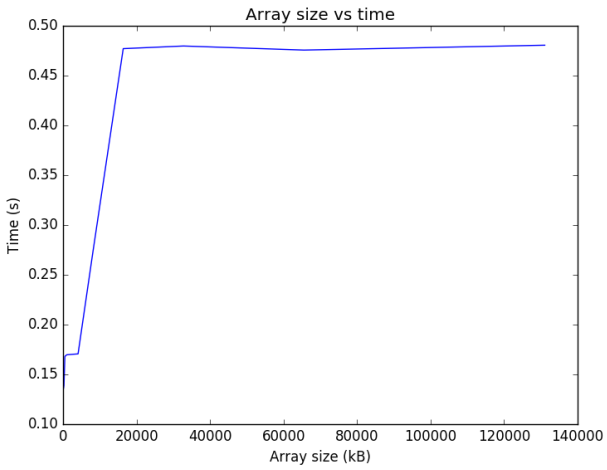

Figure 3: Relationship between array size and time

Lab 2: Accuracy

Task 1

Number of 1s	Sum
500000	500000.0
1000000	1000000.0
18000000	16777216.0
18500000	16777216.0
19000000	16777216.0
19500000	16777216.0

Table 2: Adding 1 to 0 accuracy problem

Task 2

Number of 1s	Sum
500000	500000.3
1500000	1500000.2
3500000	3500000.2
4000000	4000000.2
6000000	6000000.0
6500000	6500000.0
7000000	7000000.0
7500000	7500000.0
9500000	9500000.0

Table 3: Adding 1 to 0.3 accuracy problem

Task 3

Order	Sum
Sum from 20 to 1	584.660156
Sum from 1 to 20	584.660156

Table 4: Adding pseudo random numbers in different orders

Task 4

Trial	Sum
1	3056623.750000
2	3056623.750000
3	3056623.750000
4	3056623.750000
5	3056623.750000
6	3057561.000000
7	3057560.750000
8	3057560.750000
9	3057561.000000
10	3057561.000000

Table 5: Adding 10000 psudo random numbers using 24 threads

Lab 2: Communication, speedup

Task 7

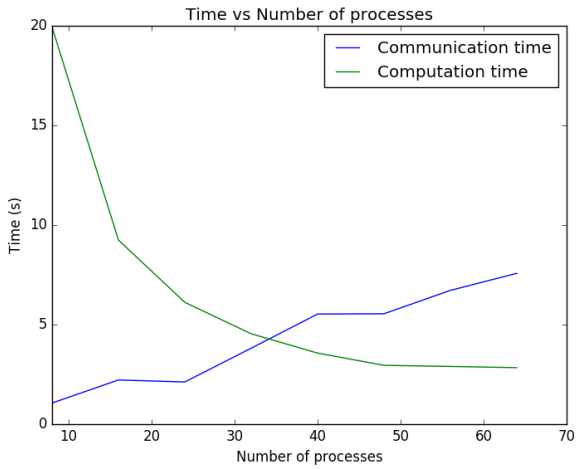

Figure 4: Number of processes vs Communication time and Computation time

1 Part 2

1.1 Tabulation

1.2 Discussion

1.3 Conclusion