

hevc\_hv\_uniwgt\_4t\_16w\_msa

hevc\_hv\_uniwgt\_4t\_8w\_msa

hevc\_hv\_uniwgt\_4t\_8multx4\_msa

```
graph LR; A[hevc_hv_uniwgt_4t_16w_msa] --> C[hevc_hv_uniwgt_4t_8multx4_msa]; B[hevc_hv_uniwgt_4t_8w_msa] --> C;
```

The diagram illustrates a data flow where two separate inputs, 'hevc\_hv\_uniwgt\_4t\_16w\_msa' and 'hevc\_hv\_uniwgt\_4t\_8w\_msa', are combined into a single output, 'hevc\_hv\_uniwgt\_4t\_8multx4\_msa'. The output box is shaded gray, while the input boxes are white with black borders. Blue arrows indicate the direction of the flow from the inputs to the output.