

hevc_hv_uni_4t_16w_msa

hevc_hv_uni_4t_8w_msa

hevc_hv_uni_4t_8multx4_msa

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graph LR; A[hevc_hv_uni_4t_16w_msa] --> C[hevc_hv_uni_4t_8multx4_msa]; B[hevc_hv_uni_4t_8w_msa] --> C;
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The diagram illustrates a data flow where two separate inputs, 'hevc_hv_uni_4t_16w_msa' and 'hevc_hv_uni_4t_8w_msa', are combined into a single output, 'hevc_hv_uni_4t_8multx4_msa'. The output box is shaded gray, while the input boxes are white. Blue arrows indicate the direction of the flow from left to right.