Multi-FPGA-Prototyping LX760 Quad
MFP-LX760-Q

User's Guide rev1.1

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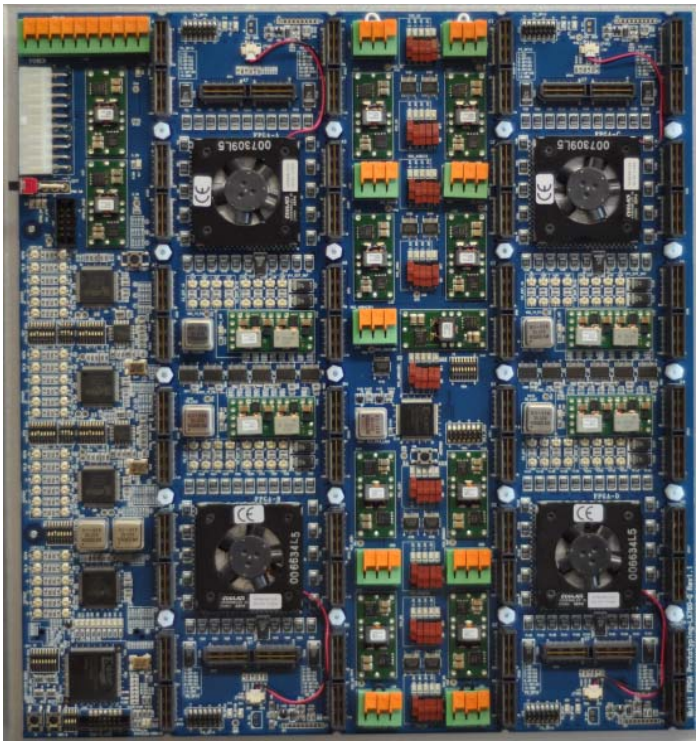

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2011-02-14

About Huins
Huins is a company to introduce ASIC Prototyping Systems and has been leading the ASIC Prototyping technology for over a decade with its cutting-edge architectures, solutions and methodologies. Its family of MFP-LX760-Q and RPS-760x Series SoC ASIC Prototyping Systems with high technology allowing any FPGA to directly connect to any other FPGA enables the highest performance in prototyping.

For more information please see www.huins.com/en/

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This user guide provides comprehensive information about Multi-FPGA-Prototyping LX760 Quad Board.

Version :

VERSION	Date	Content	Approval
1.0-00.00	2010-11-04	<Preliminary_rev1.0> Multi FPGA Prototyping LX760 Quad User's Guide	HUINS
1.1-00.00	2011-1-20	<Rev1.1> Multi FPGA Prototyping LX760 Quad User's Guide	HUINS

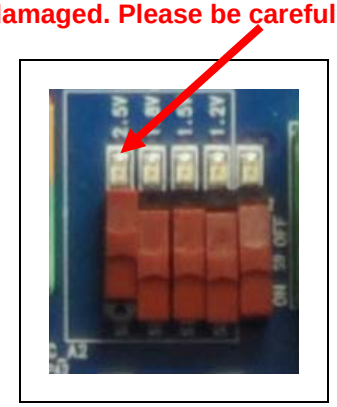
WARNING

Be careful to use the MFP-LX-760Q. It is very sensitive to static discharge and make sure that you're properly grounded whenever handling the board directly.

MFP-LX-760-Q has 9 VCCO regions (VCC_A2, VCC_C5, VCC_A45C12, VCC_C6D4, VCC_A6B4C3D1, VCC_A3B1, VCC_B56D23, VCC_B2, VCC_D5) on the board. Each VCCO region has 5 red VCCO selecting switches (five red slide switches). User can adjust the VCCO voltage as 2.5/1.8/1.5/1.2V with that switches.

When a VCCO selecting switch is set a corresponding LED will be turned on. If 2.5V switch is set, the LED marked 2.5V will be light.

- **Never set more than two switches simultaneously.**
- **User has to select only one V_{CCO} of 2.5V/1.8V/1.5V/1.2V unless the LX760 FPGA I/O block may be permanently damaged. Please be careful to set only ONE switch!**



- **Never change the Vcco Selection switchs while power on.**
- **Before VCCO selection, check Voltage of daughter cards.**

If any other voltage except 2.5/1.8/1.5/1.2V is required, MFP-LX760Q board power switch **should be turned off** before supplying external power via the VCCO power connectors.

User needs to be careful to **set a suitable voltage** of daughter board. User needs to **check the same voltage** on daughter board through I/O connectors ! Don't use different voltages on the connecting daughter boards.

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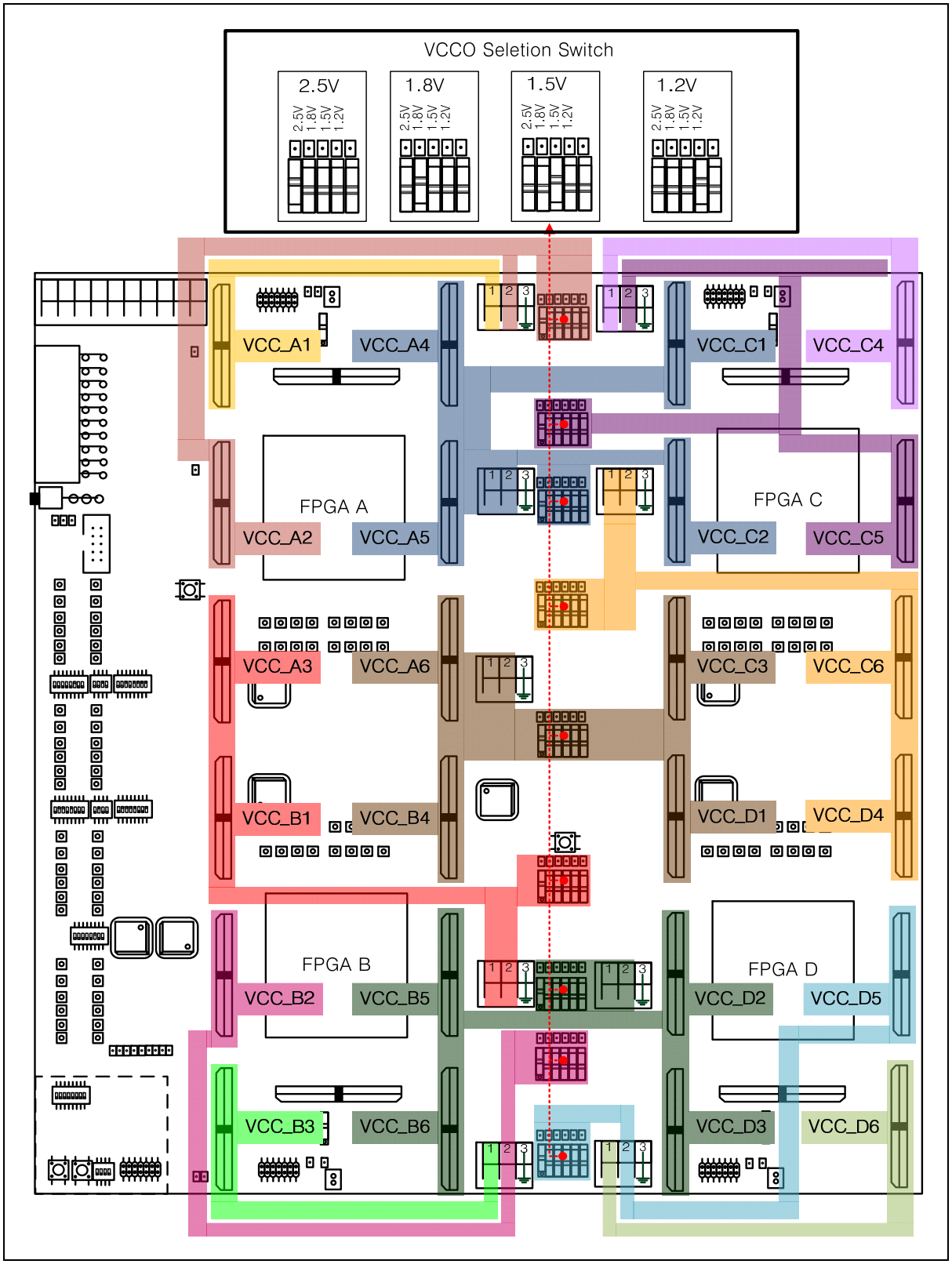
The VCCO Regions is shown as follows. This is described on Chapter 2.3, 2.4.



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1. Overview

MFP-LX760-Q is a high performance ASIC prototyping based on quad Xilinx LX760 FPGAs for SoC/IP Verification. It is designed for all ASIC prototyping needs, IP development and end user evaluations.

Advanced process geometries provide new opportunities to integrate more functionality into smaller, lower cost devices. However, as process geometries shrink, design complexity, development time and design risk increase. A growing number of designers are meeting these verification and development challenges and reducing overall risk by using FPGAs to prototype their ASICs and/or initial production. By incorporating the prototyping as part of the verification methodology, a designer may find a functional bug that was not detected during simulation but could only be uncovered during full system verification. This ability to find problems before taping the design out could save a company millions of dollars in reengineering and tooling costs.

The MFP-LX760-Q and RPS-760x series are Huins's third-generation ASIC Prototyping Systems. Featuring the industry's largest and fastest FPGA, the Virtex 6 LX760 FPGA-based MFP-LX760-Q and RPS-760x series are designed to debug and verify today's most advanced SoC designs. The MFP-LX760-Q and RPS-7604 are able to support designs up to 50 million ASIC gates. By leveraging the system's flexible architecture, both ASIC prototyping systems can be connected to provide support for up to 50 million ASIC gates. The systems are architected and designed to operate at system clock speeds up to 320MHz.

The MFP-LX760-Q ASIC Prototyping Systems set a new standard for ASIC verification, ASIC prototyping, system performance, price/capacity, interconnect flexibility and ease-of-use. The systems offer an organized chassis which includes user add on logic, modules, test codes.

The 30-layers board is carefully designed for maximum performance, with respect to signal integrity, speed and other critical issues. Signals to connectors and between FPGAs are length matched, thus minimizing skew and allowing very high speed signaling. Many kinds of daughter boards are available for MFP-LX760-Q. And these daughter boards are connected to MFP-LX760-Q through an equidistant matrix (70x50 mm)

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1.1. Features

High Performance ASIC / SoC Prototyping System

Based on quad Xilinx Virtex-6 FPGA XC6VLX760-FF1760
Flexible Prototyping System
Support Peripheral I/O modules: DDR3, SDRAM, SRAM, Flash memory, Ethernet, DVI/HDMI, PCIe, USB, Ethernet, etc

MFP-LX760-Q is high-speed SoC IP prototyping platform

MFP-LX760-Q is carefully designed for maximum performance, with respect to signal integrity, speed and other critical issues. Signals to connectors and between FPGAs are length matched, thus minimizing skew and allowing very high speed signaling.

MFP-LX760-Q offers a maximum flexibility.

The same board would be reused in several projects or configurations by replacing optional boards containing I/O and custom subsystems.
Several option daughter boards are available to mount additional application-specific resources like processors, memory devices, PCI express interfaces, etc.

1.2. Specifications

- 4 Xilinx Virtex-6 LX760 devices in FF1760 packages
- FPGA I/O Vcco regions (2.5V, 1.8V, 1.5V, 1.2V) can be selectable
  - 9 regions can individually be adjusted to: 2.5, 1.8, 1.5, or 1.2 V
  - All 13 regions can be sourced externally for other voltages
- Total 3134 I/Os
  - 2856 I/Os : 119pins Connectors 24ea (LVDS support)
  - 40 I/Os : 10pins GPIOs 4ea
- Total 741 signals for FPGA interconnection
  - FPGA A↔FPGA B: 286, FPGA C↔ FPGA D: 286 signals
  - FPGA A↔FPGA C: 66, FPGA B↔ FPGA D: 66 signals
  - FPGA A↔FPGA B↔FPGA C↔FPGA D : 37 signals
- 119 pins are available, 1 Vcco per I/O connector
- 4 Global clock signals and 16 Clock in/out connectors for each FPGA
  - 4 Single ended or 4 differential pair clock lines
  - Clock skew control
  - FPGA 16 Clock connectors(12 Differential, 4 Single ended)
  - 4 Programable clock controller
  - 6 OSC, 2 Programmable PLL(2~344MHz)
- Configuration via JTAG, SystemACE from a CompactFlash card
- ATX power supply

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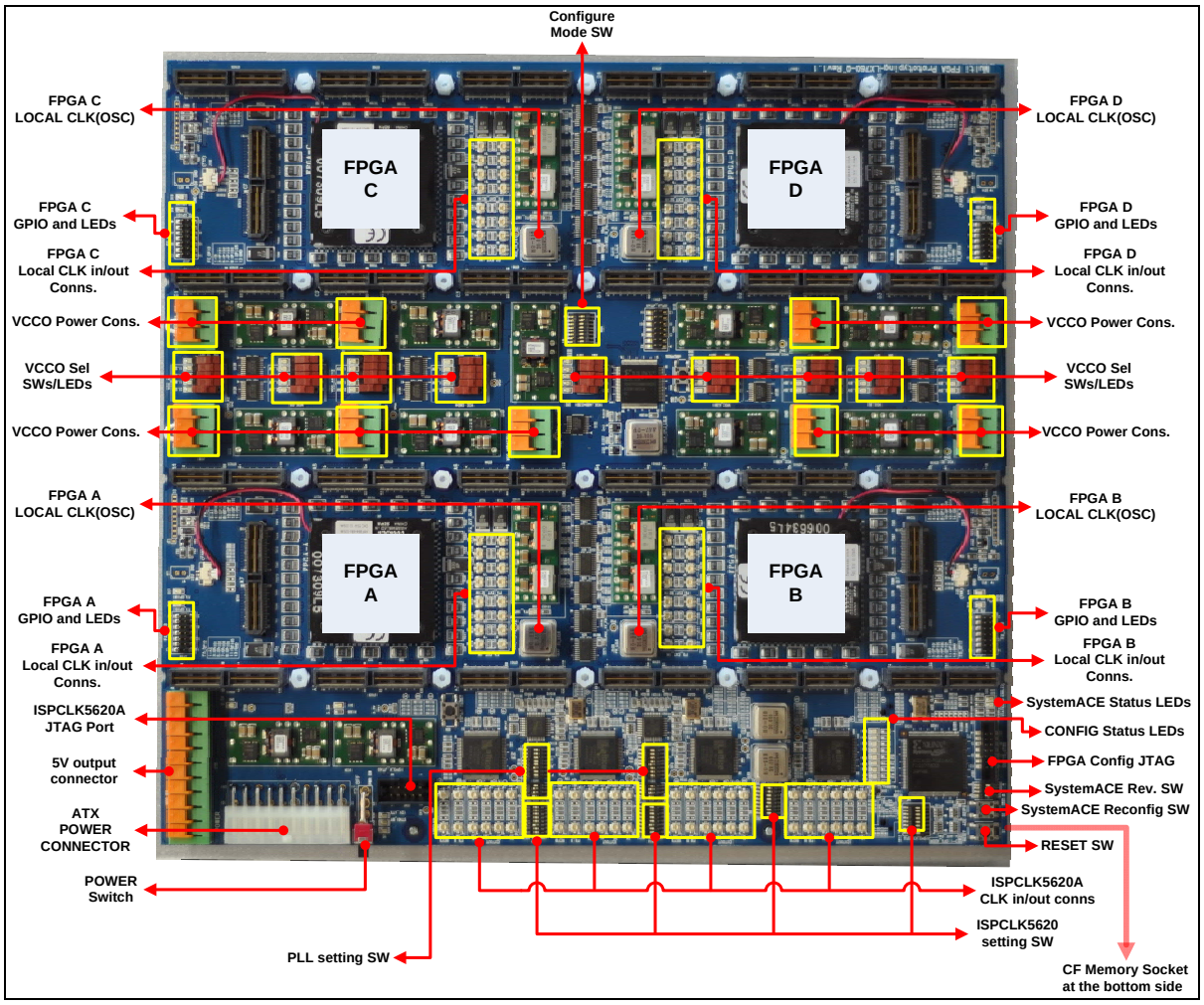

< Board (top side)>

The MFP-LX760-Q has 4 Xilinx Virtex-6 FPGA XC6VLX760 and 24 120pin connectors on the top of PCB and 24 120pin connectors on the bottom of PCB (RapidBus). These connectors are divided into 13 different Vcco regions. User can adjust voltages by slide switches. Additional daughter board power can be supplied by Vcco power connector (VCCO Power Cons.). Each 120pin connector has dedicated pin for power. The top side A7, B7, C7, D7 (120pin connector) of MFP-LX760-Q are tied up 2.5V.

User can download FPGA design file to FPGA via JTAG cable or Compact-Flash memory (CF Memory). CF Memory socket is on the bottom side. Two MFP-LX760-Q can be stacked via 120pin connector and connected side by side via CON I/O board.

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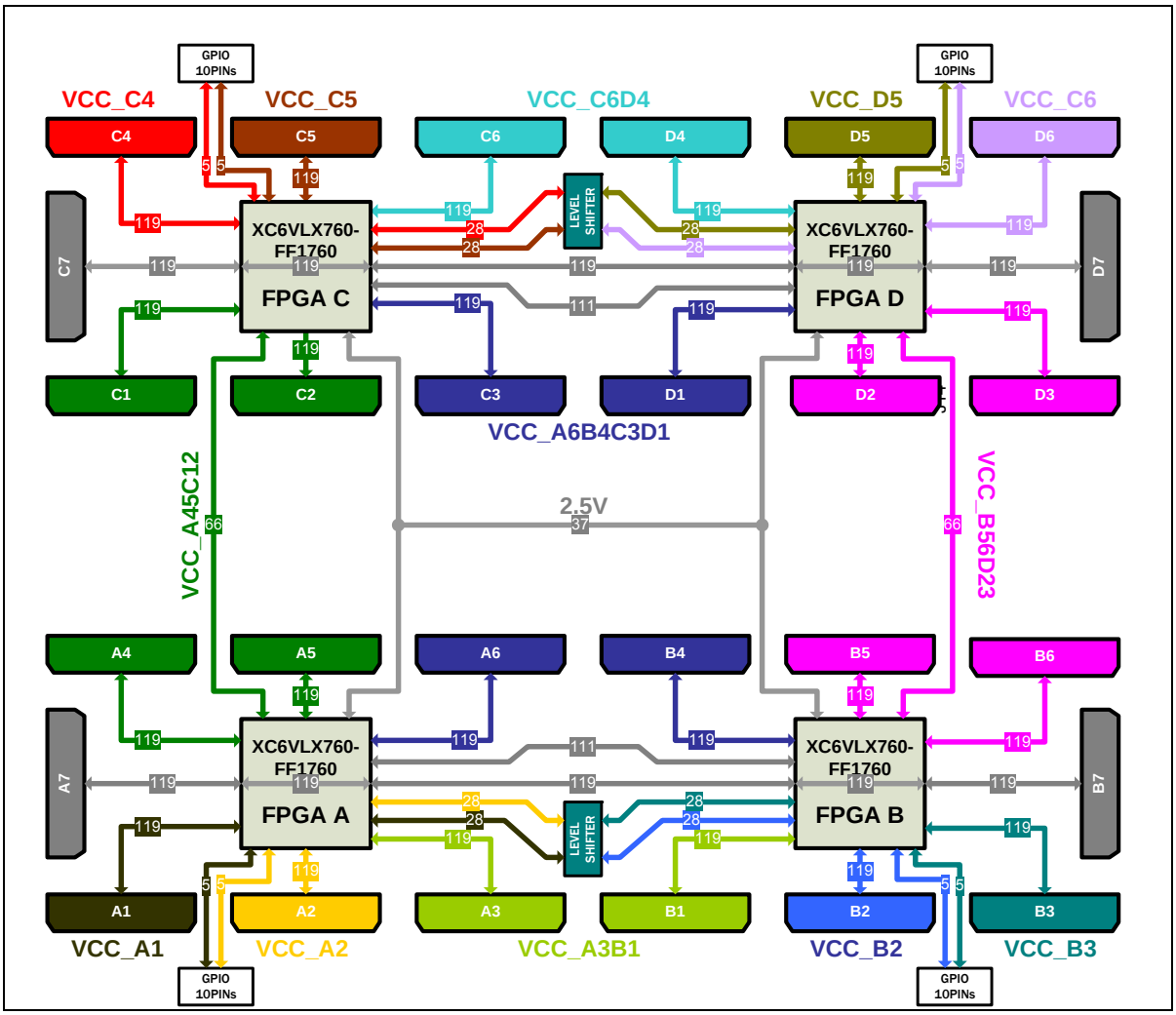
1.3. MFP-LX760-Q Block diagram



< MFP board Block Diagram >

■ Power

MFP-LX760-Q has 14 Vcco regions.

- **9 V_{CCO} regions connectors for daughter boards**
  Connector : [C5] [C6, D4] [D5] [C1, C2, A4, A5] [C3, D1, A6, B5]
  [D2, D3, B5, B6] [A2] [A3, B1] [B2]
  Voltage level of 9 regions are set one of 2.5V, 1.8V, 1.5V, 1.2V by slide switch. Voltage input of 9 regions comes from its board regulator or external power.

- **4 V_{CCO} regions connectors for daughter boards**
  Connector : [A1] [B3] [C4] [D6]
  Voltage level of 4 regions are set one of 2.5V, 1.8V, 1.5V, 1.2V by slide switch. Voltage input of 4 regions comes from its board regulator or external power.

- **1 V_{CCO} connectors for interconnection is always set to 2.5V.**
  Connector : [A7, B7, C7, D7]

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■ MFP-LX760-Q

Item	Specifications	
FPGA	4 Virtex6(XC6VLX760-FF1760)	
Main Clock Source	Four ISPCLK5620AV (Clock Output Range : 2 ~ 400MHz)	
Reference Clock	2 PLL(ICS8401) outputs : 16 ~ 344MHz 2 OSC Sockets	
FPGA Local Clock	1 OSC Socket to each FPGA	
Clock	1 DS and 1SE Reference Clock input to each ISPCLK5620AV Each ISPCLK5620AV output : 4 DS or 8 SE Clock output (FPGA Clock input) 4 DS or 8 SE Clock output (External Clock Connector) 6 DS and 4 SE Clock input/output to each FPGA ※ DS : Differential pair Signal ※ SE : Single Ended	
FPGA Interconnection	Total	741 Connections
	FPGA A ↔ FPGA B	Normal Connection : 111 Through Level Shifter : 56 Connected to CON7 : 119
	FPGA C ↔ FPGA D	Normal Connection : 111 Through Level Shifter : 56 Connected to CON7 : 119
	FPGA A ↔ FPGA C	Normal Connection : 66
	FPGA B ↔ FPGA D	Normal Connection : 66
	FPGA A ↔ FPGA B ↔ FPGA C ↔ FPGA D	37
I/O Total	Board I/O Total	3134
I/O	FPGA I/O Total	2856 I/O
	FPGA A	Total 714 I/O (119 x 6ea), LVDS
	FPGA B	Total 714 I/O (119 x 6ea) , LVDS
	FPGA C	Total 714 I/O (119 x 6ea) , LVDS
	FPGA D	Total 714 I/O (119 x 6ea) , LVDS
GP I/O	40 (four 10pin male connectors)	
FPGA Configuration JTAG	14pin Config JTAG port SystemACE CF (Revision Selectable)	
Accessories	FPGA Int. Regulator	
	User Manual Ver 1.0	
	ETC Regulator	1V/30A 4ea
	FPGA VCCO Regulator	1.8V/3A 1ea 2.5V/15A Regulator 1ea 3.3V/15A Regulator 1ea
	JTAG Cable	2.5V/1.8V/1.5V/1.2V / 15A Regulator 9ea
Power Supply	Power Cable 220V or 110V	
	ATX PC Power Supply 220V/110V AC	

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1.4. Option daughter boards

Item	Specifications	Default	Comments
CON1x1	Interconnection 1x1	X	
CON1x2	Interconnection 1x2	2	
CON2x1	Interconnection 2x1	4	
CON2x2	Interconnection 2x2	1	
DEBUG	MICTOR connector	2	
SDRAM	64MB SDR SDRAM module	X	Need "CON1x1 Level shifter"
AsyncSRAM/Flash	1MB AsyncSRAM, 32MB NorFLASH	X	
DISPLAY/AUDIO	TFT-LCD connector, CIS connector, VGA port , AC97 audio	X	
COMM	100/10 Ehternet , USB2.0 HOST/OTG, UART 2port, IrDA 1port	X	
CON1x1 Level shifter	2.5V to 3.3V Level shifter	X	

- CON1x1, CON1x2, CON2x1, CON2x2 daugter boards is useful for more connection.
- DEBUG daughter board with MICTOR connector can be interfaced with Logic Analyzer.

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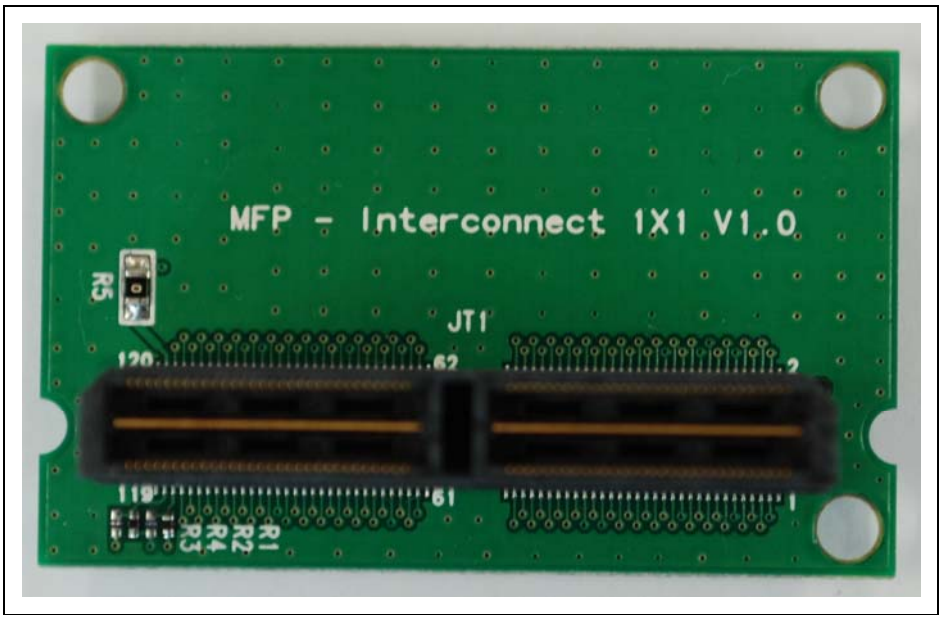
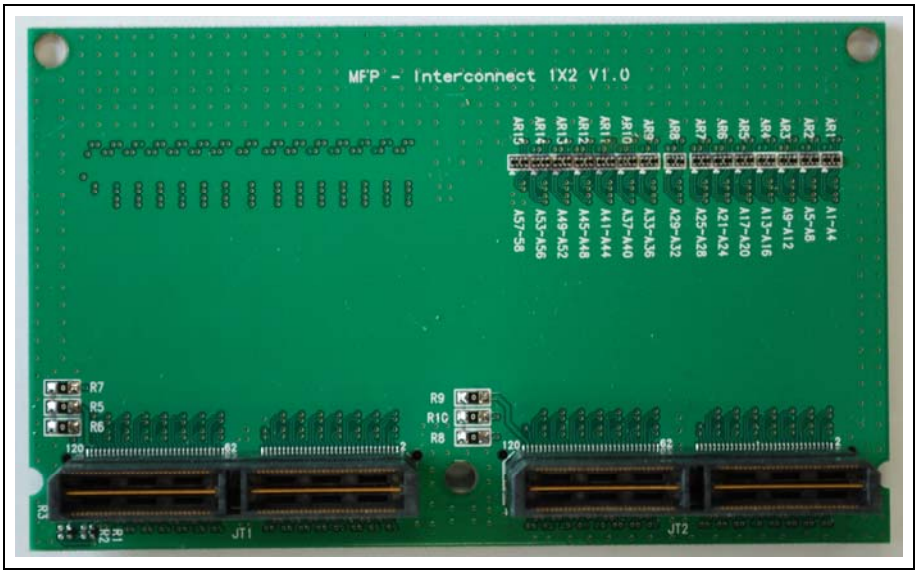


[Interconnect 1x1 Module Rev1.0]



[Interconnect 1x2 Module Rev1.0]

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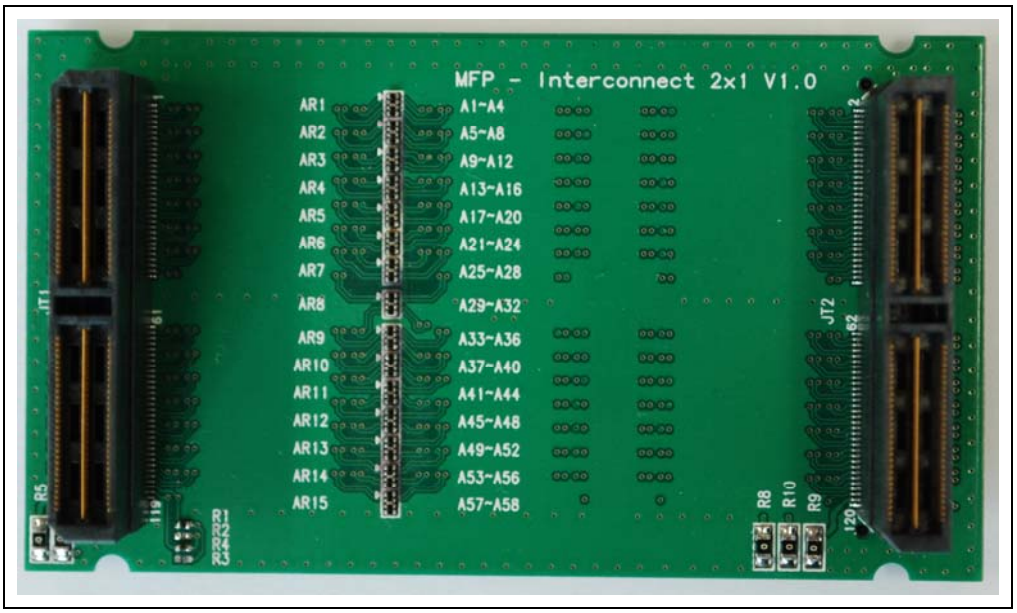
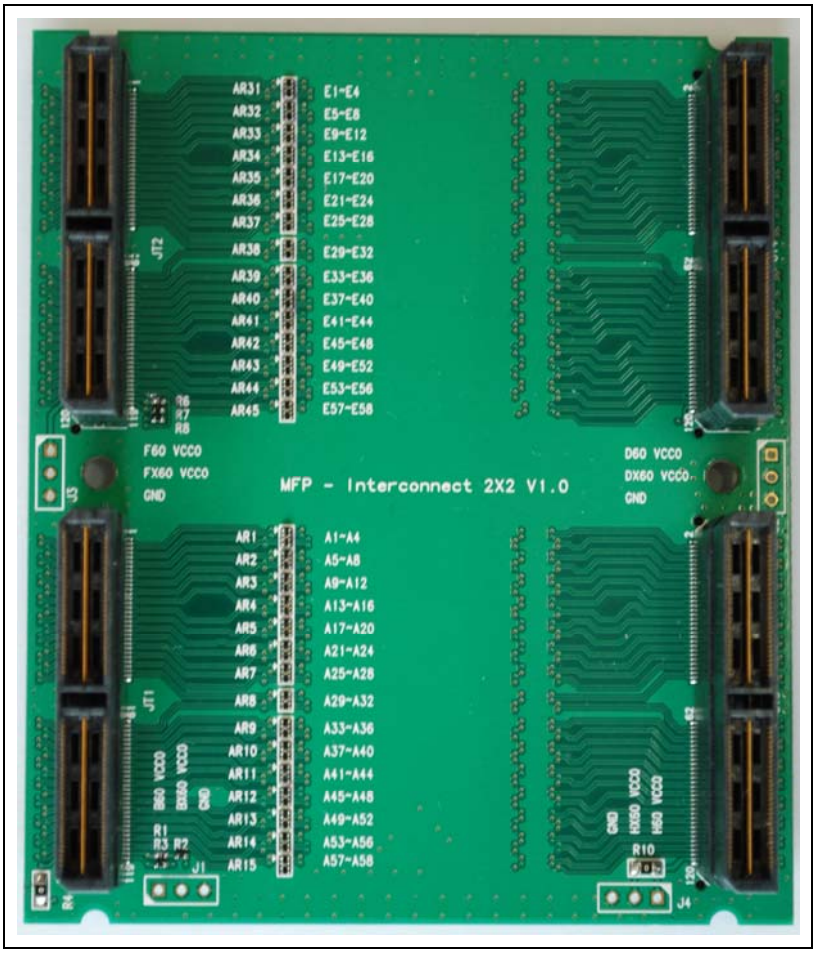


[Interconnect 2x1 Module Rev1.0]



[Interconnect 2x2 Module Rev1.0]

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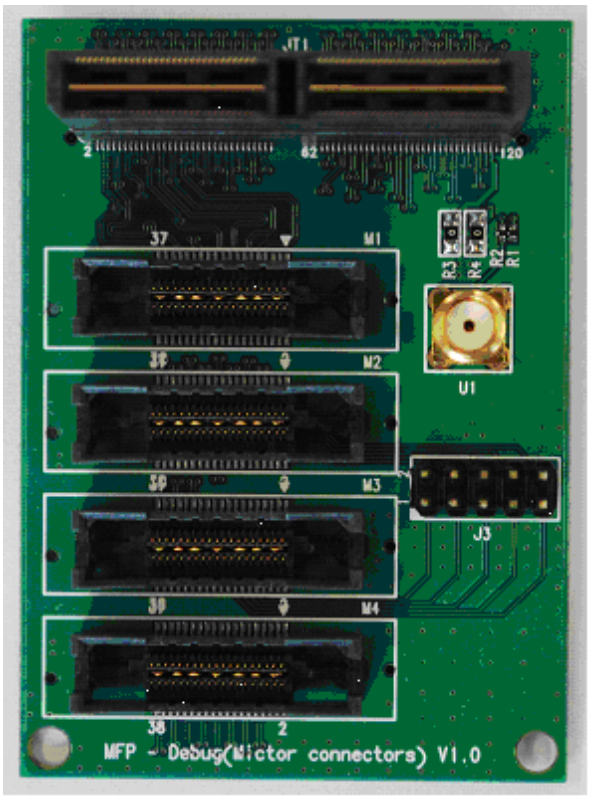

[Debug Module Rev1.0]

[SDR SDRAM Module Rev1.0]

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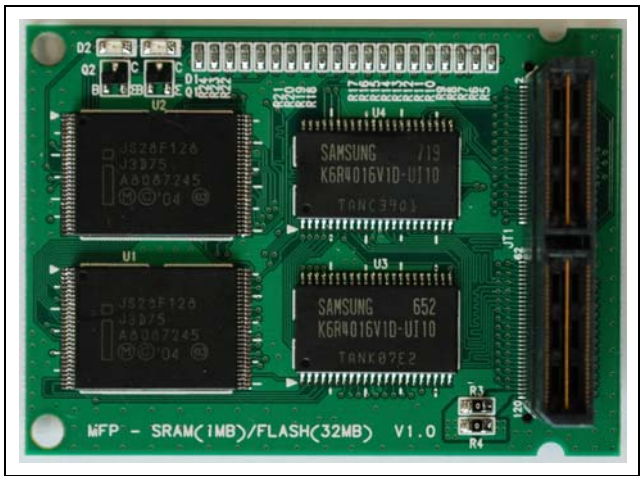
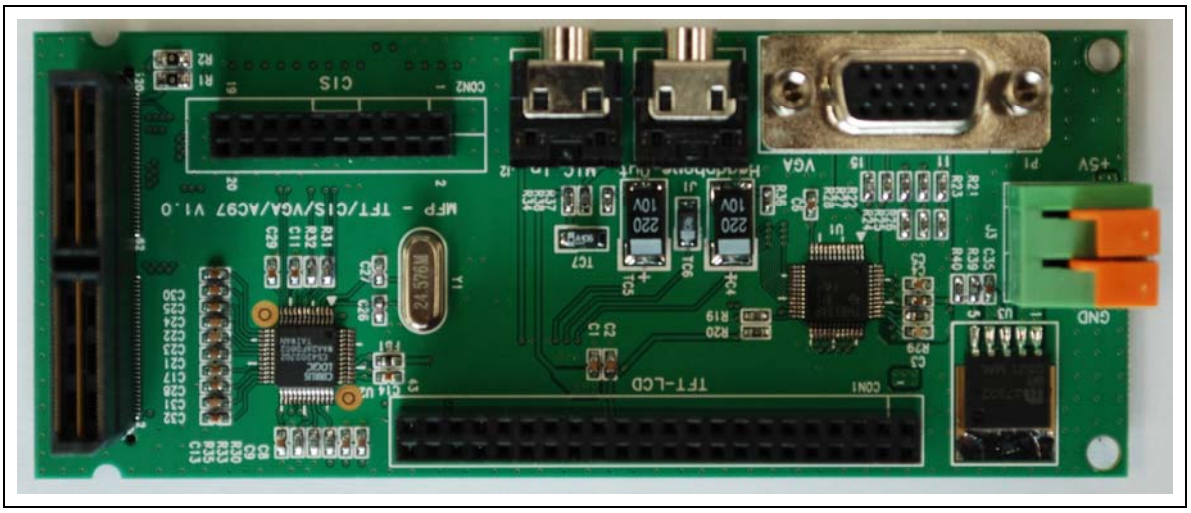


[SRAM / FLASH Module Rev1.0]



[Display/AUDIO Module Rev1.0]

[Communication Module Rev1.0]

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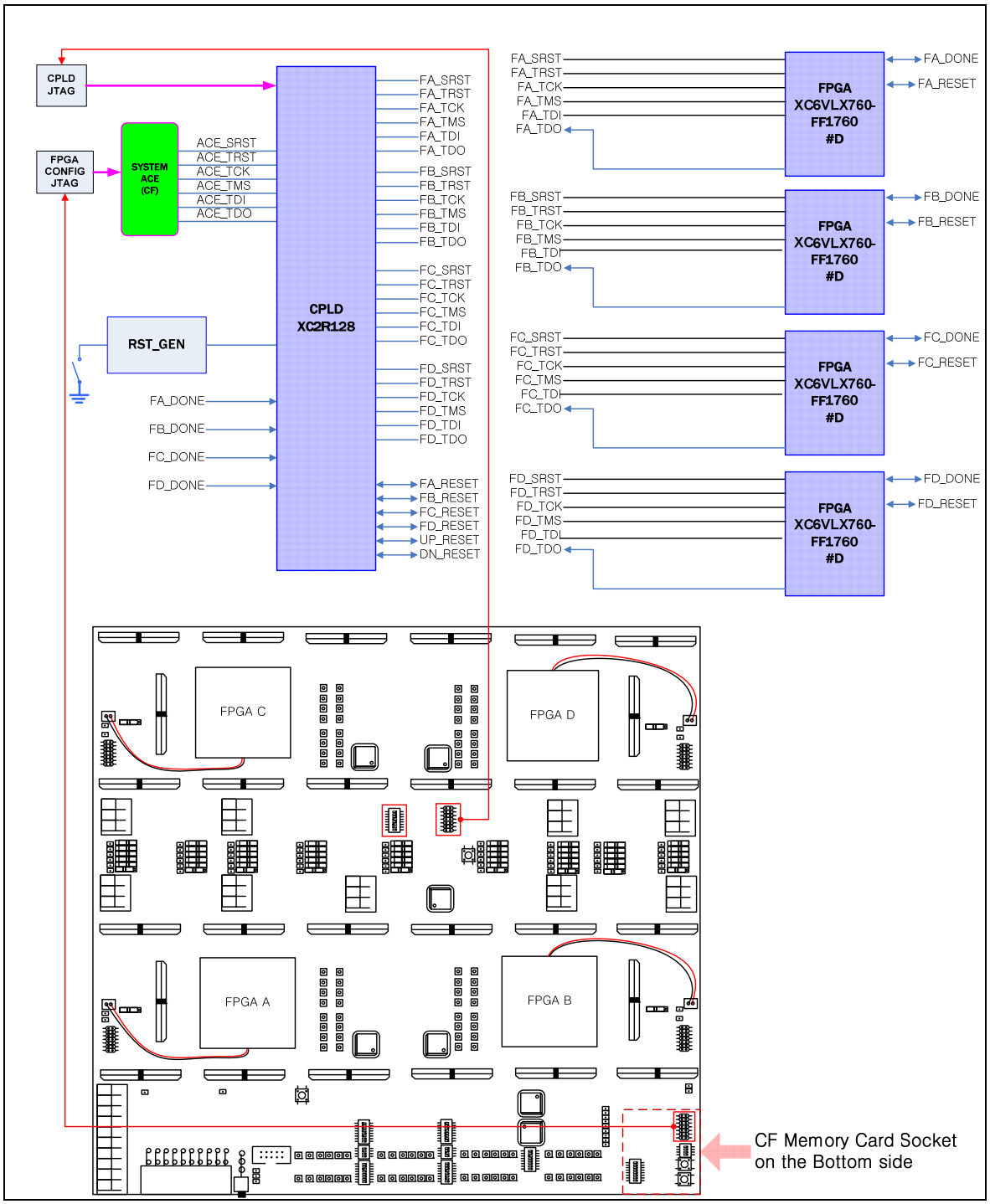
2. Detail description

2.1. FPGA JTAG chain / RESET

2.1.1. Block Diagram

The four FPGA JTAGs are connected to CPLD through SystemACE from JTAG port as follows.



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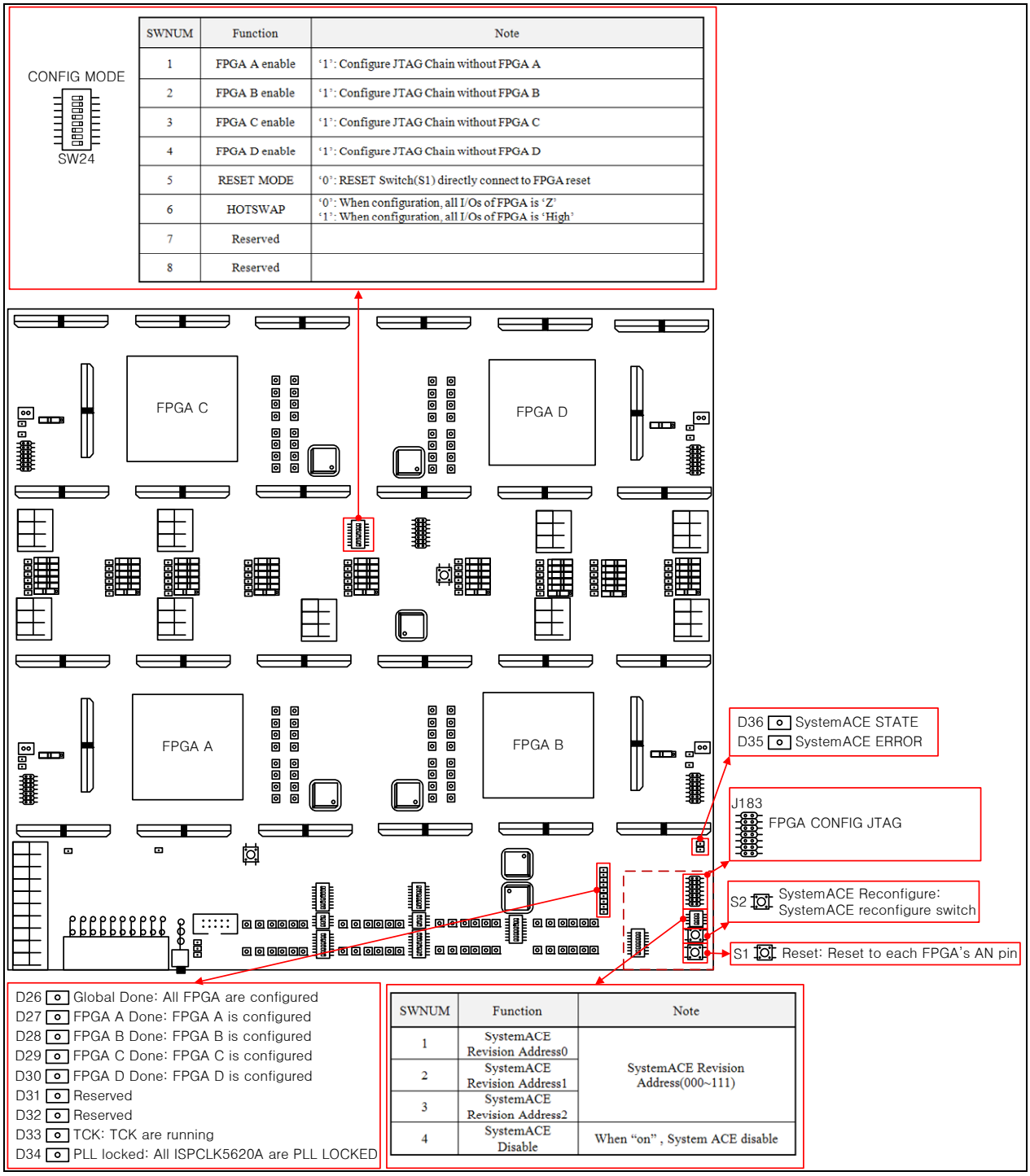
2.1.2. FPGA Configuration Mode

User can change FPGA configuration mode by SW24. User can delete FPGA from JTAG chain by configuration mode switch (SW24). After User can select SW24 #5 for 40ms reset after configuration of all FPGA and SW #6 for FPGA HSWAP.



SWNUM	Function	Note
1	FPGA A enable	'1': Configure JTAG Chain without FPGA A
2	FPGA B enable	'1': Configure JTAG Chain without FPGA B
3	FPGA C enable	'1': Configure JTAG Chain without FPGA C
4	FPGA D enable	'1': Configure JTAG Chain without FPGA D
5	RESET MODE	'0': RESET Switch(S1) directly connect to FPGA reset
6	HOTSWAP	'0': When configuration, all I/Os of FPGA is 'Z' '1': When configuration, all I/Os of FPGA is 'High'
7	Reserved	
8	Reserved	

SWNUM	Function	Note
1	SystemACE Revision Address0	SystemACE Revision Address(000~111)
2	SystemACE Revision Address1	
3	SystemACE Revision Address2	
4	SystemACE Disable	When "on" , System ACE disable

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2.2. CLOCK

In order to minimize clock skew and reflections, the global clocks are distributed through high-speed clock buffers that drive each FPGA on individual board traces. All clock lines are individually length matched to all FPGAs to reduce skew.

The four Global Clocks are generated from the board. The 4 global clock generators (ispclk5620AV) output to 4 FPGAs and external 8 connectors according to predefined profile from reference clock.

The two inputs of reference clocks of ISPCLK5620AV are Programmable Clock (ICS8402) and other two inputs are Oscillator.

The clock connectors on the board are MHF type connector and these are used for input of reference clock and input of external feedback clock and output of external clock.

ISPCLK5620AV is predefined and user cannot change it.

Each FPGA receives Global clock and local input from Oscillator. All FPGAs are connected to 8 External clock output, 4 External clock in/out, and 4 single ended clock in/out connectors through Clock Cable.

■ On-board programmable clock generators(ispClock5620) : 4 ea

- Reference clock input comes from PLL(ICS8402) and oscillator
- Clock output is set by 8pin DIP S/W
- External reference clock input pin : 2 MHF(Micro High Frequency) connectors
- External feedback clock input pin : 2 MHF connectors
- External clock output pins : 8 MHF connectors
- FPGA global clock pin : 8 ea

■ On-board FPGA(Virtex-6 LX760) clock

- 8 global clock pins to each FPGAs :generated by ispClock5620
- 12 clock input/output pins to each FPGAs are connected to 12 MHF connectors and can be selectable as differential or Single Ended clock.
- 4 clock input/output pins to each FPGAs are connected to 4 MHF connectors as Single Ended clock
- 1 clock oscillator sockets to each FPGAs

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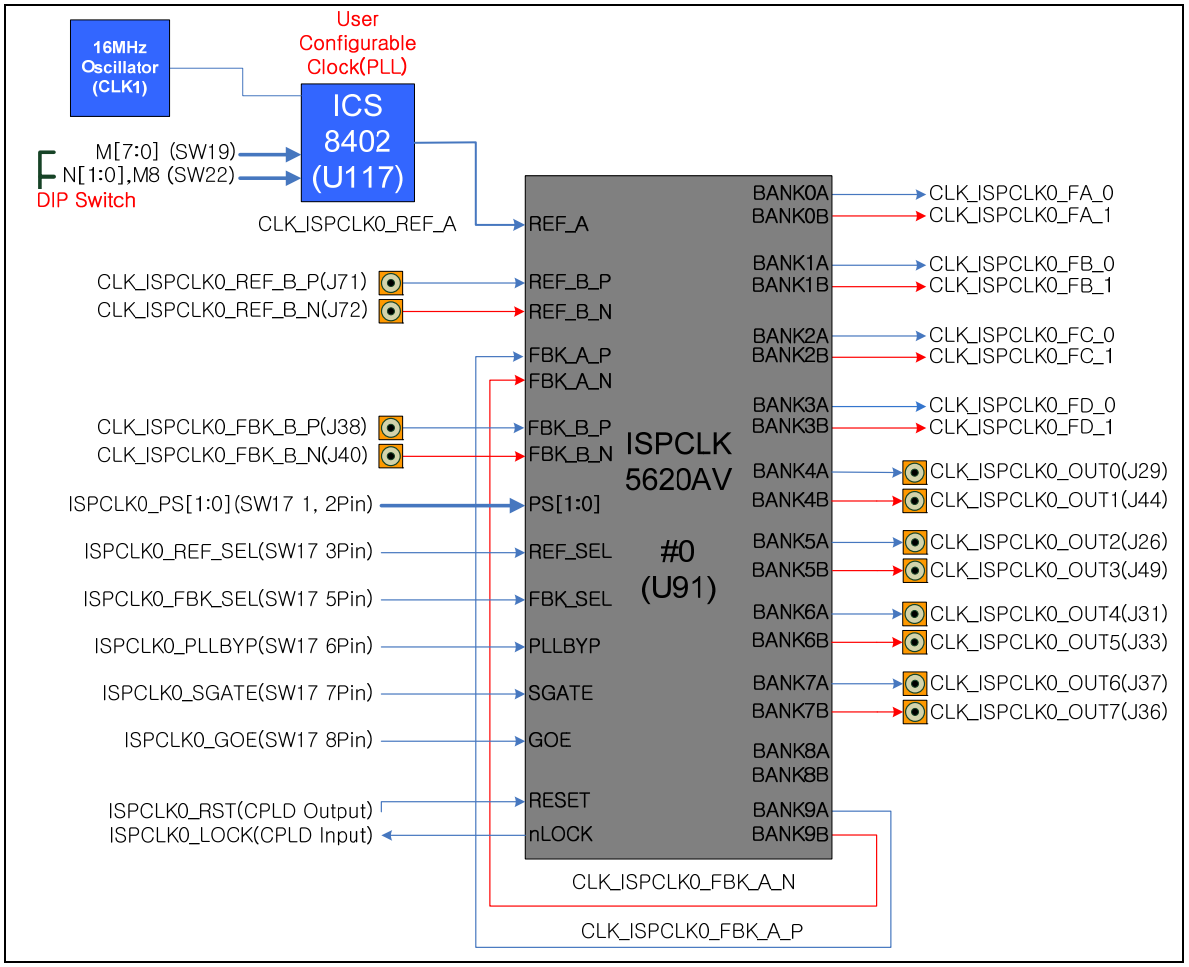
2.2.1. CLOCK Generators

2.2.1.1. CLK0

CLK0 is sourced from ICS8402(Programmable clock) or external clock connector as reference clock by mode switch. The Clock generator output to 4 FPGAs and 8 external connectors.



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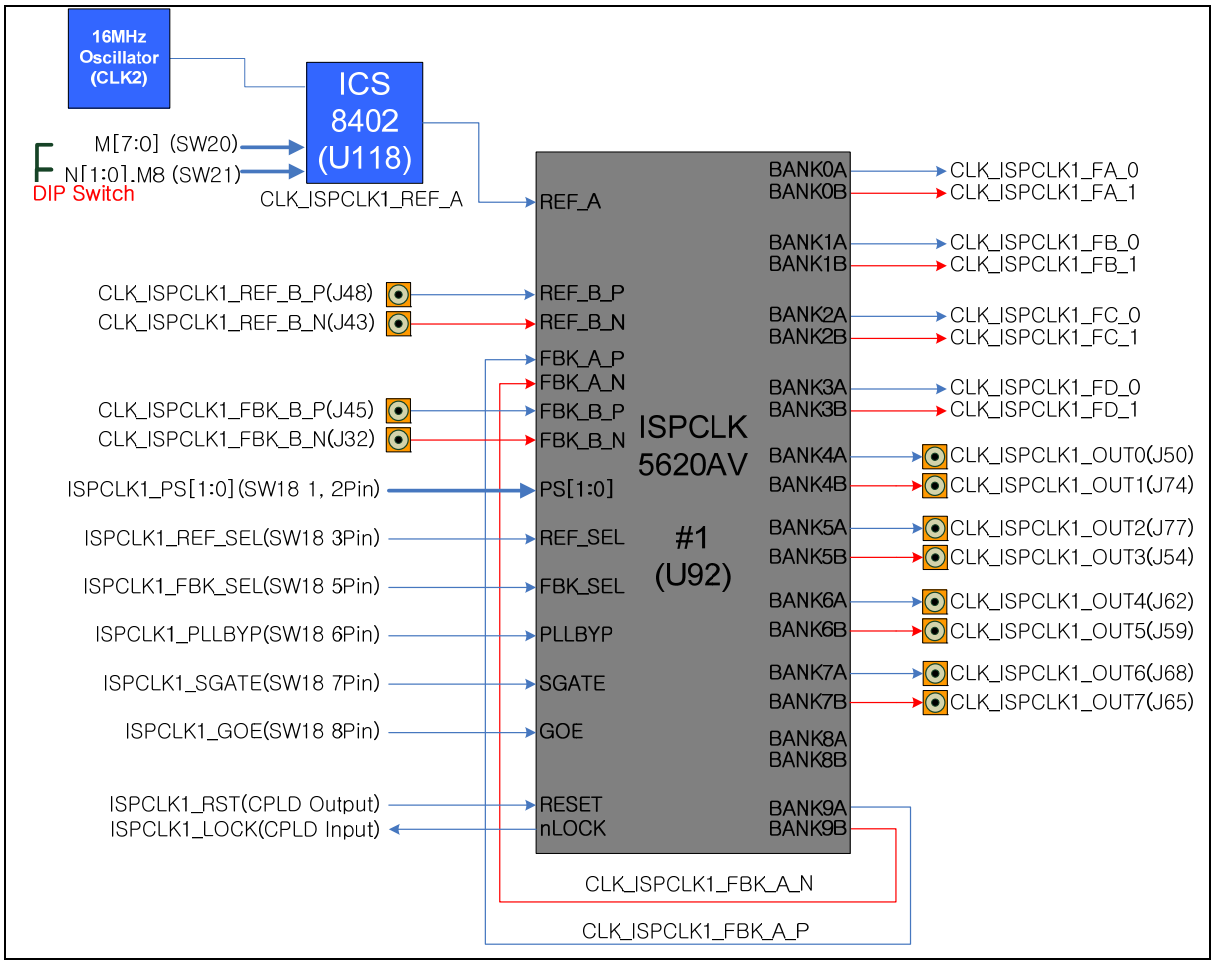
2.2.1.2. CLK1

CLK1 is sourced from ICS8402(Programmable clock) or external clock connector as reference clock by mode switch. The Clock generator output to 4 FPGAs and 8 external connectors.



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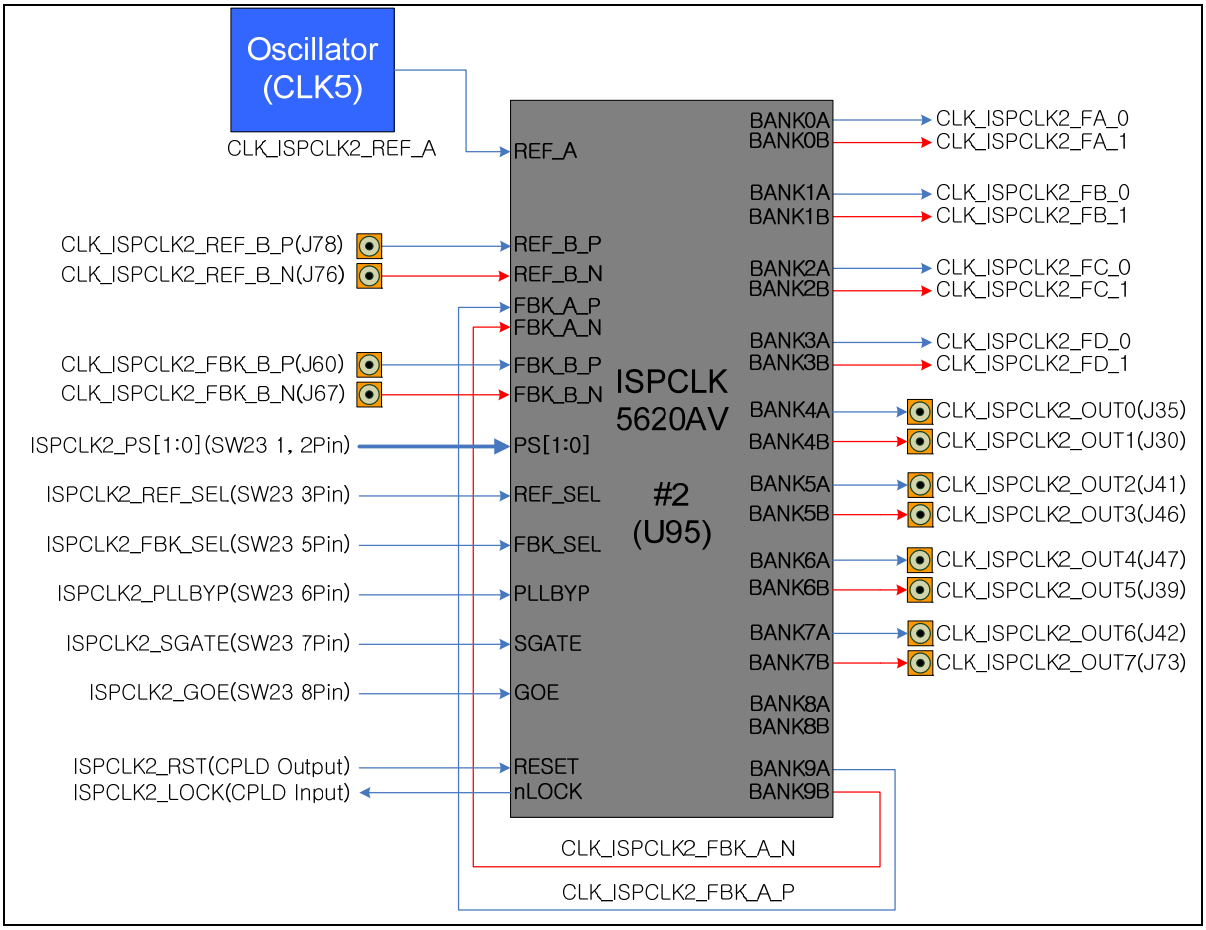
2.2.1.3. CLK2

CLK2 is sourced from Oscillator or external clock connector as reference clock by mode switch. The Clock generator output to 4 FPGAs and 8 external connectors.



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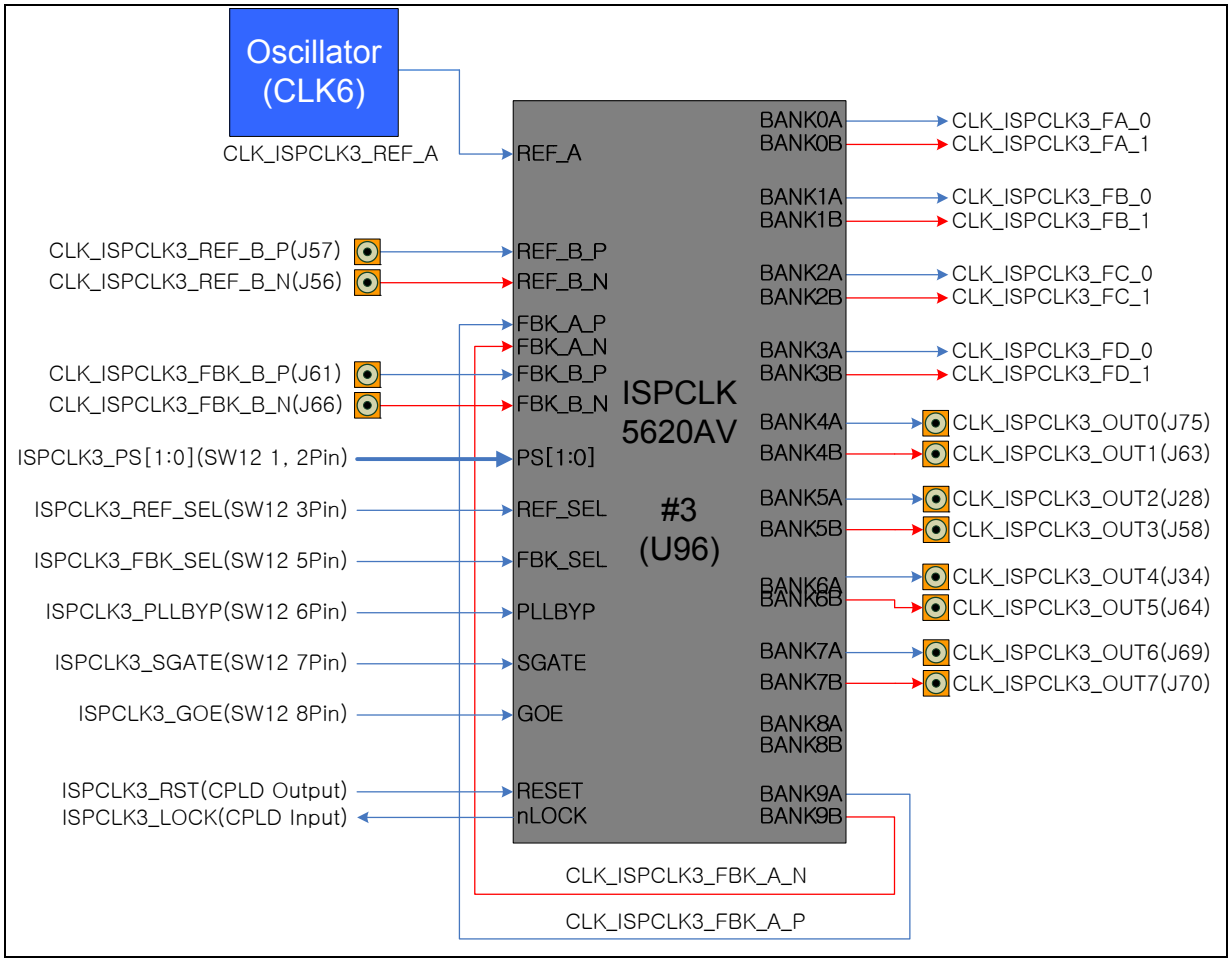
2.2.1.4. CLK3

CLK3 is sourced from Oscillator or external clock connector as reference clock by mode switch. The Clock generator output to 4 FPGAs and 8 external connectors.



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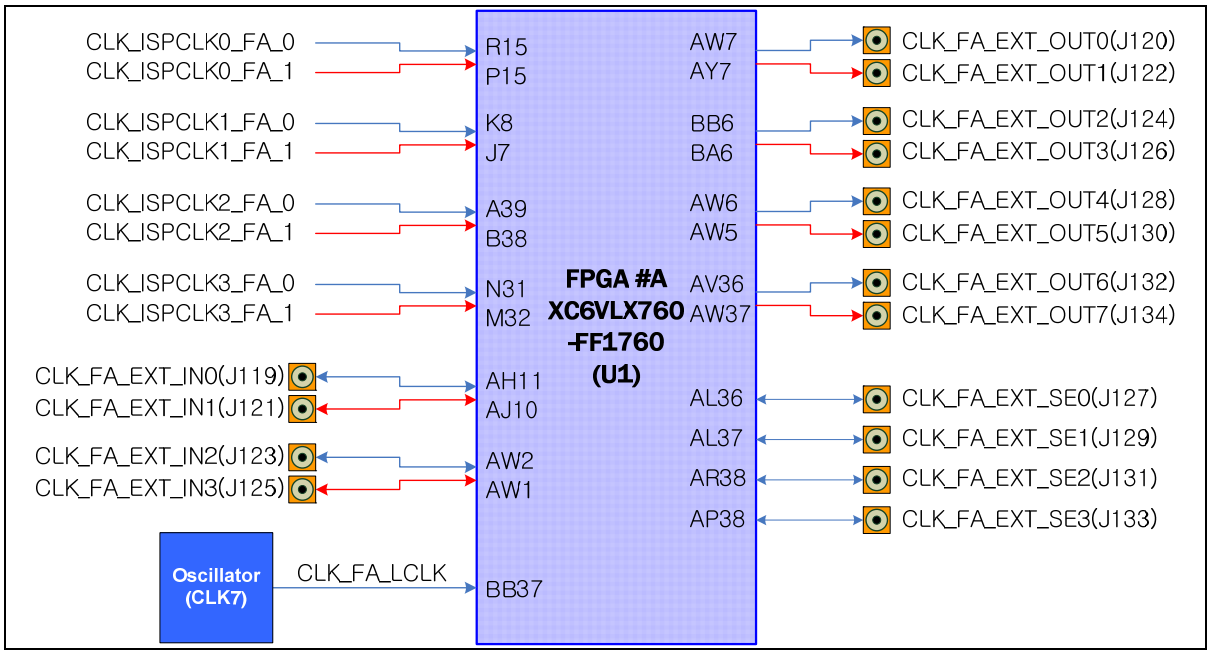
2.2.2. FPGA Clock In/Out

Each FPGA clocks are sourced from Global clock and local clock input (Oscillator). In order to connect another clock, these are connected to 8 External clock output, 4 External clock in/out, 4 single ended clock in/out connectors through Clock Cable.

2.2.2.1. FPGA A



CLK_ISPCLK0_FA_0(P) CLK_ISPCLK0_FA_1(N)	CLK input from Clock Generator0	Differential Signal (Single ended enable)
CLK_ISPCLK1_FA_0(P) CLK_ISPCLK1_FA_1(N)	CLK input from Clock Generator1	
CLK_ISPCLK2_FA_0(P) CLK_ISPCLK2_FA_1(N)	CLK input from Clock Generator2	
CLK_ISPCLK3_FA_0(P) CLK_ISPCLK3_FA_1(N)	CLK input from Clock Generator3	
CLK_FA_EXT_IN0(P) CLK_FA_EXT_IN1(N)	CLK Input / Output Clock Connectors	Differential or Single Ended
CLK_FA_EXT_IN2(P) CLK_FA_EXT_IN3(N)	CLK Input / Output Clock Connectors	Differential or Single Ended
CLK_FA_EXT_OUT0(P) CLK_FA_EXT_OUT1(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FA_EXT_OUT2(P) CLK_FA_EXT_OUT3(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FA_EXT_OUT4(P) CLK_FA_EXT_OUT5(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FA_EXT_OUT6(P) CLK_FA_EXT_OUT7(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FA_EXT_SE0	CLK input from Clock Connector	Single Ended Only
CLK_FA_EXT_SE1	CLK input from Clock Connector	Single Ended Only
CLK_FA_EXT_SE2	CLK input from Clock Connector	Single Ended Only
CLK_FA_EXT_SE3	CLK input from Clock Connector	Single Ended Only
CLK_FA_LCLK	CLK input from Oscillator Socket	Single Ended Only

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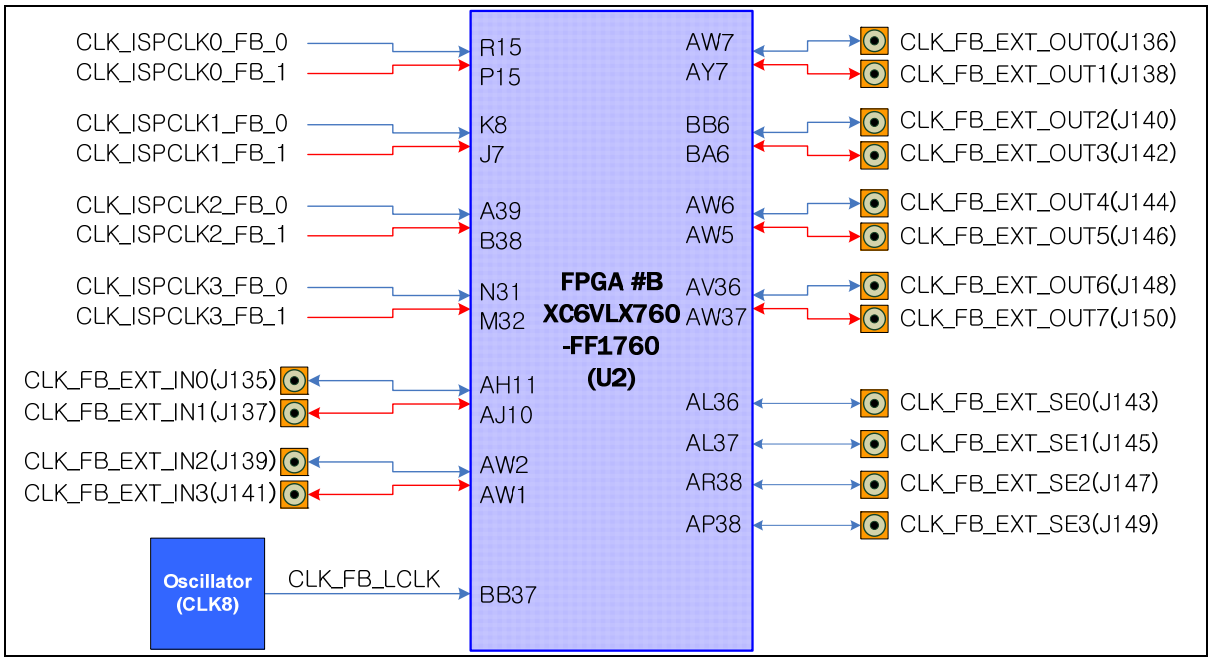
2.2.2.2. FPGA B



CLK_ISPCLK0_FB_0(P) CLK_ISPCLK0_FB_1(N)	CLK input from Clock Generator0	Differential Signal (Single ended enable)
CLK_ISPCLK1_FB_0(P) CLK_ISPCLK1_FB_1(N)	CLK input from Clock Generator1	
CLK_ISPCLK2_FB_0(P) CLK_ISPCLK2_FB_1(N)	CLK input from Clock Generator2	
CLK_ISPCLK3_FB_0(P) CLK_ISPCLK3_FB_1(N)	CLK input from Clock Generator3	
CLK_FB_EXT_IN0(P) CLK_FB_EXT_IN1(N)	CLK Input / Output Clock Connectors	Differential or Single Ended
CLK_FB_EXT_IN2(P) CLK_FB_EXT_IN3(N)	CLK Input / Output Clock Connectors	Differential or Single Ended
CLK_FB_EXT_OUT0(P) CLK_FB_EXT_OUT1(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FB_EXT_OUT2(P) CLK_FB_EXT_OUT3(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FB_EXT_OUT4(P) CLK_FB_EXT_OUT5(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FB_EXT_OUT6(P) CLK_FB_EXT_OUT7(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FB_EXT_SE0	CLK input from Clock Connector	Single Ended Only
CLK_FB_EXT_SE1	CLK input from Clock Connector	Single Ended Only
CLK_FB_EXT_SE2	CLK input from Clock Connector	Single Ended Only
CLK_FB_EXT_SE3	CLK input from Clock Connector	Single Ended Only
CLK_FB_LCLK	CLK input from Oscillator Socket	Single Ended Only

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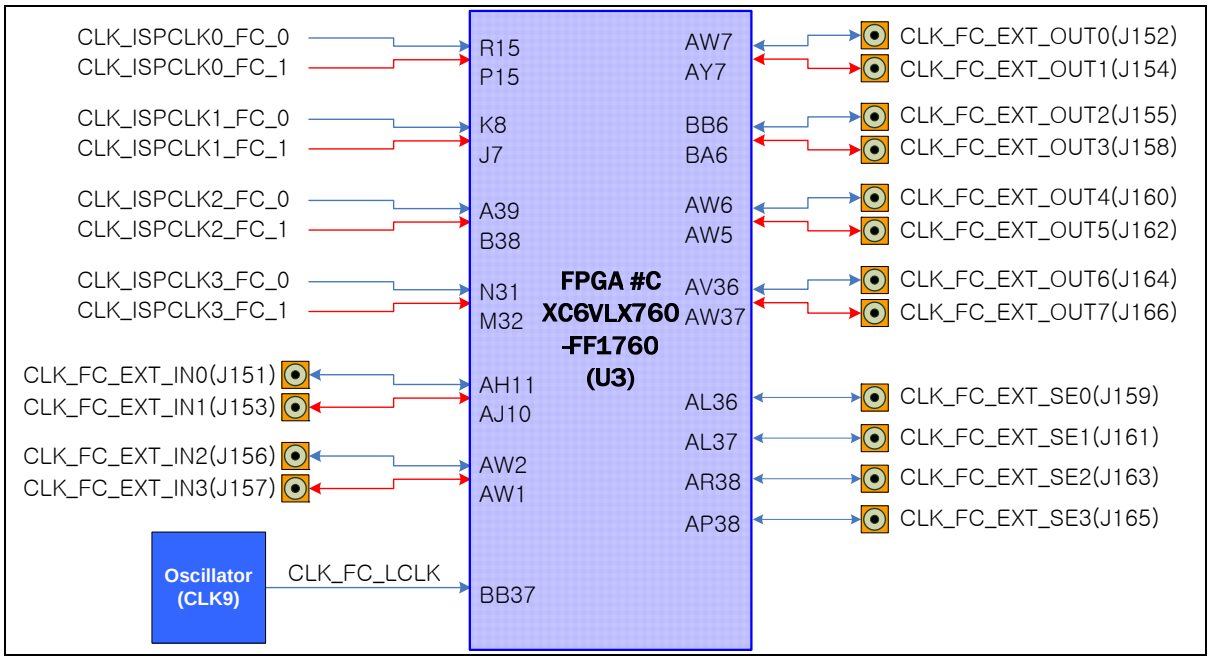
2.2.2.3. FPGA C



CLK_ISPCLK0_FC_0(P) CLK_ISPCLK0_FC_1(N)	CLK input from Clock Generator0	Differential Signal (Single ended enable)
CLK_ISPCLK1_FC_0(P) CLK_ISPCLK1_FC_1(N)	CLK input from Clock Generator1	
CLK_ISPCLK2_FC_0(P) CLK_ISPCLK2_FC_1(N)	CLK input from Clock Generator2	
CLK_ISPCLK3_FC_0(P) CLK_ISPCLK3_FC_1(N)	CLK input from Clock Generator3	
CLK_FC_EXT_IN0(P) CLK_FC_EXT_IN1(N)	CLK Input / Output Clock Connectors	Differential or Single Ended
CLK_FC_EXT_IN2(P) CLK_FC_EXT_IN3(N)	CLK Input / Output Clock Connectors	Differential or Single Ended
CLK_FC_EXT_OUT0(P) CLK_FC_EXT_OUT1(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FC_EXT_OUT2(P) CLK_FC_EXT_OUT3(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FC_EXT_OUT4(P) CLK_FC_EXT_OUT5(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FC_EXT_OUT6(P) CLK_FC_EXT_OUT7(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FC_EXT_SE0	CLK input from Clock Connector	Single Ended Only
CLK_FC_EXT_SE1	CLK input from Clock Connector	Single Ended Only
CLK_FC_EXT_SE2	CLK input from Clock Connector	Single Ended Only
CLK_FC_EXT_SE3	CLK input from Clock Connector	Single Ended Only
CLK_FC_LCLK	CLK input from Oscillator Socket	Single Ended Only

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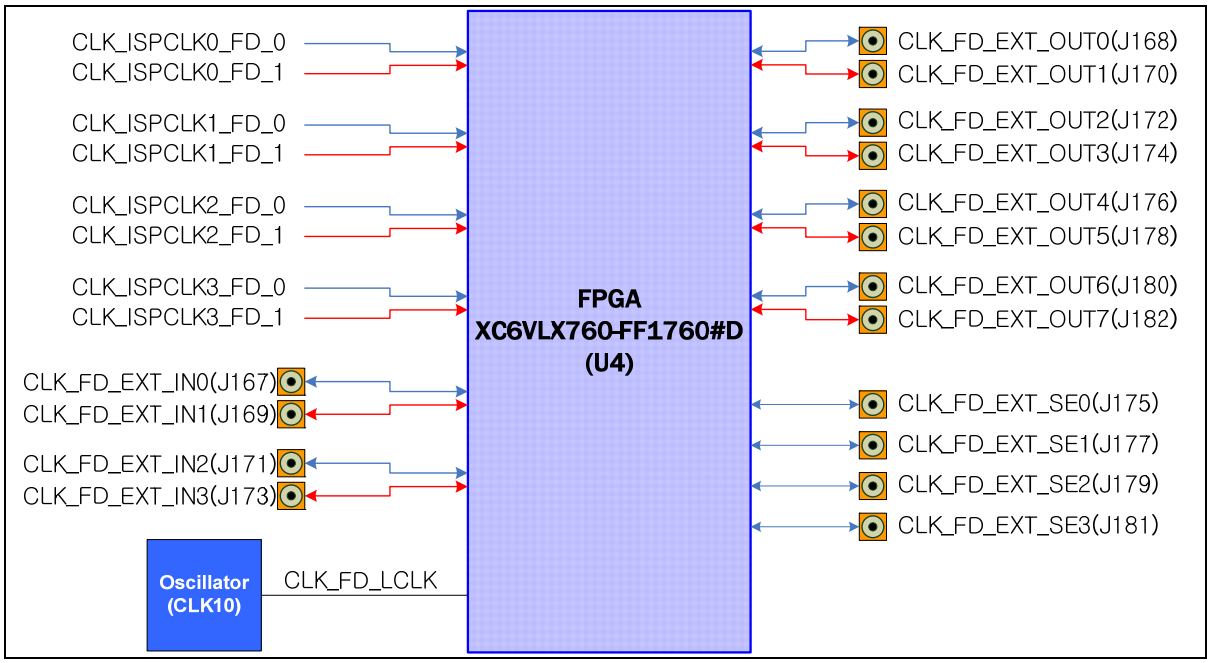
2.2.2.4. FPGA D



CLK_ISPCLK0_FD_0(P) CLK_ISPCLK0_FD_1(N)	CLK input from Clock Generator0	Differential Signal (Single ended enable)
CLK_ISPCLK1_FD_0(P) CLK_ISPCLK1_FD_1(N)	CLK input from Clock Generator1	
CLK_ISPCLK2_FD_0(P) CLK_ISPCLK2_FD_1(N)	CLK input from Clock Generator2	
CLK_ISPCLK3_FD_0(P) CLK_ISPCLK3_FD_1(N)	CLK input from Clock Generator3	
CLK_FD_EXT_IN0(P) CLK_FD_EXT_IN1(N)	CLK Input / Output Clock Connectors	Differential or Single Ended
CLK_FD_EXT_IN2(P) CLK_FD_EXT_IN3(N)	CLK Input / Output Clock Connectors	Differential or Single Ended
CLK_FD_EXT_OUT0(P) CLK_FD_EXT_OUT1(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FD_EXT_OUT2(P) CLK_FD_EXT_OUT3(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FD_EXT_OUT4(P) CLK_FD_EXT_OUT5(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FD_EXT_OUT6(P) CLK_FD_EXT_OUT7(N)	CLK ouput to Clock Connectors	Differential or Single Ended
CLK_FD_EXT_SE0	CLK input from Clock Connector	Single Ended Only
CLK_FD_EXT_SE1	CLK input from Clock Connector	Single Ended Only
CLK_FD_EXT_SE2	CLK input from Clock Connector	Single Ended Only
CLK_FD_EXT_SE3	CLK input from Clock Connector	Single Ended Only
CLK_FD_LCLK	CLK input from Oscillator Socket	Single Ended Only

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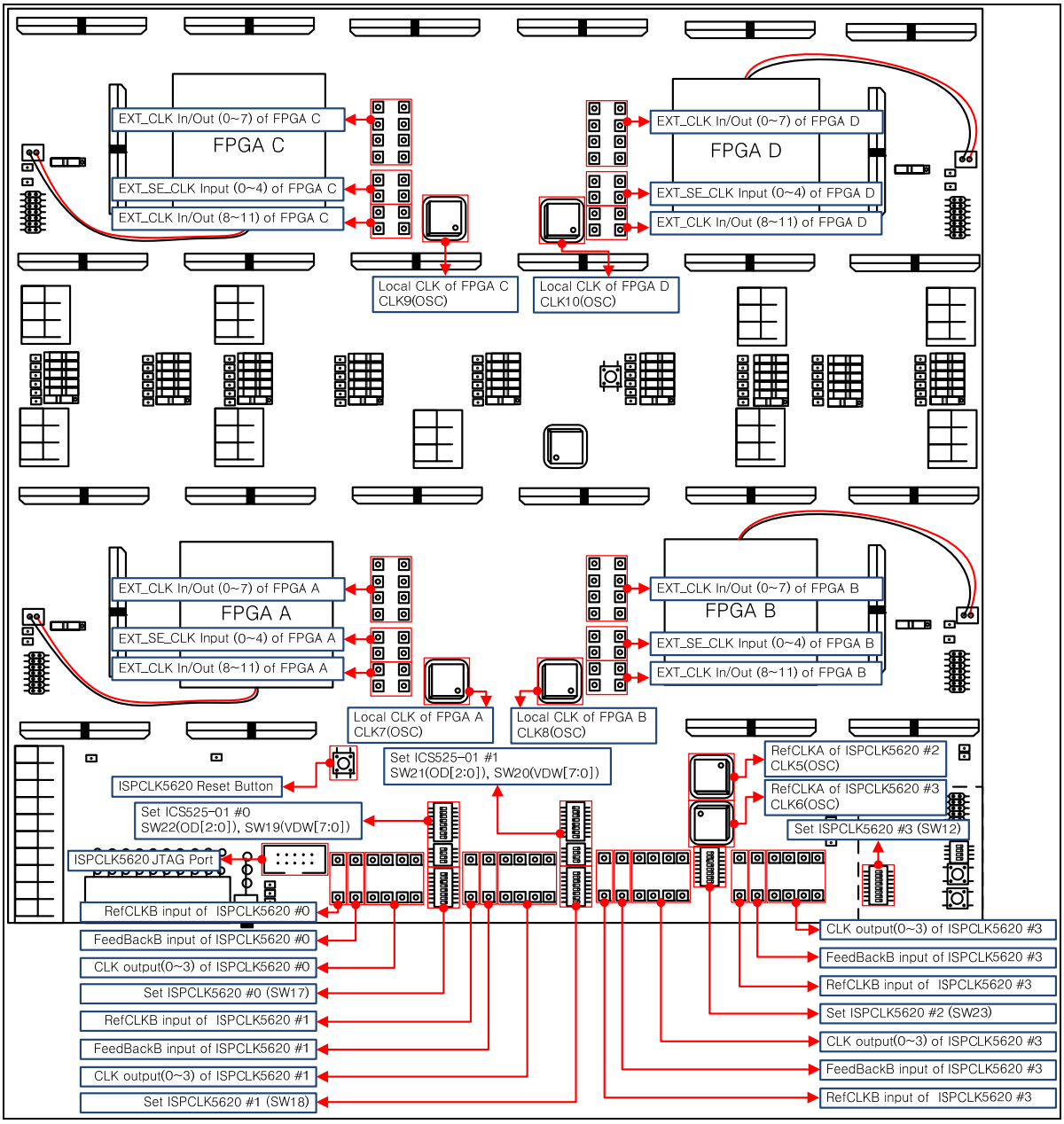
2.2.3. Clock Connectors / Sockets / Adjustment Switchs



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2.2.4. ISPCLK5620AV

ISPCLK5620AV is a Programmable clock generator that receives reference clock input. It distributes clocks according to predefined Profile. It can be selected by "Profile select mode", "PLL bypass mode" and "Reference clock select mode", "output control".

(1) ISPCLK5620AV Adjustment switch

Switch NUMBER	SW17	SW18	SW23	SW12
ISPCLK5620AV	#0	#1	#2	#3
CLK_SIGANL	ISP_CLK0	ISP_CLK1	ISP_CLK2	ISP_CLK3

(2) ISPCLK5620AV Adjustment switch pins

Switch NUM	1	2	3	4	5	6	7	8
Function	GOE	SGATE	PLL_BYP	FB_SEL		REF_SEL	PS1	PS0
Note							Profile Select	

SWNUM	Function	Note
8	PS0	Profile select "00" PS0, "10" PS1, "01" PS2, "11" PS3
7	PS1	
6	REF SEL	Reference Clock select "0" : REF_A ISPCLK0 : PLL(ICS8401) / U117 ISPCLK1 : PLL(ICS8401) / U118 ISPCLK2 : OSC Socket / CLK5 ISPCLK3 : OSC Socket / CLK6 "1" : REF_B ISPCLK0 : J71 / J72 ISPCLK1 : J48 / J43 ISPCLK2 : J78 / J76 ISPCLK3 : J57 / J56
5	NC	
4	FB SEL	Feedback Clock select "0" : REF_A On board loop from ISPCLK output BANK#8 "1" : REF_B ISPCLK0 : J38 / J40 ISPCLK1 : J45 / J32 ISPCLK2 : J60 / J67 ISPCLK3 : J61 / J66
3	PLL BYP	ISPCLK5620AV PLL Bypass "0" PLL active mode "1" PLL Bypass mode
2	SGATE	ISPCLK5620A SGATE (synchronous output control)
1	GOE	ISPCLK5620A GOE (global output enable) "0" BANKxA and BANKxB : clock "1" BANKxA and BANKxB : high impedance

※ "1" when SW on(up), "0" when SW off(down)

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(3) ISPCLK5620AV Profile setting

PLL_Bypass	Profile Select	ISPCLK_TO_FPGA	EXT_OUT_0/1/2/3
0	00	REF_CLK x 2	REF_CLK x 2
0	01	REF_CLK x 1	REF_CLK x 1
0	10	REF_CLK / 4	REF_CLK / 4
0	11	Reserved	
1	00	REF_CLK x 1	REF_CLK x 1
1	01	REF_CLK / 2	REF_CLK / 2
1	10	REF_CLK / 8	REF_CLK / 8
1	11	Reserved	

2.2.5. ICS8402 Frequency Synthesizer

ICS8402 is a Programmable clock. It receives reference clock and generate clock from the value of "M and N".

(1) ICS8402 Adjustment

SW22	SW19	SW21	SW20
Reference CLK_A Of ISPCLK0		Reference CLK_A Of ISPCLK1	
N[1:0],Vco_sel,M[8]	M[7:0] M Divider	N[1:0], Vco_sel, M[8]	M[7:0]

SWNUM SW22, SW21	Function	Note
1	N[1]	ICS8402 Output Divider(N Divider) 00 : CLK_out / 2 01 : CLK_out / 4 10 : CLK_out / 8 11 : CLK_out / 16
2	N[0]	
3	VCO_sel	ICS8402 VCO select 0 : VCO bypass ICS8402 Output_clk = Input_clk / N_divider 1 : VCO Active ICS8402 Output_clk = Input_clk × M / N_divider
4	M[8]	ICS8402 M divider digit 8

※ "1" when SW on(up), "0" when SW off(down)

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2.2.6. CLOCK Generation Range

The ICS8402 and ISPCLK5620AV have clock output ranges. The step to set max/min clock ranges is shown as table.

[Table of Clock range when reference clk of ICS8402 is 16MHz]

ref clk	ICS8402					ISP5620A		Gclk_out		
	M		N	Fout		pll bypass	P S			
	min	max		min	max			min	max	Step(MHz)
16	16	43	2	128	344	1	0	128	344	8
16	16	43	4	64	172	1	0	64	172	4
16	16	43	8	32	86	1	0	32	86	2
16	16	43	16	16	43	1	0	16	43	1
16	16	43	2	128	344	1	1	64	172	4
16	16	43	4	64	172	1	1	32	86	2
16	16	43	8	32	86	1	1	16	43	1
16	16	43	16	16	43	1	1	8	21.5	0.5
16	16	43	2	128	344	1	2	16	43	1
16	16	43	4	64	172	1	2	8	21.5	0.5
16	16	43	8	32	86	1	2	4	10.75	0.25
16	16	43	16	16	43	1	2	2	5.375	0.125
16	16	25	2	128	200	0	0	256	400	16
16	20	43	4	80	172	0	0	160	344	8
16	40	43	8	80	86	0	0	160	172	4
16	16	43	16	16	43	0	0	32	86	2
16	16	25	2	128	200	0	1	128	200	8
16	20	43	4	80	172	0	1	80	172	4
16	40	43	8	80	86	0	1	80	86	2
16	16	43	16	16	43	0	1	16	43	1
16	20	43	2	160	344	0	2	40	86	2
16	40	43	4	160	172	0	2	40	43	1
16	16	43	8	32	86	0	2	8	21.5	0.5
16	16	43	16	16	43	0	2	4	10.75	0.25

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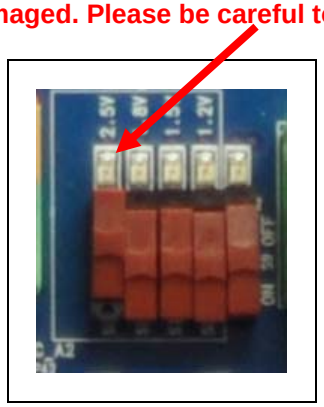
2.3. VCCO selection

Be careful to use the MFP-LX-760Q. It is very sensitive to static discharge and make sure that you're properly grounded whenever handling the board directly.

MFP-LX-760-Q has 9 VCCO regions (VCC_A2, VCC_C5, VCC_A45C12, VCC_C6D4, VCC_A6B4C3D1, VCC_A3B1, VCC_B56D23, VCC_B2, VCC_D5) on the board. Each VCCO region has 5 red VCCO selecting switches (five red slide switches). User can adjust the VCCO voltage as 2.5/1.8/1.5/1.2V with that switches.

When a VCCO selecting switch is set a corresponding LED will be turned on. If 2.5V switch is set, the LED marked 2.5V will be light.

- **Never set more than two switches simultaneously.**
- **User has to select only one V_{CCO} of 2.5V/1.8V/1.5V/1.2V unless the LX760 FPGA I/O block may be permanently damaged. Please be careful to set only ONE switch!**



- **Never change the Vcco Selection switchs while power on.**
- **Before VCCO selection, check Voltage of daughter cards.**

If any other voltage except 2.5/1.8/1.5/1.2V is required, MFP-LX760Q board power switch **should be turned off** before supplying external power via the VCCO power connectors.

User needs to be careful to **set a suitable voltage** of daughter board. User needs to **check the same voltage** on daughter board through I/O connectors ! Don't use different voltages on the connecting daughter boards.

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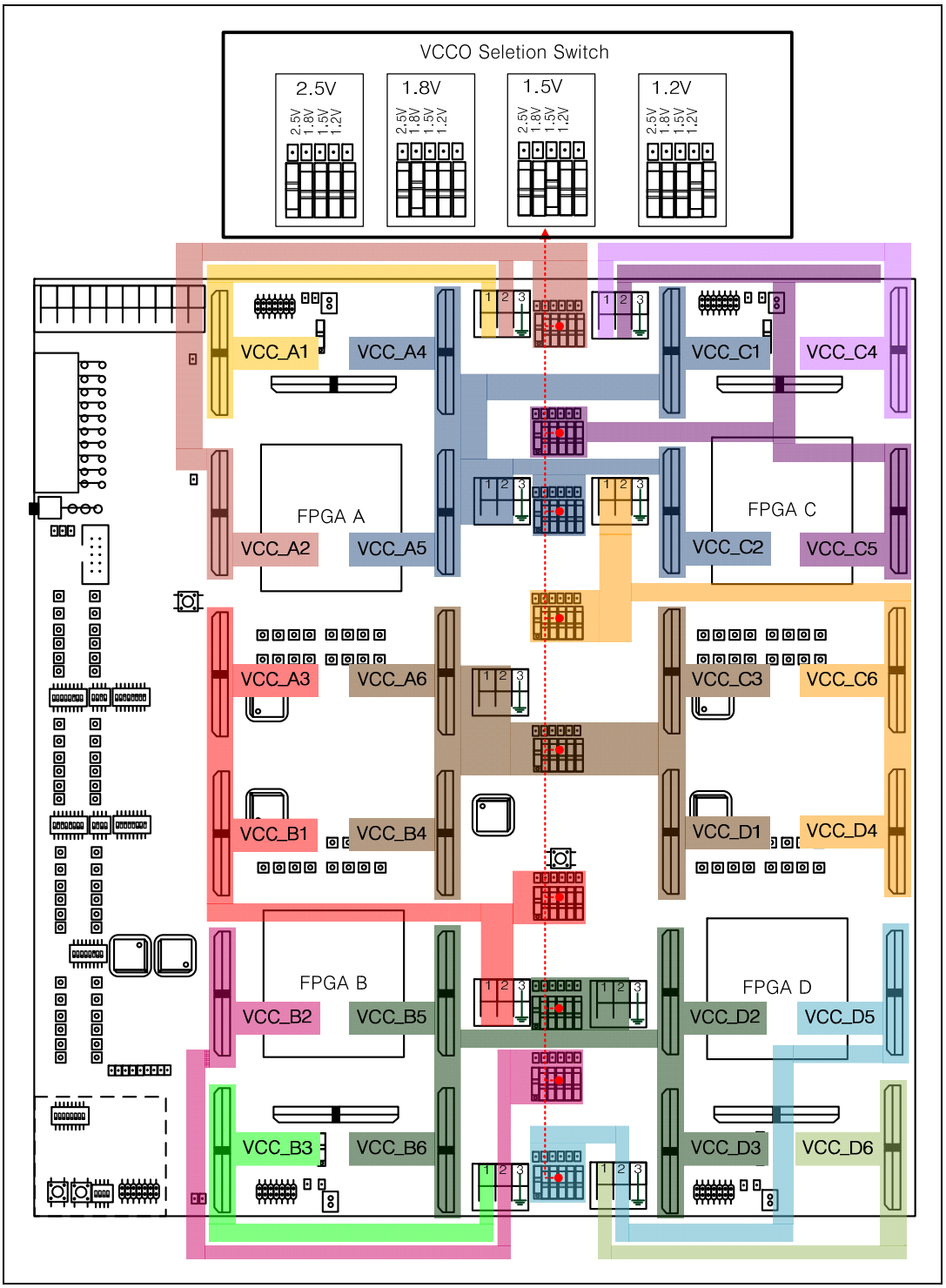

WARNING

Only one of the VCCO selection switch should be in the LED "on" state
Never change the Vcco Selection switch while power on.
Before VCCO selection, check Voltage of daughter cards.
User has to select one V_{CCO} of 2.5V/1.8V/1.5V/1.2V.

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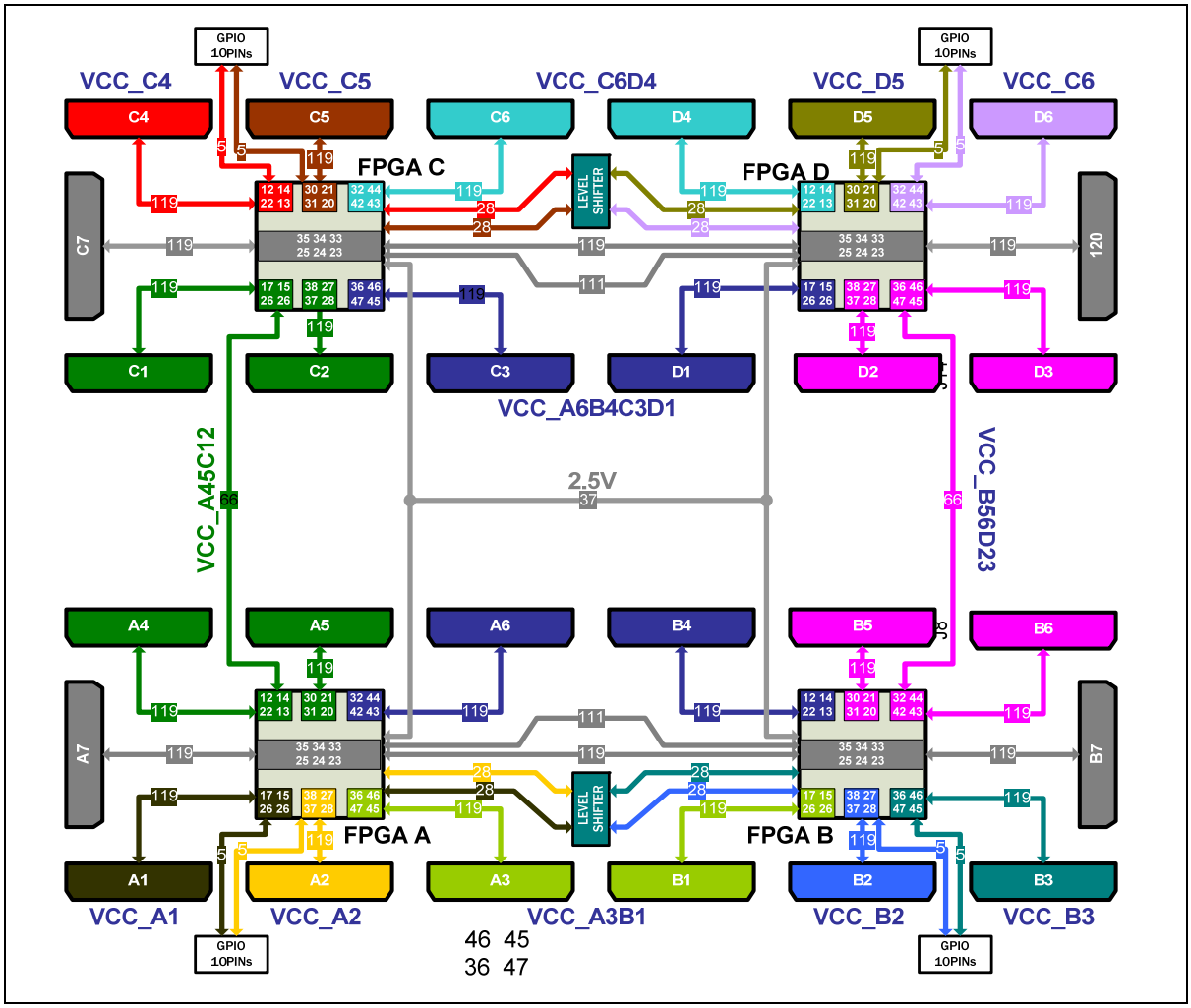
2.4. FPGA BANK VCCO Regions

There are 14 FPGA Bank VCCO Regions. These are assigned to each connectors and FPGA. The 9 of 14 (**VCCA2,VCC_B2,VCC_C5,VCC_D5, VCC_A3B1, VCC_C6D4,VCCA45C12, VCC_B56D23, VCC_A6B4,C3,D1**) have optional VCCO voltages(2.5/1.8/1.5/1,2V).

The 4 of 14 (**VCC_A1,VCC_B3,VCC_C4,VCC_D6**) are useful for connecting other voltage.

The 1 of 14 (Connector **A7, B7, C7, D7**) is tied up to 2.5V.



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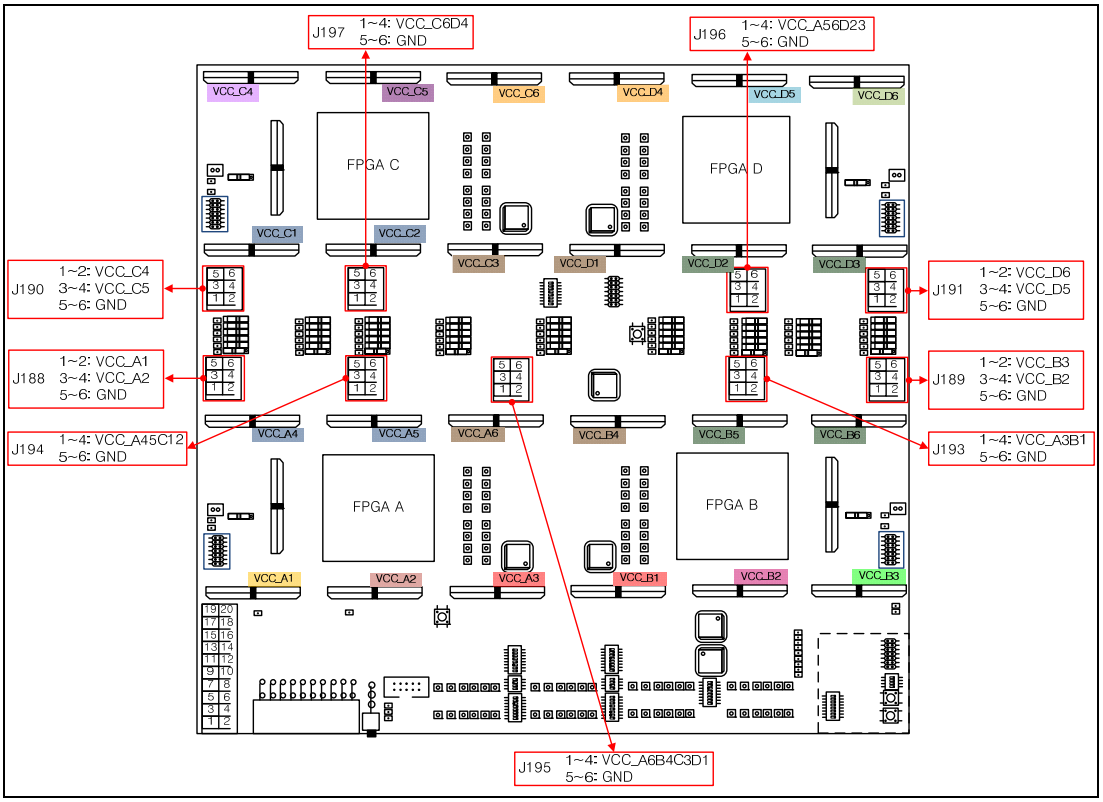
2.5. VCCO connectors

There are 9 VCCO outputs. The VCC_A1, VCC_B3, VCC_C4, VCC_D6 of 9 VCCO should be connected to other VCCO. When MFP-LX760-Q is delivered, The VCC_A1 is connected to VCC_A2, VCC_B3 is connected to VCC_B2, VCC_C4 is connected to VCC_C5, VCC_D6 is connected to VCCD5.



J188	1~2 : VCC_A1, 3~4 : VCC_A2, 5~6 : GND	Transmitting external power to A1 and A2 or connecting A1 with A2.
J189	1~2 : VCC_B3, 3~4 : VCC_B2, 5~6 : GND	Transmitting external power to B2 and B3 or connecting B2 with B3.
J190	1~2 : VCC_C4, 3~4 : VCC_C5, 5~6 : GND	Transmitting external power to C4 and C5 or connecting C4 with C5.
J191	1~2 : VCC_D6, 3~4 : VCC_D5, 5~6 : GND	Transmitting external power to D5 and D6 or connecting D5 with D6.
J193	1~4 : VCC_A3B1, 5~6 : GND	Transmitting external power to A3 and B1 or transmitting the power of A3 and B1 to external.
J194	1~4 : VCC_A45C12, 5~6 : GND	Transmitting external power to A4, A5, C1 and C2 or transmitting the power of A4, A5, C1 and C2 to external.
J195	1~4 : VCC_A6B4C3D1, 5~6 : GND	Transmitting external power to A6, B4, C3 and D1 or transmitting the power of A6, B4, C3 and D1 to external.
J196	1~4 : VCC_B56D23, 5~6 : GND	Transmitting external power to B5, B6, D2 and D3 or transmitting the power of B5, B6, D2 and D3 to external.
J197	1~4 : VCC_C6D4, 5~6 : GND	Transmitting external power to C6 and D4 or transmitting the power of C6 and D4 to external.

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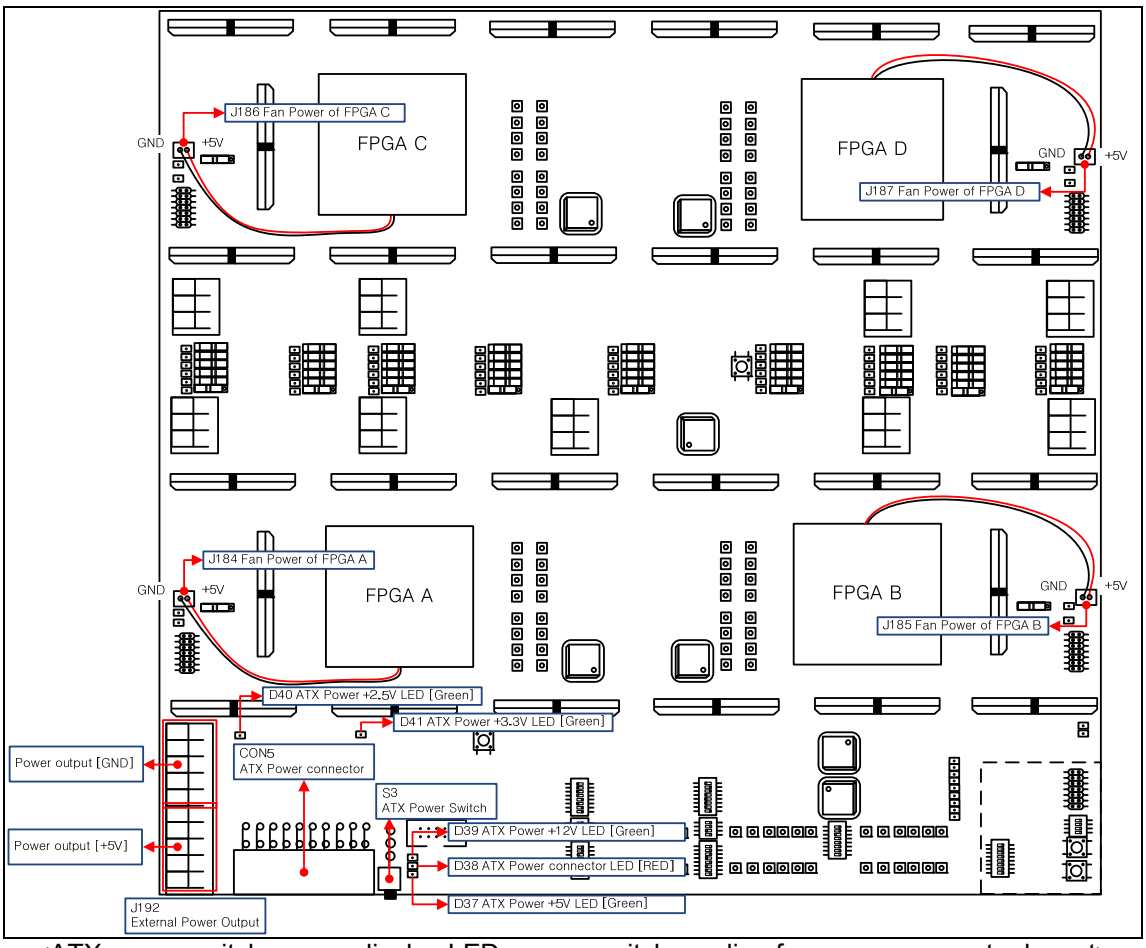
2.6. Board Power

MFP-LX760-Q is using ATX Power supply. There are LEDs on the board for Power "ON".

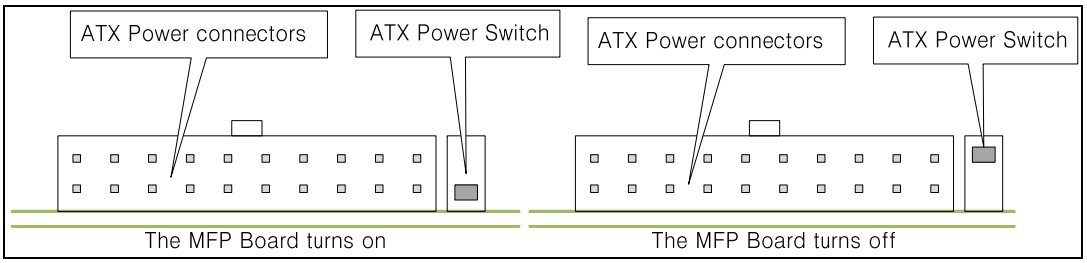


<ATX power switch, power display LED, power switch, cooling fan power connector layout>

J184/J185/J186/J187/J192 is +5V output connector. J184/J185/J186/J187 connector is power for cooling fan for FPGA. J192 connector is power for daughter boards.

The D38 LED (RED) is on if ATX power is off and connected to MFP-LX760-Q board. The D39 LED(Green:+12V) and D37 LED(Green :+5V) are on if ATX Power is on.

S3 switch should be down if ATX power is on.



<Handling the ATX Power Switch>

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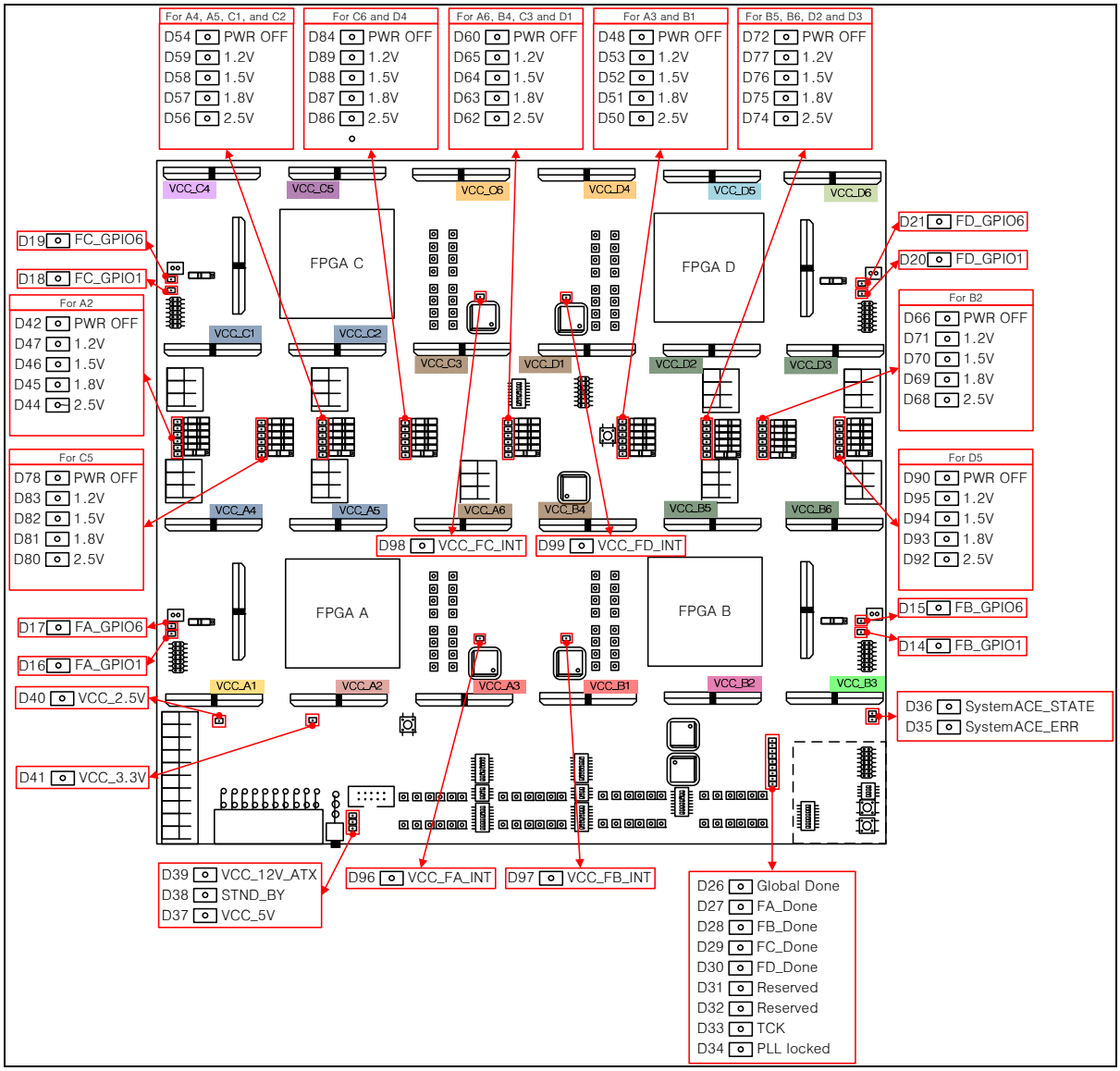
2.7. LEDs

LEDs on the board indicate status of FPGA and power.



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NUMBER	Silk	Description
D14	FB_GPIO1	First pin of [FPGA B] GPIO is high.
D15	FB_GPIO6	Sixth pin of [FPGA B] GPIO is high.
D16	FA_GPIO1	First pin of [FPGA A] GPIO is high
D17	FA_GPIO6	Sixth pin of [FPGA A] GPIO is high
D18	FC_GPIO1	First pin of [FPGA C] GPIO is high.
D19	FC_GPIO6	Sixth pin of [FPGA C] GPIO is high.
D20	FD_GPIO1	First pin of [FPGA D] GPIO is high
D21	FD_GPIO6	Sixth pin of [FPGA D] GPIO is high
D26	GLOBAL DONE	After All FPGAs are rightly programmed, they are operating.
D27	FA_DONE	[FPGA A] is rightly programmed, it is operating.
D28	FB_DONE	[FPGA B] is rightly programmed, it is operating.
D29	FC_DONE	[FPGA C] is rightly programmed, it is operating.
D30	FD_DONE	[FPGA D] is rightly programmed, it is operating.
D31		Reserved
D32		Reserved
D33	TCK	TCK are running
D34	PLL locked	All ISPCLK5620AV are pll locked
D35	SystemACE_STATE	If this LED is blink, all FPGAs are being programmed by SystemACE. If this LED evenly beams, all FPGAs programmed by SystemACE are rightly operating.
D36	SystemACE_ERR	Because a error of SystemACE is generated, SystemACE can't be used.
D37	VCC_5V	ATX power is supplying 5V power to the MFP-LX760-Q board.
D38	STND_BY	The MFP-LX760-Q board has been linking with ATX power.
D39	VCC_12V_ATX	ATX power is supplying 12V power to the MFP-LX760-Q board.
D40	VCC_2.5V	2.5V power is supplied to the MFP board.
D41	VCC_3.3V	3.3V power is supplied to the MFP board.
D42	PWR OFF	Power is supplied to A2 connector.
D44	2.5V	2.5V power is supplied to A2 connector.
D45	1.8V	1.8V power is supplied to A2 connector.
D46	1.5V	1.5V power is supplied to A2 connector.
D47	1.2V	1.2V power is supplied to A2 connector.
D48	PWR OFF	Power is supplied to A3 and B1 connector.
D50	2.5V	2.5V power is supplied to A3 and B1 connector.
D51	1.8V	1.8V power is supplied to A3 and B1 connector.
D52	1.5V	1.5V power is supplied to A3 and B1 connector.
D53	1.2V	1.2V power is supplied to A3 and B1 connector.
D54	PWR OFF	Power is supplied to A4, A5, C1 and C2 connector.
D56	2.5V	2.5V power is supplied to A4, A5, C1 and C2 connector.
D57	1.8V	1.8V power is supplied to A4, A5, C1 and C2 connector.

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NUMBER	Silk	Description
D58	1.5V	1.5V power is supplied to A4, A5, C1 and C2 connector.
D59	1.2V	1.2V power is supplied to A4, A5, C1 and C2 connector.
D60	PWR OFF	Power is supplied to A6, B4, C3 and D1 connector.
D62	2.5V	2.5V power is supplied to A6, B4, C3 and D1 connector.
D63	1.8V	1.8V power is supplied to A6, B4, C3 and D1 connector.
D64	1.5V	1.5V power is supplied to A6, B4, C3 and D1 connector.
D65	1.2V	1.2V power is supplied to A6, B4, C3 and D1 connector.
D66	PWR OFF	Power is supplied to B2 connector.
D68	2.5V	2.5V power is supplied to B2 connector.
D69	1.8V	1.8V power is supplied to B2 connector.
D70	1.5V	1.5V power is supplied to B2 connector.
D71	1.2V	1.2V power is supplied to B2 connector.
D72	PWR OFF	Power is supplied to D2, D3, B5 and B6 connector.
D74	2.5V	2.5V power is supplied to D2, D3, B5 and B6 connector.
D75	1.8V	1.8V power is supplied to D2, D3, B5 and B6 connector.
D76	1.5V	1.5V power is supplied to D2, D3, B5 and B6 connector.
D77	1.2V	1.2V power is supplied to D2, D3, B5 and B6 connector.
D78	PWR OFF	Power is supplied to C5 connector.
D80	2.5V	2.5V power is supplied to C5 connector.
D81	1.8V	1.8V power is supplied to C5 connector.
D82	1.5V	1.5V power is supplied to C5 connector.
D83	1.2V	1.2V power is supplied to C5 connector.
D84	PWR OFF	Power is supplied to C6 and D4 connector.
D86	2.5V	2.5V power is supplied to C6 and D4 connector.
D87	1.8V	1.8V power is supplied to C6 and D4 connector.
D88	1.5V	1.5V power is supplied to C6 and D4 connector.
D89	1.2V	1.2V power is supplied to C6 and D4 connector.
D90	PWR OFF	Power is supplied to D5 connector.
D92	2.5V	2.5V power is supplied to D5 connector.
D93	1.8V	1.8V power is supplied to D5 connector.
D94	1.5V	1.5V power is supplied to D5 connector.
D95	1.2V	1.2V power is supplied to D5 connector.
D96	VCC_FA_INT	1V Power is supplied to [FPGA A]
D97	VCC_FB_INT	1V Power is supplied to [FPGA B]
D98	VCC_FC_INT	1V Power is supplied to [FPGA C]
D99	VCC_FD_INT	1V Power is supplied to [FPGA D]

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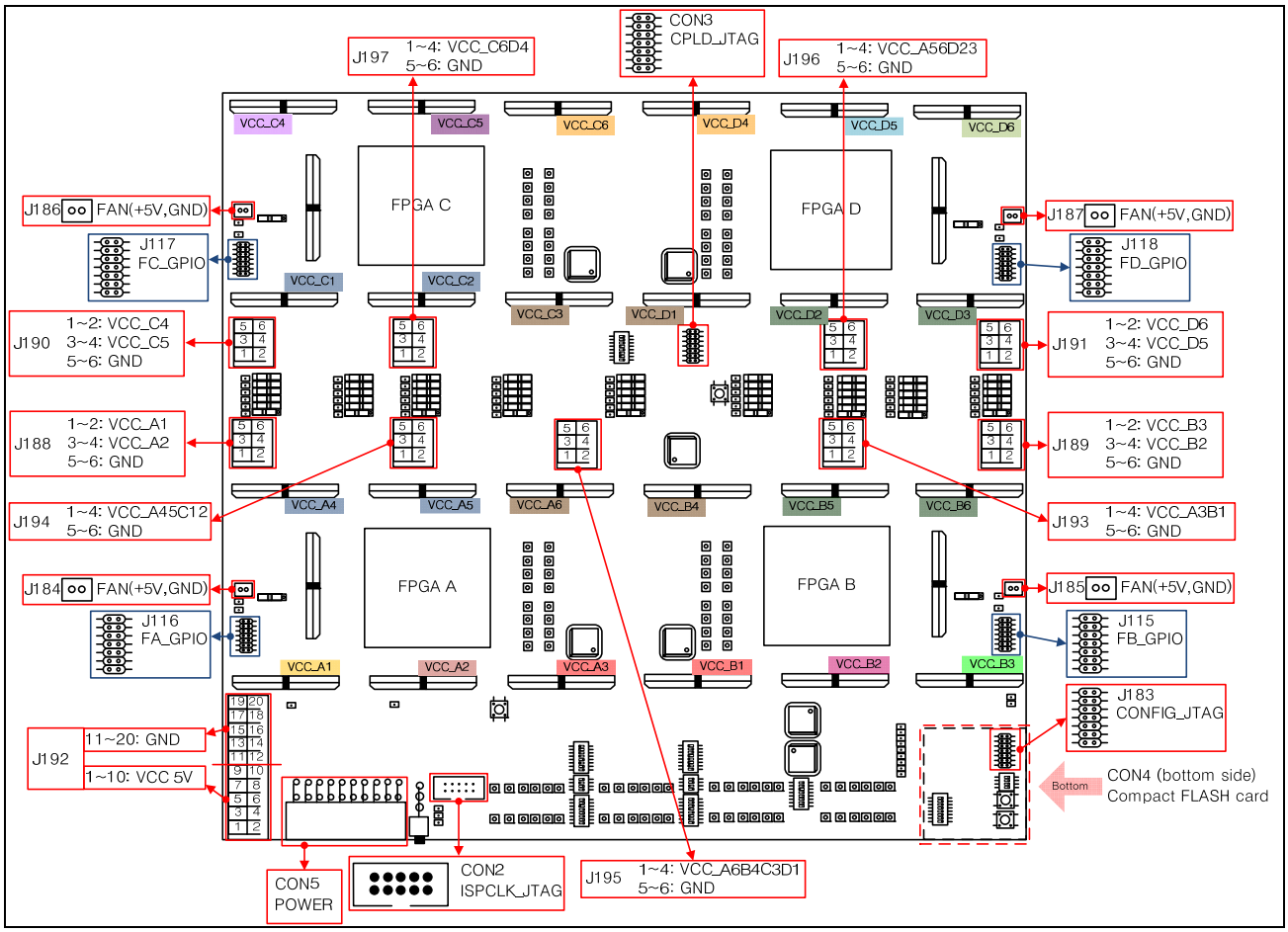
2.8. Connector layout and description



NUMBER	Silk	Description
CON2	ISPCLK_JTAG	To scan JTAG chain of ISPCLK5620AV (Do not Use)
CON3	CPLD_JTAG	To scan JTAG chain of CPLD (XC2C128)
CON4	Compact FLASH Card	To insert Compact FLASH Card
CON5	POWER	To supply power to the MFP Board
J115	FB_GPIO	GPIO connector for "FPGA B"
J116	FA_GPIO	GPIO connector for "FPGA A"
J117	FC_GPIO	GPIO connector for "FPGA C"
J118	FD_GPIO	GPIO connector for "FPGA D"
J183	CONFIG_JTAG	To scan JTAG chain of 4 FPGAs and 12 PROMs
J184	FAN(+5V,GND)	To supply POWER to the FAN of [FPGA A]
J185	FAN(+5V,GND)	To supply POWER to the FAN of [FPGA B]
J186	FAN(+5V,GND).	To supply POWER to the FAN of [FPGA C]
J187	FAN(+5V,GND).	To supply POWER to the FAN of [FPGA D]
J188	1~2 : VCC_A1, 3~4 : VCC_A2,5~6:GND	Transmitting external power to A1 and A2 or connecting A1 with A2.
J189	1~2 : VCC_B3, 3~4 : VCC_B2, ~6:GND	Transmitting external power to B2 and B3 or connecting B2 with B3.
J190	1~2 : VCC_C4, 3~4 : VCC_C5, ~6:GND	Transmitting external power to C4 and C5 or connecting C4 with C5.
J191	1~2 : VCC_D6, 3~4 : VCC_D5, ~6:GND	Transmitting external power to D5 and D6 or connecting D5 with D6.
J192	1~10:VCC-5V, 11~20:GND	External +5V
J193	1~4 : VCC_A3B1, 5~6:GND	Transmitting external power to A3 and B1 or transmitting the power of A3 and B1 to external.
J194	1~4 : VCC_A45C12, 5~6:GND	Transmitting external power to A4, A5, C1 and C2 or transmitting the power of A4, A5, C1 and C2 to external.
J195	1~4 : VCC_A6B4C3D1, 5~6:GND	Transmitting external power to A6, B4, C3 and D1 or transmitting the power of A6, B4, C3 and D1 to external.
J196	1~4 : VCC_B56D23, 5~6:GND	Transmitting external power to B5, B6, D2 and D3 or transmitting the power of B5, B6, D2 and D3 to external.
J197	1~4 : VCC_C6D4, 5~6:GND	Transmitting external power to C6 and D4 or transmitting the power of C6 and D4 to external.

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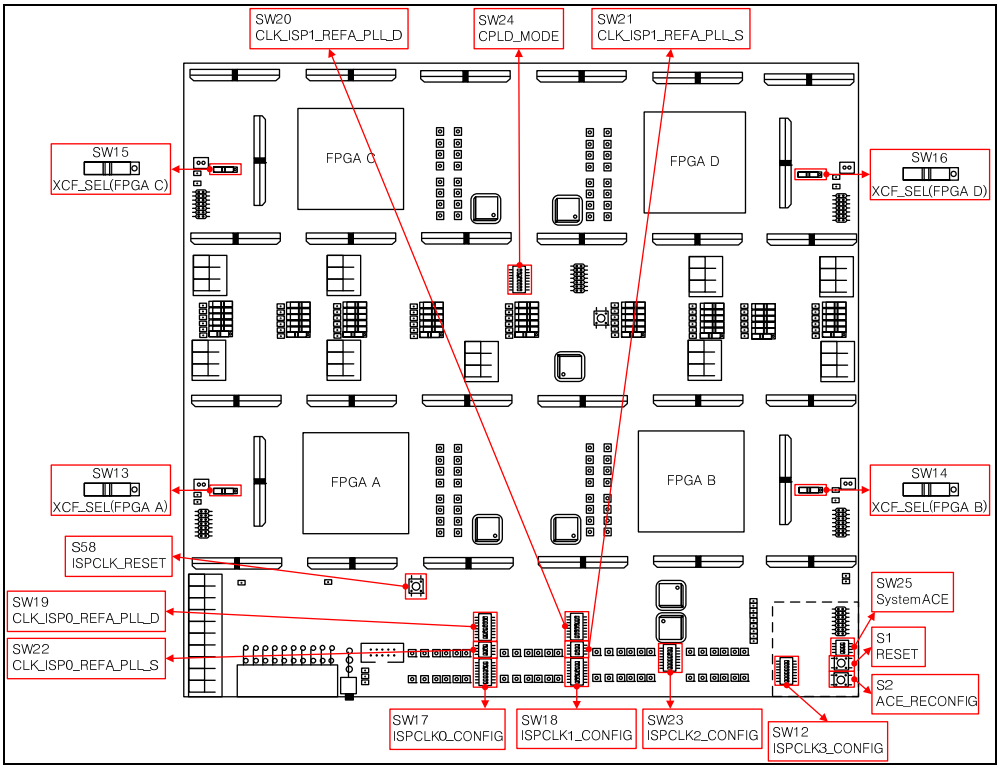
2.9. Switch layout and description



Reference	Silk	Description
SW17	ISPCLK0_CONFIG	8:GOE,7:SGATE,6:PLLBYP,5:FB_SEL, 3:REF_SEL,2~1:PS.
SW18	ISPCLK1_CONFIG	8:GOE,7:SGATE,6:PLLBYP,5:FB_SEL, 3:REF_SEL,2~1:PS.
SW23	ISPCLK2_CONFIG	8:GOE,7:SGATE,6:PLLBYP,5:FB_SEL, 3:REF_SEL,2~1:PS.
SW12	ISPCLK3_CONFIG	8:GOE,7:SGATE,6:PLLBYP,5:FB_SEL, 3:REF_SEL,2~1:PS.
SW19	CLK_ISP0_REFA_PLL_D[7:0]	VCO Divider Value of ICS8402
SW22	CLK_ISP0_REFA_PLL_S[2:0]	Output Driver Value of ICS8402
SW20	CLK_ISP1_REFA_PLL_D[7:0]	VCO Divider Value of ICS8402
SW21	CLK_ISP1_REFA_PLL_S[2:0]	Output Driver Value of ICS8402
SW24	CPLD_MODE	To enable [FPGA A/B/C/D], RESET mode, HOTSWAP.
SW25	SystemACE	MODE (4:ACE_EN, 3~1:CFG_ADDR)
S1	RESET	Reset button. FPGA logic reset input.
S2	ACE_RECONFIG	To reconfigure FPGAs by SystemACE
S58	ISPCLK_RESET	To reset clock buffer

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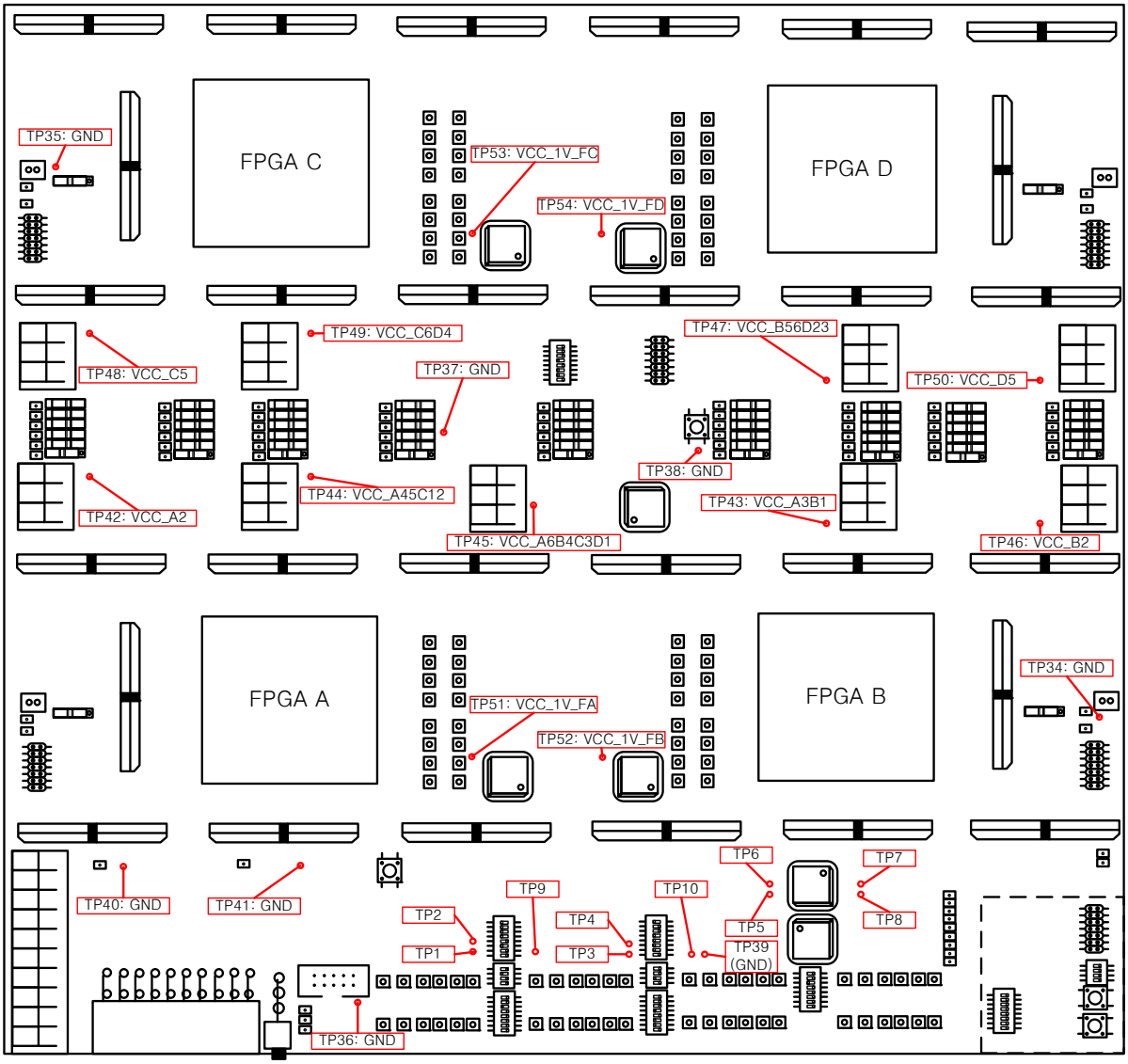
2.10. Test Point layout and description



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Reference	NAME	Description
TP1	CLK_ISPCLK0	CLK_ISPCLK0 output
TP2	CLK_ISPCLK0	CLK_ISPCLK0 output(Inverted)
TP3	CLK_ISPCLK1	CLK_ISPCLK1 output
TP4	CLK_ISPCLK1	CLK_ISPCLK1 output(Inverted)
TP5	CLK_ISPCLK2	CLK_ISPCLK2 output
TP6	CLK_ISPCLK2	CLK_ISPCLK2 output(Inverted)
TP7	CLK_ISPCLK3	CLK_ISPCLK3 output
TP8	CLK_ISPCLK3	CLK_ISPCLK3 output(Inverted)
TP9	CLK_ICS8402_A	Reference Clock Of ISPCLK0
TP10	CLK_ICS8402_B	Reference Clock Of ISPCLK1
TP34	GND	Ground
TP35	GND	Ground
TP36	GND	Ground
TP37	GND	Ground
TP38	GND	Ground
TP39	GND	Ground
TP40	GND	Ground
TP41	GND	Ground
TP42	VCC_A2	The power of connector A2
TP43	VCC_A3B1	The power of connector A3 and B1
TP44	VCC_A45C12	The power of connector A4, A5, C1 and C2
TP45	VCC_A6B4C3D1	The power of connector A6, B4, C3 and D1
TP46	VCC_B2	The power of connector B2
TP47	VCC_B56D23	The power of connector B5, B6, D2 and D3
TP48	VCC_C5	The power of connector C5
TP49	VCC_C6D4	The power of connector C6 and D4
TP50	VCC_D5	The power of connector D5
TP51	VCC_1V_FA	The 1V power of [FPGA A]
TP52	VCC_1V_FB	The 1V power of [FPGA B]
TP53	VCC_1V_FC	The 1V power of [FPGA C]
TP54	VCC_1V_FD	The 1V power of [FPGA D]

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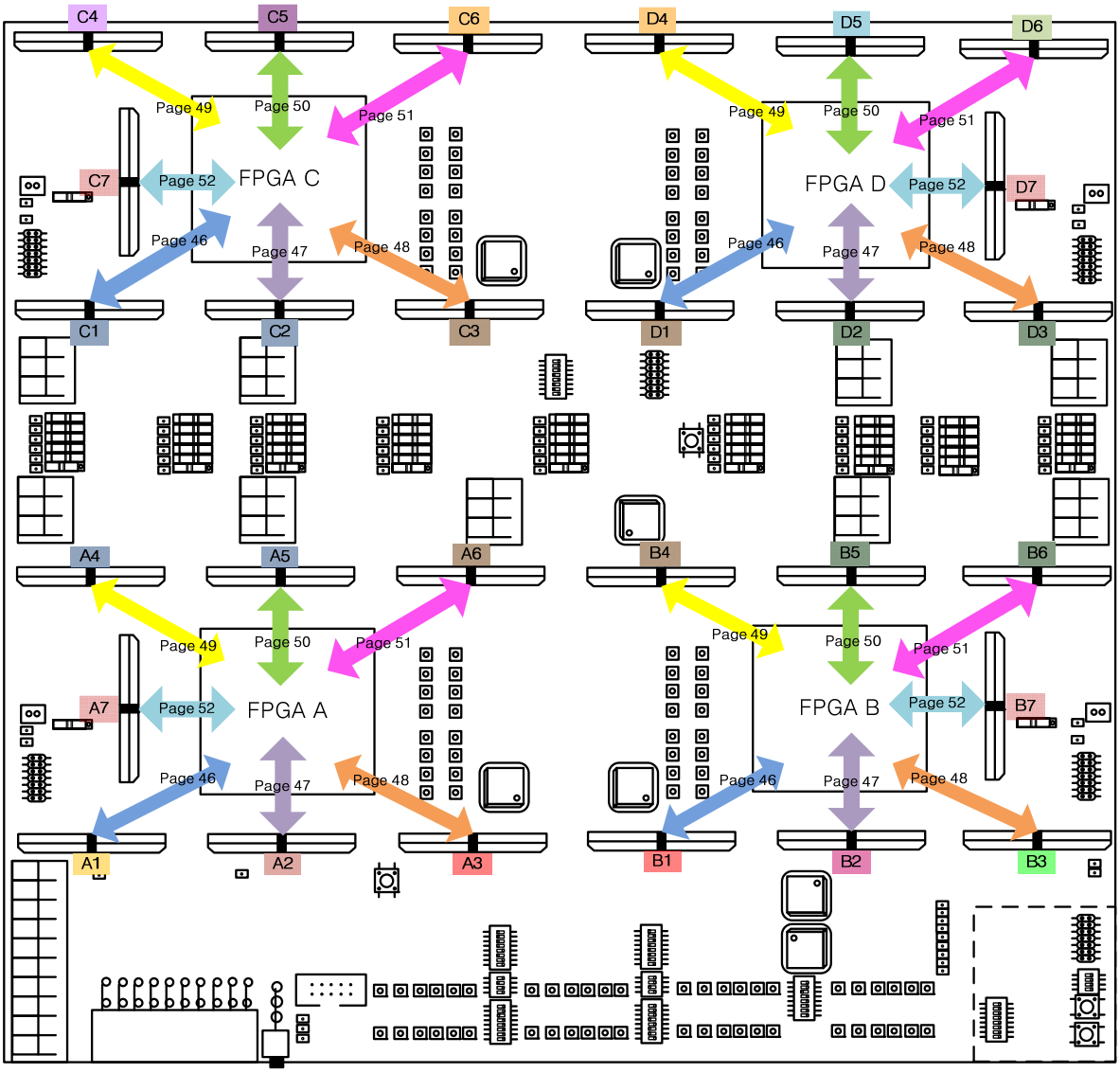
3. FPGA Pin configuration

3.1. I/O module connector



- Each FPGAs have same I/O connection structures
- [FPGA A] I/O Module connector: A1, A2, A3, A4, A5, A6, A7
- [FPGA B] I/O Module connector: B1, B2, B3, B4, B5, B6, B7
- [FPGA C] I/O Module connector: C1, C2, C3, C4, C5, C6, C7
- [FPGA D] I/O Module connector: D1, D2, D3, D4, D5, D6, D7
- FPGA A1/B1/C1/ D1 connector pin configuration
- FPGA A2/B2/C2/ D2 connector pin configuration
- FPGA A3/B3/C3/ D3 connector pin configuration
- FPGA A4/B4/C4/ D4 connector pin configuration
- FPGA A5/B5/C5/ D5 connector pin configuration
- FPGA A6/B6/C6/ D6 connector pin configuration
- FPGA A7/B7/C7/ D7 connector pin configuration

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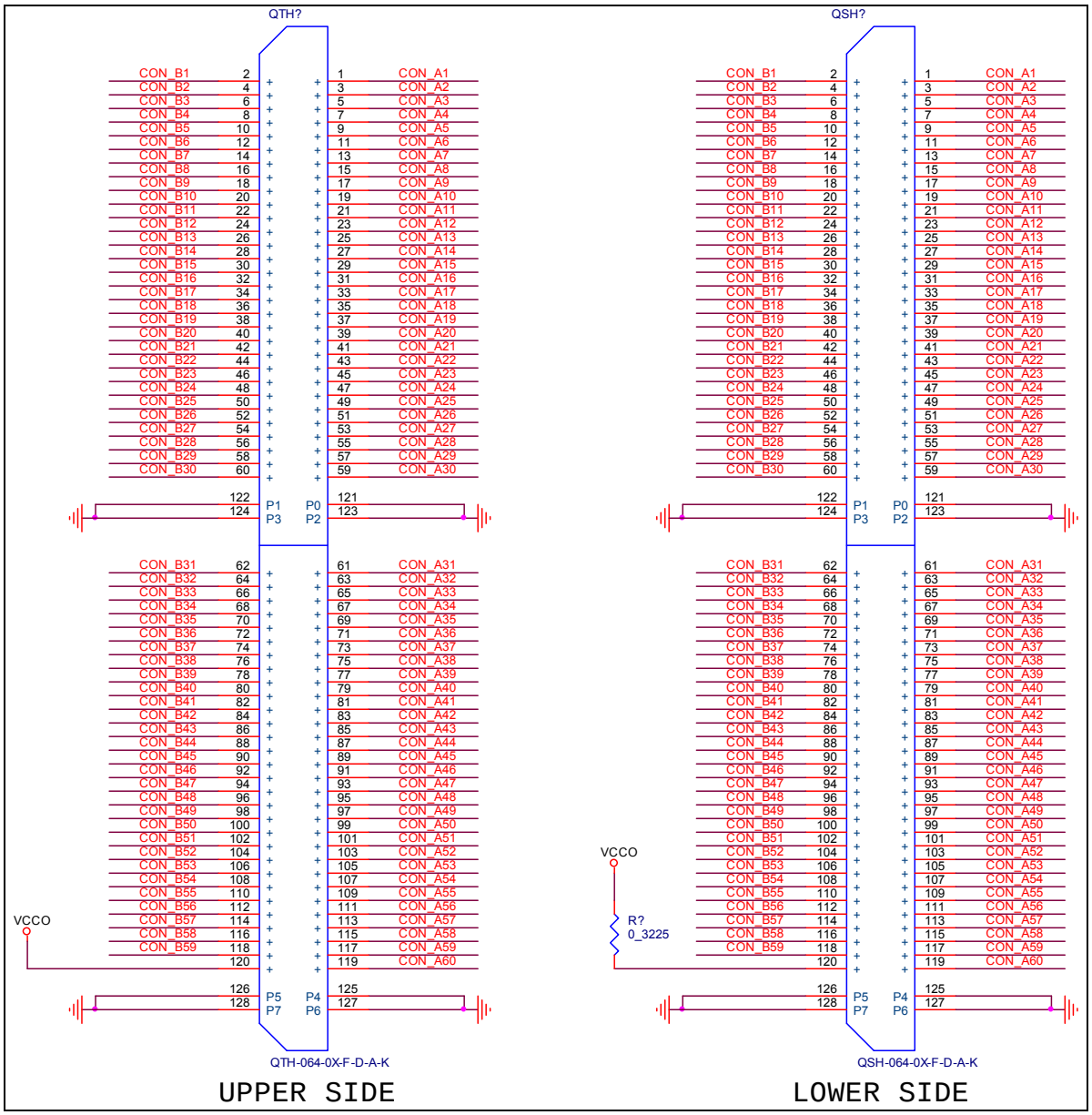
3.1.1. The schematic of I/O module connector



3.1.2. CON1 (A1, B1, C1, D1)

CON1							
Note		FPGA pin	No.	No.	FPGA pin		Note
SRCC	N	N34	B1	A1	M41	N	
SRCC	P	P33	B2	A2	M42	P	
	N	B42	B3	A3	U36	N	
	P	B41	B4	A4	V36	P	
	N	M34	B5	A5	V33	N	
	P	L35	B6	A6	U34	P	
	N	E38	B7	A7	V39	N	VREF
	P	E39	B8	A8	U39	P	
VREF	N	G38	B9	A9	T37	N	
	P	H38	B10	A10	U37	P	
	N	A40	B11	A11	W36	N	
	P	A41	B12	A12	W35	P	
	N	F39	B13	A13	T36	N	
	P	F40	B14	A14	R37	P	
	N	C39	B15	A15	T39	N	SRCC
	P	B39	B16	A16	T40	P	SRCC
SRCC	N	L34	B17	A17	V34	N	
SRCC	P	M33	B18	A18	V35	P	
	N	P32	B19	A19	Y33	N	
	P	N33	B20	A20	Y32	P	
	N	L36	B21	A21	P42	N	
	P	K37	B22	A22	P41	P	
VREF	N	E40	B23	A23	V40	N	
	P	D40	B24	A24	U41	P	
	N	D41	B25	A25	T41	N	VREF
	P	D42	B26	A26	R42	P	
	N	J35	B27	A27	W37	N	
	P	K34	B28	A28	W38	P	
	N	E42	B29	A29	P40	N	
	P	F41	B30	A30	R40	P	
	N	K35	B31	A31	W33	N	SRCC
	P	J36	B32	A32	W32	P	SRCC
SRCC	N	J31	B33	A33	R32	N	
SRCC	P	K30	B34	A34	R33	P	
	N	B32	B35	A35	R35	N	
	P	A32	B36	A36	T35	P	
	N	F32	B37	A37	N35	N	
	P	E32	B38	A38	M36	P	
VREF	N	K29	B39	A39	N36	N	
	P	J30	B40	A40	P36	P	
	N	F30	B41	A41	L39	N	VREF
	P	F31	B42	A42	M39	P	
	N	M27	B43	A43	K40	N	
	P	L27	B44	A44	L40	P	
	N	R25	B45	A45	T32	N	
	P	P25	B46	A46	T31	P	
	N	N26	B47	A47	T34	N	SRCC
	P	P26	B48	A48	U33	P	SRCC
SRCC	N	C34	B49	A49	P35	N	
SRCC	P	B33	B50	A50	R34	P	
	N	J28	B51	A51	J41	N	
	P	K28	B52	A52	K42	P	
	N	D32	B53	A53	U32	N	VREF
	P	C33	B54	A54	U31	P	
VREF	N	H31	B55	A55	P37	N	
	P	G31	B56	A56	P38	P	
	N	G32	B57	A57	F42	N	
	P	G33	B58	A58	G42	P	
	N	H30	B59	A59	G41	N	SRCC
			VCCO	A60	H40	P	SRCC

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3.1.3. CON2 (A2, B2, C2, D2)

CON2							
Note		FPGA pin	No.	No.	FPGA pin		Note
CC	N	L20	B1	A1	M26	N	
CC	P	L21	B2	A2	N25	P	
	N	L22	B3	A3	M21	N	
	P	K22	B4	A4	M22	P	
	N	F17	B5	A5	G26	N	
	P	E17	B6	A6	G27	P	
	N	E19	B7	A7	M23	N	VREF
	P	F20	B8	A8	N23	P	
VREF	N	H19	B9	A9	F27	N	
	P	G18	B10	A10	G28	P	
	N	H21	B11	A11	F29	N	
	P	G21	B12	A12	G29	P	
	N	J20	B13	A13	J26	N	
	P	K20	B14	A14	H26	P	
	N	J21	B15	A15	P22	N	CC
	P	J22	B16	A16	N21	P	CC
CC	N	A21	B17	A17	E30	N	
CC	P	B21	B18	A18	D31	P	
	N	A20	B19	A19	B31	N	
	P	A19	B20	A20	A31	P	
	N	E18	B21	A21	K27	N	
	P	F19	B22	A22	L26	P	
VREF	N	B19	B23	A23	A29	N	
	P	B18	B24	A24	A30	P	
	N	B17	B25	A25	C30	N	VREF
	P	B16	B26	A26	C31	P	
	N	D20	B27	A27	E29	N	
	P	C20	B28	A28	D30	P	
	N	A17	B29	A29	C28	N	
	P	A16	B30	A30	C29	P	
	N	H20	B31	A31	B29	N	CC
	P	G19	B32	A32	B28	P	CC
CC	N	H16	B33	A33	C24	N	
CC	P	H15	B34	A34	B24	P	
	N	D16	B35	A35	J25	N	
	P	C16	B36	A36	K24	P	
	N	F14	B37	A37	F24	N	
	P	F15	B38	A38	G24	P	
VREF	N	N19	B39	A39	D23	N	
	P	P20	B40	A40	E23	P	
	N	E15	B41	A41	K25	N	VREF
	P	E14	B42	A42	L24	P	
	N	B14	B43	A43	E25	N	
	P	B13	B44	A44	E24	P	
	N	J17	B45	A45	H25	N	
	P	K17	B46	A46	H24	P	
	N	A15	B47	A47	J23	N	CC
	P	A14	B48	A48	K23	P	CC
CC	N	D15	B49	A49	H23	N	
CC	P	C15	B50	A50	G23	P	
	N	G17	B51	A51	A24	N	
	P	H18	B52	A52	A25	P	
	N	J18	B53	A53	C26	N	VREF
	P	K18	B54	A54	B27	P	
VREF	N	L17	B55	A55	D25	N	
	P	M17	B56	A56	D26	P	
	N	N18	B57	A57	G22	N	
	P	P17	B58	A58	F22	P	
	N	L19	B59	A59	B23	N	CC
		VCCO	VCCO	A60	C23	P	CC

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3.1.4. CON3 (A3, B3, C3, D3)

CON3							
Note		FPGA pin	No.	No.	FPGA pin		Note
CC	N	A7	B1	A1	E2	N	
CC	P	B7	B2	A2	D1	P	
	N	B11	B3	A3	R10	N	
	P	B12	B4	A4	T9	P	
	N	D8	B5	A5	F2	N	
	P	E8	B6	A6	F1	P	
	N	D12	B7	A7	M4	N	VREF
	P	E12	B8	A8	L4	P	
VREF	N	C9	B9	A9	N6	N	
	P	C8	B10	A10	N5	P	
	N	A10	B11	A11	K2	N	
	P	A9	B12	A12	L2	P	
	N	G12	B13	A13	H3	N	
	P	G11	B14	A14	G3	P	
	N	A12	B15	A15	G2	N	CC
	P	A11	B16	A16	G1	P	CC
CC	N	C10	B17	A17	J3	N	
CC	P	C11	B18	A18	J2	P	
	N	G14	B19	A19	M2	N	
	P	H14	B20	A20	L1	P	
	N	E10	B21	A21	R8	N	
	P	E9	B22	A22	P8	P	
VREF	N	A6	B23	A23	H1	N	
	P	A5	B24	A24	J1	P	
	N	K15	B25	A25	M3	N	VREF
	P	L16	B26	A26	N3	P	
	N	H13	B27	A27	P6	N	
	P	G13	B28	A28	R7	P	
	N	B6	B29	A29	P10	N	
	P	C6	B30	A30	R9	P	
	N	F12	B31	A31	P7	N	CC
	P	F11	B32	A32	N8	P	CC
CC	N	L7	B33	A33	M1	N	
CC	P	M8	B34	A34	N1	P	
	N	D5	B35	A35	V10	N	
	P	C5	B36	A36	V9	P	
	N	G4	B37	A37	P3	N	
	P	H4	B38	A38	P2	P	
VREF	N	N10	B39	A39	T5	N	
	P	N9	B40	A40	U6	P	
	N	E5	B41	A41	U4	N	VREF
	P	F5	B42	A42	V4	P	
	N	A2	B43	A43	V3	N	
	P	B3	B44	A44	W3	P	
	N	H6	B45	A45	V11	N	
	P	H5	B46	A46	U11	P	
	N	A4	B47	A47	W7	N	CC
	P	B4	B48	A48	W8	P	CC
CC	N	P13	B49	A49	R2	N	
CC	P	N13	B50	A50	P1	P	
	N	L9	B51	A51	T2	N	
	P	M9	B52	A52	T1	P	
	N	J5	B53	A53	U3	N	VREF
	P	K5	B54	A54	U2	P	
VREF	N	D3	B55	A55	W5	N	
	P	E3	B56	A56	W6	P	
	N	B2	B57	A57	U9	N	
	P	B1	B58	A58	U8	P	
	N	N11	B59	A59	T4	N	CC
		VCCO	VCCO	A60	R3	P	CC

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3.1.5. CON4 (A4, B4, C4, D4)

CON4							
Note		FPGA pin	No.	No.	FPGA pin		Note
CC	N	AJ35	B1	A1	Y34	N	
CC	P	AK35	B2	A2	Y35	P	
	N	AU42	B3	A3	AA34	N	
	P	AT42	B4	A4	AB34	P	
	N	AH34	B5	A5	W40	N	
	P	AH33	B6	A6	V41	P	
	N	AJ37	B7	A7	AB36	N	VREF
	P	AK38	B8	A8	AC36	P	
VREF	N	AF32	B9	A9	Y39	N	
	P	AF31	B10	A10	AA39	P	
	N	AP42	B11	A11	AC39	N	
	P	AR42	B12	A12	AC38	P	
	N	AR40	B13	A13	W42	N	
	P	AT40	B14	A14	W41	P	
	N	AE32	B15	A15	AC35	N	CC
	P	AE33	B16	A16	AC34	P	CC
CC	N	AN40	B17	A17	AD32	N	
CC	P	AP41	B18	A18	AD33	P	
	N	AG33	B19	A19	AC41	N	
	P	AG34	B20	A20	AD42	P	
	N	AP40	B21	A21	Y42	N	
	P	AN39	B22	A22	AA41	P	
VREF	N	AT41	B23	A23	AB32	N	
	P	AU41	B24	A24	AC33	P	
	N	AV41	B25	A25	AA42	N	VREF
	P	AW42	B26	A26	AB42	P	
	N	AJ38	B27	A27	AB38	N	
	P	AK39	B28	A28	AB39	P	
	N	AW41	B29	A29	AA35	N	
	P	AV40	B30	A30	AA36	P	
	N	AH35	B31	A31	AB33	N	CC
	P	AH36	B32	A32	AA32	P	CC
CC	N	AY34	B33	A33	AE42	N	
CC	P	AY33	B34	A34	AF42	P	
	N	AP30	B35	A35	AG39	N	
	P	AP31	B36	A36	AG38	P	
	N	AU32	B37	A37	AD41	N	
	P	AV33	B38	A38	AD40	P	
VREF	N	AU33	B39	A39	AE38	N	
	P	AT32	B40	A40	AE37	P	
	N	AU34	B41	A41	AE35	N	VREF
	P	AV34	B42	A42	AE34	P	
	N	BB34	B43	A43	AH40	N	
	P	BB33	B44	A44	AJ40	P	
	N	AW35	B45	A45	AF41	N	
	P	AY35	B46	A46	AG42	P	
	N	BA35	B47	A47	AJ42	N	CC
	P	BA34	B48	A48	AJ41	P	CC
CC	N	AR29	B49	A49	AF40	N	
CC	P	AT30	B50	A50	AE40	P	
	N	AT29	B51	A51	AF35	N	
	P	AR28	B52	A52	AF34	P	
	N	AU31	B53	A53	AK40	N	VREF
	P	AV31	B54	A54	AL40	P	
VREF	N	AP28	B55	A55	AH39	N	
	P	AN28	B56	A56	AH38	P	
	N	AM28	B57	A57	AG41	N	
	P	AL27	B58	A58	AH41	P	
	N	AN29	B59	A59	AD38	N	CC
		VCCO	VCCO	A60	AD37	P	CC

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3.1.6. CON5 (A5, B5, C5, D5)

CON5							
Note		FPGA pin	No.	No.	FPGA pin		Note
CC	N	AW17	B1	A1	AY32	N	
CC	P	AY17	B2	A2	BA32	P	
	N	BB18	B3	A3	AW30	N	
	P	BB17	B4	A4	AY30	P	
	N	AW20	B5	A5	BB32	N	
	P	AV20	B6	A6	BA31	P	
	N	AV19	B7	A7	AH26	N	VREF
	P	AU19	B8	A8	AJ26	P	
VREF	N	BA15	B9	A9	AU28	N	
	P	BB16	B10	A10	AU27	P	
	N	BA16	B11	A11	AV28	N	
	P	BA17	B12	A12	AW27	P	
	N	BA14	B13	A13	BA30	N	
	P	BB14	B14	A14	BB31	P	
	N	AR19	B15	A15	AJ22	N	CC
	P	AT19	B16	A16	AJ23	P	CC
CC	N	AY20	B17	A17	AL25	N	
CC	P	AW21	B18	A18	AK24	P	
	N	AP22	B19	A19	AN23	N	
	P	AR22	B20	A20	AM23	P	
	N	AM21	B21	A21	AM26	N	
	P	AN21	B22	A22	AN26	P	
VREF	N	BA19	B23	A23	AK22	N	
	P	AY19	B24	A24	AK23	P	
	N	AP20	B25	A25	AN25	N	VREF
	P	AN20	B26	A26	AN24	P	
	N	AT20	B27	A27	AM24	N	
	P	AT21	B28	A28	AL24	P	
	N	AR20	B29	A29	AP27	N	
	P	AP21	B30	A30	AP26	P	
	N	AV21	B31	A31	AR27	N	CC
	P	AU21	B32	A32	AT27	P	CC
CC	N	BB11	B33	A33	AW26	N	
CC	P	BA12	B34	A34	AY27	P	
	N	AR17	B35	A35	AT25	N	
	P	AP17	B36	A36	AR24	P	
	N	AK19	B37	A37	AY28	N	
	P	AJ20	B38	A38	BA29	P	
VREF	N	BA10	B39	A39	AW25	N	
	P	BA11	B40	A40	AV24	P	
	N	AV15	B41	A41	AY25	N	VREF
	P	AU16	B42	A42	BA25	P	
	N	AM19	B43	A43	AW23	N	
	P	AN19	B44	A44	AW22	P	
	N	AY10	B45	A45	BB28	N	
	P	AW11	B46	A46	BB29	P	
	N	AN18	B47	A47	AY24	N	CC
	P	AP18	B48	A48	BA24	P	CC
CC	N	AY13	B49	A49	BA27	N	
CC	P	AY12	B50	A50	BB27	P	
	N	AY14	B51	A51	AY23	N	
	P	AY15	B52	A52	AY22	P	
	N	AW15	B53	A53	BB24	N	VREF
	P	AW16	B54	A54	BB23	P	
VREF	N	AT15	B55	A55	AU24	N	
	P	AT16	B56	A56	AT24	P	
	N	AM18	B57	A57	BA26	N	
	P	AL19	B58	A58	BB26	P	
	N	BB13	B59	A59	AR23	N	CC
		VCCO	VCCO	A60	AP23	P	CC

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3.1.7. CON6 (A6, B6, C6, D6)

CON6							
Note		FPGA pin	No.	No.	FPGA pin		Note
CC	N	AB2	B1	A1	AN16	N	
CC	P	AB1	B2	A2	AP16	P	
	N	AA2	B3	A3	AK15	N	
	P	AA1	B4	A4	AL15	P	
	N	AB3	B5	A5	AR13	N	
	P	AC3	B6	A6	AR14	P	
	N	AA5	B7	A7	AT11	N	VREF
	P	AA4	B8	A8	AT10	P	
VREF	N	AC5	B9	A9	AV10	N	
	P	AC6	B10	A10	AU11	P	
	N	Y2	B11	A11	AV11	N	
	P	Y3	B12	A12	AU12	P	
	N	AB8	B13	A13	AJ18	N	
	P	AB9	B14	A14	AK18	P	
	N	W2	B15	A15	AV8	N	CC
	P	W1	B16	A16	AW8	P	CC
CC	N	AA11	B17	A17	AL17	N	
CC	P	Y10	B18	A18	AM17	P	
	N	Y4	B19	A19	AN15	N	
	P	Y5	B20	A20	AP15	P	
	N	AB6	B21	A21	BB8	N	
	P	AB7	B22	A22	BB7	P	
VREF	N	AD2	B23	A23	AR12	N	
	P	AD3	B24	A24	AT12	P	
	N	AC1	B25	A25	AL16	N	VREF
	P	AD1	B26	A26	AM16	P	
	N	AB11	B27	A27	AJ17	N	
	P	AA10	B28	A28	AK17	P	
	N	AE2	B29	A29	BA9	N	
	P	AE3	B30	A30	BB9	P	
	N	Y9	B31	A31	AY9	N	CC
	P	AA9	B32	A32	AW10	P	CC
CC	N	AF9	B33	A33	AK2	N	
CC	P	AF10	B34	A34	AL1	P	
	N	AJ1	B35	A35	AP2	N	
	P	AH1	B36	A36	AR2	P	
	N	AG6	B37	A37	AK3	N	
	P	AG7	B38	A38	AL2	P	
VREF	N	AE4	B39	A39	AJ5	N	
	P	AF4	B40	A40	AJ6	P	
	N	AE5	B41	A41	AT1	N	VREF
	P	AF5	B42	A42	AT2	P	
	N	AF2	B43	A43	AK4	N	
	P	AG2	B44	A44	AL4	P	
	N	AC11	B45	A45	AM2	N	
	P	AC10	B46	A46	AM1	P	
	N	AF1	B47	A47	AU1	N	CC
	P	AG1	B48	A48	AV1	P	CC
CC	N	AE8	B49	A49	AN5	N	
CC	P	AD8	B50	A50	AN4	P	
	N	AD11	B51	A51	AR3	N	
	P	AD10	B52	A52	AR4	P	
	N	AF6	B53	A53	AH9	N	VREF
	P	AF7	B54	A54	AH10	P	
VREF	N	AG3	B55	A55	AK7	N	
	P	AH3	B56	A56	AJ8	P	
	N	AJ2	B57	A57	AM3	N	
	P	AJ3	B58	A58	AM4	P	
	N	AE9	B59	A59	AN3	N	CC
		VCCO	VCCO	A60	AP3	P	CC

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3.1.8. CON7 (A7, B7, C7, D7)

CON7							
Note		FPGA pin	No.	No.	FPGA pin		Note
MRCC	N	A37	B1	A1	D7	N	
MRCC	P	B37	B2	A2	D6	P	
	N	B36	B3	A3	E7	N	
	P	A36	B4	A4	F7	P	
	N	C38	B5	A5	F9	N	
	P	D38	B6	A6	F10	P	
SRCC	N	D37	B7	A7	F6	N	
SRCC	P	C36	B8	A8	G6	P	
	N	F35	B9	A9	G9	N	
	P	F34	B10	A10	H9	P	
MRCC	N	F36	B11	A11	G8	N	MRCC
MRCC	P	G36	B12	A12	G7	P	MRCC
	N	H33	B13	A13	H10	N	
	P	G34	B14	A14	H11	P	
	N	H34	B15	A15	J12	N	MRCC
	P	H35	B16	A16	K13	P	MRCC
SRCC	N	J32	B17	A17	J11	N	
SRCC	P	K32	B18	A18	J10	P	
VREF	N	J33	B19	A19	L11	N	SRCC
	P	K33	B20	A20	K10	P	SRCC
	N	L32	B21	A21	L12	N	SRCC
	P	M31	B22	A22	K12	P	SRCC
VREF	N	L30	B23	A23	K9	N	
	P	L31	B24	A24	L10	P	
	N	N28	B25	A25	L15	N	
	P	M29	B26	A26	M16	P	
	N	N29	B27	A27	L14	N	VREF
	P	P30	B28	A28	M14	P	
	N	P28	B29	A29	M12	N	VREF
	P	R28	B30	A30	M13	P	
	N	AM32	B31	A31	AR9	N	MRCC
	P	AM31	B32	A32	AT9	P	MRCC
MRCC	N	AU37	B33	A33	AH16	N	
MRCC	P	AU36	B34	A34	AJ16	P	
	N	AN31	B35	A35	AJ15	N	
	P	AN30	B36	A36	AK14	P	
	N	AN33	B37	A37	AJ13	N	
	P	AP33	B38	A38	AK13	P	
VREF	N	AT34	B39	A39	AL14	N	
	P	AR33	B40	A40	AM14	P	
	N	AR32	B41	A41	AN11	N	VREF
	P	AP32	B42	A42	AM12	P	
	N	AR34	B43	A43	AN13	N	
	P	AT35	B44	A44	AM13	P	
	N	AV39	B45	A45	AM11	N	
	P	AU39	B46	A46	AN10	P	
	N	AU38	B47	A47	AR7	N	SRCC
	P	AV38	B48	A48	AT6	P	SRCC
MRCC	N	AY39	B49	A49	AP13	N	
MRCC	P	BA39	B50	A50	AN14	P	
	N	AV35	B51	A51	AN9	N	VREF
	P	AW36	B52	A52	AP8	P	
	N	AW40	B53	A53	AP10	N	
	P	AY40	B54	A54	AR10	P	
	N	AW38	B55	A55	AP12	N	
	P	AY38	B56	A56	AP11	P	
	N	AY42	B57	A57	AR8	N	
	P	BA42	B58	A58	AT7	P	
VREF	N	AY37	B59	A59	AU6	N	MRCC
		VCCO	VCCO	A60	AV6	P	MRCC

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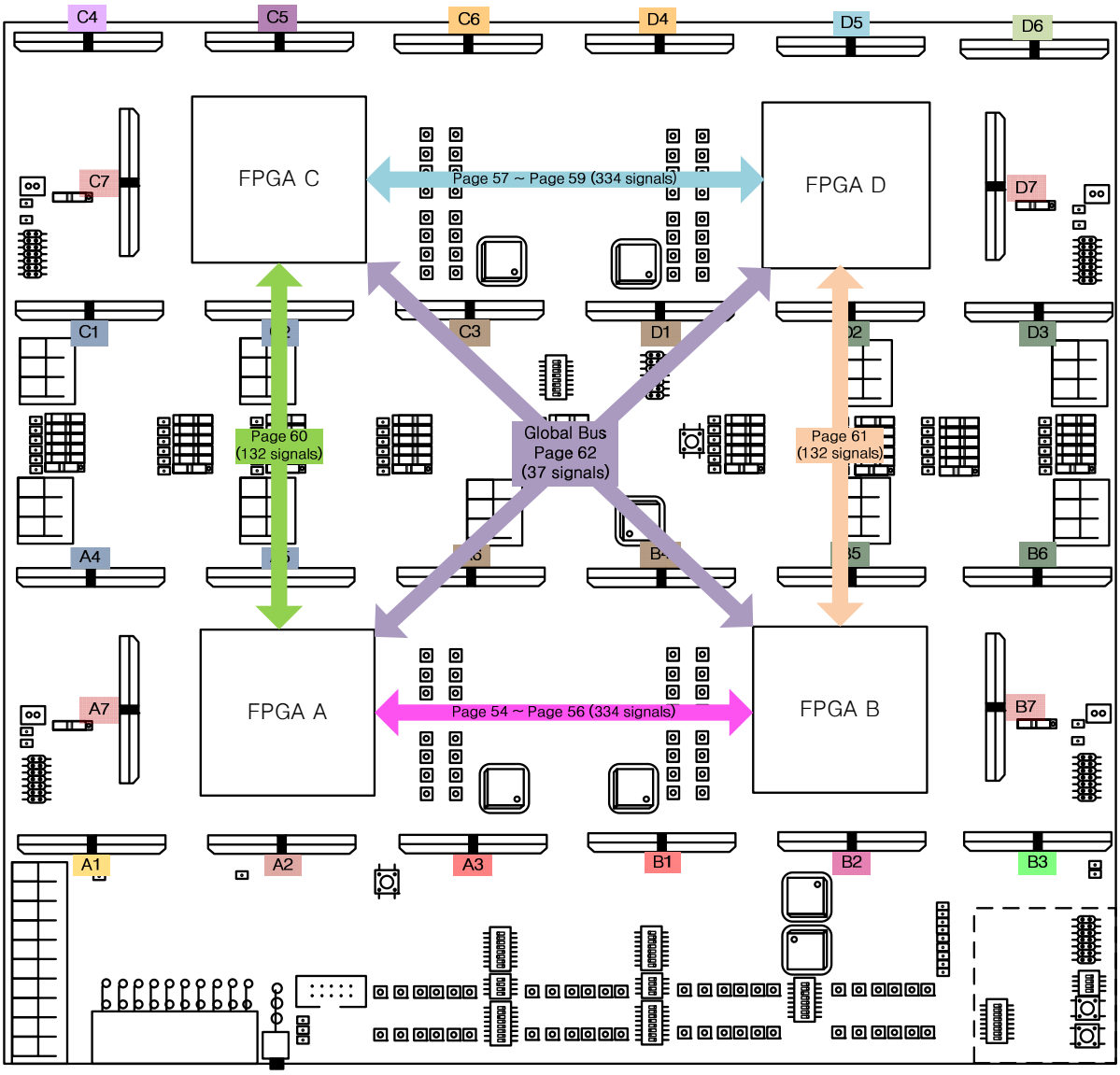
3.2. Signals between FPGAs



- 35, 36, 37 pages: Signals between FPGA C and D
  (334 total signals = 111 differential pair signals + 112 single ended signals)

- 38, 39, 40 pages: Signals between FPGA A and B
  (334 total signals = 111 differential pair signals + 112 single-ended signals)

- 41 page: Signals between FPGA A and C.
  (66 differential pair signals)

- 42 page: Signals between FPGA B and D
  (66 differential pair signals)

- 43 page: Signals between FPGA A, B, C and D
  (37 single ended signals)

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3.2.1. FPGA A to FPGA B

FPGA A - FPGA B(FAST)								
note	VCCO		FPGA A	Signal	FPGA B		VCCO	note
	2.5V	P	U1-J8	FA_FB1	U2-J8	P	2.5V	
	2.5V	N	U1-H8	FA_FB2	U2-H8	N	2.5V	
	2.5V	P	U1-N16	FA_FB3	U2-N16	P	2.5V	
	2.5V	N	U1-P16	FA_FB4	U2-P16	N	2.5V	
SRCC	2.5V	P	U1-BB4	FA_FB5	U2-BB4	P	2.5V	SRCC
SRCC	2.5V	N	U1-BB3	FA_FB6	U2-BB3	N	2.5V	SRCC
MRCC	2.5V	P	U1-AY3	FA_FB7	U2-AY3	P	2.5V	MRCC
MRCC	2.5V	N	U1-AW3	FA_FB8	U2-AW3	N	2.5V	MRCC
MRCC	2.5V	P	U1-AV5	FA_FB9	U2-AV5	P	2.5V	MRCC
MRCC	2.5V	N	U1-AV4	FA_FB10	U2-AV4	N	2.5V	MRCC
SRCC	2.5V	P	U1-AK9	FA_FB11	U2-AK9	P	2.5V	SRCC
SRCC	2.5V	N	U1-AL9	FA_FB12	U2-AL9	N	2.5V	SRCC
	2.5V	P	U1-AT5	FA_FB13	U2-AT5	P	2.5V	
VREF	2.5V	N	U1-AT4	FA_FB14	U2-AT4	N	2.5V	VREF
	2.5V	P	U1-AP7	FA_FB15	U2-AP7	P	2.5V	
	2.5V	N	U1-AP6	FA_FB16	U2-AP6	N	2.5V	
	2.5V	P	U1-AK12	FA_FB17	U2-AK12	P	2.5V	
	2.5V	N	U1-AJ12	FA_FB18	U2-AJ12	N	2.5V	
	2.5V	P	U1-AM9	FA_FB19	U2-AM9	P	2.5V	
	2.5V	N	U1-AL10	FA_FB20	U2-AL10	N	2.5V	
	2.5V	P	U1-AL12	FA_FB21	U2-AL12	P	2.5V	
	2.5V	N	U1-AL11	FA_FB22	U2-AL11	N	2.5V	
	2.5V	P	U1-F37	FA_FB23	U2-F37	P	2.5V	
	2.5V	N	U1-E37	FA_FB24	U2-E37	N	2.5V	
	2.5V	P	U1-N30	FA_FB25	U2-N30	P	2.5V	
	2.5V	N	U1-P31	FA_FB26	U2-P31	N	2.5V	
SRCC	2.5V	P	U1-AR35	FA_FB27	U2-AR35	P	2.5V	SRCC
SRCC	2.5V	N	U1-AT36	FA_FB28	U2-AT36	N	2.5V	SRCC
MRCC	2.5V	P	U1-AT37	FA_FB29	U2-AT37	P	2.5V	MRCC
MRCC	2.5V	N	U1-AR37	FA_FB30	U2-AR37	N	2.5V	MRCC
MRCC	2.5V	P	U1-AP37	FA_FB31	U2-AP37	P	2.5V	MRCC
MRCC	2.5V	N	U1-AN36	FA_FB32	U2-AN36	N	2.5V	MRCC
SRCC	2.5V	P	U1-AJ31	FA_FB33	U2-AJ31	P	2.5V	SRCC
SRCC	2.5V	N	U1-AH30	FA_FB34	U2-AH30	N	2.5V	SRCC
	2.5V	P	U1-AL31	FA_FB35	U2-AL31	P	2.5V	
VREF	2.5V	N	U1-AL32	FA_FB36	U2-AL32	N	2.5V	VREF
	2.5V	P	U1-AL29	FA_FB37	U2-AL29	P	2.5V	
	2.5V	N	U1-AK29	FA_FB38	U2-AK29	N	2.5V	
	2.5V	P	U1-AP35	FA_FB39	U2-AP35	P	2.5V	
	2.5V	N	U1-AP36	FA_FB40	U2-AP36	N	2.5V	
	2.5V	P	U1-AK30	FA_FB41	U2-AK30	P	2.5V	
	2.5V	N	U1-AL30	FA_FB42	U2-AL30	N	2.5V	
	2.5V	P	U1-AH29	FA_FB43	U2-AH29	P	2.5V	
	2.5V	N	U1-AJ30	FA_FB44	U2-AJ30	N	2.5V	
SRCC	2.5V	N	U1-BB38	FA_FB45	U2-BB38	N	2.5V	SRCC
	VCC_A3B1	P	U1-P11	FA_FB46	U2-R39	P	VCC_A3B1	
	VCC_A3B1	N	U1-P12	FA_FB47	U2-R38	N	VCC_A3B1	
MRCC	VCC_A3B1	P	U1-F4	FA_FB48	U2-N41	P	VCC_A3B1	
MRCC	VCC_A3B1	N	U1-E4	FA_FB49	U2-N40	N	VCC_A3B1	MRCC
MRCC	VCC_A3B1	P	U1-C3	FA_FB50	U2-V38	P	VCC_A3B1	MRCC
MRCC	VCC_A3B1	N	U1-C4	FA_FB51	U2-U38	N	VCC_A3B1	MRCC
	VCC_A3B1	P	U1-V8	FA_FB52	U2-K38	P	VCC_A3B1	
	VCC_A3B1	N	U1-U7	FA_FB53	U2-L37	N	VCC_A3B1	
	VCC_A3B1	P	U1-R4	FA_FB54	U2-J40	P	VCC_A3B1	MRCC
	VCC_A3B1	N	U1-R5	FA_FB55	U2-K39	N	VCC_A3B1	MRCC
MRCC	VCC_A3B1	P	U1-B8	FA_FB56	U2-M38	P	VCC_A3B1	MRCC
MRCC	VCC_A3B1	N	U1-B9	FA_FB57	U2-M37	N	VCC_A3B1	MRCC
MRCC	VCC_A3B1	P	U1-P5	FA_FB58	U2-L42	P	VCC_A3B1	
MRCC	VCC_A3B1	N	U1-N4	FA_FB59	U2-L41	N	VCC_A3B1	

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FPGA A - FPGA B(FAST)								
note	VCCO		FPGA A	Signal	FPGA B		VCCO	note
	VCC_A3B1	P	U1-D10	FA_FB60	U2-J42	P	VCC_A3B1	
	VCC_A3B1	N	U1-D11	FA_FB61	U2-H41	N	VCC_A3B1	
	VCC_A3B1	P	U1-C1	FA_FB62	U2-G37	P	VCC_A3B1	
	VCC_A3B1	N	U1-D2	FA_FB63	U2-H36	N	VCC_A3B1	
MRCC	VCC_A3B1	P	U1-V5	FA_FB64	U2-C41	P	VCC_A3B1	MRCC
MRCC	VCC_A3B1	N	U1-V6	FA_FB65	U2-C40	N	VCC_A3B1	MRCC
	VCC_A3B1	P	U1-J6	FA_FB66	U2-J38	P	VCC_A3B1	MRCC
	VCC_A3B1	N	U1-K7	FA_FB67	U2-J37	N	VCC_A3B1	MRCC
MRCC	VCC_A3B1	P	U1-J15	FA_FB68	U2-P27	P	VCC_A3B1	
MRCC	VCC_A3B1	N	U1-J16	FA_FB69	U2-R27	N	VCC_A3B1	
	VCC_A3B1	P	U1-V1	FA_FB70	U2-A35	P	VCC_A3B1	MRCC
	VCC_A3B1	N	U1-U1	FA_FB71	U2-A34	N	VCC_A3B1	MRCC
MRCC	VCC_A3B1	P	U1-T6	FA_FB72	U2-D33	P	VCC_A3B1	MRCC
MRCC	VCC_A3B1	N	U1-T7	FA_FB73	U2-E33	N	VCC_A3B1	MRCC
	VCC_A3B1	P	U1-M11	FA_FB74	U2-H29	P	VCC_A3B1	
	VCC_A3B1	P	U1-L5	FA_FB75	U2-C35	P	VCC_A3B1	
	VCC_A3B1	N	U1-M6	FA_FB76	U2-B34	N	VCC_A3B1	
MRCC	VCC_A3B1	P	U1-K3	FA_FB77	U2-D35	P	VCC_A3B1	
MRCC	VCC_A3B1	N	U1-K4	FA_FB78	U2-E34	N	VCC_A3B1	
	VCC_A6B4C3D1	P	U1-AG12	FA_FB79	U2-Y38	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	N	U1-AG11	FA_FB80	U2-Y37	N	VCC_A6B4C3D1	
	VCC_A6B4C3D1	P	U1-AF12	FA_FB81	U2-AA40	P	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	N	U1-AF11	FA_FB82	U2-Y40	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U1-AH4	FA_FB83	U2-AB37	P	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	N	U1-AG4	FA_FB84	U2-AA37	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U1-AE7	FA_FB85	U2-AF39	P	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	N	U1-AD7	FA_FB86	U2-AE39	N	VCC_A6B4C3D1	
	VCC_A6B4C3D1	P	U1-AM6	FA_FB87	U2-AD36	P	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	N	U1-AL6	FA_FB88	U2-AD35	N	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	P	U1-AU9	FA_FB89	U2-AF36	P	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	N	U1-AV9	FA_FB90	U2-AF37	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U1-Y7	FA_FB91	U2-AM42	P	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	N	U1-Y8	FA_FB92	U2-AL41	N	VCC_A6B4C3D1	
	VCC_A6B4C3D1	P	U1-AA6	FA_FB93	U2-AG36	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	N	U1-AA7	FA_FB94	U2-AG37	N	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	P	U1-AP1	FA_FB95	U2-AM39	P	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	N	U1-AN1	FA_FB96	U2-AL39	N	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	P	U1-AU14	FA_FB97	U2-AN41	P	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	N	U1-AU13	FA_FB98	U2-AM41	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U1-AL5	FA_FB99	U2-AK37	P	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	N	U1-AK5	FA_FB100	U2-AJ36	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U1-AT14	FA_FB101	U2-AJ28	P	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	N	U1-AR15	FA_FB102	U2-AK28	N	VCC_A6B4C3D1	
	VCC_A6B4C3D1	P	U1-AH8	FA_FB103	U2-AR30	P	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	N	U1-AJ7	FA_FB104	U2-AT31	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U1-AC4	FA_FB105	U2-AW32	P	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	N	U1-AB4	FA_FB106	U2-AW33	N	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	P	U1-AE10	FA_FB107	U2-AM29	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	P	U1-AD6	FA_FB108	U2-AL26	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	N	U1-AD5	FA_FB109	U2-AM27	N	VCC_A6B4C3D1	
	VCC_A6B4C3D1	P	U1-AH6	FA_FB110	U2-AK27	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	N	U1-AH5	FA_FB111	U2-AJ27	N	VCC_A6B4C3D1	

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FPGA A - FPGA B(SLOW)								
note	VCCO		FPGA A	Signal	FPGA B		VCCO	note
	VCC_A2		U1-L25	FA_FB_S112	U2-L5		VCC_B3	
	VCC_A2		U1-M24	FA_FB_S113	U2-M6		VCC_B3	
	VCC_A2		U1-P23	FA_FB_S114	U2-K3		VCC_B3	
	VCC_A2		U1-N24	FA_FB_S115	U2-K4		VCC_B3	
	VCC_A2		U1-D28	FA_FB_S116	U2-P5		VCC_B3	
	VCC_A2		U1-E28	FA_FB_S117	U2-N4		VCC_B3	
	VCC_A2		U1-E22	FA_FB_S118	U2-R4		VCC_B3	
	VCC_A2		U1-D22	FA_FB_S119	U2-R5		VCC_B3	
	VCC_A2		U1-B22	FA_FB_S120	U2-T6		VCC_B3	
	VCC_A2		U1-A22	FA_FB_S121	U2-T7		VCC_B3	
	VCC_A2		U1-F26	FA_FB_S122	U2-V5		VCC_B3	
	VCC_A2		U1-F25	FA_FB_S123	U2-V6		VCC_B3	
	VCC_A2		U1-A27	FA_FB_S124	U2-V1		VCC_B3	
	VCC_A2		U1-A26	FA_FB_S125	U2-U1		VCC_B3	
	VCC_A2		U1-E27	FA_FB_S126	U2-V8		VCC_B3	
	VCC_A2		U1-D27	FA_FB_S127	U2-U7		VCC_B3	
	VCC_A2		U1-F21	FA_FB_S128	U2-D10		VCC_B3	
	VCC_A2		U1-E20	FA_FB_S129	U2-D11		VCC_B3	
	VCC_A2		U1-D21	FA_FB_S130	U2-B8		VCC_B3	
	VCC_A2		U1-C21	FA_FB_S131	U2-B9		VCC_B3	
	VCC_A2		U1-D17	FA_FB_S132	U2-J15		VCC_B3	
	VCC_A2		U1-D18	FA_FB_S133	U2-J16		VCC_B3	
	VCC_A2		U1-D13	FA_FB_S134	U2-J6		VCC_B3	
	VCC_A2		U1-E13	FA_FB_S135	U2-K7		VCC_B3	
	VCC_A2		U1-P21	FA_FB_S136	U2-C3		VCC_B3	
	VCC_A2		U1-N20	FA_FB_S137	U2-C4		VCC_B3	
	VCC_A2		U1-G16	FA_FB_S138	U2-F4		VCC_B3	
	VCC_A2		U1-F16	FA_FB_S139	U2-E4		VCC_B3	
	VCC_A1		U1-R39	FA_FB_S140	U2-L25		VCC_B2	
	VCC_A1		U1-R38	FA_FB_S141	U2-M24		VCC_B2	
	VCC_A1		U1-N41	FA_FB_S142	U2-P23		VCC_B2	
	VCC_A1		U1-N40	FA_FB_S143	U2-N24		VCC_B2	
	VCC_A1		U1-V38	FA_FB_S144	U2-D28		VCC_B2	
	VCC_A1		U1-U38	FA_FB_S145	U2-E28		VCC_B2	
	VCC_A1		U1-K38	FA_FB_S146	U2-E22		VCC_B2	
	VCC_A1		U1-L37	FA_FB_S147	U2-D22		VCC_B2	
	VCC_A1		U1-J40	FA_FB_S148	U2-B22		VCC_B2	
	VCC_A1		U1-K39	FA_FB_S149	U2-A22		VCC_B2	
	VCC_A1		U1-M38	FA_FB_S150	U2-F26		VCC_B2	
	VCC_A1		U1-M37	FA_FB_S151	U2-F25		VCC_B2	
	VCC_A1		U1-L42	FA_FB_S152	U2-A27		VCC_B2	
	VCC_A1		U1-L41	FA_FB_S153	U2-A26		VCC_B2	
	VCC_A1		U1-J42	FA_FB_S154	U2-E27		VCC_B2	
	VCC_A1		U1-H41	FA_FB_S155	U2-D27		VCC_B2	
	VCC_A1		U1-G37	FA_FB_S156	U2-F21		VCC_B2	
	VCC_A1		U1-H36	FA_FB_S157	U2-E20		VCC_B2	
	VCC_A1		U1-C41	FA_FB_S158	U2-D21		VCC_B2	
	VCC_A1		U1-C40	FA_FB_S159	U2-C21		VCC_B2	
	VCC_A1		U1-J38	FA_FB_S160	U2-D17		VCC_B2	
	VCC_A1		U1-J37	FA_FB_S161	U2-D18		VCC_B2	
	VCC_A1		U1-P27	FA_FB_S162	U2-D13		VCC_B2	
	VCC_A1		U1-R27	FA_FB_S163	U2-E13		VCC_B2	
	VCC_A1		U1-A35	FA_FB_S164	U2-P21		VCC_B2	
	VCC_A1		U1-A34	FA_FB_S165	U2-N20		VCC_B2	
	VCC_A1		U1-D33	FA_FB_S166	U2-G16		VCC_B2	
	VCC_A1		U1-E33	FA_FB_S167	U2-F16		VCC_B2	

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3.2.2. FPGA C to FPGA D

FPGA C - FPGA D(FAST)								
note	VCCO		FPGA C	Signal	FPGA D		VCCO	note
	2.5V	P	U3-J8	FC_FD1	U4-J8	P	2.5V	
	2.5V	N	U3-H8	FC_FD2	U4-H8	N	2.5V	
	2.5V	P	U3-N16	FC_FD3	U4-N16	P	2.5V	
	2.5V	N	U3-P16	FC_FD4	U4-P16	N	2.5V	
SRCC	2.5V	P	U3-BB4	FC_FD5	U4-BB4	P	2.5V	SRCC
SRCC	2.5V	N	U3-BB3	FC_FD6	U4-BB3	N	2.5V	SRCC
MRCC	2.5V	P	U3-AY3	FC_FD7	U4-AY3	P	2.5V	MRCC
MRCC	2.5V	N	U3-AW3	FC_FD8	U4-AW3	N	2.5V	MRCC
MRCC	2.5V	P	U3-AV5	FC_FD9	U4-AV5	P	2.5V	MRCC
MRCC	2.5V	N	U3-AV4	FC_FD10	U4-AV4	N	2.5V	MRCC
SRCC	2.5V	P	U3-AK9	FC_FD11	U4-AK9	P	2.5V	SRCC
SRCC	2.5V	N	U3-AL9	FC_FD12	U4-AL9	N	2.5V	SRCC
	2.5V	P	U3-AT5	FC_FD13	U4-AT5	P	2.5V	
VREF	2.5V	N	U3-AT4	FC_FD14	U4-AT4	N	2.5V	VREF
	2.5V	P	U3-AP7	FC_FD15	U4-AP7	P	2.5V	
	2.5V	N	U3-AP6	FC_FD16	U4-AP6	N	2.5V	
	2.5V	P	U3-AK12	FC_FD17	U4-AK12	P	2.5V	
	2.5V	N	U3-AJ12	FC_FD18	U4-AJ12	N	2.5V	
	2.5V	P	U3-AM9	FC_FD19	U4-AM9	P	2.5V	
	2.5V	N	U3-AL10	FC_FD20	U4-AL10	N	2.5V	
	2.5V	P	U3-AL12	FC_FD21	U4-AL12	P	2.5V	
	2.5V	N	U3-AL11	FC_FD22	U4-AL11	N	2.5V	
	2.5V	P	U3-F37	FC_FD23	U4-F37	P	2.5V	
	2.5V	N	U3-E37	FC_FD24	U4-E37	N	2.5V	
	2.5V	P	U3-N30	FC_FD25	U4-N30	P	2.5V	
	2.5V	N	U3-P31	FC_FD26	U4-P31	N	2.5V	
SRCC	2.5V	P	U3-AR35	FC_FD27	U4-AR35	P	2.5V	SRCC
SRCC	2.5V	N	U3-AT36	FC_FD28	U4-AT36	N	2.5V	SRCC
MRCC	2.5V	P	U3-AT37	FC_FD29	U4-AT37	P	2.5V	MRCC
MRCC	2.5V	N	U3-AR37	FC_FD30	U4-AR37	N	2.5V	MRCC
MRCC	2.5V	P	U3-AP37	FC_FD31	U4-AP37	P	2.5V	MRCC
MRCC	2.5V	N	U3-AN36	FC_FD32	U4-AN36	N	2.5V	MRCC
SRCC	2.5V	P	U3-AJ31	FC_FD33	U4-AJ31	P	2.5V	SRCC
SRCC	2.5V	N	U3-AH30	FC_FD34	U4-AH30	N	2.5V	SRCC
	2.5V	P	U3-AL31	FC_FD35	U4-AL31	P	2.5V	
VREF	2.5V	N	U3-AL32	FC_FD36	U4-AL32	N	2.5V	VREF
	2.5V	P	U3-AL29	FC_FD37	U4-AL29	P	2.5V	
	2.5V	N	U3-AK29	FC_FD38	U4-AK29	N	2.5V	
	2.5V	P	U3-AP35	FC_FD39	U4-AP35	P	2.5V	
	2.5V	N	U3-AP36	FC_FD40	U4-AP36	N	2.5V	
	2.5V	P	U3-AK30	FC_FD41	U4-AK30	P	2.5V	
	2.5V	N	U3-AL30	FC_FD42	U4-AL30	N	2.5V	
	2.5V	P	U3-AH29	FC_FD43	U4-AH29	P	2.5V	
	2.5V	N	U3-AJ30	FC_FD44	U4-AJ30	N	2.5V	
SRCC	2.5V	N	U3-BB38	FC_FD45	U4-BB38	N	2.5V	SRCC
	VCC_A6B4C3D1	P	U3-P11	FC_FD46	U4-R39	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	N	U3-P12	FC_FD47	U4-R38	N	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	P	U3-F4	FC_FD48	U4-N41	P	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	N	U3-E4	FC_FD49	U4-N40	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U3-C3	FC_FD50	U4-V38	P	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	N	U3-C4	FC_FD51	U4-U38	N	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	P	U3-V8	FC_FD52	U4-K38	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	N	U3-U7	FC_FD53	U4-L37	N	VCC_A6B4C3D1	
	VCC_A6B4C3D1	P	U3-R4	FC_FD54	U4-J40	P	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	N	U3-R5	FC_FD55	U4-K39	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U3-B8	FC_FD56	U4-M38	P	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	N	U3-B9	FC_FD57	U4-M37	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U3-P5	FC_FD58	U4-L42	P	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	N	U3-N4	FC_FD59	U4-L41	N	VCC_A6B4C3D1	

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FPGA C - FPGA D(FAST)								
note	VCCO		FPGA C	Signal	FPGA D		VCCO	note
	VCC_A6B4C3D1	P	U3-D10	FC_FD60	U4-J42	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	N	U3-D11	FC_FD61	U4-H41	N	VCC_A6B4C3D1	
	VCC_A6B4C3D1	P	U3-C1	FC_FD62	U4-G37	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	N	U3-D2	FC_FD63	U4-H36	N	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	P	U3-V5	FC_FD64	U4-C41	P	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	N	U3-V6	FC_FD65	U4-C40	N	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	P	U3-J6	FC_FD66	U4-J38	P	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	N	U3-K7	FC_FD67	U4-J37	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U3-J15	FC_FD68	U4-P27	P	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	N	U3-J16	FC_FD69	U4-R27	N	VCC_A6B4C3D1	
	VCC_A6B4C3D1	P	U3-V1	FC_FD70	U4-A35	P	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	N	U3-U1	FC_FD71	U4-A34	N	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	P	U3-T6	FC_FD72	U4-D33	P	VCC_A6B4C3D1	MRCC
MRCC	VCC_A6B4C3D1	N	U3-T7	FC_FD73	U4-E33	N	VCC_A6B4C3D1	MRCC
	VCC_A6B4C3D1	P	U3-M11	FC_FD74	U4-H29	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	P	U3-L5	FC_FD75	U4-C35	P	VCC_A6B4C3D1	
	VCC_A6B4C3D1	N	U3-M6	FC_FD76	U4-B34	N	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	P	U3-K3	FC_FD77	U4-D35	P	VCC_A6B4C3D1	
MRCC	VCC_A6B4C3D1	N	U3-K4	FC_FD78	U4-E34	N	VCC_A6B4C3D1	
	VCC_C6D4	P	U3-AG12	FC_FD79	U4-Y38	P	VCC_C6D4	
	VCC_C6D4	N	U3-AG11	FC_FD80	U4-Y37	N	VCC_C6D4	
	VCC_C6D4	P	U3-AF12	FC_FD81	U4-AA40	P	VCC_C6D4	MRCC
	VCC_C6D4	N	U3-AF11	FC_FD82	U4-Y40	N	VCC_C6D4	MRCC
MRCC	VCC_C6D4	P	U3-AH4	FC_FD83	U4-AB37	P	VCC_C6D4	MRCC
MRCC	VCC_C6D4	N	U3-AG4	FC_FD84	U4-AA37	N	VCC_C6D4	MRCC
MRCC	VCC_C6D4	P	U3-AE7	FC_FD85	U4-AF39	P	VCC_C6D4	
MRCC	VCC_C6D4	N	U3-AD7	FC_FD86	U4-AE39	N	VCC_C6D4	
	VCC_C6D4	P	U3-AM6	FC_FD87	U4-AD36	P	VCC_C6D4	MRCC
	VCC_C6D4	N	U3-AL6	FC_FD88	U4-AD35	N	VCC_C6D4	MRCC
	VCC_C6D4	P	U3-AU9	FC_FD89	U4-AF36	P	VCC_C6D4	MRCC
	VCC_C6D4	N	U3-AV9	FC_FD90	U4-AF37	N	VCC_C6D4	MRCC
MRCC	VCC_C6D4	P	U3-Y7	FC_FD91	U4-AM42	P	VCC_C6D4	
MRCC	VCC_C6D4	N	U3-Y8	FC_FD92	U4-AL41	N	VCC_C6D4	
	VCC_C6D4	P	U3-AA6	FC_FD93	U4-AG36	P	VCC_C6D4	
	VCC_C6D4	N	U3-AA7	FC_FD94	U4-AG37	N	VCC_C6D4	
MRCC	VCC_C6D4	P	U3-AP1	FC_FD95	U4-AM39	P	VCC_C6D4	
MRCC	VCC_C6D4	N	U3-AN1	FC_FD96	U4-AL39	N	VCC_C6D4	
MRCC	VCC_C6D4	P	U3-AU14	FC_FD97	U4-AN41	P	VCC_C6D4	MRCC
MRCC	VCC_C6D4	N	U3-AU13	FC_FD98	U4-AM41	N	VCC_C6D4	MRCC
MRCC	VCC_C6D4	P	U3-AL5	FC_FD99	U4-AK37	P	VCC_C6D4	MRCC
MRCC	VCC_C6D4	N	U3-AK5	FC_FD100	U4-AJ36	N	VCC_C6D4	MRCC
MRCC	VCC_C6D4	P	U3-AT14	FC_FD101	U4-AJ28	P	VCC_C6D4	
MRCC	VCC_C6D4	N	U3-AR15	FC_FD102	U4-AK28	N	VCC_C6D4	
	VCC_C6D4	P	U3-AH8	FC_FD103	U4-AR30	P	VCC_C6D4	MRCC
	VCC_C6D4	N	U3-AJ7	FC_FD104	U4-AT31	N	VCC_C6D4	MRCC
MRCC	VCC_C6D4	P	U3-AC4	FC_FD105	U4-AW32	P	VCC_C6D4	MRCC
MRCC	VCC_C6D4	N	U3-AB4	FC_FD106	U4-AW33	N	VCC_C6D4	MRCC
	VCC_C6D4	P	U3-AE10	FC_FD107	U4-AM29	P	VCC_C6D4	
	VCC_C6D4	P	U3-AD6	FC_FD108	U4-AL26	P	VCC_C6D4	
	VCC_C6D4	N	U3-AD5	FC_FD109	U4-AM27	N	VCC_C6D4	
	VCC_C6D4	P	U3-AH6	FC_FD110	U4-AK27	P	VCC_C6D4	
	VCC_C6D4	N	U3-AH5	FC_FD111	U4-AJ27	N	VCC_C6D4	

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FPGA C - FPGA D(SLOW)								
note	VCCO		FPGA C	Signal	FPGA D		VCCO	note
	VCC_C5		U3-AU29	FC_FD_S112	U4-AU9		VCC_D6	
	VCC_C5		U3-AV29	FC_FD_S113	U4-AV9		VCC_D6	
	VCC_C5		U3-AW28	FC_FD_S114	U4-AT14		VCC_D6	
	VCC_C5		U3-AY29	FC_FD_S115	U4-AR15		VCC_D6	
	VCC_C5		U3-AU26	FC_FD_S116	U4-AU14		VCC_D6	
	VCC_C5		U3-AT26	FC_FD_S117	U4-AU13		VCC_D6	
	VCC_C5		U3-AV26	FC_FD_S118	U4-AH6		VCC_D6	
	VCC_C5		U3-AV25	FC_FD_S119	U4-AH5		VCC_D6	
	VCC_C5		U3-AP25	FC_FD_S120	U4-AP1		VCC_D6	
	VCC_C5		U3-AR25	FC_FD_S121	U4-AN1		VCC_D6	
	VCC_C5		U3-AT22	FC_FD_S122	U4-AL5		VCC_D6	
	VCC_C5		U3-AU22	FC_FD_S123	U4-AK5		VCC_D6	
	VCC_C5		U3-BA22	FC_FD_S124	U4-AM6		VCC_D6	
	VCC_C5		U3-BB22	FC_FD_S125	U4-AL6		VCC_D6	
	VCC_C5		U3-AU23	FC_FD_S126	U4-AH8		VCC_D6	
	VCC_C5		U3-AV23	FC_FD_S127	U4-AJ7		VCC_D6	
	VCC_C5		U3-AU18	FC_FD_S128	U4-AA6		VCC_D6	
	VCC_C5		U3-AV18	FC_FD_S129	U4-AA7		VCC_D6	
	VCC_C5		U3-BA20	FC_FD_S130	U4-Y7		VCC_D6	
	VCC_C5		U3-BB19	FC_FD_S131	U4-Y8		VCC_D6	
	VCC_C5		U3-AM22	FC_FD_S132	U4-AC4		VCC_D6	
	VCC_C5		U3-AL22	FC_FD_S133	U4-AB4		VCC_D6	
	VCC_C5		U3-AV13	FC_FD_S134	U4-AD6		VCC_D6	
	VCC_C5		U3-AV14	FC_FD_S135	U4-AD5		VCC_D6	
	VCC_C5		U3-AT17	FC_FD_S136	U4-AE7		VCC_D6	
	VCC_C5		U3-AR18	FC_FD_S137	U4-AD7		VCC_D6	
	VCC_C5		U3-AK20	FC_FD_S138	U4-AH4		VCC_D6	
	VCC_C5		U3-AJ21	FC_FD_S139	U4-AG4		VCC_D6	
	VCC_C4		U3-Y38	FC_FD_S140	U4-AU29		VCC_D5	
	VCC_C4		U3-Y37	FC_FD_S141	U4-AV29		VCC_D5	
	VCC_C4		U3-AA40	FC_FD_S142	U4-AW28		VCC_D5	
	VCC_C4		U3-Y40	FC_FD_S143	U4-AY29		VCC_D5	
	VCC_C4		U3-AB37	FC_FD_S144	U4-AU26		VCC_D5	
	VCC_C4		U3-AA37	FC_FD_S145	U4-AT26		VCC_D5	
	VCC_C4		U3-AF39	FC_FD_S146	U4-AV26		VCC_D5	
	VCC_C4		U3-AE39	FC_FD_S147	U4-AV25		VCC_D5	
	VCC_C4		U3-AD36	FC_FD_S148	U4-AP25		VCC_D5	
	VCC_C4		U3-AD35	FC_FD_S149	U4-AR25		VCC_D5	
	VCC_C4		U3-AF36	FC_FD_S150	U4-AT22		VCC_D5	
	VCC_C4		U3-AF37	FC_FD_S151	U4-AU22		VCC_D5	
	VCC_C4		U3-AM42	FC_FD_S152	U4-BA22		VCC_D5	
	VCC_C4		U3-AL41	FC_FD_S153	U4-BB22		VCC_D5	
	VCC_C4		U3-AG36	FC_FD_S154	U4-AU23		VCC_D5	
	VCC_C4		U3-AG37	FC_FD_S155	U4-AV23		VCC_D5	
	VCC_C4		U3-AM39	FC_FD_S156	U4-AU18		VCC_D5	
	VCC_C4		U3-AL39	FC_FD_S157	U4-AV18		VCC_D5	
	VCC_C4		U3-AN41	FC_FD_S158	U4-BA20		VCC_D5	
	VCC_C4		U3-AM41	FC_FD_S159	U4-BB19		VCC_D5	
	VCC_C4		U3-AK37	FC_FD_S160	U4-AM22		VCC_D5	
	VCC_C4		U3-AJ36	FC_FD_S161	U4-AL22		VCC_D5	
	VCC_C4		U3-AJ28	FC_FD_S162	U4-AV13		VCC_D5	
	VCC_C4		U3-AK28	FC_FD_S163	U4-AV14		VCC_D5	
	VCC_C4		U3-AR30	FC_FD_S164	U4-AT17		VCC_D5	
	VCC_C4		U3-AT31	FC_FD_S165	U4-AR18		VCC_D5	
	VCC_C4		U3-AW32	FC_FD_S166	U4-AK20		VCC_D5	
	VCC_C4		U3-AW33	FC_FD_S167	U4-AJ21		VCC_D5	

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3.2.3. FPGA A to FPGA C

FPGA A - FPGA C								
note	VCCO		FPGA A	Signal	FPGA C		VCCO	note
	VCC_A45C12	P	U1-Y38	FA_FC1	U3-R39	P	VCC_A45C12	
	VCC_A45C12	N	U1-Y37	FA_FC2	U3-R38	N	VCC_A45C12	
MRCC	VCC_A45C12	P	U1-AA40	FA_FC3	U3-N41	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-Y40	FA_FC4	U3-N40	N	VCC_A45C12	MRCC
MRCC	VCC_A45C12	P	U1-AB37	FA_FC5	U3-V38	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AA37	FA_FC6	U3-U38	N	VCC_A45C12	MRCC
	VCC_A45C12	P	U1-AF39	FA_FC7	U3-K38	P	VCC_A45C12	
	VCC_A45C12	N	U1-AE39	FA_FC8	U3-L37	N	VCC_A45C12	
MRCC	VCC_A45C12	P	U1-AD36	FA_FC9	U3-J40	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AD35	FA_FC10	U3-K39	N	VCC_A45C12	MRCC
MRCC	VCC_A45C12	P	U1-AF36	FA_FC11	U3-M38	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AF37	FA_FC12	U3-M37	N	VCC_A45C12	MRCC
	VCC_A45C12	P	U1-AM42	FA_FC13	U3-L42	P	VCC_A45C12	
	VCC_A45C12	N	U1-AL41	FA_FC14	U3-L41	N	VCC_A45C12	
	VCC_A45C12	P	U1-AG36	FA_FC15	U3-J42	P	VCC_A45C12	
	VCC_A45C12	N	U1-AG37	FA_FC16	U3-H41	N	VCC_A45C12	
	VCC_A45C12	P	U1-AM39	FA_FC17	U3-G37	P	VCC_A45C12	
	VCC_A45C12	N	U1-AL39	FA_FC18	U3-H36	N	VCC_A45C12	
MRCC	VCC_A45C12	P	U1-AN41	FA_FC19	U3-C41	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AM41	FA_FC20	U3-C40	N	VCC_A45C12	MRCC
MRCC	VCC_A45C12	P	U1-AK37	FA_FC21	U3-J38	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AJ36	FA_FC22	U3-J37	N	VCC_A45C12	MRCC
	VCC_A45C12	P	U1-AJ28	FA_FC23	U3-P27	P	VCC_A45C12	
	VCC_A45C12	N	U1-AK28	FA_FC24	U3-R27	N	VCC_A45C12	
MRCC	VCC_A45C12	P	U1-AR30	FA_FC25	U3-A35	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AT31	FA_FC26	U3-A34	N	VCC_A45C12	MRCC
MRCC	VCC_A45C12	P	U1-AW32	FA_FC27	U3-D33	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AW33	FA_FC28	U3-E33	N	VCC_A45C12	MRCC
	VCC_A45C12	P	U1-AM29	FA_FC29	U3-H29	P	VCC_A45C12	
	VCC_A45C12	P	U1-AL26	FA_FC30	U3-C35	P	VCC_A45C12	
	VCC_A45C12	N	U1-AM27	FA_FC31	U3-B34	N	VCC_A45C12	
	VCC_A45C12	P	U1-AK27	FA_FC32	U3-D35	P	VCC_A45C12	
	VCC_A45C12	N	U1-AJ27	FA_FC33	U3-E34	N	VCC_A45C12	
	VCC_A45C12	P	U1-AU29	FA_FC34	U3-L25	P	VCC_A45C12	
	VCC_A45C12	N	U1-AV29	FA_FC35	U3-M24	N	VCC_A45C12	
MRCC	VCC_A45C12	P	U1-AW28	FA_FC36	U3-P23	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AY29	FA_FC37	U3-N24	N	VCC_A45C12	MRCC
MRCC	VCC_A45C12	P	U1-AU26	FA_FC38	U3-D28	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AT26	FA_FC39	U3-E28	N	VCC_A45C12	MRCC
	VCC_A45C12	P	U1-AV26	FA_FC40	U3-E22	P	VCC_A45C12	
	VCC_A45C12	N	U1-AV25	FA_FC41	U3-D22	N	VCC_A45C12	
MRCC	VCC_A45C12	P	U1-AP25	FA_FC42	U3-B22	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AR25	FA_FC43	U3-A22	N	VCC_A45C12	MRCC
MRCC	VCC_A45C12	P	U1-AT22	FA_FC44	U3-F26	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AU22	FA_FC45	U3-F25	N	VCC_A45C12	MRCC
	VCC_A45C12	P	U1-BA22	FA_FC46	U3-A27	P	VCC_A45C12	
	VCC_A45C12	N	U1-BB22	FA_FC47	U3-A26	N	VCC_A45C12	
	VCC_A45C12	P	U1-AU23	FA_FC48	U3-E27	P	VCC_A45C12	
	VCC_A45C12	N	U1-AV23	FA_FC49	U3-D27	N	VCC_A45C12	
	VCC_A45C12	P	U1-AU18	FA_FC50	U3-F21	P	VCC_A45C12	
	VCC_A45C12	N	U1-AV18	FA_FC51	U3-E20	N	VCC_A45C12	
MRCC	VCC_A45C12	P	U1-BA20	FA_FC52	U3-D21	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-BB19	FA_FC53	U3-C21	N	VCC_A45C12	MRCC
MRCC	VCC_A45C12	P	U1-AM22	FA_FC54	U3-D17	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AL22	FA_FC55	U3-D18	N	VCC_A45C12	MRCC
	VCC_A45C12	P	U1-AV13	FA_FC56	U3-D13	P	VCC_A45C12	
	VCC_A45C12	N	U1-AV14	FA_FC57	U3-E13	N	VCC_A45C12	
MRCC	VCC_A45C12	P	U1-AT17	FA_FC58	U3-P21	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AR18	FA_FC59	U3-N20	N	VCC_A45C12	MRCC
MRCC	VCC_A45C12	P	U1-AK20	FA_FC60	U3-G16	P	VCC_A45C12	MRCC
MRCC	VCC_A45C12	N	U1-AJ21	FA_FC61	U3-F16	N	VCC_A45C12	MRCC
	VCC_A45C12	P	U1-BB12	FA_FC62	U3-K19	P	VCC_A45C12	
	VCC_A45C12	P	U1-AL21	FA_FC63	U3-R17	P	VCC_A45C12	
	VCC_A45C12	N	U1-AL20	FA_FC64	U3-P18	N	VCC_A45C12	
	VCC_A45C12	P	U1-AU17	FA_FC65	U3-M18	P	VCC_A45C12	
	VCC_A45C12	N	U1-AV16	FA_FC66	U3-M19	N	VCC_A45C12	

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3.2.4. FPGA B to FPGA D

FPGA B - FPGA D								
note	VCCO		FPGA B	Signal	FPGA D		VCCO	note
	VCC_B56D23	P	U2-AU29	FB_FD1	U4-L25	P	VCC_B56D23	
	VCC_B56D23	N	U2-AV29	FB_FD2	U4-M24	N	VCC_B56D23	
MRCC	VCC_B56D23	P	U2-AW28	FB_FD3	U4-P23	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AY29	FB_FD4	U4-N24	N	VCC_B56D23	MRCC
MRCC	VCC_B56D23	P	U2-AU26	FB_FD5	U4-D28	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AT26	FB_FD6	U4-E28	N	VCC_B56D23	MRCC
	VCC_B56D23	P	U2-AV26	FB_FD7	U4-E22	P	VCC_B56D23	
	VCC_B56D23	N	U2-AV25	FB_FD8	U4-D22	N	VCC_B56D23	
MRCC	VCC_B56D23	P	U2-AP25	FB_FD9	U4-B22	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AR25	FB_FD10	U4-A22	N	VCC_B56D23	MRCC
MRCC	VCC_B56D23	P	U2-AT22	FB_FD11	U4-F26	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AU22	FB_FD12	U4-F25	N	VCC_B56D23	MRCC
	VCC_B56D23	P	U2-BA22	FB_FD13	U4-A27	P	VCC_B56D23	
	VCC_B56D23	N	U2-BB22	FB_FD14	U4-A26	N	VCC_B56D23	
	VCC_B56D23	P	U2-AU23	FB_FD15	U4-E27	P	VCC_B56D23	
	VCC_B56D23	N	U2-AV23	FB_FD16	U4-D27	N	VCC_B56D23	
	VCC_B56D23	P	U2-AU18	FB_FD17	U4-F21	P	VCC_B56D23	
	VCC_B56D23	N	U2-AV18	FB_FD18	U4-E20	N	VCC_B56D23	
MRCC	VCC_B56D23	P	U2-BA20	FB_FD19	U4-D21	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-BB19	FB_FD20	U4-C21	N	VCC_B56D23	MRCC
MRCC	VCC_B56D23	P	U2-AM22	FB_FD21	U4-D17	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AL22	FB_FD22	U4-D18	N	VCC_B56D23	MRCC
	VCC_B56D23	P	U2-AV13	FB_FD23	U4-D13	P	VCC_B56D23	
	VCC_B56D23	N	U2-AV14	FB_FD24	U4-E13	N	VCC_B56D23	
MRCC	VCC_B56D23	P	U2-AT17	FB_FD25	U4-P21	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AR18	FB_FD26	U4-N20	N	VCC_B56D23	MRCC
MRCC	VCC_B56D23	P	U2-AK20	FB_FD27	U4-G16	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AJ21	FB_FD28	U4-F16	N	VCC_B56D23	MRCC
	VCC_B56D23	P	U2-BB12	FB_FD29	U4-K19	P	VCC_B56D23	
	VCC_B56D23	P	U2-AL21	FB_FD30	U4-R17	P	VCC_B56D23	
	VCC_B56D23	N	U2-AL20	FB_FD31	U4-P18	N	VCC_B56D23	
	VCC_B56D23	P	U2-AU17	FB_FD32	U4-M18	P	VCC_B56D23	
	VCC_B56D23	N	U2-AV16	FB_FD33	U4-M19	N	VCC_B56D23	
	VCC_B56D23	P	U2-AU9	FB_FD34	U4-L5	P	VCC_B56D23	
	VCC_B56D23	N	U2-AV9	FB_FD35	U4-M6	N	VCC_B56D23	
MRCC	VCC_B56D23	P	U2-AT14	FB_FD36	U4-K3	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AR15	FB_FD37	U4-K4	N	VCC_B56D23	MRCC
MRCC	VCC_B56D23	P	U2-AU14	FB_FD38	U4-P5	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AU13	FB_FD39	U4-N4	N	VCC_B56D23	MRCC
	VCC_B56D23	P	U2-AH6	FB_FD40	U4-R4	P	VCC_B56D23	
	VCC_B56D23	N	U2-AH5	FB_FD41	U4-R5	N	VCC_B56D23	
MRCC	VCC_B56D23	P	U2-AP1	FB_FD42	U4-T6	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AN1	FB_FD43	U4-T7	N	VCC_B56D23	MRCC
MRCC	VCC_B56D23	P	U2-AL5	FB_FD44	U4-V5	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AK5	FB_FD45	U4-V6	N	VCC_B56D23	MRCC
	VCC_B56D23	P	U2-AM6	FB_FD46	U4-V1	P	VCC_B56D23	
	VCC_B56D23	N	U2-AL6	FB_FD47	U4-U1	N	VCC_B56D23	
	VCC_B56D23	P	U2-AH8	FB_FD48	U4-V8	P	VCC_B56D23	
	VCC_B56D23	N	U2-AJ7	FB_FD49	U4-U7	N	VCC_B56D23	
	VCC_B56D23	P	U2-AA6	FB_FD50	U4-D10	P	VCC_B56D23	
	VCC_B56D23	N	U2-AA7	FB_FD51	U4-D11	N	VCC_B56D23	
MRCC	VCC_B56D23	P	U2-Y7	FB_FD52	U4-B8	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-Y8	FB_FD53	U4-B9	N	VCC_B56D23	MRCC
MRCC	VCC_B56D23	P	U2-AC4	FB_FD54	U4-J15	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AB4	FB_FD55	U4-J16	N	VCC_B56D23	MRCC
	VCC_B56D23	P	U2-AD6	FB_FD56	U4-J6	P	VCC_B56D23	
	VCC_B56D23	N	U2-AD5	FB_FD57	U4-K7	N	VCC_B56D23	
MRCC	VCC_B56D23	P	U2-AE7	FB_FD58	U4-C3	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AD7	FB_FD59	U4-C4	N	VCC_B56D23	MRCC
MRCC	VCC_B56D23	P	U2-AH4	FB_FD60	U4-F4	P	VCC_B56D23	MRCC
MRCC	VCC_B56D23	N	U2-AG4	FB_FD61	U4-E4	N	VCC_B56D23	MRCC
	VCC_B56D23	P	U2-AE10	FB_FD62	U4-M11	P	VCC_B56D23	
	VCC_B56D23	P	U2-AG12	FB_FD63	U4-C1	P	VCC_B56D23	
	VCC_B56D23	N	U2-AG11	FB_FD64	U4-D2	N	VCC_B56D23	
	VCC_B56D23	P	U2-AF12	FB_FD65	U4-P11	P	VCC_B56D23	
	VCC_B56D23	N	U2-AF11	FB_FD66	U4-P12	N	VCC_B56D23	

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3.2.5. FPGA A and FPGA B and FPGA C and FPGA D (Global bus)

FPGA A - FPGA B - FPGA C - FPGA D						
signal	FPGA A	FPGA B	FPGA C	FPGA D	VCCO	note
SM_D0	U1-AJ11	U4-AJ11	U3-AJ11	U2-AJ11	2.5V	
SM_D1	U1-AK10	U4-AK10	U3-AK10	U2-AK10	2.5V	
SM_D2	U1-BA4	U4-BA4	U3-BA4	U2-BA4	2.5V	
SM_D3	U1-AY4	U4-AY4	U3-AY4	U2-AY4	2.5V	
SM_D4	U1-BB2	U4-BB2	U3-BB2	U2-BB2	2.5V	
SM_D5	U1-BA2	U4-BA2	U3-BA2	U2-BA2	2.5V	
SM_D6	U1-AP5	U4-AP5	U3-AP5	U2-AP5	2.5V	
SM_D7	U1-AR5	U4-AR5	U3-AR5	U2-AR5	2.5V	
SM_D8	U1-AM7	U4-AM7	U3-AM7	U2-AM7	2.5V	
SM_D9	U1-AN6	U4-AN6	U3-AN6	U2-AN6	2.5V	
SM_D10	U1-AV3	U4-AV3	U3-AV3	U2-AV3	2.5V	VREF
SM_D11	U1-AU4	U4-AU4	U3-AU4	U2-AU4	2.5V	
SM_D12	U1-BA1	U4-BA1	U3-BA1	U2-BA1	2.5V	
SM_D13	U1-AY2	U4-AY2	U3-AY2	U2-AY2	2.5V	
SM_D14	U1-AK8	U4-AK8	U3-AK8	U2-AK8	2.5V	
SM_D15	U1-AL7	U4-AL7	U3-AL7	U2-AL7	2.5V	
SM_D16	U1-AM34	U4-AM34	U3-AM34	U2-AM34	2.5V	
SM_D17	U1-AM33	U4-AM33	U3-AM33	U2-AM33	2.5V	
SM_D18	U1-AN35	U4-AN35	U3-AN35	U2-AN35	2.5V	
SM_D19	U1-AN34	U4-AN34	U3-AN34	U2-AN34	2.5V	
SM_D20	U1-AL34	U4-AL34	U3-AL34	U2-AL34	2.5V	
SM_D21	U1-AL35	U4-AL35	U3-AL35	U2-AL35	2.5V	
SM_D22	U1-AM38	U4-AM38	U3-AM38	U2-AM38	2.5V	
SM_D23	U1-AN38	U4-AN38	U3-AN38	U2-AN38	2.5V	
SM_D24	U1-AM37	U4-AM37	U3-AM37	U2-AM37	2.5V	
SM_D25	U1-AM36	U4-AM36	U3-AM36	U2-AM36	2.5V	
SM_D26	U1-AJ33	U4-AJ33	U3-AJ33	U2-AJ33	2.5V	VREF
SM_D27	U1-AK34	U4-AK34	U3-AK34	U2-AK34	2.5V	
SM_D28	U1-AR39	U4-AR39	U3-AR39	U2-AR39	2.5V	
SM_D29	U1-AT39	U4-AT39	U3-AT39	U2-AT39	2.5V	
SM_D30	U1-AH31	U4-AH31	U3-AH31	U2-AH31	2.5V	
SM_D31	U1-AJ32	U4-AJ32	U3-AJ32	U2-AJ32	2.5V	
SM_D32	U1-BA37	U4-BA37	U3-BA37	U2-BA37	2.5V	
SM_D33	U1-BA41	U4-BA41	U3-BA41	U2-BA41	2.5V	
SM_D34	U1-BB41	U4-BB41	U3-BB41	U2-BB41	2.5V	
SM_D35	U1-BA40	U4-BA40	U3-BA40	U2-BA40	2.5V	SRCC
SM_D36	U1-BB39	U4-BB39	U3-BB39	U2-BB39	2.5V	SRCC

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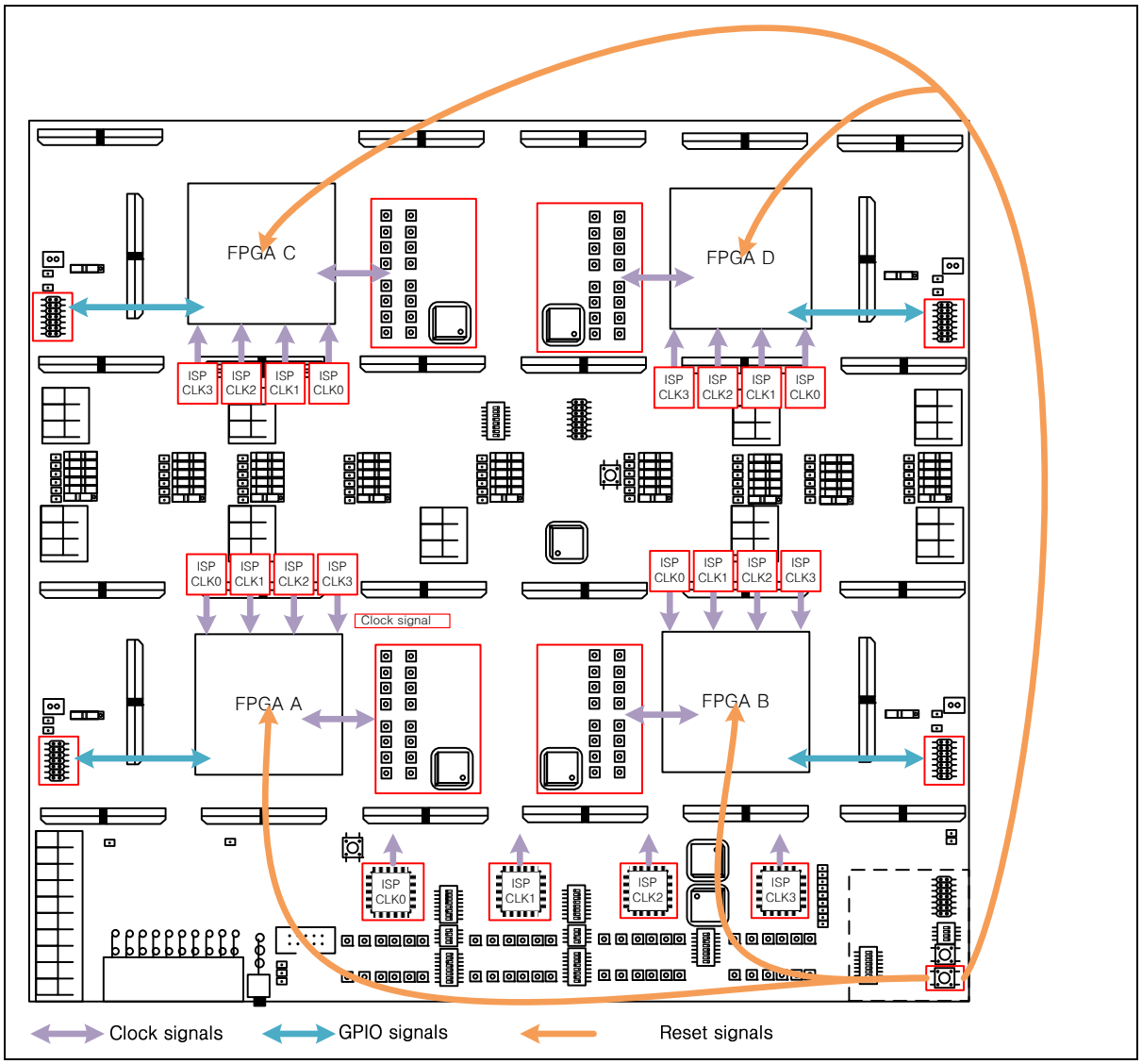
3.3. Signals between FPGAs and Devices(Reset, Clock, GPIO)



- FPGA pins connected to Reset, Clock, GPIO: 44 page
- Clocks of ISPCLK0/1/2/3 are connected to each FPGA.

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3.3.1. Clock signals

CLOCK signals						
Signal	FPGA A	FPGA B	FPGA C	FPGA D	VCCO	note
CLK_Fx_EXT_IN0	U1-AH11	U2-AH11	U3-AH11	U4-AH11	2.5V	P
CLK_Fx_EXT_IN1	U1-AJ10	U2-AJ10	U3-AJ10	U4-AJ10	2.5V	N
CLK_Fx_EXT_IN2	U1-AW2	U2-AW2	U3-AW2	U4-AW2	2.5V	P
CLK_Fx_EXT_IN3	U1-AW1	U2-AW1	U3-AW1	U4-AW1	2.5V	N
CLK_Fx_EXT_OUT0	U1-AW7	U2-AW7	U3-AW7	U4-AW7	2.5V	P
CLK_Fx_EXT_OUT1	U1-AY7	U2-AY7	U3-AY7	U4-AY7	2.5V	N
CLK_Fx_EXT_OUT2	U1-BB6	U2-BB6	U3-BB6	U4-BB6	2.5V	P
CLK_Fx_EXT_OUT3	U1-BA6	U2-BA6	U3-BA6	U4-BA6	2.5V	N
CLK_Fx_EXT_OUT4	U1-AW6	U2-AW6	U3-AW6	U4-AW6	2.5V	P
CLK_Fx_EXT_OUT5	U1-AW5	U2-AW5	U3-AW5	U4-AW5	2.5V	N
CLK_Fx_EXT_OUT6	U1-AV36	U2-AV36	U3-AV36	U4-AV36	2.5V	P
CLK_Fx_EXT_OUT7	U1-AW37	U2-AW37	U3-AW37	U4-AW37	2.5V	N
CLK_Fx_EXT_SEIN0	U1-AL36	U2-AL36	U3-AL36	U4-AL36	2.5V	P
CLK_Fx_EXT_SEIN1	U1-AL37	U2-AL37	U3-AL37	U4-AL37	2.5V	N
CLK_Fx_EXT_SEIN2	U1-AR38	U2-AR38	U3-AR38	U4-AR38	2.5V	P
CLK_Fx_EXT_SEIN3	U1-AP38	U2-AP38	U3-AP38	U4-AP38	2.5V	N
CLK_ISPCLK0_Fx_0	U1-R15	U2-R15	U3-R15	U4-R15	2.5V	P
CLK_ISPCLK0_Fx_1	U1-P15	U2-P15	U3-P15	U4-P15	2.5V	N
CLK_ISPCLK1_Fx_0	U1-K8	U2-K8	U3-K8	U4-K8	2.5V	P
CLK_ISPCLK1_Fx_1	U1-J7	U2-J7	U3-J7	U4-J7	2.5V	N
CLK_ISPCLK2_Fx_0	U1-A39	U2-A39	U3-A39	U4-A39	2.5V	P
CLK_ISPCLK2_Fx_1	U1-B38	U2-B38	U3-B38	U4-B38	2.5V	N
CLK_ISPCLK3_Fx_0	U1-N31	U2-N31	U3-N31	U4-N31	2.5V	P
CLK_ISPCLK3_Fx_1	U1-M32	U2-M32	U3-M32	U4-M32	2.5V	N
F(ABCD)_LCLK_OSC	U1-BB37	U2-BB37	U3-BB37	U4-BB37	2.5V	P

3.3.2. GPIO signals

GPIO									
Signal	FPGA A		FPGA B		FPGA C		FPGA D		note
	Pins	VCCO	Pins	VCCO	Pins	VCCO	Pins	VCCO	
Fx_GPIO1	U1-K19	VCC_A2	U2-M11	VCC_B3	U3-BB12	VCC_C5	U4-AE10	VCC_D6	LED1
Fx_GPIO2	U1-R17	VCC_A2	U2-C1	VCC_B3	U3-AL21	VCC_C5	U4-AG12	VCC_D6	
Fx_GPIO3	U1-P18	VCC_A2	U2-D2	VCC_B3	U3-AL20	VCC_C5	U4-AG11	VCC_D6	
Fx_GPIO4	U1-M18	VCC_A2	U2-P11	VCC_B3	U3-AU17	VCC_C5	U4-AF12	VCC_D6	
Fx_GPIO5	U1-M19	VCC_A2	U2-P12	VCC_B3	U3-AV16	VCC_C5	U4-AF11	VCC_D6	
Fx_GPIO6	U1-H29	VCC_A1	U2-K19	VCC_B2	U3-AM29	VCC_C4	U4-BB12	VCC_D5	LED2
Fx_GPIO7	U1-C35	VCC_A1	U2-R17	VCC_B2	U3-AL26	VCC_C4	U4-AL21	VCC_D5	
Fx_GPIO8	U1-B34	VCC_A1	U2-P18	VCC_B2	U3-AM27	VCC_C4	U4-AL20	VCC_D5	
Fx_GPIO9	U1-D35	VCC_A1	U2-M18	VCC_B2	U3-AK27	VCC_C4	U4-AU17	VCC_D5	
Fx_GPIO10	U1-E34	VCC_A1	U2-M19	VCC_B2	U3-AJ27	VCC_C4	U4-AV16	VCC_D5	

3.3.3. RESET and PLL LOCK

RESET and PLL_LOCK					
Signal	FPGA A	FPGA B	FPGA C	FPGA D	note
BRDPLL_LOCK	U1-AU7	U2-AU7	U3-AU7	U4-AU7	
RESET	U1-AU8	U2-AU8	U3-AU8	U4-AU8	

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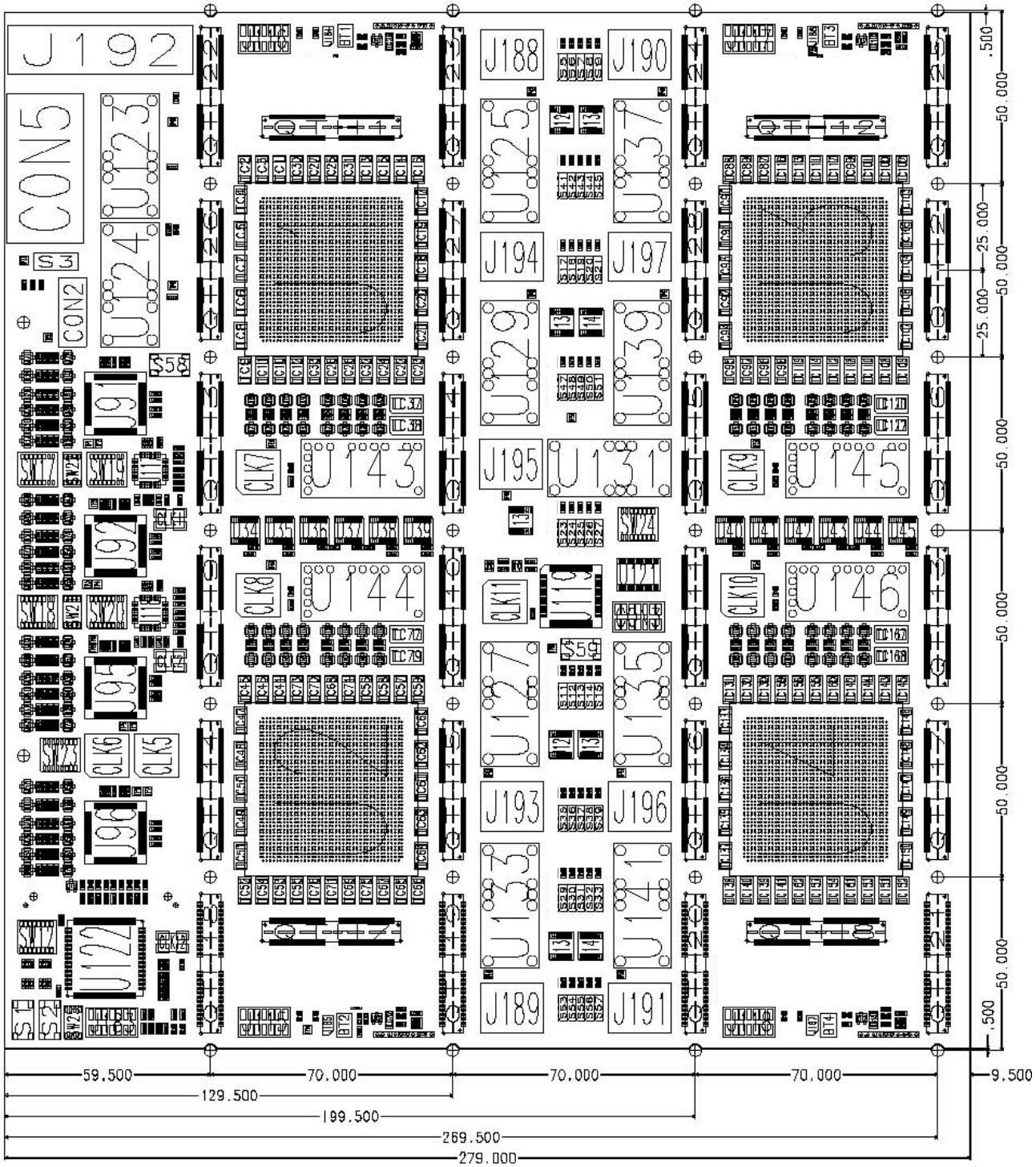
4. Dimension

4.1. Board Dimension



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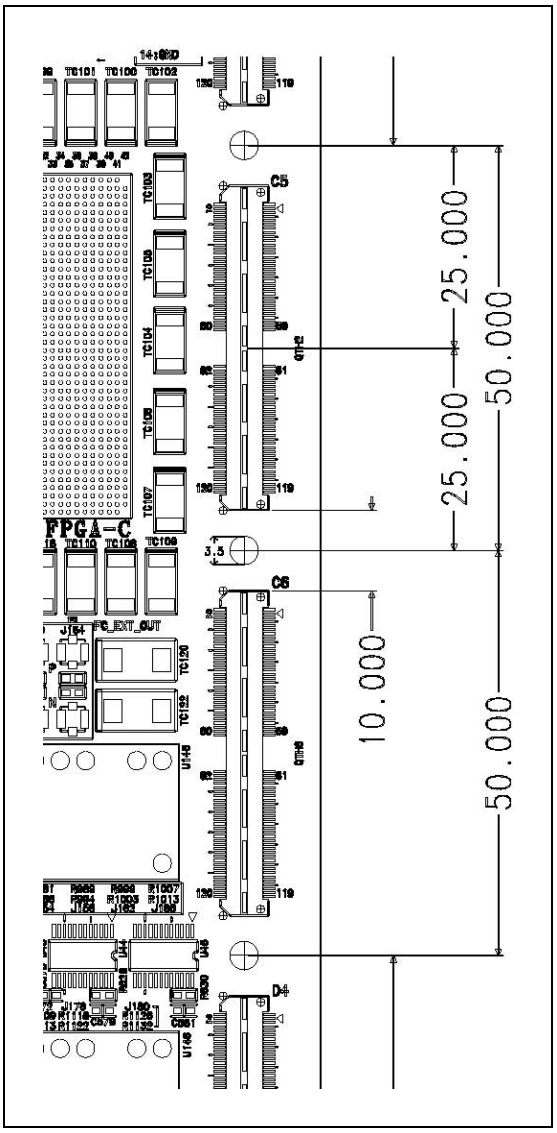
4.2. Detail Dimension of I/O Connector



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5. Configuration

For Configuring the Devices, the FPGA devices can be configured in several ways:

1. from Xilinx iMPACT via a JTAG cable
2. from a CompactFlash

The four LEDs, marked **DONE A**, **DONE B**, **DONE C**, and **DONE D**, indicate if the corresponding FPGA is configured or not. After a successful configuration, the **DONE** LEDs will change color from orange to green.

To configure FPGAs the Xilinx iMPACT tool is required. If you install Xilinx ISE, Xilinx iMPACT tool will be automatically installed.

To configure the FPGA through JTAG connector, USB Platform Cable is also required.

To configure the FPGA with SystemACE CompactFlash Solution, you need a CF-Memory Card. CF-Memory card should be formatted by a disk format utility, you can download it from http://www1.mager.org/mkdosfs/.

5.1. FPGA Configuration using JTAG connector

FPGA JTAG connector(J183) has two purposes.

(1) FPGA Configuration. You can configure FPGAs with *.bit files through JTAG connector, but FPGA configuration data will be lost after power off.

(2) FPGA internal logic debugging with ILA. The ILA is contained in the Xilinx ChipScope package.

Although FPGA configuration data will be lost after power off, because it is the most easy and fast way to configure a FPGA, JTAG is generally used to verify user design

This section explains FPGA configuration process using JTAG.

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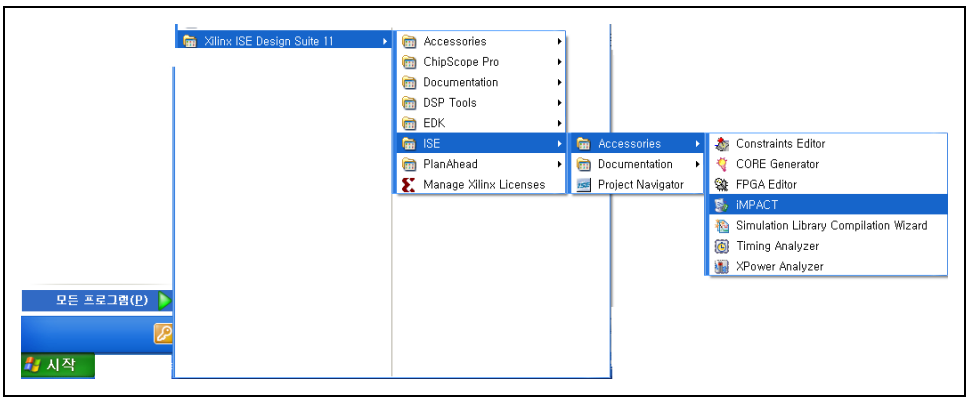
Step 1. Connect USB Platform Cable to the USB port of host computer and target board and target board MFP-LX760 Quad power on.

Step 2. Run Xilinx iMPACT and create a project file.

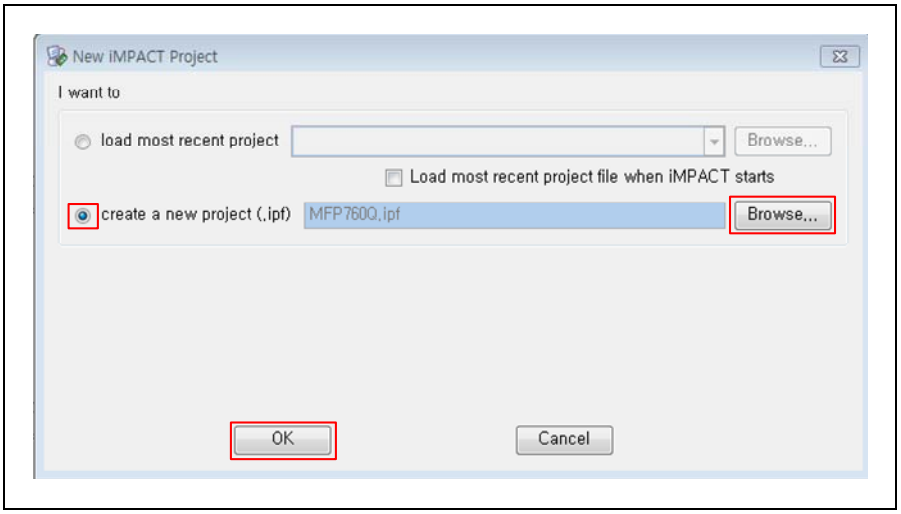
[Figure 5-1] shows where to run iMPACT. Select "Xilinx ISE Design Suite 11 ➜ISE ➜ Accessories ➜iMPACT" and click mouse left button.



[Figure 5-1] Xilinx iMPACT menu location

After running, iMPACT will ask to call a project file created previously or to create a new one.

Choose "create a new project(.ipf)" switch and browse a directory and make a file name to save project file. Commonly, project file is saved in the same directory where *.bit file is. Xilinx ISE will create a *.bit file after a sequence of Synthesis of source codes, Mapping, and P&R(Place and Route).



[Figure 5-2] iMPACT project window

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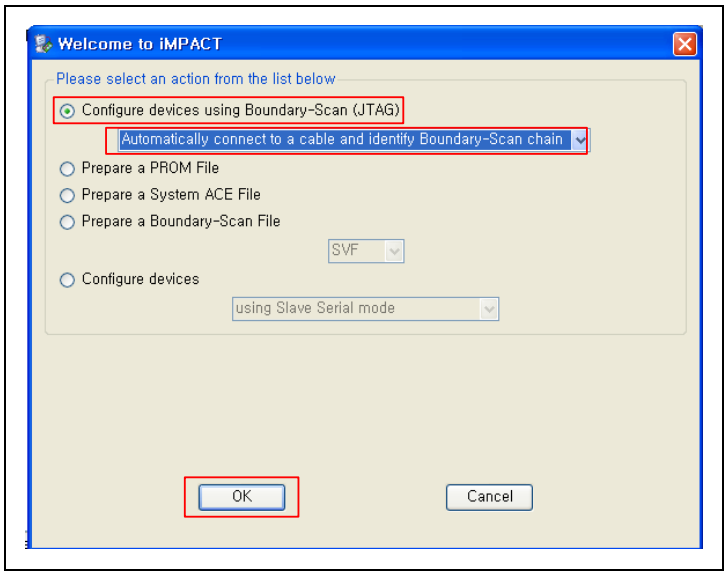
Step 3. Select JTAG configuration.

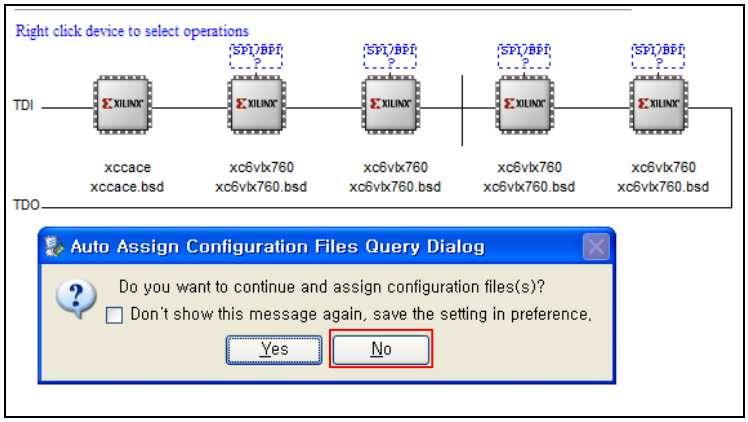
If you click "OK" button shown previous [Figure 5-2] iMPACT project window, a window will popped up to ask to select an action for configuration. Choose the first "Configure devices using Boundary-Scan" menu, and select "Automatically.." from submenu.



[Figure 5-3] Configuration method selection window

After the OK button click, following [Figure 5-4] show JTAG Chain of Virtex6 FPGAs and SystemACE.

Click "No" button, When the window pop up shown [Figure 5-4].



[Figure 5-4] MFP-LX760-Q board JTAG Scan

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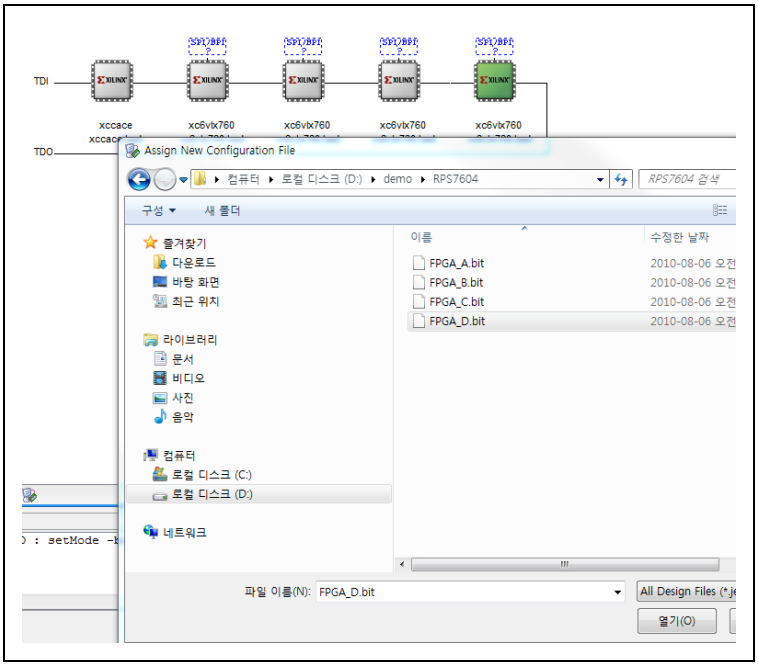
Step 4. Assign bit files to every FPGAs.

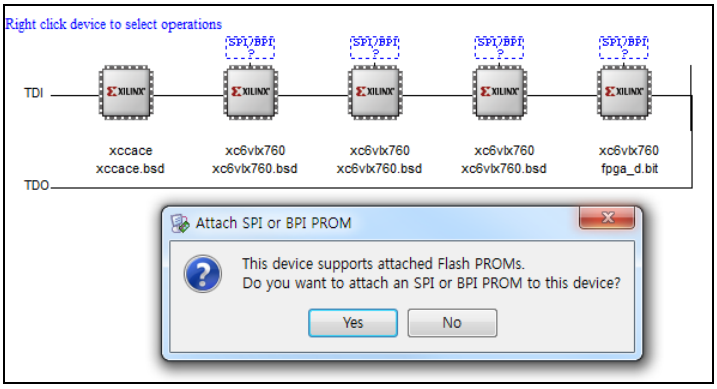
A submenu will be popped up, when you click right button after place mouse curser on a XC6LVX760 device in JTAG Chain. Select "Assign New Configuration File" and assign a *.bit file. Devices order is (left) XCCACE, FPGA A, FPGA B, FPGA C, FPGA D (right).



[Figure 5-5] Assigning bit files

Step 5. Programming FPGA configuration files(*.bit).

Move mouse curser on the FPGA and click right button. Then select "Program" on the popped up submenu. Click "OK" when "Device Programming Properties..." window is appeared to start FPGA configuration.



[Figure 5-6] FPGA configuration sequence

Click "No", when [Figure 5-6] Window show. If the FPGA configuration is successful, FPGA_DONE LED on the MFP-LX760-Q will light.

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5.2. FPGA Configuration using CF-Memory (SystemACE)

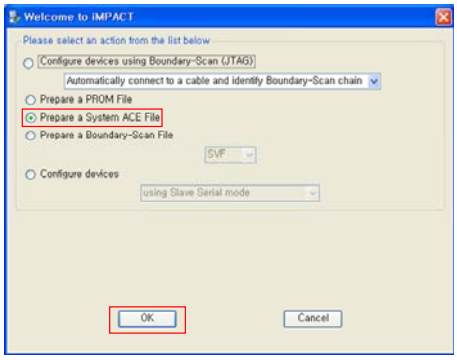
This section gives an explanation how to configure FPGAs with SystemACE and CF-Memory. To use a CF-Memory, it should be formatted by disk formatting utility such as mkdosfs, available from http://www1.mager.org/mkdosfs. System-ACE Controller Device plays a role in FPGA configuration on JTAG Chain by reading data from CF-Memory. Because CF-Memory is non-volatile memory device, it can keep data after power off.

Step 1. Run Xilinx iMPACT and create a project file.

As shown on [Figure 5-2], select iMPACT menu from "Xilinx ISE Design Suite 11 ➜ISE ➜ Accessories ➜iMPACT" and click mouse left button.

Step 2. Convert configuration file(*.bit) into SystemACE file.

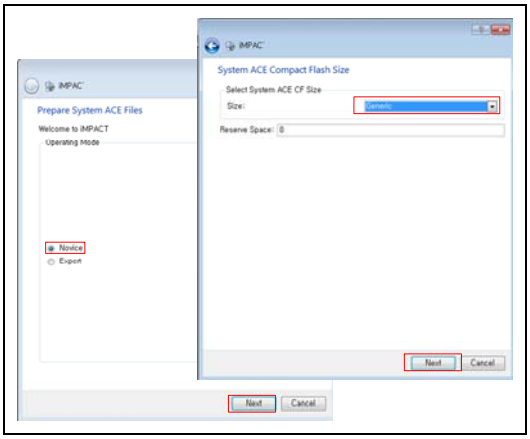
As shown on [Figure 5-7], choose "Prepare a System ACE File" switch and click "OK".



[Figure 5-7] Select an action of System ACE file creation

Step 3. Select CF memory option.

As shown on [Figure 5-8], choose "Novice" then click Next button and select "Generic" from "Select System ACE CF Size" then click Next button.



[Figure 5-8] System ACE File creation option

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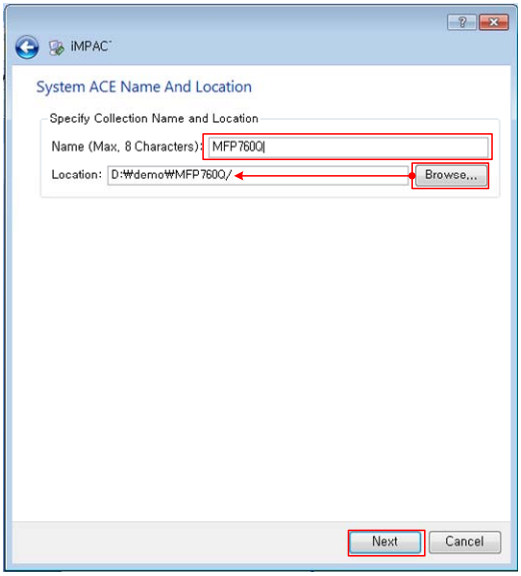
Step 4. Assign System ACE file name and directory.

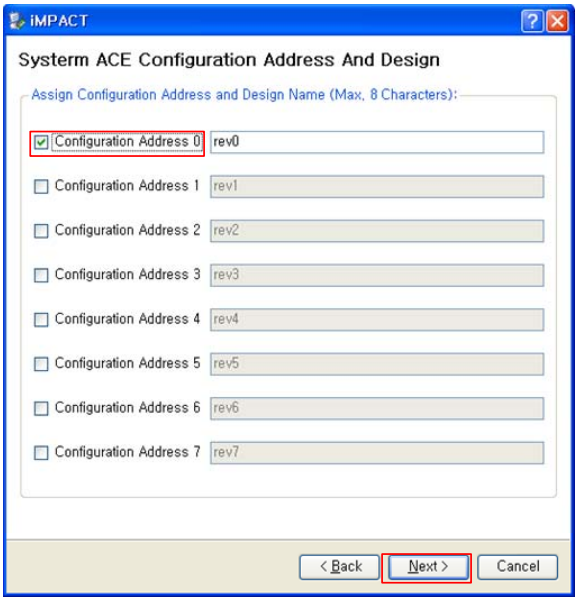
As shown on [Figure 5-9], write file name and click "Browse..." button to select directory where to save System ACE file. Click "Next" button.



[Figure 5-9] Assign file name and directory

Step 5. System ACE file Revision.

[Figure 5-10] shows a window where to select System ACE file address and its revision. System ACE controller can load 8 kind of different configuration data from CF-Memory. There is a DIP switch to select configuration data on the MFP-LX760-Q board.



[Figure 5-10] System ACE file Revision selection window

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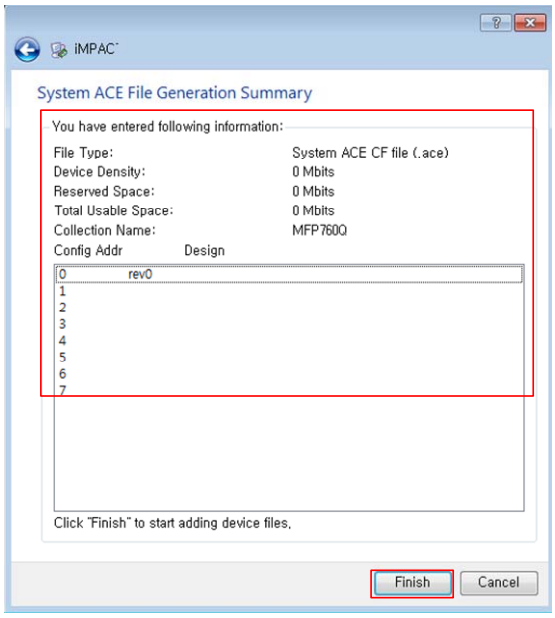
Step 6. Confirm SystemACE option.

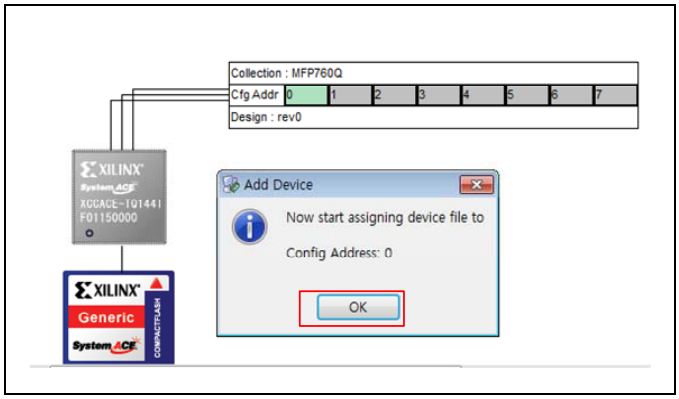
[Figure 5-11] window shows information what you have chosen. Confirm it and click "Finish".



[Figure 5-11] System ACE file generation confirmation window

Step 7. Assign bit file.

You can see "Config Address: 0" in [Figure 5-12]. That means you have chosen address 0 to store configuration data at step 5.



[Figure 5-12] Confirm System ACE address

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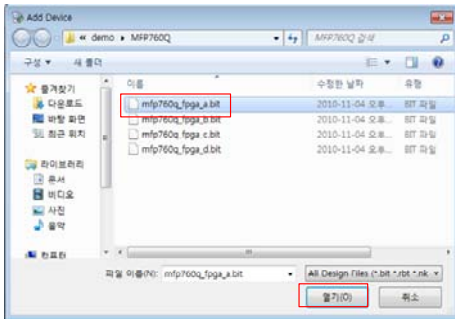
Step 8. Select a file.

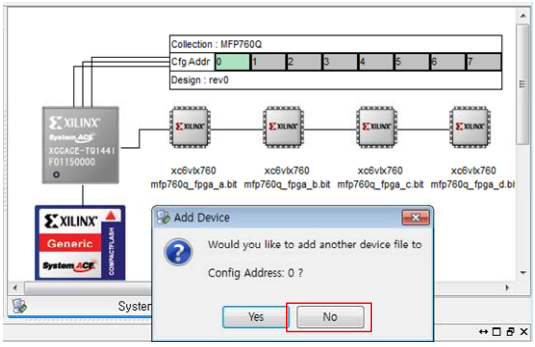
After clicking "OK" at previous step, you can see following window. Select bit file and clip "open" button.



[Figure 5-13] Configuration file selection window

Step 9. Select another configuration data.

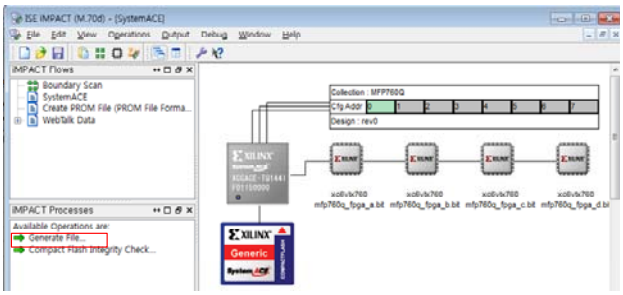
If you have more configuration data file, click "Yes" of click "No" on the following [Figure 5-14] window.



[Figure 5-14] FPGA addition window

Step 10. Create System ACE file.

Select "iMPACT Processes" tap on left bottom of iMPACT window. Double click "Generate File…" menu then System ACE file will be created.



[Figure 5-15] System ACE file creation

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Step 11. Copy System-ACE files into CF-Memory.

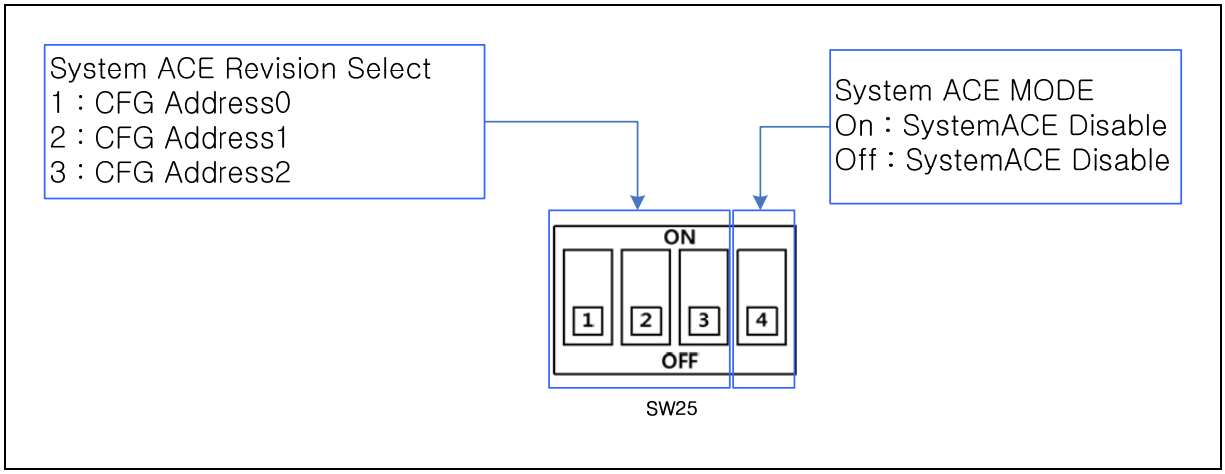
Insert CF memory into CF memory writer. Copy System-ACE files into CF-memory.

Step 12. Insert CF memory into MFP-LX760-Q CF memory slot and power on.

If all of DIP Switch (SW24) switch are OFF, "JTAG chain" includes all FPGAs.

SWNUM	Function	Note
1	FPGA A enable	'1': Configure JTAG Chain without FPGA A
2	FPGA B enable	'1': Configure JTAG Chain without FPGA B
3	FPGA C enable	'1': Configure JTAG Chain without FPGA C
4	FPGA D enable	'1': Configure JTAG Chain without FPGA D
5	RESET MODE	'0': RESET Switch(S1) directly connect to FPGA reset
6	HOTSWAP	'0': When configuration, all I/Os of FPGA is 'Z' '1': When configuration, all I/Os of FPGA is 'High'
7	Reserved	
8	Reserved	

If number 4 switch of DIP switch(SW25) is OFF, System ACE will run. If number 1, 2, 3 switches are OFF, System ACE controller will load Revision 0 configuration data.



[Figure 5-16] DIP switch setting

If you want re-configure FPGAs under power-on state, push SystemACE Push Button on [Figure 5-16]. The LED at the right of SystemACE Push Button will twinkle before FPGA configuration complete. After FPGA configuration the LED will light green or light red if configuration failed by any reason.

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6. FPGA PIN TEST

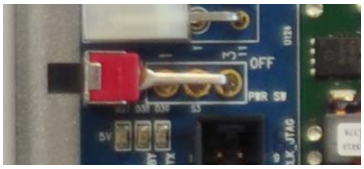
6.1. FPGA to FPGA Connection Test

6.1.1. Description

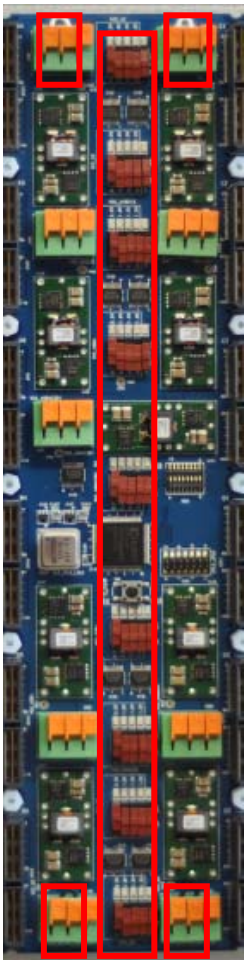
Check "FPGA to FPGA" connection status of MFP-LX760-Q board.

6.1.2. Procedure

(1) Turn of the board. (PWR SW up)



(2) Set all VCCO Selection switch to 2.5V.
Check VCC_A1, VCC_B3, VCC_C4, VCC_D6 .



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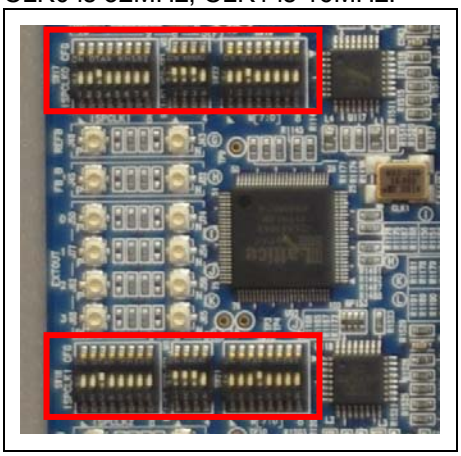
(3) Set Clock Generator
CLK0 is 32MHz, CLK1 is 16MHz.



CLK0	***CLK1***
Set 32MHz	Set 16MHz

SW17

1	2	3	4	5	6	7	8
off	off	on	off	off	off	off	Off

SW18

1	2	3	4	5	6	7	8
off	off	on	off	off	off	off	Off

SW22

1	2	3	4
on	on	on	off

SW21

1	2	3	4
on	on	on	off

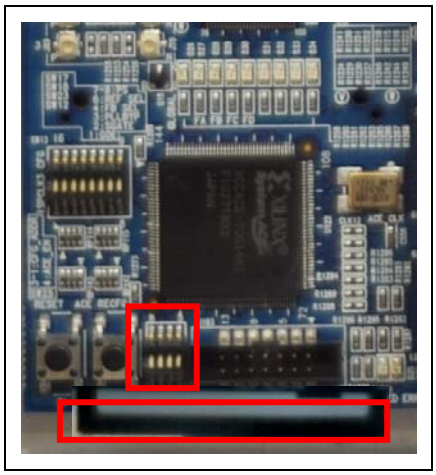
SW19

1	2	3	4	5	6	7	8
off	off	on	off	off	off	off	Off

SW20

1	2	3	4	5	6	7	8
off	off	off	on	off	off	off	Off

(4) Insert CF card after copy the board test image (ACE File at CD(MFP760_test folder)).
And Check SystemACE mode Switch(SW25)



SW25

1	2	3	4
off	off	off	off

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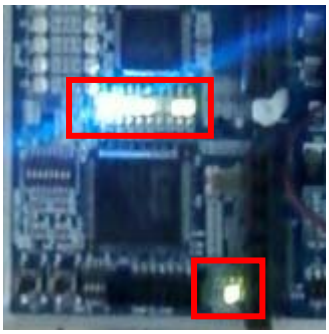
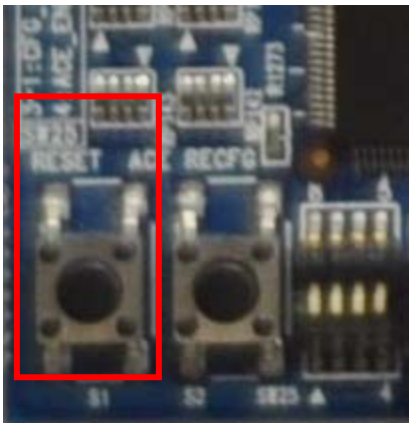
(5) Turn on the board.(Pwr SW, left side of board)

(6) Confirm the FPGAs configuration status.



SYSTEM ACE STATUS	*CONFIGURATION STATUS*
STATE LED(D35) : on ERR LED(D36) : off	GLOBAL LED(D26) : on(ALL FPGAs Config Done) FA(D28) : on(FPGA A Config. DONE) FB(D29) : on(FPGA B Config. DONE) FC(D30) : on(FPGA C Config. DONE) FD(D31) : on(FPGA D Config. DONE)

(7) Push the reset button(S1, left side on the board) after all FPGAs configuration done.



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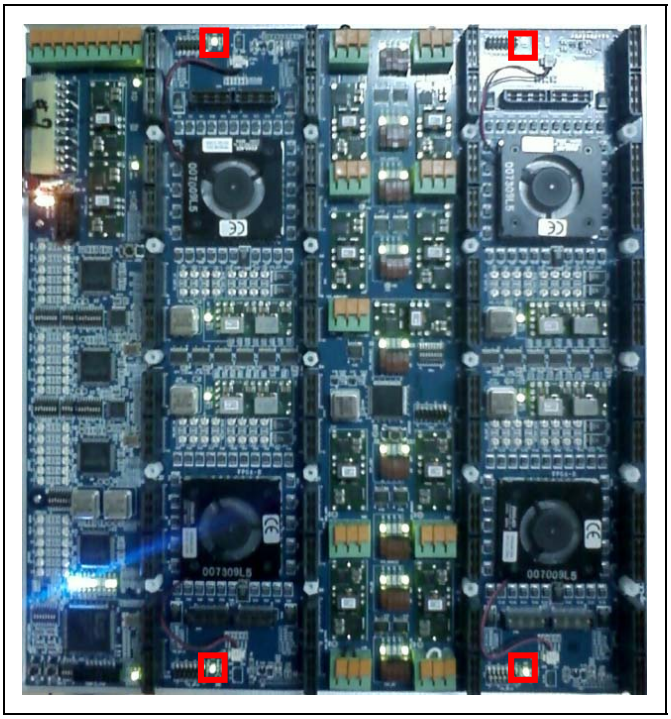
(8) Check GPIO1 LED of each FPGA.
If all LEDs are "on", FPGA to FPGA interconnections are OK.



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