120405

1. draft 0.1 release

120406

1. GTX 추가

120418

1. GTX 수정(xillinx 김홍철 부장 감수)
2. UART 1.8V 로 수정
3. Off-page connector 맞춰서 DRC error clear
4. AB7, CD7을 A7, B7, C7, D7으로 분리
5. Samtec connector 120번 NC 저항 처리

120423

1. Power 수정
 - track 핀에 RC-charge circuit 추가하여 CORE-AUX-IO로 순차 회로 추가
 - Turbo Trans open처리
2. samtec 커넥터 H1, H2, H7, H8에 연결된 전원이 Bottom에서 올라오지 않도록 NC 저항을 넣어서 차단함.

120425

1. UART enable/disable 설정 스위치 제거
2. VTT selector 추가

120502

1. DRC check and clear errors
2. GTX 저항 제거

120504

1. PTH08T240 Smart Sync 핀 GND 처리
2. Power Modual CAP datasheet 에 있는 부품으로 수정

120510

1. COIN BATT 회로 수정(AUX_1.8 diode 안거치고 VBATT으로 들어가도록)

120522

1. COIN BATT 전원 저항 안 거치고 바로 전원으로 들어가도록 회로 수정
2. VDD_GTX_1V8, VDD_GTX_AB_1V0, VDD_GTX_CD_1V0 전원 0옴 저항(6432사이즈)으로 분리 (GTX 문제 있으면 전원 차단용)
3. GLOBAL_DONE 3.3V to 1.8V 전압 분배 저항 추가.
4. nSYSRESET을 nSYSRESET과 nSYSRESET_1V8로 구분
(nSYSRESET_1V8는 분배저항 추가.)

120523

1. bank 0 전원 3.3V default에서 1.8V default로 수정
2. bank 0 신호 level shifter로 3.3V to 1.8V 구성
3. GLOBAL_DONE, nSYSRESET 신호 level shifter 추가
4. GTX Clock open된 입력 cap-resistor 추가
5. VRN, VRP 저항 47옴 -> 90옴(Virtex7 에서 방식 변경)

120529

1. D3_B50 ' D3_B48로 수정(로그서킷)
2. FA의 D14/19번핀 P/N 바뀌어 있어 SWAP(로그서킷)

120531

1. Clock generator IO 6, 7, 8번 전원 2.5V 사용할 수 있도록 수정
2. REFVTT, FBKVTT 설정 스위치 및 저항 추가

120601(V079)

1. REFVTT, FBKVTT 설정 핀 NET name 추가

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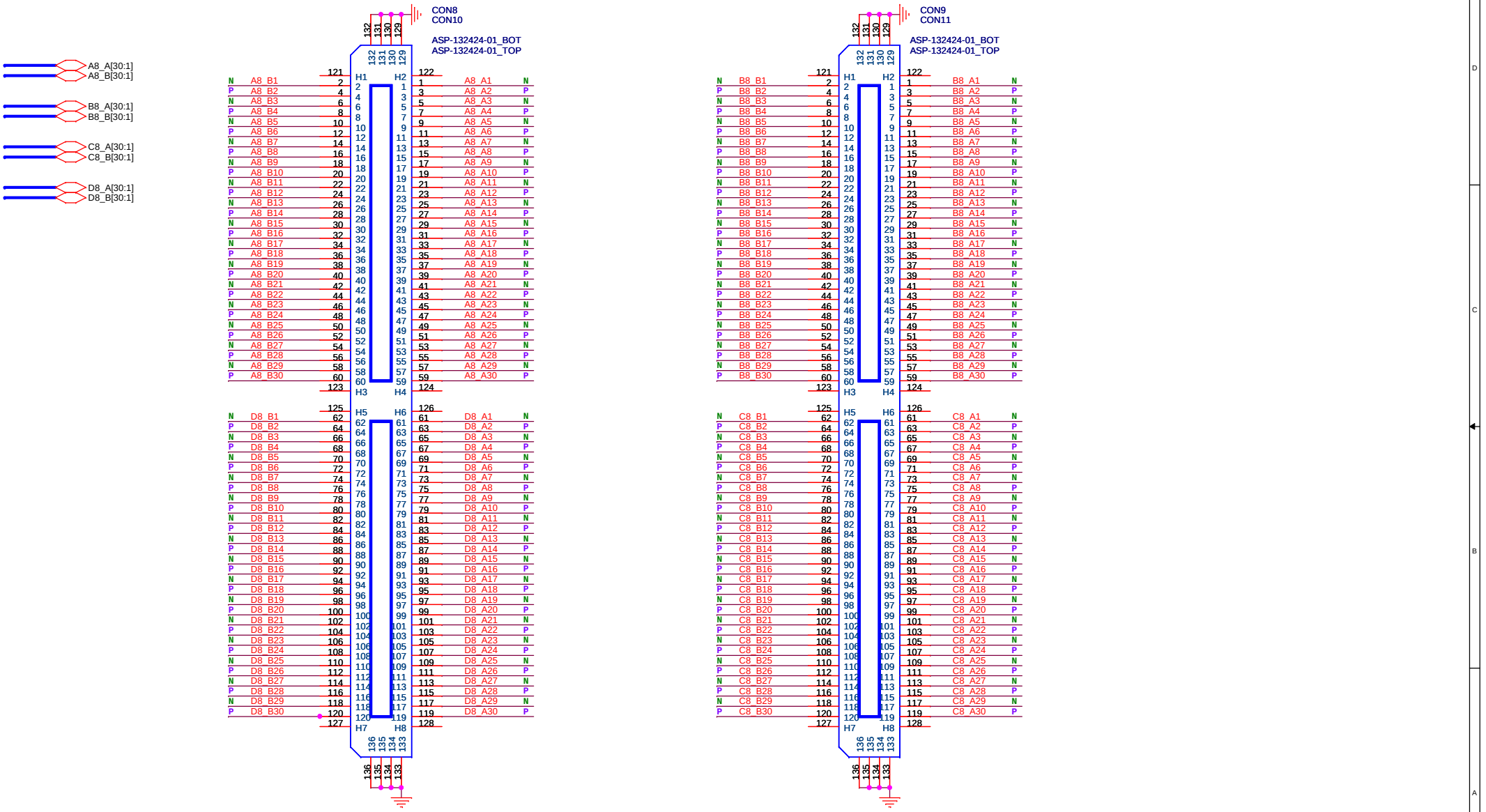

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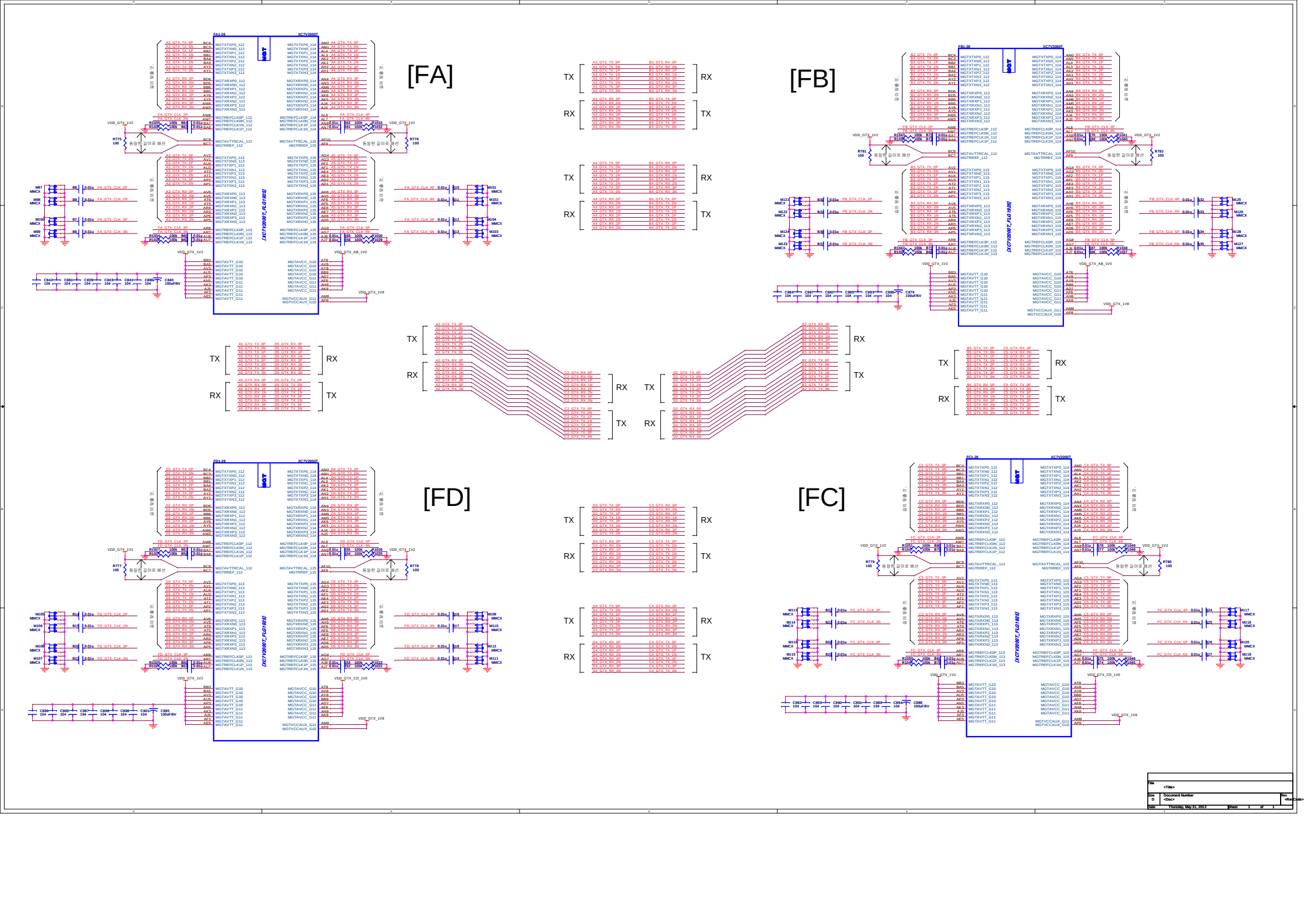
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[FC]
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TX
RX
FA1-26
FB1-26
FC1-26
FD1-26
XCTV2000T
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[XCTV2000T_FLG1926]
VDD_GTX_1V2
VDD_GTX_AB_1V0
VDD_GTX_CD_1V0
VDD_GTX_1V8
동일한 길이로 배선
FA_GTX_CLK_2P
FA_GTX_CLK_2N
FA_GTX_CLK_3P
FA_GTX_CLK_3N
FA_GTX_CLK_4P
FA_GTX_CLK_4N
FA_GTX_CLK_5P
FA_GTX_CLK_5N
FB_GTX_CLK_2P
FB_GTX_CLK_2N
FB_GTX_CLK_3P
FB_GTX_CLK_3N
FB_GTX_CLK_4P
FB_GTX_CLK_4N
FB_GTX_CLK_5P
FB_GTX_CLK_5N
FC_GTX_CLK_2P
FC_GTX_CLK_2N
FC_GTX_CLK_3P
FC_GTX_CLK_3N
FC_GTX_CLK_4P
FC_GTX_CLK_4N
FC_GTX_CLK_5P
FC_GTX_CLK_5N
FD_GTX_CLK_2P
FD_GTX_CLK_2N
FD_GTX_CLK_3P
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MMCX
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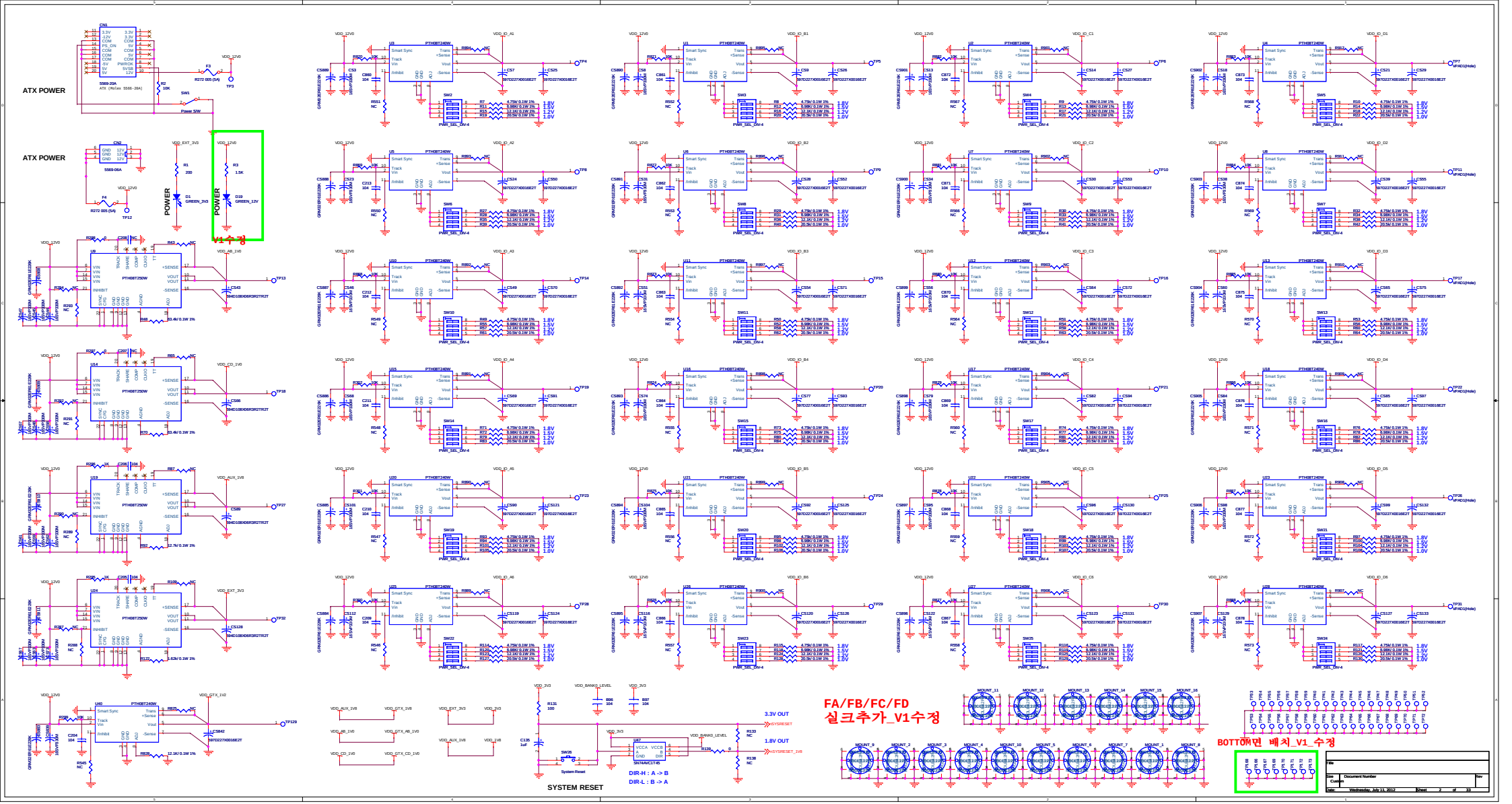
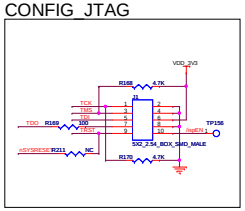
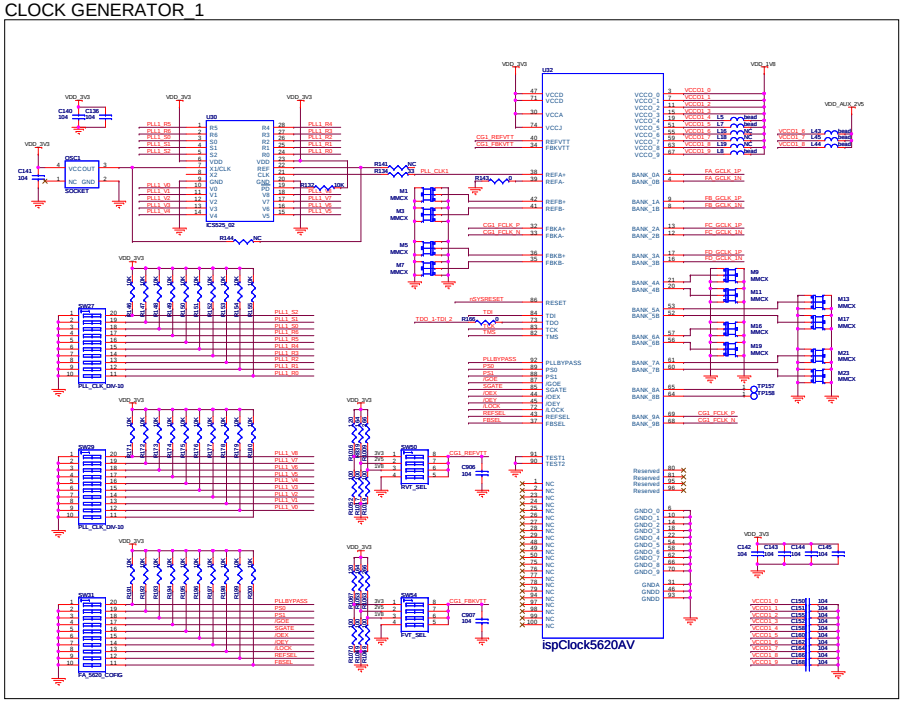

ATX POWER
ATX POWER
POWER
POWER
V1수정
FA/FB/FC/FD
실크추가_V1수정
BOTTOM면 배치_V1 수정
SYSTEM RESET
3.3V OUT
1.8V OUT
DIR-H : A -> B
DIR-L : B -> A

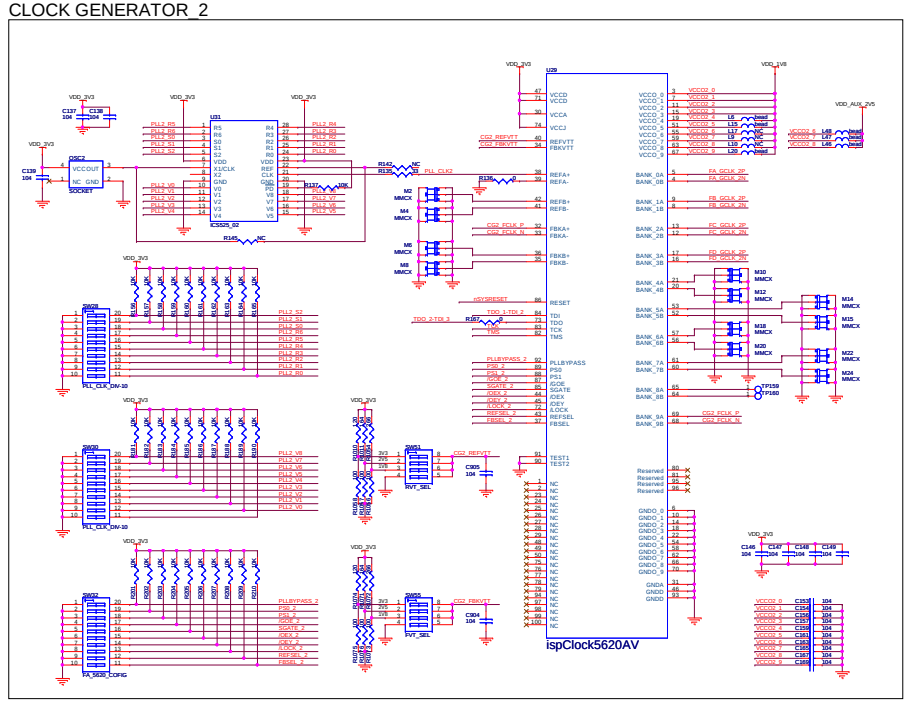
CONFIG_JTAG



CLOCK GENERATOR_1



CLOCK GENERATOR_2



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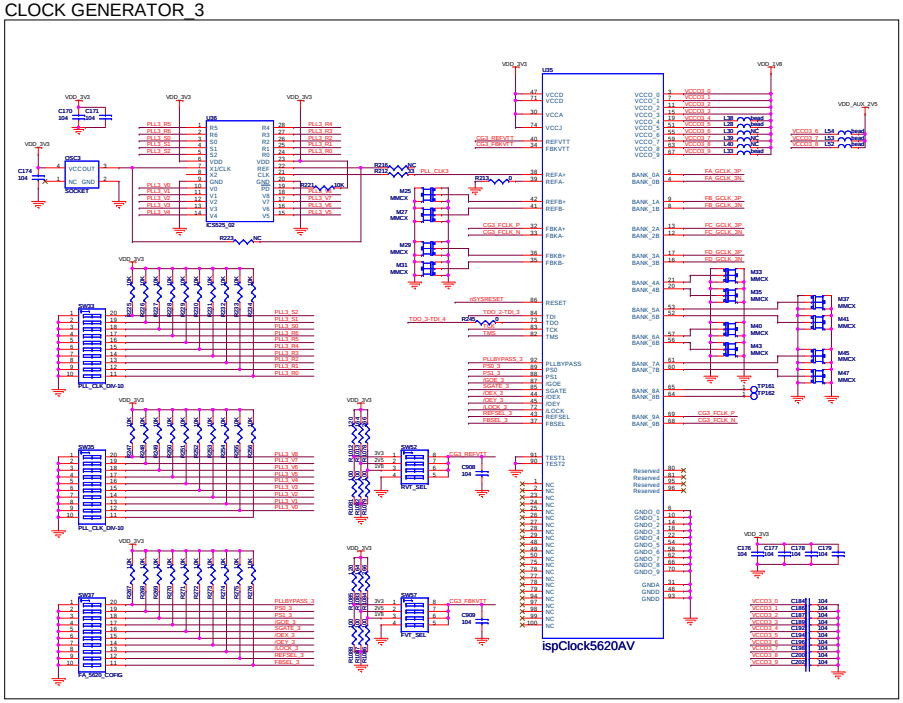
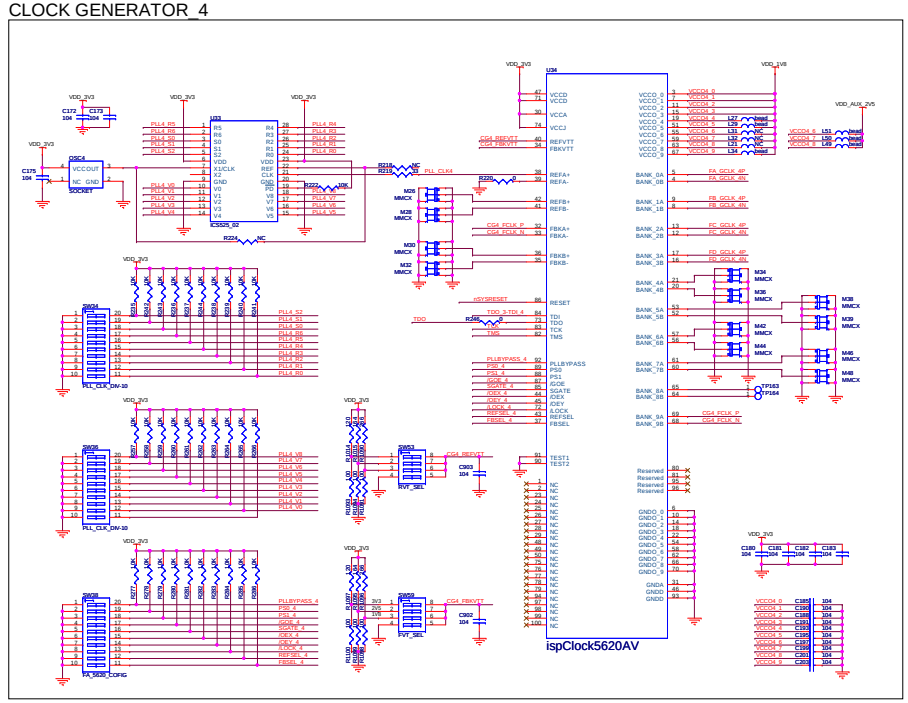


CLOCK GENERATOR_4



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FA_UART1_TX
FB_UART1_RX
FB_UART1_TX
FC_UART1_RX
FC_UART1_TX
FD_UART1_RX
FD_UART1_TX
FA_UART2_RX
FA_UART2_TX
FB_UART2_RX
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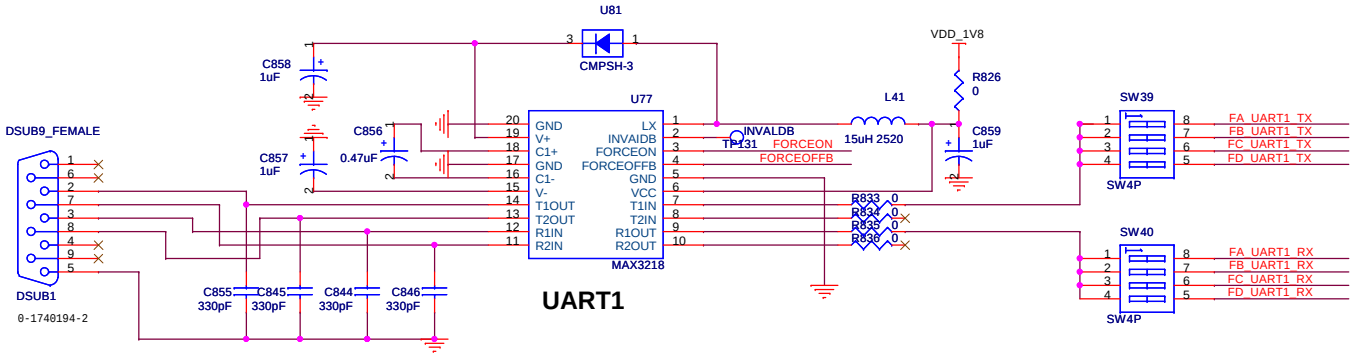
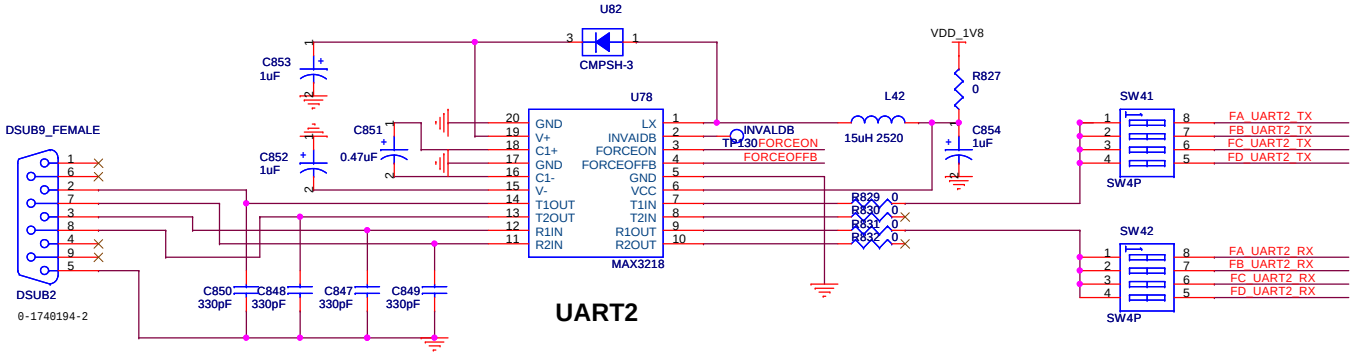
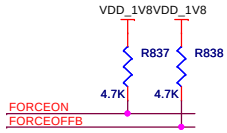
FC_UART2_RX
FC_UART2_TX
FD_UART2_RX
FD_UART2_TX







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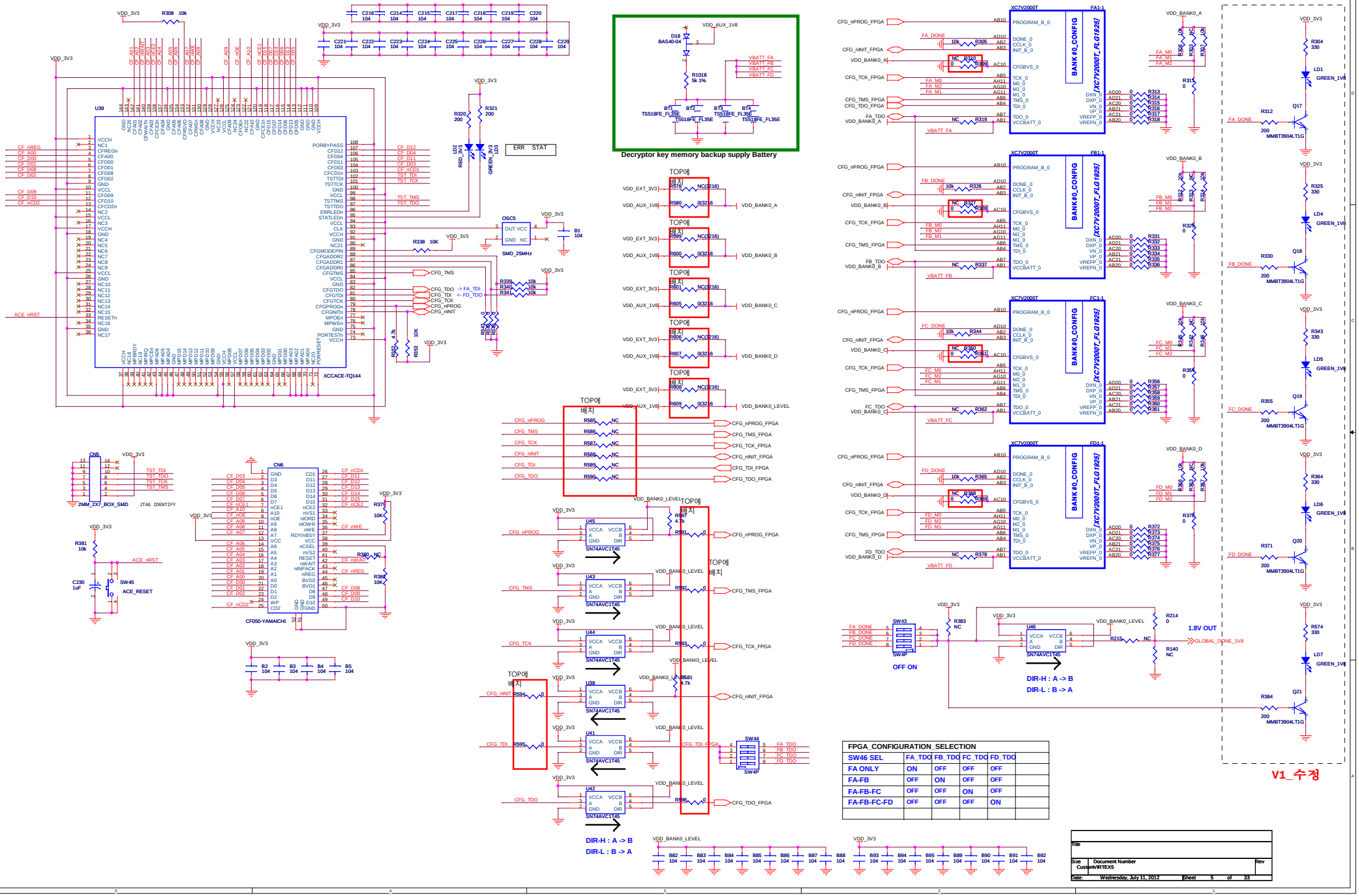

FPGA_CONFIGURATION_SELECTION				
SW46 SEL	FA_TDO	FB_TDO	FC_TDO	FD_TDO
FA ONLY	ON	OFF	OFF	OFF
FA-FB	OFF	ON	OFF	OFF
FA-FB-FC	OFF	OFF	ON	OFF
FA-FB-FC-FD	OFF	OFF	OFF	ON

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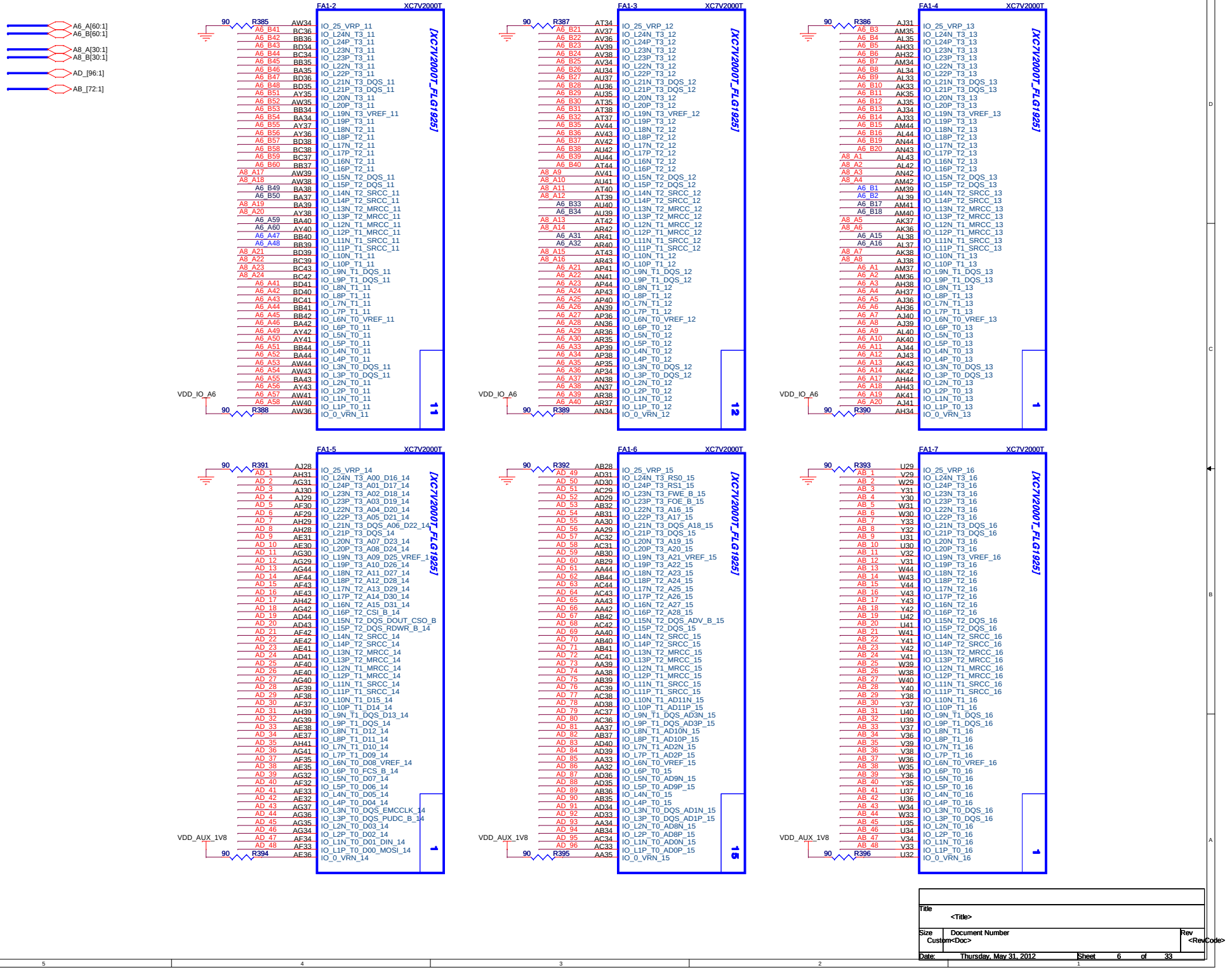
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A6_B[60:1]
A8_A[30:1]
A8_B[30:1]
AD_[96:1]
AB_[72:1]
FA1-2
XC7V2000T
[XC7V2000T_FLG1925]
VDD_IO_A6
VDD_AUX_1V8
FA1-3
FA1-4
FA1-5
FA1-6
FA1-7
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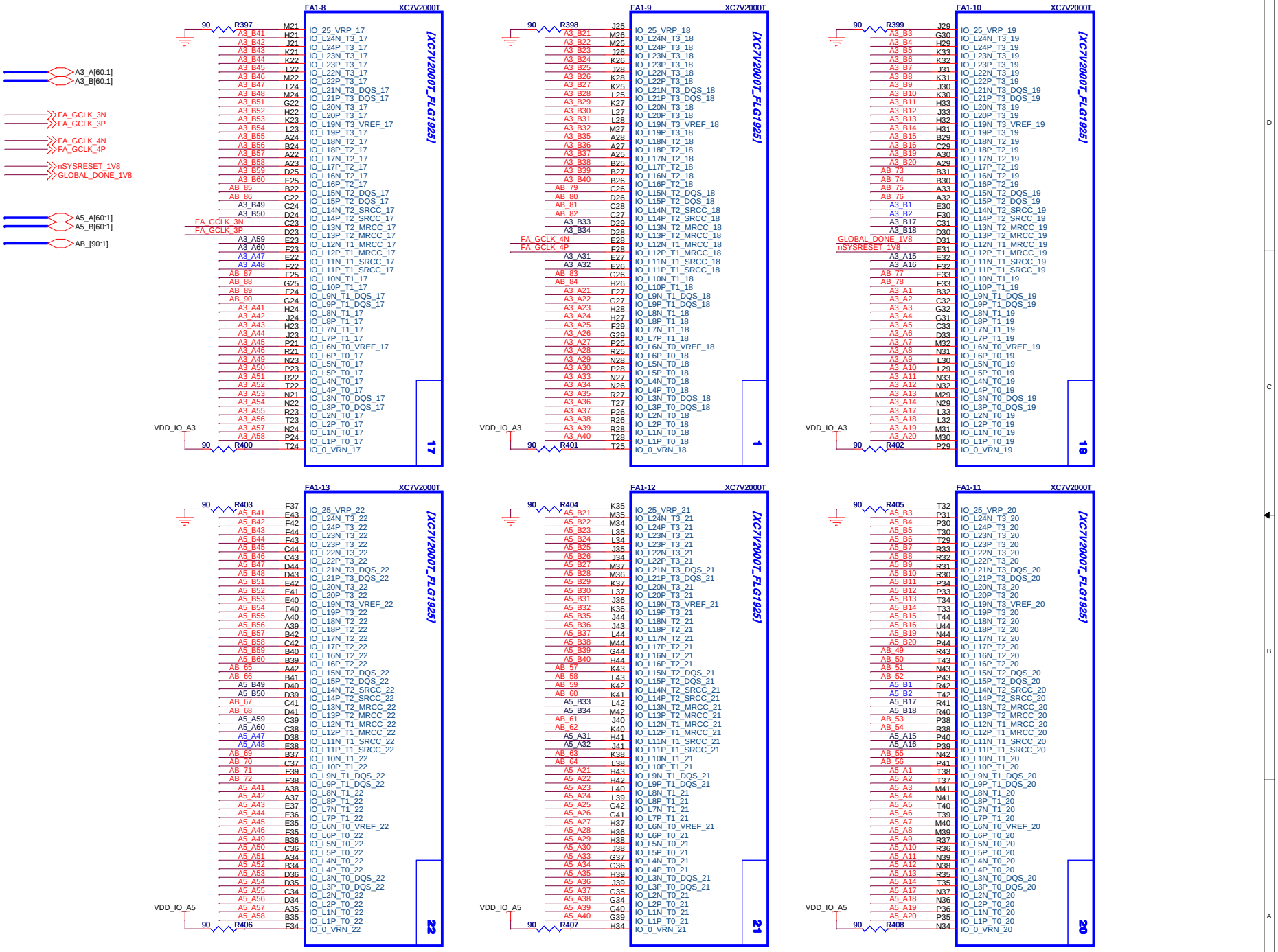

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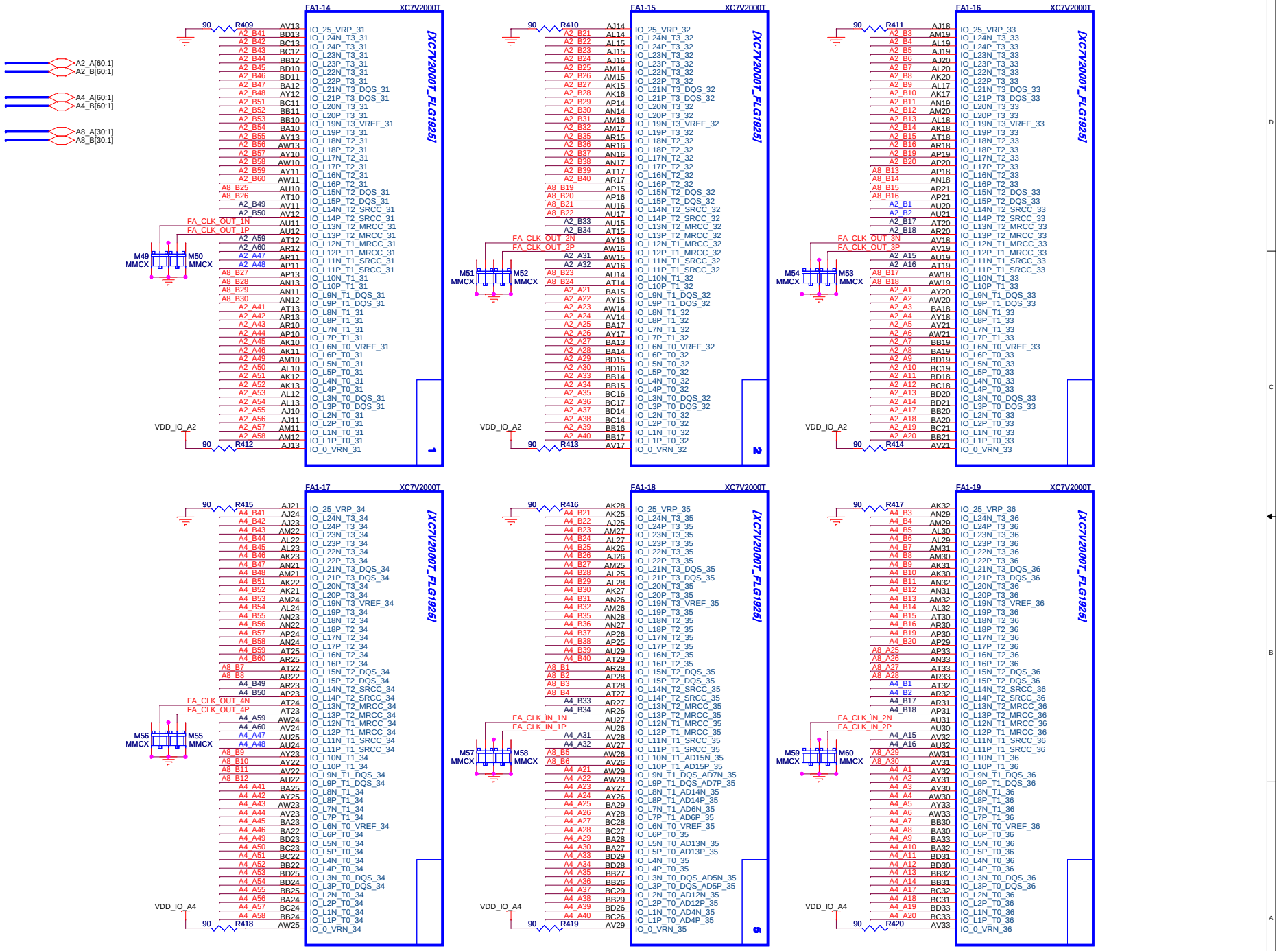

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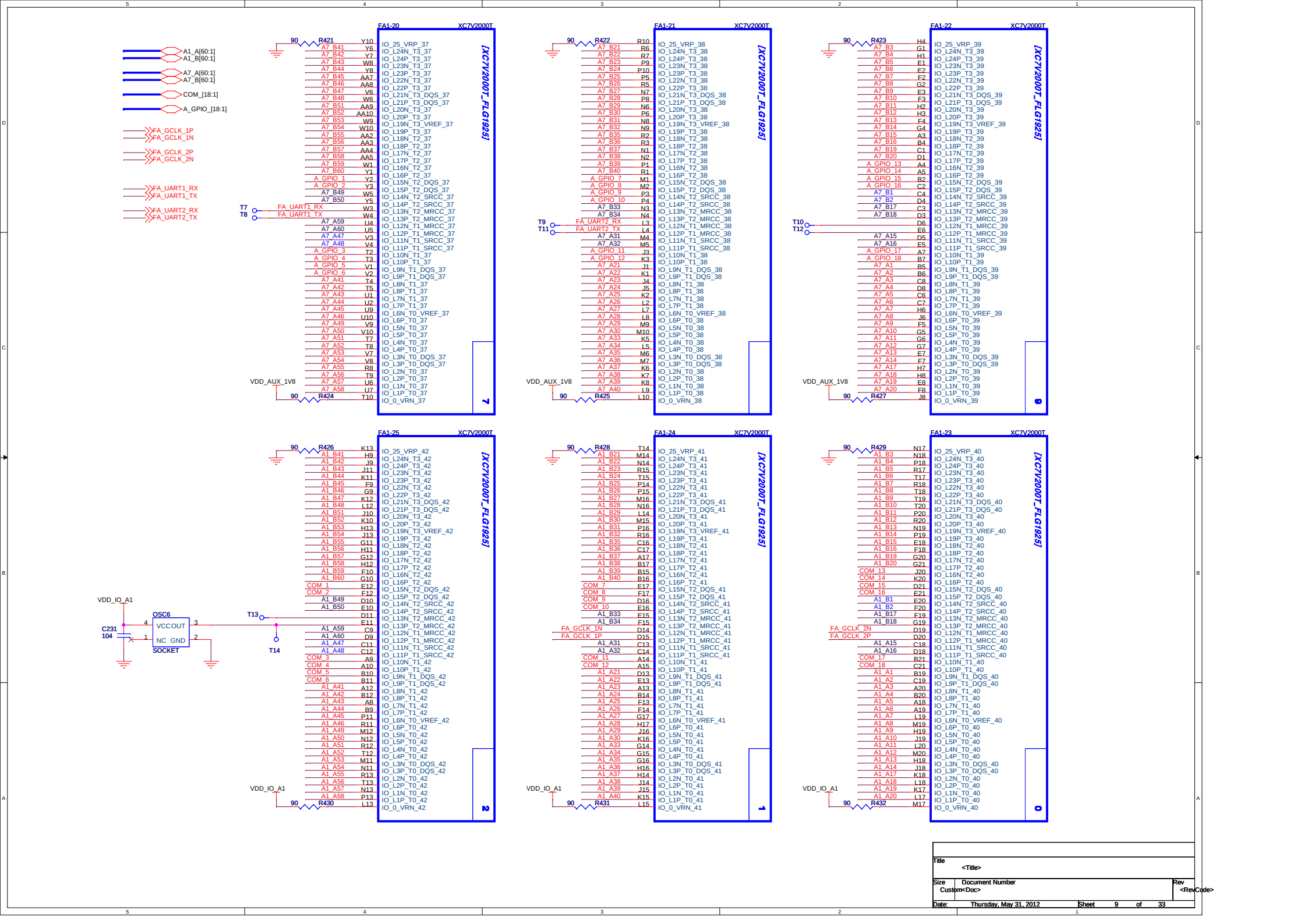
A1_A[60:1]
A1_B[60:1]
A7_A[60:1]
A7_B[60:1]
COM_[18:1]
A_GPIO_[18:1]
FA_GCLK_1P
FA_GCLK_1N
FA_GCLK_2P
FA_GCLK_2N
FA_UART1_RX
FA_UART1_TX
FA_UART2_RX
FA_UART2_TX
FA1-20 XC7V2000T
FA1-21 XC7V2000T
FA1-22 XC7V2000T
FA1-25 XC7V2000T
FA1-24 XC7V2000T
FA1-23 XC7V2000T
[XC7V2000T_FLG1925]
R421
R422
R423
R424
R425
R426
R427
R428
R429
R430
R431
R432
VDD_AUX_1V8
VDD_IO_A1
OSC6
VCCOUT
NC GND
SOCKET
C231
104
T7
T8
T9
T10
T11
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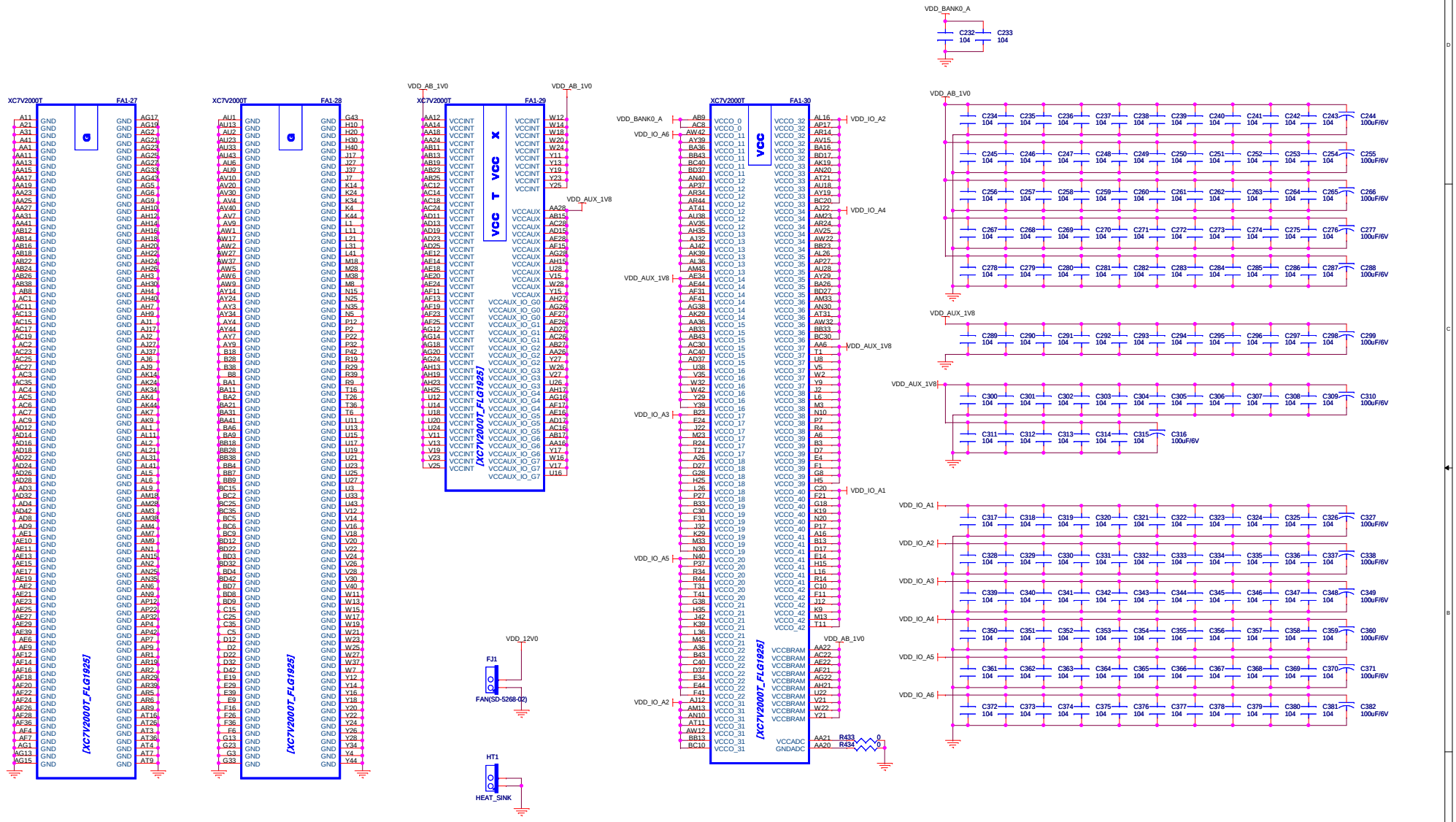

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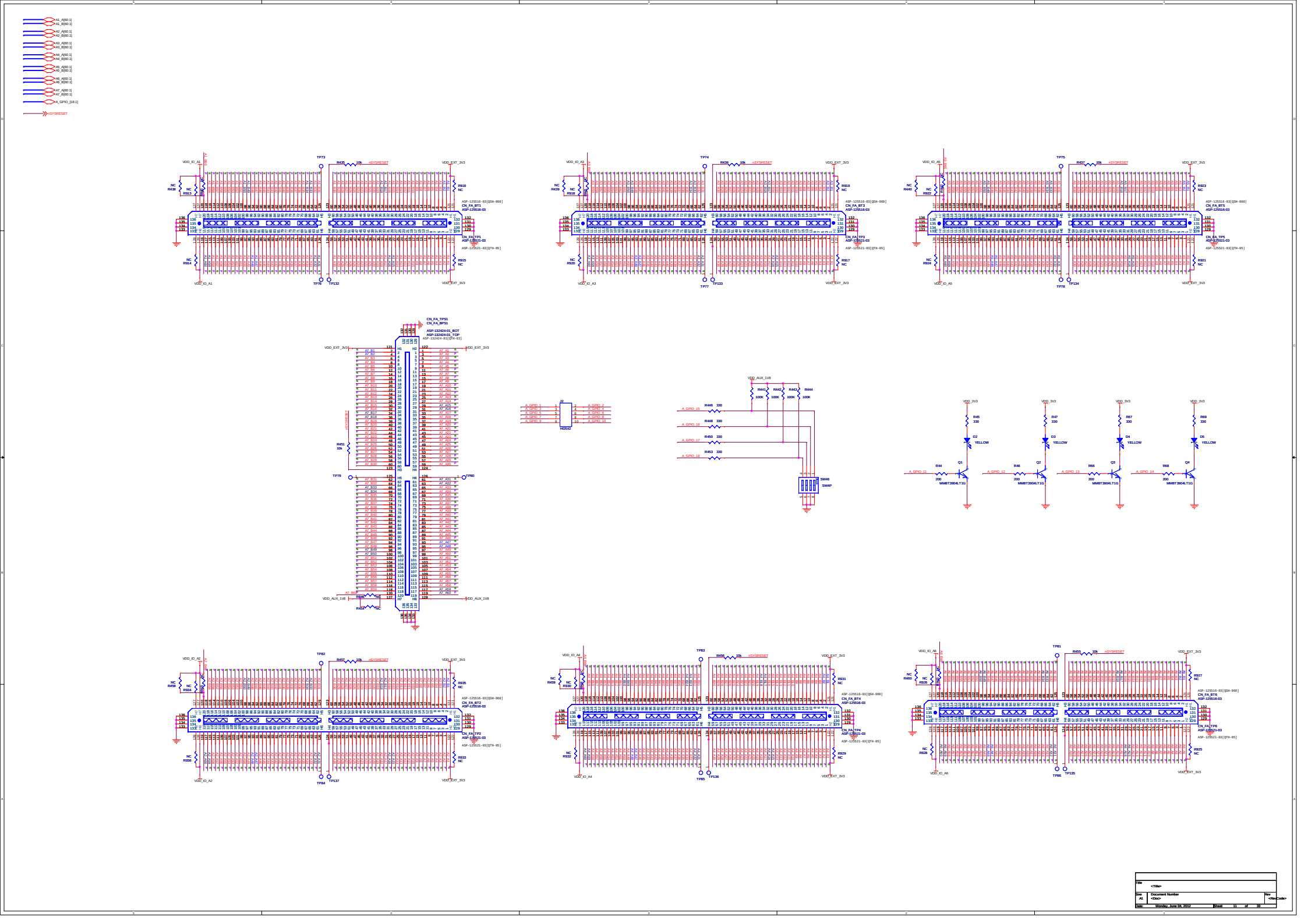

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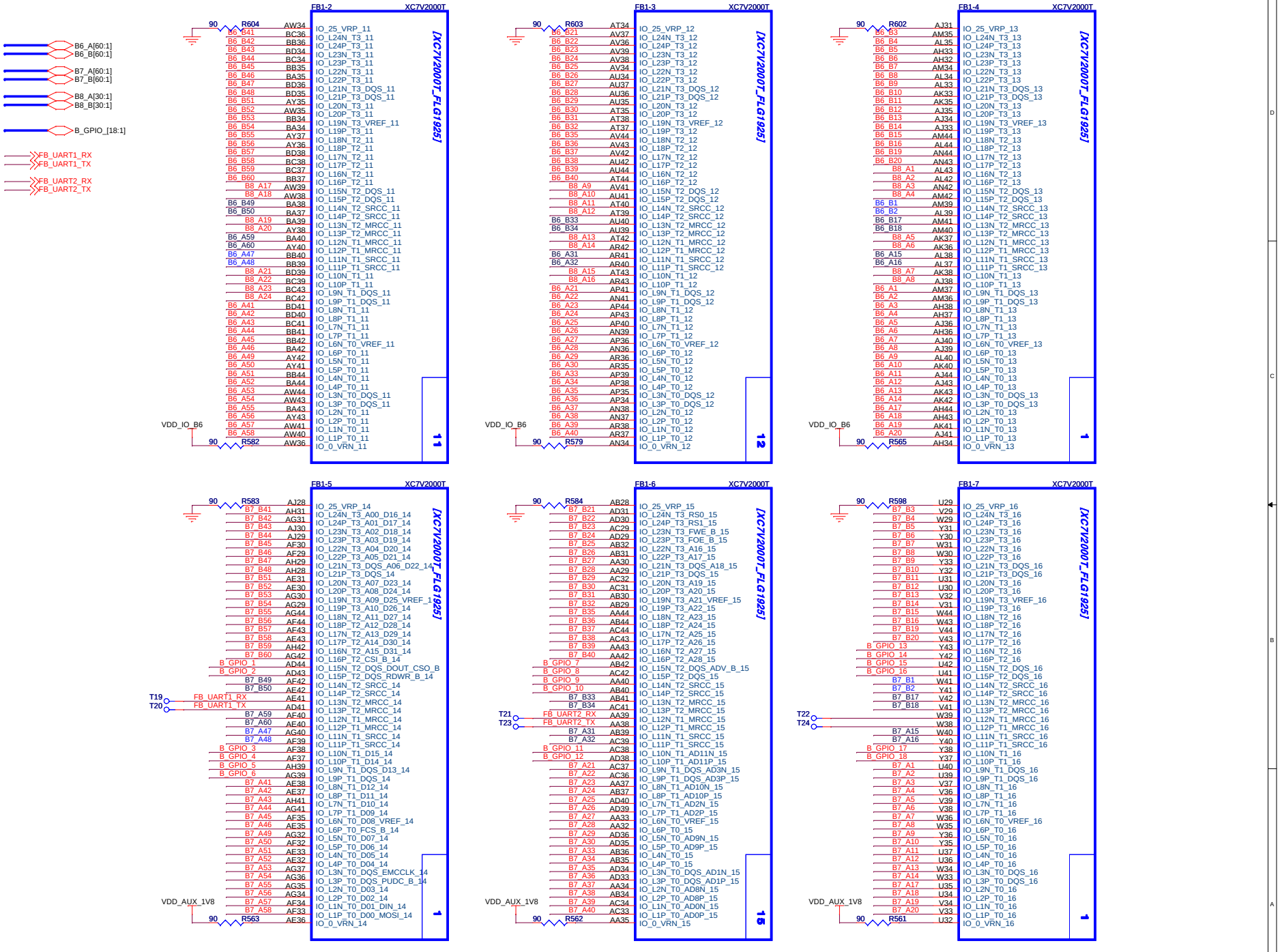

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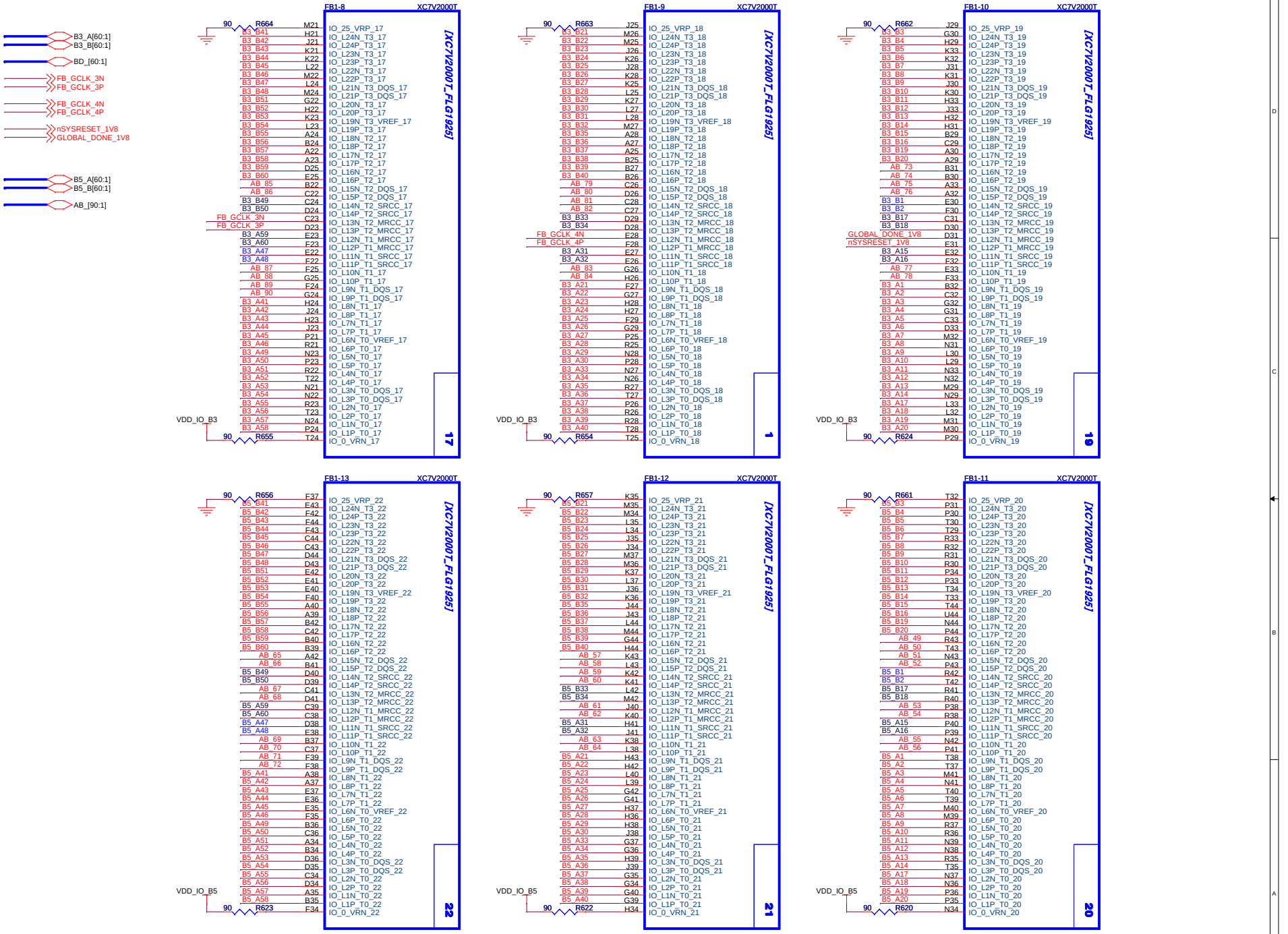

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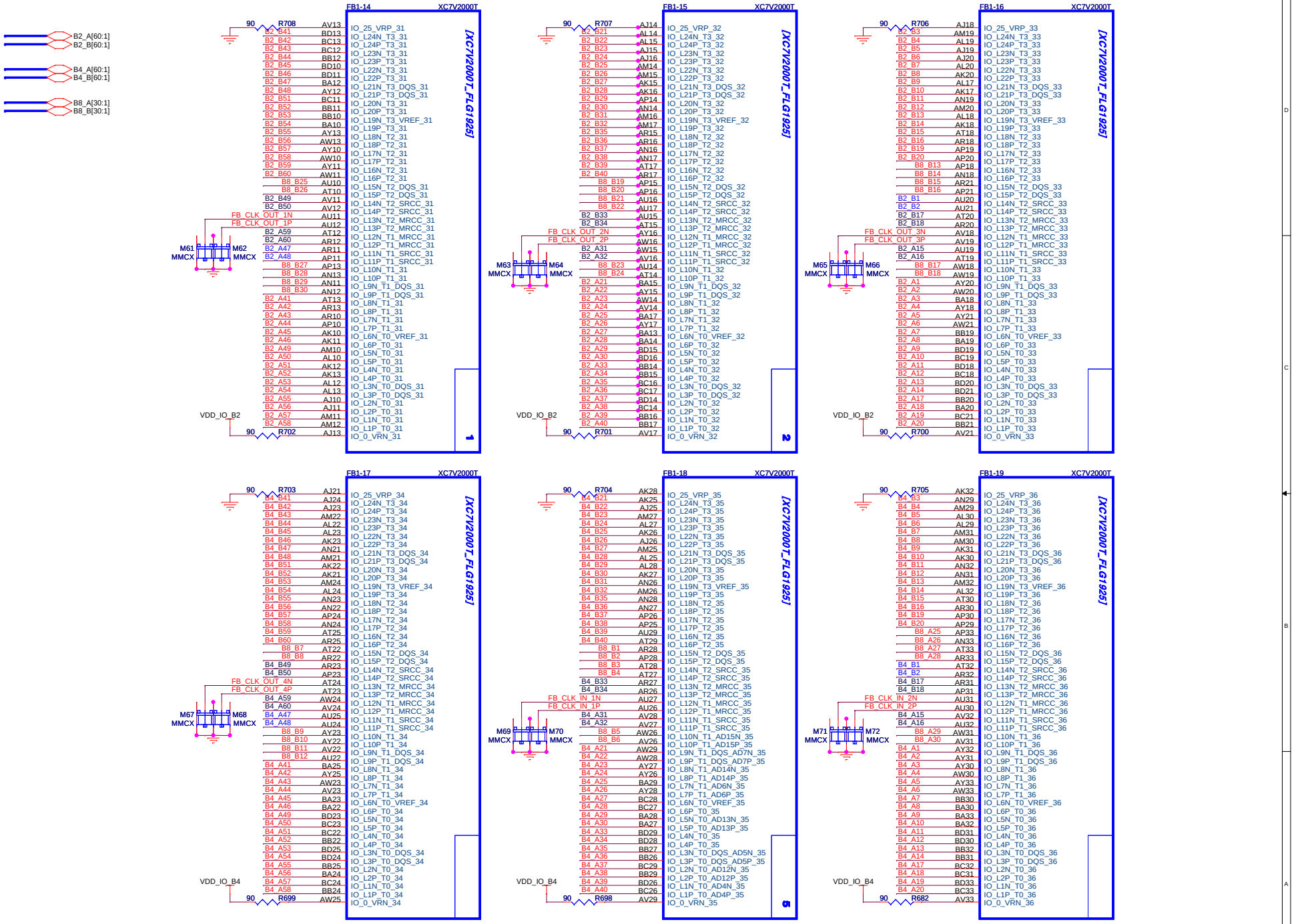

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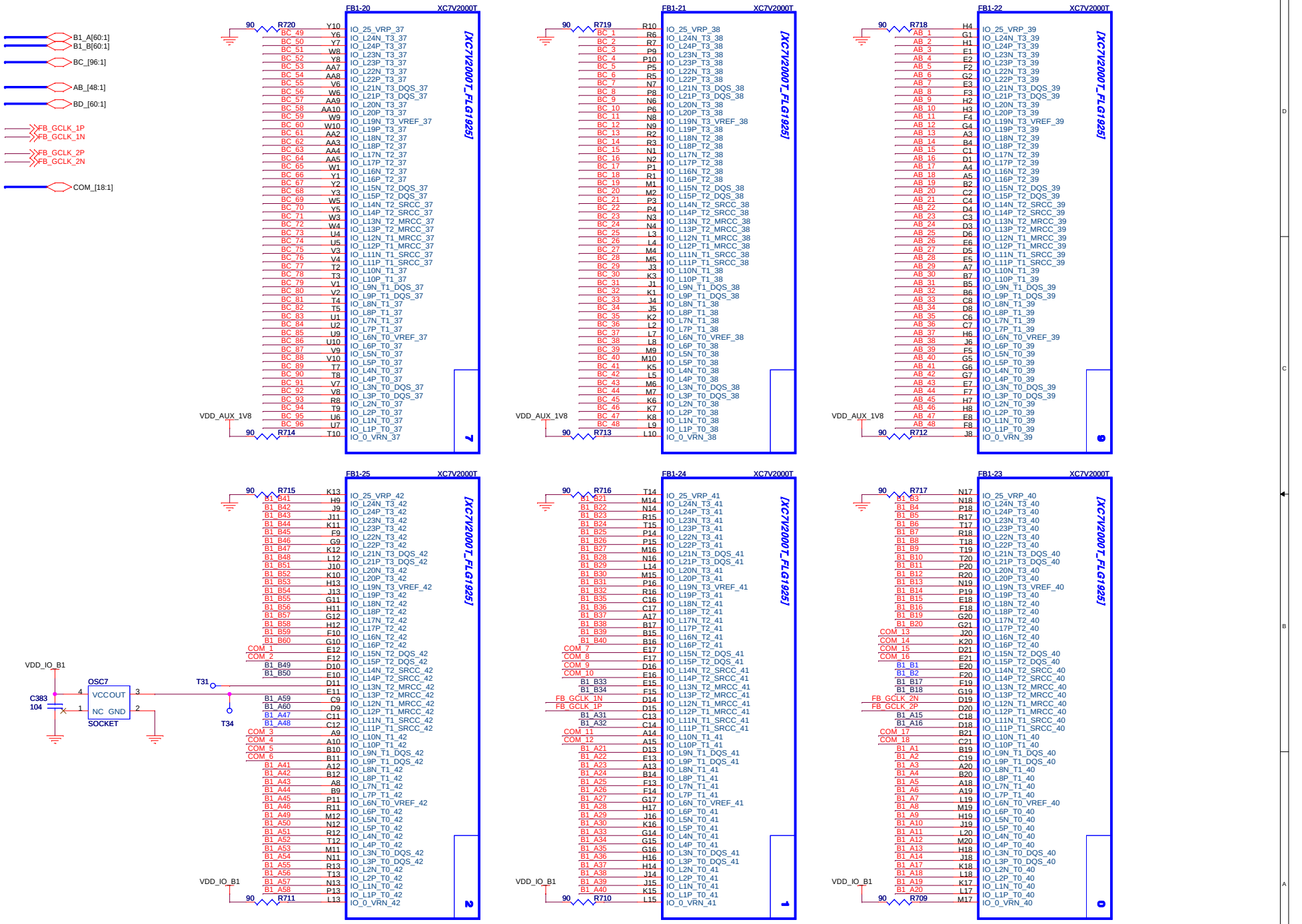

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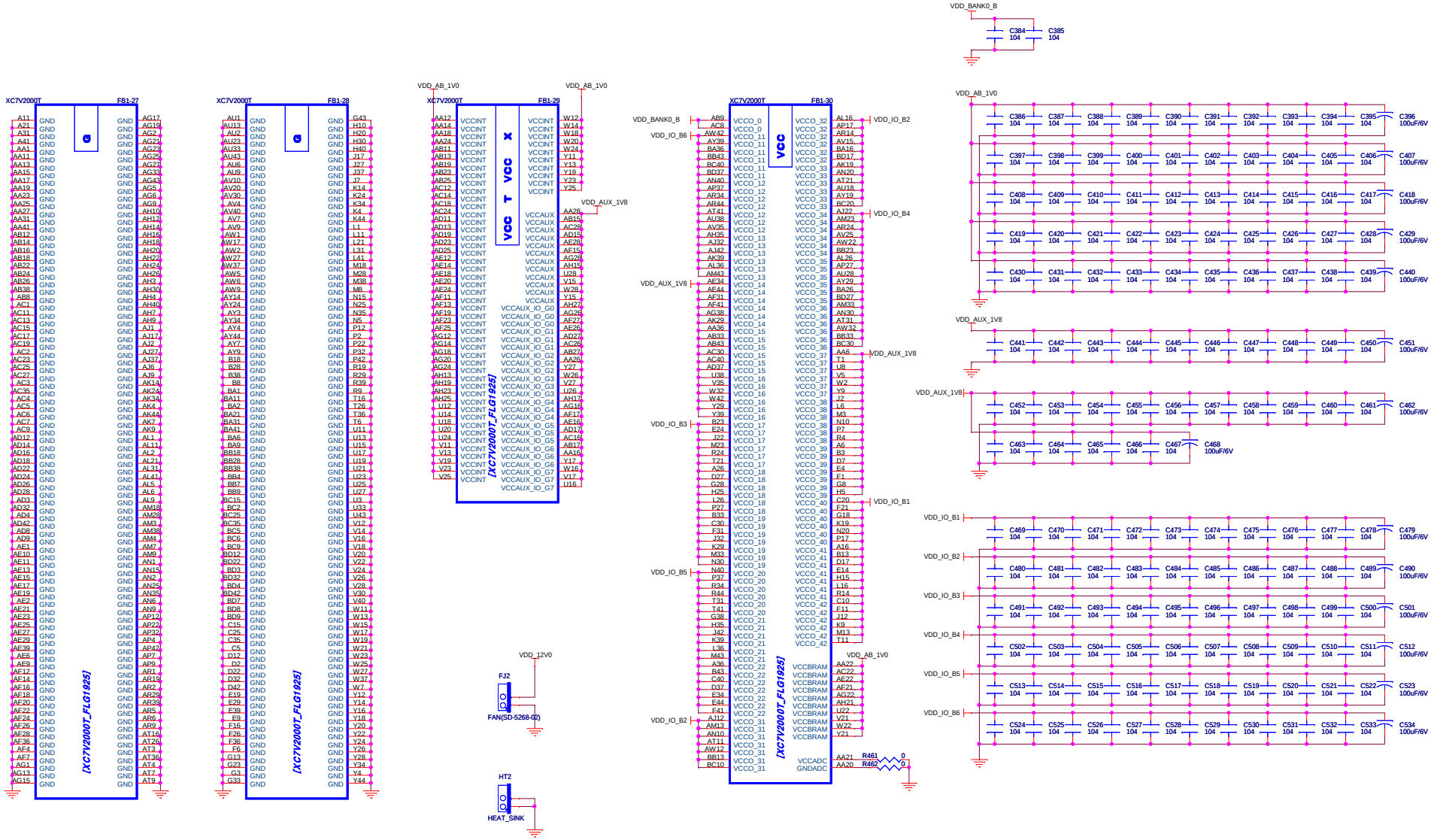
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FB1-27
FB1-28
FB1-29
FB1-30
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VDD_AUX_1V8
VDD_BANK0_B
VDD_IO_B6
VDD_IO_B2
VDD_IO_B4
VDD_IO_B3
VDD_IO_B5
VDD_IO_B1
VDD_12V0
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HT2
HEAT_SINK
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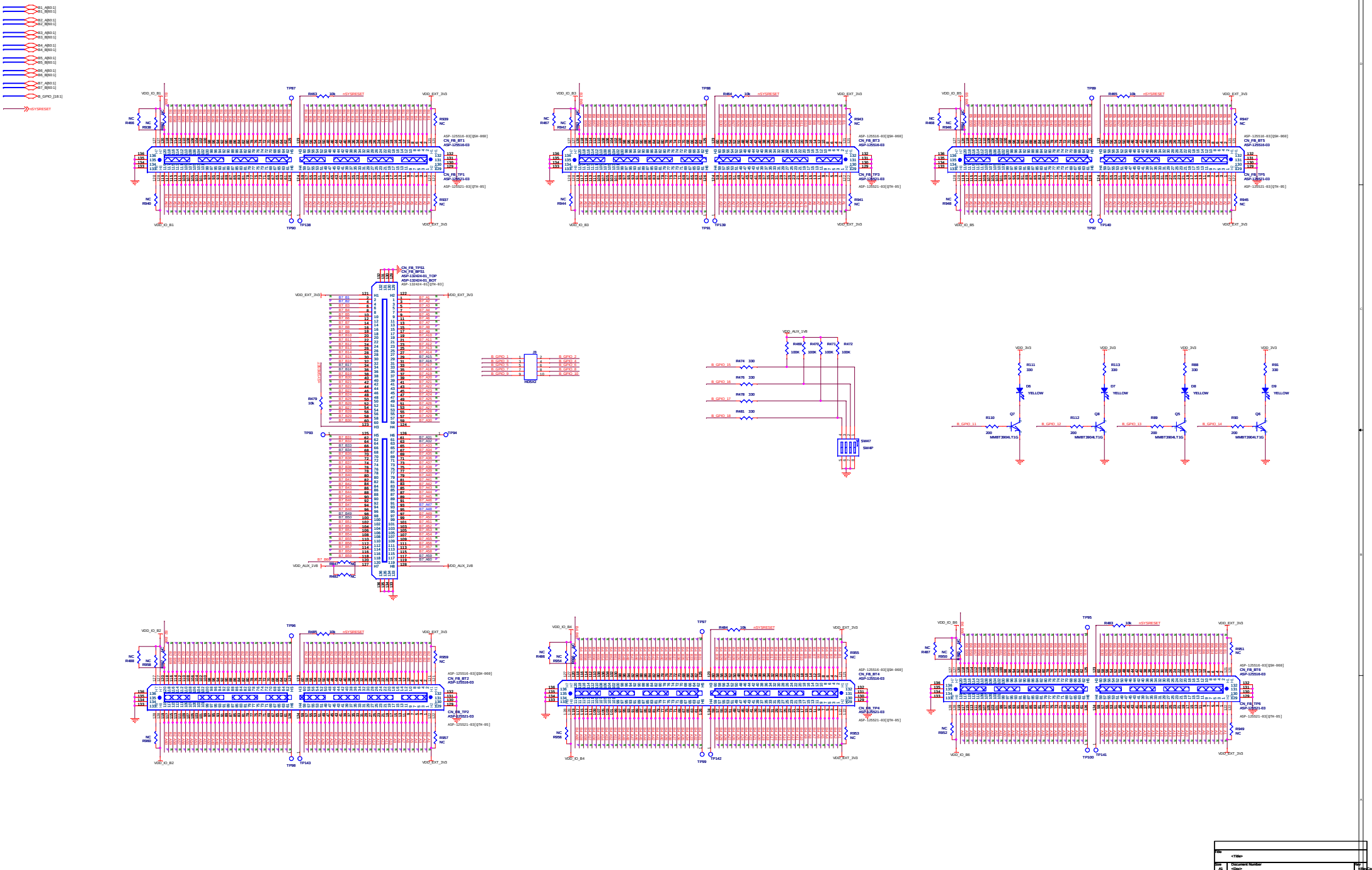

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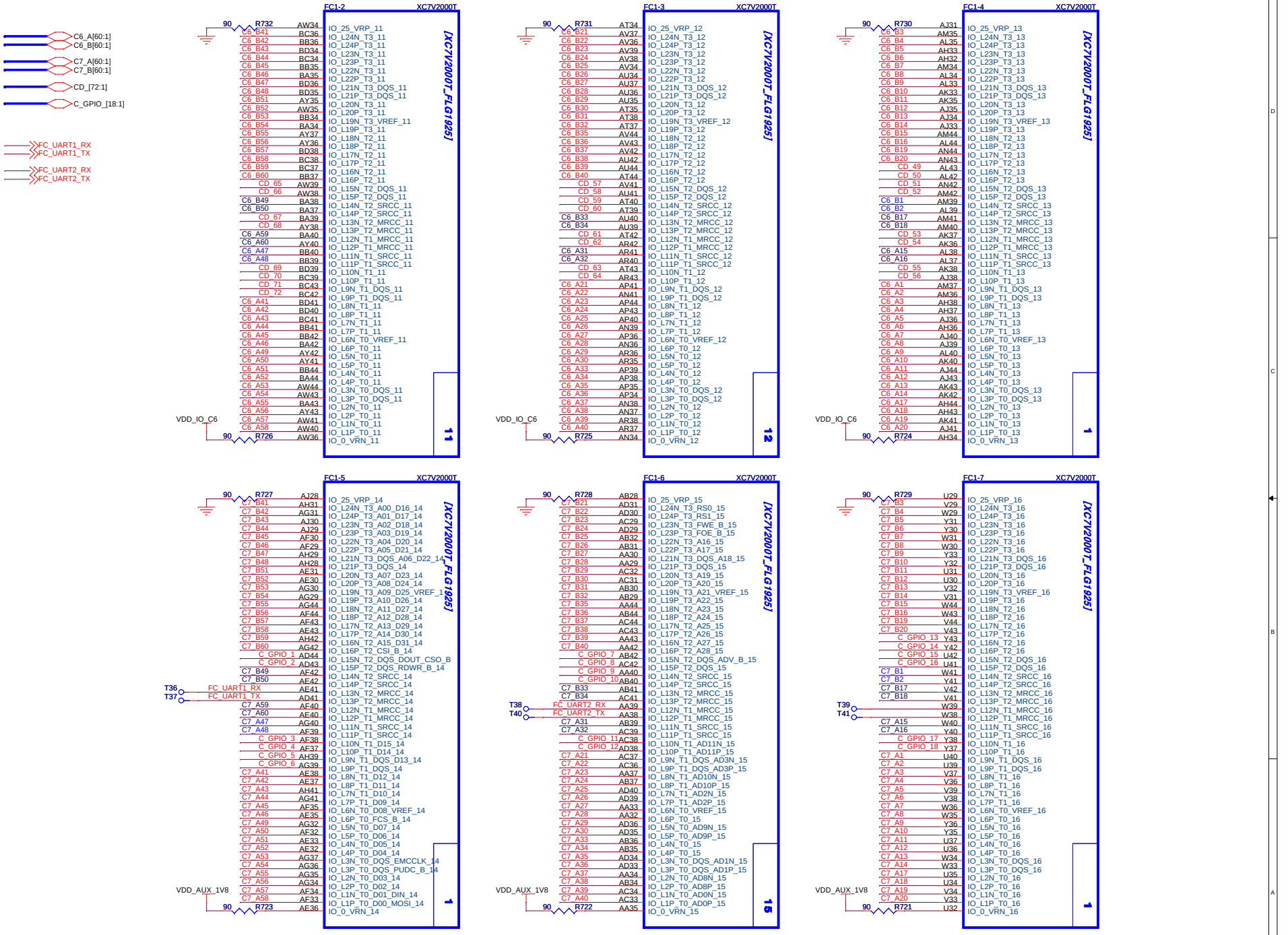

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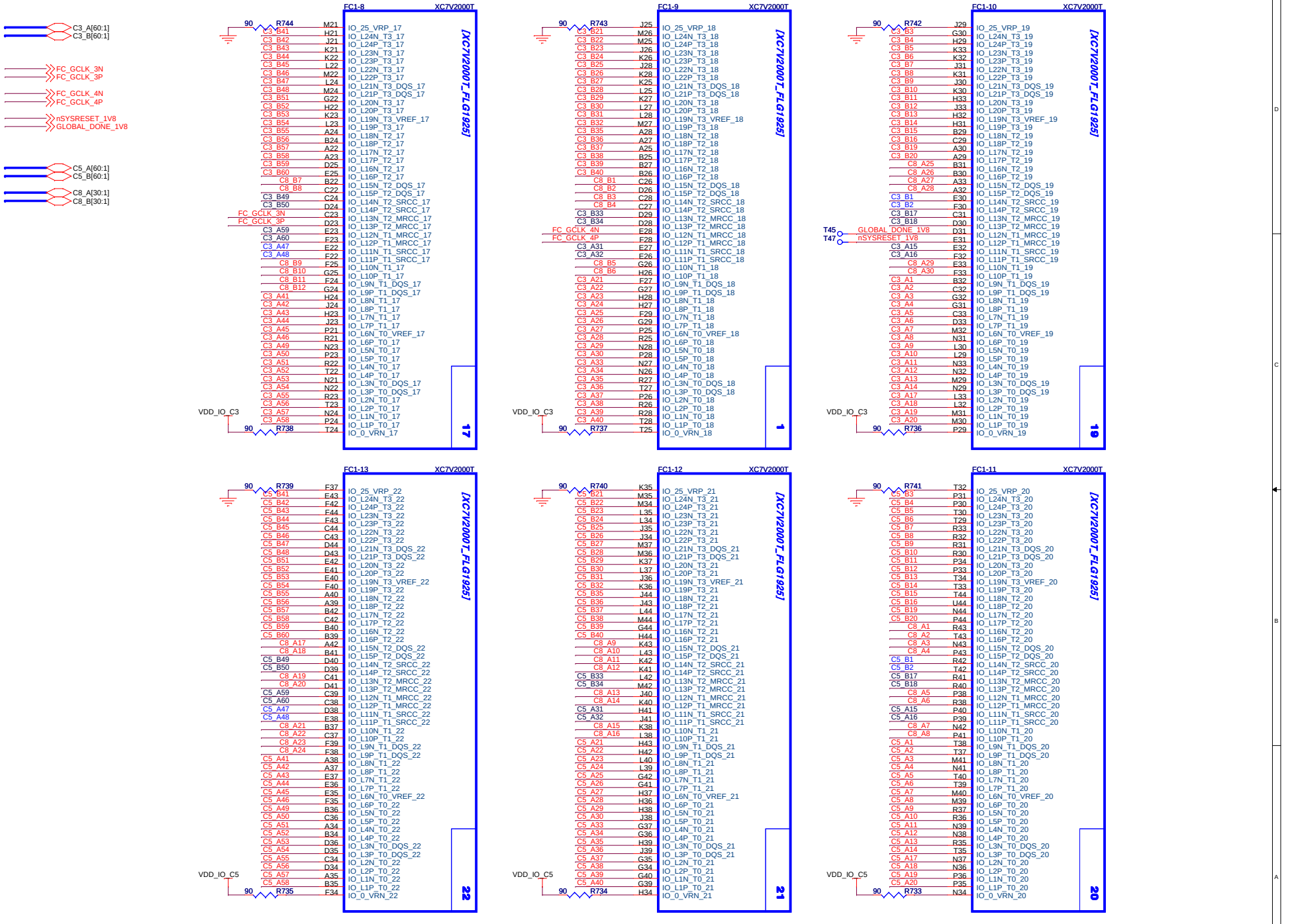

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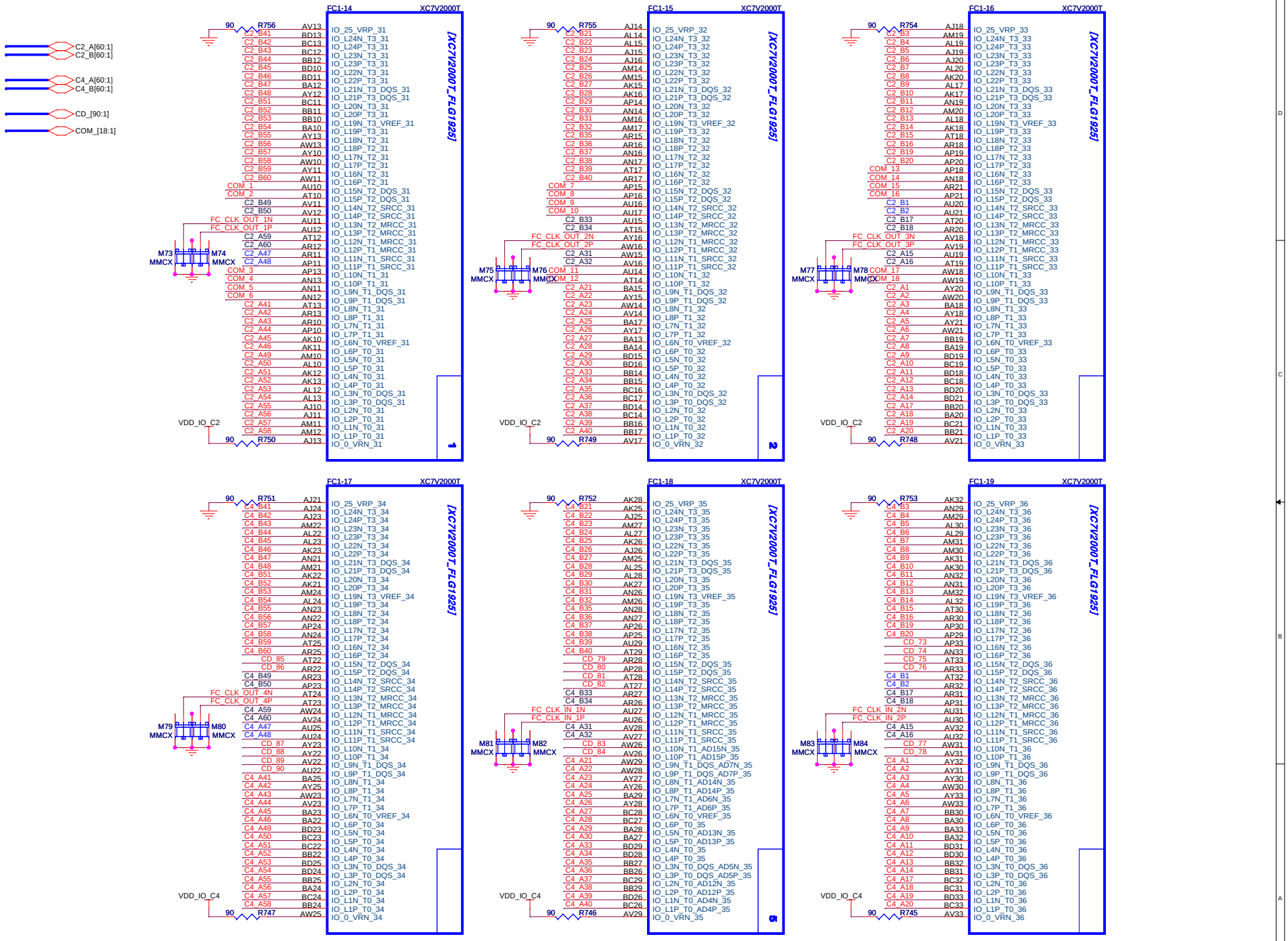

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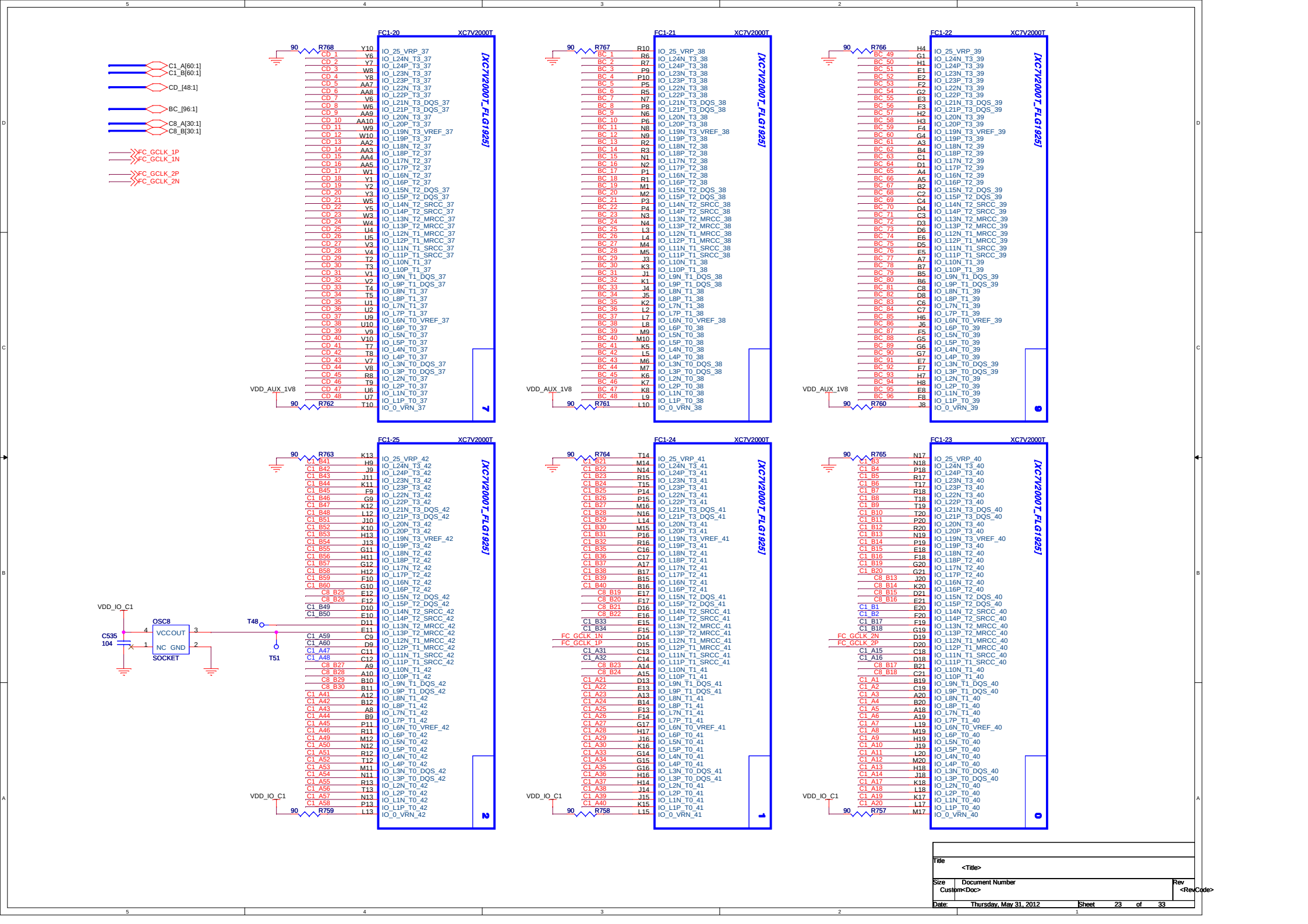

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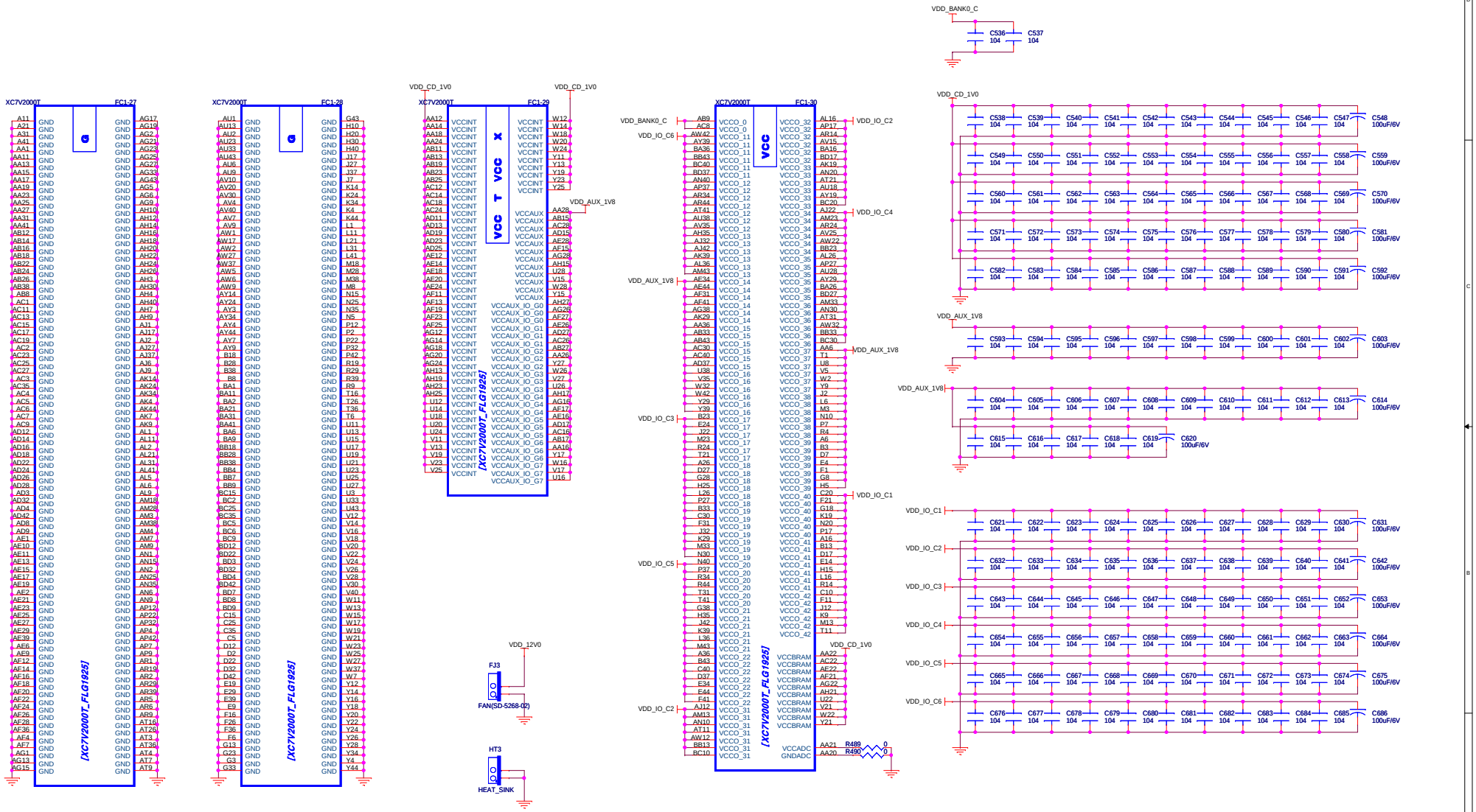

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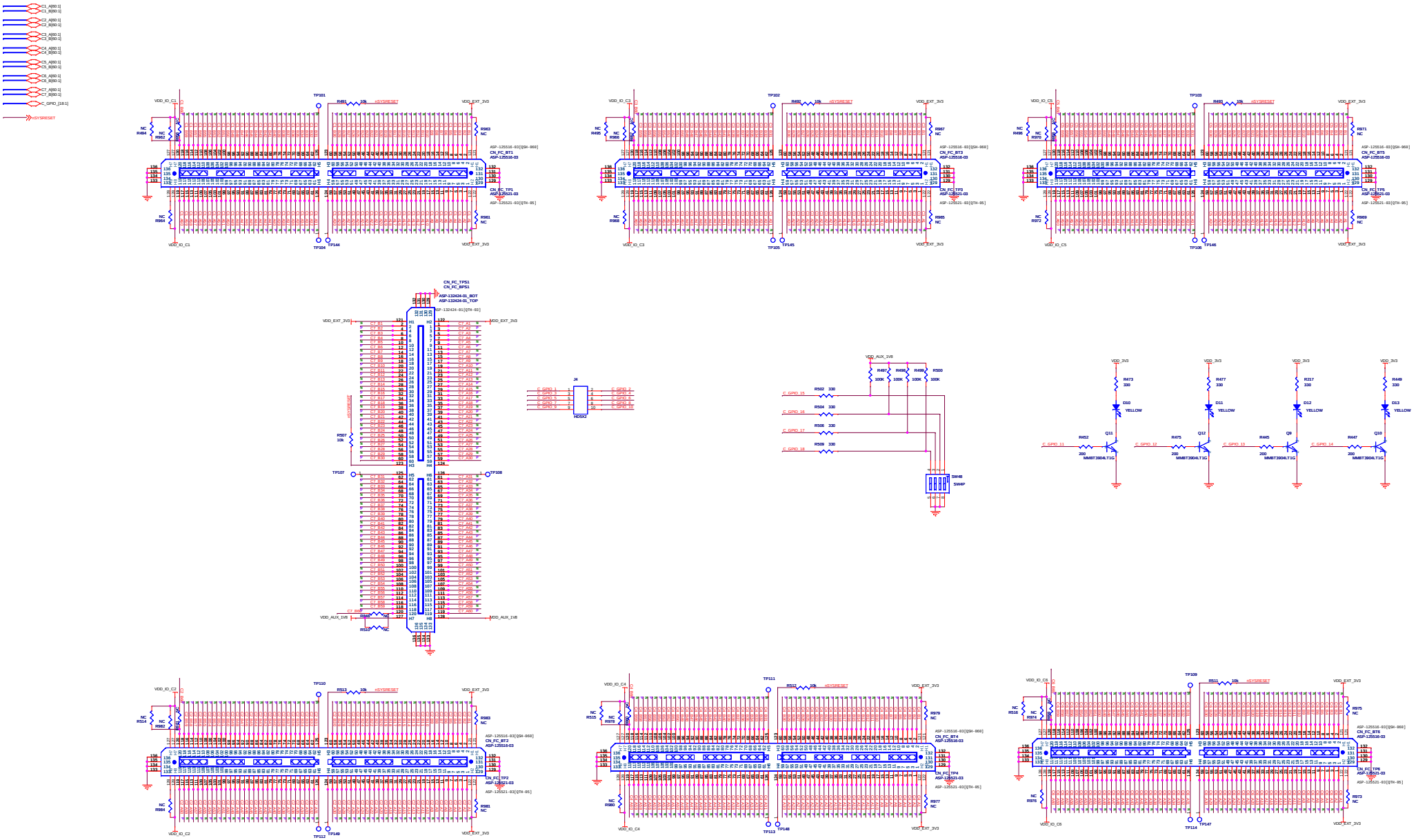

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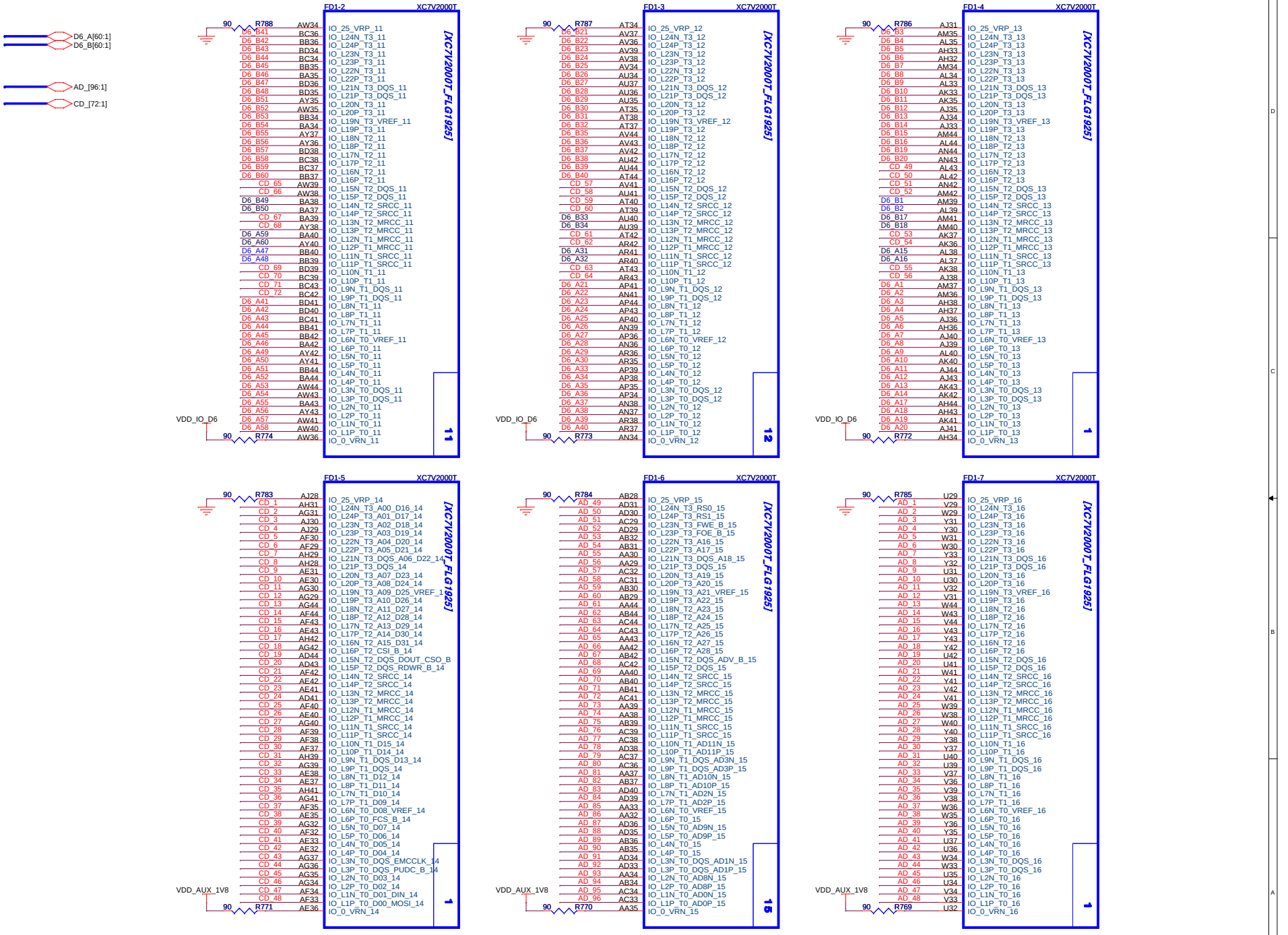

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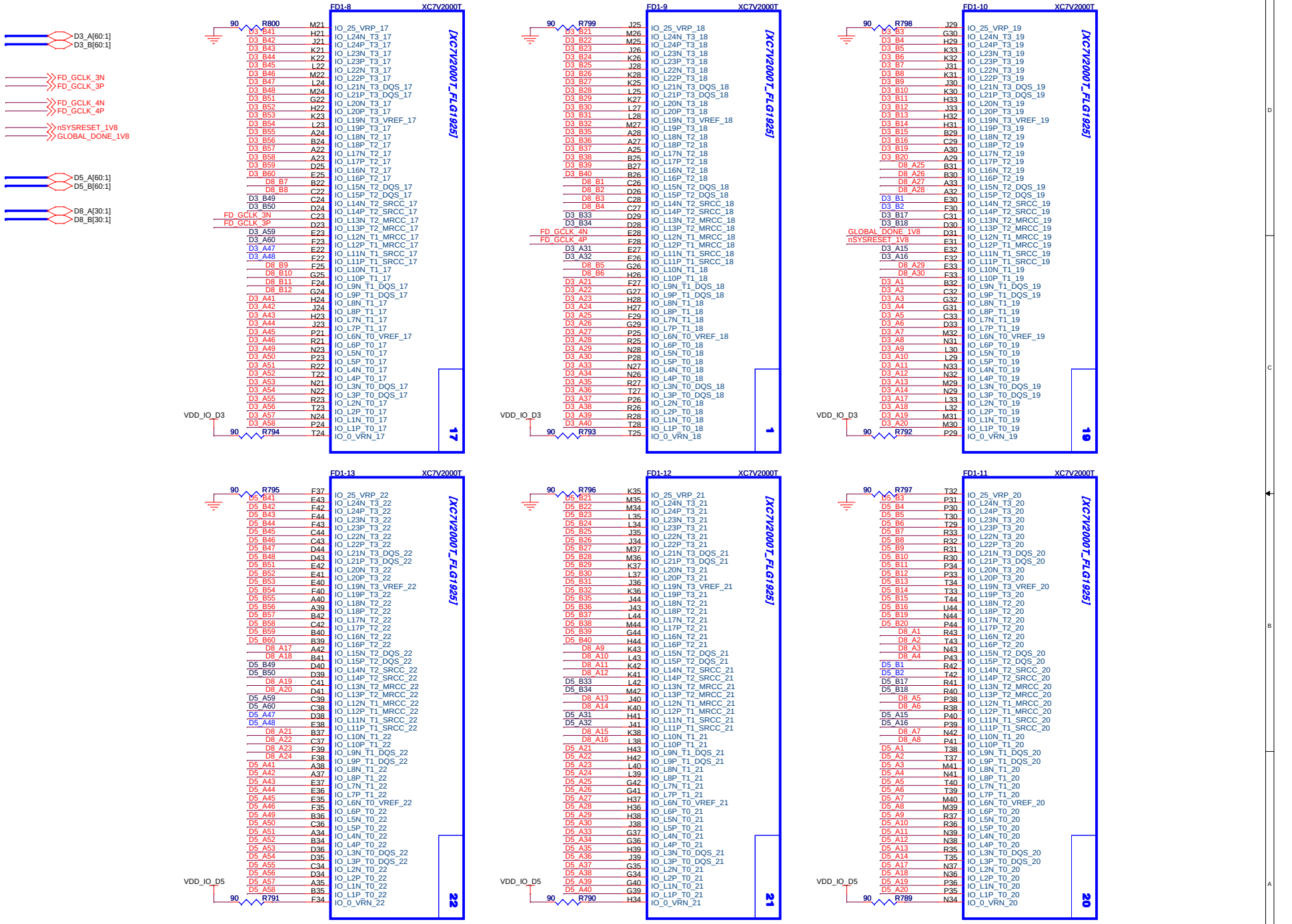

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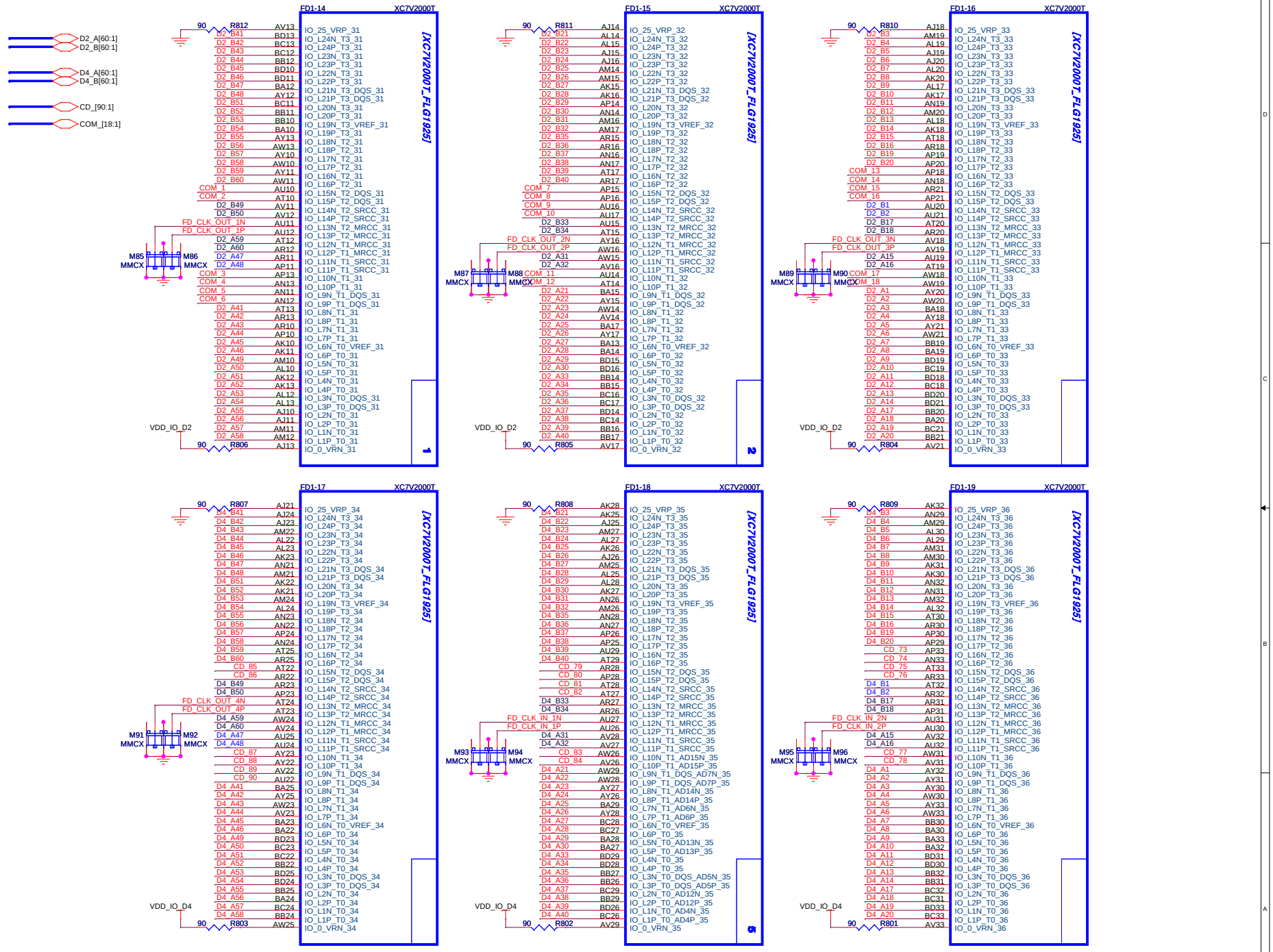

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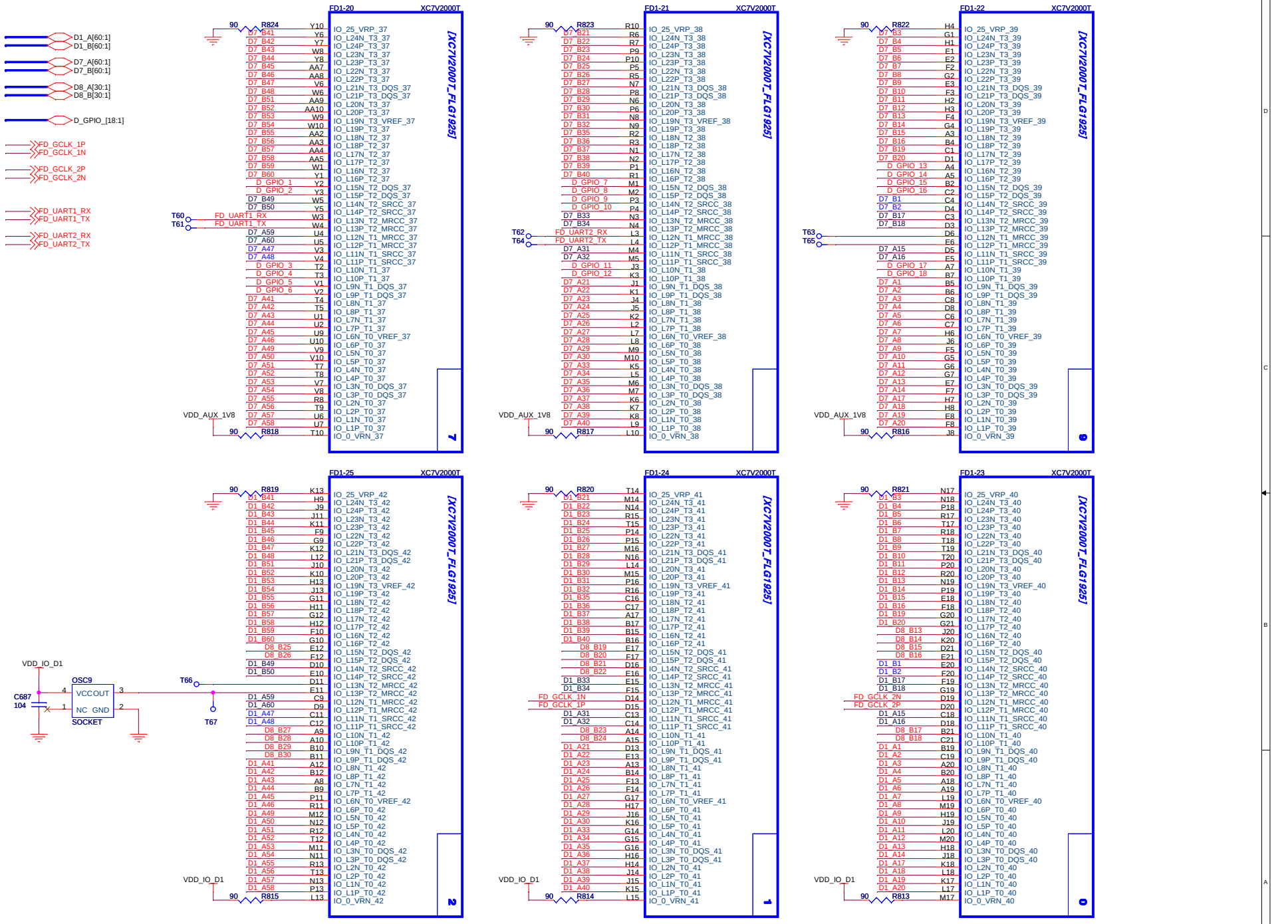

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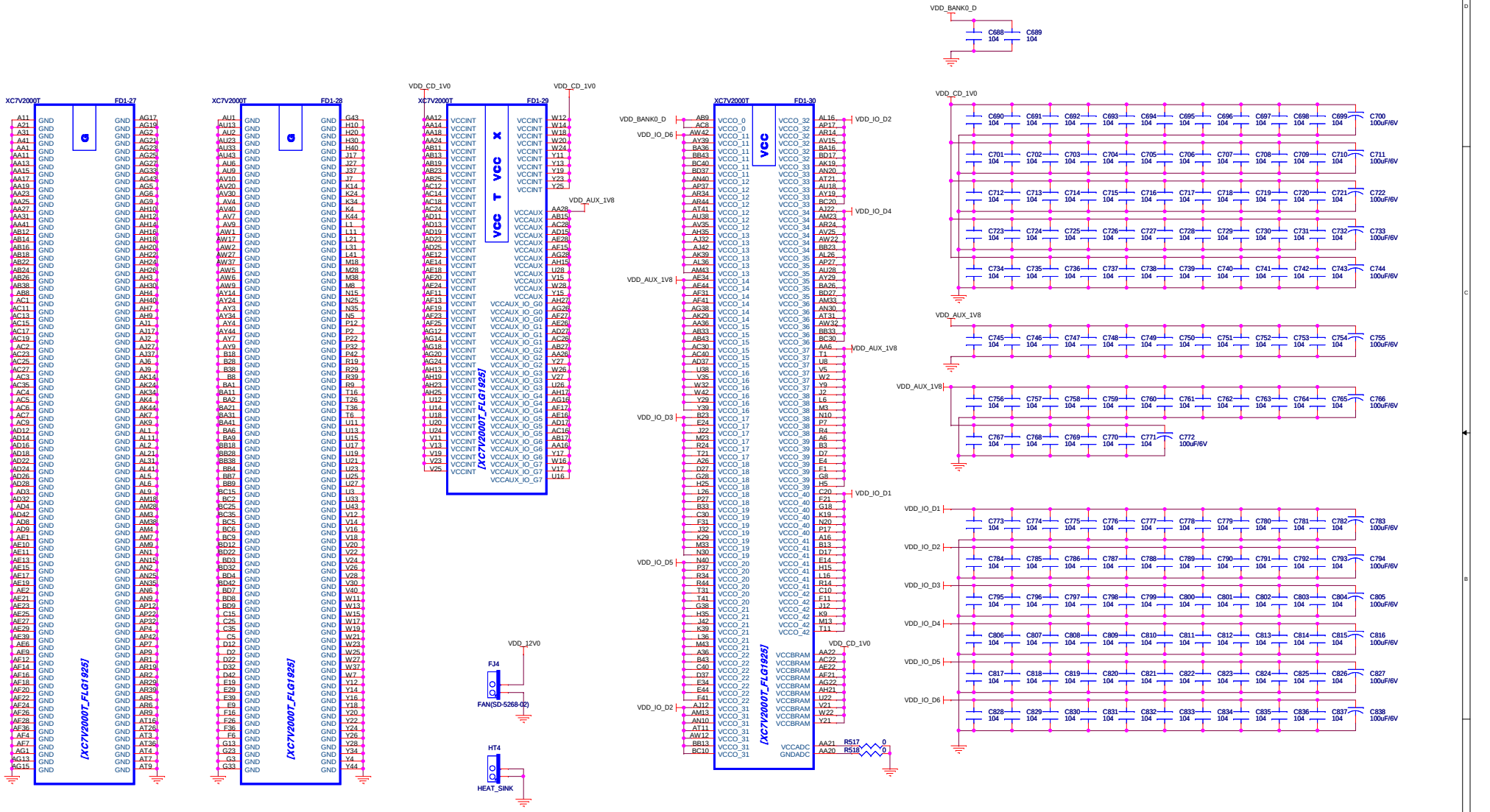

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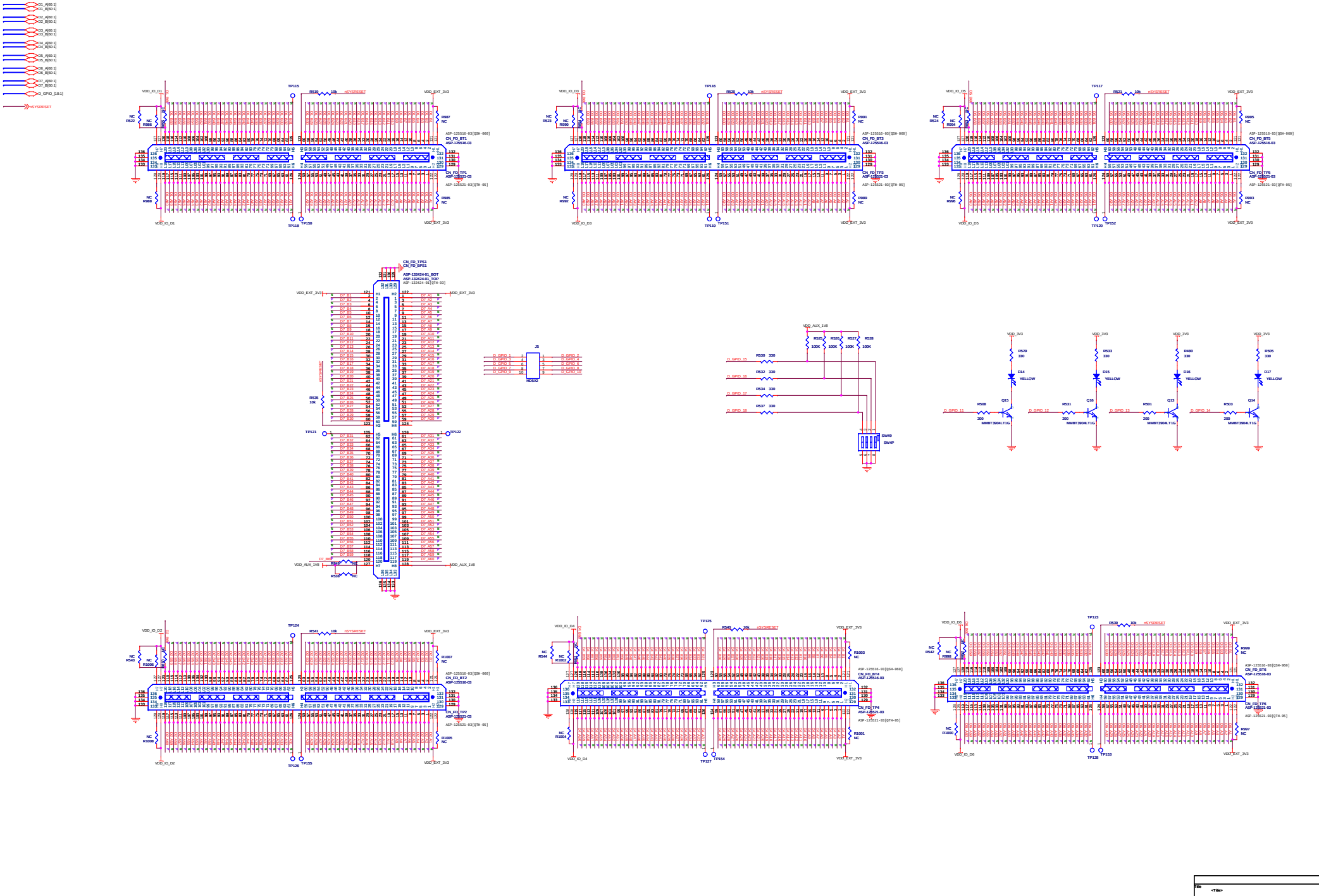

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