cadence®

Cadence VIP Catalog

Industry-leading solution has verified thousands of production designs across dozens of protocols

Cadence provides mature verification IP (VIP) and memory models that automate verification for 30+ standard protocols and 6,000+ memory components. Cadence® VIP Catalog supports all major simulators and the Universal Verification Methodology (UVM).

One-Stop Shop

Cadence VIP Catalog provides support for more than 30 complex protocols and more than 15,000 memory models. Proven on thousands of customer designs and supporting all major simulators, Cadence VIP Catalog is your reliable one-stop shop. Our leading-edge protocol support means you can be first to market with the latest technology. The scalable Cadence VIP supports all stages of product development, including in-depth IP verification, multiprotocol system-on-chip (SoC) verification, and accelerated hardware/software system verification.

Benefits

- Reduce risk by partnering with Cadence, the world leader in verification IP
- Focus scarce resources on proprietary added value by offloading verification of standard interfaces
- Increase confidence in product quality by leveraging the combined verification experience gathered over thousands of prior verification projects and now embedded in the VIP

Features

- Supports all major logic simulators
- 30+ protocols with first-to-market support for emerging standards such as AMBA 4 ACE, PCI Express Gen 3, SuperSpeed USB, Ethernet 40G/100G, and the MIPI protocols
- 15,000+ memory models including support for new memory types such as DDR4, Wide I/O, and ONFI 3.0
- Protocol compliance checking via the Compliance Management System (CMS) and PureSuite solutions
- Assertion-based VIP for formal verification of selected protocols
- Accelerated VIP for the most widely used complex protocols to support hardware acceleration of large SoCs and hardware/software integration
- Support for all common testbench languages including SystemVerilog and e
- Support for the Universal Verification Methodology (UVM)

Supported Interfaces	
Protocols	Memories
AMBA 4 ACE	DDR2
AMBA AHB	DDR3
AMBA AXI3,4	DDR4
AMBA APB	DDR4 SDRAM
CAN	DDR NVM
Ethernet	EEPROM
HDMI	Flash ONFI 3.0
I2C	Flash PPM
JTAG	Flash Toggle2NAND
LIN	GDDR3
MIPI CSI	GDDR4
MIPI DSI	GDDR5
MIPI M-PHY	LBA NAND
MIPI SLIMbus	LPDDR2,3
MIPI UniPro	LRDIMM
MIPI DigRF	MMC 4.4
OCP	One NAND
PCI Express	QDR SRA
PCI	SD Card
PLB	SDIO
SAS	SDRAM
SATA	SRAM
Serial Rapid IO	SRAM cellular
USB	Toggle NAND
USB SuperSpeed	Wide I/O SDRAM
	Plus other memory types

Simulator Support

Cadence VIP Catalog products support logic simulators from all the major electronic design automation (EDA) providers. This ensures that customers can make maximum use of their EDA investment while performing consistent, high-quality verification of standard interfaces.

Common Testbench Interface

All the VIP and memory models provide a common testbench interface that reduces the learning curve for verification teams and simplifies the maintenance of complex test environments. For advanced SystemVerilog users, the VIP supports the industry-standard UVM. Integration examples are provided to ensure quick bring-up time in SystemVerilog testbenches and reduced time-to-first-test.

Emerging Protocol Leadership

Cadence invests heavily in early support for emerging protocols, often providing VIP well before the new protocol specifications reach the 1.0 release level. This investment takes the form of active participation in protocol committees and working groups and close collaboration with leading-edge customers. By providing early delivery of VIP, Cadence is helping the industry to deliver game-changing products built around these new protocols.

Verifying Protocol Compliance

The Cadence VIP Catalog offers two solutions for advanced compliance verification—the Compliance Management System (CMS), and the PureSuite™ Test Suite.

CMS provides parameterized test scenarios for exploring the coverage space in a constrained-random simulation environment. Users set constraints to guide the generation of random test sequences to explore areas of interest. Tight correlation between functional coverage results and the protocol specification make it easy to interpret results and identify coverage holes.

PureSuite provides an extensive library of directed compliance tests that are easy to implement. The quick bring-up reduces time-to-first-test and the large test suites provide extensive compliance testing.

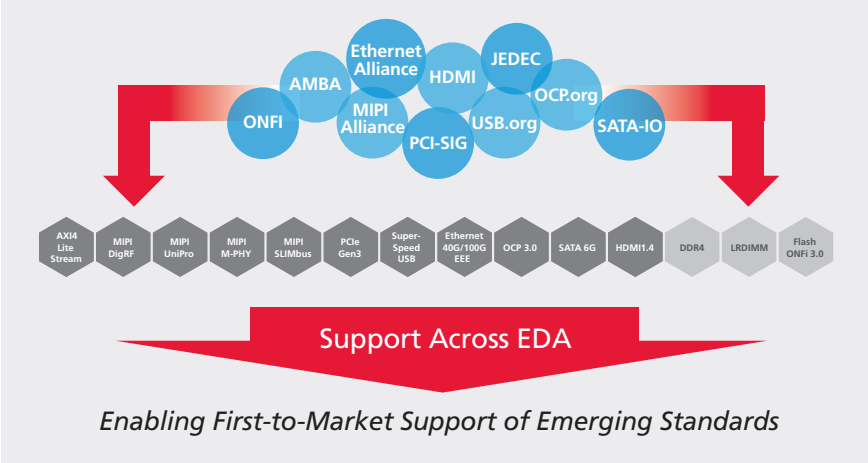

Figure 1: Cadence supports the rapid adoption of emerging protocols with early introduction of new VIP

CMS

The CMS provides a protocol-specific, metric-driven verification environment that includes:

- Executable verification plan mapped to the protocol specification
- Library of constrained random tests to isolate design-under-test (DUT) corner cases
- Integrated coverage model to grade verification completeness
- Compliance checks and metrics to identify DUT verification gaps

Protocol compliance starts with the Verification Plan (vPlan). All verification objectives are captured in the vPlan and correlated to the protocol specification on a paragraph-by-paragraph basis. A library of constrained-random test sequences

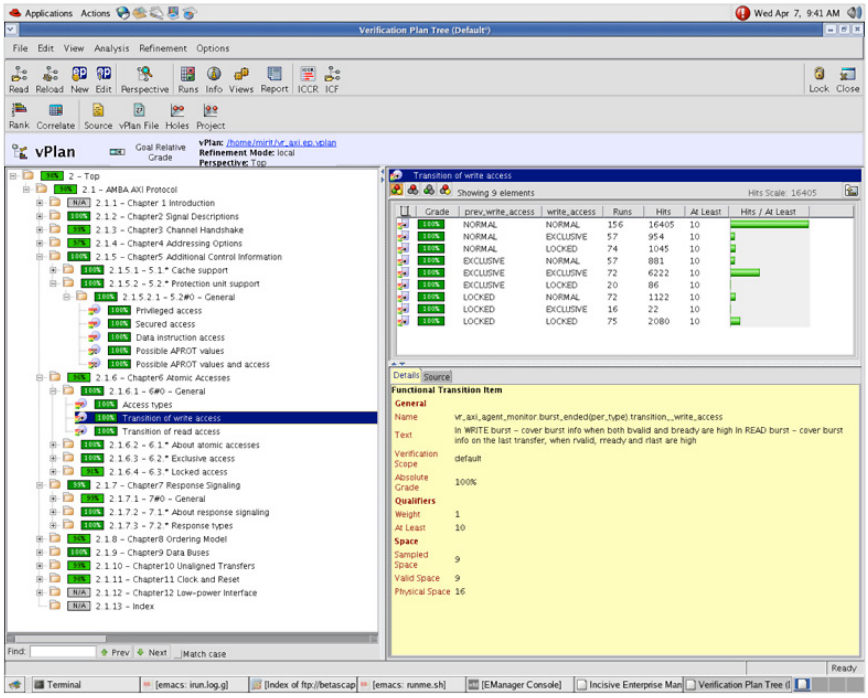

Figure 2: CMS example showing AMBA AXI vPlan with coverage resulting from multiple simulation runs

then stimulates the DUT with multiple parameter combinations for each coverage point of interest.

Results from multiple simulation runs are integrated and graphically displayed in the vPlan window. Cumulative coverage vs. plan is displayed and any coverage gaps are clearly identified. The verification engineer then adjusts the test-generation constraints to focus additional test sequences on the coverage points of interest.

Project management is facilitated through various reports and charts, which measure progress vs. plan. Early warning is thus provided for schedule deviations and resource limitations.

PureSuite Test Suite

Each PureSuite test is designed to cover specific compliance checklist items, and each test includes a detailed description of purpose, assumptions, scenario, and expected results. Tests are driven from the VIP across the protocol interface toward the design under test, or can be initiated from the application interface of the design. Capabilities include:

- Thousands of pre-built tests for exercising specific functionality and corner cases
- Matched to the protocol's compliance checklist
- Error recovery testing
- All protocol layers and key state machines covered
- Configurable based on DUT implementation and target device selection
- Context-sensitive test selection
- Specification and test coverage generation
- Cumulative coverage reporting

"We brought up the CMS compliance test suite in our verification environment in just a day. Our team was impressed with the rapid results. We identified a number of failures right away and we're now working to dramatically expand our regression runs to take full advantage of the CMS."

– Mike Bartley, Founder and CEO, TVS

Scalable Verification Solution

Cadence provides users with a scalable VIP solution. Many VIP Catalog products not only support verification using popular logic simulators, but also support accelerated verification using the Palladium platform. This enables users to tradeoff verification functionality for speed as they progress from block to chip to system-level verification. In addition, Cadence provides assertion-based VIP for use with Cadence formal verification engines. Assertion-based VIP is particularly useful for design engineers since no stimulus is required.

Assertion-Based VIP

Assertion suites are provided for selected protocols. Typically consisting of 100 to 200 protocol checks, these suites provide a convenient mechanism for design engineers to participate in the verification of their modules. Using formal analysis tools such as Cadence Incisive® Formal Verifier, modules may be verified while the design is still in process without requiring testbench creation.

Formal Verification

Formal analysis uses properties to define the desired behavior of a design within the design's environment. There are two types of properties:

- **Assertions:** Properties that express the desired behavior of a design under verification
- **Constraints:** Properties that express the behavior of the environment

The assertion-based VIP includes hundreds of properties to formally verify compliance to specifications. The properties are fully validated. Engineers can connect them directly to their design without concern for false negative results.

Since no stimulus or testbench is required, design engineers can initiate the verification process before handing off the design to the verification team.

Cadence supports "pure formal" analysis with Cadence Incisive Formal Verifier, and integrated formal and dynamic simulation technologies in Cadence Incisive Enterprise Verifier XL. Both tools leverage the familiar SimVision GUI. This ensures ease of use when moving between simulation and formal verification.

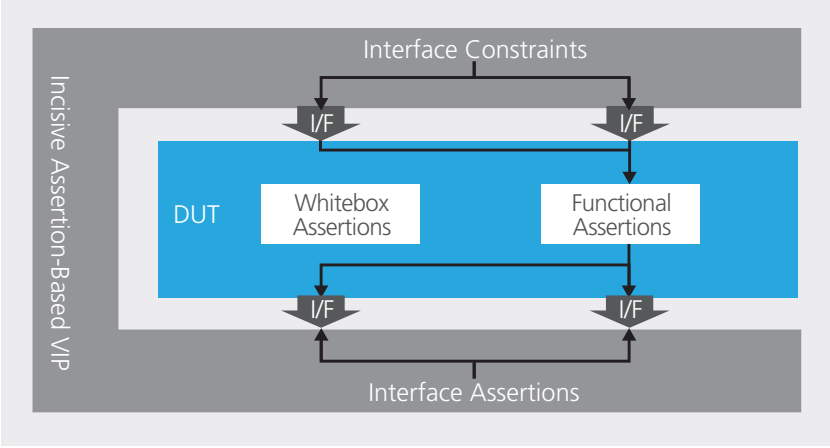

Figure 3: Assertion-based VIP provides constraints and assertions to support formal analysis

Accelerated VIP

To provide users high-end verification performance, many VIP Catalog products support accelerated verification using the Palladium platform. This enables users to tradeoff verification functionality for speed as they progress from block to chip to system-level verification.

Cadence Accelerated VIP supports three different use modes. These are transaction-based C acceleration, transaction-based UVM acceleration, and signal-based UVM acceleration. The C acceleration mode provides the absolute highest performance and throughput for system-level verification. The UVM acceleration modes enable reuse of the simulation testbench and a higher degree of verification capability. This allows users to tradeoff performance and verification capability to meet their needs at each stage in the design process.

Advantages of Cadence Accelerated VIP

- Easy to control tradeoff between performance and verification capability
- C acceleration mode for maximum performance and throughput
- UVM acceleration mode for maximum testbench reuse
- Verifies protocol compliance during simulation and acceleration

Flexible Packaging

Cadence VIP Catalog provides flexibility in product licensing to meet a wide range of needs. All VIP are available as individual a-la-carte licenses for dedicated protocol verification. The VIP and memory models are also available in portfolios to provide a cost-effective solution for customers verifying SoCs containing multiple protocols or developing a range of projects whose protocol requirements vary over time.

Cadence Services and Support

- More information regarding Cadence VIP Catalog is available at: http://www.cadence.com/products/fv/ verification_ip
- Hands-on demos of Cadence Verification IP are available at the Xuropa online community: www.xuropa.com/cadence
- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

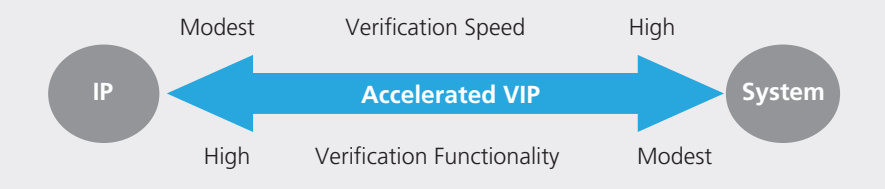

Figure 4: Accelerated VIP enables users to control tradeoffs between verification capability and performance

Use Model	Signal-Based Acceleration	Transaction-Based Acceleration	
User Interface	UVM	UVM	C
Performance	Modest	Medium	High
Environment Reuse	High	High	Modest
Verification Functionality	High (Protocol Verification)	Medium-High	Modest (System Dataflow Verification)

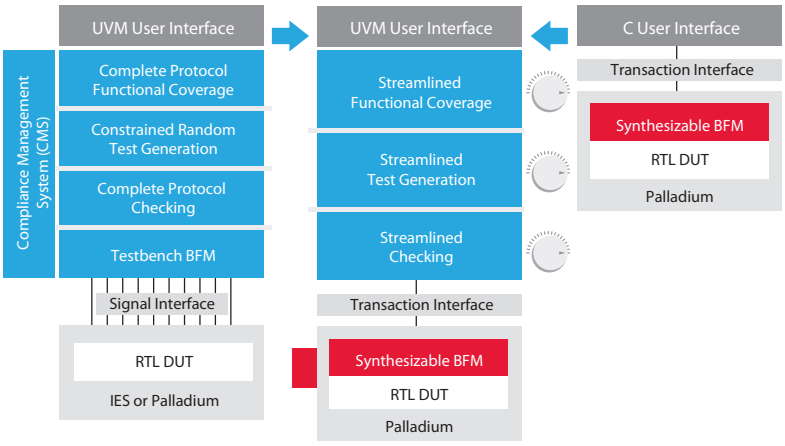

Figure 5: Three verification IP acceleration use modes

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Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com