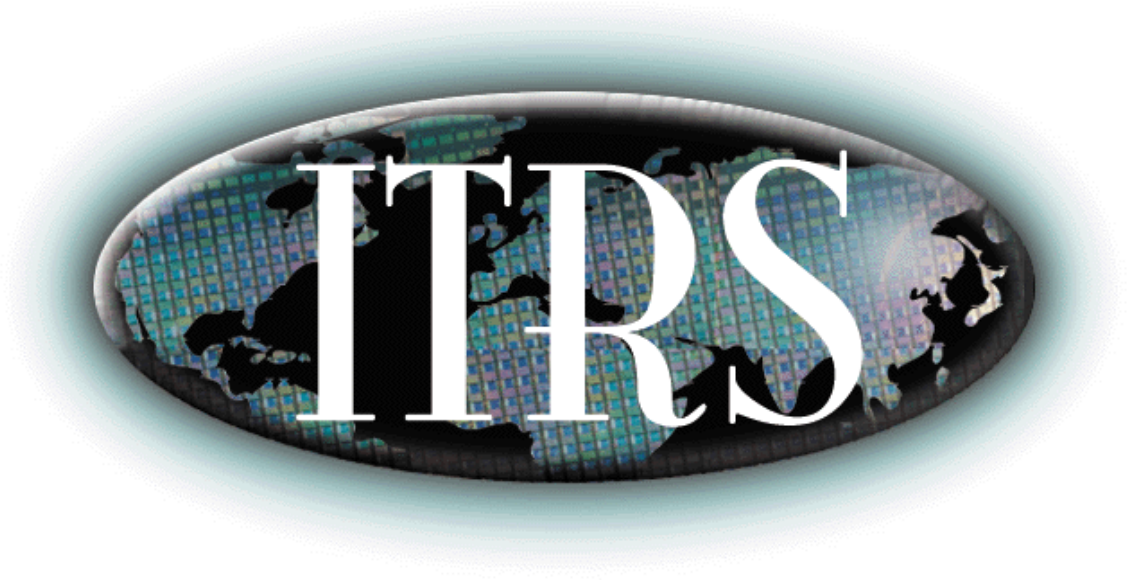

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2013 EDITION

MODELING AND SIMULATION

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MODELING AND SIMULATION

1. SCOPE

Technology Modeling and Simulation covers the region of the semiconductor modeling world called extended TCAD, and it is one of the few enabling methodologies that can reduce development cycle times and costs. Extended TCAD, within the scope of this document, covers the following topical areas, as shown in Fig. MS1: 1) *Equipment/feature scale modeling*—hierarchy of models that allows the simulation of the local influence of the equipment (except lithography) on each point of the wafer, especially in deposition, etching and CMP processes, starting from the equipment geometry and settings; 2) *Lithography modeling*—modeling of the imaging of the mask by the lithography equipment, the photoresist characteristics and processing; 3) *Front end process modeling*—the simulation of the physical effects of manufacturing steps used to build transistors up to metallization, but excluding lithography; 4) *Device modeling*—hierarchy of physically based models for the operational description of active devices; 5*) Interconnect and integrated passives modeling*—the operational response (mechanical, electro-magnetic, and thermal properties) of back-end architectures; 6) *Compact modeling*—compact models for active, passive, and parasitic circuit components, and new circuit elements based on new device structures; 7) *Package simulation*—electrical, mechanical, and thermal modeling of chip packages; 8) *Materials modeling*—simulation tools that predict the physical properties of materials and, in some cases, the subsequent electrical properties; 9) *Reliability modeling*—the modeling of reliability and related effects on process, device and circuit level; 10) *Modeling for design robustness, manufacturing and yield*—the development of additional models and software to enable the use of TCAD to study the impact of inevitable process variations and dopant fluctuations on IC performance and in turn design parameters, manufacturability and the percentage of ICs that are within specifications; 11) *Numerical methods and Interoperability of tools* —all algorithms needed to implement the models developed in any of the other sections, including grid generators, surface-advancement techniques, (parallel) solvers for systems of (partial) differential equations, and optimization routines, and the interfacing/integration between various simulation programs. As shown in Figure MS1, these areas can be grouped into equipment-, feature and IC-scale. Items 8 to 11 are unique because they in fact cross-cut almost all other topics in Modeling and Simulation. Material and reliability issues are becoming more and more important in all processes as well as for active devices and interconnects. Design robustness, manufacturing and yield are affected by all areas simulated. Numerical algorithms are shared by most of the areas in simulation.

Suppliers of modeling and simulation capability are mainly universities and research institutes funded by government and/or projects. TCAD vendors play an important role in the development of those capabilities, and are in most cases the interfaces between R&D and the end customer in industry, customizing the R&D results into commercially supported simulation tools. Simulation efforts in semiconductor industry mainly focus around the adaptation and application of the simulation capabilities to the development and optimization of technologies, devices, and ICs.

The development of new modeling capability generally requires long-term research, and increasingly interdisciplinary activities, which can be carried out best in an academic or a laboratory setting. For this reason, a vigorous research effort at universities and independent research institutes is a prerequisite for success in the modeling area, together with a close cooperation with industry, along the simulation food chain mentioned above. Because the necessary basic work generally needs significant development time, it is vital that adequate research funds will be made available in a timely manner in order to address the industry's future critical needs. Currently, the shortage of such research funds is even more severe than the technical difficult challenges summarized below. For example, similar to the 2011issue again several Modeling and Simulation requirements listed in the 2011 ITRS had in this 2013 issue to be pushed out and delayed in time because sufficient R&D could not be done due to insufficient research funding.

Compared with the 2011 ITRS, the scope of the Modeling and Simulation challenges has considerably changed, while those of the individual subchapters have been kept unchanged. The difficult challenges shown below evolved from the 2009 challenges based on relevant changes of the options studied or prioritized, and requirements raised by the other ITWGs, as well as based on the development of the state-of-the-art. Concerning the Modeling and Simulation requirements, Table MS3 on the accuracy specifications, which among others also mentions the estimate of costs and time saving by the use of simulation in development, is not included in the 2013 chapter because it still needs to be updated.

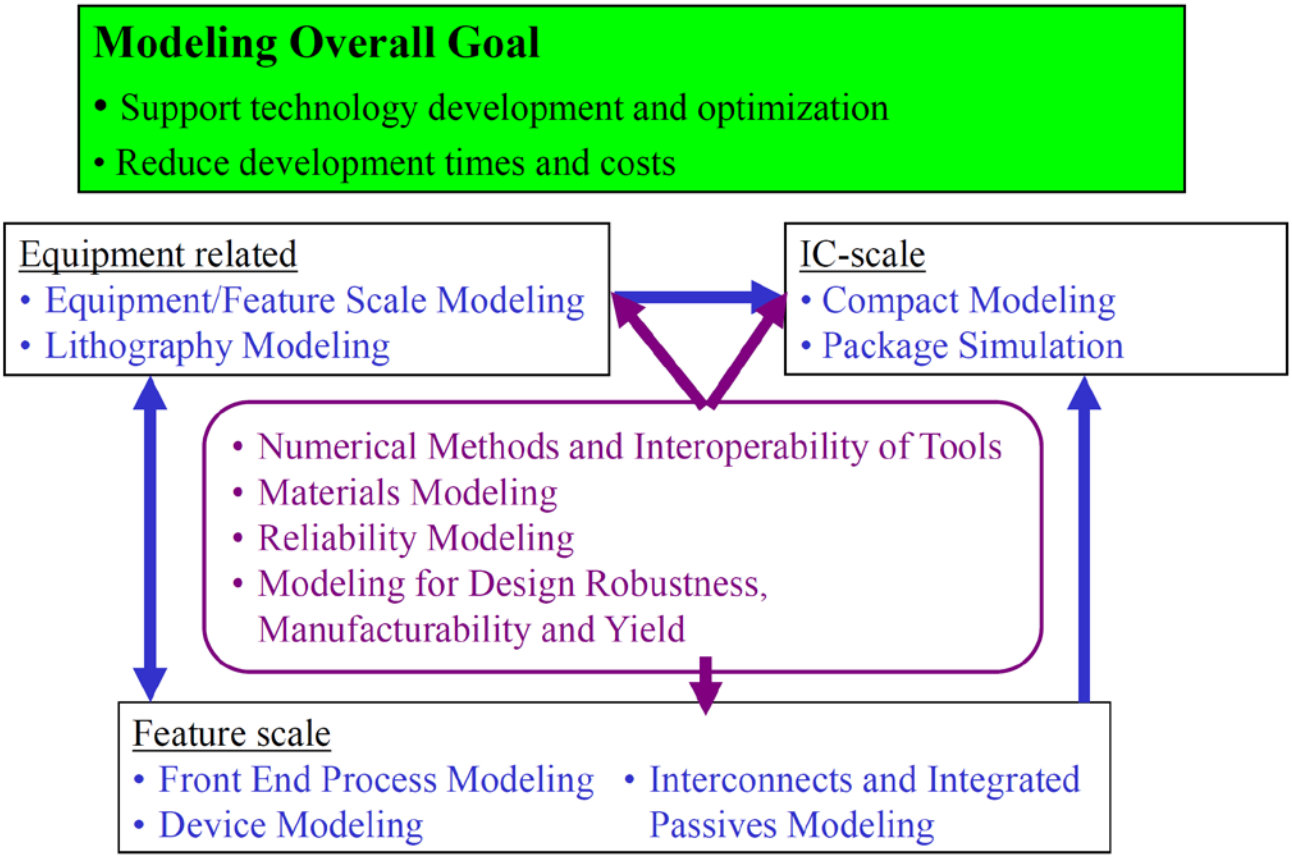

Figure MS1 Modeling and Simulation Scopes and Scales

2. DIFFICULT CHALLENGES

The difficult challenges highlighted in Table MS1 are those Modeling and Simulation requirements which on one hand must be met in time to support the high-level progress of the roadmap and on the other hand are most critical to fulfill due to their technical difficulty and the R&D resources needed. Additionally, it should be noted that a key difficult challenge present across most of the modeling areas is that of experimental validation. This challenge is especially difficult because for most processes many physical effects interact with each other and must be appropriately separated by well-selected experiments, in order to be able to develop predictive models and not simply fit experimental data. As devices shrink and new materials are introduced into the technology arena, new and enhanced analytical techniques are vital that can extract the necessary information for this model development and evaluation validation from the experiments. This critical need is mentioned as a cross-cut item with the Metrology ITWG.

Table MS1 Modeling and Simulation Difficult Challenges

Difficult Challenges 2013-2020	*Summary of Issues*
Integrated modeling of equipment and feature scale processes	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-k metal gate); reaction mechanisms (reaction paths and (by-) products, rates ...) , and simplified but physical models for complex chemistry and plasma reactions
	Linked equipment/feature scale models (including high-κ metal gate integration, flows for RIE processes, damage prediction)
	Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling
	Oxidation below 800C using non-thermal energy sources, e.g. for STI sidewalls, liner oxides, interfacial oxides
	Spin-on-dielectrics (stress, poriosity, dishing, viscosity, …) for high aspect ratio fills, evolution during transformation and densification
	Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
	Pattern/microloading effects in radiative annealing or plasma processing
	Impact of wafer situation (temperature, reaction) on gas flow/reactions in reactor
	Simulation of wafer polishing, grinding and thinning
	Modeling of impact of consumables (e.g. resists, slurries, gas quality ….) on process results
Lithography simulation as contribution to further scaling	Simulation of multi-layer defect propagation, inspection and characterization, and their impact on defect printing. Mask-level correction or optimization including defect repair or compensation based on defect signature available from characterization
	Modeling of pellicle effects and pellicle defects simulation, particle printability, including EUV pellicles
	EUV / ebeam resist effects, e.g. secondary electron propagation, resist heating, stochastic effects and LER, including process effects for LER mitigation
	Advanced resist materials and processing effects, including negative tone development, resist reflow, finite polymer-size / molecular resist effects / nano-particle resists; adhesion, mechanical stability, pattern collapse
	Simulation of special patterning techniques such as spacer formation in multi-step patterning applications, directed self-assembly for pattern formation, layout decomposition, guiding pattern optimization, defect prediction and metrology
	Modeling metrology equipment and data extraction for enhancing model calibration accuracy and defect prediction, including for DSA
	Modeling lifetime effects of equipment and masks, including lens and mirror heating effects; mask deformation due to clamping and its impact on imaging and overlay
	Simulation of single and multi-beam e-beam lithography for mask making and wafer direct write applications, including proximity effects and compensation techniques
	Simulation next generation mask-less patterning techniques such as nano-imprint lithography, including post-exposure material processing effects
	Co-optimization of all variables within the exposure process, including source intensity distribution, polarization, mask (main and assist features), projection lens filters and aberrations as well as wave front properties
Nanoscale process modeling for new materials, technologies and architectures	Coupled diffusion/(de)activation/damage/stress models and parameters esp. for low-temperature in Si-based substrates
	Coupled diffusion/(de)activation/damage/stress models and parameters including low-temperature, SPER, millisecond processes in Ge-on-Si, III/V-on-Si (esp. InGaAs-on-Ge-on-Si), and ultra-thin body devices, taking into account possible anisotropy in thin layers
	Diffusion in nanometric thin layers and at/across abrupt/non-abrupt interfaces
	Diffusion of O, N, O vacancies, metal through advanced gate stacks
	Modeling of interface and dopant passivation by hydrogen or halogens from deposition/forming gas anneal
	Modeling the impact of front-end processing-induced damage to devices on their leakage, noise and reliability behavior during operation
	Morphology after deposition and etching of nanometric thin layers/pillars (metal and others)
	Process modeling for 2D materials (e.g. graphene, MoS2, BN, ..)
Nanoscale device modeling for novel devices	General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra
	Coupling traditional electronic models for memories with new state variables (e.g. spin, polarization, local material composition, phase state, mass density/mechanical stress, bonding arrangement, …)
	Models for gate stacks with ultra-thin/high-k dielectrics for relevant channel materials (e.g. Ge, SiGe, InGaAs, ...) w.r.t. electrical permittivity, built-in charges, influence on workfunction by interface interaction with metals, reliability, tunneling currents and carrier transport
	Modeling of salicide/silicon contact resistance predictive enough to allow for engineering (e.g. Fermi-level depinning to reduce Schottky barrier height; e.g. using DFT), including process dependency
	Advanced numerical device simulation models and their efficient usage for predicting and reproducing statistical fluctuations of structure , dopant and material variations in order to assess the impact of variations on statistics of device performance, including non-Gaussian distributions
	Physical models for novel channel materials, e.g., p-type Ge and compound III/V (esp. n-type InGaAs-on-Ge-on-Si) channels, esp. concerning thin layers, interfaces, defects and traps, …
	Accurate, robust and computational efficient modeling of wide bandgap devices

Table MS1 Modeling and Simulation Difficult Challenges

	Modeling for novel materials and stacks for thin film diodes
	Uni/bipolar two-terminal selector devices suitable for low temperature backend integration in memory technology
	Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation. Coupling between atomistic process and continuum or atomistic device simulation
	Statistical reliability modeling for ultimate CMOS and new memory devices, including tgeneration, nature and characteristics of traps
	Reliability modeling for HV MOS devices
	Modeling of drastic structural changes during operation, including operation-dependent thermo-mechanical stress
	Models for electron transport in ultra fine patterned interconnects
	Scalable compact models [1] for More-than-Moore devices including switches, filters, accelerometers, oscillators …
	Compact models [1] for new memory devices, such as PCM, and standardisation of models for III/V (esp. InGaAs-on-Ge-on-SI) devices
Modeling of chemical, thermomechanical, electrical and reliability properties of new materials including thin layers and stacked structures	Computational materials science tools to predict materials synthesis, structure, properties, process options, operating and reliability behavior for new materials applied in devices and interconnects, including especially for the following: 1) Layer stacks for gates, junctions and channels: Predictive modeling of dielectric constant, bulk polarization charge, ferroelectric/-magnetic properties, surface states, phase change, thermomechanical, optical properties, transport properties, reliability, breakdown, and leakage currents including band structure, phonon coupling, tunneling from process/materials and structure conditions, including impact of stress on various properties 2) Models for novel integrations in (3D) interconnects including data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties and stability of physical parameters (e.g. keff)
	Correlation of polymers/resist properties to the molecules size and impact at both process(litho) and device (roughness) scale
	Impact of microstructure, trapping at grain boundaries on transport on polycrystalline materials, in particular polysilicon channels used for TFTs and 3D memories
	Impact of microstructure and interfaces on the electrical properties of integrated interconnections metals
	Dielectrics properties and channel properties under high local electric field and strong non-homogeneous stress/strain fields, esp. with respect to reliability
	Dynamics of the transitions for device based on phase transition mechanism, esp. with respect to reliability
	Modeling of ALD layers depending on deposition equipment
Hierarchical simulation	Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3D and package: - possibly consisting of different technologies, - covering and combining different modelling and simulation levels as well as different simulation domains '- including manufacturability
	Efficient extraction of impact of equipment - and/or process induced variations on devices and circuits, using simulations
	Computer-efficient assessment of building block/circuit-level using process/device/circuit simulation, including process variations
	Computer-efficient inclusion of aging, reliability and variability at device level including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently
Multiphysics simulation	Model thermal-mechanical, thermodynamic and electrical properties of low κ, high κ, and conductors for efficient on-chip and off-chip incl. SIP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension
	Thermal modeling for 3D ICs and assessment of modeling and CAD tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keepout regions, …). Size effects (microstructure, surfaces, ...) and variability of thinned wafers
	Combined EM and drift diffusion simulation to include inductance effects in substrate caused by interconnects and bond wires
	Signal integrity modeling for 3D ICs
	Identify effects and apply/extend models which influence reliability of interconnects/packages incl. 3D integration (e.g., stress voiding, electromigration, fracture initiation, dielectric breakdown, piezoelectric effects)
	Modeling of electronic transport, heat generation and transfer, atomic migration driven by heat and field, spin
	Physical models and simulation tools to predict adhesion and fracture toughness on interconnect-relevant interfaces (homogeneous and heterogeneous), packages and die interfaces
	Mechanical stability of small features with high aspect ratio
	Impact of small sized features / thin layers on mechanical properties
	Dynamic simulation of mechanical problems of flexible substrates and packages

Table MS1 Modeling and Simulation Difficult Challenges

	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, fast and efficient optical interconnect models of larger domain
	Physical design tools for integrated electrical/optical systems
Difficult Challenges Beyond 2020	*Summary of Issues*
Modeling of properties of new materials integrated with device modeling and metrology	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating and reliability behavior for new materials applied in devices and interconnects, including especially for the following: 1) Modeling-assisted metrology: Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications 2) Use of such tools for accumulation of databases for semi-empirical computation 3) Better integration between material and device/interconnect modeling
	Modeling of materials for non-charge based devices beyond PCM / RRAM
	Flexible predictive first principles calculation processes for material screening
Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials	Ab-initio modeling tools for the development of novel nanostructure materials, processes and devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), deterministic doping and doping by chemical functionalization, quantum dots, atomic electronics, multiferroic materials and structures, materials for non-charge-based Beyond-CMOS devices)
	Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …). Modeling impact of geometry (esp. edge effects / edge roughness), interfaces and bias on transport for carbon-based nanoelectronics (carbon nanotubes and monollayer/bilayer graphene structures)
	Compact models for maturing emerging devices
Holistic and open common data set for all physical data relevant for modeling	Identification of basic physical parameters needed for predictive models at all levels, classified according to their impact on accuracy of simulation
	Extraction of realiable values for key physical parameters, based on selective experiments able to separate between parameters and/or reliable first-principle calculations
	Assessment of parameter accuracy and impact of extraction uncertaincy
	Parameters for advanced Si-based and non-Si-based materials
	Parameters for volume materials, thin layers, and two-dimensional structures
	Standardized format for data sets to be used with simulation tools from various sources
	Comprehensive open source data base available for use with tools of relevant vendors

Notes for Table MS1:
[1] In Compact Modeling no spatially resolved models are used. Approximately analytically solveable, physically based models give guidance for the used relations between electrical quantities. The goal is a description of device behavior (currents, charges, noise) in circuit simulators

Compared with the 2011/2012 ITRS, the Modeling and Simulation Difficult Challenges have considerably changed both in content and in structure: On one hand side, areas like Compact Modeling are no more considered as top-level Difficult Challenges but rather as very important requirements, with some specific aspects also showing up in the list of items of other Difficult Challenges. Second, due to the ever growing importance of Equivalent Scaling material aspects have got ever important also in the Modeling and Simulation Difficult Challenges, and are now especially addressed in one near-term and one long-term challenge on material modeling. Furthermore, the increasing diversity of the device architectures addressed in the ITRS has resulted in the inclusion of one near-term and one long-term challenge on device modeling. Besides this, the high importance and difficulty of hierarchical simulation, multiphysics simulation and data sets is now demonstrated by the inclusion of respective challenges in this chapter.

2.1. DIFFICULT CHALLENGES FOR 2013–2020

Lithography simulation including EUV—Various tricks have been introduced to extend the applicability of optical lithography to even smaller dimensions, with substantial support from lithography simulation. The further technological development also requires large additional improvements in the area of lithography simulation, among others because the number of available resolution enhancement techniques increases. Compared with the 2011/2012 ITRS, a few issues and details were removed from this challenge because they have either been met in the meantime or because they are now requirements but no more challenging. Overall, the challenge has been restructured, now spanning from defect issues through resist effects, special and new advanced patterning techniques, the link to metrology, lifetime effects and mask making to the co-optimization of various aspects which influence the quality of lithographically printed features. Especially, techniques which are prioritized for smaller feature sizes like spacer formation in multi-step patterning, co-optimization, or Directed Self Assembly are included in this challenge. If the models and capabilities requested by this challenge were developed, they would greatly expand the application area of lithography modeling. The lithography simulation challenge extends from feature scale to full chip, from equipment and mask effects to defect printing on the

wafer, and from prediction of nominal CD values and resist shapes to process windows, and lifetime effects of equipment and masks. It is being addressed below in the subchapter on Lithography Modeling.

Nanoscale process modeling for new materials, technologies and architectures—This is the key challenge for the prediction of result from device fabrication. Concerning its scope it is an extension from the 2011/2012 near-term challenge on "Front-end process modeling for nanometer structures" to include other process steps except for lithography which is addressed by a separate challenge as mentioned above. Several of the issues listed in the corresponding 2011/2012 challenge have been skipped in the 2013 issue, because they have in the meantime got at last partly available in commercial tools or changed their character from challenging to "only" required, On the other hand, the issue on "Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces" has been integrated into a separate near-term challenge on "Hierarchical simulation", together with several aspects from other areas of simulation. Most important and challenging in the area of process modeling is the modeling of ultra-shallow junction formation, which starts from very low energy implant and especially focuses on the thermal annealing and diffusion of dopants, and especially on activation and deactivation. Due to the strongly reduced thermal budgets needed for shallow junctions, that process is highly transient and is governed by the diffusion and reaction of dopant atoms and defects, and especially by the dynamics of clusters of these two. Implantation damage, amorphization, re-crystallization, and silicidation must be accurately simulated. Anisotropy in models and parameters potentially introduced by thin layers must be investigated. Already in the 2011/2012 ITRS, material priorities have changed due to choices made by the ERD and PIDS ITWGs: Material options to be simulated also include III/V-on-silicon, e.g. InGaAs-on-Ge-on-Si. Diffusion in nanometric thin layers and at/across abrupt and non-abrupt interfaces must be treated. To enable the simulation of device leakage, noise and reliability during operation process-induced damage must be modeled. In general, model development, calibration, and evaluation as well as process characterization require numerous experimental activities and large progress in the metrology for dopants, defects, and stress, especially regarding two- and three-dimensional measurements. Modeling of interface and dopant passivation from deposition and forming gas anneal has been added as well as the morphology of nanometric thin layers after deposition and etching. Furthermore, process modeling for 2D materials has been added. This challenge is being addressed below in the subchapter on Process Modeling.

Integrated modeling of equipment, materials, feature scale processes, and influences on devices—Variations of the results of a process step caused by the fabrication process and equipment used are key issues for manufacturability and yield of a technology. This refers especially to variations between neighboring devices or inhomogeneities across the wafer or between different wafers, and to drifts of process results between maintenance of equipment, for example, due to coating of chamber walls. Such variations are especially caused by lithography, plasma deposition and etching, chemical vapor deposition, electroplating, chemical mechanical polishing (CMP), or result from dopant fluctuations. The impact of equipment, process and/or pattern induced variations on devices and circuits must be assessed, which needs corresponding improvements of process and device simulation tools. Furthermore, also the effects of variations of consumables composition and quality must be included in the simulations. Generally, predictive simulation is still limited by lack of knowledge of the physical properties of materials and the chemical processes involved. The development of accurate models for reactions paths, the extraction of reliable values for the required parameters, and also the development of reduced chemistry models that include only the primary mechanisms needed for practical applications is an important challenge. For better linking with feature-scale simulation, surface chemistry and plasma-surface interactions must be appropriately modeled. Integrated equipment and feature scale simulation has become increasingly important for processes where a clear separation and interface between equipment- and feature-scale effects cannot be defined. Partly also the back-coupling from the wafer situation to the gas flows and reactions in the equipment must be included. A variety of deposition and removal processes must be modeled, as well as the properties of spin-on-dielectrics and wafer preparation and thinning in back-end processing. This challenge is being addressed below in the subchapter on Equipment/Feature Scale Modeling.

Nanoscale device modeling for novel devices —A fundamental question of the microelectronics industry continues to be what the ultimate limits of CMOS technology and devices are. The key subject addressed by this challenge is the predictive simulation of materials, processes, and device behavior including reliability. Material models are needed especially for gate-stacks including high-κ materials, for Ge or compound III/V channels, and for interconnects including size-dependent resistivity of copper and low-κ dielectrics. In this 2013 issue, the scope of this challenge has been extended to include wide bandgap devices and especially memory devices which utilize state variables different from charge. On the other hand, most material issues have been shifted to the material modeling challenges newly introduced. Furthermore, some challenging requirements for compact modeling have been included. Contact resistance is a key issue for scaling and requests appropriate modeling. Quantum-based and non-equilibrium (ballistic) device simulations are needed. Coupling between atomistic and continuum simulators is required. Simulations must also be applicable beyond standard planar CMOS. Generally, this challenge evolves in parallel to the prioritization of channel replacement materials

(e.g. InGaAs-on-Ge-on-Si) and device architectures by the ERD and PIDS ITWGs. Besides accuracy, efficiency and robustness are key issues. Both atomistic fluctuations and process-induced variations critically affect the manufacturability of the ultimate CMOS devices and must therefore be dealt with in simulation. This problem of variability crosscuts most of the subchapters below.

Modeling of chemical, thermomechanical, electrical and reliability properties of new materials including thin layers and stacked structures—Due to the ever growing importance of equivalent scaling which utilizes the properties of materials newly integrated, the importance of material modeling has strongly grown. In turn, in addition to a long-term challenge which has been updated compared to the 2011/2012 issue also this near-term challenge on material modeling has been included in the 2013 Modeling and Simulation chapter. New materials are required especially for gate stacks and interconnect structures. In consequence, equipment, process, device and compact models must be extended to include these new materials. Stress engineering must be enabled. Due to the short-term need, such material models may in part still be phenomenological rather than derived from first principles. This challenge crosscuts most of the subchapters below.

Hierarchical simulation—Various simulation approaches and levels, such as atomistic, continuum, and compact modeling, each have their advantages and drawbacks. These differences refer not only to the physical description employed but also to the simulation domains used in space and/or time, like for equipment, device, circuit, package, or system simulation. Nominal performance must be simulated at various levels, as well as its variation resulting from equipment effects, statistical effects, or aging e.g. due to operation. Obviously, the holistic inclusion of all these levels, approaches and effects in a tool which employs just one meshing strategy and resolution and one class of algorithms is neither possible nor desirable, because tailored algorithms and meshes are either requested to allow for efficient simulation or even to enable the treatment within acceptable memory usage, or convergence of algorithms at all.

Multiphysics simulation—Increasingly it has no more been sufficient to focus the simulation of a process step or of a device to one physical effect at a time, like the diffusion and reaction of oxygen during oxidation, or carrier transport in device modeling. Additional effects such as oxide flow and mechanical stress in oxidation, or the impact of mechanical stress on carrier mobilities already long ago became critical for the overall process results and device performance. Whereas such effects were years ago of secondary nature but needed nevertheless to be appropriately included to enable accurate simulation, several of them have in the meantime been actively used to optimize process results or device performance, such as stress engineering to improve transistor performance. In turn, several physical effects of completely different nature, such as carrier transport, mechanical stress, and thermal heating and flow, must be simulated in parallel and with comparable accuracy to yield appropriate simulation results. Besides the increased complexity and numerical effort caused by the increase of the number of equations to be solved in parallel, additional problems arise from the different space and time scales and from different requirements on meshing and discretization schemes caused by the various physical effects to considered. With novel materials and state variables different from charge being introduced, the challenge of this multiphysics simulation is becoming even more severe. Variations at all levels, size effects of material properties and various aging effects which affect reliability need to be appropriately described by physical models and furthermore add to the complexity which has to be mastered in multiphysics simulation. Increasingly, multiphysics simulation is required in most of the subchapters described below.

2.2. DIFFICULT CHALLENGES BEYOND 2020

Modeling of chemical, thermomechanical, and electrical properties of new materials— The introduction of new materials which are needed in technology development due to physical limits that otherwise would prevent further scaling can be expected to continue throughout the roadmap. Especially, computational material science tools need to be developed and applied to contribute to the assessment and selection of new materials in order to reduce the experimental effort, and to contribute to the databases required for semi-empirical calculations. Predictivity concerning the impact of material synthesis, structure, properties, process options, operating and moreover reliability behavior is absolutely needed. This refers especially to non-charged based devices beyond PCM/RRAM, whereas these latter ones need already to be studied in near term. Furthermore, modeling must assist metrology to enable the characterization of novel materials and devices. This challenge crosscuts most of the subchapters below.

Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials—Within the Emerging Research Devices chapter new device structures such as nanowires, carbon nanotubes, nanoribbons, quantum dots, molecular electronic, multiferroic materials and structures, and generally materials for non-charge-based beyond-CMOS devices are being discussed as good candidates to complement CMOS in the long-term. For the assessment and optimization of such devices and their fabrication technologies suitable process and device simulation tools must be developed, including e.g., deterministic doping, quantum transport, tunneling phenomena, and spin transport. The impact of geometries and interfaces is highly important for carbon-based electronics and must be simulated. Compared with the 2011/2012 ITRS, Beyond-CMOS device architectures which employ state variables different from charge have been partly transferred into a near-term challenge. In turn, this long-term challenge especially deals with nanowires and carbon-based electronics.

Holistic and open common data set for all physical data relevant for modeling—Accurate data for all relevant physical parameters is at the core for reliable and predictive simulation at all levels. Among others it must be avoided that different and contradictory values of such parameters are used when different simulation tools are employed in parallel or in sequence. First, it must be identified which truly physical—other than just phenomenological—parameters are needed for simulation at all levels. Here, it is especially important to assess how sensitive simulation results are to uncertainties of such parameters. In some cases it might be both very difficult and also not necessary to extract parameters separately, but just their combinations, such as for earlier models the diffusion coefficient and the equilibrium concentration of vacancies in silicon. Parameters required must be extracted either from selective experiments which are not influenced by other effects or by uncertainties of other parameters, or from reliable first-principle calculations which are themselves not affected by of fundamental parameters, models, or inaccuracies of calculation. This applies not only to advanced silicon-based materials but also to other material options including carbon-based ones. Especially, the frequent basic difference between volume materials/parameters and those for thin layers or even two-dimensional structures must be taken into account. The use of the same consolidated data sets within tools from different sources/vendors would be especially beneficial for industry. This would be facilitated by standardized data formats and especially by comprehensive open source data bases.

3. TECHNOLOGY REQUIREMENTS

3.1. CAPABILITIES AND ACCURACY REQUIREMENTS

Modeling and simulation encompasses a variety of applications with widely varying requirements. For example, in applications closely associated with design, speed and accuracy of phenomenological models are the primary requirements, while predictability in uncalibrated regimes is secondary. Examples are compact modeling and the lithography models built into OPC systems. In applications associated with technology development, the requirement may be considered a mixture of physically based models and calibrated/parameterized empirical models. Traditional TCAD applications, when used to optimize technology development (using highly calibrated simulators), fit this description. Finally, there are modeling areas in which the basic physics are being explored. Examples are Monte Carlo device simulators, or first principles calculations of diffusion parameters for dopant diffusion in silicon. To give useful guidance for all these application areas, tables for the Modeling and Simulation capabilities required in near-term and long-term have been included in this chapter. Refer to Table MS2a and MS2b. These follow an updated structure compared with the 2011/2012 ITRS and furthermore contain many important changes in the details. The table MS3 on the accuracy requirements included in the 2011/2012 chapter is not included here, but is planned to be updated for the 2014 issue. It should be stated, however, that there is an overall trend to require more predictive physical models that need less calibration. Moreover, integration between different process steps (which influence each other) and between feature- and equipment scale becomes more important and close, and makes it increasingly difficult to specify single items without taking others into consideration simultaneously.

The "Capabilities" requirements table (Table MS2a and b) is meant to describe the technology requirements for Modeling and Simulation that demand new features of modeling to be developed, or describe where existing models and tools are still largely unsatisfactory. An example would be the capability to model chemically amplified photoresists. In this case, the basic ability to simulate predictively the performance of such a nonlinear resist needs to be developed. This type of requirement is often tied either to the introduction of new technologies or to new regimes of physical phenomena at smaller dimension.

Table MS2a *Modeling and Simulation Technology Requirements: Capabilities—Near-term Years*

Table MS2b *Modeling and Simulation Technology Requirements: Capabilities—Long-term Years*

In the following paragraphs the needs for each of the eleven topical areas mentioned in the Scope are discussed in more detail. As mentioned above the areas "Materials Modeling," "Reliability Modeling," "TCAD for Design, Manufacturability and Yield," and "Numerical Methods and Interoperability of Tools" are crosscutting all the other areas. Therefore, in addition to being discussed in their specific sections, they are also mentioned in many of the other paragraphs.

3.2. EQUIPMENT / FEATURE SCALE MODELING

Equipment and feature-scale modeling involves simulation of reactor-scale effects such as geometry and extrinsic process variables like pressure, pad roughness, etc. in combination with pattern and feature-related effects, such as surface chemistry and local temperature variations, to accurately predict process results. So far feature scale simulation and equipment models have mostly been addressed separately in the context of multi-scale-length modeling with various approximations developed to link scales. The mission of equipment modeling is evolving in its scope and now includes unit process simulation (such as quantitative simulation of individual process steps) through to integration of hierarchical simulation levels and process steps. In this respect, the entire manufacturing life-cycle starting with the concept and feasibility and ending in continuous improvement will be increasingly impacted by equipment simulation that is based on fundamental phenomena and mechanisms. Many of these themes are being addressed concurrently within the various technical communities where there are logical interfaces. New efforts require multidisciplinary approaches and tight coupling to associated technical areas such as lithography, metrology, front-end TCAD, material sciences, mechanics, and *ab initio* computations methods.

Though the task of integrating the various disciplines into one comprehensive approach accounting for physics and chemistry on a microscopic level is formidable, it appears, in view of the skyrocketing cost of experimentation and in view of the multitude of variables, only prudent. Equipment design with the aid of computational electromagnetism and computational fluid dynamics including plasma and chemical reactions is becoming more significant. Analysis and design of nano-scale processes will be improved with modeling and simulation of chemical and surface reactions at the feature scale. The technological issues for the equipment / feature scale modeling are summarized below.

- *Data needs*

  The first-principles nature of the advanced process and equipment simulation requires a more comprehensive process characterization and fundamental data input both in terms of material and surface properties as well as in terms of parameters characterizing the underlying microscopic mechanisms. Although the algorithms for modeling of plasma etching seem to be mature, the capability of quantitative prediction strongly depends on the fundamental data of physical, chemical, and surface reactions. Since modeling for CVD process including PECVD has matured, however, as new materials are introduced for MOCVD process for example, fundamental chemical data for these materials are absolutely required. In terms of thermal processing like furnace, rapid thermal processing in the ball park of seconds and millisecond annealing comprehensive models based on chambers details predicting results on wafer level are often available at equipment companies. Therefore the simulation of pattern effects and light radiation on wafer level (e.g. temperature uniformity) are well understood but impacts on feature scale dimensions are fully neglected.

  In the realm of CVD and ALD the required data starts with the description of the precursors, species transport, bulk reactions, and surface interactions. Quantum chemistry tools are available to characterize most reactive systems. However, they are inadequate without streamlined computational approaches linking *ab initio* data to macroscopic models for a self-consistent simulation capability. The streamlining is also imperative to speed up the rate of

mechanism calibration. A good example is the required quantum chemical characterization of precursors used for high-κ dielectric deposition.

In plasma processes, electron impact cross-section and kinetic data for radicals, ions, dissociation fragments, and excited states are crucial ingredients for predictive simulation. Emphasis should be placed on realistic determination of dissociation pathways leading to important precursors. Judicious approximations will be required to characterize excited states of the species and product decay cascades. It is obvious that such data requirements will put a heavy burden on special experimental arrangements with clearly defined experimental boundary conditions and novel test vehicles (like calibrated sensors etc.) to provide viable model input data. Even if fundamental data and reaction path in plasma process could be accessed easily, it is inevitable that plasma modeling should take into account approximations with a reduced number of species, simplified chemistry, and no hydrodynamic effects because of the high computational costs. In order to capture fast and accurate diagnostics, more effective mesh generators, memory saving technology and field solvers, etc. need to be considered – see also the subchapter on "Numerical Methods and Interoperability of Tools" below.

The most neglected area in this regard is the lack of fundamental data for gas-surface or plasma-surface interactions (especially for photoresist, ULK materials, metal composites, and alloys). Since *ab-initio* approach to surface interaction requires too heavy computer resources, the experimental validation assisted by computational analysis is not only cost-effective but also indispensable for finding out the principal reaction mechanism. Another candidate is the employment of molecular dynamics. It should target metal alloys deposition processes for advanced metallization in interconnect and gate stack applications for MOSFETs. Specific needs include microscopic representation of metallic systems in terms of improved inter-atomic potentials and a microscopic representation of amorphous surfaces and doped films.

In the CMP arena, basic process characterization is poorly understood and more systematic and fundamental approaches to characterize these systems are required. Experimental data is needed to characterize the wear of polishing pads and conditioners as a function of process conditions, along with their dynamic impact on polish rates. In the case of electro-CMP, the adsorption/desorption behavior of slurry additives on the deposition surface and in the presence of an electric field is largely unknown, and their temporal decomposition characteristics in the bath poorly understood.

In addition to its importance in ECMP, electroplating would benefit from quantum chemistry calculations being extended to liquid systems, particularly in the presence of electro-magnetic fields. The modeling of electroless deposition with complex bath and surface chemistries for the deposition of CoWPM system materials has an especially strong need for fundamental quantum chemistry derived bath-kinetic and surface kinetic parameters.

- *Model validation and empirical model development*

  One of the major efforts required for better model validation is sensor development and metrology, especially for models predicting the fabrication and behavior of ultra-thin films and ultra-fine structures. Cost-effective verification of process chemistry models is needed. For CMP, measurements of the various physical parameters related to processes involving consumables such as polishing pads, conditioner disks, and slurries are at an immature state. For plasma, CVD and ALD models, surface process chemistry diagnostics such as pin hole experiments that characterize the transport of species to the wafer and through a facsimile of a feature need to be proliferated. Approaches whereby surfaces may be probed *ex situ* and returned to an *in situ* state in real time should be exploited for highly non-equilibrium processes. Standards of test structures (such as overhang cavity structures) and wafers dedicated to specific diagnostics such as temperature measurement are also needed for model calibration and process control. Enhanced capability real time FTIR, interferometry, and improved post-mortem diagnostics such as XPS and SIMS will be needed to validate coupled atomistic-scale to chamber-scale models of device fabrication.

  In addition, silicon lattice deformations are now systematically implemented as performance booster and stress management is required to stick with device specifications of advanced nodes. In that frame, a full bridge of the whole physics involved is mandatory: More precisely a deep knowledge on material rheology, stress relaxation phenomena and electrical transport features need to be introduced. Smart device management could be addressed by simulation, but dedicated models, calibration and experiments must be developed.

- *Feature scale simulation and integrated model development*

  Internal dynamic equipment settings or preconditions require a high degree of fidelity in the coupling between equipment chamber models and feature scale models. For example, the impact of chamber condition on feature evolution is a well-known phenomenon though a minimally researched topic. In the case of plasma processes

(including plasma ALD), particular attention needs to be paid minimizing numerical roughness for better resolution of the topography evolution of thin films. In general, new materials introduced at an ever more rapid pace at advanced technology generations entails inherently more complex process-surface material combinations and reactions. Specific experiments and an increasing reliance on atomistic simulation will be required to sort through the myriad processes on surfaces. Related aspects of plasma etching include line edge roughness (LER), gate profile control, process induced damage (PID), and maintenance of electrical and mechanical integrity (stress) of devices. Related aspects to oxidation (thermal or non-thermal) are growth on 3D structures (conformality) or atomic interface roughness for getting better electrical oxide quality.

Feature-scale models can often provide basic understanding of process details such as trench fill and etch residue effects, but the full benefit is often realized by integration with an associated equipment-scale model. Reactor-scale effects can often have a first order effect on feature-scale results and linking between atomistic feature-scale simulations and reactor-scale models needs to be standardized to help accommodate this linking.

Related to the feature/reactor linking problem are the problems of integration of models for various processes. Numerical infrastructure of process integration is complex and by no means standard. Communication between various unit process simulation tools (including layout tools) is of crucial importance. Specific opportunities exist in first-principles based tiling design and integration guided mask design. Models capturing process variations (lot-to-lot or tool-to-tool) present even a bigger challenge.

As double and "multi" patterning solutions continue to be a significant vehicle for extending Moore's Law, it is imperative to increase the predictive accuracy of etch models to the level of lithographic models. That would be an essential precursor to integrating lithography and etch models, required by multi-patterning. In the short-run, a practical solution might be to create phenomenological models that include both photoresist behavior and the end-results of the etch process; the long term solution must address the decoupling of such individual phenomena.

- *Multi-generation equipment / wafer model*

  Historically equipment models have been very module focused with various researchers using different solvers, discretization methods, and mesh generators. The area would benefit from standardization of these various components allowing the physics of the problem and boundary conditions to be the only focus. This has happened to some extent but an effort to move in the direction of a standardized workbench for physical model development could be beneficial for faster development of new module simulations as well as for smoother development of integrated models, as discussed above.

- *Emerging integrations*

  Rising constrains on core process developments implies to find alternative technology solution. Amongst options, wafer level packaging, die stacking and other integrations methods are adopted: Beyond shortening again the gap from Back-End to Front-End considerations, untypical materials and processes are entering in wafer fabs. Several concerns must be faced and fundamental options must be defined at an early development phase, thus simulation would be more than ever a crucial tool to prevent deadlock. A wide range of models must be developed to ensure acceptable time to market and wafer yield. Silicon thinning and back grinding, wafer bondings, through silicon connections induced stress, carrier conceptions, are examples of new fields for semiconductor modeling to consider.

3.3. LITHOGRAPHY MODELING

Lithography modeling and simulation needs have been sub-divided into six areas: 1) optical image modeling, 2) electromagnetic scattering analysis, 3) modeling of direct patterning techniques, 4) resist modeling, 5) integrated modeling systems, and 6) coupling of metrology and modeling. These areas are discussed below.

- *Optical image modeling*—More accurate, flexible, and efficient imaging models are needed for simulation su**p**port in the development of new process technology, e.g., multi- patterning. Advanced image models must cover all types of polarization effects such as spatial variation of polarization inside source and projector pupils, birefringence of lenses and mask blanks, the spatial variation of lens transmission, and polarization aberrations. For EUV lithography, high NA and innovative mask and illuminator designs that are able to address the requirements of high volume production tools pose extra modeling challenges. Additional polarization (variation) effects introduced at interfaces such as lens or mirror surfaces, mask backside, or mask pellicle need to be considered as well. Improved

simulation approaches are required to describe flare effects resulting from physically rough surfaces in lithographic imaging systems, where the different nature of EUV and optical flare needs to be reflected in the model.

Accurate image modeling including polarization and (polarization and wavelength dependent) aberration and apodization effects has become state of the art. Future model developments should be focused on the following topics:

- Efficient and realistic modeling of flare as induced by the mask and the projection system, especially for EUV, also taking pattern density on the mask into account across the entire exposure field
- Efficient and accurate modeling of light source characteristics and spatial coherence effects, e.g. laser-bandwidth effects; exploration of statistical effects such as speckle effects and photon noise, out-of-band radiation
- Critical evaluation of present models to cover exposure tool specific effects, such as variation of relative position of mask and wafer during scan, aberration averaging, geometric boundary conditions in the illumination and projection system defining or impacting the lithography process (e.g. shape of the exposure slit, field position dependent illumination angle, devices controlling internal reflections and flare, etc.)
- Improvement of the flexibility of the software to model various double exposure scenarios including interference assisted lithography (IAL) and to provide simulation support for complementary lithography
- Modeling of optical material properties (e.g. birefringence in mask and projection optics as well as inside the wafer stack), property changes under exposure, and the impact on the overall image formation
- Evaluation of Abbe versus Hopkins based singular value decomposition techniques, simulation infrastructure for effective source-mask-optimization
- Evaluation and optimization of EUV masks and EUV-multilayers for systems with NA > 0.3, off-axis illumination, and for EUV at a wavelength of 6.5nm
- Interaction of lens and mask induced aberration effects and their impact on Source-Mask-Pupil-Optimization SMPO
- Impact of pellicles on imaging performance; printability of pellicle defects (including EUV)
- Pattern specific wave front optimization to maximize process window
- Modeling of image border or field edge effects in EUV lithography, introduced by the residual reflectivity of the absorber material, causing CD variations in adjacent exposure fields on the wafer

- *Electromagnetic scattering analysis*—Electromagnetic scattering analysis has become part of the mainstream investigation capability. Scattering from topographic (even binary) masks and from wafer topography underlying more or less planarizing layers or resist are two examples of applications requiring rigorous electromagnetic capability. More efficient modeling techniques are needed for the critical evaluation and optimization of reticle-related optical resolution enhancements and for the description of light scattering from mask defects. The accuracy of approximate methods such as mask decomposition techniques, boundary layer models and filtering techniques must be evaluated over a wide range of lithographic process parameters. For EUV masks in particular, a fully rigorous treatment of the electromagnetic fields propagating through the reflective multi-layer sandwich structure or the absorber layer(s) and investigation of mask shadowing effects, especially for various OPC schemes, which may be needed for patterning at 16 nm and below, is required. The severity (or printability) of inherent multi-layer and absorber defects needs to be analyzed carefully, as well as the impact of defects or particles added on surfaces during handling. Simulation has to provide support for the evaluation and optimization and verification of defect repair or compensation, esp. OPC-like approaches for buried multilayer defects on EUV masks. Phase effects and mask induced aberrations (due to the finite thickness of the absorber and structured multi-layers) or incoherence effects (due to the finite size of the light source and the variation of the incidence angle across the exposure slit) and their impact on OPC and feature dependent variations of the best focus position need to be taken into account. With smaller mask structures, effects due to absorber roughness and their impact on line edge roughness (LER), top surface roughness, and wafer CD variation become more important. Accurate modeling of multiple exposure or other patterning techniques requires also an efficient modeling of wafer side scattering or wafer topography effects. Light scattering from the patterned hard mask and light induced modification the optical properties of bottom antireflective coatings (BARC) potentially impacts the performance of the BARC in the second lithography step of a litho-etch-litho-etch (LELE) process. Moreover, wafer topography effects may also have an impact on the OPC for

the second lithography step, depending on the details of the geometry and the resist system. General study of methods to address inverse problems in micro- and nano-optics: support of scatterometry, identification of required geometrical and material "corrections" for advanced OPC and for mask and wafer defects.

- *Direct pattering techniques*—Accurate and predictive modeling of direct patterning techniques such as e-beam direct write (EBDW) or Nano-Imprint is required in order to benchmark the lithographic performance against optical / immersion / EUV based processes. The modeling of EBWD applications should include exposure tool specific properties (e.g. single beam vs. multiple beams, low vs. high keV electron energies) as well as substrate specific effects (e.g. secondary electron generation and scattering / backscattering, stack and material dependencies in case of patterned substrates; charging; heating). Those effects are also relevant for the application of e-beam lithography in mask making, especially as proximity corrections are sensitive to underlying mask substrate, i. e. quartz or EUV multi-layers.

- *Resist modeling*—Predictive resist modeling will continue to be the bottleneck in lithography simulation. Accurate models for chemically amplified resists, which include solvent diffusion, post-apply bake, post-exposure bake, diffusion (of acid and quencher), line edge roughness, and surface interactions, are needed and must be capable of correctly predicting three-dimensional resist patterns, CD as well as cross section profile. Model extensions are required to improve the predictability of models for negative-tone resists and to describe immersion-specific effects such as leaching of different chemical species from the resist into or back from the immersion fluid. New process technologies such as double patterning might require materials with advanced properties such as non-linearity or reversible bleaching and multilayer resist systems, which need to be captured by the corresponding models. The accurate modeling of litho-process-litho-etch (LPLE) processes requires new model developments to describe the interaction between various resist and BARC layers and the modeling of freezing or curing processes, including associated volume effects such as resist sliming or swelling, which can significantly impact exposure latitude and process window. Thin and multilayer resist models that link the lithography to the etch process are becoming important, as well as specific development process models, for instance to describe techniques such as negative tone development or cover new materials such as developable BARCs or gradient BARCs. Photoresist patterns must be evaluated with respect to their 3D profile, etch resistance and mechanical stability. Because of the increasing importance of polymer-size effects, e.g., their impact on line edge roughness and line width variation, there is a growing need for resist studies based on mesoscopic models and/or computational molecular modeling and stochastic modeling. The modeling of the trade-off among LER, resolution, and sensitivity requires special attention. Predictive modeling of EUV resists requires the modeling of secondary electron effects and their impact on the lithographic performance.
  - *Some additional EUV topics:* Simulation models have to be extended and used to explore resolution limiting factors of EUV, including secondary electron blur, diffusion effects, pattern collapse and molecular statistics (LER). Early exploration of resist models for EUV at a wavelength of 6.5nm
  - Modeling of effects at the resist-substrate-interface, e.g. in the presence of under-layers (EUV), and their impact on process latitude and robustness
  - New resist materials: Accurate modeling of mixed versus polymer bound PAGs, molecular resists, nano-particle resists
  - Modeling of directed self-assembly: Bridging the gap between molecular dynamic modeling, coarse grained approaches and compact models for co-optimization of litho- and DSA processes

- *Integrated modeling systems*—For lithographic imaging close to the theoretical resolution limits, the interaction among different components of the lithographic system such as the illumination system, the mask, the projection system, and the resist over wafer topography becomes increasingly complex. With so many independent parameters, and an avalanche of data to understand, computer-based optimization systems are a requirement to fine-tune future technologies that will operate near the limit of diffraction optics. Specifically, this includes the optimization of mask and source parameters in optical resolution enhancement techniques and the ability to understand how the resist response influences these optimal parameters. It becomes more important to take 3D resist profile results into account in such optimization tasks, as the predictive power of contour based models is limited. New integration techniques like double patterning come along with additional etch, deposition, or planarization techniques that need to be considered in lithography simulation. The influence of underlying wafer topography must be understood and eventually taken into account. Integrated modeling systems are also required for extensive defect printability studies from the mask through the final product. New criteria and algorithms for the evaluation of lithographic processes

have to be evaluated. Especially the impact of varying input parameters such as illumination conditions, mask feature sizes, aberrations, resist thickness, PEB temperatures and others have to be taken into account. Further, as double exposure approaches become more popular, optimization becomes even more difficult and resource-consuming.

The link between lithography simulation and OPC application becomes more important: OPC model generation requires assistance by predictive, rigorous simulation models in order to generate accurate OPC models for the most advanced nodes within adequate time. Corresponding standardized interfaces between tools need to be provided. Finally, as double and "multi" patterning solutions continue to be a significant vehicle for extending Moore's Law, it is imperative to increase the predictive accuracy of etch models to the level of lithographic models. That would be an essential precursor to integrating lithography and etch models, required by multi-patterning. This has been noted also in the section focusing on equipment/feature scale modeling.

- *Model calibration: coupling of metrology and modeling*—Because some resist modeling parameters cannot be directly determined through experiments, efficient and standardized methods for the calibration of photoresist modeling parameters with experimental data (e.g. CD obtained by a Scanning Electron Microscope, cross sections obtained by an Atomic Force Microscope) have to be applied. More predictive process simulation requires a stronger connection between models and metrology tools. Methods have to be developed that translate the output of metrology tools into appropriate or corresponding simulation parameters and results. A more fundamental understanding about the generation of metrology data, eventually through simulation, is necessary to extract meaningful evaluation parameters from simulation results. Effects due to the measurement process itself need to be considered (e.g. resist slimming, or layout density effects), and corresponding correction have to be applied when comparing measured and simulated results. While aberration data for lenses and the measurement of illumination source shapes have become common, full polarization-specific characterization of sources and lenses is required. With the use of electromagnetic scattering simulations, accurate three-dimensional shapes and optical parametric descriptions of all mask materials are now required. Experimental schemes for the measurement of resist parameters, especially for 193 nm immersion and EUV, have to be devised or improved. Methods that are developed to simulate lithographic processes can also be used to evaluate metrology tools such as scatterometers and aerial image measurement systems (AIMS). For example, the coupling of measured AIMS data with a predictive resist model can enhance the predictability of AIMS based mask defect printability analysis. A link between experimental defect characterization (e.g. of a EUV multilayer defect) and rigorous simulation could be used to develop and validate possible correction or compensation schemes. Other applications are the modeling of wafer alignment signals to analyze the process impact on overlay, aberration measurement, and the extraction of resist modeling parameters from appropriate measurements.

  A standardized methodology for resist model parameter calibration is required to obtain a parameter set that allows predictive lithography process simulation. This includes a specification of experimentally derived input data (e.g. CDs for selected feature types, profile information such as resist height and sidewall angle, material properties as far as they can be determined experimentally), simulation setup, and metrology information, since the quality of the resist model strongly depends on the quality of the metrology data.

Besides the classical application areas of lithography simulation mentioned above, simulation activities in associated fields are becoming increasingly more important. Light sources are key drivers of any lithography technique; however, modeling related to their development, above all EUV source-related, should require particular attention, especially with respect to sources for high volume manufacturing.

The massive application of optical resolution enhancement techniques such as OPC, PSM, polarization, and off-axis illumination will increase the importance of lithography simulation for process development and optimization. The combination of well-planned experiments and predictive lithography simulation will help contain process development costs and accelerate the process development cycle.

3.4. PROCESS MODELING

Process modeling includes the simulation of the physical effects of manufacturing steps used to build integrated circuits. Traditionally the focus has been mostly in the front-end process (up to contact formation), since active devices were formed before metallization; however with the trend towards 3D device and 3D interconnects, novel memories integrated in the back-end process, and logic moving towards non-planar architectures or even heterogeneous integration, the whole process flow has to be modeled accurately and such traditional distinction is less relevant. At the same time advanced

devices tend to rely less on doping engineering and more on material engineering; therefore process modeling will need to be complemented by - and eventually integrated with - material modeling (please refer to the corresponding section) . Please also note that lithography simulation is discussed in a separate subchapter, see above. Synergy between lithography, process and material modeling is needed to understand and optimize device fabrication, to push the limits of traditional planar devices scaling, and to develop alternative device architectures. The modeling challenges in these areas are driven by the reduction of feature size and footprint, by the increasingly complex metrology of scaled and/or non-planar devices and by the pletora of new materials used to overcome scaling roadblocks. These not only cause higher demands on model accuracy, but also require models for effects previously considered as second order, or models of new materials as well as the introduction of new simulation techniques.

With the reducing thermal budget, accurate lateral doping and damage distributions need to be modeled. Monte Carlo implant models are definitely required for application that cannot be adequately addressed by analytic models, for example, doping of sidewalls of narrow trenches or fins, such as for the S/D extension of FinFETs, and generally for implants with complex layer stacks on a strongly non-planar topography. Modeling needs to be extended to include accurate damage accumulation and in-situ annealing kinetics during the ion implant process step and its dependence on temperature, fluence and beam scan, especially for "cocktail ion implant" and subsequent annealing process in silicon and silicon-related materials. Analytic models will need to be refined with respect to lateral dopant and damage distributions and to cover a large energy range from very low energy (less than 1 KeV) where the interface has a large contribution to high-energy (some MeV). Modeling of molecular implants and alternative doping processes such as solid source and plasma immersion ion implantation (PIII) is also required. For PIII of narrow structures with high feature scales, simulation of the energy and angle distributions of the ions extracted from the plasma may be necessary.

An optimum trade-off between minimized dopant diffusion and sufficient (maximized) dopant activation is key for the formation of shallow junctions and low device access resistance. In some technologies, a trade-off with leakage currents may be part of the objectives. Improved physical understanding of the related mechanisms is therefore directly important for technology development and also the prerequisite for any work on physical modeling. Continuum models for doping diffusion and activation need continued refinement to be able to adequately capture technologies with reduced thermal budgets and a wider range of impurity species, including the effect of the pre-amorphization techniques and subsequent recrystallization. Point-defect based diffusion models will need to be considerably refined especially concerning the kinetics of dopants and defects in clustering, activation, and deactivation during post-activation processes at elevated temperatures, in addition to capturing traditional transient enhanced diffusion effects. Also, the accuracy of the models for OED (oxidation-enhanced diffusion) during RTP (rapid thermal process) needs to be improved. An additional aspect to be considered and passed to device simulation is the formation of defect clusters in the space charge regions of pn junctions. Such clusters, comprising point defects, dopants and co-implanted species, may introduce levels in the band gap and cause detrimental leakage currents. With the trend to millisecond annealing schemes and beyond, the usage of appropriate temperature profiles becomes mandatory. On the other hand, this will be a problem especially for laser annealing where the spatial and temporal characterization of the temperature is challenging. The effect of interfaces, especially non-SiO_2 interfaces, is becoming increasingly important. Here, the segregation, trapping, and interface diffusion of impurities needs to be modeled for all kinds of silicides and dielectrics, including high-κ material stacks, taking into account the influence of N, C, F, Ge, metallic impurities and knock-on oxygen. Dopant redistribution during epitaxial growth and related snow-plough effects need to be predictively captured. Moreover, as the mechanical stress engineering plays a crucial role in the CMOS technology improvement roadmap, all these models for diffusion, clustering, and dopant activation must take into account the effect of the local mechanical stress. Dopant diffusion/activation models in alternative materials (such as SiGe, SiC, Ge and III-V materials like GaAs and InGaAs) need also to be improved, as well as those for very thin body (such as SOI) needed with or without any intrinsic mechanical stresses where interaction with interfaces is of first order.

Statistical modeling of grain orientation and size evolution during manufacturing is needed for polycrystalline materials (e.g. CMOS metal gates and polysilicon channel in 3D Flash).

Atomistic process models are playing an increasingly important role, both as direct simulation approaches for front-end processes (Kinetic Monte Carlo), and as a pathway to improved continuum model development and parameter extraction. Detailed insight into defects structure and energetics, dopants migration paths and dopant-defect interactions using *ab initio* methods will be needed for understanding the kinetics of reduced thermal budget processes and e.g. the role of other impurities such as fluorine, carbon, or germanium. Extreme diligence has to be exercised though to make sure that effects associated e.g. with too small cell sizes or the bandgap problem do not dominate the results. Computational materials science will also allow atomistic studies of new processes, materials, and interfaces, such as high-κ dielectric deposition and interface properties. Effective methods for bridging ab initio calculations to continuum models and to link process

and material modeling (please also refer to the corresponding section) still need to be developed and incorporated into mainstream TCAD flows.

As engineering of mechanical stress effects for device mobility improvement is becoming increasingly important, models for the effect of stress on reliability, dislocation generation, and dopant diffusion need to be developed. Stress resulting from all process steps including those coming from material texture modification and including stress generated by the presence of impurities, clusters and extended defects must be considered over the full range of temperatures used in processing and must be transferred to device simulation tools. Thin film growth needs to be better modeled, such as silicidation and radical-based oxidation, including the reliability impact of stress in corners and small 3D structures, as well as defect generation in such structures. Non-thermally grown dielectrics density and wet etch rate evolution (such as SOD or HARP densification) need to be described and coupled with mechanical stress. Implantation damage in dielectrics and its annealing kinetics should also be described both for accurate etch morphology prediction and for device reliability modeling.

For advanced gate stacks and alternative channel materials, modeling of high-κ dielectric film properties, interactions with substrates, and properties/ interactions with metal gates is a critical need to enable continued equivalent oxide thickness (EOT) scaling. Models should span from deposition conditions through geometrical shape of the gate stack and modifications during processes at elevated temperatures to structural properties such as crystallization, interface defect density for use in device simulation or for reliability issue such as the Bias Temperature Instability (BTI). In multilayer gate stacks the diffusion of different species needs to be modeled and linked to the work function (dipole charge) and traps density. Similarly nitridation of silicon dioxide should be predictively linked with interface charge for device simulation.

Feature-scale models for deposition and etching, including CMP, need to be linked to equipment simulation. This link will allow determination of the influence of equipment settings on feature topography as well as on inhomogeneities on the wafer and from wafer to wafer. This should also result in more physical feature scale models in particular for the last introduced deposition techniques such as MOCVD or ALD and for epitaxial growth of semiconductors and dielectrics. Modeling of these processes will become more critical as the industry moves beyond planar MOS to more complex device structures and 3-D integration schemes.

For each of these front-end modeling areas, approaches need to be developed to enable estimation of the performance impact of variation in critical front-end process steps. These include stochastic effects such as random dopant fluctuation and systematic effects such as within-wafer etch variation. Modeling these effects, along with lithography variations due to focus and dose variations, proximity effects and line edge roughness, is required for a better DFM strategy.

Brave new or improved metrology and analytical techniques are essential for the choice and calibration of accurate process models, especially tools for ultra shallow junctions, thin films and novel materials (or novel material interfaces).

3.5. DEVICE MODELING

Numerical device modeling refers in general to a suite of numerical models and methods describing carrier transport in materials. Models range from the simple drift diffusion, which solves Poisson and continuity equations, to more complex and CPU intensive ones as the energy balance, which solve some higher moment simplification of the Boltzmann equation. In addition, the complex physics of today's devices mandates at times the usage of Monte Carlo codes, which stochastically solve the Boltzmann equation, and the usage of Schrödinger solvers that account for quantum effects. The choice of the appropriate model depends on the problem and the level of details required and it is therefore left to the user. Despite the significant advances of recent years in both numerics and physics, continuous development is required to meet the increasingly challenging industry needs for device exploration and optimization. Device modeling is used for scaling studies and technology optimization; therefore, the ability to correctly represent today's performance and predict tomorrow's limitations is paramount. What follows is a review of the most outstanding limitations.

Gate stack—Gate dielectrics have become so thin that tunneling gate current is today an important design factor. Comprehensive quantum modeling of the entire gate stack (channel-dielectric-electrode) is needed to represent the behavior of oxides and nitrided-oxides that are only a few atomic layers thick. Following the widespread adoption of high-k dielectrics and metals, details of tunneling and charge transport in the dielectric, effective dielectric constants of complex dielectric stacks, interface states and dipoles, and charge and trap distribution in high-κ materials must be accurately described. Fundamental material modeling is required to aid in the search for alternative, high-κ gate dielectrics and their evaluation. The focus has to be especially on channel mobility but also on flat-band voltage shift and hysteresis effects by Fermi-level pinning and built-in charges caused by interface and oxide defects (e.g. P_b centers and

oxygen vacancies). Threshold and capacitance characteristics, as well as reliability issues are of topmost importance. Models for breakdown of gate dielectrics, including oxides, nitrided oxides and new dielectric materials, need to be available for simulations on various applications and dielectric reliability. Additionally TCAD models for dielectric degradation and trap evolution have to be provided (please also refer to the section on Reliability Modeling). Models for trap evolution at the dielectric-silicon interface have been suggested, but MOSFETs require improved modeling of trap evolution at long stress times to correctly predict variation of electrical characteristics.

Stress and strain—Different materials and layer stacks in source-drain and channel regions as well as volume expansion due to material reactions (e.g. oxidation or silicidation) or thermal mismatch during processing result in stress and strain fields that increasingly determine the device characteristics. In order to predict currents correctly for all possible channel orientations a full-tensorial description of arbitrary stress fields has to be included. Comprehensive models must include the effect on band-structure (band-edges, effective density-of-states and masses). The effects on Si and new material channel mobility are of paramount importance, especially the nonlinearities for GPa stress fields. They include anisotropic piezoresistivity (caused mostly by stress dependence of the effective masses and momentum relaxation times), as well as stress induced changes of effective saturation velocity.

Contact resistance—With shrinking device dimensions, the contact resistance contribution to the total device resistance will increase and thus will play a more important role in predictive simulation of the current-voltage characteristics and transconductance. A correct modeling of salicide/silicon contact and silicon sheet resistance (high doping activation and mobility) is a prerequisite for a correct device description and to enable contact engineering (e.g., by Fermi-level depinning reducing Schottky barrier height).

3D modeling—Especially for narrow devices (e.g., Flash or SRAM memory and logic cells) and FinFETs using strain for mobility enhancement the coupling among the various spatial directions requires a full three-dimensional device modeling taking into account realistic 3D geometries and doping distributions. Effects such as gate line edge roughness or width dependence greatly impact devices output characteristics and they need to be taken into account during device optimization studies. This implies that 3D simulations are no longer reserved for occasional, limited use but are a real need for everyday tasks. Therefore, device editors productively coupled to process emulators and simulators, meshing algorithms and solvers have to be enhanced to the point that 3D tools have complexity and computational requirements similar to 2D.

Dopant, geometric and structural fluctuations—Ever shrinking geometries have created a singular problem unlike any other: Because of the small volumes involved modest random fluctuations of implanted dopants will give rise to considerable differences in local doping concentration, which in turn will have a tremendous impact on devices characteristics. Similar effects arise from fluctuations in trap concentrations, poly or metal grains size in the gate, as well as of gate dielectric and UTB (Ultra-Thin Body)-SOI silicon layer thickness. Such fluctuations will broaden the device parameters distribution and will therefore need to be taken into account for any optimization or manufacturability study. In this regime, each single device type will have to be represented by an entire distribution of individual devices with random doping concentration (producible, for example, via Monte Carlo methods) and preferably in 3D, which re-emphasizes the need for fast 3D simulators. An efficient, suitable description of this distribution with accurate results for the tails is mandatory for assessments of key figures of merit like SRAM noise margin, Flash Read Window Budget, etc.

RF—Development of bipolar specific models lags behind that of models aimed at conventional CMOS scaling despite being as much or possibly more necessary. Consequently, support of RF, analog and mixed-signal CMOS, BiCMOS, and bipolar circuit design requires enhancements, especially in the numerical treatment of small signal analysis (AC) and large signal transient behavior . Efficient tools are needed to analyze device performance, to characterize non-quasistatic effects, to minimize the requirement for time- and cost intensive RF measurements and to provide predictive data in the downscaled regime. Comprehensive internal noise modeling must cover all the important internal noise sources from the sub-kHz up to at least the 100-GHz regime and include 1/f- and RTS-noise. Efficient models for substrate noise coupling have to be provided to couple comprehensive descriptions of external noise sources to the transport equations in a flexible way. Finally, self-heating of devices and circuits and frequency dependency of physical parameters must be taken into account. An accurate modeling of gate RC propagation delay is extremely important for RF-CMOS.

CMOS scaling—Novel device architectures and ultimate CMOS scaling require more rigorous modeling. Channel lengths or silicon films of a few nanometers cannot be accurately represented without partially ballistic transport models, which also include quantum effects related to the electronic band structure and phonon spectra. Several approaches have been suggested so far, but they partially lack rigorous justifications in their approximations or are prohibitively computational intensive. Simpler schemes are based on self-consistent Poisson-Schrödinger equations, whereas more advanced methods exploit Green's or Wigner's functions to solve the Wigner transport equation, the Kadanoff-Baym equation, or the many-

particle quantum Liouville equation. Of special importance are a consistent mobility model for the modified local density approximation (MLDA) and the density gradient model. With transport engineered devices (exploiting optimized stress and channel orientation combinations) becoming mainstream and the introduction of novel gate stacks these topics are of central importance. For the industrial user it is of paramount importance that the related algorithms are computationally efficient, robust and numerically accurate.

Novel logic devices—In recent years, a large variety of novel device architectures has been proposed, including extensions to the conventional CMOS FET channel, as well as devices beyond conventional FETs. For CMOS FET extension, a promising method to suppress the short-channel effect exploits thin films. Therefore, fully-depleted ultra-thin body SOI, multiple-gate FETs, 1-D structures such as nanowires, and various forms of double-gate or surround-gate structures, including FinFETs, have been investigated. For these structures the partially ballistic and quantum transport models discussed above are as indispensable as comprehensive mobility models for arbitrary channel directions. Additional device features being exploited include novel gate stacks, non-planar or elevated S/D structures, transport engineered devices with strained Si, SiGe, Si:C or Ge, or even hybrid substrates enabling III/V materials on silicon, for which a correct and comprehensive description of stress and strain effects, morphology, band-structure and defects/traps becomes an essential requirement. Among the most promising candidates for novel channel materials enhancing mobilities are GaAs or InGaAs layers for nFET and Ge layers for pFET. Self heating will be important especially for devices fabricated on SOI wafers or using layers containing Ge or Ge substrate. Emerging logic technologies beyond CMOS may exploit physics such as collective spin, ionic transport, or electromechanical effects that must be captured in modeling and simulation tools. Therefore, such devices require the modeling of spin, magnetic interaction, and electrical polarization phenomena

Novel memory devices—Similarly, emerging memory technologies (such as are STT-MRAM, PCM and RRAM) may employ materials that are magnetic, paramagnetic, ferroelectric, or that undergo phase transitions during device operation. For RRAM a local (filamentary) or distributed (bulk) drastic change of material properties has to be described as a result of several microscopic phenomena, such as ionic or neutral species migration, chemical reduction/oxidation reactions, or agglomeration of structural defects. A particularly challenging requirement is that such structural changes occur dynamically during device operation: Thus a self-consistent treatment is required, coupling physical effects traditionally present separately in either process or device simulation. Similarly for PCM it is mandatory to self-consistently model self-heating and phase transitions (including crystal nucleation and growth). Besides traditional state variables new ones need to be introduced describing the time and space dependence of local composition, phase state, and mass density (and/or mechanical stress). Several novel memory devices critically depend on transport or trapping in poly-crystalline or amorphous materials; appropriate modeling requires a consistent treatment of the effect of localized and extended electronic states.

Modeling requirements for novel devices—For all novel devices, in particular when atomic migration is involved, reliability modeling becomes increasingly important. Commercially-available tools will be required in order to enable the development of emerging research devices, as well as the related materials and processes. Such tools will need to include the physical effects already mentioned and also the impact of geometry and interfaces. They have to be efficient to enable the design and evaluation of devices and architectures beyond traditional planar CMOS or conventional memories.

Miscellaneous—Good progress was made in the last decade for the modeling of substrate current and hot carrier injection effects. Monte Carlo and spherical harmonics-based solutions of the Boltzmann transport equation have allowed a detailed understanding of the generation and dynamics of hot carriers. However, scaled devices require further development, especially concerning multi-subband transport, space dependent band structures and transport in thin dielectric layers (for instance injection, ballistic transport, trapping and detrapping in nitride, high-k, or hybrid metal gate floating gate memories). Highly demanded degradation and reliability analysis relies on similar models taking into account a structural modification during device operations due e.g., to hydrogen or metallic ions migration, trap states creation/transformation, or stress induced voiding. Prediction of reliability under steady state and transient conditions or ESD has become an important aspect of the technology scaling analysis. Unfortunately, only post-processing or empiric models are available. For low power devices, the junction leakage current due primarily to band-to-band and trap-assisted generation seriously limits the process window. Non-local tunneling models supporting tunneling through individual traps are needed to statistically model junction leakage for DRAM and SILC for Flash data retention . To address design for manufacturability issues representation of devices variability (doping, gate line width etc.) has to be developed and interfaced to circuit design. Simulation for large area devices also needs to be explored. Power amplifiers or optical devices are usually built from many transistor cells connected together through a huge interconnect system. The impact of distribution effects on device parameters is not well understood and modeled, especially when thermal and electromagnetic effects are at play. Large signal behavior would be required but traditional TCAD is prohibitive because

of the number of grid points necessary to discretize the whole system. A correct treatment of the physical effects of individual dopant atoms and traps (including single trap giant RTN) in commercial continuum and Monte Carlo device simulators becomes increasingly important.

3.6. INTERCONNECTS AND INTEGRATED PASSIVES MODELING

Interconnects continue to play an important role as a limiting factor for staying in pace with Moore's law to double the transistor and interconnect densities every 2 years. This refers both to their electrical performance and to their reliability, and in turn requires coupled electrical, mechanical, and thermal simulation. Concerning reliability, electromigration, stress voiding and extrusion are most important aspects, as well as Time Dependent Dielectric Breakdown (TDDB) for dielectric, but also initiation and propagation of cracks and delamination. Both electrical performance and reliability are critically influenced by process conditions and material properties including the microstructure of copper and (porous) low-κ materials. Performance and reliability critically depend on design, but with further shrinking distances and cross sections the deviations from ideal structures resulting from real fabrication processes is another important factor. Similar to front-end technology, modeling has to cover material properties, fabrication process and then the modeling of the performance and reliability of interconnects. Moreover the need for simulation at the scale of LER and critical dimensions also increases especially for thermal and mechanical topics (for electrical it is required already for quite some time).

As the operation speed of devices is increasing to the multiple GHz range and the complexity of interconnect systems continuously increases in particular by the introduction of 3-D die integration scheme like TSV and TMV, software tools with higher accuracy and better efficiency become necessary. The ability to predict the electrical and parasitic properties of complex interconnect structures continues to be a challenge. Software tools and methodologies that link process results to results at the IC level, that identify reliability issues or design deficiencies, that give the designer capabilities to explore alternative interconnects easily are needed.

In addition to the aforementioned front-end concerns, specific technology trends imply to enlarge process ranges involved. More precisely, since novel integration solutions are developed in order to support specification targets, the failure modes observed in interconnects are now moving into a larger scale. Indeed, unit parts used to ensure the electrical connection between transistor and assembly board is becoming shorter, and the whole yield loss contributors, such as mechanical, thermo mechanical, thermal and material flows need to be rethought.

Potential solutions exist, but all these solutions need further development for being suitable to a day-by-day use in the design flow. The potential for the advanced modeling of the electrical performance falls in two categories:

- First, if the semiconductor substrate is high resistive, then the electromagnetic response can be captured in linear dependencies. In that case the substrate can be treated as a low conductive medium that is characterized by its conductivity and permittivity. Numerous modeling approaches are available that are based on a full wave approach. The method-of-moments (MoM) and the partial-element-equivalent-circuit (PEEC) method are pursued as a valuable scheme to simulate the electromagnetic environment. The finite-difference-time-domain method is also pursued for characterized interconnects and integrated passives in the high-frequency regime.
- The second category deals with the situation that the substrate is fully taken into account as a semiconductor, thereby responding in a non-linear manner to electromagnetic fields. Moreover, a second non-linearity is induced by the fact that the field-source dependency needs to be addressed self-consistently. Some attempts have been presented that considers the self-consistent coupling of the Maxwell equations to the semiconductor device equations. The feasibility of the solution is demonstrated, however in order to convert this solution into a practical tool, a series of developments are still required. Reduced-order modeling techniques have high potential and deserve to be further developed and explored.

All full wave solutions suffer from a severe computational burden to extract the electrical behavior of lines over 100 nm to 1 cm length scales without increasing the complexity of the problem. A typical simulation of the electromagnetic behavior requires an about ten-fold larger set of node variables to be solved as compared to a steady-state simulation. Due to the dynamic character, the vector potential for the magnetic field must be included. In order to deal with the frequency dependence both the phases and amplitudes of the variables need to be stored. Therefore, fast linear solvers play a key-role in implementing full wave solutions in the design flow.

Besides the demand to understand in sufficient detail these high-frequency effects, an increasing need is to simulate integrated passive elements. In order to characterize these passive elements it is needed to simulate these components in realistic circumstances. The modeling of these passive elements must include the variability due to layout configuration as

well as local variation such as LER, texture, roughness, shapes and others. Furthermore as the current density is increasing in metal line and via as well as the electric field in dielectric, reliability modeling is required. Realistic use case scenarios must be defined and applied to such a simulation due to the lower and lower margin to failure. This aspect is a generic trend in future IC design.

Of high priority are the coupled thermal and mechanical performance properties of thin multi-layer films. Structural and compositional properties of thin films need to be obtained and related to reliability effects not only for thin multi-layer films but also for thin multi-layer films patterned for critical dimensions. The mechanical properties of these thin films, such as fatigue, fracture, and stress voiding, also affect reliability performance. Thermal cycling can trigger fractures that may not be foreseen.

An important reliability risk factor is residual stresses in multi-layer thin films. Each thermal process causes microstructural transformation of metal films which in turn induces residual stresses. Modeling of mechanisms of grain growth and transformation will improve understanding of entire stress budget in thin films which influences nucleation and propagation of cracks.

Simulation tools are needed to study these effects more effectively than by experiment alone. The interplay with equipment and feature scale simulation becomes an increasingly important factor for being successful. The change to low-κ dielectrics with low thermal conductivity has placed much more emphasis on combined electrical and thermal modeling in the suite of modeling and simulation tools needed for interconnect technology development.

For many of these topics a comprehensive and validated database of material properties is essential. It should be accompanied by accurate fundamental material modeling which has to cover mechanical (stiffness tensor, critical quantities for crack and delamination initiation, mass density), thermal (conductivity, specific heat capacity, density) and electrical properties (dielectric permittivity, etc.) and their mutual dependence like temperature dependence of mechanical properties, density dependence of dielectric permittivity etc. Even more important for many mechanical reliability issues is a predictive modeling of the stress/strain field after manufacturing which is very challenging for modeling of fabrication processes.

With respect to 3D integration the impact of TSVs on front-end device characteristics due to surrounding strain field is one of the most important sources of systematic variations of these devices. Moreover it adds another aspect to the more general but increasingly important topic of chip-package interactions of all kinds. Mismatch concerning the coefficient of thermal expansion of various materials causes thermal ramps and cycles to be important sources for mechanical stress. They appear during various fabrication steps (soldering) or during operations and can cause mechanical fatigue or failures. Many issues can be looked in detail only by spanning from cm-scale packaged chips down to nm-scale interconnect feature size. Virtual homogenized materials the parameters of which have to be determined by appropriately averaging of constituent materials and their relative abundance in the different layers of the interconnect stack are required on large scale models. On smaller scales layout information is essential also for tools addressing mechanical and thermal questions.

Modeling can definitely address these concerns, particularly thanks to the increasing capabilities of numerical tools. However, new physical phenomena might be expected and included in simulations:

- Delamination occurrences have drastically increased following low-κ integration. Brittle fractures, located at interfaces, cannot be addressed anymore with commonly used stress based analyses. Tools must be enhanced to better support fracture mechanics, such as energy based ones. On the other hand, on top of numerical issues, novel failure analysis techniques are enabled for correlation purpose. This is particularly true for fracture mechanics, for which the understanding remains one of the bottleneck. In that frame, three dimensional views of the crack features, in situ non-destructive observation and tracking of the delamination propagation will bring crucial insights for failure criteria development. Finally, despite the facts that putting thresholds and quantitative values in that kind of mechanisms is still tricky, progress have been recently observed and will allow to acquire more predictive models.
- As for the need to define worst cases of test structures and ensure that experimental reliability results indeed correspond to real life conditions of devices, the electromigration related issues must be simulated. As the size reduction leads to increase the influence of interfaces, hence both bulk and surface mechanisms must be considered and calibrated.
- Even in thermo-mechanical induced stress, critical dimension reduction also tends to invalidate the commonly used bulk approaches in material models: For example, microstructural effects in copper lines, or pore effects in dielectrics will became a dominant factor. Multiscale and multi-physics simulation must be precisely carried out to bridge these scales.

- For the physically and microstructural small cracks, the classical continuum mechanics concept may not be appropriate anymore and micromechanics treatment of the material at the microscopic material scales would be more favorable.

With respect of fabrication processes for low-k dielectrics the following modeling topics are required.

- effect of deposition and processing conditions on
  - bonding
  - structure
- effect of plasma etch on
  - bonding
  - adhesion
- effect of plasma etch, composition, bulk and interface structure and bonding on
  - dielectric permittivity
  - elastic moduli
  - hydrophobicity
  - inhomogeneousity

The diffusion of Cu through thin film Cu barriers should be modeled especially with respect to thin film effects.

Interconnect performance simulation is getting especially difficult because the problem widely spans in four respects, as follows:

1. An increased coupling of electrical and thermal-mechanical simulation is necessary.
2. The final target is performance and reliability at least at chip level. However, with shrinking dimensions and increasing aspect ratios this is more and more influenced by process details leading to deviations from ideal interconnect shapes, the problem spans from few Angstroms to several mm.
3. In the end details on feature level as well as the physical effects discussed above increasingly influence the performance of the actual design. In turn, the various levels of interconnect simulation need suitably to be coupled with design in a bi-directional manner.
4. Simultaneous simulation of interconnects and packaging is mandatory especially in case of multi-die integration scheme both on the mechanical/thermal aspects as well as for the electrical performance behavior.

Strong coupling exists between thermo-mechanical stress and its influence on carrier transport in devices. Therefore, the need for including self-consistent simulation methodologies to model these effects at device level is critical for TSV and other 3D interconnect technologies. Design rules related to keep-out-zones (KOZ) are needed to optimize layout efficiency without compromises to device performance. Modeling tools can be useful to formulate these rules and to validate them through electrical characterization.

Process modeling of TSV and related 3DI technology is critical to understand the evolution of high aspect ratio structures, impact on adjacent active area, including stress profiles and their evolution, defect propagation and their influence. Coupled “dopant-defect” diffusion characteristics impact device leakage as well as switching performance due to parasitic depletion capacitance near trenches. Predictive modeling of these phenomena should start with robust modeling of the fabrication process.

Integration of passive elements such as on-chip inductors, capacitors and resistors require detailed modeling along with parasitic elements. Self-consistent modeling should include bias-dependent parasitic components due to semiconductor junctions in contact with or in close proximity with interconnects.

In the context of emerging research materials graphene interconnect are one possible option. For them the effects of contact size, interface materials and process conditions on contact resistance as well as edge related effects (roughness and passivation) on conductance are important modeling topics. For very small sizes the transition to ballistic transport regimes and scattering on various interfaces only has to be modeled.

Certainly the modeling of carbon nano tubes (CNT) is also an important aspect for emerging research materials. Not only modeling of their electrical properties is important but also simulation of the effect of catalyst and growth conditions on the growth direction, structure and properties of CNTs.

Moreover, novel interconnect scheme should be designed jointly by technology people and CAD people. In the near time, the CAD flow will include both software management and embedded sensors to drive product working, stay below critical temperature or stress threshold, and hence optimize life time.

To solve these issues hierarchical simulation methodologies and tools must be developed to take best advantage from each other.

3.7. COMPACT MODELING

An important task for circuit element modeling (referred here as "SPICE/Compact models") is to achieve concurrent device/circuit development, dealing with the increasing amount and intensity of interactions between process, layout, and device extrinsic and circuit level parasitics.

Accurate modeling of circuit behavior, including parasitics, is crucial for first-time-right designs. Physically influenced compact models strongly enhance the predictability for future technologies. The models should take into account statistics and variations of the processing, including aging, reliability and statistical correlations for feasibility of manufacturability. These models should be available long before process qualification. This enables chip design before technology release, enabling a fast product ramp-up once the technology is qualified.

Compact models for circuit simulation are key to chip design productivity. Many design challenges can be found in the *Design chapter*. Examples are the increase of clock frequency, the decrease of supply voltage, the increased importance of weak inversion, and the exponential increase of the circuit complexity in order to predict accurately power dynamic performance and power static leakage at system level. Model accuracy and CPU efficiency are two opposing requirements leading to a hierarchy of models. The most accurate models are used to simulate small circuits. Less accurate models are derived to simulate larger circuits, and so forth. Similarly, this dichotomy implies a hierarchy of models at several structural levels - device level, cell level, and block level.

Historically analog simulation needs have driven the development of compact models. Both analog and digital designers then use these models. The increasing number of (analog and digital) devices per chip requires faster models and improved convergence in the simulation tools. Device models will include many more detailed effects. Parasitic effects, like series resistance, inductance and capacitance, as well as leakage, noise, distortion and non-quasi-static effects have become of more importance. Furthermore variability at local level or at global level resulting from layout configuration must be accurately included as variation becomes more and more important as the dimension of the devices decreases. Robust and accurate parameter extraction algorithms are essential for each model.

CMOS devices—Compact models for future CMOS generations should model new effects correctly with a high accuracy to have good predictability at design level. Examples are multigate high mobility channel materials and high-κ metal gate stacks. State of the art MOS models are based on surface-potential based modeling, which provides a simple connection from the device simulation to the circuit simulation. It enables reduction of model parameters resulting in fast parameter extraction and easy inclusion of variability and statistics. For some applications longer-channel devices are used at high frequencies, making non-quasi-static models essential. For analog and RF applications the modeling of excess noise and distortion will need attention as well as Random Telegraph noise in the temporal domain. A strong request is that RF (noise) measurements are undesirable and compact models can predict noise without extra parameter extraction. Due to new effects, models will become more complex. In combination with the ever increasing circuit sizes care must be taken to limit calculation times, e.g., by developing 'fast models' (fast versions of the full model) or using look-up tables. Given the small dimensions, variability and statistics will be more prominent is this class of devices. Local variations will become more important than global variations for these generations. These effects have to be implemented in compact models for further propagation in the hierarchical modeling chain approach. A consistent treatment of local and global variations is required to allow for a computer-efficient inclusion of statistics in circuit simulations, preferably before process freeze.

Non-CMOS devices—For non-CMOS devices, the number of options in the PIDS chapter is still very large, requiring huge efforts in the modeling domain. For bipolar devices, models will be extended towards extreme HBTs, either in SiGe(C) or in III-V materials. For memories models are needed for new memory concepts like RRAM, FRAM, MRAM, and phase-change, as mentioned in the PIDS chapter. The probability of switching between two or more states in such advanced memory cells has to be introduced and properly handled by the whole simulation chain. Even for advanced discrete products, e.g., RF-power devices, dedicated model challenges exist to deal with thermal effects and interactions.

Reliability—Predictive DC and RF reliability simulation will be more important as more designs will be close to the hard reliability limits. Predictive circuit-level simulation, based on device level compact models, is essential to guarantee safe chip-design. The compact models should be able to statistically capture the dynamics of degradation and recovery. In addition, the prediction of electromigration from interconnect layout needs improvements to avoid overly pessimistic margins as well as the ones related to Time Dependent Dielectric Breakdown in dielectrics (TDDB).

RF—The circuit modeling for RF will extend to the 100 GHz range where third harmonic distortion is still important. Models for scalable active and passive devices, such as inductors, transmission lines, varactors and interconnects, including their parasitic elements, are crucial for good RF circuit modeling. For several larger (active or passive) elements the non-quasi-static effects will be significant and should be modeled accurately. To support heterogeneous integration, CAD-tools must handle multiple interactions between circuit models, building block models, interconnect, dies and packages.

Interconnect—The importance of interconnect modeling increases with the stronger contribution to circuit delays and cross talk. The complexity and the size of the interconnect network poses serious challenges. Different applications need models for different effects, like cross talk, matching, inductive coupling (also in 3D), skin effects, and size effects (see the *Interconnect* chapter). A hierarchical interconnect simulation approach is necessary to keep simulation times reasonable. Accurate proximity parasitic elements at the device level from Parasitic Extraction (PEX) tools must be introduced in netlist and in particular an accurate Middle Of Line parasitics computation for pre/post layout compatibility. For RF applications full wave description of interconnect devices, like transmission lines and antennas, will be common for high speed or high frequencies. If the full-wave description of interconnect gets important beyond the device level, serious efforts are needed on complexity reduction algorithms.

Interaction between elements—Increased integration density causes non-negligible interactions between neighboring devices. This must be modeled on the basis of the layout of a circuit. Three-dimensional parasitic effects such as fringing effects may strongly influence RF circuit performances. In large circuits even long-range effects will gain in importance. Examples are the substrate-coupling effects, e.g., a digital clock signal that propagates to the analog and RF parts and disturb their specifications. Self-heating effects will get more important with scaling for the FinFETs and nano-wires. Hence, self-heating and mutual heating and cooling effects should be modeled in more detail over the full chip. For RF applications, large-scale electromagnetic field effects will gain in importance. This should be taken into account beyond the device level on the circuit level. An efficient simulation methodology is key for this task.

3.8. PACKAGE SIMULATION

IC-package co-design is a key crosscut issue with system-level considerations becoming increasingly important. In the past a package designer might have been presented with the die footprint including the placement of the die I/O pads as well as the placement of the I/O connections to the printed circuit board (PCB). With increasing pin counts and overall size constraints this practice often results in packages that are unreasonably expensive or that cannot be manufactured. Beyond being routable and manufacturable, a package must meet demanding requirements with respect to signal integrity, power, temperature, and mechanical integrity. The required integrated electrical, thermal, and mechanical simulations must be performed with consideration of the die and the system which always gain in complexity with the increase of the integration density and the introduction of 3D integration schemes, and this is possible only with communication enabled by co-design tools. A properly designed co-design tool will interact directly with both the package and die databases and have the capability of communicating results between the two.

The more common package models today are lumped discrete models based on IBIS and SPEF specifications or compatible to SPICE. There will continue to be demand for such models due to their simplicity and speed of simulation. In the near term these simple models need to be improved to describe the package better. SPEF models are appropriate for the IC when the self-inductance of small short connections is important, but the absence of large current loops renders mutual inductance negligible. In a package with relatively long traces, large current loops, and bond wires, mutual inductance can be extremely important, and it is becoming more important in the IC. IBIS models describe the cross-coupling well, but all die pins on a given package net are generally shorted together, significantly limiting the possibilities for simulation. Neither of these formats properly addresses power and ground issues. With SPICE one can build more complex models of the ground and power structures, but the models tend to be cumbersome and slow.

Modeling of power and ground structures in the package is extremely important. I.R-drop due to current bottlenecks, noise, and simultaneous switching issues are critically important with repercussions for thermal analysis. It is difficult to

ascertain if enough decoupling capacitors have been placed in the correct places to guarantee performance, or perhaps too many have been added, thereby negatively impacting cost and package size.

There is a clear need to move beyond models based upon discrete elements to distributed and transmission line models. In simple packages there may be very limited power and ground structures, while in a typical ball grid array (BGA) package only half of a given trace may cross a ground plane. In a more complex flip-chip design there may be many ground and power planes on alternating layers. Especially with increasing initiatives for package re-use, models for these packages may be generated once, and then passed to many consumers. Hence, there is a need to form a consensus on packaging model formats that are generally useful and easily shared. Alternative modeling schemes such as reduced-order models should be investigated with appropriate interpolation methodology to ensure predictivity in the whole parameter variation space. To allow for the increasing complexity and interactions of the IC-package-PCB system, a modular approach that allows for different implementations of different component models may likely be required, especially when considering system-in-package or system-on-chip solutions. It may be necessary to simultaneously consider digital, analog, RF, and even micro-electro-mechanical systems (MEMS) and optical components. Refer to the Assembly and Packaging chapter.

Generating simulation models is creating new challenges with regard to numerical methods. Package geometries are such that usually there is no substitute for fully three-dimensional field-solver extraction. In a flip-chip package there are sometimes so many layers and power and ground structures that the extraction of a single signal net may be very costly. In a multi-chip module (MCM) there may be longer traces that couple many nets together, requiring a very large minimal set for extraction. In either case, decomposing the problem into smaller pieces introduces significant fictitious fringing spoiling the power/ground extraction. The development of scalable multi-scale field-solver engines that can manage full-package extraction is essential; scalability will likely be achieved through implementation on a parallel cluster. At the same time efficiencies with regard to time and memory consumption need to be further improved. Respecting causality and correct DC solutions are essential requirements.

The introduction of low-κ dielectrics with low thermal conductivity increases the need for thermal analysis. With further miniaturization power density increases and it will become increasingly challenging to dissipate the heat generated by ICs through packages and systems into the. This attribute also requires co-design tools that facilitate simultaneous analysis. Furthermore, current flow through ground and power structures must be understood because current bottlenecks can lead to hot spots.

Inherent and thermally induced mechanical stresses throughout the layer stack must be identified and modeled. The low-κ dielectrics often have reduced mechanical integrity, while at the same time thermal stresses are more severe. The stresses are especially enhanced with non-uniform heating induced by the die, by current bottlenecks in the ground and power planes, and with reduced thermal conductivity.

In addition to specific failure mechanisms and front end back interactions induced by new material integrations, the increasing complexity of packaging options drives the need for improved modeling to reduce test cost and development time. Since process windows and main influent parameters are definitely dependent on the packaging options, generic modeling cannot be applied anymore and actual product configurations must be considered. Furthermore, the whole process flow, including front end, assembly and packaging steps, must be simulated to examine precise residual stresses, critical loading conditions, and thus optimize both package and interconnect features. This would finally lower the cycle time to introduce new products while ensuring device integrity. In order to allow such requirements, dedicated modeling procedures must be carried out at the several simulation levels involved. This includes multi-scale methods, calibration of virtual “homogenized” materials representing averages of structures too fine to be resolved on larger scales, consideration of dynamics and multi-physics phenomena that particularly occur during assembly processes, and non-linearity of the material behaviors. As a consequence, thanks to the development of the whole modeling flow and helped with a limited amount of experimental validations, a major role would be played by thermal and mechanical simulations. These need improved material models for bulk and interface properties. Currently, relevant data does not get broadly released from industry. Finally, since interactions from front end to packaging features are increasingly closer, a co-design between the related teams is definitely required.

3.9. MATERIALS MODELING

The determination of the electrical, mechanical, chemical, and thermal characteristics of materials is essential because of their impact on semiconductor device and integrated circuit manufacturing and performances. Application areas of materials modeling in semiconductor technology are relevant for many near-term and long-term challenges and they cover a wide range of materials and properties. Furthermore, besides bulk material, thin films, surfaces and interfaces, the mesomaterial (between bulk and atomistic) range must be considered. The impact of elaboration conditions on materials

properties must also be considered in closed link with Equipment / Feature Scale Modeling and Process Simulation subchapters. Consequently, both empirical and first principle materials modeling and simulation are needed.

There are two fundamental aspects for materials modeling in semiconductor technology:

- First, material properties database form the basis of modeling and simulations in all aspects of semiconductor technology, e.g., equipment, process, device, package, patterning and interconnect topical areas. Consequently, they are major input parameters in all models and simulators allowing retrieving specific figures of merit per topical areas. The driving force here is growing complexity and the decreasing size of semiconductor devices, which requires an increasing accuracy and the inclusion of additional physical effects into models and simulators. Modeling and simulation tools are only as good as the input material parameters. In many cases, these parameters are difficult to determine by experiments alone. Material Databases are needed that contain both experimental and empirical material parameters, and, where not available, calculated from first principles. From first principles, mesomaterial properties must be derived to predict the functional properties at device scale.
- Second, datamining is needed to systematically explore a wide range of new materials and test them for their utility in future semiconductor technologies with their specific constraints. The driving forces here are the physical limits of material systems used to date. Many alternate materials are being suggested as possible solutions for some of the critical semiconductor roadmap roadblocks. Here the link with Numerical Methods and Interoperability of Tools subchapter appears fundamental.

For both aspects, the central motivations are the additional physical insight obtainable by simulation as compared to experiments and the cost and time savings because many complex experimental characterizations are replaced by faster and less expensive simulations. Nonetheless, experimental verification is fundamental, not only for empirical but also for first principle and atomistic simulation methods. Experimental verification must accompany the development and application of theoretical methods from an as early stage as possible. This requires long-term planning and the collaboration of experts in modeling and experiments. It leads to the selection and fine-tuning of accurate simulation methods and the optimal use of experimental and computational resources as demonstrated for the case of determining the atomistic surface configurations or for the case of determining properties of dopant clusters and more recently for the computation of thermo-electric properties of complex compounds.

The complexity of materials modeling is increasing due to a variety of factors. 1) The number of materials has continued to increase with each technology. 2) Size: Most of the devices have dimensions close to material domain sizes (e.g., grain size, thin film thickness). 3) Topography: Non-planar material structures modulate properties and behavior due to different materials at multiple interfaces. 4) Topology of the nanostructures and molecules (e.g., 2D materials (graphene sheets, Transition-Metal-Disulfide or di-Selenide, germane, etc.), Transition-Metal-Oxide, etc.). In addition, one of the practical difficulties in application of materials modeling is the inability to scale to larger size domains efficiently.

The importance of materials modeling for semiconductor technology is a driving force for the development and refinement of new methods. On the other hand, applications of materials modeling in semiconductor technology can also profit greatly from developments from other research areas, e.g., physical chemistry or metallurgy. A wide variety of methods and simulation tools are available. However, *several general challenges must be addressed* in order to fulfill the requirements for the applications of materials modeling in semiconductor technology:

- An increasingly large number of material parameters is required, both as input in other simulators and for the exploration of new material systems. This demands an increasingly large computational and organizational effort. Therefore, the calculation process must be automated to a large degree. Flexible tools enabling an efficient workflow are needed.
- The wide variety of materials modeling methods and tools is a good basis for tackling the various materials related questions in semiconductor technology. However, the lack of interoperability represents a major impediment. Standards for data exchange between tools and an integration of their user interfaces are required.
- Since material modeling is a prerequisite for other modeling and simulation challenges, a fast reaction to changed requirements and priorities is essential for the overall development speed of modeling and simulation. For the continually changing requirements of semiconductor technology, a flexible framework of standard tools and methods is needed as a basis for the development of specialized applications.
- With device active regions continuing to shrink to several tens of nanometers for the physical channel length and to the nanometer range for the effective oxide thickness of high-κ gate dielectric materials, materials simulation and modeling tools that go from atomistic descriptions to continuum results will become critical. In the long term, the

relevant materials modeling approaches might be integrated into the modeling toolsets of the various topical areas. The materials modeling tools must be prepared for this integration. The smaller devices get, the closer process and device simulation get to materials modeling on the atomic level. At the extreme end, for example for charge transport in single molecules, these three modeling tasks are essentially based on one unifying approach, i.e. Schrödinger's equation for the molecule.

- In many areas of materials modeling there are two key tasks. One is the approximate solution of Schrödinger's equation. The other is to extract the desired physical parameters, using as few evaluations of the approximate solutions as possible. Currently, both tasks are usually performed within one monolithic simulation tool. A modularization of the simulations tools with respect to these two key tasks enables a faster and independent development and improvement of the respective methods.
- *Ab initio* methods for the investigation of excited states are required whereas most readily available *ab initio* methods and tools are still restricted to ground state calculations.
- *Ab initio* methods must be extended and optimized for the non-charge-based technologies and materials of some emerging research devices, e.g., devices based on spin phenomena.

Specific materials modeling problems to be addressed for the different topical areas include the following:

- Materials models are needed for improved (especially chemically amplified) resists, for advanced mask making and for multilayer mirrors to be used in EUV lithography. The impact of molecule sizes on the resist structure and properties must be incorporated in the determination of line edge and line width roughness.
- Interconnect performance and reliability will be strongly affected by the microstructure and interfaces as well as the resultant change in conductance of copper, which must be taken into account in the simulation. Another issue for materials modeling is low-κ dielectrics.
- For front-end process modeling, important material properties include the diffusion and clustering parameters of point defects and dopants. These parameters must be determined in crystalline as well as amorphous semiconductor materials and at interfaces. The strain dependence of these parameters must also be determined. Due to these dependencies and due to the combination of several dopants and co-dopants, a large number of parameters must be determined. Due to the atomistic nature of doping and the growing importance of process variations, the diffusion and clustering parameters must be known to such a level of detail that these effects can be captured accurately by the process simulators down to low temperature (500°C).
- Most models used in device simulation can be considered as material models, because they are based, for example, on the electronic structure of the semiconductor, for example dielectric properties, and channel transport properties, including quasi-ballistic transport. Here also, major progress is needed due to shrinking dimensions, higher local electrical fields and especially due to the use of global and local strained channels including, for example, strained substrates (sSi), SiGe, Ge, III-V, SOI, sSOI, GeOI and other new materials. See the Device Modeling subchapter of this Modeling and Simulaiton chapter, and the Emerging Research Materials chapter.
- Finally, most devices are based on phase transition. Major progress is needed to model not only the possible states but also the dynamics of the transitions in order not only to be able to predict the properties of the materials but also there evolution in time during operation.

3.10. RELIABILITY MODELING

As reliability issues become more and more important for the semiconductor industry, modeling is increasingly requested to provide design tools not only to achieve better device performance, but also more robust reliability margins. Modeling is required for the theoretical investigation of the failure mechanisms and of their root causes, but also to explore their relationship with front- and back-end-of-the-line technology on one hand and with design needs and test effectiveness on the other hand.

Since failures are mostly related with the presence of defects and traps in active and passive layers, modeling is expected to investigate the intrinsic defects associated with new materials and their interfaces, but also extrinsic defect creation mechanisms during wafer processing, such as plasma damage and ion implantation induced damage in gate stacks. Accurate modeling of mechanical stress (induced e.g. by lattice mismatch, volume expansion during growth or release during etch) and of its interaction with implantation damage is needed to predict the generation of extended crystal

defects, which can reduce the test yield and increase leakage, eventually leading to product failure under operating conditions. Process related fluctuations may also statistically enhance on-field failure rates if combined with other degradation mechanisms.

Recent years have witnessed a lively debate regarding the root causes of the bias temperature instability (BTI). While most researchers agree that the creation of oxide and interface charges is responsible, the model details are often diametrically different. It has been revealed that the degradation is particularly difficult to predict under dynamic (stress and recovery) bias conditions. Lacking a suitable model for the description of the degradation under arbitrary bias conditions, the degradation of a transistor in a realistic circuit setting is hard to predict. Model development is particularly hampered by the difficulties related to the experimental verification and by the strong bias dependence of the recovery. As such, model evaluation is closely tied to the development and detailed understanding of advanced characterization techniques. With the introduction of alternative high-k gate stacks and the plethora of material systems currently under investigation, a predictive model for BTI (PMOS and NMOS) is urgently needed.

Another mechanism which is also explained by the creation of oxide and interface charges is hot carrier injection (HCI). While BTI is basically a one-dimensional problem where the electrostatics of the transistor is relatively simple to describe, the modeling of HCI is considerably more complex due to the occurrence of hot carriers in the channel. In particular for sub 100nm devices, hot carriers cannot be adequately described by the conventional drift-diffusion formalism and more accurate solutions of the Boltzmann transport equation are required (such as Monte Carlo and spherical harmonics expansion methods). Unfortunately, this is accompanied by a considerable increase in required CPU time and efficient solutions for the problem are urgently needed. A special case is high-voltage devices, which often imply a complex geometry (multi-finger gates, drift regions, LOCOS bird's beak, etc.) which is difficult to capture. Even though many published empirical model exist, a thorough understanding of HCI and a predictive model are still lacking.

Closely related to the defects responsible for BTI and HCI are the random telegraph signals (RTS) and 1/f noise. While modeling of RTS is not strictly a reliability issue, bias and temperature stress has been shown to modify both RTS and 1/f. As such, a better understanding of oxide and interface defects will benefit the understanding of RTS and 1/f. Similar considerations hold for stress-induced leakage current (SILC), which is explained by strategically placed defects in the insulator. Depending on the interaction of their energy levels and the Fermi-levels in the gate and substrate, they contribute to the gate leakage current. Time dependent dielectric breakdown (TDDB) is related with the dynamic evolution under stress conditions of such defects, which is still difficult to model without a-posteriori calibration.

One aspect that is not covered by present simulation methodologies is that BTI, HCI, TDDB, and RTS are likely due to electrochemical reactions occurring at related defects or precursors. Care has to be therefore taken that double-counting is avoided by developing a more complete understanding of the interaction between these degradation effects.

Finally, numerous recent studies have demonstrated that nano-scale device degradation is stochastic, meaning that even nominally identical devices will degrade differently under identical stress conditions. Along similar lines, only a small number of defects will be present in ultrascaled devices. Furthermore, these defects have statistically distributed properties (such as activation energies) due to the amorphous nature of the oxides and interfaces. As a consequence, device lifetimes will become statistical quantities and their distribution needs to be understood. TCAD and EDA tools supporting the analysis of such devices are urgently needed.

Understanding of the above listed mechanisms is still in its infancy when highly advanced devices employing high-mobility materials in combination with advanced gate stacks are being introduced. Predictive physics-based models are urgently needed in order to aid further development of these technologies. Still, as a short time solution, more pragmatic approaches should be developed which allow for accurate Model-to-Hardware correlation results.

The major reliability concerns for Non-Volatile Memories come from charge retention and endurance requirements, which in conventional floating gate devices are strictly related to charge trapping/detrapping of defects states in the sealing dielectrics. Additional modeling issues arise in nitride-based architectures where localized stored charge can redistribute within the trapping layer and new capture and emission mechanisms come into play. Furthermore for the overall device reliability (especially for multi-level applications) the role of array disturbs has to be modeled to optimize write and erase algorithms and the bit failure rate has to be accurately estimated in order to deploy appropriate Error Correction Code modules. For Phase Change Memories an accurate electro-thermal modeling is critical to investigate array disturbs, reset state data retention and the endurance under high local current densities and temperature gradients conditions, which can cause composition variations and electromigration. Other challenging reliability modeling issues are radiation hardness in SRAM and wafer thinning related defectivity (in particular for DRAM). Another reliability modeling issue in DRAM is the retention time degradation of cell transistors, which is related to the generation of defects under thermoelectric and/or mechanical stress, e.g., thermal annealing, burn-in test or warpage. Finally, upcoming

memory devices like RRAM require physically accurate modeling schemes in order to judge whether they can be reliably operated over a long time.

For the backend-of-the-line (BEOL), well-known effects related to the increasing interconnect density, number of layers, and power consumption will be acerbated by the introduction of new interconnect materials. Special attention will have to be paid to low-*k* materials and copper metallization for which a considerable amount of work has been done to address reliability issues like low-*k* line-to-line insulation degradation under bias-temperature stress, thermal dissipation, thermo-mechanical mismatch with the surrounding materials, low yield strength leading to delamination, cracking and extrusion, as well as the high susceptibility to moisture penetration during processing. There are still fundamental problems to be modeled that affect the time dependent dielectric breakdown (TDDB) properties of low-k and especially ultra low-k materials, namely the increasing porosity, the potential damage and/or contamination during process integration, the physical causes of the noise induced by soft breakdown events and its correlation with hard breakdown events, as well as the TDDB kinetics with the related acceleration factors. Hereby the impact of the copper metallization strongly depends on the local topology (e.g., roughness and voids) and on the surrounding materials (e.g., barrier, seed layers, and dielectrics) such that research should be focused on failure mechanisms occurring at the interfaces due to electromigration and to the formation of voids in close vicinity of the vias.

Triggering of low resistivity paths through latchup is still an active issue because of technology scaling. Furthermore, new interaction issues arise due to mixed signal applications and system level interactions. Process-related solutions are centered on highly doped wells, bottom well isolation through buried layers, lateral well isolation through shallow or deep trench STI isolation structures, and SOI. In this framework, carrier injection from parasitic structures needs to be accurately modeled. Internal and external latchup needs to be simulated in a very early development phase in mixed mode and over long distances also by using dedicated tools to extract (and mesh) automatically the 3D device geometry and doping from the layout.

The electrostatic discharge (ESD) charge transfer from an external body to a device can produce thermal-induced hard failures (e.g., gate oxide and junction breakdown, melting of interconnects), soft errors (e.g., latchup, injection-induced snap-back in nMOS), or a combination of both. Some requirements for ESD are common to latchup. Modeling for ESD has to focus in particular on heat generation and propagation (especially in SOI), carrier mobility and impact ionization up to melting temperature of the silicon, transistor instabilities (like MOS snap-back and BJT gain degradation), N-well resistors (limitation, ballasting), poly-defined and substrate diodes, silicon controlled rectifiers, substrate effects (resistance, current, ground bouncing, noise coupling), lateral parasitic, current filamentation, current saturation of metal lines and vias, and finally on dielectric breakdown (gate oxides, low-k). Significant room for development still exists to efficiently capture electro-thermal effects in 3D circuits. This requires device and mixed-mode transient simulation, physical and predictive models, physical model validation, as well as system level simulation.

In power MOS devices using wide bandgap semiconductors (SiC, GaN, ..), one of the main reliability problems is threshold voltage (Vth) instability, where Vth increases after long periods of gate bias stress are much more significant than in silicon power devices. There is general consensus that the observed instability problems are due to charge trapping at and near the semiconductor/SiO_2 interface. As the extent of Vth instabilities is significantly affected by the ramp rate of the gate voltage used for the measurement of the threshold shift, dedicated transient trapping and detrapping models are needed.

Ionizing radiation is either produced inside the device itself (e.g., package materials, radioactive isotopes of silicon and doping species) or extrinsically (e.g., cosmic ray, external source) and can affect integrated circuits as well as high voltage components. Ionizing radiation leads to time-dependent degradation of the device performance (junction leakages, threshold voltage shift in MOS, parametric degradation in bipolar devices) and/or to single event upset events that can produce both hard failures (gate oxide rupture, latchup, breakdown), as well as soft errors (e.g., data loss in a memory), observed as a soft error rate (SER). The impact of SER over the years is almost constant or even increasing in spite of the reduced sensitivity for the single units due to device scaling and the use of countermeasures (e.g., SOI, redundancy, error detection and correction). This is because of the corresponding increase of the number of units in a system. Viable models and simulators are still lacking to extrapolate the SER from the cell up to the system level from accelerated tests, which are able to keep track of the error propagation and to provide enough statistical accuracy.

Independently of the application field, new package technologies are continuously introduced to cope with the requirements in terms of package size shrinking, increased terminals count, increased speed, increased power density and dissipation, increased ESD and electromagnetic immunity, new interconnect materials, increased usage in extreme environments, and environmental sustainability. The variety of interdependent physical parameters increasingly leads to the need for more accurate models and procedures for fast and low-cost reliability assessment of new designs either based

on traditional reliability testing, or on numerical simulations (virtual prototyping), which can account for the dependence on multiple physical parameters at the same time (e.g., temperature and humidity).

As the number of materials and interfaces increases, major long-term reliability hazards are related to thermal cycles, thermal dissipation, interfacial delamination, and thermomechanical mismatch within the package and with the assembly (and in some cases to material interdiffusion and electromigration). In such cases, global physical parameters (e.g., fullchip temperature distribution) often strongly depend on parameters at the microscopic scale (e.g., local current density), such that the need for multiscale simulation methodologies is increasing. Finally, since the reliability of an electronic package is ultimately determined by the environment and application in which it is used, systematic modeling of mission profiles is required for accurate lifetime prediction over long periods of time.

One of the greatest challenges for design for reliability is the capability to enable failure rate calculations at all hierarchical levels (up to SoC) as it is now mandatory for some market segments like automotive through the ISO26262 norm. This item will require in the future some dedicated developments that must be taken care of urgently.

While considerable work is still required to refine existing TCAD tools for reliability assessment, an alternative pathway requires mentioning, namely the effort to make products intrinsically resilient against degradation through an adequate mix of reliability sensors and feedback loops (either based on hardware and/or software). While this strategy may appear unavoidable in future nanoscale nodes due to the intrinsic variability, the analysis and qualification of the functionality of these add-ons would considerably benefit from predictive TCAD reliability models.

Within the very broad spectrum of reliability issues summarized above, modeling and simulation can be helpful for several applications:

- For understanding the fundamental physical mechanisms
- To optimize elementary devices geometry/doping (and indirectly the process flow) for reliability
- To establish safe layout/design rules
- To assess the Safe Operating Area and Mission Profile for each elementary device
- In the interpretation of raw electrical characterization results (e.g., to factor out the role of degradation and recovery) and to complement Physical/Electrical Failure Analysis
- In product lifetime prediction and to determine extrapolation laws and acceleration factors for accelerated testing
- To find the most effective test strategies to screen weak sub-populations
- To estimate the needed redundancy and Error Correction Code resources
- To assess the fault coverage effectiveness for embedded circuits used in Built-In Self-Test
- To assist Design for Reliability through:
    - SPICE and behavioral level modeling of degradation to check impact on analog/digital circuits
    - better methodologies and tools at EDA level (at least post-layout) to identify location/probability/impact of failures (critical nets/hot spots, including self-heating with SOI)
- For virtual prototyping (especially for system- and package-level reliability issues)

However some of the above listed goals can be achieved only if a few challenges are met in terms of models and tools capabilities:

- *Predictive* modeling of traps/defects creation/annealing (both during wafer processing and under operating conditions)
- Accurate coupled (*multi-physics*) electro-thermo-mechanical modeling
- Statistical handling of individual atomistic level configurations of traps, dopant/contaminant atoms, electron/holes
- Hierarchical multi-scale modeling (where the possible involved levels are system/board, package, chip, block/circuit, device, and atomistic)
- Capability to dynamically handle structural changes during device simulation
- Compact and behavioral modeling of the failure mechanisms and elementary devices degradation.

3.11. MODELING FOR DESIGN ROBUSTNESS, MANUFACTURABILITY AND YIELD

With devices shrinking well into the deca-nanometer range, the variability of process results due to variations of fabrication parameters, such as defocus in lithography, temperature profiles in millisecond anneal, or statistical fluctuations of a small number of dopant atoms gets increasingly important. As mentioned in several of the focal ITRS chapters and their cross-cut texts, this variability increasingly challenges further device scaling and the overall progress of the roadmap. Moreover, the manufacturability and robustness of designs as well as the yield of the circuits and systems increasingly require that such variability is already addressed at the design stage. In turn, within the 2011 ITRS Design chapter, "Manufacturability" is highlighted both as a near-term and a long-term challenge, including among others performance/power variability and uncontrollable threshold voltage variability, respectively. Already from the 2005 ITRS a dedicated section has been devoted to "Design for Manufacturability". Threshold voltage fluctuations due to random dopant distributions in the channel increase with scaling since they are inversely proportional to the square root of the area, and their relative impact increase even more dramatically as the nominal threshold voltage is reduced. A similar effect holds for geometries (e.g., for gate CD) where it is generally very difficult to reduce absolute variations in the same way as the nominal values. In turn, variation as a percentage of the nominal value increases. The Modeling and Simulation subchapter on "Modeling for Design Robustness, Manufacturability and Yield" deals with the support TCAD can and should give to the challenges and requirements primarily addressed in the "Design for Manufacturability" part of the "Design" chapter. In this way it is intended to complement actions which are and have to be carried out at design level, and are therefore included in the Design chapter.

As pointed out in the cross-cut texts between Modeling and Simulation and almost all other chapters of the ITRS, TCAD must contribute to the assessment and minimization of the impact of such process variations and dopant fluctuations on the performance and reliability of devices, ICs, and systems, which critically affect manufacturing, yield and design robustness. The key advantage of TCAD is that well-defined variations can be very easily introduced into a simulation run on a computer, and subsequently their impact on performance and reliability figures can be calculated separately for each variability mechanism, as well as for a combination of different mechanisms. Integrated process/device/interconnect/circuit simulation employing sufficiently predictive physical models could then be used to calculate the spread of relevant quantities such as physical channel length, threshold voltage, off- and drive currents, signal delay, etc. Compared with this the experimental study of the impact of such variations is at least very difficult and expensive, if not impossible. This is due to the inherent difficulties to produce experimentally and to characterize reliably a well-defined nanometer scale variation of a patterning process and the resulting geometry, or the number of dopant atoms in the channel region, and their precise locations.

Variations can be classified into random and systematic. Typical random variation mechanisms are random dopant fluctuations, mask defects (particles) and line edge roughness (LER) fluctuations in lithography, gate dielectric thickness fluctuations, grain-induced charges in polysilicon or metal gates, etc. Especially lithography steps are sources of many different systematic variations, such as misalignment, defocus, illumination dose fluctuations, proximity effects between different features, lens aberrations and mask imperfections. The latter two are expressed by the Mask Error Enhancement Factor MEEF. Other typical systematic variation mechanisms are stress proximity effect, well proximity effect (WPE), etch visibility and micro-loading effects, iso-dense bias in deposition and etching, changes of etch and deposition rates across the wafer, transient enhanced diffusion (TED) proximity effect, pattern-dependent heat absorption during flash or laser anneals, process drift over time, etc. All of these effects can be addressed by modeling on different levels, from modeling microscopic mechanisms to analyze fundamental effects, to TCAD-level analysis to quantify the impact on transistor performance, and then to compact or even behavioral models accounting for the impact of transistor variations on circuit functionality and performance. The compact models are necessary to handle thousands and millions of transistors on the circuit, where each model has to run within milliseconds rather than hours of CPU time. However, a key problem is that it is difficult to characterize and quantify these variations, e.g. because equipment vendors either do not have this information or do not want to share it with their customers. Furthermore, a symmetric (e.g. Gaussian) distribution of one or the other of these variations may lead to strongly asymmetric distributions of gate lengths and electrical parameters, because process steps and also device architectures may act as filters which strongly change the distribution of the variations. Especially variations which are caused by the same process step or mask level may be correlated. In this case the correlation must be traced through the whole simulation chain, because it may have a key influence on the device or system: E.g. if both gate length and width are decreased due to defocus in a lithography step, then the first variation would increase the drive current, whereas the second one would decrease it – thus both variations would to some extent compensate each other. This demonstrates that corner models are no more sufficient because they may be overly pessimistic.

Some systematic variations can partly be reduced by modeling-driven optimization techniques to achieve more uniform layout patterns (e.g., by adopting regular fabrics and by the insertion of dummy features) and proximity corrections. Furthermore residual systematic variations can be described with compact models, and therefore do not necessarily affect the circuit performance since they can be compensated by design. However, many of the systematic variations either appear as random (such as defocus, process drift and the imperfections of stepper lens) or lack an appropriate compact model and therefore are not accounted for. Such systematic variations and all random variations can only be addressed increasing the design margin, thus forcing the circuits to run slower. To avoid this, microscopic and TCAD level modeling can be used to characterize and minimize the random variations and compact modeling has to be used to account for systematic variations.

There are large areas of application and potential merits of Modeling for Design Robustness, Manufacturability and Yield:

- Assessment of layout dependent device performance by use of coupled process and device simulation which for example enables the study of layout-dependent stress effects, proximity effects in lithography, visibility and micro-loading effects in etching, layout-dependent transient-enhanced diffusion of dopants in the channel and source/drain, scattering of high-energy implants off photoresist mask (usually observed as a WPE), or large-scale CMP effects.
- Despite restricted design rules (RDR), there are significant layout-induced proximity variations due to the effects listed above, with the on-state current changing by over 30% at 45 nm node when a transistor with the same channel length and width is placed into different layout contexts. Considering that stress propagation length is determined by silicon mechanical properties and does not change with scaling, each subsequent technology node doubles the number of neighbors that introduce stress into any given transistor. This means that transistor performance increasingly depends on the layout context within a standard cell as well as from the neighbor cells.
- Advancing along technology nodes some of the variability mechanisms diminish or disappear, like random dopant fluctuations in the channels of fully depleted transistors such as Ultra-Thin Body and BOX (UTBB) FDSOI devices or FinFETs. However, new variability mechanisms come into play, sometimes surpassing the existing ones, such as the FinFET sensitivity to the shape and size of the fin. Overall, the ever-shrinking transistors contain fewer and fewer atoms so that the presence of each atom and its particular location increasingly impact transistor performance. Therefore, variability is here to stay and will likely play a major role in design and manufacturing of future ICs.
- Even larger can be the effect of a single, strategically placed trap since the capture and emission of one electron or hole can cause a large fluctuation in time of the overall conduction (giant Random Telegraph signal Noise, or RTN), which in turn can cause circuit failure if not properly addressed.
- The ability to predict the statistical distribution of random process variations and of RTN is particularly critical in multi-Gb memories, where the requirement to insure reliability in the parts per billion range for parts containing billions of memory cells leads to the need to evaluate bit failure rates (and therefore unlucky atomistic dopant and traps configurations) extrapolating probabilities around 10^{-18}.
- Sensitivity analysis of device performance variation caused by process variation: This would enable the identification of the maximum variations of certain process parameters that are still acceptable to keep the variations of the device performance within specifications. Compared with the state-of-the-art of the available technology this allows judgment of whether the device variability specifications (for example, 3σ spread of V_{th}) can be achieved, and which are the most critical process steps to be improved.
- Starting from a given technology and its variations or dopant fluctuations TCAD could be used not only to assess the nominal performance of certain device architectures but also their spread. This enables a much better assessment of the device architectures because with further shrinking features and higher integration moderate improvements of nominal performance may be far less important than the selection of processes and architectures which cause less variations in the performance of the final device or IC.
- A severe problem for standard reliability characterization by accelerated testing (often referred to as stressing) is that devices which are subject to variability may exhibit a significantly different behavior under stress compared to nominal devices. In turn, accelerated testing may lead to in misleading results, and TCAD may be used to help to solve this problem. Conversely, TCAD may also estimate the reliability of "worst case" devices and more generally investigate statistical reliability
- Complement standard SPICE models that currently bridge between process technology and design by information on the impact of process variations on design. This would enable a much more accurate assessment of the manufacturability of a design. For example, instead of global values and tolerances of design parameters such as gate length and $V_{th,}$ the requirements may be relaxed in some areas and tightened in others, allowing the

manufacturing of ICs with better performance, smaller size or higher reliability - without changing the technology used - by just adapting the design to the local neighborhoods.

- Assessment of the impact on devices and ICs of the variations introduced by a certain piece of equipment. This assessment would complement traditional advanced process control (APC) methods to decide about feed-forward and feed-backward equipment control and about when equipment maintenance is needed to limit drift or variations of process parameters. Process compact models (PCM) that are based on pre-calibrated TCAD simulations are being successfully used to counter-act such process drift by changing the downstream process flow on the fly.
- The calculated transistor and interconnect variations can be plugged into circuit simulation and statistical static timing analysis (STA) tools to estimate performance variations of IC as a whole. This approach enables the assessment of the impact of process variations on yield. By identifying the most critical processes, the yield can be maximized by appropriate changes of those processes or the design.
- Yield can be severely impacted by extrinsic junction leakage due to dislocations. Modeling the evolution of implantation induced defects and the interaction with mechanical stress along the process flow can be very useful to identify the most critical processing steps and layout configuration and therefore to optimize both in order to reduce yield loss due to crystal defectivity.
- Seams/voids in isolation regions or at their interfaces often lead to leaky paths or even shorts which reduce yield. Predictive simulation of robust isolation architectures requires the accurate modeling of the evolution along the process flow of some local properties of dielectric materials, such as density, mechanical stiffness and wet etch rate. In particular to fill high aspect ratio trenches and holes it is often necessary to use materials with poor as-deposited robustness (e.g. SOD), and accurate modeling of their densification is important to optimize integration robustness.
- Especially in conjunction with double patterning and the need to etch thick layer stacks with very tight pitch, advanced modelling can be used to predict the risk of yield loss due to pattern collapse and/or feature stitching.
- Power devices and MEMS require coupled simulation of heat transfer, including cooling fluids, and electro-magnetic cross-talk, which is essentially multi-physics modeling.

In summary, there are large prospects for “Modeling for Design Robustness,” “Modeling for Manufacturability,” and “Modeling for Yield.” However, the potential merits of the application of TCAD to study the impact of major variability mechanisms listed above can only be gained if several challenges are met by Modeling and Simulation:

- First, sufficiently general and predictive physical models must be available and be implemented in the TCAD tools used. The general requirements on these models are discussed in the other sections of this Modeling and Simulation chapter. A specific aspect of Modeling for Design, Manufacturability and Yield is that the primary objective is the study of the impact of the variations, not the prediction of the absolute performance figures. Therefore, calibration of the models prior to their use is acceptable. The basic requirement is, however, that the models correctly capture the trend, which means that the direction of the variations of the performance figures as well as their magnitude must be predicted.
- Second, the level of integration between process, device and circuit simulation must be drastically improved: For example, the integration of physical 3D simulation of the patterning steps lithography, etching, deposition, and CMP with each other and with doping processes and 3D device simulation is not yet available in commercial simulation tools. Adaptive meshing for non-planar and especially time-dependent geometries is still a key limiting factor. For Modeling for Design Robustness, Manufacturability and Yield this integration challenge is drastically increased because all kinds of numerical errors—resulting from discretizations in space and time and from the change between different meshes used in different simulation modules, for example—must be controlled to make sure that the final calculated device or IC variations are not significantly falsified by numerical noise.
- Third, the most difficult challenge for TCAD for Design, Manufacturability and Yield is the need to bridge between microscopic process and device simulation on the nanometer scale and the design of an IC with millions to billions of components on some ten square millimeters. Typical 3D TCAD simulation requires mesh with about 10^5 mesh points to describe a device. Extending this to chip level would require the order of magnitude of 10^{14} mesh points, which is impractical in both the required memory and CPU time. In consequence, suitable strategies and algorithms must be developed for hierarchical simulation: Nanoscale process and device simulation is only carried out for small critical areas. Then appropriate data on the level of SPICE compact models and behavioral models including their variations are extracted, and communicated to design.

- Conventional methodologies for the treatment of variations, such as corner models ("slow-slow" and "fast-fast") are no more sufficient because they cannot appropriately deal with variations which may be partly statistically dependent, partly statistically independent. In turn, they tend to overestimate the impact of variability and may lead to overly pessimistic designs. Careful usage of a hierarchy of modeling tools with TCAD and compact model levels can be instrumental in providing the input for statistical static timing analysis tools and build robust ICs without excessive design margins.

3.12. NUMERICAL METHODS AND INTEROPERABILITY OF TOOLS

Numerical methods and algorithms need improvement to support the growing complexity of physical phenomena to be addressed by extended TCAD. For example, more accurate solutions of the Boltzmann transport equation in device simulation are required. To include stress and strain and several defect species and complexes in the simulation of dopant diffusion and activation requires dealing with an increasing number of coupled partial differential equations over the device grid. More recently, an increasing demand has been put on the simulation of electromagnetic effects such as the skin effect in conductors, the proximity effect and the substrate coupling. Increasingly, the interaction between different effects becomes key for the performance and reliability of devices or system – e.g. the coupled electro-thermal-mechanical simulation which is needed for various application areas. These are examples of how increased requirements on predictability and accuracy of models induce more complex models and, in turn, drive the discretization methods and linear solver technology. Moreover, physical processes with different intrinsic time- and/or length scales critically influence each other, and have to be simulated adequately in a coupled manner—point-defect diffusion occurs on a several orders of magnitude faster time scale than macroscopic process time. The gas flow, depletion, and reaction in a deposition furnace on a macroscopic scale are the basis for the chemical vapor deposition in a contact hole, there also critically affected by the local geometry on a deep sub-micrometer scale. Requirements for multiscale simulation and co-design, e.g. for chip and package, are continuously extending and increasing, raising additional requirements on the integration and performance of tools. In turn, the need for hierarchical simulation approaches is increasing, which start from a nanoscopic description with continuum or atomistic models, followed by some data reduction to enable the simulation of complex systems. Such methods are among others required for the simulation of the impact of process variations, see the subchapter on *Modeling for Design Robustness, Manufacturing and Yield.*

Increasing numbers of independent variables or accuracy requirements lead in many domains of modeling to the transition to a completely different level of approach, such as Monte-Carlo instead of analytical simulation of ion implantation; atomistic modeling instead of (or complementing) continuum diffusion equations; and rigorous solutions of Maxwell equations instead of (or complementing) the traditional thin mask approximation to enable the simulation of advanced masks (phase shifting masks, source-mask optimization) in optical lithography. These advanced approaches frequently require the development of new problem-specific and efficient algorithms, as the application of standard algorithms would result in prohibitive time and memory requirements. Not only the linear solvers as stand-alone libraries demand continuous improvement, but also research is required on how the set of discretized equations are scheduled and organized before submission to the linear solvers is done. In consequence, the state-of-the-art of the numerical methods and algorithms available or being developed mainly in other domains of science must be permanently checked from the point of view of the application requirements of all domains of simulation, described in this roadmap, and be used to influence and kick-off developments required.

Meshing, although always important for the efficient and accurate solution of differential equations, has become a major issue because device architectures are now essentially three-dimensional. The increase of the numbers of steps to be included in process simulation, and especially the frequent use of simulation splits to investigate process options and the sensitivity of electrical device data on process details requires completely automated grid generation. This automated grid generation must be reliable for all kinds of device geometries and distributions of volume variables. In addition, meshing tools must be capable of resolving all critical features of the device or equipment, like small geometry features or steep dopant gradients, without unacceptable drawbacks in terms of mesh nodes, computation time needed for mesh generation, or adaptation in the refinement as well as the coarsening direction. Mesh adaptation to match changes in volume variables and interface positions and to minimize numerical errors in the solvers used is a key issue – here, especially in case of nonstructured/nonhierarchical meshes proper unrefinement is equally important to mesh refinement but frequently more difficult.

Mesh generation time is especially critical in case of simulation splits or simulation runs with a large number of process steps. Considerable problems are caused especially in three-dimensional simulations by moving gradients of volume variables and even more by moving geometries: These require parallel mesh refinement and unrefinement or the use of

moving mesh nodes, in most cases with additional requirements on the shape or quality of the mesh elements to be met to enable an appropriate solution of the physical model equations to be solved.

Meshing algorithms must guarantee that discretization errors caused by the removal or by the movement of mesh nodes do not negatively affect the simulation results: Especially for applications in sensitivity analysis it must be guaranteed that changes of the results are due to physical reasons and not critically affected by changes of the meshes used in the different simulations.

A promising solution to this problem is that a new mesh should use as many nodes and elements of the preceding mesh as possible and appropriate, such as during the simulation of oxidation. Stable and efficient algorithms are needed to trace the change of device geometries especially in the three-dimensional simulation of process steps like etching where multiple layers have to be considered. Such algorithms must reliably avoid artifacts in device topology and allow for appropriate volume meshing. Currently, none of the several approaches used (triangulated surfaces, cells, level set; delooping) has demonstrated to solve all relevant application problems.

These meshing requirements outlined above are further extended by the growing demand for equipment and material simulation. While in this case the problem of moving geometries hardly exists, adaptation to time-dependent volume variables is still critical. A major concern is to combine the very different scale in the simulation problem: the on-chip features are on the nanometer to micron scale whereas the equipment scale is in the centimeter range. Automatic mesh generation and adaptation is especially important to resolve critical features of equipment geometry and the wafers to be processed, while avoiding a too high number of mesh nodes. This problem gets severe when coupling equipment and feature scale simulation. Several current tools for computational fluid dynamics (CFD) calculations suffer from a complicated procedure to define the geometry to be simulated and to provide necessary information for mesh generation.

Particle-based Monte-Carlo codes need an increase in speed as well as variance reduction techniques to minimize noise within acceptable simulation times. The rapidly increasing demand for more GFLOPS will at least be partly met by improving hardware, provided current trends continue. Parallel solution strategies are also needed in order to address computationally intensive 3D simulation needs and simulation of large circuits. This especially includes the use of distributed systems. These systems are currently standard in industry. However, it has to be critically investigated which kind of simulations will only be possible with large shared-memory computers, and whether and how sufficiently powerful systems will be accessible to industry and research.

Linear solvers are often the bottleneck in the computation. Many millions of algebraic equations need to be solved simultaneously by a two-fold iterative scheme. For example, the unification of the drift-diffusion model and the Maxwell equations demands that ~10 variables are solved for each grid node. The outer loop that is needed to address the non-linear coupling can be substantially speeded up by intelligent forward guessing strategies. Further improving of these methods will drastically reduce the number of iterations. The inner loop that is required for obtaining the updates can be improved considerably by re-ordering strategies, optimal preconditioning, partitioning of the equation set, and multigrid methods. Speeding up direct solution of the linear system is very helpful when iterative methods face convergence problems. This latter applies especially for circuit simulation, in the time domain as well as in the frequency domain. All the mentioned methods need to be exploited and optimized for TCAD applications.

Additional work must be spent on algorithm architectures and implementation to make solvers execute efficiently on multi-core processors. In addition special purpose floating point processors based on graphical processing units could speed up numerical calculation a lot which is currently demonstrated in many physical applications.

Research is also needed on arriving at robust solution techniques: Effectively this means that in general an optimization sequence avoids local minima where the flow gets trapped. Techniques need to be developed for how to escape from these traps without fully destroying the result achieved so far. These strategies should then be implemented in the software tools in order to facilitate their respective ease of use.

Research is also needed on developing robust and efficient parameter extraction algorithm. Without a well-calibrated parameter set, simulators lose their practical values. However, calibration work is frequently a time consuming and delicate issue, due to a large number of parameters and the so-called “local minimum problem.” Some algorithms, such as genetic algorithm (GA), may be good candidates to solve this problem, but only if remarkable improvements in its efficiency are realized. Furthermore, it is not always guaranteed to obtain a set of complete measurements for calibration. A sophisticated scheme for interpolation from randomly measured results is also needed.

A continuous challenge is inverse modeling, which has a potential capability of providing us with information of parameters that are difficult to measure such as two-dimensional dopant distribution, the dominant chemical-reaction-path, etc. From the mathematical point of view inverse modeling is a delicate issue because a limited set of data has to be correlated to a large collection of configurations that could reproduce the restricted data set, in other words the problem is

under-determined. This means that in many cases, no satisfactory solution can be obtained, or in other cases, the obtained solution represents one example of millions of configurations. However, it has the potential of opening a new way of application for modeling and simulation. Preferring one configuration over another one should be guided by objective criteria. The latter may be found by entropy principles or information theoretical considerations.

A breakthrough for efficiently calculating stochastic variations in models is needed to meet the strong requirements of evaluating and/or simulating deviations of device performances due to uncontrollable fluctuation or variations under device fabrication. Traditional computing approaches such as the Monte-Carlo method require a prohibitively large number of trials, as the number of fluctuating variables increases. It will be necessary to introduce new algorithms for this purpose, such as numerical methods to solve stochastic partial-differential-equations. Hierarchical simulation approaches which employ data reduction on their ways from nanoscopic simulation to system behavior are one potential solution. A widely spread and well-known component of such an approach is the extraction of variation- aware compact models from device simulations. Variability simulation with verification and variation-aware compact modeling will be a hot issue for 10nm regime technology, and efficient and accurate algorithms will be needed.

Interoperability of tools continues to be a major problem in two respects: First, the transfer from one simulation step to the next frequently leads to basic changes in the data representation, algorithms and in the requirements for the numerical meshes used, because these are usually optimized for the application and tool in question with respect to accuracy and speed. For the transition from one step to the next the problem is now to minimize discretization errors resulting from the change from one data representation (e.g., level-set to string-based topography description) or one mesh to the next. In the latter case the problem even occurs in cases where the kind of mesh stays the same (e.g., 3D tetrahedral Delaunay), but the mesh refinement criteria are changed, e.g., adapting to electrical fields in device simulation instead to doping gradients in diffusion simulation. Furthermore, also the numerical effort and computation time to change from one data representation and mesh to the other must be controlled and be kept at an acceptable level. The second problem is a non-technical one: It is important for users to be able to choose between tools from different sources, and especially also to combine tools from different sources in order to best meet their requirements – e.g., a tools from vendor A for some parts of process simulation, tools from vendor B for the rest of process simulation and for device simulation, tools from vendor C for circuit simulation. This needs at least open and documented interfaces between the various tools, or in the ideal case even interfaces which are standardized for a certain kind of data transfer, e.g., from 3D dopant to 3D device simulation. Whereas such open or even standardized interfaces would be very beneficial for the users, they are unfortunately not necessarily in the interest of the software suppliers.

4. POTENTIAL SOLUTIONS

Modeling and Simulation software tools span the entire semiconductor world. These tools are being used daily with increasing efficiency. This document has above presented specific needs to increase this effectiveness and to provide impact on our industry in the future. Whereas the discussion on the requirements given above implicitly included the potential technical solutions to meet them, some general actions are needed to enable Modeling and Simulation to fulfill these needs and in this way to provide the forecasted benefits to the semiconductor industry:

- Increase cross-discipline efforts will be vital in order to leverage on the expertise of fields that were originally not related and are now needed to work together to cope with the challenges outlined in this document. This is getting increasingly more important due to the introduction of new materials and especially due to the assessment and introduction of novel device architectures which use state variables other than charge.
- Adequate resources for research must be mobilized and directed to efficiently work towards the technical solutions for the challenges and requirements defined. In addition to the definition of the top-level requirements in the ITRS, interactions between industry and research institutes both at universities and at independent laboratories must continue to be enhanced and extended to guide the activities towards the industrial requirements detailed in this roadmap. Especially, this interaction must also include the promotion and enabling of mid- to long-term research actions needed in Modeling and Simulation, which is generally pre-competitive and therefore an excellent field for broad cooperation. Nevertheless, near-term needs and financial boundary conditions in industry have so far frequently led to strong reductions of such activities, with the consequence of endangering the mid- to long-term success of the roadmap. This became again apparent during the preparation of the 2013 ITRS where it was found that several requirements stated in the 2011 ITRS have so far not been met due to missing support for the necessary R&D work.
- Software houses, research institutes and universities must be strongly encouraged to standardize and/or open up some of their universally used modeling and simulation modules to avoid multiple work in the pre-competitive area.

In the ideal case there should be supplier-independent standard interfaces that allow for the combination of tools from different sources, or at least standardized model-interfaces that allow R&D institutes to focus on the development of added-value features, like new models, while being compatible with supported software environments from the beginning and in this way reduce time-to-application. Existing proprietary model interfaces of some commercial tools have already proven to strongly promote cooperation with research institutes and universities and, in turn, strongly accelerated model development and its use in industry. Standardization of interfaces would largely enhance that benefit. The semiconductor industry can have a central role in this respect by requesting such standardization when deciding about their software investments.

- With equipment suppliers playing an ever larger role in process development, the target should be that not only a basic process is sold with the equipment but also an appropriate simulation tool (or at least a model with well-established parameters) to describe this equipment and process. For a well-characterized and stabilized process sufficient data should be available to enable the development of these features with high added value. Cooperation of equipment suppliers with university and independent research institutes is vital for this process. Compatibility with overall simulation environments generally offered by software houses should be achieved via the standardized or open interfaces mentioned above, or via direct cooperation with relevant software vendors. In order not to limit the semiconductor industries' choice of equipment and software either the standardized interfaces or non-exclusive cooperation would be preferred. Related IPR problems need to be solved well in time.
- To further optimize the industrial benefit from simulation, the methodologies for evaluating the impact of Modeling and Simulation must be improved. The target should be to identify more in detail in which way simulation can most efficiently support the industrial development ("value for money"), but also to get a more clear view of the overall benefit in terms of reduction of development time and costs as estimated in Table MS3 of the 2011/12 ITRS, which is not included in the 2013 issue because it still needs to be updated. Making the cost benefit from Modeling and Simulation more transparent should also help to get sufficient resources for the required R&D work without which the cost benefit cannot be achieved.

The most important general technical development needed in the field of Modeling and Simulation is that of integration—not only between equipment and process, between different processes, process to device, device to circuit, layout and design, but also between different levels of description. In some cases the Modeling and Simulation software tools are linked together (such as traditional TCAD process and device simulators, design tools), while in many other areas the software tools are still separated. If one examines the cycle time for development of a new technology, much of that time and cost is not in the individual module development, but at the integration level. There is a continued strong need for Modeling and Simulation tools to be better linked for determining unforeseen interactions of one step on the next. This type of effort is needed for the following:

- The interfacing or integration of individual equipment/feature scale simulation tools. An example is the linking of a lithography simulation tool that predicts exposure characteristics in photoresist with a plasma-etching tool that predicts etch profiles for process latitude and sensitivities.
- The interfacing of materials structural simulation tools with software that predicts electronic properties. An example where these tools would be useful is in the development of high-κ dielectric thin films. Future software tools in this area then might treat the gate stack as a system rather than as individual components. Unforeseen materials interaction issues, better "what-if" analyses, and reliability effects could be studied.
- The integration of chip performance tools with package thermal, mechanical, and electrical simulation tools to create a co-design environment.
- Structured data sets that contain needed physical constants that facilitate parameter passing between tools.
- The integration of device simulators with robust methods for creating compact models and device files for design.
- Generally, a hierarchy of closely coupled simulation tools must be developed - from spreadsheet to *ab initio*. This would allow the industry to select the most appropriate level of description for their simulation problem in question, along with appropriate and efficient data transfer when the application requires investigations at different levels (for example, for influence of process variations on design). The growing need of such an approach is underlined by the subchapter on Modeling for Design Robustness, Manufacturing and Yield in this Modeling and Simulation chapter which was newly introduced in the 2005 ITRS as "TCAD for Design, Manufacturing and Yield".

5. CROSS-CUT ISSUES

In the following, links between Modeling and Simulation and all other ITWGs are outlined. These are based on a thorough investigation of the material from these ITWGs and broad cross-ITWG discussions, and partly include citations from earlier versions of other sections of this roadmap.

5.1. DESIGN / SYSTEM DRIVERS

One of the key problems that challenges design in connection with further shrinking feature sizes is the increasing variability of design-related parameters, resulting either from variations of fabrication parameters or from the intrinsic atomistic nature, affecting for example, channel doping. This problem is discussed in detail throughout the Design chapter, and especially in the part on Design for Manufacturability. Modeling and Simulation can and must help to ease this problem by assessing the quantitative impact of such variabilities on the relevant design parameters: Statistical variations as well as drifts of fabrication parameters must be translated via appropriate equipment, process, and device simulation as well as parameter extraction into the resulting distribution of design parameters, such as size and spacings of active and passive devices, transistor characteristics, and coupling of interconnects leading to signal delay and distortion. The atomistic nature of dopants is very important which in some cases results in just one or a few dopant atoms being at average present in the channel region, giving rise to enormous relative fluctuations of doping and, in turn, electrical device parameters. Especially important are the interactions between different subsequent process steps, such as lithography and etching, which may either amplify or smoothen out such process fluctuations. E.g. variations of threshold voltage which can be caused by many different process variations also lead to spreads and higher values of leakage currents, due to the exponential dependence of leakage on Vth. Simulation should further contribute to the assessment of the impact of parasitics, delay variations, noise, and reliability issues, including thermal effects during operation. The treatment of such "second-order" effects is especially important for analog design where, for example, matching is a key issue, and process variations may lead to the need of active mismatch compensation in design. The overall target is to link design parameters more closely to the technology and device architectures used, especially including their process-induced variations, in order to help designers to select appropriate safety margins, which may vary within the layout. This should also help design to avoid the overcompensation of variations in design resulting from the use of corner models, which more and more tend to be over-pessimistic. Analog and RF designs have driven the needs for high precision compact modeling as well as for characterization and extraction of all kinds of device non-idealities. However, variations and non-idealities such as noise and parasitic elements make extraction of simple rules for higher levels of abstraction in analog and RF circuit design (or even layout) very difficult. The added value which only simulation can provide is that a wide set of variations may be investigated largely automatically, within relatively small time, and at relatively small costs. In this way Modeling and Simulation must contribute to the solution of the problem that historical process tolerance levels can in future no more be met, and that therefore realistic estimates of the new tolerances and their implications must be provided. To achieve this goal, appropriate methodologies must be developed to extract from the microscopic TCAD simulations which are mostly carried out on device or cell level relevant information in a format which allows further processing with design tools—e.g., via SPICE parameters and their statistical distribution.

On short-term time scale especially issues related with mask making, e.g., the efficient definition and assessment of assist features needed to transfer features from layout into the photoresist, and variations of electrical data such as threshold voltage, are especially important. Simulation must not only contribute to the correction and adaptation of masks to make sure that the feature printed on the wafer approximates well enough the "ideal" structure intended by the designer, but also help to avoid costly overcorrection of the mask features, for example, by complicated assist structures and to select the most cost efficient mask structure for the printing of the required features on the wafer. Besides this, a challenge is especially the uncontrollable CD and dopant variability. In the end Modeling and Simulation should contribute to the design challenge of yield prediction and optimization, by providing the information on the impact of process variations and of dopant fluctuations, and on the printability of defects which would allow the designers to adapt their design to be less sensitive to these non-ideal effects and in this way maximize yield. Since variability is expected to be the source of multiple critical DFM and resilience challenges, a systematic method to roadmap required and/or desired variability trends will become a crucial component of the overall Design roadmap. It may also allow for design-manufacturing "co-roadmapping," which may help gather indications of whether our industry should invest in variability reduction or in design robustness/productivity improvements. Refer to the Design and System Drivers chapters.

5.2. TEST AND TEST EQUIPMENT

Modeling and simulation of test equipment instrument, electrical delivery path, probe card or loadboard, and the device-under-test are required by the Test ITWG. Most important for Test is the signal integrity of power delivery and high speed signals. Whereas modeling of these issues can build especially upon the field of interconnect and package simulation,

some of the issues (e.g., probe card and test socket) to be described are outside the classical domains of simulation considered by the Modeling and Simulation ITWG. It is, however, encouraged that the simulation community would extend their activities to contribute also to these problems which are important to support test activities. Another important aspect is the changing circuit sensitivity which may transfer an originally benign defect into a killer defect in future technology generations. Support from simulation would be important to assess the effect of defects especially on circuit performance. This may help Test to define criteria for defect detection. Wafer thinning or thermal processing during packaging may make a device or circuit fail which was successfully tested at wafer level – it would be very important if simulation could support Test to deal with this problem. Moreover, systematic variations may in Test appear random if their probability is very low - simulation should support a proper classification of such defects. Furthermore, support from Modeling and Simulation is needed to differentiate between a good die which is influenced by intrinsic process variations and a defective die. Especially, a die may be influenced by process variations in a way that is still functional under standard application conditions, but due to insufficient margin fails after temperature or voltage stress employed in reliability tests. Here, support from Modeling and Simulation is needed to provide reliable models for these stressing mechanisms – similar to the link with metrology such models are needed to calculate the reliability data aimed at from the measurement data which are only available under the test conditions which are different from the later use of the circuits. In summary, seamless integration of simulation and modeling into the testing process is an important opportunity for test. (Refer to the Test and Test Equipment chapter.)

5.3. PROCESS INTEGRATION, DEVICES, & STRUCTURES (PIDS)

The key innovations requested by the PIDS chapter include enhanced mobility (leading to strained Si), high-κ dielectrics, metal gate electrodes, elevated source/drain, advanced annealing and doping techniques, Non-Classical CMOS (such as Fully Depleted SOI), and enhanced saturation current which requests ballistic transport. Other partly more long-term issues include atomic-level fluctuations, statistical process variations including line-edge and line-width roughness and SOI thickness, high transport channel materials such as germanium, III/V or carbon nanotubes and nanowires, new interconnect schemes, mixed signal device technology which will drive major changes in process, materials, physics, design, etc. With further shrinking feature sizes, new process steps, architectures and materials reliability issues on device, interconnect and circuit level are getting even more important and need support from Modeling and Simulation to achieve the development speed required. Especially for devices which use SOI or new channel replacement materials, existing models, such as for dopant diffusion and activation, carrier transport or for stress must be extended to cope with interface effects which get increasingly important compared with bulk properties. Many new materials and structures have been proposed, yet currently very little is known about the corresponding failure mechanisms. There has been an increase in process variability with scaling (e.g., distribution of dopant atoms, CMP variations, line-edge roughness). At the same time the size of a critical defect decreases with scaling. These trends will translate into an increased time spread of the failure distributions and, thus, a decreasing time to first failure. We need to develop reliability engineering software tools (e.g., screens, qualification, reliability-aware design) that can handle the increase in variability of the device physical properties, and to implement rigorous statistical data analysis to quantify the uncertainties in reliability projections. Design for Reliability needs simulation tools for concurrent optimization of circuit performance and reliability, and for the simulation of electromigration, thermal-mechanical stress, and process induced charging. Reliability mechanisms that are sensitive to device parameters will couple with variability which is itself increasing with scaling. This will make reliability projection with limited number of measurements extremely difficult and may squeeze out the benefit of scaling. Support e,.g. from Modeling and Simulation to assess and minimize this effect is especially needed Finally, non-classical CMOS devices require the development of appropriate compact models to support their introduction.

These issues are especially included in the Modeling and Simulation subchapters on “Front-End Process Modeling,” “Device Modeling” and “Interconnects and Integrated Passives Modeling.” Furthermore, Non-Classical CMOS devices require the development of appropriate compact models to support their introduction. (Refer to the PIDS chapter.)

5.4. EMERGING RESEARCH DEVICES

Emerging Research Devices increasingly utilizes state variables different from charge (e.g., spin), which require a substantial extension of the current scope of modeling and simulation to the atomic scale. Other objectives are to extend CMOS with high mobility channel replacement materials such as InSb, InGaAs, InAs, InAsSb, Ge and others, and to introduce carbon-based nanoelectronics. The transfer of channel replacement materials such as InGaAs and Ge, and non charge-based device architectures such as STT-MRAM and RRAM from the Emerging Research Devices chapter to the Front-End Processes and PIDS chapters highlights that these materials and architectures approach industrialization and therefore need to be treated by standard simulation tools. For CMOS, the development of means to control the variability of critical dimensions and statistical distributions is a long-term difficult challenge. Additional challenges are to sustain the required reduction in leakage currents and power dissipation in these ultimately scaled CMOS gates and to introduce

these new materials into the MOSFET while simultaneously minimizing the increasing variations in critical dimensions and statistical fluctuations in the channel (source/drain) doping concentrations.

Modeling and simulation are critical in both providing fundamental understanding of the physical mechanisms and processes for both charge-based and non-charge-based information processing technologies and in interpreting metrology for nanotechnology structures. As the size of materials for devices continues to decrease, the impact of interfaces on the measured material properties will make separation of "bulk" and interface properties much more difficult. This increased role of interfaces together with new quantized physical phenomena caused by the nano-scale device structures drives improvement of first principle or *ab initio* modeling. This will allow predictive simulation of nanometer scale material properties and of nanoscale devices with non-charge state variables. To this end, existing tool must be enhanced especially with respect to the modeling of excited states.

Due to the diversity of the Emerging Device Architectures being considered, and its long-term nature, required modeling and simulation cannot be just an extension of current models and tools needed within other areas of the ITRS. New modeling and simulation in the cross disciplinary nano domain must comprehend considerable contributions from other areas such as biology and chemistry. (Refer to the Emerging Research Devices chapter.)

5.5. EMERGING RESEARCH MATERIALS

Emerging Research Materials require basic models that correlate composition, structure, and synthesis to material properties. This includes especially low dimensional material synthesis and properties; spin material properties; and strongly correlated electron material properties. With device dimensions of 22 nm or below, materials modeling or computational materials has become a critical part of technology development and is needed to address several components of technology development. The complexity of materials modeling is increasing due to three reasons: 1) The number of materials has continued to increase (over 3× increases over a period of 20 years), 2) the ratio of surface-to-volume of the material is inversely proportional to the dimension of the structure, and 3) smaller numbers of atoms that could lead to larger statistical variations. These lead to more atoms of different chemical nature being packed in smaller dimensions. As a result, the measured bulk material properties differ from observed materials behavior in nanostructures. Besides this, also macromolecules and pixilated materials are addressed as options for advanced photoresists. Direct self-assembly and deterministic doping are key processes being suggested. Also in the area of Emerging Research Materials metrology must be supported by modeling. Dopants and defects strongly affect various Emerging Research Materials and Devices. To deal with these requirements improvement of first principle modeling is needed to allow predictive simulation of nm scale material properties. A key problem here is that frequently the simulation of excited states is necessary, but not possible with state-of-the-art tools. A platform for different simulation tools, such as TCAD and ab-initio calculations, is a long-term challenge both for ERM and the Modeling and Simulation ITWG. Due to the diversity of the Emerging Device Materials being considered, and its long-term nature, required modeling and simulation cannot be just an extension of current models and tools needed within other areas of the ITRS. In turn, the Emerging Research Materials chapter contains a dedicated modeling section which refers to materials which have so far not been transferred for inclusion into other ITRS chapters such as Front-End Processes, Interconnects or PIDS, which means that the delineation between Modeling is changing in parallel to such transfers. Device architectures transferred to PIDS and in turn also to M&S include some III-V and Ge channels. More details are given in the body of the ERM text. (Refer to the Emerging Research Materials chapter.)

5.6. RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

The requirements on simulation from RF and Analog/Mixed Signal Technologies for Wireless Communications include not only silicon-based substrates but also III-V compounds, various device architectures beyond MOSFET, and the capabilities to simulate frequencies up to 100 GHz and beyond, higher levels of integration, cross-talk among circuit blocks, noise, and signal isolation. These requirements, in turn, increase the need for coupled device/circuit/system simulation of System-on-Chip (SoC) and System-in-Package (SiP); analog device modeling including the protection against electrostatic discharge; accurate and fast 3D electromagnetic and RF simulation and visualization; efficient 3D modeling and simulation for mixed signal circuits; thermal modeling and simulations that are integrated with RF and digital design tools; computationally efficient physical models for carrier transport in compound semiconductors; bandgap engineering; and accurate, fast and predictive Analog/RF compact models. In addition to geometry scaling, the device designer has additional degrees of freedom in device optimization, epi engineering – tailoring of device layers to support high breakdown fields and high mobility/saturation velocity. The III-V devices in this chapter are all formed with epitaxial layers (and not by ion implantation), and even the SiGe HBTs are increasingly formed by epitaxy..

Device matching is a key issue. Simulation of heat generation and removal and thermal dissipation is even more important than for standard CMOS due to the higher power densities typically present in high-speed device operation or in the wide bandgap semiconductors and or if wafer thinning used. The description of analog performance requires process and device simulation to be able to provide sufficient accuracy for prediction of mismatch and 1/f noise, e.g., for new high-κ gate dielectrics. The higher operating frequencies require simulations of the epitaxy steps and the alternative dopants (e.g., C). These aspects are to some extent addressed in the "Device Modeling," the "Interconnect and Integrated Passives Modeling," the "Circuit Element Modeling" and the "Materials Modeling" sections of this chapter. In addition, there is a role for modeling and simulation to assist in design strategies for RF isolation. RF signal isolation must be carefully managed to prevent performance degradation as the wireless communication schemes become more complicated. (Refer to the RF and Analog/Mixed-signal chapter.)

5.7. FRONT-END PROCESSES

The FEP challenges surround the introduction of new materials and of non-classical CMOS. This raises various requirements on Modeling and Simulation. Especially, in the era of material-limited device scaling, material issues need to be addressed in most modeling areas. This includes among others strained materials – so the importance of modeling of stress and strain is further growing. New device architectures, mobility-enhanced channels and alternate interfacial layers request especially large progress in numerical device simulation, together with improvements of the simulation of the process steps used to fabricate these devices, e.g., the formation of shallow junctions. Limited thermal stability of some candidate material systems may request alternative annealing strategies. Both shrinking device dimensions and the non-planar architectures, especially also SOI devices, increase the impact of interfaces because the volumes in between are decreasing. These effects must be appropriately included in the physical process and device models. Upper corners of STI critically affect device behavior and must therefore be accurately modeled. Process and/or material variabilities are getting increasingly important as devices further scale – a premier example is the redistribution of variance allowance between lithography and etching already included in the 2005 roadmap. Variability in the placement of dopant atoms and their final location, along with variations resulting from process control introduced by patterning, cleaning and deposition constitute a dominant scaling challenge, requiring considerable effort in developing new variability tolerant process techniques . Micro-loading among various CDs and various pitches becomes more critical as feature size shrinks. Simulation can and must contribute to assessing the impact of such variations on the final device and chip. The performance and reliability of high-κ dielectrics must be modeled. Measurement of integrated low-k data is an extraction issue which needs simulation. The formation of ultra-shallow, abrupt, highly (non-equilibrium) activated drain extensions continues to be a major challenge, and support from modeling is required both to improve the physical understanding for the processes used (e.g., kinetics of dopants and point defects during annealing) and to subsequently optimize them by numerical simulation. This knowledge is also needed for defect engineering, which aims at achieving shallower junctions by the exploitation of the interaction between dopant atoms and defects. Conformal doping is important for FinFETs and must be treated in simulation. Furthermore, the reduction of critical dimensions (CD) and the control of their variations including Line Width Roughness (LWR) and LER are generally a key issue, and it is highly desirable to use simulation to identify among the many parameters influencing CD the most important ones, in order to minimize experimental effort. (Refer to the Front end Processes chapter.)

5.8. LITHOGRAPHY

Support from Modeling and Simulation is critical both to push the limits of traditional optical and extreme ultraviolet (EUV) lithography and to assess new Next Generation Lithography technologies. Furthermore, an intimate link between equipment-scale and feature-scale simulation is required for state-of-the-art lithography simulation. Equipment scale effects often require modeling with random variables with user-defined or user-measured probability distributions. While calculation of lithographic image formation relies on well-established physical models, the physical/chemical understanding of resist processes, particularly for chemically amplified resists, is far less advanced. Resist models are typically semi-empirical, and they require fitting and calibration with experimental data.

The key requirements for simulation of optical imaging are accuracy, speed of computation, and the capability to model the effects of non-ideal masks, non-ideal lenses, multilayer resists and non-planar substrates. With mask feature sizes at 4x reduction during imaging becoming comparable with the wavelength, polarization effects and the exact mask topography need to be included. Problem-specific algorithms and implementations are needed to deal with the "tricks" used when pushing optical lithography to the limits, such as off-axis illumination, complicated mask geometries including phase-shifting, optical proximity correction (OPC), and double or even multiple exposure/patterning. Especially the latter technique requires the rigorous treatment of wafer topography in the simulation. Tools must be predictive and efficient enough to support source mask optimization (SMO) and inverse lithography (IL).

Non-idealities of the optical system used are getting more and more critical and must be appropriately addressed in simulation. The influence of defects on the mask and on the wafer is becoming more and more important and requires appropriate simulation capabilities especially for the identification of "killer defects".

New techniques used in EUV or future next generation lithography (NGL) techniques, such as replacement of lenses by multilayer mirrors and the use of reflecting masks EUV lithography must be appropriately modeled and included in the simulation programs. Mask pattern generators and some NGL options - including proximity electron lithography and maskless lithography - involve imaging with electrons. Simulations of stochastic space charge effects, geometrical aberrations and electron optical lens design performance using either magnetic or electrostatic lens elements are needed. Direct Self Assembly DSA which is being driven by ERM is another interesting near-term option, which needs to be addressed by simulation. Support from simulation for narrowing down the options for future Next Generation Lithography has been and will continue to be important.

A specific challenge for lithography Modeling and Simulation is to accurately predict the behavior of state-of-the-art photoresists over a wide range of imaging and process conditions. For these, better physical/chemical models must be developed to predict three-dimensional resist geometries after development and process windows, including effects such as Line-Edge Roughness (LER) and Line-Width Roughness (LWR). Better calibration techniques are required both for model development and for customizing models implemented in commercial tools to appropriately describe the photoresists in question. Calibration obviously depends on the quality of input data, e.g., CD measurements. Therefore, it is necessary to better understand and estimate measurement errors. Systematic errors should be dealt with by models of the measurement tools, for example, CD-SEMs. With the growing importance of LWR and LER, lithography simulation needs to contribute to the assessment of their influence on device and interconnect performance (LER) and variability (LWR). Since here not the roughness of the resist patterns is important but that of the etched structures, intimate coupling with etching simulation is indispensable. Simulations of etching are important to understand the relationship between 3D edge roughness and profiles in resist features and the resulting roughness and profiles in etched gates, contacts or trenches. Intimate links with etching simulation must also be established also to predict the geometry of non-ideal mask edges which are frequently result of the mask-making lithography steps. Generally, many challenges are associated with variability control, not just scaling. Variability control not only must keep up with dimensional scaling, but often needs to improve even faster. To further extend optical lithography, new practices are required to better comprehend the increasing variation of critical dimensions as a fraction of the feature size in the design process. These practices are usually referred to as "design for manufacturing" (DFM). DFM allow designers to account for manufacturing variations during circuit design optimization, enabling the IC fabrication process to be optimized to provide the highest performance at a minimal cost. Ultimately, the designer could optimize the circuit with knowledge of all physical variations in the fabrication process and their statistical distribution. Starting with optical proximity correction to put nominal images on target, mask patterns are now designed to improve depth of focus, increase contrast, and reduce MEEF. The scope of computational lithography also includes illuminator design, which has expanded as exposure systems with more versatile illuminators have become available.

A specific requirement for lithography Modeling and Simulation is the need for very efficient simulation tools which allow the simulation of large areas and/or the conduction of simulation studies for a multitude of variations of physical parameters or layouts to support growing design for manufacturing (DFM) needs. In fact, lithographic simulations of full-chip layouts are now needed to verify OPC and phase assignment data to avoid expensive masks being fabricated with errors or with corrections having only marginal performance. These simulations must be reasonably accurate and execute at high speed to evaluate the entire layout in a reasonable amount of time. Furthermore, simulation must contribute to the increased integration between design, modeling, lithographic resolution enhancement techniques and extensive metrology needed to maintain expected circuit performance.

Besides models of image formation and resist profile generation in the lithography process, mechanical models are also critical for designing lithography tools. Refinement and application of finite element methods is important for assuring exposure tools, masks and wafers remain stable enough to meet demanding overlay tolerances. Static and dynamic models of lens mounting stability, stage stability and also aspects of exposure tool hardware design are critical. Static and dynamic mechanical models are also critical for designing adequate mounting methods for masks and wafers to maintain desired position under high stage acceleration values and to maintain desired flatness. Equilibrium and non-equilibrium models of thermal effects are also essential for exposure tool design, especially for modeling heating of the immersion fluid in immersion lithography and its effect on distortion and aberrations. Models of fluid flow for immersion have also been essential in designing fluid delivery systems that minimize immersion-specific defect formation. (Refer to the Lithography chapter.)

5.9. CROSS-CUT BETWEEN INTERCONNECT AND DESIGN AND MODELING AND SIMULATION

The interconnect performance of future technology generations can no longer be provided by material and technology improvements alone. Therefore the interaction between material science, wafer technology, design, modeling, and simulation is becoming of even greater importance in supporting the continuing interconnect scaling. Current interconnect design tools cannot accurately predict the performance of an entire multilevel interconnect system. Furthermore, the models are largely based on RC not RLC parameters. Optimization of designs for maximum performance is often effected by a trial and error method. As frequencies and the number of interconnect layers increase, time to market of many leading edge parts is being impacted by the ability to lay out and choose the correct interconnect routing, (function block placement, interconnect level and corollary line size) to achieve an overall device performance target. The design capability must be significantly expanded to allow users to utilize both the near term and the far term proposed interconnect systems effectively. The upcoming new interconnect challenges are especially:

1. RLC capable models will be needed for systems with 10 GHz and above operation. (30 GHz in free space wavelength is ~1cm). This capability will also be needed for systems using RF or terahertz wave interconnections.
2. The impact of the Cu resistivity increase on delay time must be considered in realistic models. These models need to take into account line width, line aspect ratio, sidewall roughness, metal grain size, and the respective coefficients for grain boundary-, surface- and impurity-scattering.
3. Signal delay uncertainties because of crosstalk effects between neighboring interconnects and the impact of dummy metal features need to be considered in appropriate models. Because of increasing line aspect ratios these effects may become major issues.
4. Process variations (e.g., CD tolerances, line height variations, sidewall roughness, etc.) will become of ever increasing importance with further shrinking of interconnect line and via sizes. They affect not only interconnect performance but also its reliability, e.g. via local field enhancement due to notches with nanometer range and reduced distances caused by LER. Therefore variation tolerant designs and variation sensitive models and simulations are needed to support the upcoming technology generations.
5. A means to optimally place function blocks will be needed for the ‘3D” integrated circuits not only on an individual die but also now on a stack of die.
6. New models must be developed to optimize optical interconnect systems that include emitter and detector latency.
7. All of the above technologies will increase the heat dissipation of the die as a whole and increase the number of occurrences of reliability critical ‘hot spots’ within the die. Predictive thermal models, that can accommodate thermal impacts of low-κ dielectrics with reduced heat conductivity, RF standing waves, the multiple heat generating layers embedded in the 3D IC stack, and heat generated by, as well as thermal performance of optical devices and quantum well devices will be needed.

Modeling and Simulation is a key tool to support all of the technology areas working with the interconnect problem. The required modeling and simulation capabilities range from high-level predictions of interconnect impact on IC layout and electrical behavior (such as signal delay, distortion, and interconnect reliability) to prediction of resistivity increase of further shrinking copper interconnects (due to grain structures, Cu/barrier interfaces and impurities) and the physical structure and properties of new low-κ dielectrics and other more exotic interconnect materials.

In all of these cases Modeling and Simulation should provide predictions accurate enough to reduce as much as possible the need and costs of extensive experiments. These needs span from first simulations carried out to screen the field for well-directed experiments on new interconnect technologies and architectures to predictive capability within experimental error for relatively mature technologies.

As in many other fields of technology, the need in interconnects for Modeling and Simulation is ever increasing due to the larger number of parameters and effects to be included. For example, the introduction of low-κ dielectrics with low thermal conductivity is drastically increasing the need for combined thermal, mechanical, and electrical modeling.

Specific interconnect needs for modeling and simulation include: performance prediction (including grain structure, surface scattering, high frequency effects and reliability) for complex (e.g., 3-D) structures fabricated with real non-idealized processes (including etching, PVD, CMP), with hierarchical capability to choose the appropriate tradeoff between speed and accuracy for the application in question; electro-thermal-mechanical simulations including chip-package-board interactions (CNPI); tools and methodologies to connect product and process designs in an integrated flow to meet target specifications or identify deficiencies; tools to calculate the reliability of interconnects and the degradation

of electrical circuit performance due to resistivity increases over time of interconnect wires and vias, and materials modeling capabilities to predict structure as well as physical and electrical performance of materials used in interconnect structures (metal, barrier and dielectric – including getting more realistic ranges of κ values). Simulation should be able to provide a system level time-dependent interconnect reliability analysis framework. Especially important is the size-dependent resistivity of copper, its surface diffusion and electromigration, time-dependent dielectric breakdown TDDB, and copper thinning and dishing in CMP. The treatment of the variability associated with line edge roughness, trench depth and profile, via shape, double patterning for M1 interconnects, etch bias, and thinning due to cleaning is a key challenge to interconnects and their simulation. Simulation of the variability of trench and via structures in low-κ dielectric material is especially important because variability of interconnects would cause RC degradation (Refer to the Interconnect and Design chapters.)

5.10. FACTORY INTEGRATION

The Modeling and Simulation chapter deals with the physical processes occurring during device fabrication and within a piece of equipment, a device, or circuit. This physical simulation is very different from the discrete simulation of wafer flow, equipment usage, or lot scheduling which are within the core of Factory Integration. Nevertheless, also the physical Modeling and Simulation can and must contribute to the strategic goal of Factory Integration: cost, productivity, and speed.

Especially, the overall objective of physical Modeling and Simulation, to reduce the development times and costs of new technologies and ICs, is in line with one of the Factory Integration goals: to enable rapid process technology shrinks and wafer size changes. Physical Modeling and Simulation can and must contribute to this goal by exploiting equipment, process, device and circuit simulation tools especially to investigate the possibilities and impacts of shrinking the technology initially introduced in a fabrication line to smaller feature sizes, which is vital for the reduction of fabrication costs. Moreover, similar to the Yield Enhancement chapter also for Factory Integration the use of physical Modeling and Simulation to investigate the influence of process variations on the amount of devices and ICs which are within product specifications is highly important. This can also help to increase the productivity of equipment: For example, in the 2011 Factory Integration chapter statistical control of process equipment was requested. Using such quantitative data on equipment variability, simulation can be useful to quantify the impact on device or IC performance of variations within an equipment or between different pieces of equipment as well as of process variations (for example, in lithography) and in this way contribute to the right strategy for efficient use of the equipment or appropriate optimization of the process flows to achieve the highest yield. Specific support from physical Modeling and Simulation is needed in the area of APC (Advanced Process Control) and Forward/Backward Control: Here, efficient physical process models are needed to be able to adapt process steps to compensate for deviations which occurred in preceding steps or for process drifts which frequently occur between the regular maintenance and calibration processes of the equipment used. In this context the key requirement on physical Modeling and Simulation is not the development of predictive (sometimes even three-dimensional) models but of simplified and computer-efficient tools which in the ideal case allow for in-line and real-time application, coupled with in-situ or in-line metrology and APC software. (Refer to the Factory Integration chapter.)

5.11. ASSEMBLY AND PACKAGING

The rapid change in package requirements as new packaging processes and architectures are adopted places a premium on modeling and simulation tools to speed the introduction of new packages that successfully meet all requirements. The cross-cut needs from Assembly and Packaging to Modeling and Simulation consist of co-design in three respects: Between chip and package; including as well mechanical, electrical, thermal, and reliability simulation; and co-simulation of RF, Analog/mixed signal, DSP, EM, and Digital. They are closely related to the requirements on Modeling and Simulation raised from the Interconnect chapter. Additionally, lower voltages and higher currents have significantly increased the need for chip-package co-design to minimize the effects of high-current transients on very low-level signal lines. RF/mixed signal models are needed, and modeling tools need to be extended to enable the simulation of complex SoC and SiP packages.

Assembly and Packaging technologies are driven to simultaneously meet very demanding requirements in the areas of performance, power, junction temperature, and package geometries, but also with respect to reliability and lifetime. Advanced modeling tools covering the related electrical, thermal, mechanical and reliability aspects are needed to support the development and optimization of these technologies. In-depth knowledge of failure mechanisms is essential. Especially important is that these effects can no longer be treated separately and must, in turn, also simultaneously be simulated. Whereas the requirements in terms of processes, materials, and effects to be included in Modeling and Simulation are rather similar to those raised by the Interconnect chapter, the key additional requirement is the need to manage the large complexity and configurations of chip-package co-designs, including thinned wafers and Through-

Silicon-Vias, and length scales varying from nm to cm. This requests memory and CPU efficient hierarchical simulation capabilities to be able to deal with the high clock frequencies and high densities occurring. Reduction techniques in time-domain or frequency-domain are needed as well as computationally efficient full-wave simulation tools. Thermal and mechanical models used must be based on realistic material data, including air flow, stress predictions in accelerated test, micro-models for interface fracture behavior, and macro structure models for package dynamics behavior including vibration and mechanical shock. Understanding material interfaces for metal/polymer, polymer/polymer, and intermetallics for process development and reliability projection will be extremely important. Thinned die, low-κ and other new materials and new package types such as stacked die and other 3D circuits must be included. Frequently material behavior and parameters of thin layers are different from their bulk counterparts and therefore need to be newly established. Material properties data are needed over a large range of loading and environmental conditions. Models need also to include manufacturing and assembly processes such as adhesive/undersell flow or BGA rework. Simulation methods to predict reliability limited, for example, by electromigration, thermal migration and hot spots are needed to speed up development processes. Similar to interconnects, noise and crosstalk must be simulated and minimized. From the view of packaging, design and process tolerances should be taken into account especially for backend of the line. Also for packaging simulation faster simulation capability is needed because currently simulation sometimes takes days.

The proliferation of new package architectures combining multiple active and passive devices in a single package SiP have increased the need for modeling and simulation tools. Such structures cannot meet cost and reliability requirements without the ability to simulate thermal, mechanical, and electrical properties of the complete SiP.

It is anticipated that near-term Modeling and Simulation needs of Assembly and Packaging will be addressed by non-optimally combining available capabilities, or by evolutionary extension of these capabilities. In the longer term it is desired that a more complete system approach will be provided. Full integrated modeling and prediction of 3D chips and packages is required. (Refer to the Assembly and Packaging chapter.)

5.12. Environment, Safety and Health

Also Modeling and Simulation is requested to respond to ESH issues. Obviously, there is a major positive effect from the use of simulation for the reduction of the numbers of wafers needed during process development and optimization, which saves costs and (partly ESH-relevant) resources. Moreover, simulation should also contribute to the reduction of resources including critical chemicals during production, by minimizing deposited wafer thicknesses, material removal in CMP, and the frequency of cleaning processes to the amount really needed to achieve the desired result in terms of device and IC performance and reliability. To this end not only appropriate models and simulation tools must be available, similar to the requests by the other chapters, but also resource conservation must be introduced as an additional target figure and metric for simulation.

For the optimization of ESH issues, the elementary chemical reactions in each relevant process must be understood as far as possible, and new measurement and evaluation methods must be implemented for developing processes which have the lowest ESH impact. Similarly, availability of these measurement methods and knowledge of the reactions is also a key requirement for the development of predictive models for those processes, which are dealt with in the Modeling and Simulation chapter. In turn, many enabling measurement techniques can be shared between ESH and the Modeling and Simulation community, although the final targets of the two areas are different: Assessment of material consumption and occurrence of hazardous species for ESH versus the geometry, doping, and morphology of layer stacks in Modeling and Simulation. Moreover, the implementation of such models in equipment simulation programs, especially for plasma processes, also offers the possibility to ESH to obtain quantitative data on the generation of hazardous species and in the ideal case also for optimization of equipment and process conditions to minimize the generation of these species or their release from the process equipment. Moreover, simulation can frequently contribute to characterization techniques by converting measured data (like spectra) into quantitative data (for example, on gas composition). See the cross-cuts with Metrology. In this way ESH and Modeling and Simulation have the potential to support each other well. (Refer to the ESH chapter.)

5.13. Yield Enhancement

Besides the standard use of Modeling and Simulation to reduce development times and costs, links between Yield Enhancement and Modeling and Simulation are twofold: First, Modeling and Simulation can contribute to the assessment of the influence of defects on the ICs. An obvious example is the question whether mask defects of a specific size, kind, and position are printed during an optical or EUV lithography and subsequent etching steps. This can be studied by state-of-the-art lithography simulation tools, which also allows identification of critical defect sizes above which the device or IC is destroyed, for example because the defect will cause otherwise separate lines to be connected. Especially for the investigation of defect limits for patterning steps simulation offers very good prospects provided the simulation tools are

further developed accordingly. The propagation of defects in subsequent process steps through to devices and ICs and the mutual interactions of defects can be studied with various other Modeling and Simulation tools to monitor and minimize their impact. In this way Modeling and Simulation could in many cases best answer the question whether a certain kind of defect at a certain stage of processing is critical or not, and what could be its corresponding threshold size.

Another important problem is the assessment of the impact of largely inevitable process fluctuations on the performance of devices and ICs. Many parameters in a fabrication line are distributed around their nominal values with some tolerances, like focus positions and illumination doses in lithography, anneal temperatures, times, and ramp profiles, or have some drift in time. Advanced process control (APC) is frequently used to reduce the impact of such fluctuations by feeding metrology data back into process recipes. Control models are largely based on silicon data that is expensive to generate and might be available for mature processes only. Coupled process and device simulations can help to develop more accurate APC models in shorter time. By using process and device models calibrated in the process integration phase, APC models can already be developed for process transfer and production ramp up.

A second method addressing the problem of process fluctuations uses coupled process and device simulation to calculate the spread of critical product parameters resulting from such distributions of fabrication parameters, or the intrinsic variability of process steps (e.g., line edge roughness and other CD variations) or dopant fluctuations. Using this method statistical SPICE models can be derived before statistical fabrication data is available, and in this way contribute to the early assessment and optimization of the yield for a specific product and fabrication technology. Effects which are of most concern to yield enhancement have already in 2005 included line edge roughness, the impact of which can be well assessed with (especially lithography) process simulation. Moreover, process variations and defects are frequently closely related: A variation may gradually change a continuous variable like a line width in a way that devices or ICs suffer a discontinuous change, e.g., that a line is interrupted in a subsequent process step. This problem was already mentioned in the 2007 Yield Enhancement chapter: “Where does process variation stop and defect start?” In such cases a defect which seems to be random in nature can in reality be due to a systematic mechanism, like limited depth-of-focus in optical lithography. Simulation can be used to detect and quantify such effects. In turn, already in the 2007 and 2009 Yield Enhancement chapters it was stated: “Research into precise yield model assisted by TCAD is becoming important because SMLY (Systematic Mechanisms Limited Yield) issues tend to restrict yield ramping rate and attainment level.”

Obviously, these contributions from Modeling and Simulation to Yield Enhancement require sufficient generality, accuracy, and speed of application of the simulation tools to be used, and are a challenge for the future development of Modeling and Simulation. (Refer to the Yield Enhancement chapter.)

5.14. METROLOGY

Strong bi-directional links exist between Metrology and Modeling and Simulation. A key issue in the development of physical models for semiconductor fabrication processes and equipment as well as devices is the availability of measurement techniques and methodologies that are capable of characterizing quantities such as geometry and chemical composition of layer stacks, dopant distributions, (point) defects, stress/strain, carrier concentrations, lifetime and mobility with the high accuracy and spatial resolution, and low detection limit required to enable model development and evaluation. Metrology is needed that gives sufficient information for true three-dimensional structures. In many cases it must be applicable to real structures rather than test structures designed for that specific purpose. A further complication results from the required measurement and model accuracy approaching or even getting lower than the distance between individual (dopant) atoms. In these cases the interpretation of measurement results becomes questionable, whereas in simulation the transition from continuum models based on partial differential equations to atomistic calculations is being accomplished. Moreover, the introduction of new materials and new device architectures frequently gives rise to the need to characterize quantities which were not existing or not relevant before – especially here Modeling and Simulation needs accurate and reliable measurements to enable model development and the extraction of the required parameters.

The requirements of Modeling and Simulation contribute to driving the development of Metrology. However, simulation not only raises requirements but also can and must contribute to the development and use of metrology itself. The physical understanding of the processes occurring in the semiconductor and other materials considered is in many cases extremely valuable or even indispensable to interpret data collected in metrology and to convert them into quantitative information, to give realistic error estimates, and even to design or customize a measurement method. Generally speaking, Metrology has repeatedly confirmed its requirement to “use modeling to connect what you can measure with what you can see” —and related issues mentioned in the Metrology chapter are manifold, see the Metrology chapter. For example, simulation can be used to relate variations of process parameters or atomic fluctuations to spreads of quantities that are measured, and in this way help to correctly interpret measurements: Quantify how much the variation of the variable to be measured on one hand side and the error of the measurement method on the other hand side contribute to the variation and repeatability of the measurement signal recorded. Some other examples are the use of simulation to support and

complement mask metrology, scatterometry, and the application of metrology for APC. Frequently a layer or a device is during characterization stressed by temperature or voltage, for example, in a way which is quite different from its standard operation conditions, but needed to shorten measurement times to acceptable values, or specific test structures are used which however change the quantity to me measured, e.g., in case of mechanical stress. Also in such cases reliable modeling tools are needed to calculate the quantity of interest from the signal which was more or less modified by the measurement itself—currently, insufficient knowledge about the physical mechanisms involved and in turn the lack of appropriate simulation support frequently invalidates the measurement result.

Frequently modeling groups directly contribute to the development and customization of measurement methodologies required to provide the data needed for model development. For example, with the increasing variety of new materials and processes in gate etch processes and complexity of gases and materials involved in dielectric etch and process cleans, simulation is called for creating a reliable means to characterize process emissions. In most cases, what evolves from surfaces or in the gas phase is unknown or difficult to synthesize outside of the particular process set-up and equipment. An emerging means of identifying species of potential environmental risk is through computational spectra generation. Synthetic reference spectra for materials can be generated with relative ease using computational chemistry approaches. For example, FTIR (Fourier-Transform Infrared Spectroscopy) spectra have been used to identify radicals of the RuOx system in Ruthenium etch processes and to scan for noxious gases to ensure they are not produced in highly polymerizing dielectric etch gas chemistries. In both these cases, experimental reference spectra are difficult to generate or difficult to obtain.

Furthermore, it is frequently possible to verify simulation models and tools using measurement methods available (such as 2D measurement of cross sections), and then to use them beyond the domain directly accessible to measurement techniques (for example, for 3D profiling) because in that cases the physics has not changed and the difference between the two situations can reliably be handled by the algorithms in the simulator (solving partial differential equations in three instead of two dimensions). To conclude, Metrology and Modeling and Simulation must continue and even further extend their efforts to cooperate closely to take best advantage from each other. (Refer to the Metrology chapter.)

5.15. MEMS

Compared with memory and logic devices, interconnects and packages discussed in the paragraphs above, for MEMS additional materials, processes and structures are needed. Besides this, (electro-thermo-)mechanical effects get even more important that for the other applications mentioned above.

In turn, modeling and simulation for MEMS on one hand needs and uses many of the capabilities already available or requested for transistors, interconnects and packages. On the other hand, some processes get more important, new processes come into play, new materials are added, and different structures need to be addressed. This results in additional requirements for simulation: Additional polymers, eutecticum, contact materials (touching, bonding, temporary) need to be considered. Besides or instead of costly projection lithography, proximity/contact lithography must be simulated. For deposition, other processes such as embossing, imprint, inkjet must be included, and the impact on mechanical properties gets even more important. Whereas stress simulation is already a key requirements in other areas, simulation of stinction e.g. due to surface tension must be included. Furthermore, the capping of cavities by bonding or sealing must be addressed, with the cavities being under pressure or in vacuum. Various kinds of flows (laminar, capillary, electroosmotic, electrophoresic, ….) and also migration of gas through material must be addressed in MEMS performance modeling, together with the simulation of electrostatics and electromagnetics already inherited from other areas.

These additional requirements from MEMS need to be addressed especially in the M&S subchapters on Material Modeling, Lithography Modeling, Process Modeling, and Package Simulation. Extension of the respective sections is in progress but now yet finalized.