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DisplayPort™ Standard

DisplayPort Standard

Version 1.1

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Purpose

The purpose of this document is to define a flexible system and apparatus capable of transporting video, audio and other data between a Source Device and a Sink Device over a digital communications interface.

Summary

The DisplayPort™ standard specifies an open digital communications interface for use in both internal connections, such as interfaces within a PC or monitor, and external display connections, including interfaces between a PC and monitor or projector, between a PC and TV, or between a device such as a DVD player and TV display.

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Genesis Microchip Inc.	Jeffrey Lin (jeffrey.lin@gnss.com)	Pending U.S. Patent Applications 10/726,794 (Claims 1-3, 5-23, 26-44, 45, and 46) 10/726,802 (Claims 2-7, 9-14, and 16-20) 10/726,438 (Claims 2-22, and 24-27) 10/727,131 (Claims 1-16) 10/726,440 (Claims 1-33) 10/726,350 (Claims 2-18) 10/726,362 (Claims 1-18) 10/726,895 (Claims 1-18) 10/726,441 (Claims 1-3, and 5-17) 10/726,934 (Claims 1-8)
JAE Electronics, Inc.	Mark Saubert (saubertm@jae.com)	U.S. Patent 6,315,616 (Claims 9, 11, 14) Pending U.S. Patent Application 10/287,925
Molex Inc.	Scott Sommers (scott.Sommers@molex.com)	U.S. Patent 6,280,209 (at least Claim 1) 6.457,983 (at least Claims 1 and 23) 6,575,789 (at least Claim 1) Pending U.S. Patent Applications 10/246,289 11/190,138

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Intel Corp.	Lakshmi Uppala (Lakshmi.k.uppala@intel.com)	Intel believes it may have intellectual property relevant to the practice of the specification which is related to High-bandwidth Digital Content Protection ("HDCP"). Intel commits to license such intellectual property on reasonable and non-discriminatory term under the HDCP license procedures set forth at http://www.digital-cp.com/home

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Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

If you have a product, which incorporates DisplayPort, you should ask the company that manufactured your product for assistance. If you are a manufacturer, VESA can assist you with any clarification you may require. Submit all comments or reported errors in writing to VESA using one of the following methods.

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Acknowledgements

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Revision History

DisplayPort Version 1 May 2006

Initial release of the DisplayPort standard

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Revised to clarify details; introduce the class of ‘hybrid device’; extend support for content protection schemes to include HDCP; and change requirements for power at DisplayPort connectors.

1 Introduction

DisplayPort is an industry standard to accommodate the growing broad adoption of digital display technology within the PC and CE industries. It consolidates internal and external connection methods to reduce device complexity, supports necessary features for key cross industry applications, and provides performance scalability to enable the next generation of displays featuring higher color depths, refresh rates, and display resolutions.

1.1 DisplayPort Specification Organization

The DisplayPort specification is organized into the following sections that define the overall architecture and structure of the display interface:

Chapter 1 –Introduction

The introduction chapter defines the high level industry needs for DisplayPort, and the resulting technical objectives that the protocol, electrical, and mechanical sections are intended to satisfy. This chapter also includes a glossary of terms for the overall specification, references, and overview of DisplayPort architecture.

Chapter 2 –Link Layer

The link layer chapter describes the protocol specification for configuring and managing the flow of data over both the forward (host to display) transport channel and the auxiliary bi-directional channel.

Chapter 3 – Physical Layer

The physical layer chapter describes the electrical specification of the DisplayPort transmitter and receiver implementations. It also defines the required circuitry and encoding methodology for transmitting data to and from the DisplayPort Link Layer over a cable or circuit board traces.

Chapter 4 – Mechanical

The mechanical chapter defines the connector and cable specification for both internal and external DisplayPort connectors used to convey the electrical signals defined by the DisplayPort physical layer.

Chapter 5 – Source/Sink Device Interoperability

The device and link media requirements chapter describes the device and display formats required to support interoperability between source and Sink Devices that implement DisplayPort connections.

1.2 DisplayPort Objectives

This DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability for broad application within PC and consumer electronics (CE) devices. The interface is designed to support both internal chip-to-chip and external box-to-box digital display connections. Potential internal chip-to-chip applications include usage within a notebook PC for driving a panel from a graphics controller, and usage within a monitor or TV for driving the display component from a display controller. Examples of box-to-box applications for DisplayPort include display connections between PCs and monitors, projectors, and TV displays. DisplayPort is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and television displays.

DisplayPort is designed to meet several key needs within the PC and CE industries as defined in section 1.2.1. These industry needs are expanded into a set of technical objectives in section 1.2.2 for the DisplayPort specification to ensure that the display interface can support current and future industry requirements.

Specific objectives for external and internal display connections are defined in sections 1.2.3 and 1.2.4 respectively for the DisplayPort specification. Section 1.2.5 defines the additional objectives for CE devices applications.

1.2.1 Key Industry Needs for DisplayPort

The following PC and CE industry needs were considered in the development of the DisplayPort architecture and resulting interface specification:

1) Drive maximum application and re-use of digital technology to enable reduced device costs associated with implementing a digital display connection.
2) Enable a common signaling methodology for both internal and external display connections to reduce device complexity and promote commoditization.
3) Enable an extensible architecture that supports an optional robust content protection capability that may be economically implemented.
4) Enable high quality optional digital audio transmission capability.
5) Enable higher levels of silicon integration and innovation within rendering and display devices to reduce device complexity and enable digital interface commoditization.
   Examples of potential DisplayPort integration capability include transmitter integration within a graphics or display controller, and receiver integration within a timing controller on a module.
6) Simplify cabling for internal and external digital display connections.
7) Address performance concerns with existing technologies by providing higher bandwidth over fewer wires.
8) Apply embedded clock architecture to reduce electromagnetic interference (EMI) susceptibility and physical wire count.
9) Provide a small form factor connector that can be plugged in by feel, and whose design will enable four connectors to be placed on a full height Peripheral Component Interconnect (PCI) card bracket.
10) Enable broad PC and CE industry via an open and extensible industry standard.

DisplayPort addresses these industry needs by defining an electrical and protocol specification that may be readily implemented in module timing controllers, graphics processors, media processors, and display controllers.

A forward drive channel is defined that is scalable from one to four lanes, and implements a micro-packet architecture that supports variable color depths, refresh rates, and display pixel formats. A bi-directional auxilary channel is defined that also implements micro-packet architecture for flexible delivery of control and status information.

DisplayPort includes a mechanical specification that defines a small, user-friendly external connector that is optimized for use on thin profile notebooks in addition to allowing up to four connectors on a graphics card. A standard module connector for internal applications is also defined in the mechanical section of the specification.

1.2.2 DisplayPort Technical Objectives

The cross industry needs defined for DisplayPort above may be translated into specific technical objectives. These technical objectives are:

1) Provide a high bandwidth forward transmission link channel, with a bi-directional auxiliary channel capability.

2) Provides application support for up to 10 Gbps (giga bits per second) forward link channel throughput to address long term PC industry needs to support greater than QXGA (2048 x 1536) pixel format and greater than 24 bit color depths.

3) Provides application support for up to 1 Mbps (mega bit per second) auxiliary channel throughput with a maximum latency of 500 micro-seconds

4) Supports variable color depth transmission of 6, 8, 10, 12 or 16 bits per component

5) Supports EMI compliance to FCC/CISPR B standard with a margin of at least 6db

6) Supports existing VESA and CEA standards where applicable.

7) Architecture that does not preclude legacy transmission support (e.g. DVI and LVDS) to and from DisplayPort components.

8) Supports hot plug and unplug detection and link status failure detection

9) Supports full bandwidth transmission via direct drive over a two meter cable.

10) Supports reduced bandwidth transmission via direct drive over a 15 meter cable. DisplayPort supports a minimum of 1080p lines at 24bpp, 50 / 60 Hz over 4 lanes at 15 meters.

11) Supports audio skew of less than 1ms

12) Supports a bit error rate of 10^{-9} for raw transport per lane, and 10^{-12} symbol error rate for audio and control data after ECC encoding / decoding.

13) Supports sub 65 nanometer (0.065 micron) process technologies for integration in Source Devices, and supports 0.35 micron process technologies for integration in Sink Devices.

1.2.3 DisplayPort External Connection Objectives

For external connections between a Source Device and a Sink Device, the DisplayPort specification is designed to achieve the following technical objectives:

1) Supports reading of the display EDID (Extended Display Identification Data) whenever the display is connected to power, even trickle a.c. power.

2) Supports DDC/CI (Display Data Channel/Command Interface) and MCCS (Monitor Control Command Set) command transmission.

3) Supports external display configurations that do not include scaling, a discrete display controller, or on screen display (OSD) functions, enabling low cost, digital monitors.

4) For external notebook PC applications, DisplayPort allows support for direct drive through a docking connector configuration. A repeater function in the dock is strongly recommended.

5) The external DisplayPort connector is identical for all display applications and provides support for four lanes. Captive cables may support one. Two or four lanes to reduce cost.

6) The external DisplayPort connector includes a multi-purpose power pin.

7) The external DisplayPort connector is symmetrical such that the same connector may be used on both source and Sink Devices.

8) The external DisplayPort connector supports connection without the need for visual alignment.

9) The external DisplayPort connector is sized to allow four connectors to fit on a standard full height ATX/BTX bracket opening for PCI, AGP (Accelerated Graphics Port), and PCI-Express add in cards.

1.2.4 DisplayPort Internal Connection Objectives

For internal connections such as within a notebook PC, or within a display, the DisplayPort specification is designed to achieve the following technical objectives:

1) DisplayPort defines a common module connector to simplify internal device connections.
2) The number of lanes in the internal cable is implementation dependent, and may be one, two or four.
3) Internal DisplayPort connections may support both maximum and reduced link bandwidths.
4) Internal DisplayPort connections support low link power modes.
5) Hot plug support for internal DisplayPort connections is implementation dependent.

1.2.5 DisplayPort CE Connection Objectives

For application to consumer electronics devices, the DisplayPort specification is designed to address the following technical objectives:

1) DisplayPort optionally delivers digital audio data concurrent with display data.
2) Provides support for maintaining synchronization for delivery of audio and video data to within +/- 1ms.
3) DisplayPort architecture supports an optional robust content protection capability that may be economically implemented.
4) DisplayPort supports equivalent functionality to the feature sets defined in CEA-861-C for transmission of high quality uncompressed audio-video content, and CEA-931-B for the transport of remote control commands between sink and Source Devices.
5) DisplayPort supports variable audio formats, audio codings, sample frequencies, sample sizes, and audio channel configurations. DisplayPort supports up to eight channels of LPCM (Linear Pulse Code Modulation) audio at 192 kHz with a 24 bit sample size.
6) DisplayPort supports variable video formats based on flexible aspect, pixel format, and refresh rate combinations based on the VESA DMT and CVT timing standards and those timing modes listed in the CEA-861-C standard.
7) DisplayPort supports industry standard colorimetry specifications for consumer electronics devices including RGB and YCbCr 4:2:2 and YCbCr 4:4:4.

1.2.6 Content Protection for DisplayPort

For implementations of the DisplayPort interface where content protection is desired, it is recommended that either DPCP (Display Port Content Protection) Version 1.0 or HDCP Version 1.3 be used. This is recommended in order to minimize incompatibilities between DisplayPort devices in the market.

1.3 Acronyms

Table 1-1: List of Acronyms

Acronym	Stands For
API	Application Programming Interface.
BER	Bit Error Rate
bpc	Bits Per Component

Acronym	Stands For
bpp	Bits Per Pixel
CDR	Clock-to-Data Recovery
CEA	Consumer Electronics Association
CP	Content Protection
CVT	Coordinated Video Timings
DB	Data Byte
DDC/CI	Display Data Channel/Command Interface
DPCP	DisplayPort Content Protection
DPCD	DisplayPort Configuration Data
DJ	Deterministic Jitter
DMT	Discrete Monitor Timing
DP	DisplayPort
ECC	Error Correcting Code
E-DDC	Enhanced Display Data Channel
EDID	Extended Display Identification Data
EOS	Electrical Over-Stress
ESD	Electro Static Discharge
GPU	Graphics Processor Unit
HB	Header Byte
HBR	High Bit Rate
HDCP	High-bandwidth Digital Content Protection
HPD	Hot Plug Detect
ISI	Inter-Symbol Interference
LFSR	Linear Feedback Shift Register.
lsb	Least Significant Bit
Maud	M value for audio
MCCS	Monitor Control Command Set
msb	Most Significant Bit
Mvid	M value for video
Naud	N value for audio
nb	nibble
Nvid	N value for video
NORP	Number Of Receiver Ports
OCP	Over Current Protection
OUI	Organizational Unique ID
PB	Parity Byte
PCB	Print Circuit Board
PRBS	Pseudo Random Bit Sequence
RBR	Reduced Bit Rate
RJ	Random Jitter
RTL	Register Transfer Level
SSC	Spread Spectrum Clock
TCON	Timing Controller
TDR	Time Domain Reflectometry
TIA	Timing Interval Analyzer

Acronym	Stands For
TIE	Timing Interval Error
TU	Transfer Unit
UI	Unit Interval
VB-ID	Vertical Blanking ID
VESA	Video Electronics Standard Association
VHDL	Very high speed integrated circuit Hardware Description Language

1.4 Glossary

Table 1-2: Glossary of Terms

Terminology	Definition
ANSI 8B/10B	Channel coding specification as specified in ANSI X3.230-1994, clause 11
AUX CH	Half-duplex, bi-directional channel between DisplayPort transmitter and DisplayPort receiver. Consists of 1 differential pair transporting self-clocked data. The DisplayPort AUX CH supports a bandwidth of 1Mbps over DisplayPort link. DisplayPort Source Device is the master (also referred to as AUX CH requester) that initiates an AUX CH transaction. DisplayPort Sink Device is the slave (also referred to as AUX CH replier) that replies to the AUX CH transaction initiated by the requester.
Box-to-box connection	DisplayPort link between two boxes that is detachable by an end user. A DisplayPort cable-connector assembly for the box-to-box connection shall have four Main Link lanes.
Bpc	Bits per color, the number of bits for each of R,G, B or Y, C_b, and C_r.
Bpp	Bits per pixel, the number of bits for each pixel. For RGB and YC_bC 4:4:4, the bpp value is three times the bpc value. For YCbCr 4:2:2, the bpp value is two times the bpc value.
Captive cable	DisplayPort cable that is attached to Sink Device and cannot be detached by an end user. Captive DisplayPort cable may have one, two, or four Main Link lanes, while end-user-detachable cable is required to have four Main Link lanes.
Branch Device	Devices located in between root (Source Device) and leaf (Sink Device). Examples are: - Repeater Device, - DisplayPort to legacy converter, - Legacy to DisplayPort converter, - Replicater device, - Composite device. For definitions of these Branch Devices, refer to section 2.1.4.
CEA range	Nominal zero luminance intensity level at 16 for 24 bpp, 64 for 30 bpp, 256 for 36 bpp, and 1024 for 48 bpp. Maximum luminance intensity level at maximum code value allowed for bit depth, namely, 235 for 24 bpp RGB, 940 for 30 bpp RGB, 3760 for 36 bpp RGB, and 15040 for 48 bpp RGB. **Note:** The RGB CEA range is defined for 24, 30, 36, 48 bpp RGB only.
Debouncing timer	A timer that counts the "debouncing period" to elapse after a mechanical contact (for example, plugging in a cable-connector assembly to a receptacle connector) to give the signals on the connectors time to settle.
De-spreading	An operation by a Sink Device for getting rid of down-spread of the stream clock when the clock is regenerated from the down-spread link symbol clock.
DPCP	DisplayPort Content Protection - one of the content protection system options for the DisplayPort link. **Note:** DPCP is not part of the DisplayPort standard.
DisplayPort receiver	Circuitry that receives the incoming DisplayPort Main Link data. It also contains the transceiver circuit for AUX CH.
DisplayPort transmitter	Circuitry that transmits the DisplayPort Main Link data. Also contains the transceiver circuit for AUX CH.
DisplayPort Configuration Data (DPCD)	Mapped to the DisplayPort address space of DisplayPort Sink Device. A DisplayPort Source Device reads the receiver capability and status of the DisplayPort link and the Sink Device from DPCD address. In addition, DisplayPort Source Device writes to the link configuration field of DPCD to configure and initialize the link.

Terminology	Definition
Down-spread	Spreading a clock frequency downward from a peak frequency. As compared to "center-spread", avoids exceeding the peak frequency specification.
Embedded connection	DisplayPort link within a box that is not to be detached by an end user. DisplayPort cable for the embedded connection may have one, two, or four Main Link lanes.
Gen-lock	Locking the output timing of a circuit to the input timing. For example, the DisplayPort receiver may Gen-lock its DE output timing to the timing of DE signal it receives from a transmitter on the other end of the link.
HDCP	High- bandwidth Digital Content Protection - one of the content protection system options for the DisplayPort link. **Note:** HDCP is not part of the DisplayPort standard.
HPD Pulse	There are two kinds of HPD (Hot Plug Detect) pulse depending on the duration. - A Sink Device, when issuing an IRQ (interrupt request) to the Source Device, must generate a low-going HPD pulse of 0.5ms → 1ms in duration. Upon detecting this "IRQ HPD pulse", the Source Device must read the link / sink status field of the DPCD and take corrective action. - When a source detects a low-going HPD pulse longer than 2ms in duration, it must be regarded as a hot-plug-event HPD pulse. Upon detecting this hot-plug-event HPD pulse, the source must read the receiver capability field and link / sink status field of the DPCD and take corrective action.
Hybrid device	A Branch Device responsible for transporting data between one or more Sources Devices to one or more Sink Devices by means other than that provided for by the physical layer as defined in chapter 3 and mechanical, cable-connector assembly specifications as defined in section 4.1. A hybrid device may use alternative wired or wire-free means including optical or radio technology. Such a device shall transport the Link Layer as defined in chapter 2. The interfaces of hybrid devices must meet the interface requirements of both Source and Sink Devices.
Idle pattern	Link symbol pattern sent over the link when the link is active with no stream data being transmitted.
Leaf Device	Sink Device, located at a leaf in a DisplayPort tree topology.
Link clock recovery	Operation of recovering the link clock from the link data stream.
Link layer	Server providing services as instructed or requested by the stream- / link-policy maker.
Link policy maker	Manages the link and is responsible for keeping the link synchronized. All DisplayPort devices must have a link policy maker.
Link symbol clock	Link symbol clock frequency is 270 MHz for 2.7 Gbps per lane, while it is 162 MHz for 1.62 Gbps per lane.
Main link	Uni-directional channel for isochronous stream transport from DisplayPort Source Device to DisplayPort Sink Device. Consists of 1, 2, or 4 lanes, or differential pairs. Supports 2 bit rates: 2.7Gbps per lane (referred to as "high bit rate") and 1.62Gbps per lane (referred to as "low bit rate" or "reduced bit rate").
Main stream attributes	Attributes describing the main video stream format in terms of geometry and color format. Inserted once per video frame during the video blanking period. Used by the DisplayPort receiver in reconstructing the stream.
Physical layer (PHY)	Consists of logical and electrical sub-blocks. The physical layer decouples data transmission electrical specifications from the DisplayPort link layer.

Terminology	Definition
PRBS7	7-bit pseudo random bit sequence according to ITU-T Recommendation O.150, "General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment", May 1996 G(x) = x^7 + x^6 + 1 (non-inverted signal) Length of sequence = 127 bits The actual sequence must be: ----- direction ----->* 0010000011000010100 0111100100010110011110101001 1111010000111000100100110 11 0101101111011000110100101 11 0111001100101010111111 10000 Note: Upper left transmitted first and lower right transmitted last.
Rendering function	Function of displaying / processing the stream data. For example, video display, speaker, and format converter.
Root Device	Source Device, located at a root in a DisplayPort tree topology.
Secondary data	Data transported over the Main Link which is not main video stream data. Audio data and InfoFrame packet are examples.
Sink Device	Contains one sink function and at least one rendering function, and is a Leaf Device in a DisplayPort tree topology.
Sink function	Sink functionality (reception of stream) of DisplayPort
Source Device	Contains one or more source functions and is a root in a DisplayPort tree topology.
Source function	Source functionality (transmission of stream) of DisplayPort
Stream clock	Used for transferring stream data into a DisplayPort transmitter within a DisplayPort Source Device or from a DisplayPort receiver within a DisplayPort Sink Device. Video and audio (optional) are likely to have separate stream clocks
Stream clock recovery	Operation of recovering the stream clock from the link symbol clock.
Stream policy maker	Manages transportation of an isochronous stream.
Symbol	There are data symbols and control symbols. Data symbols contain 8 bits of data and are encoded into 10-bit data characters via channel coding as specified in ANSI X3.230-1994, clause 11 (abbreviated as "ANSI 8B/10B" in this document) before being transmitted over a link. DisplayPort also defines nine control symbols used to frame data symbols. Control symbols are encoded into nine of the twelve 10-bit special characters of ANSI 8B/10B (called K-codes).
TCON	Timing controller circuit that outputs control and data signals to driver electronics of a display device.
Time stamp	A value used by a clock circuit in order to keep two systems synchronized
Transfer unit (TU)	Used to carry main video stream data during its horizontal active period. TU has 32 to 64 symbols per lane (except at the end of the horizontal active period), each consisting of active data symbols and fill symbols.
Trickle power	Power for Sink Device that is sufficient to let the Source Device read EDID via the AUX CH, but insufficient to enable Main Link and other sink functions. For sink to drive the HPD signal high, at least the trickle power must be present. The amount of power needed for the trickle power is sink implementation specific.
VB-ID	Data symbol indicating whether the video stream is in vertical blanking interval, whether video stream is transported, and whether to mute audio.
VESA range	Nominal zero luminance intensity level at code value zero. Maximum luminance intensity level is the maximum code value allowed for the bit

Terminology	Definition
	depth. Specifically, 63 for 18-bpp RGB, 255 for 24-bpp RGB, 1023 for 30-bpp RGB, 4095 for 36-bpp RGB, and 65,535 for 48-bpp RGB.
Via	A cross-over between layers of multi-layer PCB (print circuit board)
Video horizontal timing	Horizontal timing means video line timing. For example, horizontal period and horizontal synchronization pulse mean line period and line synchronization pulse, respectively. The term “horizontal” does not necessarily correspond to the physical orientation of the display device. For instance, a line may be oriented vertically on a “portrait” display.
Video vertical timing	Vertical timing means video frame (or field) timing. For example, vertical period and vertical synchronization pulse mean a frame (or field) period and a frame synchronization pulse, respectively The term “vertical” does not necessarily correspond to the physical orientation of the display device. For instance, a line may be oriented vertically on a “portrait” display.

1.5 References

Table 1-3: Reference Documents

Document	Version / Revision	Date
ANSI X3.230-1994, FibreChannel – Physical and Signaling Interface (FC-PH)		1994
ANSI/EIA-364-09C, Durability Test Procedure for Electrical Connectors and Contacts		June 1999
ANSI/EIA-364-13B, Mating and Unmating Forces Test Procedure for Electrical Connectors		December 1998
ANSI/EIA-364-17B, Temperature Life with or without Electrical Load Test Procedure for Electrical Connectors and Sockets		June 1999
ANSI/EIA-364-20C, Withstanding Voltage Test Procedure for Electrical Connectors, Sockets, and Coaxial Contacts		June 2004
ANSI/EIA-364-21C, Insulation Resistance Test Procedure for Electrical Connectors, Sockets, and Coaxial Contacts		May 2000
ANSI/EIA-364-23B, Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets		December 2000
ANSI/EIA-364-27B, Mechanical Shock (Specified Pulse) Test Procedure for Electrical Connectors		May 1996
ANSI/EIA-364-28D, Vibration Test Procedure for Electrical Connectors and Sockets		July 1999
ANSI/EIA-364-31B, Humidity Test Procedure for Electrical Connectors		May 2000
ANSI/EIA-364-32C, Thermal Shock (Temperature Cycling) Test Procedure for Electrical Connectors and Sockets		May 2000
ANSI/EIA-364-41C, Cable Flexing Test Procedure for Electrical Connectors		June 1999
ANSI/EIA-364-70, Temperature Rise Versus Current Test Procedure for Electrical Connector and Sockets		May 1998
ANSI/EIA-364-98, Housing Locking Mechanism Strength Test Procedure for Electrical Connectors		June 1997
CEA-861-C, A DTV Profile for Uncompressed High Speed digital Interface		August 2005
CEA-931-B, Remote Control Command Pass-Through Standard for Home Networking		September 2003
High-Bandwidth Digital Content Protection System, Amendment for DisplayPort	1.3 / 1.0	December 2006
IEC61000-4-2, EN/IEC6100-4-2 (former IEC 801-2), Electromagnetic Compatibility for Industrial process Measurements and Control Equipment-Part 4, Electrostatic Discharge requirements, International Electromechanical Commission		2001
ITU-R BT.601-5, Studio Encoding parameters of digital television for standard 4;3 and wide screen 14:9 aspect ratio		1995
ITU-R BT.709-5, Parameter Values for the HDTV standards for production and international Programme Exchange		2002
JEDEC JESE22-A114-A, JEDEC Standard No. JESD22-A114-B, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)		June 2000
VESA Glossary of Terms – see www.vesa.org	Current	Current
VESA Intellectual Property Rights (IPR) policy 200	B	February 2005

Document	Version / Revision	Date
VESA Display Data Channel Command Interface Standard (DDC/CI)	Version 1, revision 1	October 2004
VESA Enhanced Display Data Channel Standard (E-DDC	Version 1, revision 1	March 2004
VESA Enhanced Extended Display Identification Data (E-EDID) Standard	Release A, revision 2	September 2006
VESA Monitor Control Command Set (MCCS) Standard	Version 3	July 2006
VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT) Standard	Version 1, revision 10	October 2004

1.6 Nomenclature for Bit and Byte Ordering

This section describes the bit and byte ordering of the Main Link and the AUX CH.

1.6.1 Bit Ordering

1.6.1.1 Parallel Bit Ordering

- Main Link
  - Within a byte, bit 0 is the least significant bit (lsb) and bit 7 is the most significant bit (msb).

msb							lsb
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

  - For 8 bits per color, red bit 7 (R7) is placed at bit 7 and red bit 0 (R0) is placed at bit 0

msb							lsb
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R7	R6	R5	R4	R3	R2	R1	R0

  - For 6 bits per color, red bit 5 is placed at bit 7 (R5) and green bit 4 (G4) is placed at bit 0

msb							lsb
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R5	R4	R3	R2	R1	R0	G5	G4

- AUX CH
  - Within a byte, Bit 0 is the least significant bit while Bit 7 is the most significant bit

1.6.1.2 Serial Bit Ordering After Channel Encoding

- Main link (ANSI 8B/10B)
  - The least significant bit is transmitted first and the most significant bit last.
- AUX CH (ManchesterII)
  - The most significant bit is transmitted first and the least significant bit last.

1.6.2 Byte Ordering

- Main link, main stream
  - The most significant byte is transmitted first.
    For example, if the color bit depth of an RGB pixel is 16 bits per color, R15:8 (red bits 15 → 8) is transmitted first and is followed by R7:0 (red bits 7 → 0).

R15:8
R7:0

- When certain parameters of the main stream attribute packet have multiple bytes, the most significant byte is transmitted first.
  For example, Mvid23:16 is transmitted first, followed by Mvid15:8, and then, by Mvid7:0.

Mvid23:16
Mvid15:8
Mvid7:0

- Main link, secondary data packet
  - The least significant byte is transmitted first as shown in the audio sample data example below.

Audio sample0 channe0 byte 0
Audio sample0 channe0 byte 1
Audio sample0 channe0 byte 2
Audio sample0 channe0 byte 3

- AUX CH
  - In burst write / read operations over the AUX CH, the address is increased by one after each data byte. For the DPCD fields that have multiple bytes, the least significant byte is stored at the lowest address. During burst operation of an AUX CH transaction, therefore, the least significant byte is transported first.

Test_H_Total bits7:0 (address 00222h)
Test_H_Total bits 15:8 (address 00223h)

Source IEEE OUI bits 7:0 (address 00300h)
Source IEEE OUI bits 15:8 (address 00301h)
Source IEEE OUI bits 23:16 (address 00302h)

Note: As specified in section 1.6.1, the most significant bit is transported first and the least significant last over the AUX CH.

1.7 Overview of DisplayPort

DisplayPort link consists of a main link, an auxiliary channel (AUX CH), and a hot-plug detect (HPD) signal line.

As shown Figure 1-1 below, the Main Link is a uni-directional, high-bandwidth and low-latency channel used to transport isochronous data streams such as uncompressed video and audio. The auxiliary channel is a half-duplex bidirectional channel used for link management and device control. The HPD signal also serves as an interrupt request by the Sink Device.

In addition, the DisplayPort connector for a box-to-box connection has a power pin for powering either a DisplayPort repeater or a DisplayPort-to-Legacy converter.

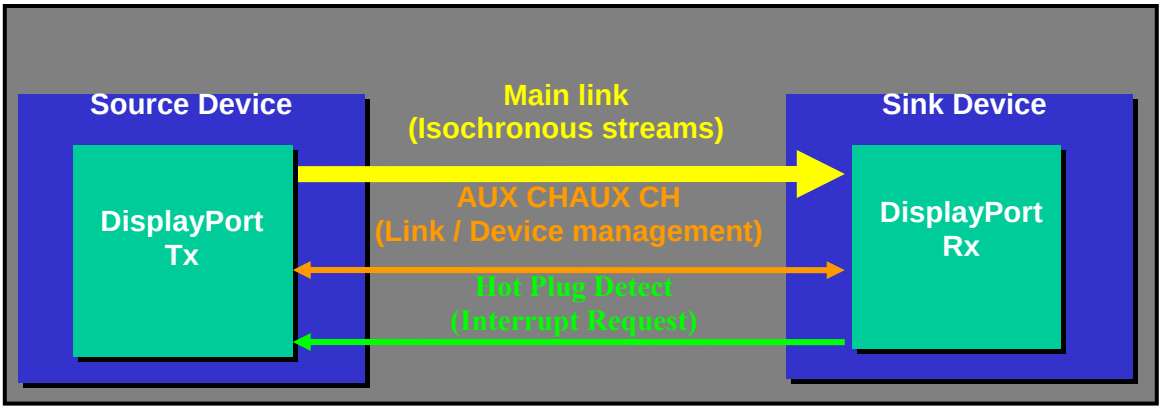


Figure 1-1: DisplayPort Data Transport Channels

1.7.1 Make-up of the Main Link

The Main Link consists of one, two or four ac-coupled, doubly terminated differential pairs (called lanes). AC-coupling facilitates the silicon process migration since the DisplayPort transmitter and receiver may have different common mode voltages.

Two link rates are supported, 2.7 Gbps and 1.62 Gbps per lane. The link rate is decoupled from the pixel rate. The pixel rate is regenerated from the link symbol clock using the time stamp values M and N. The capabilities of the DisplayPort transmitter and receiver, and the quality of the channel (or a cable) will determine whether the link rate is set to 2.7 Gbps or 1.62 Gbps per lane.

The number of lanes of Main Link is 1, 2, or 4 lanes. The number of lanes is decoupled from the pixel bit depth (bits per pixel, or bpp) and component bit depth (bits per component, or bpc). Component bit depths of 6, 8, 10, 12, and 16 are supported with the colorimetry formats of RGB, YCbCr 4:4:4 / 4:2:2 in DisplayPort regardless of the number of Main Link lanes.

All the lanes carry data. There is no dedicated clock channel. The clock is extracted from the data stream itself that is encoded with ANSI 8B/10B coding rule (the channel coding specified in ANSI X3.230-1994, clause 11).

Source and Sink Devices are allowed to support the minimum number of lanes required for their needs. The devices that support two lanes are required to support both one and two lanes, while those that support four lanes are required to support one, two and four lanes. An external cable that is detachable by an end user is required to support four lanes to maximize the interoperability between source and Sink Devices.

Excluding the 20% channel coding overhead, the DisplayPort Main Link provides for the application bandwidth (also called the link symbol rate) of:

- Link rate = 2.7 Gbps

- 1 lane = 270 Mbytes per second
- 2 lanes = 540 Mbytes per second
- 4 lanes = 1080 Mbytes per second

- Link rate = 1.62 Gbps
  - 1 lane = 162 Mbytes per second
  - 2 lanes = 324 Mbytes per second
  - 4 lanes = 648 Mbytes per second

DisplayPort devices may freely trade pixel bit depth with pixel format and the frame rate of a stream within the available bandwidth. Examples are shown below:

- Over four lanes
  - 12-bpc YCbCr 4:4:4 (36 bpp), 1920 x 1080p @ 96Hz
  - 12-bpc YCbCr 4:2:2 (24 bpp), 1920 x 1080p @ 120Hz
  - 10-bpc RGB (30 bpp), 2560 x 1536 @ 60Hz
- Over one lane
  - 8-bpc YCbCr 4:4:4 (30 bpp), 1920 x 1080i @60Hz
  - 6-bpc RGB (18 bpp), 1680 x 1050 @ 60Hz

The data mapping of a stream to the Main Link is devised to facilitate the support of various lane counts. For example, the pixel data is packed and mapped over a four lane Main Link as follows, regardless of the pixel bit depth and colorimetry format:

- Pixel data mapping over a four lane Main Link
  - Pixels 0, 4 : Lane 0,
  - Pixels 1, 5 : Lane 1
  - Pixels 2, 6 : Lane 2
  - Pixels 3, 7 : Lane 3

The stream data is packed into “micro-packets” which are called “transfer units”. The transfer unit length is in the range of 32 to 64 link symbols per lane. After the stream data is packed and mapped to main link, the packed stream data rate will be equal to or smaller than the link symbol rate of the main link. When it is smaller, stuffing symbols are inserted.

During the horizontal and vertical blanking period of the main video stream, almost all the link symbols are stuffing symbols, which may be substituted with a stream attribute packet (containing the image height, width, etc. of the main video stream) used for regenerating the stream in the Sink Device, and optional secondary-data packets such as audio stream packets.

1.7.2 Make-up of AUX CH

AUX CH consists of an ac-coupled, doubly terminated differential pair. Manchester II coding is used as the channel coding for the AUX CH. As is the case with main link, the clock is extracted from the data stream.

AUX CH is half-duplex, bi-directional. The Source Device is the master and the Sink Device the slave. A Sink Device may toggle the HPD signal to interrupt the Source Device which would prompt an AUX CH request transaction.

AUX CH provides a data rate of 1Mbps over the supported cable lengths of up to 15m and longer. Each transaction takes no more than 500 us with a maximum burst data size of 16 bytes, this avoids AUX CH contention problems by one application starving other applications.

1.7.3 Link Configuration and Management

Upon hot plug detection, the Source Device configures the link through link training. The correct number of lanes is enabled at the correct link rate with the correct drive current and equalization level, through the handshake between DisplayPort transmitter and receiver via AUX CH.

During normal operation following link training, the Sink Device may notify a link status change, for example, loss of synchronization, by toggling the HPD signal, this causes interrupt request. The Source Device then checks the link status via the AUX CH and takes corrective action. This closed-loop link operation enhances the robustness and interoperability between source and Sink Devices.

Since the link rate is decoupled from the stream rate, the DisplayPort link may stay active and stable even when the timing of a transported stream changes.

1.7.4 Layered, Modular Architecture

Figure 1-2: shows the layered architecture of DisplayPort.

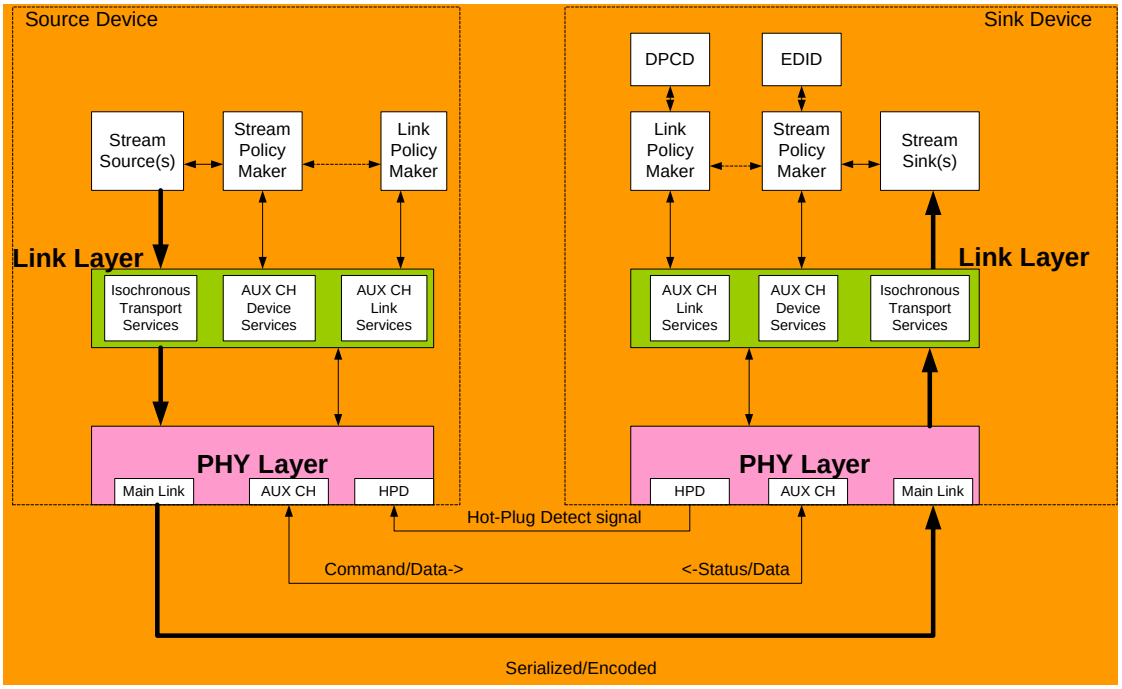


Figure 1-2: Layered Architecture

In Figure 1-2: above, DPCD (DisplayPort Configuration Data) in the Sink Device describes the capability of the receiver, just as EDID describes that of the Sink Device. Link and stream policy makers manage the link and the stream, respectively. Details (state machine, firmware, or system software) are implementation specific.

Note: At some future time the physical layer may be replaced while the link layer remains unchanged. This allows the DisplayPort specification to evolve along with the technology to maintain its cost and performance position.

Also, the micro-packet based data transport enables a seamless extension of the DisplayPort specification toward supporting multiple audio-visual streams and other data types. Switches and hubs may be used to route streams among multiple sources and Sink Devices.

When content protection is required, it is recommended that either DPCP (DisplayPort Content Protection) Version 1.0 or HDCP Version 1.3 is used.

2 Link Layer

2.1 Introduction

This chapter describes the services provided by the link layer of DisplayPort. These services are:

- Isochronous transport services over the main link

  The isochronous transport services maps the video and audio streams onto the Main Link with a set of rules, explained in Section 2.2.1), so that the streams can be correctly re-constructed into the original format and time base in the Sink Device.

- Link and device management services over the AUX CH

  Link services are used for discovering, configuring, and maintaining the link (as explained in Section 2.5.3). The AUX CH read / write access to DPCD (DisplayPort Configuration Data) address is used for these purposes. Device services support device-level applications such as EDID read and MCCS control (Section 2.5.4). In addition, the AUX CH may be used for optional content protection.

In conjunction with the description of these services, AUX CH states / arbitration and transaction syntax are also covered in this chapter.

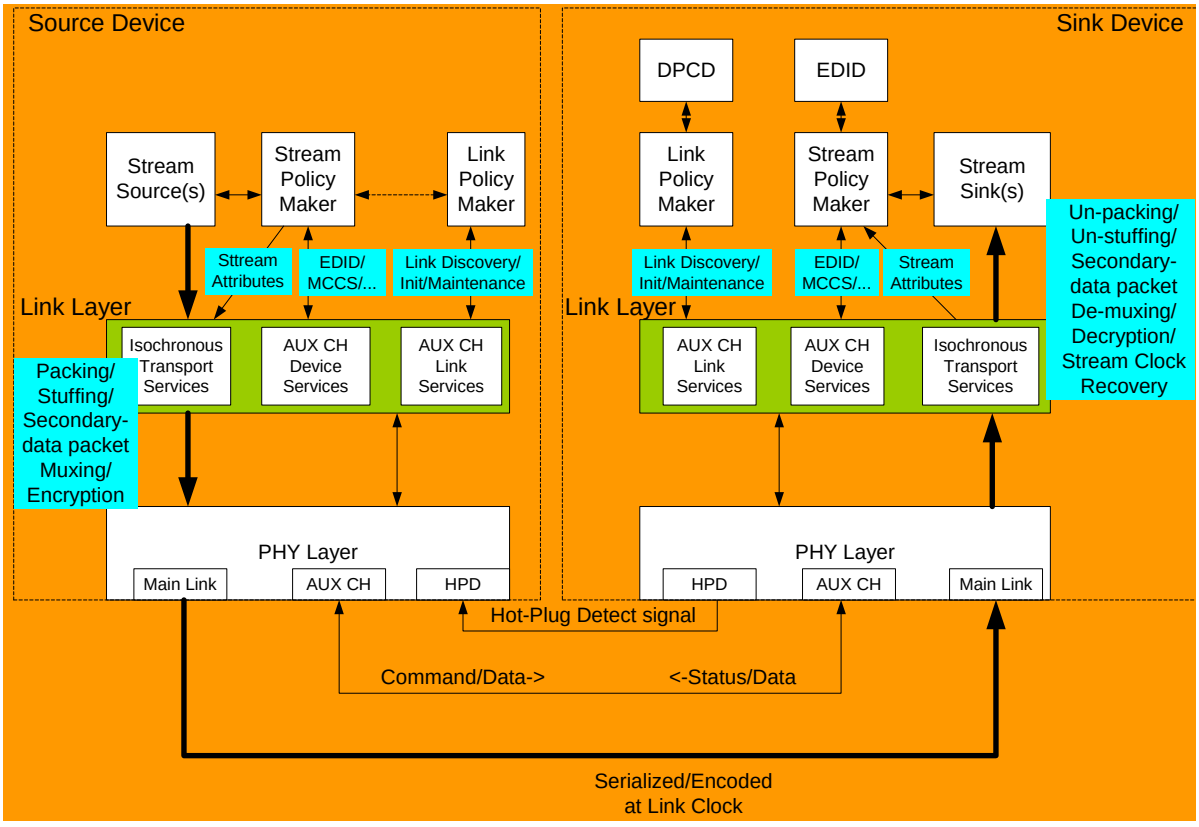


Figure 2-1: Overview of Link Layer Services

The link layer provides services as instructed or requested by the stream link policy makers (Figure 2-1). The stream policy maker manages the transport of the stream. The link policy maker manages the link and is responsible for keeping the link synchronized.

In this section (and in the entire DisplayPort specification as well), only the interactions between the policy makers and the link layer are described. The syntax for these interactions (that is, the API) is implementation specific, and beyond the scope of this document.

2.1.1 Number of Lanes and Per-lane Data Rate

DisplayPort supports three options for the number of Main Link lanes and two options for Main Link data rate per lane as follows:

- 4, 2, or 1 lanes
- 2.7 Gbps or 1.62 Gbps per lane

The link layer specification, and the data mapping specification in particular, is defined to facilitate the support of these lane count options.

The per lane data rate is determined not only by the capabilities of DisplayPort transmitter and receiver but also by the quality of a channel, or a cable.

The DisplayPort Sink Device must indicate the capability of its receiver in the receiver capability field of the DPCD, as described in Section 2.5.3.1.

After reading the receiver capability, the DisplayPort Source Device must configure the link by writing to the link configuration field of the DPCD in the DisplayPort Sink Device and then running link training.

Through this process of receiver capability discovery and link training, the DisplayPort source and Sink Devices are able to negotiate for the optimal lane count and per lane data rate for a given connection.

2.1.2 Number of Main, Uncompressed Video Streams

The scope of DisplayPort specification is limited to the transport of a single, uncompressed video stream as the main stream, with the optional insertion of secondary data packets such as an audio stream packet.

Transport of multiple main streams is not covered in the current specification. However, the DisplayPort specification allows for seamlessly extension to support the transport of multiple uncompressed video streams and other data types.

2.1.3 Basic Functions

The basic functions of DisplayPort devices are described below.

- Source function – the source functionality (that is, transmission of stream) of DisplayPort
- Sink function – the sink functionality (that is, reception of stream) of DisplayPort
- Rendering function – displays / portrays / processes the received stream: Examples are video display, speaker, and format converter.

2.1.4 DisplayPort Device Types and Link Topology

A device will contain at least one DisplayPort function as well as other functions such as a display, speakers, recording device or even an entire computer.

The DisplayPort specification covers the following device types:

- Source Device - a device that contains one or more source functions and is a root in a DisplayPort tree topology.
- Sink Device – a device that contains a single sink function, at least one rendering function and is a leaf in a DisplayPort tree topology.

- Repeater Device (one input, one output) – a device that contains one sink function and one source function. Repeaters may include "box to box" Hybrid Devices.
- Legacy-to-DisplayPort Converter (one input, one output) – a device that contains one legacy sink function and one DisplayPort source function.
- DisplayPort-to-Legacy Converter (one input, one output) – a device that contains one DisplayPort sink function and one legacy source function.
- Replicater Device (one sink function and k source functions, where k is a positive integer > 1) - this device may include a legacy converter sink and / or one or more legacy converter sources. Concentrator Device (k sink functions and one source function, where k is a positive integer >1)
- Composite Device – a replicater with a rendering function. For example, a display that has one or more downstream ports. A format converter that alters the stream is regarded as a composite device. If one of the outputs on a replicater is a legacy converter then that output will be deemed a rendering function. Composite Devices may include "box to box" Hybrid Devices.

DisplayPort devices with a source function and / or a sink function must have a link policy maker. A Source Device that originates or processes (for example, format conversion) the stream data and Sink Devices must also have a stream policy maker.

DisplayPort devices with a sink function must have a DPCD. Sink Devices and composite devices must also have an EDID.

Using the above device types, DisplayPort networks consisting either of a single hop or multiple hops (daisy chain or tree) may be configured.

From the perspective of the device location within a link, the devices are categorized as follows:

- Root Device = Source Device
- Leaf Device = Sink Device
- Branch Device = Devices other than a Source Device or a Sink Device described above.

A DisplayPort Source Device is link topology agnostic – for example, a Source Device must not inquire how many downstream ports its immediate downstream device has or how many downstream hops are present in its downstream link. The Source Device needs only to read the Sink Device capability (EDID) and the link capability (DPCD) from its immediate downstream device and to source a stream accordingly.

Figure 2-2 → Figure 2-7 show examples of DisplayPort link topologies.

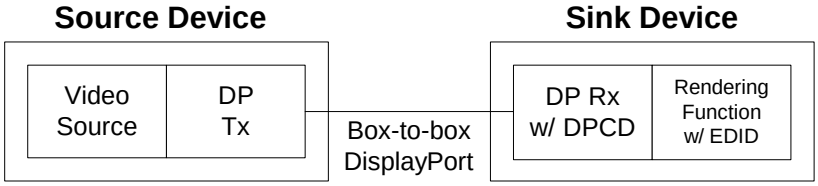


Figure 2-2: Single Hop, Detachable DisplayPort Link

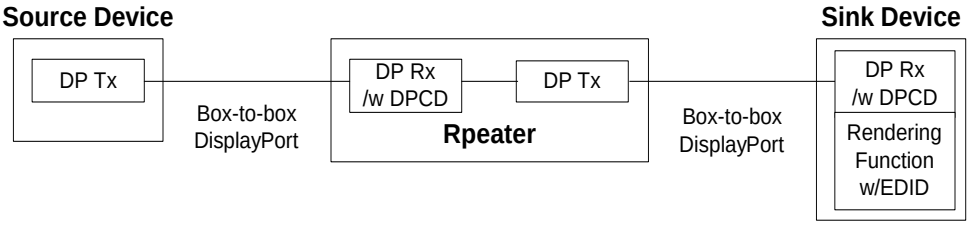


Figure 2-3: DisplayPort Source Device to DisplayPort Sink Device via a Repeater

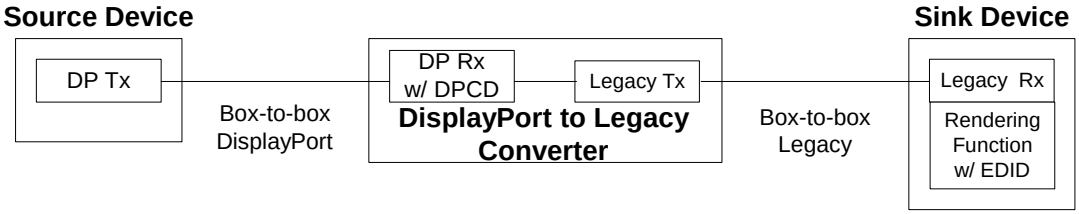


Figure 2-4: DisplayPort Source Device to Legacy Sink via DisplayPort to Legacy Converter

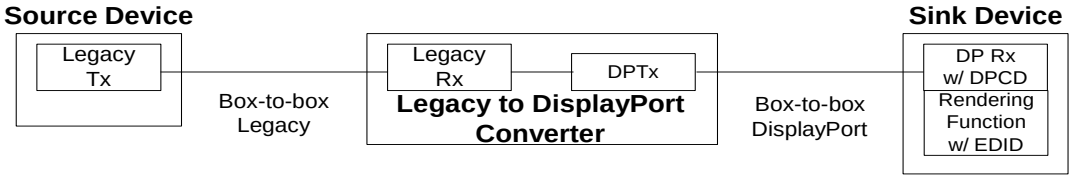


Figure 2-5: Legacy Source Device to DisplayPort Sink Device via a Legacy to DisplayPort Converter

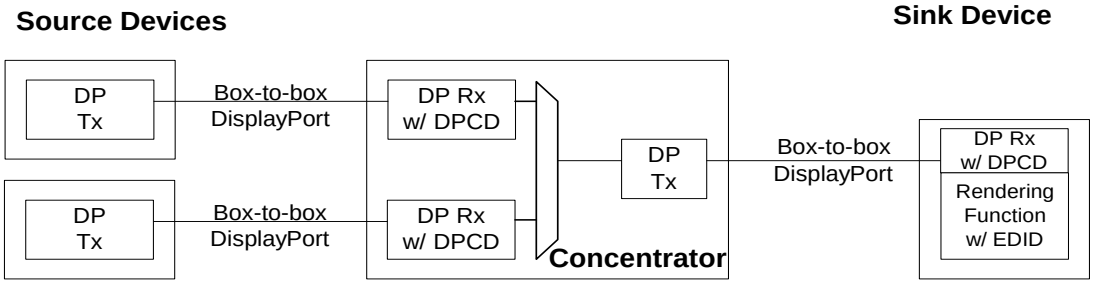


Figure 2-6: Multiple Source Devices to a Sink Device via a Concentrator

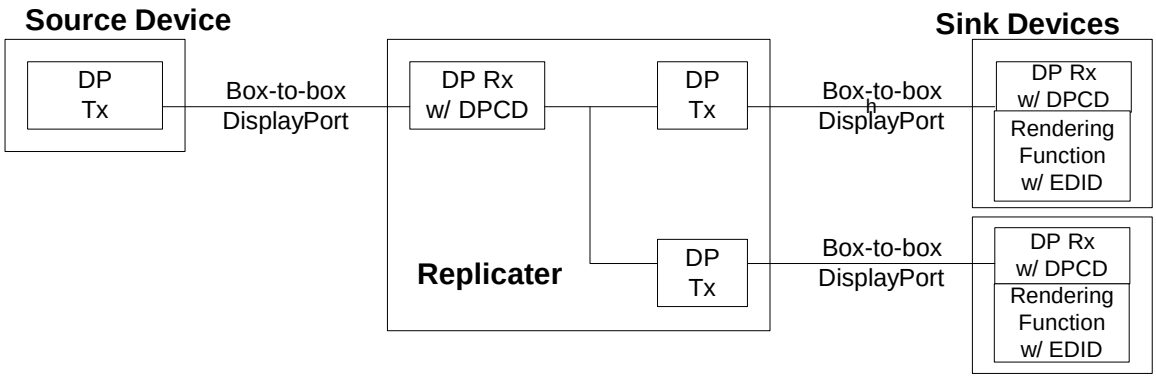


Figure 2-7: A Source Device to Multiple Sink Devices via a Replicator

2.1.4.1 EDID and DPCD of Branch Devices

After an EDID read by the Source Device, a Branch Device must reply with the EDID of the downstream Sink Device.

A Branch Device must update its receiver capability field to comprehend not only its own DPCD but also the downstream DPCD.

For example, even if a repeater device is capable of supporting up to four lanes of main link, it must report support for two lanes to the Source Device if its downstream link is only capable of up to two lanes.

2.1.4.1.1 EDID and DPCD Access Handling by Replicater Device (INFORMATIVE)

How replicater device handle EDID and DPCD access by an upstream device is implementation specific.

Examples:

When only one Sink Device is connected to its downstream ports, the replicater device may reply with the EDID of that Sink Device.

When multiple Sink Devices are connected, the replicater device may reply with the EDID of one of the Sink Devices.

When such an approach is taken, the replicater device "NACK's" the EDID read over the AUX CH only when no device is connected to it.

The same approach may be taken for the DPCD of the downstream links. It is the responsibility of a replicater device manufacturer to describe the EDID and DPCD handling policy to a user (for example, in a user's manual and / or with labeling).

Note: The replicater device is recommended to choose the same downstream port for EDID and DPCD access.

2.1.4.1.2 EDID and DPCD Access Handling by Composite Device (INFORMATIVE)

Handling of EDID and DPCD access by a composite device is implementation specific. For example, it may reply with the EDID of its own sink and may choose not to comprehend the DPCD of its downstream link.

Note: The DisplayPort specification does not currently define a mechanism through which the upstream device can read multiple EDID's of Sink Devices connected to Branch Device(s).

2.1.4.2 Docking Station (INFORMATIVE)

A docking station is either a replicater device or a composite device (with format converting function) embedded in a Source Device. Since it is embedded, the management policy is implementation specific and beyond the scope of this specification.

DisplayPort AUX CH address space of 00300h - 003FFh is reserved for vendor specific usage for Source Devices. This address space may be used to configure a docking station.

2.2 Isochronous Transport Services

The isochronous transport services of the link layer provide the following:

- Mapping of stream data to and from Main Link lanes
  - Packing and unpacking
  - Stuffing and unstuffing
  - Framing and unframing
  - Inter-lane skewing and deskewing
- Stream clock recovery
- Insertion of main stream attributes data
- Optional insertion secondary data packet with ECC
  - Audio stream packet
  - CEA861-C InfoFrame packet

2.2.1 Main Stream to Main Link Lane Mapping in the Source Device

The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed with secondary data and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping for transport over the main link. The stream data must enter the link layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY layer at the LS_Clk rate after this mapping.

Figure 2-8 and Figure 2-9 show the data mapping in source and Sink Devices, respectively.

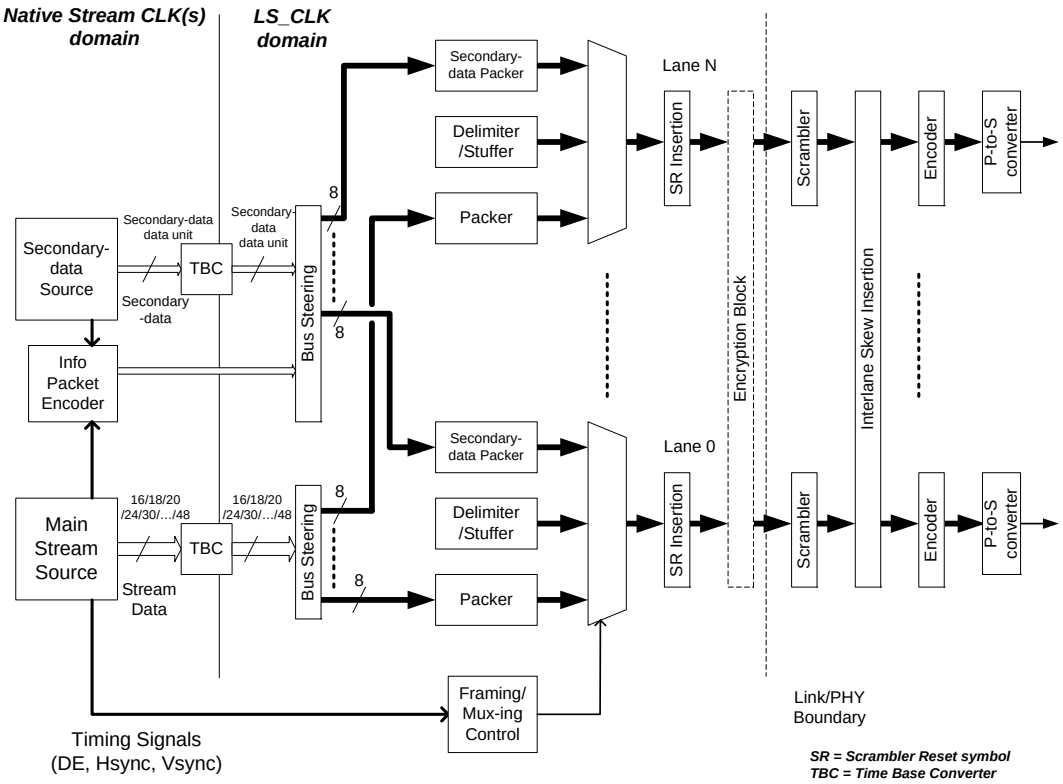


Figure 2-8: High Level Block Diagram of Transmitter Main Link Data Path

Notes:

a) Logical block diagram. Actual implementation may vary.

b) The ECC and CP encryption blocks are both optional. To support secondary data packets, ECC is required.

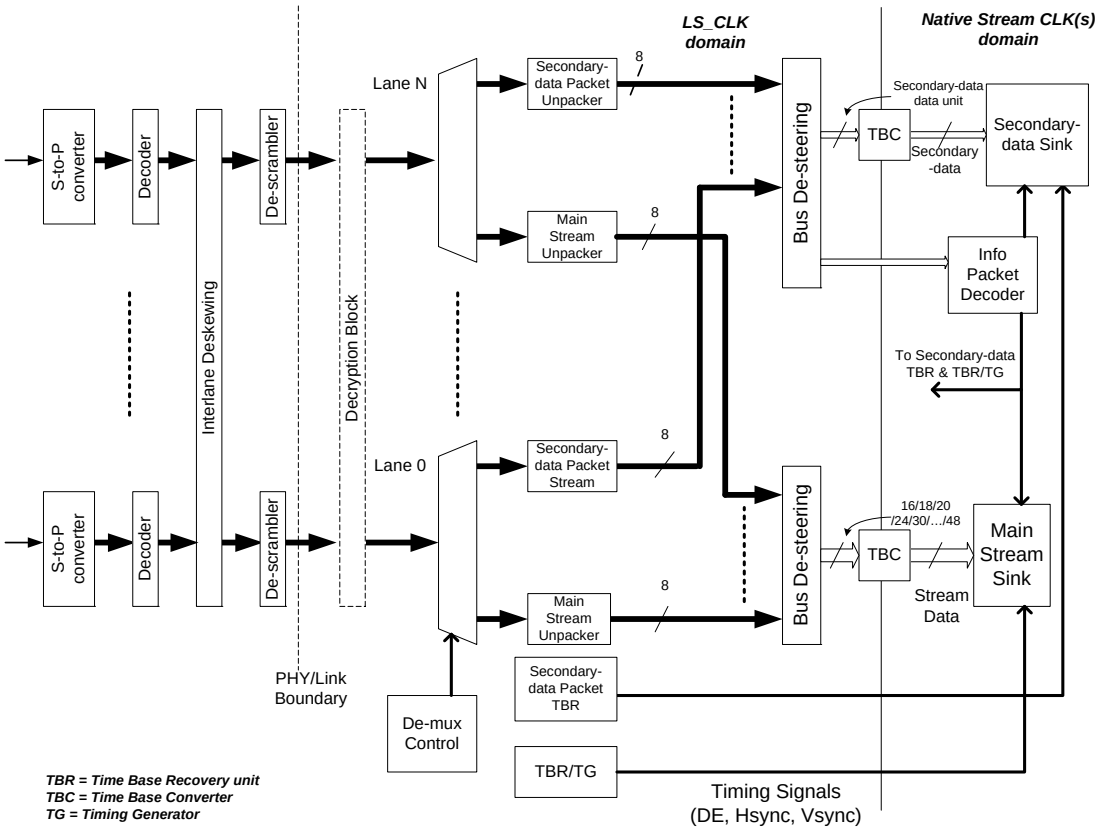


Figure 2-9: High Level Block Diagram of Receiver Main Link Data Path

Notes:

a) Logical block diagram. Actual implementation may vary.

b) The ECC and CP encryption blocks are both optional. To support secondary data packets, ECC is required except for the extension secondary packet (section 2.2.5.4).

Main link data mapping shall take place in the following order:

- Main stream data packing, stuffing, and framing
- Optional secondary data framing and multiplexing

2.2.1.1 Control Symbols for Framing: Default Framing Mode

For framing data, the following seven control symbols must be used:

- BS (Blanking Start)
  - Inserted after the last active pixel during the vertical display period.
  - Inserted at the same symbol time during vertical blanking period as during vertical display.
  - This framing symbol must be periodically (every 2^{13} or 8,192 symbols) inserted for active links with no main video stream data to send. In this condition, the BS symbol is immediately followed by VB-ID with its NoVideoStream_Flag set to 1. (For more information on VB-ID, refer to Section 2.2.1 on p.35. This link symbol pattern is referred to as the "Idle Pattern".
- BE (Blanking End)
  - Inserted immediately before the first active pixel of a line only during the vertical display period

- FS (Fill Start)
  - Inserted at the beginning of stuffing symbols in the transfer unit.
    Note: Transfer unit is described in Section 2.2.1.4.1
  - Omitted when there is only one stuffing symbol. In this case, FE (Fill End) is inserted without FS.
  - FS and FE are inserted with no stuffing data symbols in between when there are only two stuffing symbols.
- FE (Fill End)
  - Inserted at the end of stuffing symbols within transfer unit.
- SS (Secondary-data Start)
  - Inserted at the beginning of secondary data
- SE (Secondary-data End)
  - Inserted at the end of the secondary data
- SR (Scrambler Reset)
  - Every 512th BS symbol must be replaced with a SR symbol by Source Device to reset the LFSR of the scrambler.
- CPBS (Content Protection BS)
  - Used by a CP system. Called "CP" symbol in the Enhanced Framing Mode described in section 2.2.1.2.
- CPSR (Content Protection SR)
  - Used by a CP system. CPSR resets the LFSR of the scrambler just as SR does. Called "BF" symbol in the Enhanced Framing Mode described in section 2.2.1.2.

These control symbols must be inserted in all lanes in the same LS_Clk cycle (before they get inter-lane skewed by 2 LS_Clk cycles just before going to the PHY Layer). The link layer must distinguish these control symbols from data symbols so that the physical layer can properly encode these control symbols using "special characters".

For example, the link layer may use the 9th bit to indicate whether the accompanying 8-bit data represents control symbols or data symbols. There are many ways for link layer to implement this distinction, the method used is implementation specific and beyond the scope of this document.

2.2.1.2 Control Symbols for Framing: Enhanced Framing Mode

BS, SR, CPBS, and CPSR symbols must be replaced as shown in Table 2-1 in enhanced mode. The enhanced framing mode is enabled only when both DisplayPort source and Sink Devices support it.

A DisplayPort Sink Device indicates its support with ENHANCED_FRAME_CAP bit in the receiver capability field of DPCD (bit 7 of address 2h). A DisplayPort Source Device enables it by writing 1 to ENHANCED_FRAME_EN bit in the link configuration field of DPCD (bit 7 of address 101h) as described in Table 2-52. Once enabled, BS, SR, CPBS, and CPSR symbols must be replaced with the four symbol sequence in Table 2-1 regardless of the lane count of the main link.

Table 2-1: Control Symbols for Framing

Default Framing Mode Symbols	Enhanced Framing Mode Symbols
BS	BS + BF + BF + BS
SR	SR + BF + BF + SR
CPBS (called CP symbol in Enhanced Framing Mode)	BS + CP + CP + BS
CPSR (called BF symbol in Enhanced Framing Mode)	SR + CP + CP + SR
BE	BE (no change)
FS	FS (no change)
FE	FE (no change)
SS	SS (no change)
SE	SE (no change)

The mapping of these control symbols to ANSI 8B/10B special characters is described in Section 3.5.1.2

When a DisplayPort transmitter operating in Enhanced Framing Mode is transmitting the Idle Pattern, the transmitter must insert the fur symbol sequence of BS (or SR) every 2^{13} or 8,192 symbols. In other words, there must be 8,188 symbols between the last (the fourth) symbol of the four symbol sequence for BS (or SR) and the first symbol of the next four symbol sequence.

In both Default and Enhanced Framing Modes, every 512th BS (or CPBS) symbol must be replaced with SR (or CPSR). The last symbol of the four symbol sequence for SR (or CPSR when content protection is enabled) must be used to reset the scrambler.

When switching between the Idle Pattern transmission and a stream transmission, the Source Device must avoid any overlap of the four symbols for BS, SR, CPBS and CPSR.

A DisplayPort transmitter with HDCP capability must support the Enhanced Framing Mode.

2.2.1.3 Main Video Stream Data Packing

The link layer must first steer pixel data in a pixel-within-lane manner as shown in Table 2-2.

Table 2-2: Pixel Steering into Main Link Lanes

Number of Lanes	Pixel Steering (N is 0 or positive integer)
4	Pixel 4N to lane 0 Pixel 4N+1 to lane 1 Pixel 4N+2 to lane 2 Pixel 4N+3 to lane 3
2	Pixel 2N to lane 0 Pixel 2N+1 to lane 1
1	All pixels to lane 0

These rules apply regardless of the color space / pixel bit depth of the video stream. As shown in Figure 2-10, the first set of active partial pixel data of a line must follow the control symbol, BE.

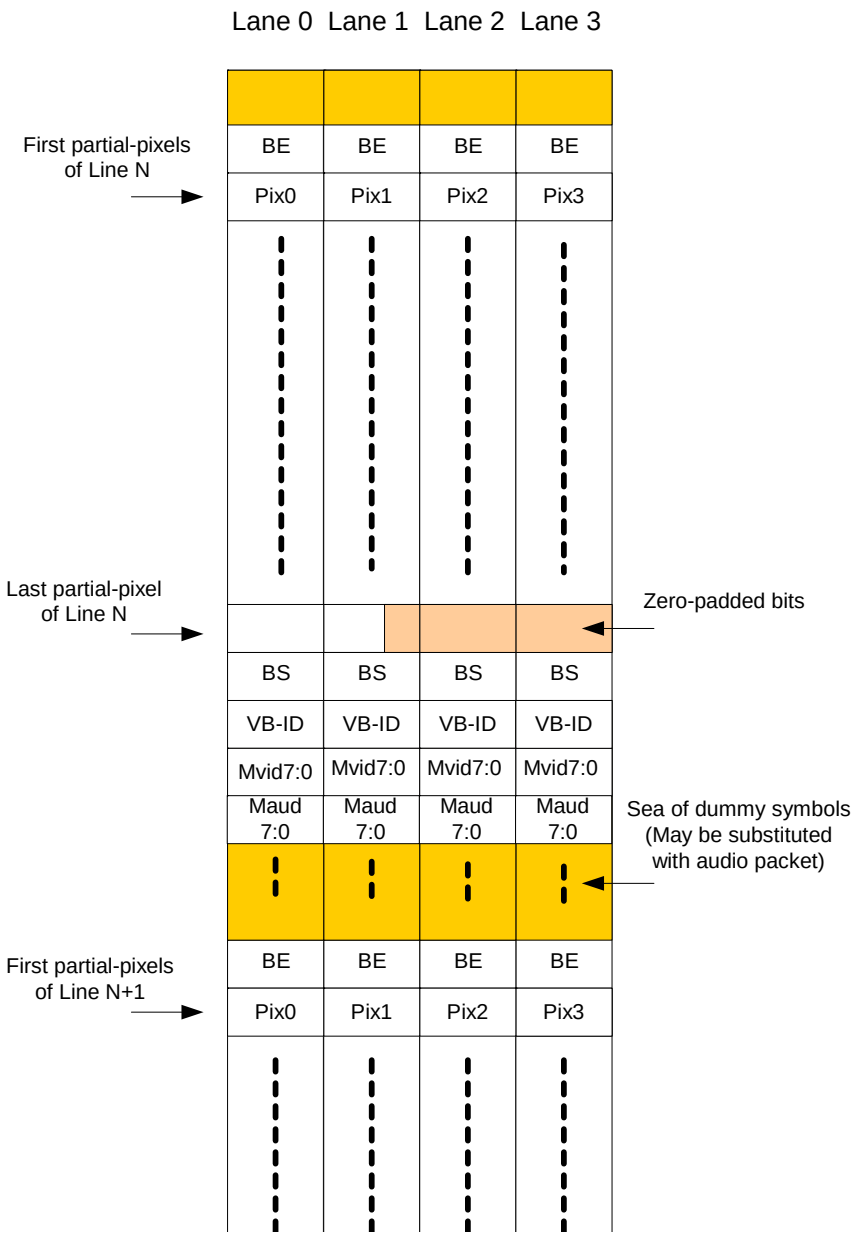


Figure 2-10: Main Video Stream Data Packing Example for a Four Lane Main Link

When there is no audio stream transported, Maud 7:0 must be set to 00h. When there is no video stream transported, Mvid 7:0 must be set to 00h.

During the last symbol time for a line of pixel data, there may be insufficient pixel data to provide data on all lanes of the link. The DisplayPort transmitter must send zeros for those bits (zero-padded bits).

Immediately following the last symbol period of a line of data the control symbol, BS must be inserted on all lanes of the link.

The Sink Device, knowing the number of active pixels per horizontal line (from the main stream attribute), must discard zero-padded bits as “don’t care.”

Figure 2-10 shows that a new line must always start with pixel 0 on lane 0 following BE.

The BS must be followed on all lanes by VB-ID, Mvid 7:0, and Maud 7:0.

- VB-ID must carry the following information:

- Whether the main video stream is in the vertical display period or the vertical blanking period.
- Whether the main video stream is in the odd field or the even field for interlaced video
- Whether the main video stream is interlaced or non-interlaced (progressive)
- Whether the BS is inserted while no video stream is being transported. The symbols transmitted over the Main Link when no video stream is active are shown in 0.
- Whether to mute the audio

Table 2-3: VB-ID Bit Definition

VB-ID Bit	Bit Name	Bit Definition
Bit 0	VerticalBlanking_Flag	This bit must be set to 1 at the end of the last active line and stay 1 during the vertical blanking period. This bit is also set to 1 when there is no video stream (as indicated by bit 3 set to 1).
Bit 1	FieldID_Flag	This bit must be set to: 0 right after the last active line in the top field. 1 right after the last active line of the bottom field Refer to Figure 2-19 and Figure 2-20 for definitions of the top and bottom fields. For progressive (non-interlaced) video there is no bottom video and this bit remains 0.
Bit 2	Interlace_Flag	This bit must be set to 1 when the main stream is an interlaced video. For non-interlaced video or no video, this bit must stay 0.
Bit 3	NoVideoStream_Flag	This bit must be set to 1 when preceding BS is inserted while no video stream is transported. When this bit = 1, the Mvid 7:0 value must be "don't care." **Note:** An audio stream may be transported even when no main video stream is being transported.
Bit 4	AudioMute_Flag	This bit must be set to 1 when the audio is to be muted.
Bit 5	HDCP SYNC DETECT	Used by HDCP capable DisplayPort receivers to detect the CP lock status. Refer to HDCP Specification 1.3 – Amendment for DisplayPort
Bits 7:6	RESERVED	Reserved (All 0's)

- Mvid 7:0
  - The least significant 8 bits of the time stamp value M for the video stream. When there is no video stream transported, set to 00h.
    The time stamp must be used for stream clock recovery, the subject of which is covered in Section 2.2.3.
- Maud 7:0
  - The least significant 8 bits of the time stamp value M for the audio stream. When there is no audio stream transported, set to 00h.

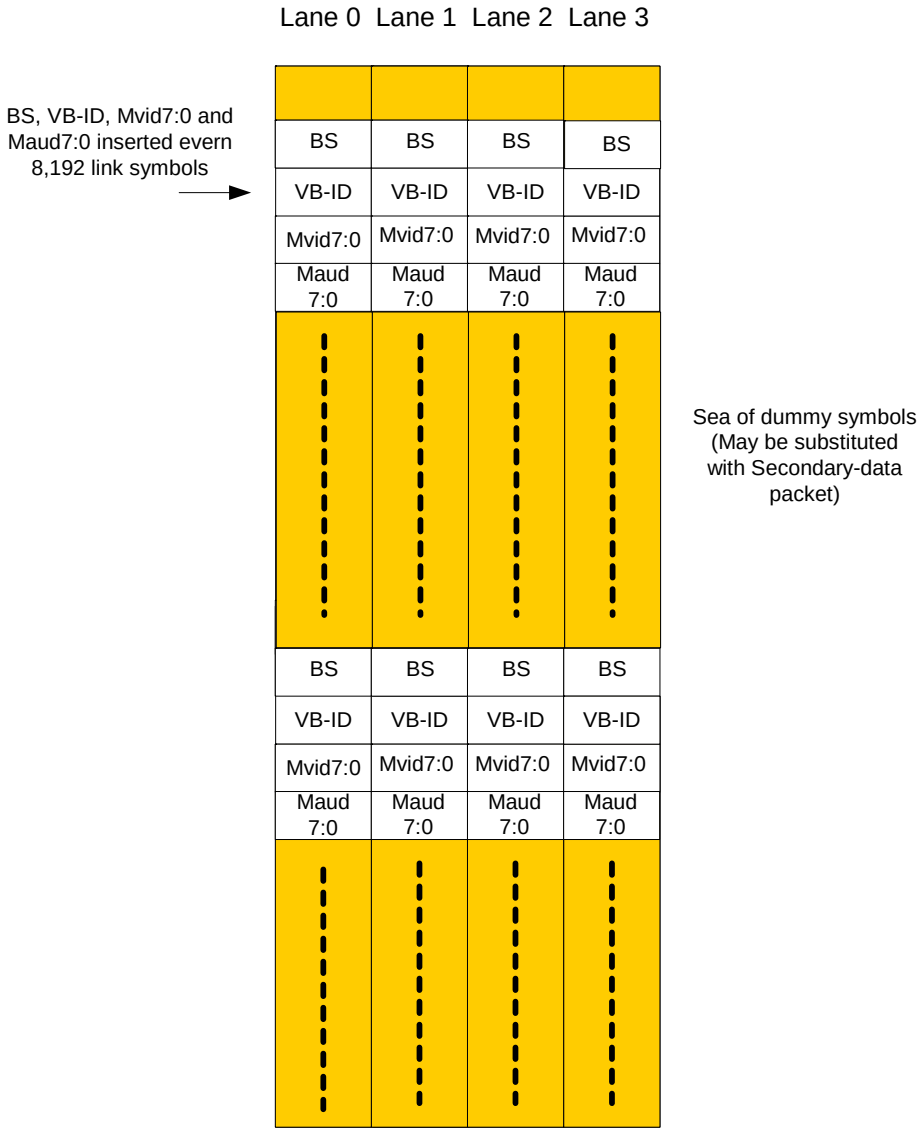


Figure 2-11: Link Symbols Over the Main Link Without Main Video Stream

Mvid 7:0 must be set to 00h. When there is no audio stream transported, Maud 7:0 must be set to 00h.

The VB-ID, Mvid 7:0 and Maud 7:0 must be transported four times, regardless of the number of lanes in the Main Link as shown in Figure 2-12.

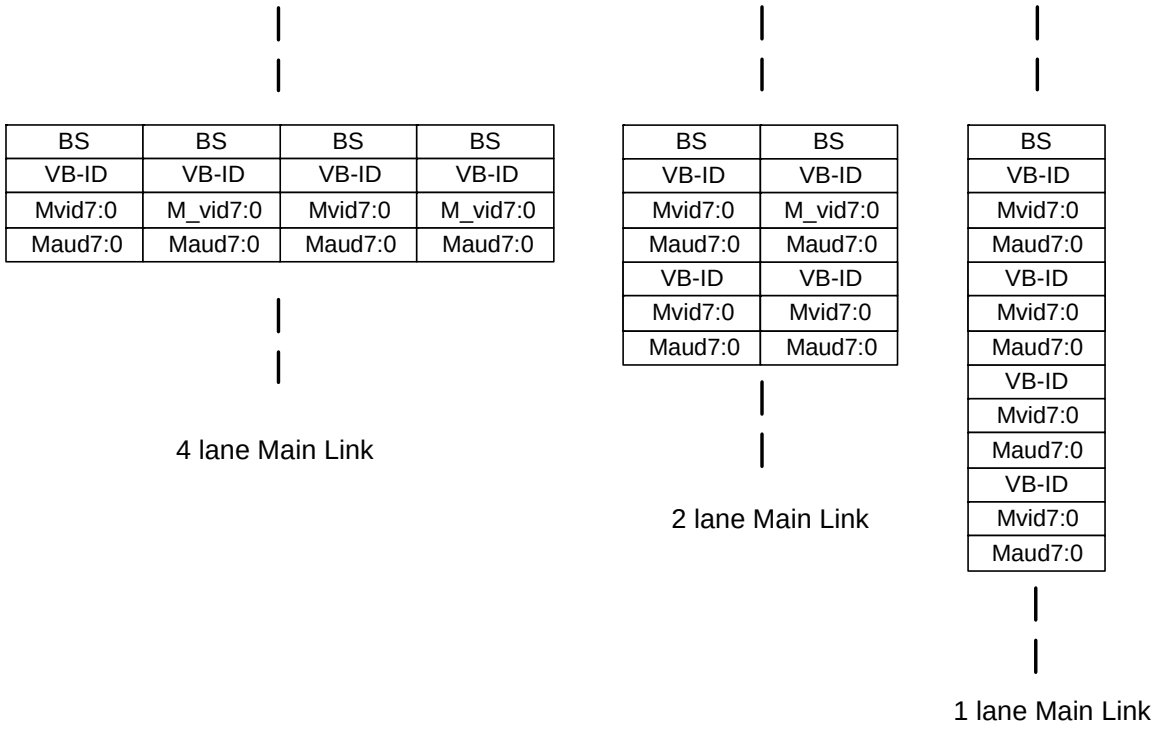


Figure 2-12: VB-ID, Mvid 7:0 and Maud 7:0 Packing Over the Main Link

If there is no audio stream, Maud 7:0 must be set to 00h. If there is no video stream, Mvid 7:0 must be set to 00h.

Table 2-4 is an example of how a video stream with pixel format of 1366 x 768 and 30 bits-per-pixel (bpp) RGB color depth is mapped to a four lane Main Link.

Table 2-4: 30 bpp RGB (10 Bits / Component) 1366 x 768 Packing to a Four Lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3	
BE	BE	BE	BE	
R0-9:2	R1-9:2	R2-9:2	R3-9:2	<-- Start of Active Pixel
R0-1:0|G0-9:4	R1-1:0|G1-9:4	R2-1:0|G2-9:4	R3-1:0|G3-9:4	
G0-3:0|B0-9:6	G1-3:0|B1-9:6	G2-3:0|B2-9:6	G3-3:0|B3-9:6	
B0-5:0|R4-9:8	B1-5:0|R5-9:8	B2-5:0|R6-9:8	B3-5:0|R7-9:8	
R4-7:0	R5-7:0	R6-7:0	R7-7:0	
G4-9:2	G5-9:2	G6-9:2	G7-9:2	
G4-1:0|B4-9:4	G5-1:0|B5-9:4	G6-1:0|B6-9:4	G7-1:0|B7-9:4	
B4-3:0|R8-9:6	B5-3:0|R9-9:6	B6-3:0|R10-9:6	B7-3:0|R11-9:6	
R8-5:0|G8-9:8	R9-5:0|G9-9:8	R10-5:0|G10-9:8	R11-5:0|G11-9:8	
G8-7:0	G9-7:0	G10-7:0	G11-7:0	
B8-9:2	B9-9:2	B10-9:2	B11-9:2	
B8-1:0|R12-9:4	B9-1:0|R13-9:4	B10-1:0|R14-9:4	B11-1:0|R15-9:4	
R12-3:0|G12-9:6	R13-3:0|G13-9:6	R14-3:0|G14-9:6	R15-3:0|G15-9:6	
G12-5:0|B12-9:8	G13-5:0|B13-9:8	G14-5:0|B14-9:8	G15-5:0|B15-9:8	
B12-7:0	B13-7:0	B14-7:0	B15-7:0	

R1360-9:2	R1361-9:2	R1362-9:2	R1363-9:2	
R1360-1:0|G1360-9:4	R1361-1:0|G1361-9:4	R1362-1:0|G1362-9:4	R1363-1:0|G1363-9:4	
G1360-3:0|B1360-9:6	G1361-3:0|B1361-9:6	G1362-3:0|B1362-9:6	G1363-3:0|B1363-9:6	
B1360-5:0|R1364-9:8	B1361-5:0|R1365-9:8	B1362-5:0|---	B1363-5:0|---	
R1364-7:0	R1365-7:0	---	---	
G1364-9:2	G1365-9:2	---	---	
G1364-1:0|B1364-9:4	G1365-1:0|B1365-9:4	---	---	
B1364-3:0|---	B1365-3:0|---	---	---	<-- End of Active Pixel
BS	BS	BS	BS	
VB-ID	VB-ID	VB-ID	VB-ID	
Mvid7:0	Mvid7:0	Mvid7:0	Mvid7:0	
Maud7:0	Maud7:0	Maud7:0	Maud7:0	

Notes:

1) One row of data is transmitted per LS_Clk cycle. The transmitter must send 0's for "---" in the above table.

2) R0-9:2 = red bits 9:2 of pixel, G = green, B = blue, BS = blanking start, BE = blanking end. VB-ID = video blanking ID. Mvid 7:0 and Maud 7:0 are portions of the time stamps for video and audio stream clocks.

The following sections show how 24, 18, 30 bit RGB pixels and 16, 20, and 24 bit YCbCr 4: 2:2 pixels are mapped into four, two and one lane Main Links.

As can be seen in Table 2-5 → Table 2-31, when only one lane is enabled of either a two or four lane DisplayPort device, lane 0 must be enabled. When only two lanes are enabled, lanes 0 and 1 must be enabled.

2.2.1.3.1 24-bpp RGB / YCbCr 4:4:4 (8 bits per component)

24-bpp RGB / YCbCr 4:4:4 stream mapping into a four, two or one lane Main Link is shown in Table 2-5 - Table 2-7. Bit 7 of each color is mapped to bit 7 of each lane, while bit 0 of each color is mapped to bit 0 of each lane.

Table 2-5: 24 bpp RGB to a Four Lane Main Link Mapping

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

Table 2-6: 24 bpp RGB Mapping to a Two Lane Main Link

Lane 0	Lane 1
R0-7:0	R1-7:0
G0-7:0	G1-7:0
B0-7:0	B1-7:0
R2-7:0	R3-7:0
G2-7:0	G3-7:0
B2-7:0	B3-7:0
R4-7:0	R5-7:0
G4-7:0	G5-7:0
B4-7:0	B5-7:0

Table 2-7: 24 bpp RGB Mapping to a One Lane Main Link

Lane 0
R0-7:0
G0-7:0
B0-7:0
R1-7:0
G1-7:0
B1-7:0
R2-7:0
G2-7:0
B2-7:0
R3-7:0
G3-7:0
B3-7:0

Note: In Table 2-5 → Table 2-7, for YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

2.2.1.3.2 18 bpp RGB (6 Bits per Component)

Table 2-8 → Table 2-10 show an 18 bpp RGB stream mapping into onto four, two and one lane main links. Bit 5 of R0 is mapped to bit 7 of lane 0 while bit 4 of G0 is mapped to bit 0 of lane 0.

Table 2-8: 18 bpp RGB Mapping to a Four Lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-5:0|G0-5:4	R1-5:0|G1-5:4	R2-5:0|G2-5:4	R3-5:0|G3-5:4
G0-3:0|B0-5:2	G1-3:0|B1-5:2	G2-3:0|B2-5:2	G3-3:0|B3-5:2
B0-1:0|R4-5:0	B1-1:0|R5-5:0	B2-1:0|R6-5:0	B3-1:0|R7-5:0
G4-5:0|B4-5:4	G5-5:0|B5-5:4	G6-5:0|B6-5:4	G7-5:0|B7-5:4
B4-3:0|R8-5:2	B5-3:0|R9-5:2	B6-3:0|R9-5:2	B7-3:0|R11-5:2
R8-1:0|G8-5:0	R9-1:0|G9-5:0	R10-1:0|G10-5:0	R11-1:0|G11-5:0
B8-5:0|R12-5:4	B9-5:0|R13-5:4	B10-5:0|R14-5:4	B11-5:0|R15-5:4
R12-3:0|G12-5:2	R13-3:0|G13-5:2	R14-3:0|G14-5:2	R15-3:0|G15-5:2
G12-1:0|B12-5:0	G13-1:0|B13-5:0	G14-1:0|B14-5:0	G15-1:0|B15-5:0

Table 2-9: 18 bpp RGB Mapping to a Two Lane Main Link

Lane 0	Lane 1
R0-5:0|G0-5:4	R1-5:0|G1-5:4
G0-3:0|B0-5:2	G1-3:0|B1-5:2
B0-1:0|R2-5:0	B1-1:0|R3-5:0
G2-5:0|B2-5:4	G3-5:0|B3-5:4
B2-3:0|R4-5:2	B3-3:0|R5-5:2
R4-1:0|G4-5:0	R5-1:0|G5-5:0
B4-5:0|R6-5:4	B5-5:0|R7-5:4
R6-3:0|G6-5:2	R7-3:0|G7-5:2
G6-1:0|B6-5:0	G7-1:0|B7-5:0

Table 2-10: 18 bpp RGB Mapping to a One Lane Main Link

Lane 0
R0-5:0|G0-5:4
G0-3:0|B0-5:2
B0-1:0|R1-5:0
G1-5:0|B1-5:4
B1-3:0|R2-5:2
R2-1:0|G2-5:0
B2-5:0|R3-5:4
R3-3:0|G3-5:2
G3-1:0|B3-5:0

2.2.1.3.3 30 bpp RGB / YCbCr 4:4:4 (10 Bits per Component)

Table 2-11 → Table 2-13 show 30-bpp RGB / YCbCr 4:4:4 stream mapping into four, two and one lane main links.

Table 2-11: 30 bpp RGB Mapping to a Four Lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-9:2	R1-9:2	R2-9:2	R3-9:2
R0-1:0|G0-9:4	R1-1:0|G1-9:4	R2-1:0|G2-9:4	R3-1:0|G3-9:4
G0-3:0|B0-9:6	G1-3:0|B1-9:6	G2-3:0|B2-9:6	G3-3:0|B3-9:6
B0-5:0|R4-9:8	B1-5:0|R5-9:8	B2-5:0|R6-9:8	B3-5:0|R7-9:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-9:2	G5-9:2	G6-9:2	G7-9:2
G4-1:0|B49:4	G5-1:0|B5-9:4	G6-1:0|B6-9:4	G7-1:0|B7-9:4
B4-3:0|R8-9:6	B5-3:0|R9-9:6	B6-3:0|R10-9:6	B7-3:0|R11-9:6
R8-5:0|G8-9:8	R9-5:0|G9-9:8	R10-5:0|G10-9:8	R11-5:0|G11-9:8
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-9:2	B9-9:2	B10-9:2	B11-9:2
B8-1:0|R12-9:4	B9-1:0|R13-9:4	B10-1:0|R14-9:4	B11-1:0|R15-9:4
R12-3:0|G12-9:6	R13-3:0|G13-9:6	R14-3:0|G14-9:6	R15-3:0|G15-9:6
G12-5:0|B12-9:8	G13-5:0|B13-9:8	G14-5:0|B14-9:8	G15-5:0|B15-9:8
B12-7:0	B13-7:0	B14-7:0	B15-7:0

Note: For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-12: 30 bpp RGB Mapping to a Two Lane Main Link

Lane 0	Lane 1
R0-9:2	R1-9:2
R0-1:0|G0-9:4	R1-1:0|G1-9:4
G0-3:0|B0-9:6	G1-3:0|B1-9:6
B0-5:0|R2-9:8	B1-5:0|R3-9:8
R2-7:0	R3-7:0
G2-9:2	G3-9:2
G2-1:0|B2-9:4	G3-1:0|B3-9:4
B2-3:0|R4-9:6	B3-3:0|R5-9:6
R4-5:0|G4-9:8	R5-5:0|G5-9:8
G4-7:0	G5-7:0
B4-9:2	B5-9:2
B4-1:0|R6-9:4	B5-1:0|R7-9:4
R6-3:0|G6-9:6	R7-3:0|G7-9:6
G6-5:0|B6-9:8	G7-5:0|B7-9:8
B6-7:0	B7-7:0

Note: For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-13: 30 bpp RGB Mapping to a One Lane Main Link

Lane 0
R0-9:2
R0-1:0|G0-9:4
G0-3:0|B0-9:6
B0-5:0|R1-9:8
R1-7:0
G1-9:2
G1-1:0|B1-9:4
B1-3:0|R2-9:6
R2-5:0|G2-9:8
G2-7:0
B2-9:2
B2-1:0|R3-9:4
R3-3:0|G3-9:6
G3-5:0|B3-9:8
B3-7:0

Note: For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

2.2.1.3.4 36 bpp RGB / YCbCr 4:4:4 (12 Bits per Component)

Table 2-14 - Table 2-16 show 36 bpp RGB / YCbCr 4:4:4 stream mapping into four, two and one lane main links.

Table 2-14: 36 bpp RGB Mapping to a Four lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-11:4	R1-11:4	R2-11:4	R3-11:4
R0-3:0|G0-11:8	R1-3:0|G1-11:8	R2-3:0|G2-11:8	R3-3:0|G3-11:8
G0-7:0|B0-11:8	G1-7:0|B1-11:8	G2-7:0|B2-11:8	G3-7:0|B3-11:8
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-11:4	R5-11:4	R6-11:4	R7-11:4
R4-3:0|G4-11:8	R5-3:0|G5-11:8	R6-3:0|G6-11:8	R7-3:0|G7-11:8
G4-7:0|B4-11:8	G5-7:0|B5-11:8	G6-7:0|B6-11:8	G7-7:0|B7-11:8
B4-7:0	B5-7:0	B6-7:0	B7-7:0

Note: For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-15: 36 bpp RGB Mapping to a Two Lane Main Link

Lane 0	Lane 1
R0-11:4	R1-11:4
R0-3:0|G0-11:8	R1-3:0|G1-11:8
G0-7:0|B0-11:8	G1-7:0|B1-11:8
B0-7:0	B1-7:0
R2-11:4	R3-11:4
R2-3:0|G2-11:8	R3-3:0|G3-11:8
G2-7:0|B2-11:8	G3-7:0|B3-11:8
B2-7:0	B3-7:0

Note: For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-16: 36 bpp RGB Mapping to a One Lane Main Link

Lane 0
R0-11:4
R0-3:0|G0-11:8
G0-7:0|B0-11:8
B0-7:0
R1-11:4
R1-3:0|G1-11:8
G1-7:0|B1-11:8
B1-7:0

Note: For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

2.2.1.3.5 48 bpp RGB / YCbCr 4:4:4 (16 Bits per Component)

Table 2-17 → Table 2-19 show 48 bpp RGB / YCbCr 4:4:4 stream mapping into four, two and one lane main links.

Table 2-17: 48 bpp RGB Mapping to a Four Lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
R0-15:8	R1-15:8	R2-15:8	R3-15:8
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-15:8	G1-15:8	G2-15:8	G3-15:8
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-15:8	B1-15:8	B2-15:8	B3-15:8
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-15:8	R5-15:8	R6-15:8	R7-15:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-15:8	G5-15:8	G6-15:8	G7-15:8
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-15:8	B5-15:8	B6-15:8	B7-15:8
B4-7:0	B5-7:0	B6-7:0	B7-7:0

Note: For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-18: 48 bpp RGB Mapping to a Two Lane Main Link

Lane 0	Lane 1
R0-15:8	R1-15:8
R0-7:0	R1-7:0
G0-15:8	G1-15:8
G0-7:0	G1-7:0
B0-15:8	B1-15:8
B0-7:0	B1-7:0
R2-15:8	R3-15:8
R2-7:0	R3-7:0
G2-15:8	G3-15:8
G2-7:0	G3-7:0
B2-15:8	B3-15:8
B2-7:0	B3-7:0

Note: For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

Table 2-19: 48 bpp RGB Mapping to a One Lane Main Link

Lane 0
R0-15:8
R0-7:0
G0-15:8
G0-7:0
B0-15:8
B0-7:0

Lane 0
R1-15:8
R1-7:0
G1-15:8
G1-7:0
B1-15:8
B1-7:0

Note: For YCbCr 4:4:4, replace R with Cr, G with Y, and B with Cb.

2.2.1.3.6 16 bpp YCbCr 4:2:2 (8 Bits per Component)

Table 2-20 → Table 2-22 show 16 bpp YCbCr 4:2:2 stream mapping into four, two and one lane main links.

Table 2-20: 16 bpp YCbCr 4:2:2 Mapping to a Four Lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-7:0	Cr0-7:0	Cb2-7:0	Cr2-7:0
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-7:0	Cr4-7:0	Cb6-7:0	Cr6-7:0
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0
Cb8-7:0	Cr8-7:0	Cb10-7:0	Cr10-7:0
Y8-7:0	Y9-7:0	Y10-7:0	Y11-7:0

Table 2-21: 16 bpp YCbCr 4:2:2 Mapping to a Two Lane Main Link

Lane 0	Lane 1
Cb0-7:0	Cr0-7:0
Y0-7:0	Y1-7:0
Cb2-7:0	Cr2-7:0
Y2-7:0	Y3-7:0
Cb4-7:0	Cr4-7:0
Y4-7:0	Y5-7:0
Cb6-7:0	Cr6-7:0
Y6-7:0	Y7-7:0
Cb8-7:0	Cr8-7:0
Y8-7:0	Y9-7:0
Cb10-7:0	Cr10-7:0
Y10-7:0	Y11-7:0

Table 2-22: 16 bpp YCbCr 4:2:2 Mapping to a One Lane Main Link

Lane 0
Cb0-7:0
Y0-7:0
Cr0-7:0
Y1-7:0
Cb2-7:0
Y2-7:0

Lane 0
Cr2-7:0
Y3-7:0
Cb4-7:0
Y4-7:0
Cr4-7:0
Y5-7:0

2.2.1.3.7 20 bpp YCbCr 4:2:2 (10 Bits Per Component)

Table 2-23 → Table 2-25 show a 20-bpp YCbCr 4:2:2 stream mapping into four, two and one lane main links.

Table 2-23: 20 bpp YCbCr 4:2:2 Mapping to a Four Lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-9:2	Cr0-9:2	Cb2-9:2	Cb2-9:2
Cb0-1:0|Y0-9:4	Cr0-1:0|Y1-9:4	Cb2-1:0|Y2-9:4	Cb2-1:0|Y3-9:4
Y0-3:0|Cb4-9:6	Y1-3:0|Cr4-9:6	Y2-3:0|Cb6-9:6	Y3-3:0|Cr6-9:6
Cb4-5:0|Y4-9:8	Cr4-5:0|Y5-9:8	Cb6-5:0|Y6-9:8	Cr6-5:0|Y7-9:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0
Cb8-9:2	Cr8-9:2	Cb10-9:2	Cr10-9:2
Cb8-1:0|Y8-9:4	Cr8-1:0|Y9-9:4	Cb10-1:0|Y10-9:4	Cr10-1:0|Y11-9:4
Y8-3:0|Cb12-9:6	Y9-3:0|Cr12-9:6	Y10-3:0|Cb14-9:6	Y11-3:0|Cr14-9:6
Cb12-5:0|Y12-9:8	Cr12-5:0|Y13-9:8	Cb14-5:0|Y114-9:8	Cr14-5:0|Y15-9:8
Y12-7:0	Y13-7:0	Y14-7:0	Y15-7:0

Table 2-24: 20 bpp YCbCr 4:2:2 Mapping to a Two Lane Main Link

Lane 0	Lane 1
Cb0-9:2	Cr0-9:2
Cb0-1:0|Y0-9:4	Cr2-1:0|Y1-9:4
Y0-3:0|Cb2-9:6	Y1-3:0|Cr2-9:6
Cb2-5:0|Y2-9:8	Cr2-5:0|Y3-9:8
Y2-7:0	Y3-7:0
Cb4-9:2	Cr4-9:2
Cb4-1:0|Y4-9:4	Cr4-1:0|Y5-9:4
Y4-3:0|Cb6-9:6	Y5-3:0|Cr6-9:6
Cb4-5:0|Y6-9:8	Cr6-5:0|Y7-9:8
Y6-7:0	Y7-7:0

Table 2-25: 20 bpp YCbCr 4:2:2 Mapping to a One Lane Main Link

Lane 0
Cb0-9:2
Cb0-1:0|Y0-9:4
Y0-3:0|Cr0-9:6
Cr0-5:0|Y1-9:8
Y1-7:0
Cb2-9:2
Cb2-1:0|Y2-9:4

Lane 0
Y2-3:0|Cr2-9:6
Cr2-5:0|Y3-9:8
Y3-7:0

2.2.1.3.8 24 bpp YCbCr 4:2:2 (12 Bits per Component)

Table 2-26 → Table 2-28 show 24bpp YCbCr 4:2:2 stream mapping into four, two and one lane main links..

Table 2-26: 24 bpp YCbCr 4:2:2 Mapping to a Four Lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-11:4	Cr0-11:4	Cb2-11:4	Cr2-11:4
Cb0-3:0|Y0-11:8	Cr0-3:0|Y1-11:8	Cb2-3:0|Y2-11:8	Cr2-3:0|Y3-11:8
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-11:4	Cr4-11:4	Cb6-11:4	Cr6-11:4
Cb4-3:0|Y4-11:8	Cr4-3:0|Y5-11:8	Cb63:0|Y6-11:8	Cr6-3:0|Y7-11:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-27: 24 bpp YCbCr 4:2:2 Mapping to a Two Lane Main Link

Lane 0	Lane 1
Cb0-11:4	Cr0-11:4
Cb0-3:0|Y0-11:8	Cr0-3:0|Y1-11:8
Y0-7:0	Y1-7:0
Cb2-11:4	Cr2-11:4
Cb2-3:0|Y2-11:8	Cr2-3:0|Y3-11:8
Y1-7:0	Y3-7:0

Table 2-28: 24 bpp YCbCr 4:2:2 Mapping to a One Lane Main Link

Lane 0
Cb0-11:4
Cb0-3:0|Y0-11:8
Y0-7:0
Cr0-11:4
Cr0-3:0|Y1-11:8
Y1-7:0

2.2.1.3.9 32 bpp YCbCr 4:2:2 (16 Bits per Component)

Table 2-29 → Table 2-31 show 32 bpp YCbCr 4:2:2 stream mapping into four, two and one lane main links.

Table 2-29: 32 bpp YCbCr 4:2:2 Mapping to a Four Lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
Cb0-15:8	Cr0-15:8	Cb2-15:8	Cr2-15:8
Cb0-7:0	Cr0-7:0	Cb2-7:0	Cr2-7:0
Y0-15:8	Y1-15:8	Y2-15:8	Y3-15:8
Y0-7:0	Y1-7:0	Y2-7:0	Y3-7:0
Cb4-15:8	Cr4-15:8	Cb6-15:8	Cr6-15:8
Cb4-7:0	Cr4-7:0	Cb6-7:0	Cr6-7:0
Y4-15:8	Y5-15:8	Y6-15:8	Y7-15:8
Y4-7:0	Y5-7:0	Y6-7:0	Y7-7:0

Table 2-30: 32 bpp YCbCr 4:2:2 Mapping to a Two Lane Main Link

Lane 0	Lane 1
Cb0-15:8	Cr0-15:8
Cb0-7:0	Cr0-7:0
Y0-15:8	Y1-15:8
Y0-7:0	Y1-7:0
Cb2-15:8	Cr2-15:8
Cb2-7:0	Cr2-7:0
Y2-15:8	Y3-15:8
Y2-7:0	Y3-7:0

Table 2-31: 32 bpp YCbCr 4:2:2 Mapping to a One Lane Main Link

Lane 0
Cb0-15:8
Cb0-7:0
Y0-15:8
Y0-7:0
Cr0-15:8
Cr0-7:0
Y1-15:8
Y1-7:0
Cb2-15:8
Cb2-7:0
Y2-15:8
Y2-7:0
Cr2-15:8
Cr2-7:0
Y3-15:8
Y3-7:0

2.2.1.4 Symbol Stuffing and Transfer Unit

To avoid the oversubscription of the link bandwidth, the packed data rate must be equal to or lower than the link symbol rate. When the packed data rate is lower than the link symbol rate, the link layer must perform symbol stuffing. Stuffing symbols (both stuffing frame symbols and dummy data symbols) must be inserted in all lanes in the same LS_Clk cycle before inter-lane skewing.

The way symbols are stuffed must be different between active video period and blanking period.

- During the active video period:
  - Stuffing symbols must be framed with control symbols FS & FE within Transfer Unit (TU) as shown in Figure 2-13. (TU is described with an example in the next section, Section 2.2.1.4.1.) All the symbols between FS and FE must be stuffing dummy data symbols, while all the symbols in the TU before FS must be valid data symbols.
  - FS and FE must be inserted in all lanes in the same LS_Clk cycle.
  - When there is only one symbol to stuff, FE must be used and FS is omitted.
  - Transfer unit size must be 32 to 64 link symbols per lane.
  - The last TU of a horizontal video line must end with BS and must not end with a FS/FE insertion.
- During the blanking period:
  - All non-control symbols between the first BS of the blanking period and the first BE of the active video period are dummy stuffing data symbols (except for VB-ID, Mvid 7:0, and Maud 7:0). These dummy data symbols may be substituted with secondary data packets. Note that BS is inserted at the same symbol time during vertical blanking period as during the active video period, as stated in section 2.2.1.1.
  - During vertical blanking period, BS is transmitted on each lane followed by VB-ID, Mvid 7:0 and Maud 7:0. All the rest of the symbols between the BS at the beginning of vertical blanking interval and the BE at the end of the vertical blanking interval are dummy symbols that may be substituted with secondary data packets.

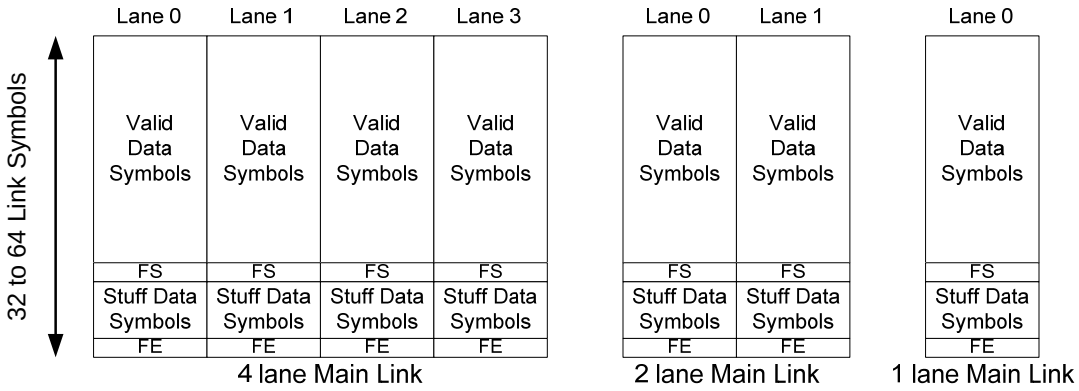


Figure 2-13: Transfer Unit

The transfer unit (TU) size must be in the range of 32 to 64 link symbols per lane. The DisplayPort Source Device must fix the TU size for a given video timing format.

The first pixel data of the horizontal active display line, immediately after BE, must be placed as the first valid data symbols of the first TU of a line. The partial pixel data of Pixel 0 must always be placed on Lane 0.

TU may end at a partial pixel boundary. For example, a part of the blue data of a pixel may be transported in one TU while the rest of the blue data for that pixel is transported in the next TU. The ratio of the valid symbol to stuffing symbol is determined by the ratio between the packed data stream rate and the link symbol rate. Depending on the packed stream rate relative to link symbol rate, a certain number of valid symbols will accumulate every "TU-size" link symbol clock cycles. The DisplayPort transmitter within the Source Device will transmit those valid symbols over the Main Link while the next accumulation starts. This process will repeat until the end of a video line is reached, which is marked by the insertion of BS symbol on all the lanes.

Using the above stuffing method, the number of valid data symbols per TU per lane (except for the last TU of a line which may be cut because of the end of active pixel) will be approximated with the following equation:

# of valid data symbols per lane = packed data rate / link symbol rate * TU size

The last TU at the end of the horizontal active display period may (or is likely to) have fewer valid data symbols than that obtained from the above equation. The DisplayPort receiver must discard all the data symbols after BS (except for VB-ID, Mvid 7:0, and Maud 7:0) as well as those "zero-padded bits" at the end of the horizontal active display period.

2.2.1.4.1 Transfer Unit Example (INFORMATIVE)

Table 2-32 shows an example of transfer unit for a 1366 x 768, 30 bpp RGB video stream (Strm_Clk = 80MHz) transported over a four lane Main Link running at 2.7 Gbps (or 270 Msymbols per second per lane). The TU size is fixed to 64 link symbols per lane in this example.

The number of valid symbols within the transfer unit is calculated as follows:

Stream: 30 bpp, 80 MHz → Packed data rate over 4 lanes = 75 Msymbols / second / lane

Average valid symbols per TU = 75M / 270M * 64 = 17.8

The number of valid data symbols per TU will naturally alternate, and over time, the average number will come to the appropriate non-integer value calculated from the above equation.

Table 2-32: Transfer Unit of 30 bpp RGB Video Over a 2.7 Gbps Per Lane Main Link

Lane 0	Lane 1	Lane 2	Lane 3
BE	BE	BE	BE
R0-9:2	R1-9:2	R2-9:2	R3-9:2
R0-1:0|G0-9:4	R1-1:0|G1-9:4	R2-1:0|G2-9:4	R3-1:0|G3-9:4
G0-3:0|B0-9:6	G1-3:0|B1-9:6	G2-3:0|B2-9:6	G3-3:0|B3-9:6
B0-5:0|R4-9:8	B1-5:0|R5-9:8	B2-5:0|R6-9:8	B3-5:0|R7-9:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-9:2	G5-9:2	G6-9:2	G7-9:2
G4-1:0|B4-9:4	G5-1:0|B5-9:4	G6-1:0|B6-9:4	G7-1:0|B7-9:4
B4-3:0|R8-9:6	B5-3:0|R9-9:6	B6-3:0|R10-9:6	B7-3:0|R11-9:6
R8-5:0|G8-9:8	R9-5:0|G9-9:8	R10-5:0|G10-9:8	R11-5:0|G11-9:8
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-9:2	B9-9:2	B10-9:2	B11-9:2
B8-1:0|R12-9:4	B9-1:0|R13-9:4	B10-1:0|R14-9:4	B11-1:0|R15-9:4
R12-3:0|G12-9:6	R13-3:0|G13-9:6	R14-3:0|G14-9:6	R15-3:0|G15-9:6
G12-5:0|B12-9:8	G13-5:0|B13-9:8	G14-5:0|B14-9:8	G15-5:0|B15-9:8
B12-7:0	B13-7:0	B14-7:0	B15-7:0
R16-9:2	R17-9:2	R18-9:2	R19-9:2
R16-1:0|G16-9:4	R17-1:0|G17-9:4	R18-1:0|G18-9:4	R19-1:0|G19-9:4
G16-3:0|B16-9:6	G17-3:0|B17-9:6	G18-3:0|B18-9:6	G19-3:0|B19-9:6
FS	FS	FS	FS
Dummy Data Symbols (44 x 4)			
FE	FE	FE	FE
B16-5:0|R20-9:8	B17-5:0|R21-9:8	B18-5:0|R22-9:8	B19-5:0|R23-9:8
R20-7:0	R21-7:0	R22-7:0	R23-7:0

Note: The pixel rate in this example is 80 Mpixels per sec. The Main Link bit rate is 2.7 Gbps per lane. The first TU of a line is marked by the blue arrow to the right of the table.

As can be seen in the above example, the valid data in a transfer unit may end at non-pixel boundary.

2.2.1.5 Main Stream Attribute/Secondary-Data Packet Insertion

The dummy stuffing data symbols during the video blanking periods (both vertical and horizontal) may be substituted either with main stream attributes data or a secondary data packet. Both must be framed with SS and SE control symbols as shown in Figure 2-14.

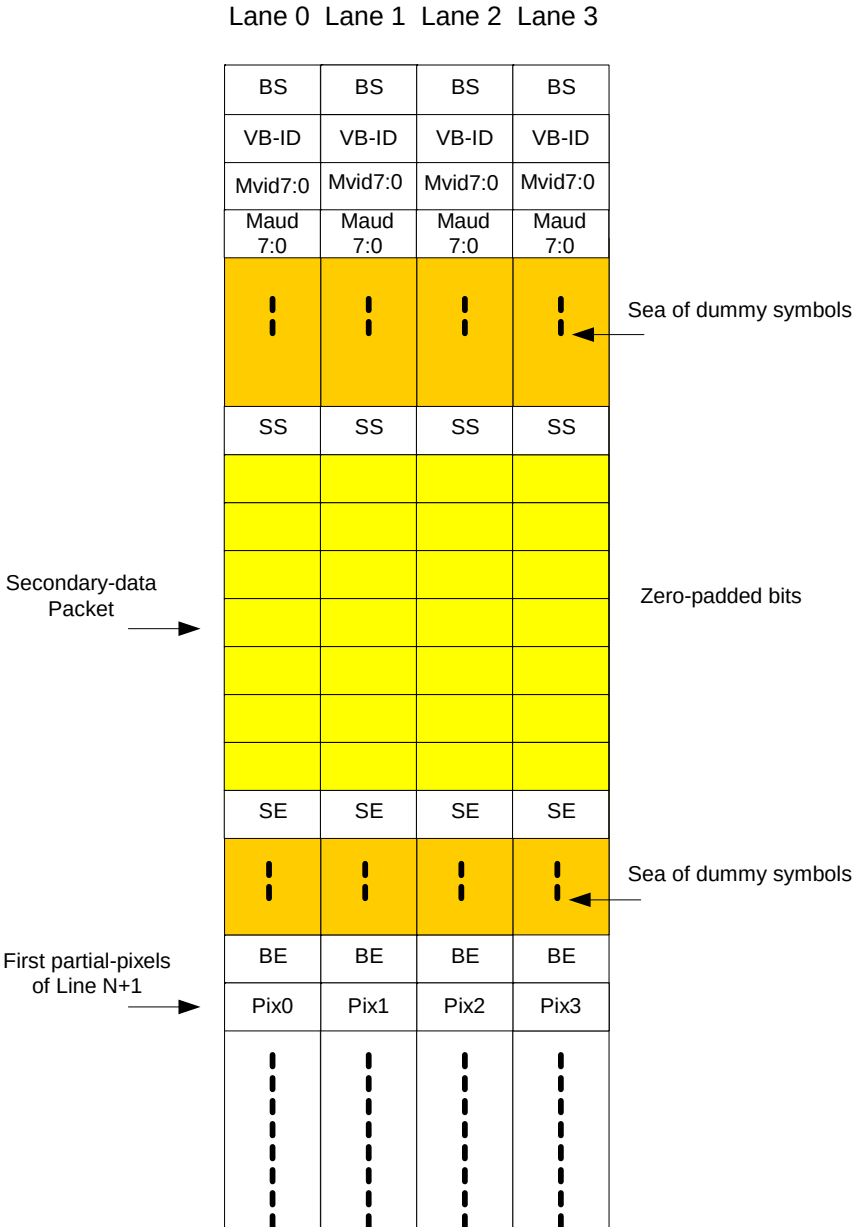


Figure 2-14: Secondary Data Insertion

Secondary data packets are used, for example, for the following purposes:

- CEA861C InfoFrame packet
- Audio stream packet
- Audio time stamp packet

Main stream attribute data must be protected via redundancy. The redundancy must be further enhanced via inter-lane skewing as described in the next section. Secondary data packets must be protected via ECC (error correcting code) based on Reed Solomon code as described in Section 2.2.6.

2.2.1.6 Inter-lane Skewing

After inserting the Main Link attributes data (and optionally, secondary data packet), the DisplayPort transmitter must insert a skew of two LS_Clk cycles between adjacent lanes. Figure 2-15 shows how the symbols must be transported after this inter-lane skewing. All the symbols, both those transmitted during video display period and those transmitted during video blanking period, are skewed by two LS_Clk period between adjacent lanes.

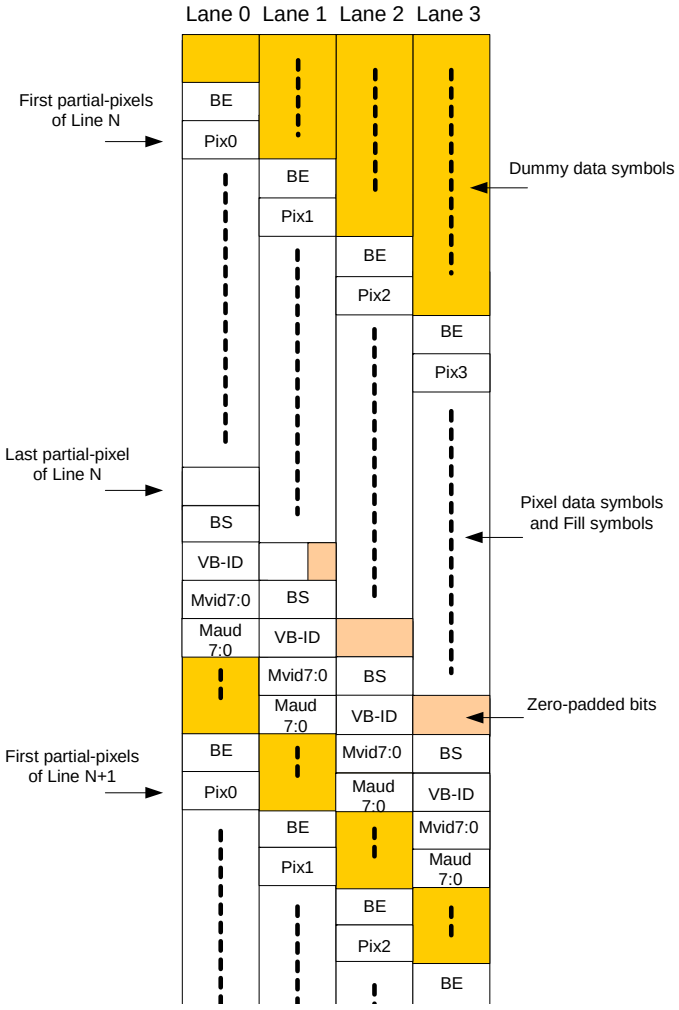


Figure 2-15: Inter-lane Skewing

The purpose of the inter-lane skewing is to increase the immunity of the link against external noise. Without inter-lane skewing an external impulse may, for example, corrupt the Mvid7:0 symbols on all lanes. Inter-lane skewing reduces the possibility of such a corruption.

2.2.2 Stream Reconstruction in the Sink

The stream reconstruction by the link layer in the Sink Device must be a mirror image of what takes place within the Source Device. The following actions must be taken by the Sink Device:

- Inter-lane de-skewing
  - Must remove the two LS_Clk skewing among adjacent lanes inserted by the transmitter
- Error correction
  - All the values of DisplayPort main stream attributes except for time stamp value M must stay constant. Therefore, the DisplayPort receiver must filter out any intermittent data corruption by comparing with the previous values.
  - As for the time stamp values Mvid / Maud and VB-ID, “majority voting” must be used to determine the value.
- Secondary-data packet de-multiplexing
  - Secondary data must be de-multiplexed using SS and SE as the separator.
    The DisplayPort receiver shall perform Reed-Solomon (15, 13) (RS (15, 13)) decoding upon extracting the secondary data packet.
- Symbol un-stuffing
  - Remove stuffing symbols.
- Data unpacking
  - Data unpacking must take place to reconstruct pixel data from data characters transported over the main link. Unpacking is dependent on the pixel data color depth and format (as described in Section 2.2.1.3),
- Stream clock recovery
  - Stream clock recovery is covered in the next section.

2.2.3 Stream Clock Recovery

This section describes the details of original stream clock recovery from the Main Link in the Sink Device. The following equations conceptually explain how the Stream clock (Strm_Clk) must be derived from the Link Symbol clock (LS_Clk) using the Time Stamps, M and N:

- f_Strm_Clk = M/N * f_LS_Clk, where
  - N = Reference pulse period / t_LS_Clk
  - M = Feedback pulse period / t_Strm_Clk

The f_Strm_Clk and the f_LS_Clk are the stream clock and the link symbol clock frequencies, while the t_Strm_Clk and t_LS_Clk are the stream clock and the link symbol clock periods, respectively. The reference pulse and feedback pulse are shown in Figure 2-16 below.

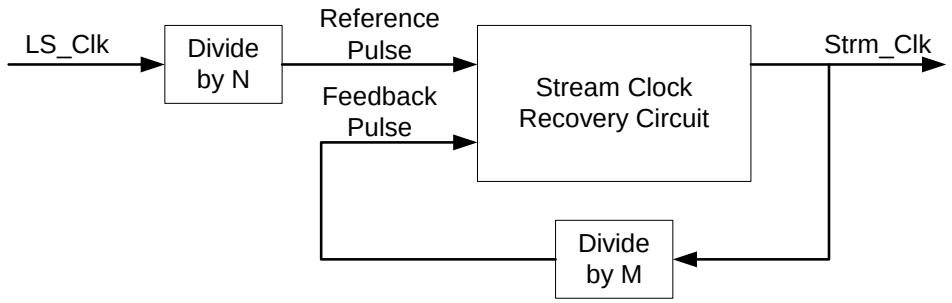


Figure 2-16: Reference Pulse and Feedback Pulse of Stream Clock Recovery Circuit

The above equation can also be expressed as:

- M/N = f_Strm_Clk/f_LS_Clk

Both M and N must be 24-bit values.

When the DisplayPort transmitter and the stream source share the same reference clock, the N and M values stay constant. This way of generating link clock and stream clock is called Synchronous Clock mode. A DisplayPort Source Device may select a stream clock frequency that allows for static and relatively small (for example, 64 or less) M and N values. These choices are implementation specific.

If the Stream clock and Link Symbol clock are asynchronous with each other, the value of M changes over time. This way of generating link clock and stream clock is called Asynchronous Clock mode. The value M must change while the value N stays constant. The value of N in this Asynchronous Clock mode must be set to 2^{15} or 32,768.

When in Asynchronous Clock mode, the DisplayPort transmitter must measure M using a counter running at the LS_Clk frequency as shown in Figure 2-17. The full counter value after every [N x LS_Clk cycles] must be transported in the DisplayPort Main Stream attributes. . The least significant eight bits of M (Mvid7:0) must be transported once per main video stream horizontal period following BS and VB-ID.

When Mvid7:0 crosses the 8-bit boundary, the entire Mvid23:0 will change. For example, when Mvid23:0 is 000FFFh at one point in time for a given main video stream, the value may turn to 0010000h at another point. The Sink Device is responsible for determining the entire Mvid23:0 value based on the updated Mvid7:0.

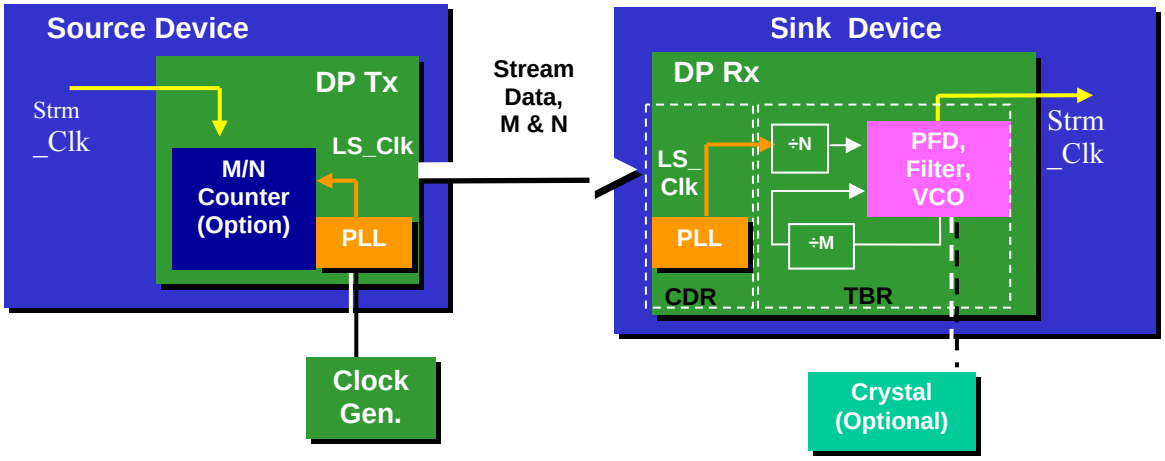


Figure 2-17: M and N Value Determination in Asynchronous Clock Mode

Note: Use of an N value of 32,768 does not mandate that the reference pulse period be 32,768 * t_LS_Clk which is roughly 121us for the high link rate. The value of N (which is 32,768 or 8000h) and M (which is measured by the counter in the transmitter) may be divided by power of two (or right-shifted) to realize the reference pulse period suited for each implementation

The method for right-shifting M depends on the required accuracy and jitter tolerance of each application. The simplest method of rounding up to the nearest integer value (thus, resulting in approximated stream clock regeneration) may be used for certain applications where the regenerated stream timing is gen-locked to the incoming data. Other applications may use a more elaborate fractional M PLL based approach for increasing the accuracy while maintaining the low jitter.

In some implementations, the value of M may be accumulated multiple times to use even bigger N and M values for stream clock regeneration.,

How to use (or even not to use) M and N values for the stream clock regeneration is implementation specific.

2.2.3.1 De-spreading of the Regenerated Stream Clock

Support for down-spreading of the link frequency (with modulation frequencies of 30 kHz or 33 kHz) to minimize EMI is required for Sink Devices compliant with the DisplayPort specification. Support for down-spreading by Source Devices is an implementation decision and is optional.

A DisplayPort Sink Device must indicate whether it is capable of supporting a down-spread link frequency in the DPCD by either setting or clearing the MAX_DOWNSPREAD bit.

For a certain Sink Device, such as an audio Sink Device, the regenerated stream clock must not have down-spreading. Such Sink Devices must perform de-spreading when regenerating the stream clock. The method of de-spreading is implementation specific.

2.2.4 Main Stream Attribute Data Transport

This section describes the Main Stream attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes must be as follows:

- M and N for stream clock recovery (24 bits each)
- Horizontal and vertical totals of the transmitted main video stream, in pixel and line counts, respectively (16 bits each)
- Horizontal and vertical active start from the leading edges of Hsync and Vsync in pixel and line counts, respectively (16 bits each)
- Hsync polarity / Hsync width and Vsync polarity and Vsync width in pixel and line count, respectively (1 bit for polarity and 15 bits for width)
  - Hsync / Vsync polarity
    - 0 = Active high pulse: Synchronization signal is high for the sync pulse width
    - 1 = Active low pulse: Synchronization signal is low for the synch pulse width
- Active video width and height in pixel and line counts, respectively (16 bits each)
- Miscellaneous (8 bits)
  - Synchronous Clock (bit 0)
    - 0 = Link clock and stream clock asynchronous
    - 1 = Link clock and stream clock synchronous
      (When 1, the value M shall be constant unless link clock down-spread enabled)
  - Component format (bits 2:1)
    - 00 = RGB
    - 01 = YCbCr 4:2:2
    - 10 = YCbCr 4:4:4
    - 11 = Reserved
  - Dynamic range (bit 3)
    - 0 = VESA range (from 0 to the maximum)
    - 1 = CEA range
  - YCbCr Colorimetry (bit 4)
    - 0 = ITU-R BT601-5
    - 1 = ITU-R BT709-5
  - Bit depth per color / component (bits 7:5)
    - 000 = 6 bits
    - 001 = 8 bits
    - 010 = 10 bits
    - 011 = 12 bits

        - 100 = 16 bits
        - 101, 110, 111 = Reserved
- Miscellaneous (8 bits)
    - Interlaced vertical total even (bit 0)
        - 0 = Number of lines per interlaced frame (consisting of two fields) is an odd number.
        - 1 = Number of lines per interlaced frame (consisting of two fields) is an even number.
    - Reserved (bits 7:1)
        - Set to 0's.

These Main Stream Attribute data must be transported as shown in Figure 2-18 (after 2-LS_Clk inter-lane de-skewing).

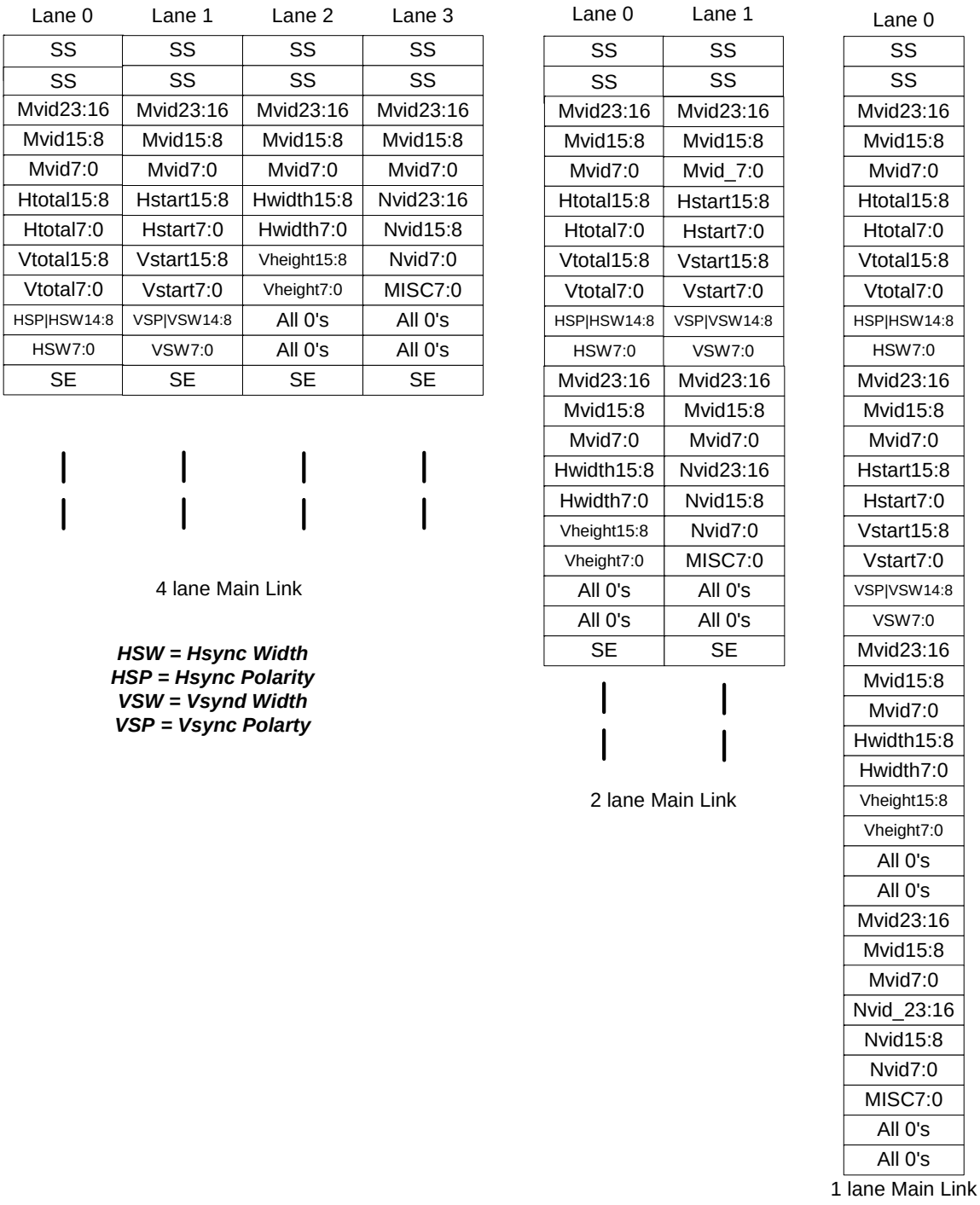


Figure 2-18: Transport of DisplayPort_MainStream_Attribute

The Main Stream Attributes packet must be distinguished from a secondary-data packet by the fact that it starts with two consecutive "SS" symbols per lane.

2.2.4.1 Main Stream Attribute for Interlaced Video Stream

An interlaced video streams frame consists of two fields:

- The top field containing the first active line of a frame

- The bottom field containing the second active line of a frame

Figure 2-19 shows the video format of an interlaced video stream that has an odd number of lines per frame and Figure 2-20 shows the case with an even number of lines per frame.

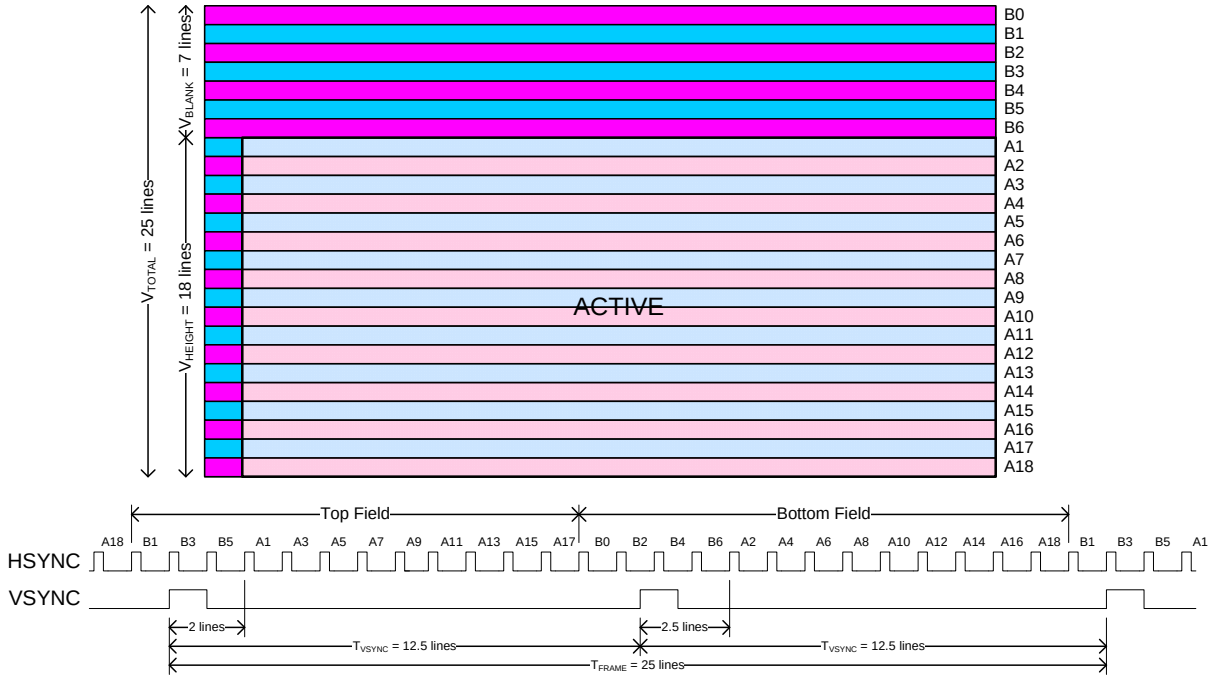


Figure 2-19: Interlaced Video Format / Timing for Odd Number of Lines per Frame

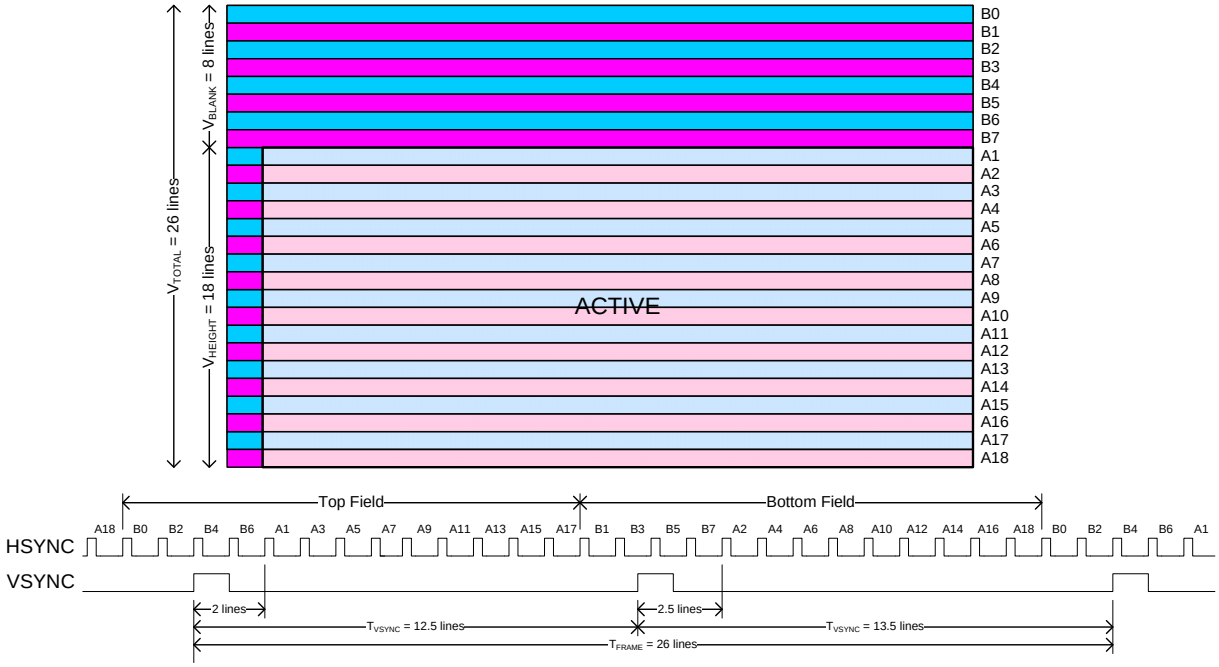


Figure 2-20: Interlaced Video Format / Timing for Even Number of Lines per Frame

When transporting an interlaced video stream, the timing parameters of the top field must always be conveyed in the Main Steam Attribute packet.

As defined in Table 2-3, VB-ID bit 2 must be set to one when an interlaced video stream is transported. Bit 1 of VB-ID is set to zero right after the last active line of the top field and to one right after the last active line of the bottom field. For non-interlaced video, bits 2:1 must remain 00).

In the example shown in Figure 2-19, the Vertical Active Start, Vertical Total, Vertical SYNC Width and Vertical Active Height of the Main Stream Attribute must be set to:

- Vertical Active Start = 2 (decimal)
- Vertical Total = 12 (decimal)
- Vertical SYNC Width = 1 (decimal)
- Vertical Active Height = 9 (decimal)

In the example shown in Figure 2-20 the Vertical Active Start, Vertical Total, Vertical SYNC Width and Vertical Active Height of the Main Stream Attribute must be set to:

- Vertical Active Start = 2 (decimal)
- Vertical Total = 13 (decimal)
- Vertical SYNC Width = 1 (decimal)
- Vertical Active Height = 9 (decimal)

In addition, bit 0 of Miscellaneous must be set to one when the number of lines per frame of the interlaced video stream is an even number.

2.2.5 Secondary-data Packing Formats

Table 2-33 shows how the secondary-data packet is constructed.

Table 2-33: Secondary-data Packet Header

Byte#	Content
HB0	Secondary-data Packet ID
HB1	Secondary-data Packet type
HB2	Secondary-data-packet-specific header byte0
HB3	Secondary-data-packet-specific header byte1

For DisplayPort, the following packet types are defined as shown in Table 2-34.

Table 2-34: Secondary-data Packet Type

Packet Type Value	Packet Type	Transmission Timing
00h	DisplayPort reserved	
01h	Audio_TimeStamp	At least once per video frame
02h	Audio_Stream	During H / V blank period of Main Video stream
03h	DisplayPort reserved	
04h	Extension	During H / V blank period of Main Video stream
05h - 7Fh	DisplayPort reserved	
80h + InfoFrame Type	CEA-861C InfoFrame	For each InfoFrame packet type, once per video frame during V-blank, 28 data bytes

If there are multiple audio streams transported simultaneously, secondary-data packet ID in HB0 must be used to associate the Audio Stream packet with its Audio Time Stamp packet and CEA-861C Audio InfoFrame packet.

2.2.5.1 InfoFrame Packet

Figure 2-21 shows an InfoFrame packet over the Main Link. (As for the parity bytes, or PB's in the diagram, refer to Section 2.2.6.). A DisplayPort Device must comply with CEA-861C when using InfoFrame. In other words, the usage of AVI InfoFrame Version 1.0 is prohibited.

InfoFrame packets must be sent once per frame during the vertical blanking period of the main video stream. For the transport of an Audio InfoFrame packet without main video stream, refer to Section 2.2.5.3.6. For more information about audio transport over DisplayPort, refer to Chapter 7.

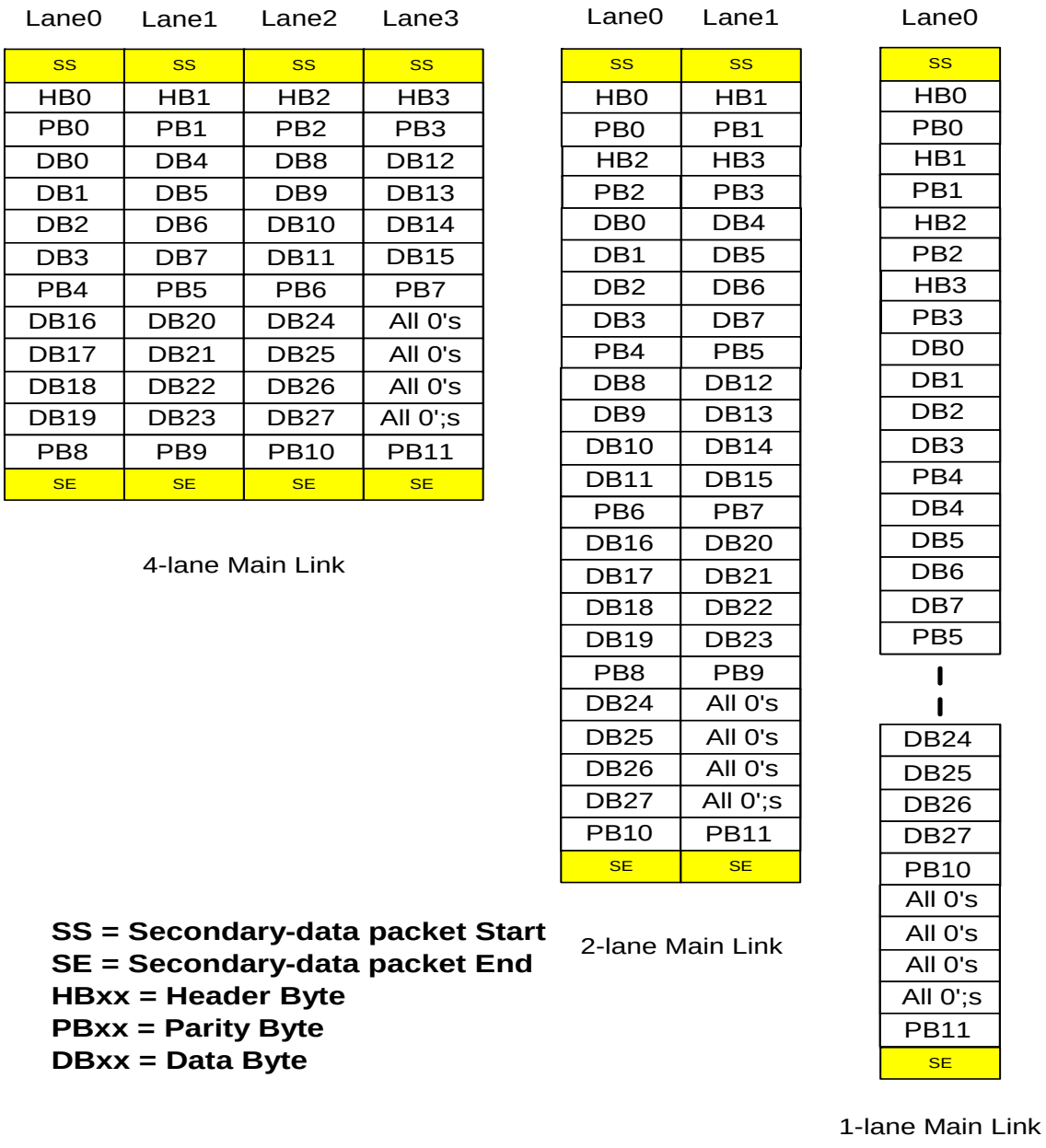


Figure 2-21: InfoFrame Packet

2.2.5.1.1 InfoFrame Packet Header

Table 2-35 summarizes the packet header bytes of InfoFrame packets

Table 2-35: Header Bytes of InfoFrame Packet

Byte#	Content
HB0	Secondary-data Packet ID InfoFrame packet, Audio Time Stamp packet, and Audio Stream packet must have the same Packet ID when they are associated with the same audio stream.
HB1	80h + InfoFrame Type value
HB2	Bits 7:0 = Least significant eight bits of (Data Byte Count – 1) For InfoFrame, the value must be 1Bh (that is, Data Byte Count = 28 bytes. Unused bytes must be zero-padded.)
HB3	Bits 1:0 = Most significant two bits of (Data Byte Count – 1) Bits 7:2 = DisplayPort version number (11h, or 010001 binary for Version 1)

2.2.5.2 Audio_TimeStamp Packet

Figure 2-22 shows an Audio_TimeStamp packet over the Main Link.

For the transport of an Audio_TimeStamp packet without the main video stream, refer to Section 2.2.5.3.6. For more information about audio transport over DisplayPort, refer to Chapter 7.

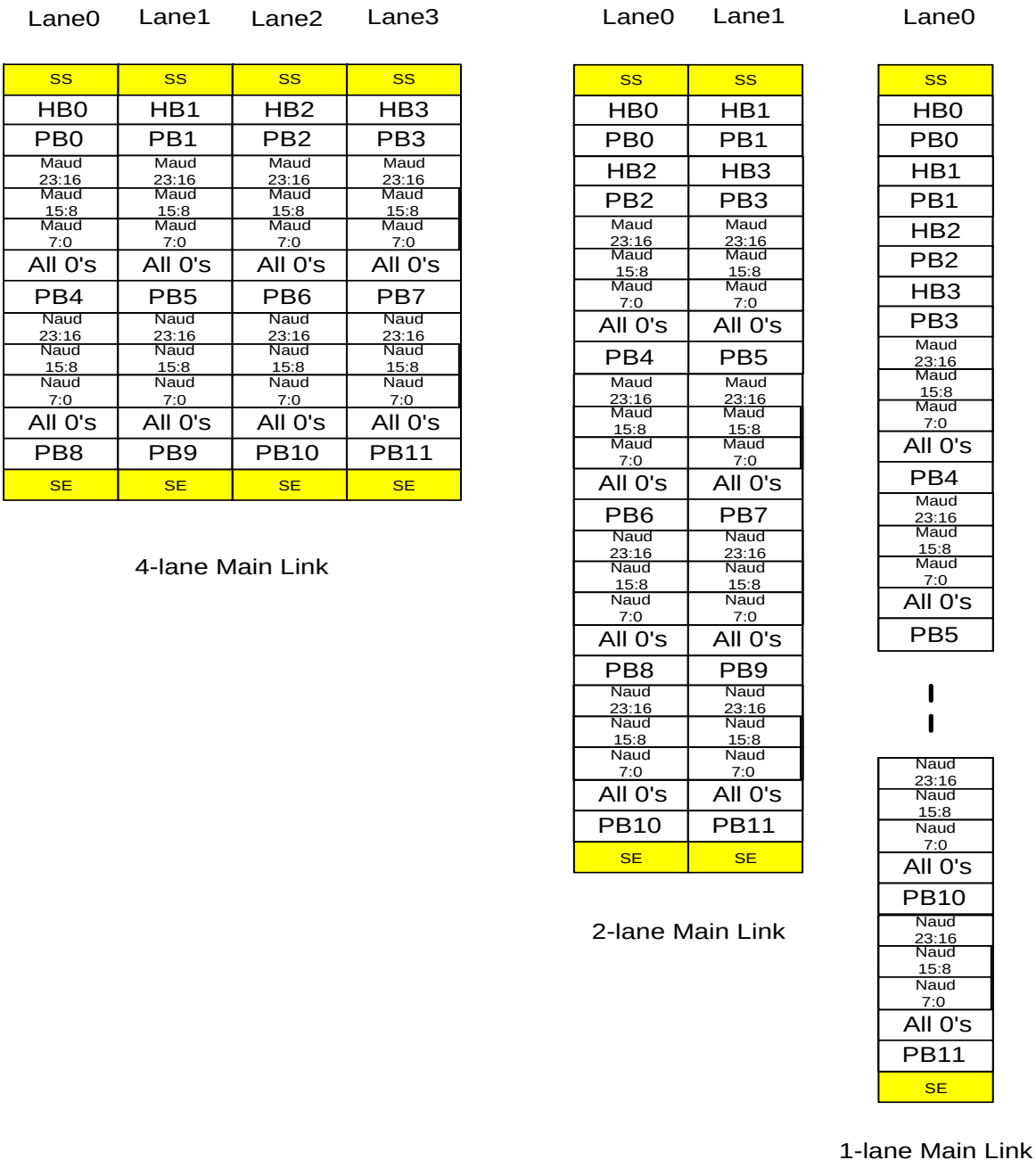


Figure 2-22: Audio_TimeStamp Packet

Audio_TimeStamp consists of Maud23:0 and Naud23:0. The relationship of Maud and Naud is expressed in the following equation:

Maud/Naud = 512 * fs / f_LS_Clk where fs is the sampling frequency of the audio stream being transported.

In addition to the Audio_TimeStamp packet, the Maud7:0 are transported once per main video stream horizontal line period immediately following Mvid7:0.

2.2.5.2.1 Audio_TimeStamp Packet Header

Table 2-36 describes the packet header bytes of Audio Time Stamp packets

Table 2-36: Header Bytes of Audio_TimeStamp Packet

Byte#	Content
HB0	Secondary-data Packet ID InfoFrame packet, Audio Time Stamp packet, and Audio Stream packet must have the same Packet ID when they are associated with the same audio stream.
HB1	01h
HB2	Bits 7:0 = Least significant eight bits of (Data Byte Count – 1) For an Audio Time Stamp packet, the value must be 17h (that is, Data Byte Count = 24 bytes). Unused bytes must be zero-padded.
HB3	Bits 1:0 = Most significant 2 bits of (Data Byte Count – 1) Bits 7:2 = DisplayPort Version Number (11h, or 010001 binary for version 1 revision 1)

2.2.5.2.2 Audio Time Stamp Values

Table 2-37 shows some examples of the audio time stamp values for various audio sampling frequencies when audio clock and Link Symbol clock are synchronous.

Note: Either when down-spreading of the link is enabled or audio clock is asynchronous to the link symbol clock, the value of M will change over time. As is the case with Mvid measurement, the Naud must be set to 2^{15} (= 32,768) for Maud measurement in asynchronous clock mode.

Table 2-37: Examples of Maud and Naud Values

f_LS_Clk = 270 MHz (2.7 Gbps)		f_LS_Clk = 162 MHz (1.62 Gbps)	
Regenerated clock = 512x 48kHz (Used when fs = 48kHz)			
Maud =	512	M =	512
Naud =	5625	N =	3375
Regenerated clock = 512x 44.1kHz (Used when fs = 44.1kHz)			
Maud =	784	M =	784
Naud =	9375	N =	5625
Regenerated clock = 512x 32kHz (Used when fs = 32kHz)			
Maud =	1024	M =	1024
Naud =	16875	N =	10125

Note: No down-spreading, with synchronous clock, assumed.

2.2.5.3 Audio_Stream Packet

Transport of an audio stream is optional. When an audio stream is transported, the AudioInfoFrame packet describing the attribute of the audio stream and Audio Timestamp packet must be also transported, each once per frame during the vertical blanking period of the main video stream.

Audio_Stream packets must be sent during both horizontal and vertical blanking periods of the main video stream. During the horizontal and vertical blanking period, DisplayPort Source Device must transmit an

Audio_Stream Packet whenever it has enough data to form a packet and access to the Main Link to transmit the packet(s). For more information about audio transport over DisplayPort, refer to Chapter 7.

2.2.5.3.1 Audio_Stream Packet Header

Table 2-38 describes the packet header of an Audio_Stream packet.

Table 2-38: Header Bytes of Audio_Stream Packet

Byte#	Content
HB0	Secondary-data Packet ID InfoFrame packet, Audio Time Stamp packet, and Audio Stream packet must have the same Packet ID when they are associated with the same audio stream.
HB1	02h
HB2	Reserved (all 0's)
HB3	Bits 2:0 = ChannelCount Actual channel count – 1 Bit 3 = Reserved (= 0) Bits 7:4 = Coding Type 0000 = IEC60958-like coding All other values are reserved for DisplayPort

2.2.5.3.2 Audio_Stream Data Mapping Over the Main Link

Channel count is the count of audio channels transmitted through DisplayPort link. The receiver must use this three bit value to decide how to interpret the payload of Audio Stream Packet. One to eight channels are supported in DisplayPort.

Table 2-39 shows the Audio_Stream Packet mapping over the Main Link for 1 → 2 channel audio and

Table 2-40 shows the mapping for 3 → 8 channel mapping.

- For one and two channel audio, two sets of 32 bit audio packet payload carry one audio sample
- For three to eight channel audio, eight sets of 32 bit audio packet payload carry one audio sample.

Those sets of 32 bit audio packet payloads that carry the same audio sample must have the same value in the SP (Sample Present) bit. If the sample is present then SP must be set to one and if the sample is absent then SP must be set to zero.

An Audio_Stream packet transfer must not stop in the middle of an audio sample.

For example, when a 2-channel audio is transmitted over a one lane Main Link, the packet may be ended after PB5 in Table 2-39 since the transmission of sample 0 is completed at that point. However, it must not end after PB4.

The mapping of audio data to channels depends on the audio-data-to-speaker mapping described in section 2.2.5.3.3.

Table 2-39: Audio_Stream Packet over the Main Link for One or Two Channel Audio

Four Lane Main Link				Two Lane Main Link		One Lane Main Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0

SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_Ch1_B0	S0_Ch2_B0	S1_Ch1_B0	S1_Ch2_B0	HB1	HB2	HB1
S0_Ch1_B1	S0_Ch2_B1	S1_Ch1_B1	S1_Ch2_B1	PB2	PB3	PB1
S0_Ch1_B2	S0_Ch2_B2	S1_Ch1_B2	S1_Ch2_B2	S0_Ch1_B0	S0_Ch2_B0	HB2
S0_Ch1_B3	S0_Ch2_B3	S1_Ch1_B3	S1_Ch2_B3	S0_Ch1_B1	S0_Ch2_B1	PB2
PB4	PB5	PB6	PB7	S0_Ch1_B2	S0_Ch2_B2	HB3
S2_Ch1_B0	S2_Ch2_B0	S3_Ch1_B0	S3_Ch2_B0	S0_Ch1_B3	S0_Ch2_B3	PB3
S2_Ch1_B1	S2_Ch2_B1	S3_Ch1_B1	S3_Ch2_B1	PB4	PB5	S0_Ch1_B0
S2_Ch1_B2	S2_Ch2_B2	S3_Ch1_B2	S3_Ch2_B2	S1_Ch1_B0	S1_Ch2_B0	S0_Ch1_B1
S2_Ch1_B3	S2_Ch2_B3	S3_Ch1_B3	S3_Ch2_B3	S1_Ch1_B1	S1_Ch2_B1	S0_Ch1_B2
PB8	PB9	PB10	PB11	S1_Ch1_B2	S1_Ch2_B2	S0_Ch1_B3
				S1_Ch1_B3	S1_Ch2_B3	PB4
				PB7	PB8	S0_Ch2_B0
				S2_Ch1_B0	S2_Ch2_B0	S0_Ch2_B1
				S2_Ch1_B1	S2_Ch2_B1	S0_Ch2_B2
				S2_Ch1_B2	S2_Ch2_B2	S0_Ch2_B3
				S2_Ch1_B3	S2_Ch2_B3	PB5

"S" stands for Sample, "B" for Byte, and "Ch" for Channel. For example, S0_Ch1_B0 means Byte 0 of Channel 1 of Sample 0.

Table 2-40: Audio Stream Packet over the Main Link for Three to Eight Channel Audio

Four Lane Main Link				Two Lane Main Link		One Lane Main Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
SS	SS	SS	SS	SS	SS	SS
HB0	HB1	HB2	HB3	HB0	HB1	HB0
PB0	PB1	PB2	PB3	PB0	PB1	PB0
S0_Ch1_B0	S0_Ch1_B0	S0_Ch2_B0	S0_Ch3_B0	HB2	HB3	HB1
S0_Ch1_B1	S0_Ch1_B1	S0_Ch2_B1	S0_Ch3_B1	PB2	PB3	PB1
S0_Ch1_B2	S0_Ch1_B2	S0_Ch2_B2	S0_Ch3_B2	S0_Ch1_B0	S0_Ch2_B0	HB2
S0_Ch1_B3	S0_Ch1_B3	S0_Ch2_B3	S0_Ch3_B3	S0_Ch1_B1	S0_Ch2_B1	PB2
PB4	PB5	PB6	PB7	S0_Ch1_B2	S0_Ch2_B2	HB3
S0_Ch5_B0	S0_Ch5_B0	S0_Ch6_B0	S0_Ch7_B0	S0_Ch1_B3	S0_Ch2_B3	PB3
S0_Ch5_B1	S0_Ch5_B1	S0_Ch6_B1	S0_Ch7_B1	PB4	PB5	S0_Ch1_B0
S0_Ch5_B2	S0_Ch5_B2	S0_Ch6_B2	S0_Ch7_B2	S0_Ch3_B0	S0_Ch4_B0	S0_Ch1_B1
S0_Ch5_B3	S0_Ch5_B3	S0_Ch6_B3	S0_Ch7_B3	S0_Ch3_B1	S0_Ch4_B1	S0_Ch1_B2
PB8	PB9	PB10	PB11	S0_Ch3_B2	S0_Ch4_B2	S0_Ch1_B3
				S0_Ch3_B3	S0_Ch4_B3	PB4
				PB6	PB7	S0_Ch2_B0
				S0_Ch5_B0	S0_Ch6_B0	S0_Ch2_B1
				S0_Ch5_B1	S0_Ch6_B1	S0_Ch2_B2
				S0_Ch5_B2	S0_Ch6_B2	S0_Ch2_B3
				S0_Ch5_B3	S0_Ch6_B3	PB5
				PB8	PB9	S0_Ch3_B0

Four Lane Main Link				Two Lane Main Link		One Lane Main Link
Lane 0	Lane 1	Lane 2	Lane 3	Lane 0	Lane 1	Lane 0
				S0_Ch7_B0	S0_Ch8_B0	S0_Ch3_B1
				S0_Ch7_B1	S0_Ch8_B1	S0_Ch3_B2
				S0_Ch7_B2	S0_Ch8_B2	S0_Ch3_B3
				S0_Ch7_B3	S0_Ch8_B3	PB6
				PB10	PB11	S0_Ch4_B0
						S0_Ch4_B1
						S0_Ch4_B2
						S0_Ch4_B3
						PB7
						S0_Ch5_B0
						S0_Ch5_B1
						S0_Ch5_B2
						S0_Ch5_B3
						PB8
						S0_Ch6_B0
						S0_Ch6_B1
						S0_Ch6_B2
						S0_Ch6_B3
						PB9
						S0_Ch7_B0
						S0_Ch7_B1
						S0_Ch7_B2
						S0_Ch7_B3
						PB10
						S0_Ch8_B0
						S0_Ch8_B1
						S0_Ch8_B2
						S0_Ch8_B3
						PB11

"S" stands for Sample, "B" for Byte, and "Ch" for Channel. For example, S0_Ch1_B0 means the Byte 0 of Channel 1 of Sample 0.

2.2.5.3.3 Speakers mapping

The transported audio channel data must be mapped to the speakers according to the eight bit data, CA7:0, which is transported as data byte four within the Audio InfoFrame, as defined in Section 6.6.2 of the CEA-861-C document.

2.2.5.3.4 Data Mapping within Audio_Stream Packet Payload

An Audio_Stream packet payload consists of four bytes of data per lane, each four bytes protected by a parity byte.

Figure 2-23 shows the data mapping within the four byte payload of an Audio_Stream packet. In the previous two tables (Table 2-39and

Table 2-40), these four bytes correspond to, for example, S0_Ch0_B0, S0_Ch0_B1, S0_Ch0_B2, and S0_Ch0_B3.

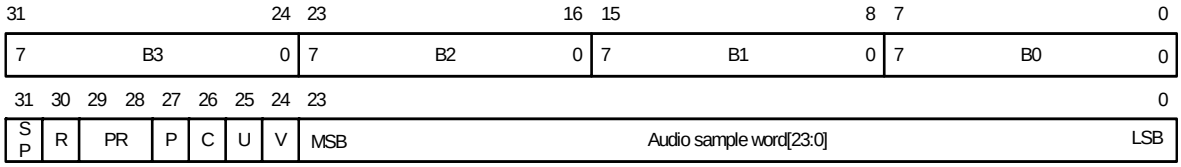


Figure 2-23: Data Mapping Within the Four Byte Payload of an Audio_Stream Packet

Table 2-41 shows the bit definition of the four byte payload shown in Figure 2-23.

Table 2-41: Bit Definition of the Payload of an Audio_Stream Packet with IEC60958-like Coding

Bit name	Bit position	Description
Audio sample word	Byte 2 bits 7:0 Byte 1 bits 7:0 Byte 0 bits 7:0	Audio data. Content of this data depends on the audio coding type. In case of LPCM audio, the most significant bit of the audio is placed in byte 2, bit 7. If the audio data size is less than 24 bits then unused least significant bits must be zero-padded.
V	Byte 3 bit 0	Validity flag
U	Byte 3 bit 1	User bit
C	Byte 3 bit 2	Channel status
P	Byte 3 bit 3	Parity bit
PR	Byte 3 bits 5:4	Preamble code and its correspondence with IEC-60958 preamble : 00 – Subframe 1 and start of the audio block (11101000 preamble) 01 – Subframe 1 (1110010 preamble) 10 – Subframe 2 (1110100 preamble)
R	Byte 3 bit 6	Reserved bit. It must be 0.
SP	Byte 3 bit 7	Sample present bit: 1 – Sample information is present and can be processed. 0 – Sample information is not present. All channels of one sample, whether used or unused, must have the same value for the sample present bit. This bit is especially useful when two channel audio is transported over a four lane Main Link. In this operation, Main Link lanes two and three may or may not have the audio sample data. This bit indicates whether the audio sample is present or not.

2.2.5.3.5 Other Audio Formats (INFORMATIVE)

DisplayPort Specification, only IEC60958-like packing format type is supported.

Using this format type, one to eight channel LPCM, AC3, and DTS audio stream can be transported. Other audio packing formats may be added in a future revision of DisplayPort specification while maintaining the consistent secondary-data mapping specification described in this document.

2.2.5.3.6 Transport of Audio Packets Without Main Video Stream

The DisplayPort Specification supports the transport of audio stream while no video stream is being transported over the link.

When the link is active without main video stream, a Source Device must insert a BS symbol followed by VB-ID, Mvid7:0, and Maud7:0, referred to as “BS symbol set”, every 2^{13}, or 8,192 link symbols. Both

NoVideoStream_Flag and VerticalBlanking_Flag of VB-ID must be set to 1 in this condition and Mvid7:0 is set to 00h. A Source Device must transmit an Audio_Stream packet after each BS symbol set. In addition, a Source Device must insert an Audio InfoFrame packet and an Audio_TimeStamp packet once after every 512th BS symbol set.

2.2.5.4 Extension Packet

The transport of an Extension Packet is an application or vendor specific option. A DisplayPort Source Device must write its 24-bit IEEE OUI (and additional data as needed) to the Source_ Specific field of DPCD (refer to Section 2.5.3.1), addresses 300h to 302h (and above), via the AUX CH. Then, it must read the 24-bit IEEE OUI (and additional data as needed) of the Sink Device from the Sink_ Specific field of DPCD, Addresses 400h to 402h (and above), via the AUX CH. Support of the 24-bit ID is optional.

A DisplayPort Source Device that supports an Extension Packet must transmit it only after it has confirmed that the other end of the link is a device that supports its Extension Packet. Likewise, a DisplayPort Sink Device must process the Extension Packet only after it has confirmed that the other end of the link is a device the Extension Packet of which this Sink Device supports.

A Branch Device must forward the AUX CH Write or Read Request transactions for the 24-bit IEEE OUI to its downstream device.

Figure 2-24 shows the minimum size of an Extension Packet mapped onto Main Link. The DisplayPort Source Device must generate parity bytes for both the header and data. Use of the parity for error checking and correction by the DisplayPort Sink Device is an implementation specific option.

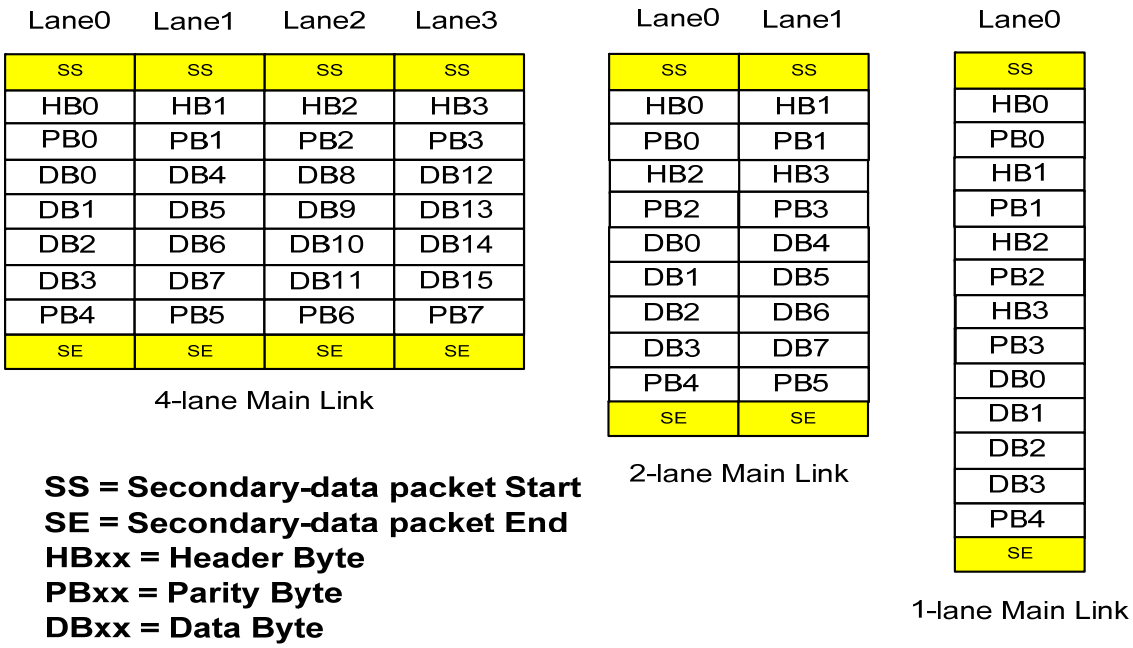


Figure 2-24: Extension Packet Mapping over the Main Link

2.2.5.4.1 Extension Packet Header

Table 2-42 summarizes the packet header bytes of InfoFrame packets

Table 2-42: Header Bytes of an Extension Packet

Byte#	Content
HB0	Usage of this byte is vendor specific
HB1	04h
HB2	Usage of this byte is vendor specific
HB3	Usage of this byte is vendor specific

2.2.6 ECC for Secondary-data Packet

All of the secondary-data packets must be protected via ECC. (DisplayPort Main Link Attributes data is protected via redundancy.)

The secondary-data packet must consist of a four byte header protected by four bytes of parity, followed by a 16 byte payload data protected by four bytes of parity. The secondary-data packet must end with a parity byte. Packets constructed with fewer than 16 bytes of data must use zero padding to fill the remaining data positions.

2.2.6.1 ECC Based on RS (15,13)

DisplayPort uses Reed-Solomon code, RS(15,13), with a symbol size of one nibble (four bits) in the ECC block.

The basic principle of error correcting encoding is to find the remainder of the message divided by a generator polynomial G(x).

The encoder works by simulating a Linear Feedback Shift Register with degree equal to G(x), and feedback taps with the coefficients of the generating polynomial of the code. In general the generator polynomial G(x) for any number of parity, configurable as the NPAR is as follows:

$$G(x) = (x - \alpha^0)(x - \alpha^1)(x - \alpha^2)(x - \alpha^3)(x - \alpha^4) \ldots (x - \alpha^{NPAR-1})$$

Since RS(15,13) with a symbol size of one nibble is chosen, the second degree generator polynomial is used as follows:

$$G(x) = (x - \alpha^0)(x - \alpha^1) = x^2 - g1 \cdot x + g0$$

Note: Subtraction is equivalent to addition in binary fields.

Therefore:

$$G(x) = x^2 + g1 \cdot x + g0 \text{ where } g1 = \alpha^4 \text{ and } g0 = \alpha$$

With encoding of the base field $GF(2^4)$, "α" is equal to (0, 0, 1, 0) which gives $\alpha^4 = (0, 0, 1, 1)$

The logic equations for implementing g1 and g0 multiplications are listed below (where c[3:0] is a 4-bit nibble being multiplied by g1 or g0):

g1·c[3:0] = {c[3]^c[2], c[2]^c[1], c[3]^c[1]^c[0], c[3]^c[0]

g0·c[3:0] = {c[2], c[1], c[3]^c[0], c[3]}

The following three messages show the outputs of ECC for input data with parity nibbles shown in underlined, bold, italic-font numbers.

- Transmitted Message:

f, e, d, c, b, a, 9, 8, ***2, 2***

- Transmitted Message:

  9, 8, 3, 2, 1, 7, 5, 4, ***8, f,***

- Transmitted Message:

  7, 6, 5, 9, 8, 1, 3, 2, ***7, 2,***

2.2.6.2 ECC g1 and g0 C-Code (INFORMATIVE)

Figure 2-25 shows the block diagram of a RS (15,13) encoder with symbol size of nibble.

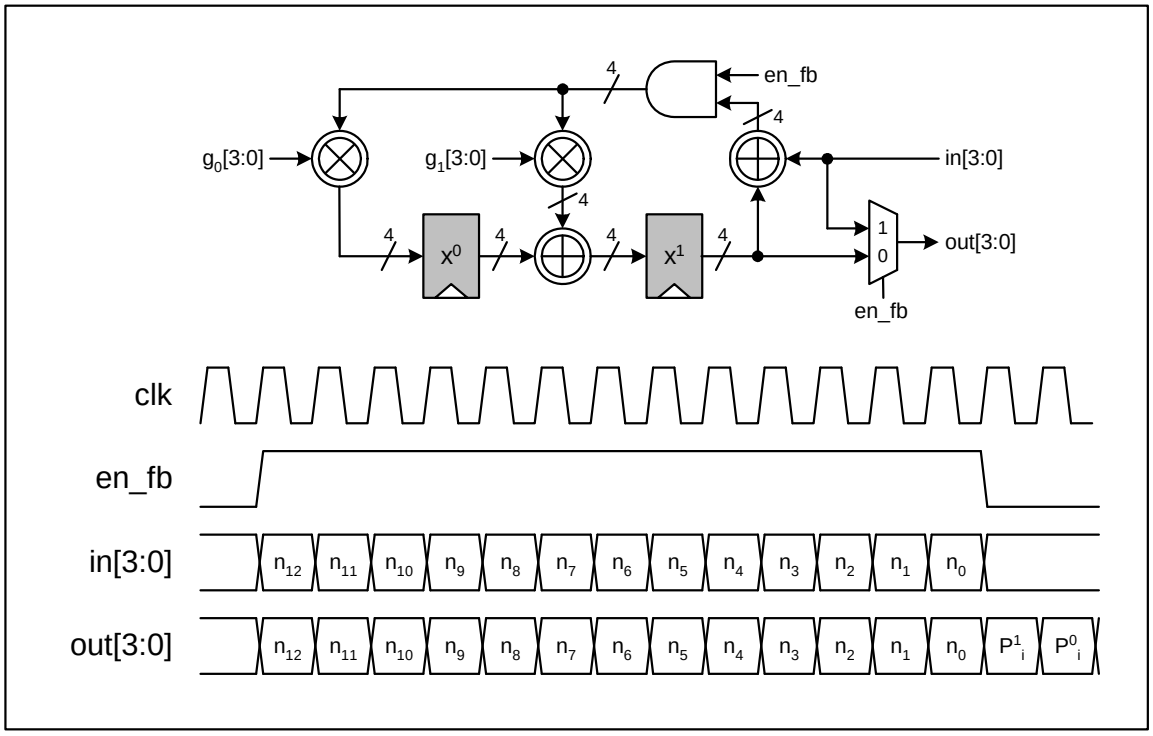


Figure 2-25: Block Diagram of a RS(15:13) Encoder

The code below shows ECC g1 and g0 in C code.

```
//-----------------------------------------------------
//c * a^1
//-----------------------------------------------------
unsigned char gfmul_1( unsigned char ) ;
unsigned char gfmul_1( a )
unsigned char a ;
{
int i ;
unsigned char c[8], gf_mul[8], r ;
```

```
 for ( i=0; i< 4; i++) {  /* Convert to single bit array for multiply */
 c[i] = a & 0x01 ;
 a = a >> 1 ;
}

gf_mul[0] = c[3] ;
gf_mul[1] = c[0] ^ c[3] ;
gf_mul[2] = c[1] ;
gf_mul[3] = c[2] ;
r = 0 ;
for ( i=0; i<4; i++) {
 r = ((gf_mul[i] & 0x01) << i) | r ;
}
return (r) ;
}
//-----------------------------------------------------
// c * a^4
//-----------------------------------------------------
unsigned char gfmul_4( unsigned char ) ;
unsigned char gfmul_4( a )
unsigned char a ;
{
int i ;
unsigned char c[8], gf_mul[8], r ;
 for ( i=0; i< 4; i++) {  /* Convert to single bit array for multiply */
 c[i] = a & 0x01 ;
 a = a >> 1 ;
}
gf_mul[0] = c[0] ^ c[3] ;
gf_mul[1] = c[0] ^ c[1]^ c[3] ;
gf_mul[2] = c[1] ^ c[2]  ;
gf_mul[3] = c[2] ^ c[3] ;
r = 0 ;
for ( i=0; i<4; i++) {
 r = ((gf_mul[i] & 0x01) << i) | r ;
```

```
}
return (r) ;
}
//-------------------------------------------------------
```

2.2.6.3 Nibble Interleaving

To further enhance the error correcting capability, the ECC block of DisplayPort incorporates nibble interleaving after the incoming data packet is error correcting encoded. Combining RS(15:13) with the nibble interleaving, the ECC block is capable of correcting up to two byte error in a 16 byte data block.

As shown in Figure 2-26 (for Payload) and Figure 2-28 (for Header), Lane 0 is interleaved with Lane 1, while Lane 2 is interleaved with Lane 3 for two and four lane Main Link configurations. Interleaving for a one lane Main Link is shown in Figure 2-27 (for Payload) and Figure 2-29 (for Header).

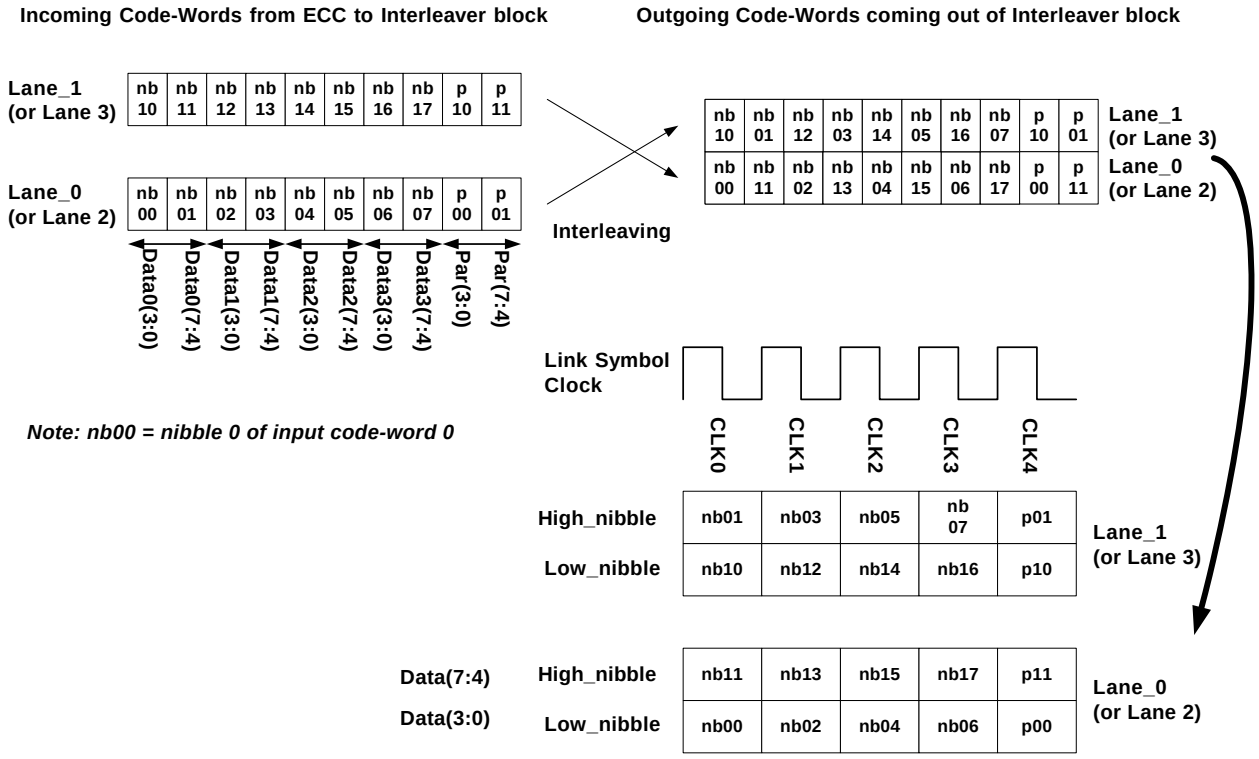


Figure 2-26: Nibble-Interleaving in the ECC Block for Two and Four Lane Main Links

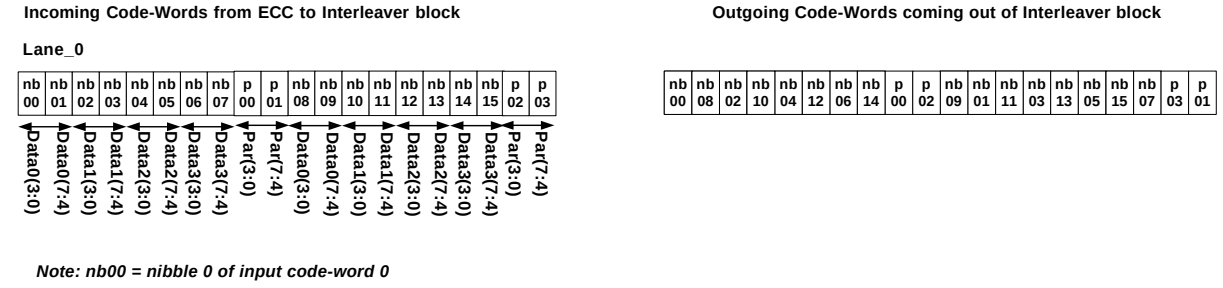


Figure 2-27: Nibble-Interleaving in the ECC Block for a One Lane Main Link

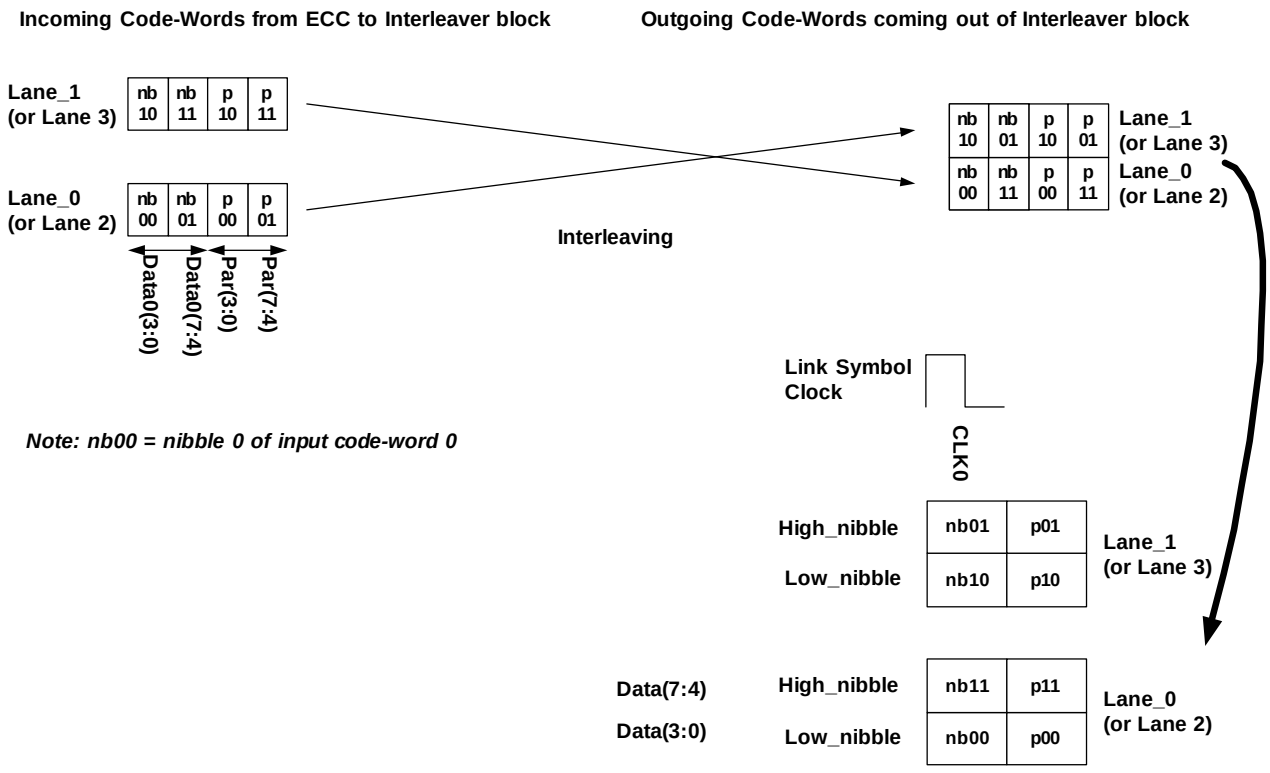


Figure 2-28: Nibble-Interleaving in the ECC Block for Two and Four Lane Main Links (Header)

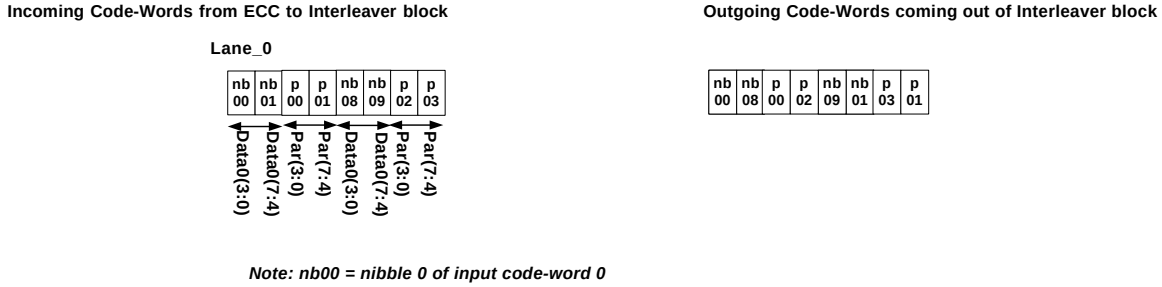


Figure 2-29: Nibble-Interleaving in the ECC Block for a One Lane Main Link (Header)

Note: The nb00 is the lowest nibble of HB0, the nb01 Is the highest nibble of HB0, the nb08 is the lowest nibble of HB1, and nb09 is the highest nibble of HB1.

Since the symbol size is a nibble (4 bits wide), the length of the code word is 15 nibbles (= $2^4 - 1$) within the ECC block.

For packet payloads, two parity nibbles (or 1 byte) must be generated for eight data nibbles (or 4 bytes) for the packet payload per lane as shown in Figure 2-30. Only10 nibbles consisting of eight data nibbles and two parity nibbles shall be used. The remaining most significant five nibbles must be zero-padded, and must not be transmitted over a DisplayPort link.

As for the packet header, four nibbles of the 15 nibbles must be used as shown in Figure 2-31. Those four nibbles consist of two data (that is, packet header) nibbles and two parity nibbles. The remaining most significant 11 nibbles must be zero-padded, and must not be transmitted. With this protection, the ECC block is capable of correcting a two byte error in a four byte packet header.

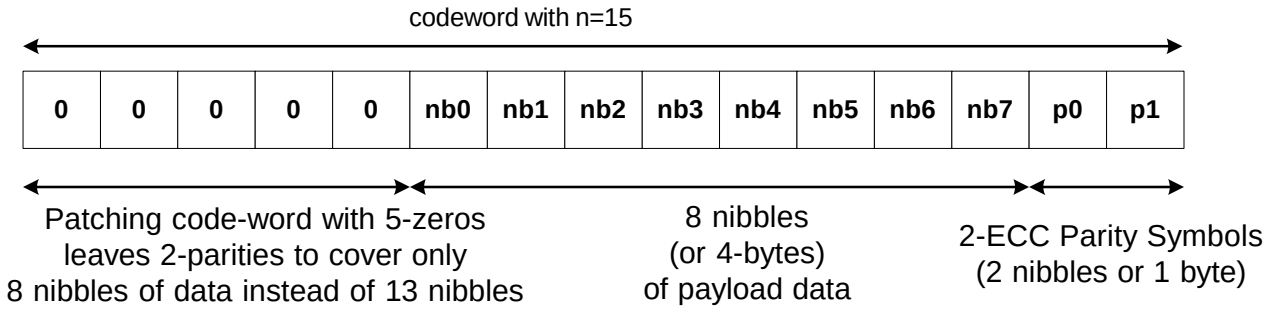


Figure 2-30: Make-up of 15 Nibble Code Word for Packet Payload

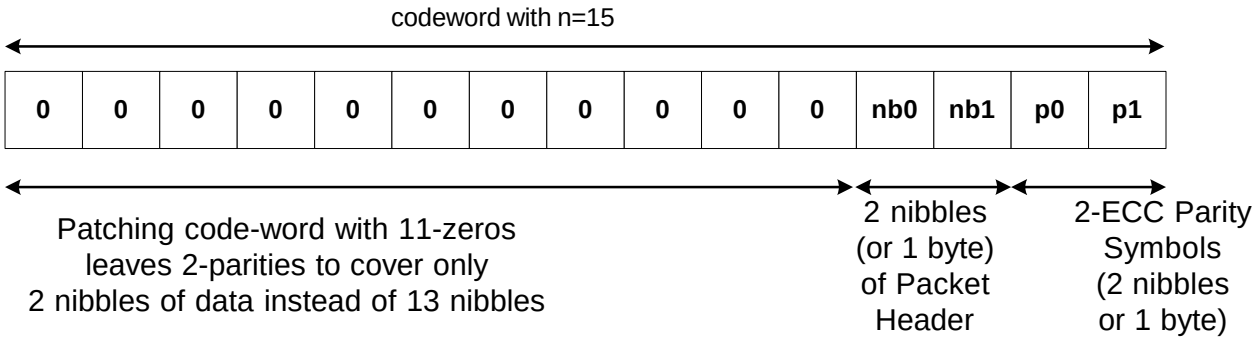


Figure 2-31: Make-up of 15 Nibble Code Word for Packet Header

2.3 AUX CH States and Arbitration

2.3.1 AUX CH STATES Overview

The AUX CH of DisplayPort is a half-duplex, bi-directional channel. The Source Device is the master of the AUX CH (called AUX CH Requester) while the Sink is the slave (AUX CH Replier). As the master, the Source Device must initiate a Request Transaction, to which the Sink responds with a Reply Transaction.

Upon detecting the Sink through the Hot Plug-Detect mechanism as described in Chapter 3 of DisplayPort Specification, the Source Device must put its AUX CH to AUX IDLE State, S2 (Figure 2-32). The Sink must also be in AUX IDLE State, D1 (Figure 2-33) when it asserts the HPD signal.

Optionally, the Sink may monitor the presence of the Source Device – see Figure 2-3 for the Source Device detection method description. If it is monitoring the presence of a Source Device, the Sink Device may enter the AUX IDLE state only when the Source is detected.

In state S2, the Source must be in "Talk Mode" and must issue a Request command as needed. The Sink, in state D1, must be in "Listen Mode" and must be waiting for a Request command.

Upon issuing a Request transaction, the Source must transition to state S3, the AUX Request CMD Pending State. In S3 state, the Source must be in "Listen Mode" waiting for the Sink to reply. Upon receipt of a Request transaction, the Sink must go to state D2, the AUX Reply CMD Pending state. Once in D2 state, the Sink must be in "Talk Mode", ready to send a reply over the AUX CH.

Upon the reception of a Request transaction, the Sink must reply within a maximum of 300 μs (Response Timer time-out period). If, for some reason, it is not able to send the reply in 300us, the Sink must go back to D1 without reply. The Source must wait for up to 400μs (Reply Timer time-out period) upon entering S3. When no reply is received in 400μs, the Source must go back to S2 and must be allowed to initiate a Request transaction as needed.

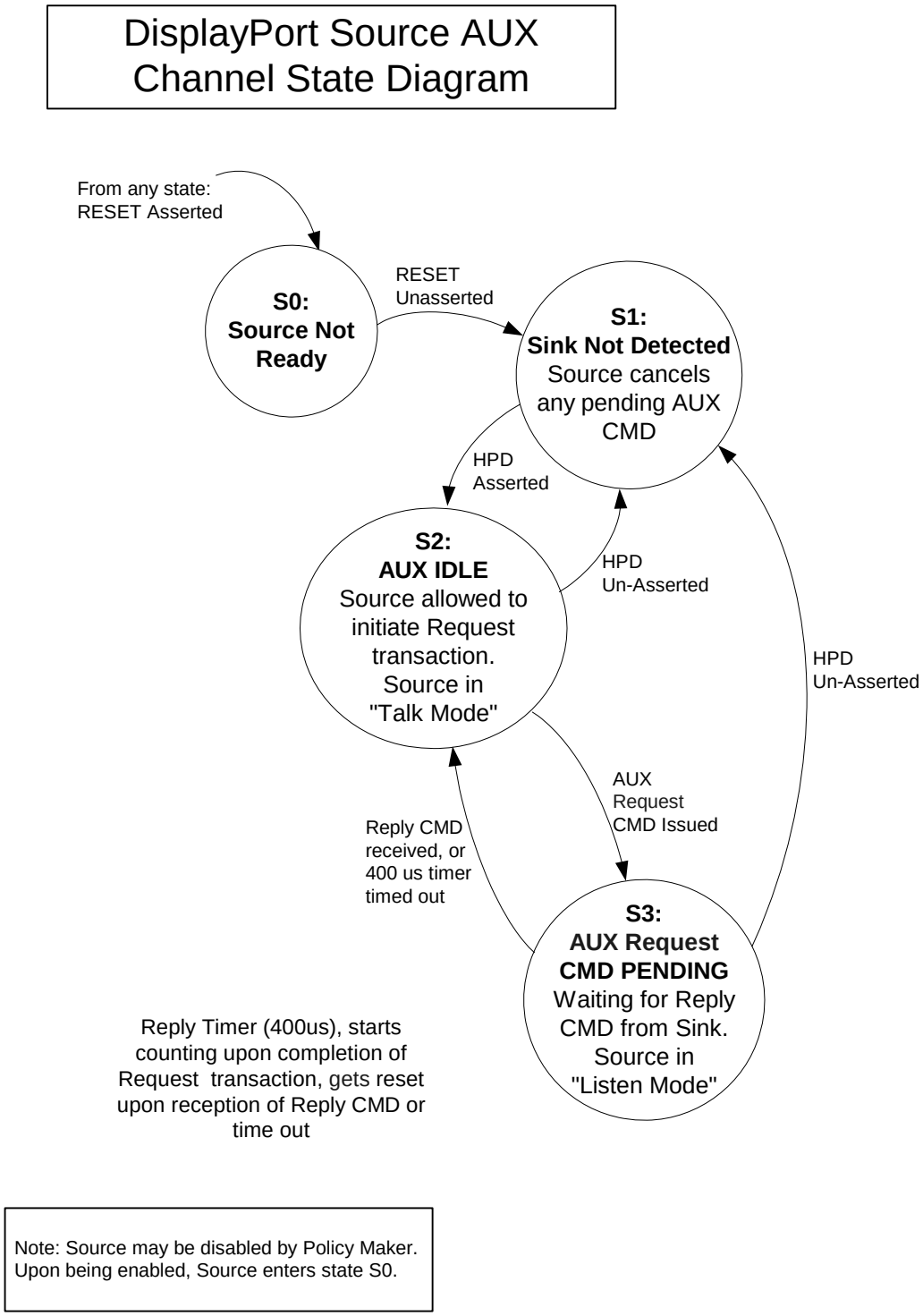


Figure 2-32: AUX CH Source State Diagram

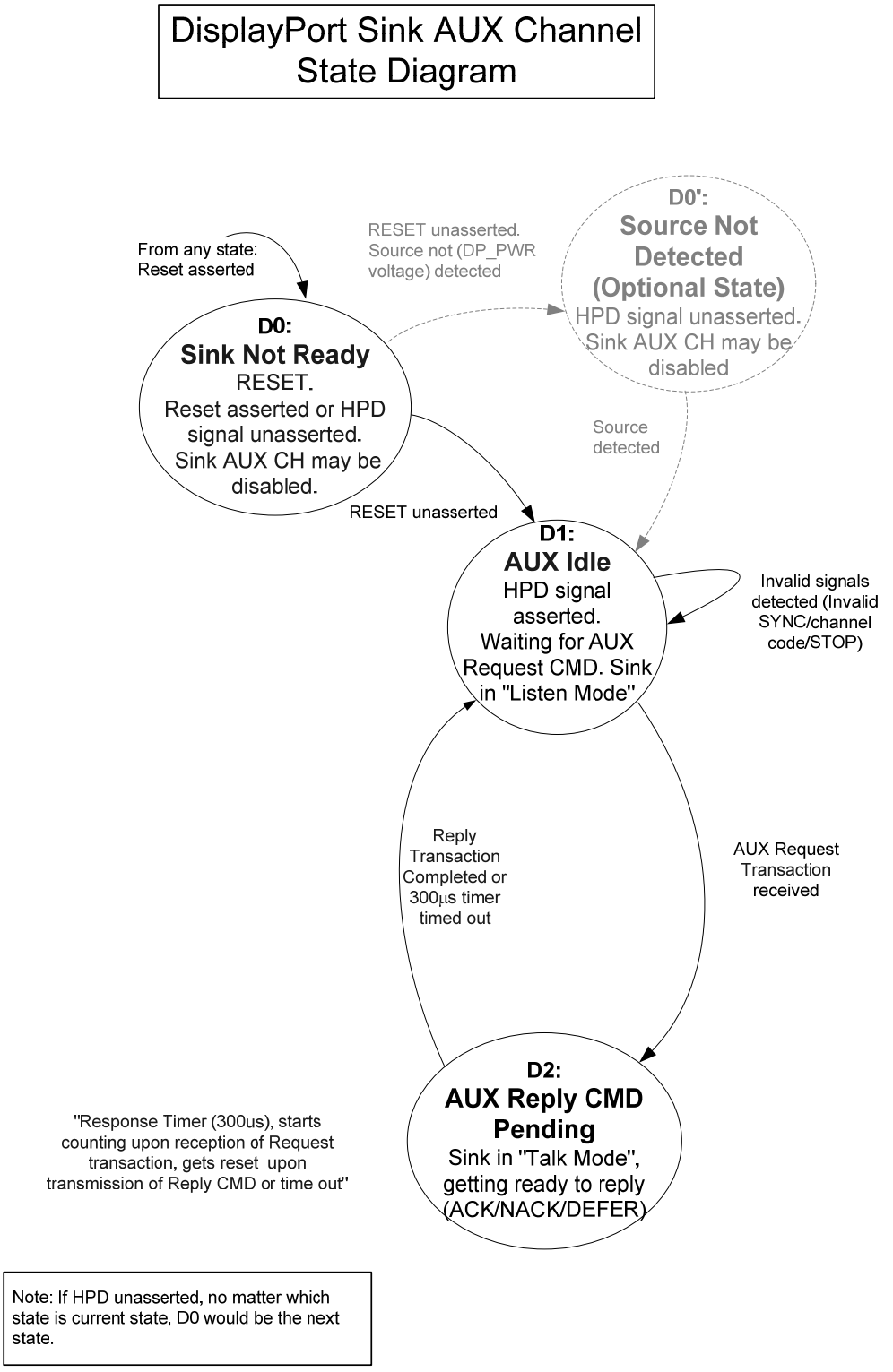


Figure 2-33: AUX CH Sink State Diagram

Transitions from D0 to D1 through the D0' state is used by Sink Devices that implement optional Source Device detect functionality. In D0' state, Reset is unasserted from Sink, but the Source is not detected. In this condition, Sink may keep HPD signal unasserted until the Source is detected. The sentence needs to be re-worded.

2.3.2 Link Layer Arbitration Control

As described above, the Source and Sink must not to be in the Talk Mode or Listen Mode at the same time. Furthermore, the Response Timer time-out period of the Sink Device must be shorter than that of Reply Timer of the Source Device. In the case of a time out, both the Source and Sink must return to the AUX IDLE state, which is Talk Mode for the Source and Listen Mode for the Sink. Therefore, contention and live lock will be avoided.

2.3.3 Policy Maker AUX CH Management

There are multiple applications and services that initiate AUX CH transactions. Some examples are:

- AUX Link Services
  - Link capability read
  - Link configuration (training)
  - Link status read
- AUX Device Services
  - EDID read
  - MCCS (Monitor Command and Control Set) control,

The DisplayPort AUX CH must not support nested transactions. In other words, one transaction must be ended before another transaction can be initiated. The Policy Maker must be responsible for determining the order in which the multiple AUX Request transactions get executed per their priorities. The Link Layer shall merely initiate AUX CH transaction as it receives the request from the Policy Maker.

A request transaction may not end in full-completion. The Sink may reply with NACK or DEFER when not ready for full-completion. The Policy Maker must decide on the follow-up action if the Request transaction is replied with NACK or DEFER.

The amount of data transported over the AUX CH per transaction must be limited to 16 bytes or fewer (that is, the burst size must be 16 data bytes maximum). This limitation is set to prevent a single transaction from monopolizing the bus for an extended period of time. With the data rate of 1Mbps, no transaction must occupy the AUX CH more than 500μs. If a given transaction requires more than 16 bytes of data to be transported, the Policy Maker must divide it into multiple transactions with no transaction larger than 16 bytes.

2.3.4 Detailed Source AUX CH State Description

Table 2-43: Source AUX CH State and Event Descriptions

State / Event	Description
S0: Reset	State S0 must be entered from any state when RESET is asserted.
S1: AUX CH unplugged	The HPD signal is un-asserted (low state). Upon entry, the level of the HPD signal must be passed up to the Link Policy Maker. The Sink Device is either not connected or has not asserted the HPD signal. The AUX CH is unavailable. Therefore, AUX CH services such as DPCD, EDID, etc. are not available.

State / Event	Description
S2: Aux IDLE	The HPD signal is asserted (high). The Sink is connected to either its main power supply or "trickle" power, though the state of the Sink Device's power switch (if any) is not specified. A message indicating AUX Channel available must be passed up to the Policy Maker. In this state no Aux Command is pending and the AUX CH is available for the Policy Maker to initiate request transactions. The source must stay in Talk Mode until a request transaction has been completed according to the AUX CH syntax as it is specified in this chapter. Upon sending STOP, the last part of a request transaction, the Source must transition to state S3 provided HPD is still asserted.
S3: AUX Request CMD PENDING	Upon completion of an AUX CH Request Transaction, the Source AUX Channel must enter state S3. In this state, the Source is waiting to receive a Reply message from the Sink. The Source must not issue commands in this state. The Source AUX Channel must stay in Listen Mode. Upon entry to this state, the Reply-Wait Timer (400 □s) must reset and start counting. The Source AUX CH must exit from this state and enter State S2, AUX IDLE state, when it receives the Reply Command from the Sink, or when its Reply Command Timer times out. In case of a Reply Timer time-out, the Source Device must retry at least three times since no reply may be due to the Sink Device "waking" from a power saving state which may take up to 1ms.
Transition from any State to S0	Occurs when Reset is asserted
Transition S0:S1	Occurs when Reset is unasserted
Transition S1:S2	Occurs upon Hot Plug Detection
Transition S2:S1 or S3:S1	Occurs upon Hot Plug Detection
Transition S2:S3	Occurs upon the completion of Source AUX CH Request Transaction
Transition of S3:S2	Must take place either when the Source AUX CH receives a Reply Command from the Sink, or when the Reply Command Timer (400 μs) times out.

2.3.5 Detailed Sink AUX CH State Description

Table 2-44: Sink AUX CH State and Event Description

State / Event	Description
D0: Sink Not Ready	The sink must transition to this state from any other state when RESET is asserted. In this state, HPD signal is unasserted. Sink AUX CH may be disabled. Upon unassertion of RESET, the Sink Device must transition to the D1 state, unless Source Device detection is implemented in which case the Sink Device must transition to the D0' state.
D0': Source Not Detected	This state is optional and may be used by Sink Devices that monitor the presence of the Source. When RESET is unasserted and HPD signal is asserted and the Source is not detected, this optional state may be entered. Upon detection of the Source Device, the Sink Device must transition to D1.
D1: Aux Idle	In this state the Sink AUX Channel must stay in "Listen Mode", waiting for the Source to send an Aux Request Command over the AUX CH. The sink AUX CH must also stay in this state after an invalid signal (e.g., invalid SYNC, STOP or channel code) is received. Upon receiving an Aux request transaction command from the Source, the Sink AUX CH must transition to state D2 and its response timer (300 μs) resets and begins counting. In Listen Mode, a Sink Device must either receive and decode the request transaction or detect the presence of a differential signal input even if it is in a power saving state. If the Sink Device is in a power saving mode and cannot reply within the Response Time-out period of 300 μs, it must exit the power saving mode within 1ms of detecting the presence of a differential signal input

State / Event	Description
	so that it can provide an AUX CH reply within three AUX CH transaction retries by the Source Device. A Sink Device must make its best effort to avoid issuing no reply except when "waking" from a power saving mode.
D2: Aux Reply CMD Pending	In this state Sink must be in "Talk Mode", getting ready to reply to the source. Upon completion of the reply transaction, the sink must transition to D1. A time-out condition of the response timer must cause the sink to transition to state D1 without initiating a reply transaction.
Transition of D0: D0' (Optional transition)	Occurs when the Reset is unasserted and HPD signal is asserted.
Transition of D0':D1 (Optional transition)	Occurs upon Source detect after the optional state of D0' is entered
Transition of D0:D1	Occurs when RESET is unasserted and when the Sink Device has asserted HPD signal and is ready to serve for AUX CH services
Transition of D1:D2	Occurs upon receiving an AUX Request transaction from the source
Transition of D2:D1	Occurs when the sink completes its reply to the source, or the sink fails to reply before the response timer (300 μs) times out

2.4 AUX CH Syntax

The syntaxes used for various AUX CH services are described in this section.

The following two categories are explained:

- Native AUX CH syntax
- Mapping of I^2C onto AUX CH syntax

This section describes the DisplayPort AUX CH transaction syntax suitable for a half-duplex, bi-directional AUX CH PHY. The number of bus turn-arounds is reduced to minimize the half-duplex overhead.

The AUX CH PHY consists of a single differential pair carrying self-clocking data. All transactions must start with a preamble "SYNC" for synchronizing the Requester (Source Device) and the Replier (Sink Device), and must end with a "STOP" condition.

A four bit command, COMM3:0, must be transmitted after the preamble, followed by a 20 bit address, ADDR19:0. The DisplayPort capability, status and control functions are directly mapped to the 20 bit address space. In addition, DisplayPort uses these 20 bits to access I^2C devices.

After the transmission of command and address, the data bytes must be transmitted except for Address-only transaction for I^2C mapping over AUX CH. Burst data transfer is supported. The burst data size must be limited to a maximum of 16 bytes.

This specification also covers the mapping of I^2C bus transactions to the DisplayPort AUX CH, and provides some examples. Bit 3 (msb) of the request command must indicate whether the transaction is a native DisplayPort or is a translated I^2C transaction.

Table 2-45: Bit / Byte Size of Various Data Types of AUX CH Syntax

Data Type	Bit Width
Command	Four bits
Address	Request transaction: 20 bits
	Reply transaction: None (0000b must be padded to Command to form a byte)
Data	Request transaction: For read: 1 Byte (Length byte) For write: 1Byte (Length byte) + N Data Bytes o Length byte ("LEN") defines the number of bytes to be written to or to be read from the AUX CH Replier (DisplayPort receiver, or Sink) by the AUX CH Requester (DisplayPort transmitter, or Source). o N = Integer value from 1 to 16. That is, Source Device is required to limit the burst data size to 16 or fewer bytes.
	Reply transaction: For read = N Data bytes. o N = Integer value from 1 to 16, the number of bytes ready to be sent. For write = 0 or 1 Data byte o When AUX CH Replier NACK's the write request transaction, it must indicate how many bytes have been written. o - For an I^2C write over the AUX CH, the AUX CH Replier, following the ACK, must indicate how many bytes have been written to the I^2C slave.

Note: In the document, "►" is attached to a signal name that is driven by the Requester, while "◄" is attached to a signal driven by the Replier.

2.4.1 Command definition

Request and reply command definitions of AUX CH transactions are described in this section.

2.4.1.1 Request command definition

Bit 3 = Native AUX CH or I^2C

1 = DisplayPort transaction

0 = I^2C transaction

- When bit 3 = 1 (Native AUX CH transaction):
  - Bits 2:0 = Request type
    - 000 = Write
    - 001= Read
- When bit 3 = 0 (I^2C transaction):
  - Bit 2 = MOT (Middle-of-Transaction) bit.
  - Bits 1:0 = I^2C_Command
    - 00 = Write
    - 01 = Read
    - 10 = Write Status_Request
    - 11 = Reserved

Note: More on MOT bit and I^2C Write Status Request in Section 2.4.5.

2.4.1.2 Reply command definition

The four bit Reply command field is divided into Native AUX CH Reply field (bits 1:0) and I^2C-over-AUX Reply field (bits 3:2). The I^2C-over-AUX Reply field is valid only when Native AUX CH Reply field is AUX_ACK (00). When Native AUX CH Reply field is not 00, then, I^2C-over-AUX Reply field must be 00 and be ignored.

Bits 1:0 = Native AUX CH Reply field

00 = AUX_ACK

- For Write transaction: All the data bytes have been written.
- For Read transaction: Ready to reply to Read request with data following.
  - DisplayPort receiver (Replier) may assert a STOP condition before transmitting the total number of requested data bytes when not all the bytes are available.

01 = AUX NACK

- For Write transaction:
  - AUX NACK must be followed by a data byte "M", where "M" indicates the number of data bytes successfully written.
  - When a Source Device is writing a DPCD address not supported by the Sink Device, the Sink Device shall reply with AUX NACK and "M" equal to zero.
  - For Read transaction:

- A Sink Device receiving a Native AUX CH read request for an unsupported DPCD address must reply with an AUX ACK and read data set equal to zero instead of replying with AUX NACK.

10 = AUX DEFER

- For Write and Read transactions:
  - Not ready for the write / read request. Source Device may retry later

11 = Reserved

Bits3:2 = I^2C-over-AUX Reply field

A DisplayPort receiver must not forward an I^2C transaction to an I^2C slave unless the AUX CH has received all the data bytes. When the DisplayPort receiver AUX CH fails to receive all the data bytes it either AUX NACK's (with "M" set equal to the number of received data bytes) or AUX DEFER's (not ready to receive the request transaction). The DisplayPort transmitter may either abort the I^2C-over-AUX transaction or retry at a later time.

I^2C-over-AUX Reply field is only valid when paired with AUX ACK.

00 = I^2C ACK

- For I^2C write transactions:
  - I^2C ACK must be followed by the data byte "M" where "M" is the number of bytes the DisplayPort receiver has written to its I^2C slave without NACK. The data byte "M" must be omitted when all the data bytes have been written. See section 2.4.5.2 for examples.
- For I^2C read transactions:
  - The I^2C slave has ACK'ed the I^2C address and the DisplayPort receiver is ready to reply with data following.
  - The DisplayPort receiver may assert a STOP condition before transmitting the total number of requested data bytes when not all the bytes are available.

01 = I^2C NACK

- For I^2C Write transaction:
  - I^2C NACK must be followed by a data byte "M". The DisplayPort receiver has written the first M bytes to its I^2C slave before getting a NACK. In case I^2C slave has NACK'ed the I^2C address , the reply transaction shall end with I^2C NACK without the data byte "M".
- For I^2C Read transaction:
  - The I^2C slave has NACK'ed the I^2C address.

10 = I^2C DEFER

- For I^2C write and read transactions:
  - The I^2C slave has yet to ACK or NACK the I^2C transaction.

11 = Reserved

2.4.2 AUX CH Response / Reply Time-outs

AUX CH Replier (the DisplayPort receiver) must start sending the reply back to the AUX CH Requester (the DisplayPort transmitter) within the response period of 300µs. The timer for Response Time-out starts ticking

after the DisplayPort receiver has finished receiving the AUX CH STOP condition which ends the AUX CH Request transaction.

The timer is reset either when the Response Time-out period has elapsed or when the DisplayPort receiver has started to send the AUX Sync pattern (which follows 10 to 16 active pre-charge pulses) for the Reply transaction.

If the DisplayPort transmitter does not receive a reply from the DisplayPort receiver it must wait for a Reply Time-out period of 400µs before initiating the next AUX CH Request transaction. The timer for the Reply Time-out starts ticking after the DisplayPort transmitter has finished sending the AUX CH STOP condition.

The timer is reset either when the Reply Time-out period elapses or when the DisplayPort transmitter detects the first zero in Manchester II code which is in active pre-charge pulses and AUX Sync pattern of the Reply transaction.

2.4.3 Native AUX CH Request Transaction Syntax

SYNC► COMM3:0|ADDR19:16► ADDR15:8► ADDR7:0► LEN7:0► (DATA0-7:0► ....) STOP

2.4.3.1 Write Request Transaction

For write transaction (COMM3:0 = 1000), the Request transaction must stop when the number of bytes (1 - 16 = LEN7:0 value + 1, all other values are invalid) has been transmitted from the Requester to the Replier.

2.4.3.2 Read Request Transaction

For read transaction (COMM3:0 = 1001), the Request transaction must stop after LEN7:0. That is, no data must be transmitted. The Requester expects the Replier to reply with [LEN7:0 value + 1] bytes (= 1 - 16 bytes) of data.

2.4.4 Native AUX CH Reply Transaction Syntax

SYNC◄ COMM3:0|0000 ◄ (DATA0-7:0◄...) STOP

2.4.4.1 Reply transaction to Write Request

A reply transaction to a write request must end in one of the two conditions below:

- The Replier has received a write request, and has completed the write. The Replier must reply to the transaction by sending AUXACK.
  - SYNC◄ 00|AUX ACK|0000 ◄ STOP,
- The Replier has received a write request, but has not completed the write. The Replier must end the transaction by sending AUX NACK as the first COMM3:0, and then, the number of written bytes M as DATA0_7:0.
  - SYNC◄ 00| NACK|0000 ◄ DATA*0*-7:0◄ STOP,

  where DATA0-7:0 shows the number of written bytes, M
- Replier has received a write request, but is not ready to accept the write request. Replier must reply with AUX_DEFER.
  - SYNC◄ 00|AUX_DEFER|0000 ◄ STOP

2.4.4.2 Reply Transaction to a Read Request

A reply transaction to a Read request must end in one of the four conditions below:

- The Replier has received a read request, but is not ready to reply with the read data. Must end the transaction by sending AUX DEFER as the first COMM3:0.
  - SYNC◄ 00|AUX DEFER|0000◄ STOP
- The Replier has received a read request and is ready. Must reply by sending AUX ACK as the first command, transmit back the number of requested bytes, assert the STOP condition, and release the AUX CH.
  - SYNC◄ 00|AUX ACK|0000◄ STOP
- The Replier has received a read request, and is ready. Must reply with AUX ACK as the first command, transmit back the number of requested bytes, assert STOP condition, and then release the AUX CH.
  - SYNC◄ 00|AUX ACK|0000 ◄ DATA*0*-7:0◄... DATA*N*-7:0◄ STOP
- The Replier has received a read request to an unsupported address. The Replier must reply with AUX ACK but send 00h for the requested length.
  - SYNC◄ 00|AUX ACK|0000 ◄ 00h◄... 00h◄ STOP

2.4.5 I^2C bus transaction mapping onto AUX CH Syntax

The mapping of an I^2C transaction onto the AUX CH transaction as defined in the DisplayPort Specification is agnostic to the application specific usage of the I^2C data bytes. Neither the DisplayPort transmitter (DP Tx) nor the DisplayPort receiver (DP Rx) must be aware of how each of the data bytes in the I^2C transaction is used for a specific I^2C application.

A single I^2C transaction may be mapped onto one or multiple AUX CH transactions to accommodate the bit-rate difference between I^2C and AUX CH. How (or whether) to divide an I^2C transaction into multiple AUX CH transactions is specific to the implementation of DP Tx. For I^2C transaction over the AUX CH, DP Tx may initiate an "Address-only" request transaction in which DP Tx will STOP the AUX CH transaction after sending the Request command field and 20-bit Address without sending LENGTH byte / data bytes.

2.4.5.1 I^2C Request Transaction Command

When bit 3 (msb) of the Request command is 0, the requested transaction must be an I^2C bus transaction. A single I^2C transaction may be divided into multiple AUX CH transactions, each with bit 3 of the Request command set to 0.

In an I^2C bus transaction, the remaining three bits of the Request command are defined as follows:

- Bit 2 = MOT (Middle-of-Transaction) bit.
  - This bit must be set when the I^2C transaction does not end (or STOP) with the current AUX CH transaction. The I^2C master in the DisplayPort receiver must send the seven bit I^2C address and read or write command only when:
    - MOT bit is set to 1 for the first time, that is, in the first AUX CH transaction for the START of an I^2C transaction,

      or
    - RepeatedStart is issued, which results either in a new I^2C address or the same I^2C address but with the read/write command opposite of the previous command.

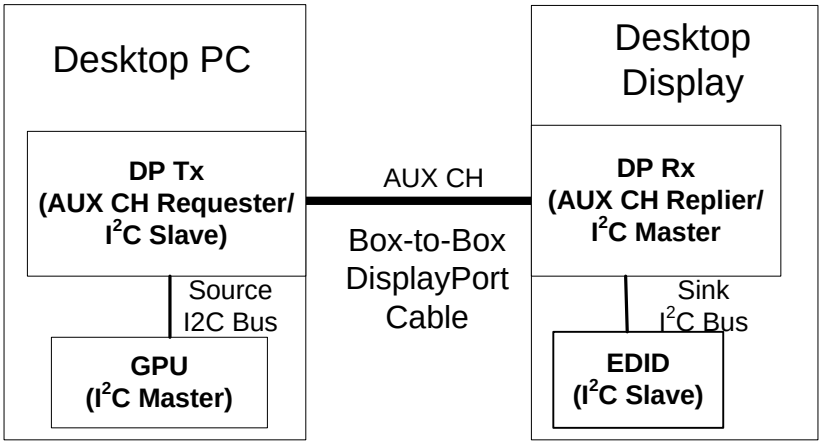
- Bits 1:0 = I²C Command
  - 00 = Write
  - 01 = Read
  - 10 = Status_Update_Request
    - When the last I²C write transaction resulted in a reply of either I²C_DEFER or ACK followed by a data byte "M" where M is the number of bytes written to the I²C slave, AUX CH Requester (DisplayPort transmitter) may issue the following special request to inquire the status of the last I²C write:

      SYNC► COM3:0 (= 0110)|0000► 0000|0000► 0|7-bit I²C address (the same as the last) ► 0000|0000 (Length byte) ► STOP►
    - To this request, AUX CH Replier (DisplayPort receiver) must reply with the latest status.
  - 11 = Reserved

2.4.5.2 I²C Write Transaction

In this section, the mapping of an I²C Write transaction onto the AUX CH transaction(s) is described using an example in which three data bytes are written. An I²C master in the Source Device will initiate an I²C Write transaction to an I²C slave in Sink Device via the AUX CH between DP Tx (in Source) and DP Rx (in Sink) as shown in Figure 2-34. Three variants of the operation are shown, demonstrating a variety of ways to accomplish the goal of performing an I²C Write transaction.

In the following descriptions, the I²C slave in the Sink Device acknowledges the I²C Write. In case the I²C slave non-acknowledges the I²C write (either I²C address is not supported or the write data byte is not accepted), what corrective action to take is up to the I²C master in the Source Device and beyond the scope of DisplayPort Specification.



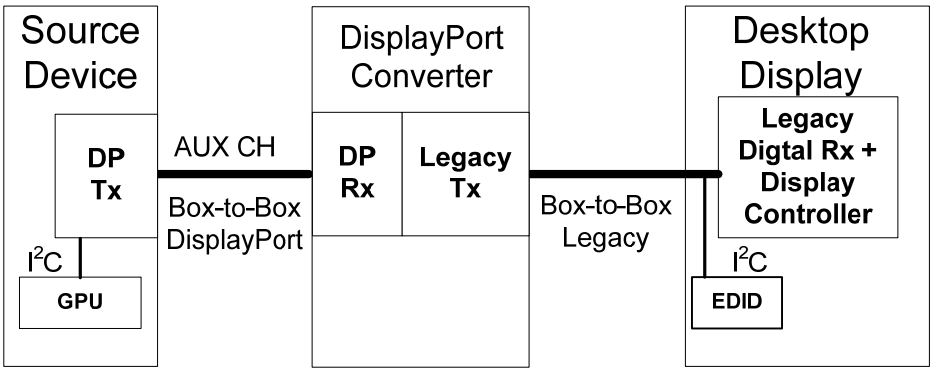


Figure 2-34: Examples of AUX CH Bridging Two I²C Buses

I²C Write example 1:

START►1001000|0►ACK◄Data0►ACK◄Data1►ACK◄Data2►ACK◄ STOP►

- I²C Write Mapping Method 1:

The I²C address byte transfer and each data byte write are mapped into separate AUX transactions. In the example shown in Table 2-46, the bit rate of the I²C bus in the Sink Device is set to 100kHz (= 10µs per bit). At this bit rate, the I²C slave in the Sink Device can acknowledge each byte within the 300µs of the Response Time-out period.

Table 2-46: I²C Write Transaction Example 1

	I²C Transaction in the Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in the Sink Device
1	START► 1001000|0► (I²C Write with I²C address = 1001000; I²C clock stretched by DP Tx before ACK)			
2		SYNC►0100|0000► 00000000►0|1001000► STOP► (Address-only transaction, with MOT = 1 and I²C address = 1001000)		
3			Wait up to 300µs	START► 1001000|0►ACK◄
4			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	
5	ACK◄Data0► (I²C clock stretched by DP Tx before ACK to Data0)			

	I²C Transaction in the Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in the Sink Device
6		SYNC►0100|0000► 00000000►0|1001000► 0000|0000►Data0► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
7			Wait up to 300□s	Data0►ACK◄
8			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	
9	ACK◄Data1► (I²C clock stretched by DP Tx before ACK to Data1)			
10		SYNC►0100|0000► 00000000►0|1001000► 0000|0000►Data1► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
11			Wait up to 300□s	Data1►ACK◄
12			SYNC◄0000|0000◄ STOP◄ (I²C ACK/AUX ACK)	
13	ACK◄Data2► (I²C clock stretched by DP Tx before ACK to Data2)			
14		SYNC►0100|0000► 00000000►0|1001000► 0000|0000►Data2► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
15			Wait up to 300□s	Data2► ACK◄
16			SYNC◄1000|0000◄ STOP◄ (I²C ACK / AUX ACK)	
17	ACK◄STOP►			
18		SYNC►0000|0000► 00000000►0|1001000► STOP► (Address-only transaction with MOT = 0 and the same I²C address, indicating I²C STOP to DP Rx)		
19			Wait up to 300□s	STOP►

	I²C Transaction in the Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in the Sink Device
20			SYNC◄1000|0000◄ STOP◄ (I²C ACK / AUX ACK)	

- I²C Write mapping method 1 with a slower I²C bus in the Sink Device:

In the version shown in Table 2-47, the bit rate of the I²C bus in the Sink Device is set to 25kHz (= 40µs per bit). At this bit rate, the I²C slave in the Sink Device cannot acknowledge even a single byte within the 300µs of the Response Time-out period. The DP Tx must issue an I²C Status Update Request in order to work with such a slow I²C bus in the Sink Device.

Table 2-47: I²C Write Transaction Method 1 with a Slow I²C Bus in the Sink Device

	I²C transaction in the Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in the Sink Device
1	START► 1001000|0► (I²C Write with I²C address = 1001000; I²C clock stretched by DP Tx before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I²C address = 1001000)		
3			Wait up to 300µs	START► 1001000|0► (DP Rx doesn't get ACK to I²C address before Reply Time-out expires)
4			SYNC◄1000|0000◄ STOP◄ (I²C DEFER / AUX ACK)	
5		SYNC►0110|0000► 00000000►0|1001000► STOP► (Status Update Request with MOT = 1 and the same I²C address)		
6			Wait up to 300µs	ACK◄ (DP Rx gets ACK to I²C address)
7			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	

	I²C transaction in the Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in the Sink Device
8	ACK◄Data0► (I²C clock stretched by DP Tx before ACK to Data0)			
9		SYNC►0100|0000► 00000000►0|1001000► 0000|0000►Data0► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
10			Wait up to 300µs	Data0► (DP Rx doesn't get ACK for Data0 write before Reply Time-out expires)
11			SYNC◄1000|0000◄ STOP◄ (I²C DEFER / AUX ACK)	
12		SYNC►0110|0000► 00000000►0|1001000► STOP► (Status Update Request with MOT = 1 and the same I²C address)		
13			Wait up to 300µs	ACK◄ (DP Rx gets ACK to Data0 write)
14			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	
15	ACK◄Data1► (I²C clock stretched by DP Tx before ACK to Data1)			
16		SYNC►0100|0000► 00000000►0|1001000► 0000|0000►Data1► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
17			Wait up to 300µs	Data1► (DP Rx doesn't get ACK for Data1 write before Reply Time-out expires)
18			SYNC◄1000|0000◄ STOP◄ (I²C DEFER / AUX ACK)	

	I²C transaction in the Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in the Sink Device
19		SYNC►0110|0000► 00000000►0|1001000► STOP► (Status Update Request with MOT = 1 and the same I²C address)		
20			Wait up to 300µs	ACK◄ (DP Rx gets ACK to Data0 write)
21			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	
22	ACK◄Data2► (I²C clock stretched by DP Tx before ACK to Data2)			
23		SYNC►0100|0000► 00000000►0|1001000► 0000|0000►Data2► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
24			Wait up to 300µs	Data2► (DP Rx doesn't get ACK for Data2 write before Reply Time-out expires)
25			SYNC◄1000|0000◄ STOP◄ (I²C DEFER / AUX ACK)	
26		SYNC►0110|0000► 00000000►0|1001000► STOP► (Status Update Request with MOT = 1 and the same I²C address)		
27			Wait up to 300µs	ACK◄ (DP Rx gets ACK to Data0 write)
28			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	
29	ACK◄STOP►			

	I²C transaction in the Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in the Sink Device
30		SYNC►0000|0000► 00000000►0|1001000► STOP► (Address-only transaction with MOT = 0 and the same I²C address, indicating I²C STOP to DP Rx)		
31			Wait up to 300µs	STOP►
32			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	

- I²C Write Mapping Method 2:

I²C address byte transfer is mapped into address only AUX CH transaction, while the write of multiple data bytes is mapped into a single AUX CH transaction (as long as the number of bytes is equal to or fewer than 16 bytes, which is the maximum burst data byte size of AUX CH transaction).

As a variation of method 2, DP Tx may combine the entire transaction (I²C address transfer and data bytes write) into a single AUX CH transaction.

Method 2 is faster than method 1. However, if the I²C slave in the sink non-acknowledges the Write Data Byte, the I²C Master in the source will not know which byte was non-acknowledged.

In the example shown Table 2-48, four bytes of data (Data0 to Data 3) are written. The bit rate of the I²C bus in Sink Device is set to 100 kHz (= 10µs per bit). At this bit rate, the I²C slave in the Sink Device can acknowledge up to three bytes within the 300µs of Response Time-out period.

Table 2-48: I²C Write Transaction Method 2

	I²C transaction in Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in Sink Device
1	START► 1001000|0► (I²C Write with I²C address = 1001000; I²C clock stretched by DP Tx before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I²C address = 1001000)		
3			Wait up to 300µs	START►1001000|0► ACK◄
4			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	

	I²C transaction in Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in Sink Device
5	ACK◄ Data0►ACK◄ Data1►ACK◄ Data2►ACK◄ Data3►ACK◄ STOP►			
6		SYNC►0000|0000► 00000000►0|1001000► 0000|0010 ►Data0► Data1►Data2► Data3► STOP► (MOT = 0, the same I²C address, Length = 3 bytes, indicating I²C STOP to DP Rx after 3 bytes of Write)		
7			Wait up to 300µs	Data0►ACK◄ Data1►ACK◄ Data2►ACK◄
8			SYNC◄0000|0000◄ 0000|0011◄ STOP◄ (I²C ACK/AUX ACK, three bytes written to I²C slave)	Data3►ACK◄ STOP► (DP Rx gets ACK to Data3 write while sending AUX Reply to DP Tx)
9		SYNC►0010|0000► 00000000►0|1001000► STOP► (Status Update Request with MOT = 0 and the same I²C address)		
10			SYNC◄0000|0000◄ STOP◄ (I²C ACK/AUX ACK, indicating DP Tx of the completion of the three byte Write to I²C Slave in Sink)	

2.4.5.3 I²C Read transaction

In this section, the mapping of an I²C read transaction onto AUX CH transaction(s) is described using two examples in which first example two bytes and in the second example 10 bytes are read. An I²C master in the Source Device will initiate an I²C read transaction to an I²C slave in the Sink Device via the AUX CH between DP Tx (in the Source) and DP Rx (in the Sink).

In the examples shown in this section the I²C Slave in the Sink Device acknowledges the I²C Read. When the I²C slave non-acknowledges the I²C Read (I²C address not supported), what corrective action to take is up to the I²C Master in the Source Device and beyond the scope of the DisplayPort Specification

Example 1: I²C Read of Two Data Bytes

START►1001000|1►ACK◄Data0◄ACK►Data1◄NACK►STOP►

- I²C Read Mapping Method 1

In method 1, the I^2C address byte transfer, and each data byte read are mapped into separate AUX transactions. In the example shown in Table 2-49, the bit rate of the I^2C bus in the Sink Device is set to 100kHz (= 10μs per bit). At this bit rate, the I^2C slave in the Sink Device can send each byte within the 300μs of Response Time-out period.

Table 2-49: I^2C Read Transaction Method 1

	I^2C transaction in Source Device	**AUX Request Transaction by DP Tx**	**AUX Reply Transaction by DP Rx**	**I^2C Transaction in Sink Device**
1	START► 1001000|1► (I^2C read with I^2C address = 1001000; I^2C Clock stretched by DP Tx before ACK)			
2		SYNC►0101|0000► 00000000►0|1001000► STOP► (Address-only I^2C read with MOT = 1 and I^2C address = 100100)		
3			Wait up to 300μs	START► 1001000|1► ACK◄
4			SYNC◄0000|0000◄ STOP◄ (I^2C ACK / AUX ACK, I^2C address is acknowledged)	
5	ACK◄ (I^2C clock stretched by DP Tx after ACK)			
6		SYNC►0101|0000► 00000000►0|1001000► 0000|0000►STOP► (I^2C read with MOT = 1, the same I^2C address, and Length = 1 byte)		
7			Wait up to 300μs	Data0◄
8			SYNC◄0000|0000◄ Data0◄ STOP◄ (I^2C ACK / AUX ACK, sends Data0)	
9	Data0◄ACK► (I^2C clock stretched by DP Tx after ACK)			
10		SYNC►0101|0000► 00000000►0|1001000► 0000|0000►STOP► (I^2C read with MOT = 1, the same I^2C address, and Length = 1 byte)		
11				ACK►Data1◄

	I²C transaction in Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in Sink Device
12			SYNC◄0000|0000◄ Data1◄ STOP◄ (I²C ACK / AUX ACK, sends Data1)	
13	Data1◄NACK► STOP►			
14		SYNC►0001|0000► 00000000►0|1001000► STOP► (Address-only I²C read with MOT = 0 and the same I²C address, indicating the I²C STOP to DP Rx)		
15			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	NACK►STOP►

I²C Read Example 2

START►1001000|1►ACK◄Data0◄ACK►Data1◄ACK►Data2◄ACK► Data3◄ACK►

Data4◄ACK► Data5◄ACK► Data6◄ACK► Data7◄ACK► Data8◄ACK►

Data9◄NACK►STOP►

- I²C Read Mapping Method 2

In Method 2, DP Tx pre-fetches read data from the I²C slave in the Sink Device via the DP Rx in order to speed up the read operation. As is the case of the previous example, the bit rate of the I²C bus in the Sink Device is set to 100kHz (= 10µs per bit). At this bit rate, the I²C slave in the Sink Device can send back up to three bytes within the 300µs of Response Time-out period.

Table 2-50: I²C Read Transaction Example 2

	I²C transaction in Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in Sink Device
1	START► 1001000|1► (I²C read with I²C address = 1001000; I²C clock stretched by DP Tx before ACK)			
2		SYNC►0101|0000► 00000000►0|1001000► 0000|1111►STOP► (I²C read with MOT = 1, I²C address = 100100, and Length = 16 bytes)		

	I²C transaction in Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in Sink Device
3			Wait up to 300µs	START► 1001000|1► ACK◄ (DP Rx gets ACK to I²C address and Data0)
4			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK, I²C address is acknowledged, but no data available yet)	
5	ACK◄ (I²C clock stretched by DP Tx after ACK)	SYNC►0101|0000► 00000000►0|1001000► 0000|1111►STOP► (I²C read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data0◄ ACK►
6			Wait up to 300µs	Data1◄ ACK► Data2◄ ACK► Data3◄ ACK►
7			SYNC◄0000|0000◄ Data0◄ Data1◄ Data2◄ Data3◄STOP◄ (I²C ACK / AUX ACK, sends Data0 to Data 3)	
8	Data0◄ACK►	SYNC►0101|0000► 00000000►0|1001000► 0000|1111►STOP► (I²C Read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data4◄ ACK►
9	Data1◄ACK► Data2◄ACK►		Wait up to 300µs	Data5◄ ACK► Data6◄ ACK► Data7◄ ACK►
10	Data3◄ACK► (I²C clock stretched by DP Tx after the last ACK as needed)		SYNC◄0000|0000◄ Data4◄ Data5◄ Data6◄ Data7◄ ◄STOP◄ (I²C ACK / AUX ACK, sends Data4 to Data7)	
11	Data4◄ACK►	SYNC►0101|0000► 00000000►0|1001000► 0000|1111►STOP► (I²C Read with MOT = 1, the same I²C address, and Length = 16 bytes)		Data8◄ ACK►
12	Data5◄ACK► Data6◄ACK►		Wait up to 300µs	Data9◄ ACK► Data10◄ ACK► Data11◄ ACK►

	I²C transaction in Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in Sink Device
13	Data7◄ACK► (I²C clock stretched by DP Tx after the last ACK as needed)		SYNC◄0000|0000◄ Data8◄ Data9◄ Data10◄ Data11◄ ◄STOP◄ (I²C ACK / AUX ACK, sends Data8 to Data11)	
14	Data8◄ACK►	SYNC►0001|0000► 00000000►0|1001000► STOP► (Address-only I²C read with MOT = 0 and the same I²C address, indicating the I²C STOP to DP Rx)		Data12◄ ACK►
15	Data9◄NACK► STOP►		Wait up to 300µs	Data13◄ ACK► Data14◄ ACK► Data15◄ ACK►
16			SYNC◄0000|0000◄ Data12◄ Data13◄ Data14◄ Data15◄◄STOP◄ (I²C ACK / AUX ACK, sends Data12 to Data15)	
17		SYNC►0001|0000► 00000000►0|1001000► STOP► (Address-only I²C read with MOT = 0 and the same I²C address, indicating the I²C STOP to DP Rx)		Data16◄ACK►
18			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	Data17◄NACK► STOP►

2.4.5.4 I²C Write followed by I²C Read

When the I²C write is followed by anI²C Read via Repeated Start condition as defined in the I²C Specification, the MOT bit of the Request Command field must stay = 1 while the transaction switches from I²C write to I²C read. Upon detecting this condition, the DP Rx must generate an I²C Repeated Start condition and switch from I²C write to I²C read.

In this section, the mapping of an I²C write transaction followed by an I²C Read transaction onto AUX CH transactions is described using an example in which one data byte is written to set an address offset within a 256 byte I²C data block and two data bytes are read.

The I²C Write Mapping Method 1 and the I²C Read Mapping Method 1 are used in this example. The DP Tx may use other methods as described in the previous sections.

In the following description, the I²C slave in the Sink Device acknowledges the I²C transaction. In case the I²C slave non-acknowledges it, what corrective action to take is up to the I²C master in the Source Device and beyond the scope of the DisplayPort Specification.

Example of I²C write followed by I²C read

START►1001000|0►ACK◄Data0►ACK◄ REPEATED_START►1001000|1►ACK◄Data0'◄ ACK► Data1' ◄ NACK► STOP►

Table 2-51: I²C Write Followed by an I²C Read

.	I²C transaction in the Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in the Sink Device
1	START► 1001000|0► (I²C write with I²C address = 1001000; I²C clock stretched by DP Tx before ACK)			
2		SYNC► 0100|0000► 00000000► 0|1001000► STOP► (Address-only transaction, with MOT = 1 and I²C address = 1001000)		
3			Wait up to 300µs	START► 1001000|0►ACK◄
4			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK)	
5	ACK◄Data0► (I²C clock stretched by DP Tx before ACK to Data0)			
6		SYNC►0100|0000► 00000000►0|1001000► 0000|0000►Data0► STOP► (MOT = 1, the same I²C address, Length = 1 byte)		
7			Wait up to 300µs	Data0► ACK◄
8			SYNC◄0000|0000◄STOP◄ (I²C ACK / AUX ACK)	
9	ACK◄ REPEATED_START► 1001000|1► (Switches to I²C read after issuing REPEATED_START condition with the same I²C address. I²C clock stretched by DP Tx before ACK to I²C read address)			

.	I²C transaction in the Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I²C Transaction in the Sink Device
10		SYNC►0101|0000► 00000000►0|1001000► STOP► (Address-only I²C read with MOT = 1 and the same I²C address, indicated I²C REPEATED_START condition to DP Rx)		
11			Wait up to 300µs	REPEATED_START ► 1001000|1► ACK◄
12			SYNC◄0000|0000◄ STOP◄ (I²C ACK / AUX ACK, I²C address is acknowledged)	
13	ACK◄ (I²C clock stretched by DP Tx after ACK)			
14		SYNC►0101|0000► 00000000►0|1001000► 0000|0000►STOP► (I²C read with MOT = 1, the same I²C address, and Length = 1 byte)		
15			Wait up to 300µs	Data0'◄
16			SYNC◄0000|0000◄ Data0'◄ STOP◄ (I²C ACK / AUX ACK, sends Data0')	
17	Data0'◄ACK► (I²C clock stretched by DP Tx after ACK)			
18		SYNC►0101|0000► 00000000►0|1001000► 0000|0000►STOP► (I²C read with MOT = 1, the same I²C address, and Length = 1 byte)		
19				ACK►Data1'◄
20			SYNC◄0000|0000◄ Data1'◄ STOP◄ (I²C ACK / AUX ACK, sends Data1')	
21	Data1'◄NACK► STOP►			

.	I^2C transaction in the Source Device	AUX Request Transaction by DP Tx	AUX Reply Transaction by DP Rx	I^2C Transaction in the Sink Device
22		SYNC►0001|0000► 00000000►0|1001000► STOP► (Address-only I^2C read with MOT = 0 and the same I^2C address, indicating the I^2C STOP to DP Rx)		
23			SYNC◄0000|0000◄ STOP◄ (I^2C ACK / AUX ACK)	NACK►STOP►

2.4.6 Conversion of I^2C Transaction to Native AUX CH Transaction *(INFORMATIVE)*

Conversion of an I^2C transaction into a native AUX CH transaction by the DisplayPort transmitter is implementation specific and is beyond the scope of this specification.

In the case of mapping of I^2C transaction over the AUX CH, the translation of I^2C to AUX CH transaction by the DisplayPort transmitter and that of the AUX CH to the I^2C by the DisplayPort receiver must agree with each other. Therefore, the translation mechanism is defined in this specification.

The conversion of an I^2C transaction to a native AUX CH transaction by the DisplayPort transmitter is transparent to the DisplayPort receiver. Whether it is converted from an I^2C transaction or not, the DisplayPort receiver will receive the same native AUX CH transaction. It is for this reason that the conversion of an I^2C transaction into a native AUX CH transaction by the DisplayPort transmitter is beyond the scope of this specification.

2.5 AUX CH Services

This section describes two types of AUX CH services, AUX CH Link Services and AUX CH Device Services. These are the Link Layer services used by "Policy Makers" for link and device management both in the Source Device and the Sink Device.

Whenever the Hot Plug Detect signal is active (the connectors are plugged in and the Sink Device has at least a "trickle" AC power), AUX CH services must be available.

There are two Policy Makers.

- Stream Policy Maker
  - Manages stream
    - Stream transport initialization, and maintenance (More on this subject is covered in the following sections)
    - Uses AUX CH Device Services
    - Gets link information from Link Policy Maker
- Link Policy Maker
  - Manages link
    - Link discovery, initialization, and maintenance
    - Uses AUX CH Link Services

Both Source and Sink Devices must have these two policy makers. Policy Makers may be implemented as operating system, software driver, firmware, or hardware state machine. The choice is implementation specific. In this document, only the semantics of the interface between the Link Layer and Stream Policy Makers is defined: Syntax (i.e., API) is implementation specific, and is not covered in the DisplayPort specification.

2.5.1 Stream Transport Initiation Sequence

The Stream Source Policy Maker, before transport initiation, must take the following actions:

- Read EDID from the Sink Device
- Set stream attributes for Main Stream attribute data and CEA 861-C InfoFrame generation
- Optionally (recommended), get the following information from the Link Policy Maker
  - Link configuration: Total link bandwidth
    - To avoiding oversubscription of the link bandwidth
  - Rx capability: Number and types of ports available in Rx
    - To determine the number and types of streams that may be transported
  - Link status: Synchronized? Excessive error symbols?
    - To make sure that the link is ready for transport

When a stream is ready for transport, the Stream Source Policy Maker must start the transport of isochronous stream along with stream attributes data.

The Stream sink, upon receiving a stable stream, must decode the stream attributes data, and start reconstructing the incoming isochronous stream.

The Stream Source Policy Maker may incorporate the link capability information for the stream source management: A DisplayPort aware Stream Source Policy Maker, for example, may try to limit the stream bandwidth to prevent link bandwidth oversubscription. If a stream is going to oversubscribe the link bandwidth, the Stream Source Policy Maker may inform the stream source. The stream source, upon receiving this notice, may take a corrective action, such as the reduction of image resolution and / or color depth (in bits per pixel).

Though it is desirable, such an interaction between two policy makers is optional. In other words, DisplayPort Link must be implemented to function with a legacy Source Policy Maker that is unaware of DisplayPort.

Diagrams of a typical action flow of the Source Device and the Sink Device upon a Hot Plug Detect event are shown in Figure 2-35**.**

Note: The diagrams an example only. It is not required, for instance, that an EDID read precede a DPCD read.

Also note that Figure 2-35 shows a typical action flow for a consumer detachable, box-to-box DisplayPort connection. When DisplayPort is used for embedded connection, such as from a GPU to a notebook panel TCON within notebook PC, a DPCD read may not be needed. In this embedded configuration, the Source (GPU) may, instead, use pre-set link capability information of the DisplayPort receiver.

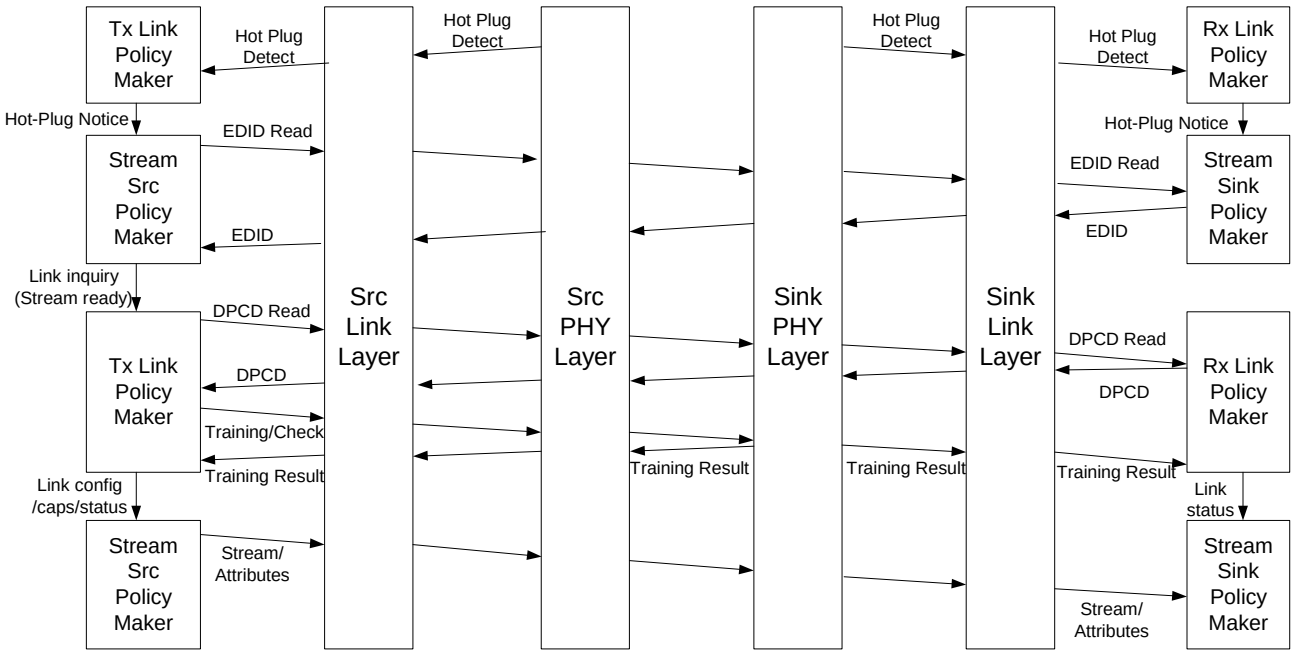


Figure 2-35: Action flow sequences of the Source upon Hot Plug Detect event (INFORMATIVE)

2.5.2 Stream Transport Termination Sequence

Examples of events causing stream termination are:

- A link error event notice by a Link Policy Maker
- A stream timing change
- A stream format change, unstable stream timing or loss of stream

The stream source must terminate the transport of the Main Stream and Secondary data. It may re-initiate the transport following the initiation sequence once the link is re-established. The recommended corrective action for the stream sink is to either display a blank screen, possibly with an alert message, or to turn off the display until stable stream reception is resumed.

2.5.3 AUX CH Link Services

In order to transport isochronous data stream from the Source Device to the Sink Device, the Link Policy Maker must first establish the Main Link. The Main Link must be established in the following sequence of steps.

Note: All the commands are memory mapped, whether setting or getting link parameters..

Step_1:

Unless it has pre-set knowledge, the Source must initiate Link Discovery, by reading the Link Capability field of the DPCD through the AUX CH. The Link Capability field must describe the link capability of the DisplayPort receiver in the Sink Device, such as the Main Link maximum bit rate and maximum number of lanes. Details on reading the DPCD are explained later in this section.

Step_2:

Based on the DPCD information, the Source must start the Link Initialization process. The following sequences must take place during Link Initialization:

- The Link Policy Maker in the Source Device must start Link Training. This function call notifies the Sink of the ensuing transport of the training pattern through the Main Link PHY layer, with link configuration and training attributes defined in this function.
- The Link Policy Maker of the Source Device must check the training status and report of final results to the Stream Policy Maker.

If the Link Policy Maker detects a failed Link Training attempt, it must take corrective action. Possible correction actions are:

- Reduction of the bit rate if the link was in the high bit rate mode,
- Termination of Link Initialization

This loop of setting the Main Link configuration and forwarding training pattern, while checking the status must end with the final result of either pass or fail. “Pass” means that the bit lock and symbol lock have been achieved on each of the configured lanes, and all the lanes are symbol locked with proper inter-lane alignment (with skew of two LS_Clk period between adjacent lanes). Otherwise, it is “fail”.

Step_3:

If a receiver is capable of de-spreading as indicated in the DPCD, then the Source may optionally get the Time Stamp N for de-spreading from the Sink, if de-spreading is needed.

After the Main Link is established, the Link Policy Maker of the Source Device must check the link status whenever it detects the HPD (Hot Plug Detect) signal toggle after the rising edge of HPD. The Source Device must ignore low or high pulse period of less than 0.25 ms. In other words, the Source Device must not check the link status until at least 0.25 ms after the rising edge.

The Sink Device must clear the HPD signal to a low level for 0.5 ms to 1 ms before setting it high again whenever there is a status change either in the link or in the device. This will notify the Source Device of the status change.

The Source Device must check the Link Status field of the DPCD through an AUX CH read transaction to identify the cause within 100 ms of the rising edge of the HPD. Upon identifying the cause, the Link Policy Maker must take corrective action.

Note (INFORMATIVE): In case the HPD signal toggling (or bouncing) is the result of the Hot Unplug followed by Hot Plug of a cable-connector assembly, then the HPD signal is likely to remain unstable during the debouncing period, which is in the order of tens of ms. The Source Device may either check the stability of the HPD signal before initiating an AUX CH read transaction or immediately initiate the AUX CH read transaction after each HPD rising edge.

2.5.3.1 Address Mapping for Link Configuration/Management

Table 2-52 shows the DisplayPort address mapping for the DPCD. The DPCD is byte addressed.

Table 2-52: Address Mapping for the DPCD (DisplayPort Configuration Data)

DisplayPort Address	Definition	Read / Write over AUX CH
	Receiver Capability Field	
00000h	DPCD_REV : DPCD revision number Bits 3:0 = Minor revision number Bits 7:4 = Major revision number 10h for DPCD Rev.1.0 11h for DPCD Rev.1.1 **Note:** The DPCD revision number does not necessarily match the DisplayPort version number.	Read Only
00001h	MAX_LINK_RATE : Maximum link rate of Main Link lanes = Value x 0.27 Gbps per lane Bits 7:0 = MAX_LINK_RATE For DisplayPort Ver.1.1, only two values are supported. All other values are reserved. 06h = 1.62Gbps per lane 0Ah = 2.7Gbps per lane A Branch Device must return the lowest common denominator of its own value and the downstream link value.	Read Only
00002h	MAX_LANE_COUNT : Maximum number of lanes = Value Bits 4:0 = MAX_LANE_COUNT For Rev.1.1, only the following three values are supported. All other values are reserved. 1h = One lane 2h = Two lanes 4h = Four lanes For one-lane configuration, Lane0 is used. For 2-lane configuration, Lane0 and Lane1 are used. A Branch Device must return the lowest common denominator of its own value and the downstream link value of Bits 4:0. For DPCD Rev.1.0 Bits 7:5 = RESERVED. Read all 0's. For DPCD Rev.1.1 Bits 6:5 = RESERVED. Read all 0's. Bit 7 = ENHANCED_FRAME_CAP 0 = Enhanced Framing symbol sequence for BS, SR, CPBS, and CPSR is not supported. 1 = Enhanced Framing symbol sequence for BS, SR, CPBS, and CPSR is supported as described in Section 2.2.1.2	Read Only

00003h	MAX_DOWNSPREAD • For DPCD Rev.1.0 Bit 0 = MAX_DOWNSPREAD 0 = No down spread 1 = 0.5% down spread Bits 7:1 = RESERVED. Read all 0's. • For DPCD Rev.1.1 Bit 0 = MAX_DOWNSPREAD 1 = 0.5% down spread Support of 0.5% down-spread is required for DisplayPort Specification Version 1.1 Sink. Therefore, this bit must be 1. Bit 5:1 = RESERVED. Read all 0's. Bit 6 = NO_AUX_HANDSHAKE_LINK_TRAINING 0 = Requires AUX CH handshake to synchronize to DisplayPort transmitter 1 = Does not require AUX CH handshake when the link configuration is already known. DisplayPort transmitter, when it activates its Main Link, may transmit Link Training Patterns 1 and 2 for the minimum of 500μs each. The known-good drive current and pre-emphasis level (or those used in the last "full" link training with AUX CH handshake) must be used when the link training is performed without AUX CH handshake. Whether Bit 6 is 0 or 1, DisplayPort Sink Device must send IRQ_HPD pulse when it cannot synchronize to the incoming stream. For those embedded implementations where there is no HPD line, either the proper operation should be guaranteed by design or the Source Device may periodically poll the link status. Bit 7 = RESERVED. Read 0.	Read Only
00004h	NORP Bit 0 = NORP : Number of Receiver Ports = Value For DisplayPort Ver.1.0, the maximum number is two, one for an uncompressed video stream and the other for its associated audio stream. The receiver can simultaneously receive up to "NORP" isochronous streams. The smallest available Receiver Port number is assigned. For example, when there is only one receiver port, the receiver port is assigned to ReceiverPort0. ReceiverPort1 shall be assigned only after Receiver Port 0 has already been assigned. Bits 7:1 = RESERVED. Read all 0's.	Read Only

00005h	DOWNSTREAMPORT_PRESENT Bit 0 = DWN_STRM_PORT_PRESENT Set to 1 when this device has downstream port(s) This bit must be set to 1 only in a Branch Device. Bits 2:1 = DWN_STRM_PORT_TYPE Indicates the downstream port type of Downstream Port 0 00 = DisplayPort 01 = Analog VGA or analog video over DVI-I 10 = DVI or HDMI 11 = Others (This downstream port type will have no EDID in the Sink Device: For example, composite video and Svideo ports) A Branch Device must provide more detailed downstream enumeration data on all of its downstream ports including Downstream Port 0 at address 00080h and above. For DPCD Ver.1.0 Bits7:3 = RESERVED. Read all 0's. For DPCD Ver.1.1 Bit3 = FORMAT_CONVERSION 0 = This Branch Device does not have a format conversion block 1 = This downstream port has a format conversion block **Note**: Applicable to a Branch Device only. Bits 7:4 = RESERVED. Read all 0's.	Read Only
00006h	MAIN_LINK_CHANNEL_CODING Bit 0 = ANSI 8B/10B This bit set to 1 when DisplayPort receiver supports the Main Link channel coding specification as specified in ANSI X3.230-1994, clause 11. Bits 7:1: RESERVED. Read all 0's.	
00007h	For DPCD Ver.1.0 Reserved. Read all 0's. For DPCD Ver.1.1 DOWN_STREAM_PORT_COUNT : Value = The number of downstream ports. 0 when there is no downstream port. Type and capability of the downstream port are enumerated at address 00080h and above. Bits 3:0 = DWN_STRM_PORT_COUNT Bits 6:4 = RESERVED. Read all 0's. Bit 7 = OUI Support 0 = OUI not supported 1 = OUI supported 00400h to 00402h for a Sink Device 00500h to 00502h for a Source Device	Reads all 0's

00008h	RECEIVE_PORT0_CAP_0 ReceiverPort0 Capability_0 Bit 0 = RESERVED. Read 0 Bit 1 = LOCAL_EDID_PRESENT 1 = This receiver port has a local EDID. 0 = This receiver port has no local EDID. "Sink Device" and "Format Converter" must have a local EDID. Bit 2 = ASSOCIATED_TO_PRECEDING_PORT 1 = This port is used for secondary isochronous stream of main stream received in the preceding port 0 = This port is used for main isochronous stream. This bit must always be zero for Receiver Port 0. Bits 7:3 = RESERVED. Read all 0's. For Receiver Port0, this bit 3 must be 0.	Read Only
00009h	RECEIVE_PORT0_CAP_1 ReceiverPort0 Capability_1 Bits 7:0 = BUFFER_SIZE Buffer size = (Value+1) * 32 bytes per lane The maximum is 8 Kbytes per lane.	Read Only
0000Ah	RECEIVE_PORT1_CAP_0 ReceiverPort1 Capability_0 Bit definition is identical to that of RECEIVE_PORT0_CAP_0. **Note**: When Receiver Port 1 not present, reads all 0's.	Read Only
0000Bh	RECEIVE_PORT1_CAP_1 ReceiverPort1 Capability_1 Bit definition is identical to that of RECEIVE_PORT0_CAP_1. **Note**: When Receiver Port 1 not present, reads all 0's.	Read Only
0000Ch - 0007Fh	RESERVED	Reads all 0's

00080h - 0008Fh	For DPCD Ver.1.0: RESERVED. Read all 0's. For DPCD Ver.1.1: 1 byte per downstream port DWN_STRM_PORT0_CAP (x = Downstream Port number. The Port_x capability is stored at address of the Downstream Port number plus 80h.) Bits 2:0 = DWN_STRM_PORT0_TYPE 000 = DisplayPort 001 = Analog VGA 010 = DVI 011 = HDMI 100 = Others without EDID support 101 – 111 = RESERVED Bit 3 = DWN_STRM_PORT0_HPD 0 = Downstream port is not HPD aware 1 = Downstream port is HPD aware Bits 7:4 = RESERVED. Read all 0's. **Note 1**: A Source Device may detect the interface type of the Sink Device by reading the Video Input Definition byte of EDID. **Note 2**: Some interfaces may not have a built-in HPD support, but a Branch Device may have its own HPD method. In that case, Bit 3 must be set to 1. For example, A Branch Device with analog VGA downstream port may periodically read EDID for the purpose of detecting an analog VGA Sink. It should be noted that the support of HPD on the downstream ports is recommended. For example, Windows Logo Program Device Requirements Version 3.01 requires HPD support on all digital display interfaces and strongly recommends it even for analog display interface.	
00090h-000FFh	Reserved for supporting up to 127 downstream devices per Branch Device	Read all 0's

Link Configuration Field		
00100h	LINK_BW_SET : Main Link Bandwidth Setting=Value x 0.27Gbps per lane Bits 7:0 = LINK_BW_SET For DisplayPort version 1, revision 1, only two values are supported. All other values are reserved. 06h = 1.62 Gbps per lane 0Ah = 2.7 Gbps per lane Source may choose either of the two link bandwidth as long as it does not exceed the capability of DisplayPort receiver as indicated in the receiver capability field.	Write / Read
00101h	LANE_COUNT_SET : Main Link Lane Count = Value Bits 4:0 = LANE_COUNT_SET For DisplayPort version 1 revision 1, only the following three values are supported. All other values are reserved. 1h = One lane 2h = Two lanes 4h = Four lanes For one-lane configuration, Lane0 is used. For 2-lane configuration, Lane0 and Lane1 are used. The source may choose any lane count as long as it does not exceed the capability of the DisplayPort receiver as indicated in the receiver capability field. For DPCD Ver.1.0: Bits 7:5 = RESERVED. Read all 0's. For DPCD Ver.1.1: Bits 6:5 = RESERVED. Read all 0's. Bit 7 = ENHANCED_FRAME_EN 0 = Enhanced Framing symbol sequence is not enabled. 1 = Enhanced Framing symbol sequence for BS, SR, CPBS, and CPSR is enabled as described in Section 2.2.1.2.	Write / Read

00102h	TRAINING_PATTERN_SET Bits 1:0 = TRAINING_PATTERN_SET : Link Training Pattern Setting 00 – Training not in progress (or disabled) 01 – Training Pattern 1 10 – Training Pattern 2 11 – RESERVED Bits 3:2 = LINK_QUAL_PATTERN_SET 00 – Link quality test pattern not transmitted 01 – D10.2 test pattern (unscrambled) transmitted (same as Training Pattern 1) 10 – Symbol Error Rate measurement pattern transmitted 11 – PRBS7 transmitted The PRBS7 bit sequence must be: ----- direction ---→ 0010000011000010100 0111100100010110011110101001 1111010000111000100100011011 0101101111011000110100101 11 0111001100101010111111110000 **Note:** Upper left is transmitted first and lower right is transmitted last. Bit 4 = RECOVERED_CLOCK_OUT_EN 0 – Recovered clock output from a test pad of DisplayPort Rx not enabled 1 – Recovered clock output from a test pad of DisplayPort Rx enabled. Bit 5 = SCRAMBLING_DISABLE 0 – DisplayPort transmitter scrambles data symbols before transmission 1 – DisplayPort transmitter disables scrambler and transmits all symbols without scrambling For DPCD Version 1.0: Bits 7:6 = reserved, read as zeros. For DPCD version 1.1 Bits 7:6 = SYMBOL ERROR COUNT SEL 00: Disparity error and Illegal Symbol error 01: Disparity error 10: Illegal symbol error 11: Reserved	Write / Read

00103h	TRAINING_LANE0_SET : Link Training Control_Lane0 Bits 1:0 = VOLTAGE SWING SET 00 – Training Pattern 1 with voltage swing level 0 01 – Training Pattern 1 with voltage swing level 1 10 – Training Pattern 1 with voltage swing level 2 11 – Training Pattern 1 with voltage swing level 3 Bit 2 = MAX_SWING_REACHED Set to 1 when the maximum driven current setting is reached. The transmitter must support at least three levels of voltage swing ,(400, 600 and 800) mV_diff_pp. If only three levels of voltage swing are supported, then program Bit 2 must be set to 1 when Bits 1:0 are set to 10. Bit 4:3 = PRE-EMPHASIS_SET 00 = Training Pattern 2 without pre-emphasis 01 = Training Pattern 2 with pre-emphasis level 1 10 = Training Pattern 2 with pre-emphasis level 2 11 = Training Pattern 2 with pre-emphasis level 3 Bit 5 = MAX_PRE-EMPHASIS_REACHED Set to 1 when the maximum drive current setting is reached. The Transmitter must support at least two levels of pre-emphasis (3.5dB and 6dB) in addition to no pre-emphasis (0dB). Support of additional pre-emphasis level is optional. If only 0dB, 3.5dB, and 6dB are supported, the transmitter must set bit5 when it sets bits 4:3 to 2h (level2), to indicate to the receiver that the maximum pre-emphasis level has been reached. Support of independent pre-emphasis level control for each lane is also optional. Bits 7:6 = RESERVED. Read all 0's.	Write / Read
00104h	TRAINING_LANE1_SET (Bit definition identical to that of TRAINING_LANE0_SET.)	Write / Read
00105h	TRAINING_LANE2_SET (Bit definition identical to that of TRAINING_LANE0_SET.)	Write / Read
00106h	TRAINING_LANE3_SET (Bit definition identical to that of TRAINING_LANE0_SET.)	Write / Read
00107h	DOWNSPREAD_CTRL : Down-spreading control Bit 0 = MODULATION_FREQ Spread spectrum modulation frequency 0 = 30 kHz 1 = 33 kHz Bit 3:1 = RESERVED. Read all 0's Bits 4 = SPREAD_AMP Spreading amplitude 0 = 0.0% down spread 1 = 0.5% down spread Bit 7:5 = RESERVED. Read all 0's. **Note**: Write 00h to declare to the receiver that there is no down-spreading.	Write / Read
00108h	MAIN_LINK_CHANNEL_CODING_SET Bit 0 = SET_ANSI 8B10B This bit selects the Main Link channel coding specification as specified in ANSI X3.230-1994, clause 11. Bits 7:1 = RESERVED. Read all 0's.	Write / Read
00109h-001FFh	RESERVED	Reads all 0's

Link / Sink Status Field		
00200h	SINK_COUNT : Sink Device count Bits 5:0 = SINK_COUNT Total number of the Sink Devices within this device and those connected to the downstream ports of this device **Note**: Branch Device must add up the Rendering Function counts read from all of its downstream ports. It must add one more if it has a local Rendering Function. Bit 6 = CP_READY Set to 1 when all of the Sink Devices (local Sink and those connected to its downstream ports) are CP-capable. This bit must be set at the conclusion of Content Protection Authentication. **Note**: The Source Device must transmit content that requires content protection only when all the Branch and Sink Devices in the link are CP-ready except for Repeater Devices. (A Repeater Device is not required to perform decryption / encryption operation, and therefore is not required to be CP-ready.) Bits 7 = RESERVED	Read only
00201h	DEVICE_SERVICE_IRQ_VECTOR Bit 0 = RESERVED for REMOTE_CONTROL_COMMAND_PENDING When this bit is set to 1, the Source Device must read the Device Services Field for REMOTE_CONTROL_COMMAND_PASS_THROUGH. Bit 1 = AUTOMATED_TEST_REQUEST When this bit is set to 1, the Source Device must read Addresses 00218h - 0027Fh for the requested link test. Bit 2 = CP_IRQ This bit is used by an optional content protection system. Bits 5:3 = RESERVED. Read all 0's. Bit 6 = SINK_SPECIFIC_IRQ Usage is vendor-specific. Bit 7 = RESERVED. Read 0.	Clearable read only. (Bit is cleared when '1' is written is written via an AUX CH write transaction.
00202h	LANE0_1_STATUS : Lane0 and Lane1 Status Bit 0 = LANE0_CR_DONE Bit 1 = LANE0_CHANNEL_EQ_DONE Bit 2 = LANE0_SYMBOL_LOCKED Bit 3 = RESERVED. Read 0. Bit 4 = LANE1_CR_DONE Bit 5 = LANE1_CHANNEL_EQ_DONE Bit 6 = LANE1_SYMBOL_LOCKED Bit 7 = RESERVED. Read 0.	Read only
00203h	LANE2_3_STATUS (Bit definition identical to that of LANE0_1_STATUS)	Read only

00204h	LANE_ALIGN__STATUS_UPDATED Bit 0 = INTERLANE_ALIGN_DONE Bits 5:1 = RESERVED. Read all 0's. Bit 6 = DOWNSTREAM_PORT_STATUS_CHANGED Bit 6 is set when any of the downstream ports has changed status. Bit 7 = LINK_STATUS_UPDATED Link Status and Adjust Request updated since the last read. Bit 7 is set when updated and cleared after read.	Read only
00205h	SINK_STATUS Bit 0 = RECEIVE_PORT_0_STATUS 0 = SINK out of synchronization 1 = SINK in synchronization Bit 1 = RECEIVE_PORT_1_STATUS 0 = SINK out of synchronization 1 = SINK in synchronization Bits 7:2 = RESERVED. Read all 0's	
00206h	ADJUST_REQUEST_LANE0_1 : Voltage Swing and Equalization Setting Adjust Request for Lane0 and Lane1 Bits 1:0 = VOLTAGE_SWING_LANE0 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3 Bits 3:2 = PRE-EMPHASIS_LANE0 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3 Bits 5:4 = VOLTAGE_SWING_LANE1 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3 Bits 7:6 = PRE-EMPHASIS_LANE1 00 = Level 0 01 = Level 1 10 = Level 2 11 = Level 3	Read only
00207h	ADJUST_REQUEST_LANE2_3 (Bit definitions as in ADJUST_REQUEST_LANE0_1)	Read only
00208h	TRAINING_SCORE_LANE0 Reserved	Read only
00209h	TRAINING_SCORE_LANE1 Reserved	Read only
0020Ah	TRAINING_SCORE_LANE2 Reserved	Read only
0020Bh	TRAINING_SCORE_LANE3 Reserved	Read only

0020Ch - 0020Fh	Reserved	Read all 0's
00210h - 00211h	SYMBOL_ERROR_COUNT_LANE0 : 15-bit value storing the symbol error count of Lane 0 00210h bits 7:0= Error Count Bits 7:0 00211h bits 6:0 = Error Count Bits 14:8 00211h bit 7 = Error count valid Set to 1 when the error count value is valid. For Symbol Error Rate Measurement (repetition of scrambled 00h) Measures the number of mismatched symbols. For PRBS7 pattern Measures the number of bit errors. Unless otherwise specified the above addresses must have ANSI 8B/10B decode error count. The 15 bit value is cleared upon an AUX CH read by the transmitter. When the symbol error count exceeds 2^{15} (= 32,768), the value must be kept at 2^{15}, instead of wrapping around..	Read only
00212h - 00213h	SYMBOL_ERROR_COUNT_LANE1 : 15-bit value storing the symbol error count of Lane 1 00212h bits7:0= Error Count Bits7:0 00213h bits6:0 = Error Count Bits14:8 00213h bit7 = Error count valid Set to 1 when the error count value is valid. For Symbol Error Rate Measurement (repetition of scrambled 00h) Measures the number of mismatched symbols. For PRBS7 pattern Measures the number of bit errors. Unless otherwise specified the above addresses must have ANSI 8B/10B decode error count. The 15-bit value is cleared upon an AUX CH read by a transmitter When the symbol error count exceeds 2^{15} (= 32,768), the value must be kept at 2^{15}, instead of wrapping around..	Read only
00214h - 00215h	SYMBOL_ERROR_COUNT_LANE2 15-bit value storing the symbol error count of Lane 2 00214h bits7:0= Error Count Bits7:0 00215h bits6:0 = Error Count Bits14:8 00215h bit7 = Error count valid Set to 1 when the error count value is valid. For Symbol Error Rate Measurement (repetition of scrambled 00h) Measures the number of mismatched symbols. For PRBS7 pattern Measures the number of bit errors. Unless otherwise specified the above addresses must have ANSI 8B/10B decode error count. The 15-bit value is cleared upon an AUX CH read by a transmitter When the symbol error count exceeds 2^{15} (= 32,768), the value must be kept at 2^{15}, instead of wrapping around..	Read only

00216h - 00217h	SYMBOL_ERROR_COUNT_LANE3 15-bit value storing the symbol error count of Lane 3 00216h bits7:0= Error Count Bits7:0 00217h bits6:0 = Error Count Bits14:8 00217h bit7 = Error count valid Set to 1 when the error count value is valid. For Symbol Error Rate Measurement (repetition of scrambled 00h) Measures the number of mismatched symbols. For PRBS7 pattern Measures the number of bit errors. Unless otherwise specified the above addresses must have ANSI 8B/10B decode error count. The 15-bit value is cleared upon an AUX CH read by a transmitter When the symbol error count exceeds 2^{15} (= 32,768), the value must be kept at 2^{15}, instead of wrapping around..	Read only
Automated Testing Sub-Field (00218h to 0027Fh below) is optional		
00218h	TEST_REQUEST : Test requested by the Sink Device. All other values reserved. Bit 0 = TEST_LINK_TRAINING 0 = no link training test requested 1 = link training test requested. See TEST_LINK_RATE and TEST_LANE_COUNT for link rate and link width requested respectively. Bit 1 = TEST_PATTERN 0 = no test pattern requested 1 = test pattern requested Bit 2 = TEST_EDID_READ 0 = no EDID read test requested 1 = EDID read test requested. Checksum of the last EDID block read is written to TEST_EDID_CHECKSUM. The source will also send a color square test pattern. For DPCD version 1.0: Bits 7:3 = RESERVED. Read all 0's. For DPCD version 1.1: Bit 3 = PHY_TEST_PATTERN Set = 1 to request the PHY test pattern as specified at address 00248h. Bits 7:4 = Reserved. Read as zeros.	Read only
00219h	TEST_LINK_RATE Bits 7:0 = TEST_LINK_RATE 06h = 1.62 Gbps 0Ah = 2.7 Gbps	Read only
00220h	TEST_LANE_COUNT Bits 4:0 = TEST_LANE_COUNT 1h = one lane 2h = two lanes 4h = four lanes All other values reserved. Bits 7:5 = RESERVED. Read all 0's.	Read only

00221h	TEST_PATTERN : Test pattern requested by the Sink Device 01h = color ramps 02h = black and white vertical lines 03h = color square	Read only
00222h - 00223h	TEST_H_TOTAL : Horizontal total of transmitted video stream in pixel count 00222h Bits 7:0 = TEST_H_TOTAL Bits 15:8 00223h Bits 7:0 = TEST_H_TOTAL Bits 7:0	Read only
00224h- 00225h	TEST_V_TOTAL : Vertical total of transmitted video stream in line count 00224h Bits 7:0 = TEST_V_TOTAL Bits 15:8 00225h Bits 7:0 = TEST_V_TOTAL Bits 7:0	Read only
00226h - 00227h	TEST_H_START : Horizontal active start from Hsync start in pixel count 00226h Bits 7:0 = TEST_H_START Bits 15:8 00227h Bits 7:0 = TEST_H_START Bits 7:0	Read only
00228h - 00229h	TEST_V_START : Vertical active start from Vsync start in line count 00228h Bits 7:0 = TEST_V_START Bits 15:8 00229h Bits 7:0 = TEST_V_START Bits 7:0	Read only
0022Ah - 0022Bh	TEST_HSYNC : Hsync width in pixel count 0022A Bit 7 = TEST_HSYNC_POLARITY 0022A Bits 6:0 = TEST_HSYNC_WIDTH Bits 14:8 0022B Bits 7:0 = TEST_HSYNC_WIDTH Bits 7:0	Read only
0022Ch - 0022Dh	TEST_VSYNC : Vsync width in line count 0022C Bit 7 = TEST_VSYNC_POLARITY 0022C Bits 6:0 = TEST_VSYNC_WIDTH Bits 14:8 0022D Bits 7:0 = TEST_VSYNC_WIDTH Bits 7:0	Read only
0022Eh - 0022Fh	TEST_H_WIDTH : Active video width in pixel count 0022Eh Bits 7:0 = TEST_H_WIDTH Bits 15:8 0022Fh Bits 7:0 = TEST_H_WIDTH Bits 7:0 E.g. 0x400 = 1024 active	Read only
00230h - 00231h	TEST_V_HEIGHT : Active video height in line count 00230h Bits 7:0 = TEST_V_HEIGHT Bits 15:8 00231h Bits 7:0 = TEST_V_HEIGHT Bits 7:0 E.g. 0x300 = 768 active	Read only

00232h- 00233h	TEST_MISC 00232h Bits 7:0 are the same definition as the miscellaneous field in the main stream attribute data. 00232h Bit 0 = TEST_SYNCHRONOUS_CLOCK 0 = Link clock and stream clock asynchronous 1 = Link clock and stream clock synchronous 00232h Bits 2:1 = TEST_COLOR_FORMAT 00 = RGB 01 = YCbCr 4:2:2 10 = YCbCr 4:4:4 11 = Reserved 00232h Bit 3 = TEST_DYNAMIC_RANGE 0 = VESA range (from 0 to the maximum) 1 = CEA range (as defined in CEA-861C Section 5) 00232h Bit 4 = TEST_YCBCR_COEFFICIENTS 0 = ITU601 1 = ITU709 00232h Bits 7:5 = TEST_BIT_DEPTH Bit depth per color / component 000 = 6 bits 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 16 bits 101, 110, 111 = Reserved 00233h Bit 0 = TEST_REFRESH_DENOMINATOR 0 = 1 1 = 1.001 00233h Bit 1 = TEST_INTERLACED 0 = non-interlaced 1 = interlaced 00233h Bits 7:2 = RESERVED. Read all 0's.	Read only
00234h	TEST_REFRESH_RATE_NUMERATOR : Indicates the refresh rate requested by the Sink Device. E.g. 60 = 60Hz numerator Refresh rate = TEST_REFRESH_RATE_NUMERATOR / TEST_REFRESH_RATE_DENOMINATOR	Read only
00235h – 0023Fh	RESERVED for test automation extensions	Reads all 0's
00240h- 00241h	TEST_CRC_R_Cr : Stores the 16 bit CRC value of the R or Cr component. 00240h bits 7:0 = CRC value bits 7:0 00241h bits 7:0 = CRC value bits 15:8	Read only
00242h - 00243h	TEST_CRC_G_Y : Stores the 16 bit CRC value of the G or Y component. 00242h bits 7:0 = CRC value bits 7:0 00243h bits 7:0 = CRC value bits 15:8	Read only
00244h - 00245h	TEST_CRC_B_Cb : Stores the 16 bit CRC value of the B or Cb component. 00244h bits 7:0 = CRC value bits 7:0 00245h bits 7:0 = CRC value bits 15:8	Read only

0 0246h	TEST_SINK_MISC Bits 3:0 = TEST_CRC_COUNT 4 bit wrap counter which increments each time the TEST_CRC_x_x are updated. Reset to 0 when TEST_SINK bit 0 = 0. Bit 5 = TEST_CRC_SUPPORTED 0 = CRC not supported by Sink Device 1 = CRC supported by Sink Device Bits 7:6 = Reserved	Read only
00247h	RESERVED for test automation extensions	Reads all 0's
00248h	For DPCD version 1.0: Reserved. Read as all zero. For DPCD version 1.1 PHY_TEST_PATTERN Bits 1:0 = PHY_TEST_PATTERN_SEL 00 = No test pattern selected 01 = D10.2 without scrambling 10 = Symbol_Error_Measuremeount_Count 11 = PRBS7 Bits 7:2 = Reserved **Note:** Values at 00206h and 00207h specify the requested voltage swing and pre-emphasis level.	Read only
00249h – 0025Fh	Reserved for test automation extensions.	Reads all 0's
00260h	TEST_RESPONSE Bit 0 = TEST_ACK 0 = writing zero has no effect on TEST_REQ state 1 = positive acknowledgement of TEST_REQ. Clears TEST_REQ interrupt flag and indicates to the sink that the source has started requested test mode. Bit 1 = TEST_NAK 0 = writing zero has no effect on TEST_REQ state 1 = negative acknowledgement of TEST_REQ. Clears TEST_REQ interrupt flag and indicates to sink that source will not start requested test mode. Bit 2 = TEST_EDID_CHECKSUM_WRITE 0 = no write to TEST_EDID_CHECKSUM 1 = EDID checksum has been written to TEST_EDID_CHECKSUM Bits 7:3 = RESERVED. Read all 0's.	Write / Read
00261h	TEST_EDID_CHECKSUM In the TEST_EDID mode, the checksum of the last EDID block that was read is written here.	Write / Read
00262h – 0026Fh	RESERVED for test automation extensions	Read all 0's.

00270h	TEST_SINK Bit 0 = TEST_SINK_START 0 = Stop calculating CRC on the next frame 1 = Start calculating CRC on the next frame Bits 7:1 = RESERVED. Read all 0's. **Note:** The CRC calculation is done on the entire frame. A 16 bit CRC is generated per color component, based on the following polynomial: $f(x) = x^{16} + x^{15} + x^2 + 1$. The CRC calculation is only done on active pixels. The msb is shifted in first. For any color format that is less than 16 bits per component, zero-pad the lsb.	Write / Read
00271h - 0027Fh	RESERVED for test automation extensions	Read all 0's.
00280h - 002FFh	RESERVED	Read all 0's.
Source Device Specific Field		
00300h	SOURCE_IEEE_OUI 7:0 Source vendor 24 bit IEEE OUI	Write / Read
00301h	SOURCE_IEEE_OUI 15:8	Write / Read
00302h	SOURCE_IEEE_OUI 23:16	Write / Read
00303h - 003FFh	RESERVED for Source Device specific usage.	Vendor specific
Sink Device Specific Field		
00400h	SINK_IEEE_OUI 7:0 Sink vendor 24 bit IEEE OUI	Read only
00401h	SINK_IEEE_OUI 15:8	Read only
00402h	SINK_IEEE_OUI 23:16	Read only
00403h - 004FFh	RESERVED for Sink Device specific usage	Vendor specific
Branch Device Specific Field		
00500h	BRANCH_IEEE_OUI 7:0 Branch vendor 24 bit IEEE OUI	Read only
00501h	BRANCH _IEEE_OUI 15:8	Read only
00502h	BRANCH _IEEE_OUI 23:16	Read only
00503h - 005FFh	RESERVED for Branch Device vendor-specific usage	Vendor specific

Sink Control Field		
00600h	For DPCD Ver.1.0: RESERVED. Read all 0's. For DPCD Ver.1.1: SET_POWER Bits 1:0 = SET_POWER_STATE 00 = RESERVED 01 = Set local sink and all downstream sinks to D0 (normal operation mode) 10 = Set local sink and all downstream sinks to D3 (power down mode) 11 = RESERVED A Branch Device must forward this value to its downstream devices. When set to D3 state, a Sink Device may put its AUX CH circuit in a "power saving" state. In this mode the AUX CH circuit may only detect the presence of a differential signal input without replying to an AUX CH request transaction. Upon detecting the presence of a differential signal input, the Sink Device must exit the "power saving" state within 1ms. Bits 7:2 = RESERVED. Read all 0's.	Write / Read
00601h-006FFh	RESERVED	Read all 0's
Usage to be Defined		
00700h - 67FFFh	RESERVED	Read all 0's
68000h - 68FFFh	RESERVED for HDCP specification	
69000h - 6FFFFh	RESERVED	Read all 0's
Usage to be Defined		
70000h - 77FFFh	RESERVED for DPCP specification.	Read only
78000h - 7FFFFh	RESERVED for DPCP specification	Write / Read

2.5.3.2 DPCD in Multi-Hop Topology

DisplayPort link has multiple hops when one or more Sink Devices connect to a Source Device via Branch Device(s). When multiple hops of DisplayPort constitutes either daisy-chain or tree topology, the DPCD of the Branch Device must comprehend the DPCD(s) of its downstream links. An upstream DisplayPort device must check only the DPCD of its immediate downstream device regardless of the link topology.

For behaviors of a Branch Device upon detecting the status change of the downstream ports, refer to Section 5.3.2.1.

2.5.3.2.1 Receiver Capability of Downstream Legacy Link

Generally speaking, a legacy link does not have a link capability field equivalent to that defined for DPCD.

Capabilities vary: Some legacy links can support both audio and video, while others are limited to video only. Supported pixel data rate and color format are also dependent on the type of legacy link and its implementation.

A DisplayPort Source Device, when connected to a legacy Sink Device via a DisplayPort-to-legacy converter, must determine the stream format based solely on the Sink Device capability expressed in the EDID of the legacy Sink Device.

2.5.3.3 Link Initialization through Link Training

DisplayPort link initialization (before transporting a stream) must be performed unless the Source Main Link transmitter and the Sink Main Link receiver are already in synchronization as indicated in the Link Status field. During link initialization AUX CH services must be used to train the link with a desired set of link configuration parameters. For a detailed description of the Link Training sequence, refer to Section 3.5.1.3.

An exception for Link Training requirement exists for embedded DisplayPort connection. When DisplayPort Source Device reads 1 in NO_AUX_HANDSHAKE_LINK_TRAINING bit of DPCD (Bit 6 of Address 3h) of DisplayPort Sink Device, it may transmit Link Training Pattern 1 (which is a repetition of D10.2 symbols without scrambling) and Link Training Pattern 2 before switching to the normal operation without a handshake over the AUX CH.

There is another exception for a box-to-box connection. When DisplayPort Source Device is resuming the transmission, the Source Device may skip the AUX CH handshake for the link training if the following conditions are met:

- The HPD signal has remained asserted.
- The Source Device has read 1 in NO_AUX_HANDSHAKE_LINK_TRAINING bit of DPCD (Bit 6 of Address 3h) after the initial Sink Device detection.

If the above conditions are met, the Source Device may transmit Link Training Pattern 1 and Link Training Pattern 2 (500μs minimum for each) before switching to the normal operation without a handshake over the AUX CH. Whether the Link Training is skipped or not, the DisplayPort Sink Device must send an IRQ_HPD pulse over the HPD signal line when it fails to synchronize to the incoming Main Link stream.

After Link Training is successfully completed (which means that DisplayPort receiver is synchronized to the incoming Main Link data) and before the transport of a main video stream starts, the Source Main Link transmitter must be sending the “idle pattern” consisting of BS symbol set (BS symbol followed by VB-ID with its NoVideoStream_Flag set to 1) inserted every 2^{13} (or 8,192) link symbol

The Source Device must start sending the idle pattern after it has cleared the Training_Pattern byte in the DPCD. The Sink Device, should be ready to receive the “idle pattern” as soon as it updates the link status field of the DPCD to indicate the successful completion of Link Training to the Source Device.

For a closed, embedded connection, the DisplayPort transmitter and receiver may be set to pre-calibrated parameters without going through the full link training sequence. In this mode, the DisplayPort transmitter may start a normal operation following the transmission of the Clock Recovery Pattern with pre-calibrated drive current and pre-emphasis level, as shown with a dotted arrow in Figure 2-36.

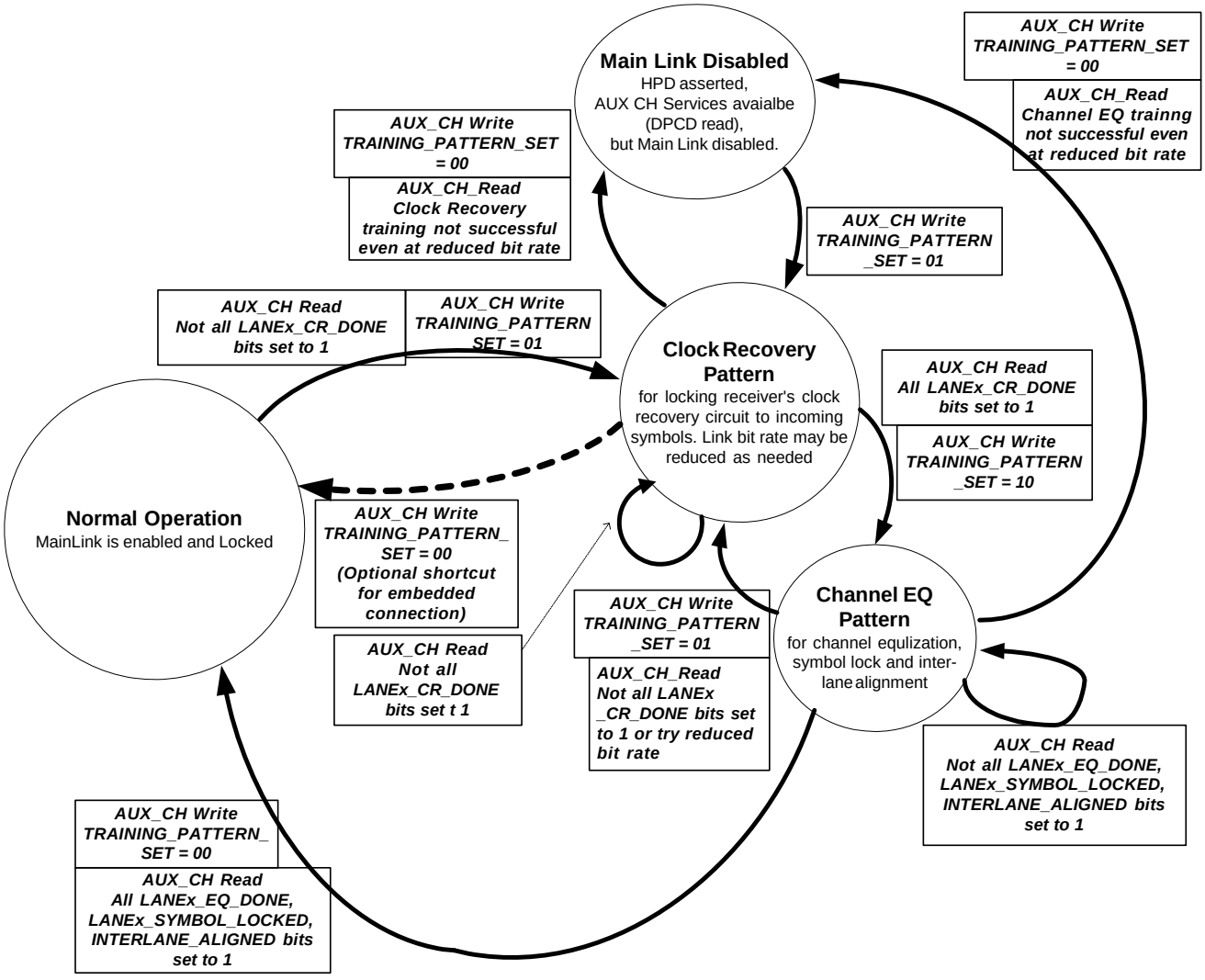


Figure 2-36: Link Training State

2.5.3.4 Link Maintenance

The Link Policy Maker of the Source Device must check the link status whenever it detects the IRQ HPD signal toggle within 100 ms of the rising edge of the HPD for possible Main Link synchronization loss. This check is performed by reading the Link Status field of the DPCD, addresses 00200h → 00205h

Note: The format change in the transported stream does not necessarily result in Link Status change as long as the link stays stable. For example, some Source Devices may choose to continue transmitting stuffing symbols when the stream has stopped. In this case, the Main Link stays synchronized.

2.5.3.5 Link Quality Test Support

DisplayPort supports a test procedure for measuring the link quality. The following features are supported:

- Transmission of a Nyquist pattern (repetition of D10.2 symbols without scrambling)
- Symbol Error measurement pattern

- PRBS7 bit pattern

2.5.3.5.1 Transmission of Nyquist Pattern

This pattern consists of repetition of D10.2 symbols (without scrambling), identical to Training Pattern 1 for Bit-lock. This pattern results in the Main Link toggling at its highest frequency (for example, 1.35 GHz when the link bit rate is 2.7 Gbps). System integrators may use this pattern to measure, for example, the jitter performance of the transmitted signals.

The DisplayPort Source Device signals the transmission of this pattern by writing 01 to bits 3:2 of TRAINING_PATTERN_SET byte.

Upon being notified of the transmission of this pattern, the DisplayPort Sink Device must blank its screen while keeping the DisplayPort receiver running.

2.5.3.5.2 Symbol Error Rate Measurement Pattern

This pattern consists of repetition of data 00h that gets scrambled by a transmitter. (Refer to Section 3.5.1.1 for details of the scrambling polynomial) The DisplayPort Source Device must periodically (every 2^{13} or 8192 symbols) transmit a BS symbol. The Physical Layer must replace every 512^{th} BS symbol with a BR symbol to reset the scrambler.

Upon being notified of the transmission of this pattern, the DisplayPort Sink Device must start increasing the SYMBOL_ERROR_COUNT_LANEx value each time it has unscrambled data value other than 00h.

The DisplayPort Source Device must read the SYMBOL_ERROR_COUNT_LANEx values some time later. Using the read values and elapsed time, it must calculate the approximate symbol error rate.

Transmitting 1E+9 link symbols takes roughly 10 seconds. Therefore, the transmitter is recommended to wait for 10 to 100 seconds before reading the Symbol Error count from a receiver.

Symbol error rate is calculated as follows:

At 2.7 Gbps:

- Symbol Error Rate in units of 10^{-9} = Error_Count / (0.27 * Measurement Period in second)

At 1.62 Gbps:

- Symbol Error Rate in units of 10^{-9} = Error_Count / (0.162 * Measurement Period in second)

2.5.3.5.3 PRBS& Bit Pattern

Refer to address 102h of the DPCD Address Mapping in Table 2-52 for a detailed description of the PRBS7 bit pattern.

2.5.4 AUX CH Device Services

Aux Device Services are used for the purpose of communication between the graphic host and the display device. The following are examples of display device services that are supported by the AUX Channel:

- EDID Support
- MCCS Support
- Sink Event Notification

EDID and MCCS over DDC/CI are supported by mapping I^2C transaction onto DisplayPort to maintain the maximum software transparency.

In addition, the AUX CH is expected to be used for an optional content protection feature.

2.5.4.1 DisplayPort Address Mapping for Device Services

Table 2-53 shows the DisplayPort address mapping for Device Services.

Table 2-53: DisplayPort Address Mapping for Device Services

DisplayPort Address	Definition	W/R over Aux.Ch.
Reserved Field for DPCP		
80000h - 80FFFh	Reserved for DPCP	
Remote Command Pass-through Field		
81000h -81FFFh	Reserved for Remote Command Pass-through	
Reserved		
82000h - FFFFFh	Reserved	Read all 0's

2.5.4.2 E-DDC Support Through I^2C Mapping

The Enhanced Display Data Channel (E-DDC) allows the display to inform the host about its identity and capability using an I^2C bus. E-DCC enables the communication channel to address a larger set of data than the 128-bytes of the base EDID block. E-DDC allows access of up to 32 Kbytes of data based on a segment pointer which allows access to multiple blocks of 256 bytes.

Using the I^2C bus transaction mapping described in Section 2.4.5, E-DDC transactions may be supported over DisplayPort AUX CH as shown below.

2.5.4.3 MCCS over DDC/CI Support through I^2C Mapping

The VESA Monitor Control Command Set Standard (MCCS) provides a set of commands that may be used to control the functions and features of the display.

By using the I^2C bus transaction mapping described in Section 2.4.5, "MCCS transactions over DDC/CI" may be supported over the DisplayPort AUX CH.

This DisplayPort specification does not define a minimum required set of MCCS commands. However, it should be noted that some specifications, including the MCCS standard and operating system logo programs do define minimum sets to be supported.

2.5.4.4 Sink Event Notification

The DisplayPort specification supports a mechanism through which a Sink Device can notify the Source Device of a sink event.

An example of how the sink event notification may be supported is described in Appendix 3.

2.5.4.4.1 Remote Command Pass-through Support

When both the Source and Sink Devices support Remote Command Pass-through as defined in the CEA931-B specification, the Source Device must check the pending command of the Sink Device when it detects that the HPD has toggled and that the cause of the HPD toggle is the pending command of Remote Command Pass-through within 100 ms after the rising edge of HPD signal.

3 Physical Layer

3.1 Introduction

The DisplayPort Physical Layer decouples the data transmission electrical specifications from the DisplayPort Link Layer, thereby allowing modularity for future Link Layer specific design enhancements and also future changes to the transport media type, such as the use of Hybrid Devices. The physical layer is further sub-divided into logical and electrical functional sub-blocks as shown in Figure 3-1.

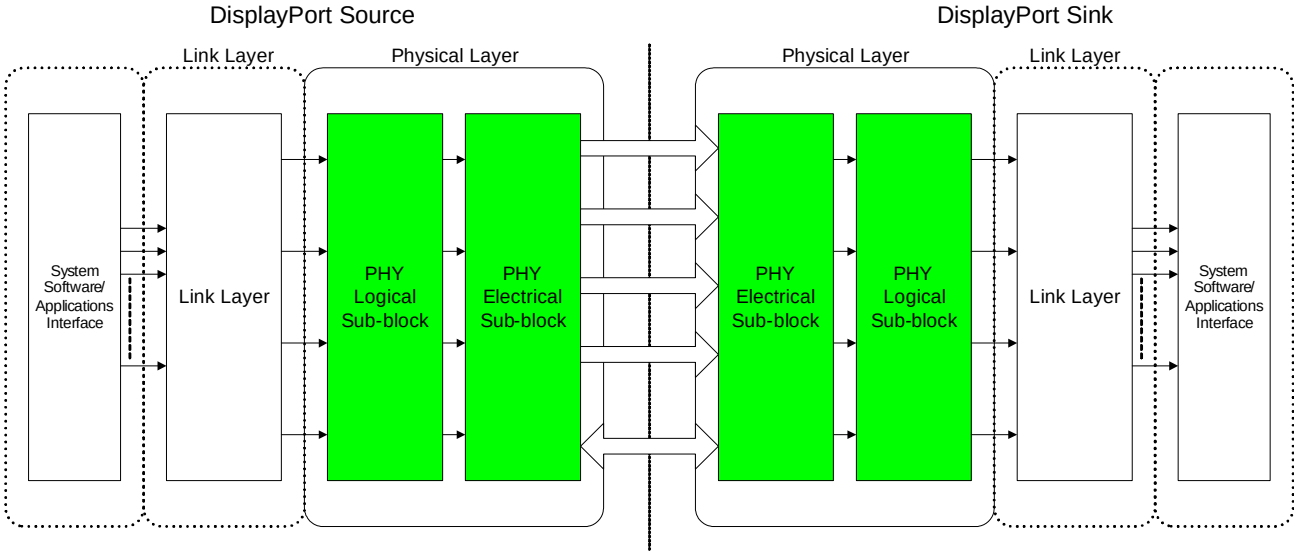


Figure 3-1: DisplayPort Physical Layer

3.1.1 PHY Functions

This section summarizes the functionalities of the DisplayPort Physical Layer.

3.1.1.1 Hot Plug/Unplug Detection Circuitry

The Physical Layer is responsible both for the detection of Hot Plug/Unplug and notification of the Link Layer.

- Logical Sub-block
  - Notifies Hot Plug/Unplug events to the upper layer
- Electrical Sub-block
  - Detects a Hot Plug/Unplug event

3.1.1.2 AUX Channel Circuitry

Physical Layer provides for the half-duplex bi-directional AUX channel for services such as Link Configuration or Maintenance and EDID access.

- Logical Sub-block
  - Generates and detects Start / Stop condition, and locks to the synchronization pattern
  - Encoding and decoding of data using Manchester-II coding: DC-balanced and self-clocked

- Electrical Sub-block
  - Consists of a single differential pair, both ends of the link equipped with driver and receiver for half-duplex bi-directional operation.
    - Driving end
      - Drives a doubly terminated, AC-coupled differential pair in a manner compliant with the AUX channel electrical specification
    - Receiving end
      - Receives the incoming differential signal and extracts the data

3.1.1.3 Main Link Circuitry

The Physical Layer provides the uni-directional Main Link for the transport of isochronous streams and secondary-data packets.

- Logical sub-block
  - Scrambling and de-scrambling
  - ANSI8B10B encoding / decoding
  - Serialization and de-serialization
  - Link Training and Link Status Monitor
    - Adjusts drive current and pre-emphasis level as needed
  - Link Quality Measurement for testability
- Electrical sub-block
  - Consists of up to four differential pairs
  - Transmitter

    Drives doubly terminated, AC-coupled differential pairs in a manner compliant with the Main Link Transmitter electrical specification
  - Receiver

    Receives the incoming differential signals and extract the data with its link CDR (clock-to-data recovery) circuits

3.1.2 Link Layer-PHY Interface Signals

This section summarizes the interface signals between Link Layer and Physical Layer

3.1.2.1 Hot Plug/Unplug Detection

Hot Plug/Unplug Detection circuitry provides for the Hot Plug/Unplug Status signal to Link Layer.

The de-bouncing timer must belong to Link Layer and not the Physical Layer.

3.1.2.2 AUX Channel

The interface signal for the AUX channel between the Link and Physical Layers must consist of an eight bit data signal plus one bit control signal. The control signal is used to indicate Start or Stop of the AUX CH transaction. The use of the one bit control signal to indicate Start / Stop conditions is implementation specific and is not be covered in this specification.

3.1.2.3 Main Link

The interface signal for the Main Link between the Link and Physical Layers consists of an eight bit data signal per Main Link lane plus a one bit control signal. The control signal is used for special symbols such as BS (Blank Start) and BE (Blank End) for framing an isochronous data stream. The use of the one bit control signal is implementation specific and is not covered in this specification.

3.1.3 PHY-Media Interface Signals

This section summarizes the interface signals between the Physical Layer and the Link Media consisting of PCB, connector, and cable. (Connector and cable may be absent for certain link configurations such as a chip-to-chip connection.)

3.1.3.1 DP_PWR / DP_PWR_RETURN

A DisplayPort Source, Sink or locally power Branch Device must provide power on the DP_PWR pin of the box-to-box DisplayPort connector. The power must be used only by a device that is directly connected to a Source, Sink or locally power Branch Device. In other words DP_PWR consumer devices must not be cascaded.

3.1.3.2 Hot Plug / Unplug Detection

One signal (HPD, or Hot Plug Detect) is used to detect a Sink Device (or a downstream device) by the Source Device (or an upstream device). Implementation of HPD is optional for an embedded link configuration. At least a "trickle power" must be present both in the Source and Sink Devices for a Hot Plug event to be detected.

Sink Devices must be ready for an AUX CH transaction whenever they assert (drive high) the HPD signal. Even in power saving mode(s), a Sink Device that keeps its HPD signal asserted must be able to detect the presence of an AUX CH differential signal input. The Sink Device must exit the power saving mode within 1ms of the differential signal being detected.

3.1.3.3 AUX Channel

The AUX Channel consists of one differential pair (AUX-CH+ and AUX-CH-).

At least "trickle power" must be present both in source and sink for the AUX Channel to be functional.

A Sink Device that supports Source Device detection, an optional feature, must monitor the DC voltage of the AUX CH lines between the AC coupling capacitors and the Sink Device.

3.1.3.4 Main Link

The Main Link consists of up to four differential pairs (Main-Link Lane0+, Main-Link Lane0-, Main-Link Lane1+, Main-Link Lane1- …).

Both Source and Sink must be fully powered for the Main Link to be functional.

3.2 DP_PWR for Box-to-Box DisplayPort Connection

DisplayPort connectors for detachable, box-to-box connections have one power pin and one return current pin on the receptacle connector. This power must be provided by the Source, Sink or locally powered Branch Device any time DisplayPort output ports of those devices are enabled. The power must be used only by a device that is directly connected either to a DisplayPort Source, Sink or locally powered Branch. The maximum cascade level of DP_PWR consuming devices is one. The DP_PWR using device may be:

- A cable powered Branch Device
- A Sink Device with a permanently attached cable

A Sink Device with a permanently attached cable may, optionally, provide DP_PWR on the DP_PWR pin of the plug connector. The Sink Device with an attached cable that is capable of providing DP_PWR on the plug connector must verify if a device that uses DP_PWR is connected to the plug connector. The DP_PWR output of a Sink Device with a permanently attached cable may only be enabled after determining the Sink Device has determined that a DP_PWR using device is attached. The method for detection of a DP_PWR using device is described in section 3.2.1.

The voltage on the DP_PWR pin of the source connector must be in the range of 3.0 V to 16.0 V and the DP_PWR pin of the sink connector must be in the range of 3.15 V to 3.45 V. The minimum power available at the DP_PWR pin must be 1.5W regardless of the power supply voltage. A device that consumes more than 1.5W of power must have a means of getting power from an alternate power source.

The DP_PWR and RETURN pins of the box to box connectors must support the maximum current rating of 500 mA.

Table 3-1: DP_PWR Specification for Box-to-Box DisplayPort Connection

Parameter	Minimum	Nominal	Maximum	Unit	Comments
Voltage Range for Source DP_PWR	3.0		16.0	Volt	3.3V – 15.0V nominal range. DC average measurement interval must not exceed 1 second.
Voltage Range for Sink DP_PWR	3.15	3.3	3.45	Volts	
Ripple voltage for SINK DP_PWR (≤ 20 MHz)			1	%	Peak to peak
Noise voltage for SINK DP_PWR (> 20 MHz)			100	mV	Peak to peak
Power Capacity per DP_PWR pin	1.5			Watt	a) Full-height PC add-in card with multiple DisplayPort Source connectors must power at least 3.0W per card b) Half-height PC add-in card with multiple DisplayPort Source connectors must power at least 1.5W per card c) DisplayPort Source connector on a PC motherboard must power 1.5W per connector regardless of the number of connectors on the motherboard.

3.2.1 DP_PWR User Detection Method

Pins 13 and 14 of the box to box receptacle connector of a DisplayPort Source Device that supplies power on the DP_PWR pin must be weakly pulled down with 100 kΩ resistors.

Those two pins of a DisplayPort device with a source function that uses power from DP_PWR must be shorted by a ≤ 100 Ω resistor.

A Sink Device with a permanently attached cable that is capable of supplying power on the DP_PWR pin of the plug connector must verify that pins 13 and 14 are shorted before enabling its DP_PWR output.

3.2.2 DP_PWR Wire

A standard DisplayPort cable must have no wire for the DP_PWR pin.

Only captive cables supplied with cable powered Branch Devices or cables permanently attached to Sink Devices are permitted to have the wire for DP_PWR. These captive / attached cables must have a standard DisplayPort plug connector (as specified in Section 4.2.1) on one end only. The other end must either be permanently attached or have a custom connector.

3.2.3 Inrush Current

Those "cable powered" DisplayPort devices that consume DP_PWR must limit the inrush during hot-plug by controlling the power-on sequence. No more than 20 mJ must be consumed over a 3ms period.

Note: 20 mJ corresponds to an average of 2A from a 3.3V power supply and 0.4A from a 15.0V power supply.

3.2.4 Voltage Droop

DisplayPort Devices that provide power at DP_PWR pin must have sufficient bypass capacitor per DisplayPort connector in order to keep the voltage droop to no more than 10% of the normal DP_PWR supply voltage.

3.2.5 Over Current Protection (OCP)

End user accessible powered connectors must implement OCP for safety and regulatory reasons. Detection of an over-current condition and reporting this condition to the system software is optional and implementation specific.

The preset trip limit must not exceed 3A at the source connector DP_PWR pin and 1.5A at the sink connector DP_PWR pin. Limit must be above allowable current transients to avoid false trips. OCP must be resetable without user mechanical intervention.

A DisplayPort Device with multiple DP_PWR outputs is permitted to use a single OCP to protect all outputs. For devices using a single OCP the preset trip limit must be 3A per device with source connectors and 1.5A per device with sink connectors. There is no requirement to maintain the DP_PWR specification on one port in the presence of a fault condition on another port.

3.3 Hot Plug / Unplug Detect Circuitry

The HPD signal is asserted by the DisplayPort Sink whenever the Sink is connected to either its main power supply or "trickle" power. HPD signal specification is shown in

Parameter	Minimum	Nominal	Maximum	Units	Comments
HPD Voltage	2.25		3.6	Volt	HPD signal to be driven by the Sink Device
Hot Plug Detection Threshold	2.0			Volt	HPD signal to be detected by the Source Device
Hot Unplug Detection Threshold			0.8	Volt	
HPD source termination	100			kΩ	Source Device must pull down its HPD input with a ≥ 100kΩ resistor.
HPD sink termination	100			kΩ	When a Sink Device is off, it must pull down its HPD output with ≥ 100kΩ resistor.
IRQ HPD Pulse Width Driven by Sink	0.5		1.0	ms	Sink generates a low going pulse within this range for IRQ (interrupt request) to the Source
IRQ HPD Pulse Detection Threshold	2.0			ms	When the pulse width is narrower than this threshold, the Source must read the link / sink status field of the DPCD first and take corrective action. When the pulse width is wider than this threshold, it is likely to be actual cable unplug / re-plug event. Upon detecting HPD high, the Source must read the link / sink status field, and if the link is unstable, read the link / sink capability field of the DPCD before initiating Link Training.

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Table 3-2: Hot Plug Detect Signal Specification

Parameter	Minimum	Nominal	Maximum	Units	Comments
HPD Voltage	2.25		3.6	Volt	HPD signal to be driven by the Sink Device
Hot Plug Detection Threshold	2.0			Volt	HPD signal to be detected by the Source Device
Hot Unplug Detection Threshold			0.8	Volt	
HPD source termination	100			kΩ	Source Device must pull down its HPD input with a ≥ 100kΩ resistor.
HPD sink termination	100			kΩ	When a Sink Device is off, it must pull down its HPD output with ≥ 100kΩ resistor.
IRQ HPD Pulse Width Driven by Sink	0.5		1.0	ms	Sink generates a low going pulse within this range for IRQ (interrupt request) to the Source
IRQ HPD Pulse Detection Threshold	2.0			ms	When the pulse width is narrower than this threshold, the Source must read the link / sink status field of the DPCD first and take corrective action. When the pulse width is wider than this threshold, it is likely to be actual cable unplug / re-plug event. Upon detecting HPD high, the Source must read the link / sink status field, and if the link is unstable, read the link / sink capability field of the DPCD before initiating Link Training.

The voltage level of the HPD pin is monitored by the Source Device. TTL levels must be used for the detection.

The Sink Device may detect the presence of the Source Device by monitoring the DC voltage level of the AUX CH lines. As shown in Figure 3-3, the Sink Device with Source detection capability must have AC-coupling capacitors within it. Source detection is an optional feature of a Sink Device.

3.4 AUX Channel

The DisplayPort AUX Channel is a half-duplex, bi-directional channel consisting of one differential pair as shown in Figure 3-2, supporting the bit rate of about 1 Mbps, for all the channel lengths. Note that the 50 Ω termination resistors may be integrated on-chip. The AUX Channel is doubly terminated with 50 Ω termination resistors on both ends, and AC-coupled on the DisplayPort transmitter end.

Figure 3-3 shows how the Sink Device may detect the presence of the source.

The AUX CH uses the Manchester-II code for the self-clocked transmission of signals as shown below in Figure 3-4.

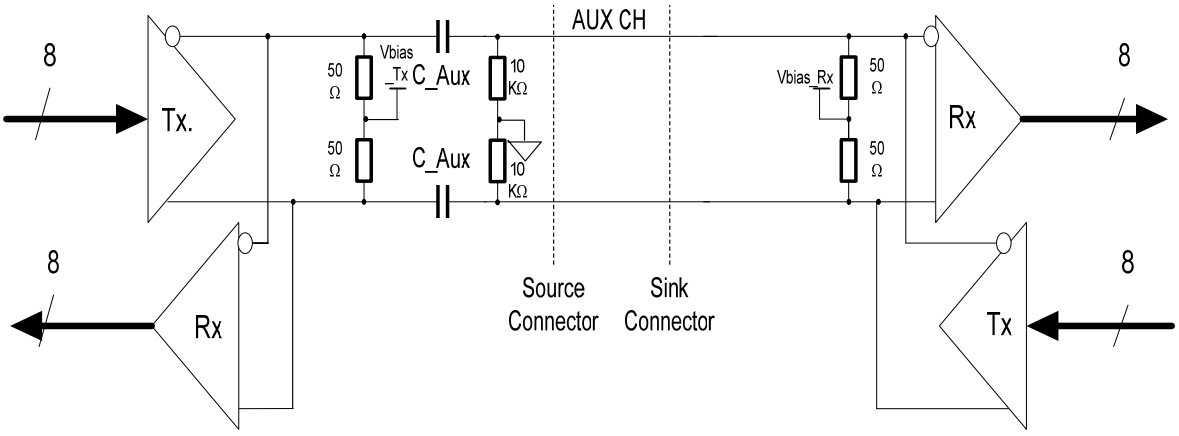


Figure 3-2: AUX CH Differential Pair

The DisplayPort Source Device must weakly pull up the AUX CH lines between the AC-coupling capacitors and the Source Connector to assist source detection by the Sink Device.

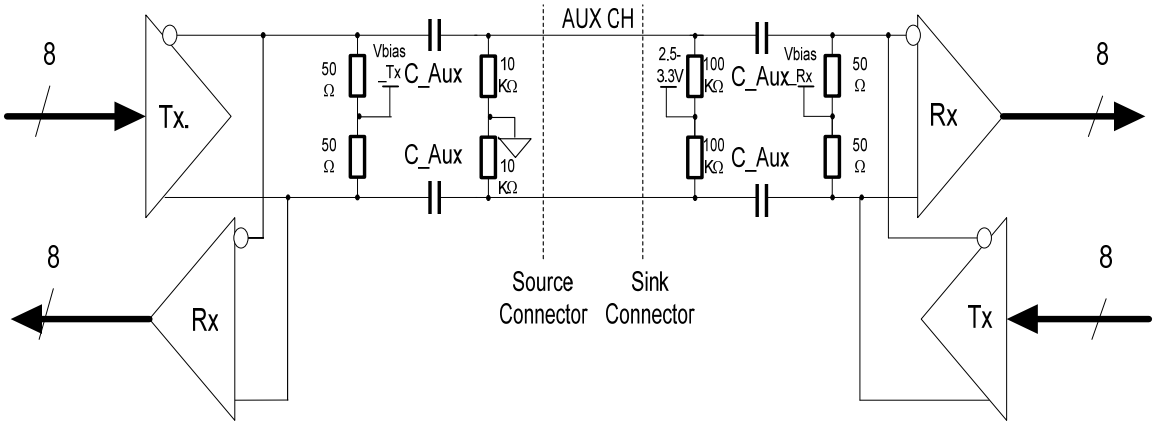


Figure 3-3: AUX CH Lines with Source Detection Monitor

Source detection capable Sink Device must have ac-coupling capacitors. The Sink Device must pull down the AUX CH lines with 1MΩ resistors between the sink connector and the ac-coupling capacitors, and monitor the DC voltage of AUX CH line as shown in Figure 3-3.

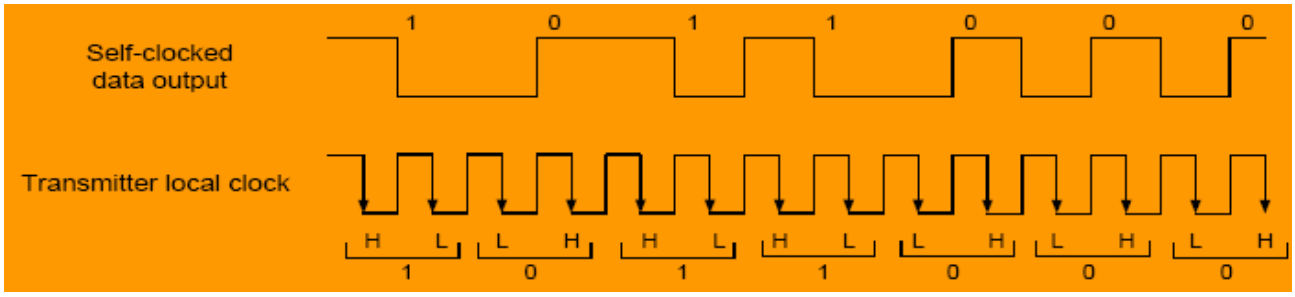


Figure 3-4: Self-clocking with Manchester II coding

3.4.1 AUX Channel Logical Sub-Block

Between transactions, the AUX Channel is in an electrical idle state. In the electrical idle state, neither device is driving the channel and, thus, both AUX-CH+ and AUX-CH- are at the termination voltage.

AUX Channel transactions are initiated by the DisplayPort transmitter which acts as an AUX CH requester. The DisplayPort transmitter, which is the driving end for a request transaction, pre-charges the AUX-CH+ and AUX-CH- to a common mode voltage by transmitting 10 to 16 consecutive 0's in Manchester II code.

After the active pre-charge, the transmitter sends an AUX Sync pattern. The AUX Sync pattern must be as follows:

- Start with 16 consecutive 0's in Manchester II code, which results in a transition from low to high in the middle of each bit period. Including active pre-charge pulses, there must be 26 to 32 consecutive 0's before the end of the AUX Sync pattern.
- End with the AUX-CH+ driven to high for a two bit period (which is 2 µs when the bit rate is 1Mbps) and low for a two bit period, which is illegal in Manchester II code. The AUX-CH- must be driven to the opposite polarity.

The receiving end, which is the DisplayPort receiver for the request transaction, must lock to this Sync pattern.

Following the Sync pattern, the driving end must send data according to the AUX CH syntax as described Section 2.4. When it has finished sending data, the driving node must assert the STOP condition. The STOP condition must be as follows:

- Drives AUX-CH+ to high and AUX-CH- to low for a two bit period, then AUX-CH+ to low and AUX-CH- to high for a two bit period, which is an illegal sequence for Manchester II
- Releases AUX CH immediately after the STOP condition
- AUX Sync pattern and STOP condition are shown in Figure 3-5.

The DisplayPort receiver, the AUX CH replier, replies to this request transaction. The DisplayPort receiver, now acting as a driving end, must let the bus park for at least 10ns, then pre-charges the bus to the common mode voltage with 10 to 16 pre-charge pulses, and initiates the reply transaction. The Sync pattern and the STOP condition are the same for a request and a reply transaction.

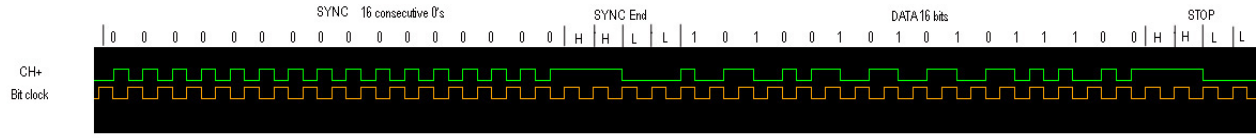


Figure 3-5: AUX CH SYNC Pattern and STOP condition

3.4.2 AUX Channel Electrical Sub-block

Table 3-3 below shows the electrical specification of the DisplayPort AUX Channel.

Table 3-3: DisplayPort AUX Channel Electrical Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	AUX Unit Interval	0.4	0.5	0.6	μs	Results in the bit rate of 1Mbps including the overhead of ManchesterII coding.
Pre-charge pulses	Number of pre-charge pulses	10		16		Each pulse is a '0' in Manchester II code.
$T_{AUX-BUS-PARK}$	AUX CH bus park time	10			ns	Period after the AUX CH STOP condition for which the bus is parked
Tcycle-to-cycle jitter	Cycle-to-cycle jitter at Source Connector pins			0.04	UI	Equal to 24 ns maximum
	Cycle-to-cycle jitter at Receiver Package pins			0.05	UI	Equal to 30 ns maximum
$V_{AUX-DIFFp-p}$	AUX Peak-to-peak Voltage at Source Connector pins	0.34		1.38	V	$V_{AUX-DIFFp-p} = 2*\|V_{AUXP} - V_{AUXM}\|$
	AUX Peak-to-peak Voltage at Receiver Package pins	0.32		1.36	V	
$V_{AUX-DC-CM}$	AUX DC Common Mode Voltage	0		VDD	V	Common mode voltage is equal to Vbias_Tx (or Vbias_Rx) voltage shown in Figure 3-2. VDD is the power supply voltage of AUX CH driver / receiver and 3.6V maximum.
$V_{AUX-TURN-CM}$	AUX turn around common mode voltage			0.4	V	Steady state common mode voltage shift between transmit and receive modes of operation.
I_{AUX_SHORT}	AUX Short Circuit Current Limit			90	mA	Total drive current of the transmitter when it is shorted to its ground.
C_{AUX}	AUX AC Coupling Capacitor	75		200	nF	The AUX CH AC coupling capacitor placed on the DisplayPort Source Device side

3.4.2.1 AC Coupling

The DisplayPort AUX Channel must be AC-coupled. The minimum and maximum values for the capacitance are specified in Table 3-3. The requirement for the inclusion of AC coupling capacitors on the interconnect media is specified at the DisplayPort transmitter. Inclusion of the AC coupling capacitors at the DisplayPort receiver is optional.

3.4.2.2 Termination

The DisplayPort AUX Channel must meet the termination impedance specified in Table 3-3 at all times when the link is active.

3.4.2.3 DC Common Mode Voltage

To facilitate the minimum bus turn around delay, the transmitting side must provide between 10 and 16 Manchester II code '0's. The steady state common mode voltage between transmit and receive modes of operation must not exceed $V_{AUX\text{-}TURN\text{-}CM}$ as specified in Table 3-3.

Source and Sink Devices must be designed to tolerate a power-on, power-off or hot plug event presenting the maximum charge redistribution of 720 nC caused by $V_{AUX\text{-}DC\text{-}CM}$ (3.6V maximum) and C_{AUX} (200 nF maximum) for the maximum period of $T_{AUX\text{-}BUS\text{-}PRECHARGE}$ or greater.

3.4.2.4 Short Circuit Requirements

The driver and receiver circuits of the AUX CH block must survive the worst-case short-circuit current of 90mA (3.6 V over 40 Ω).

3.4.2.5 Differential voltage/timing (EYE) diagram

The AUX CH_EYE mask at the transmitting integrated circuit package pins (informative) is shown in Figure 3-6 and its vertices are shown in Table 3-4.

AUX CH_EYE mask at the connector pins of the transmitting device (normative) and its vertices values are shown in Figure 3-7 and Table 3-5 respectively.

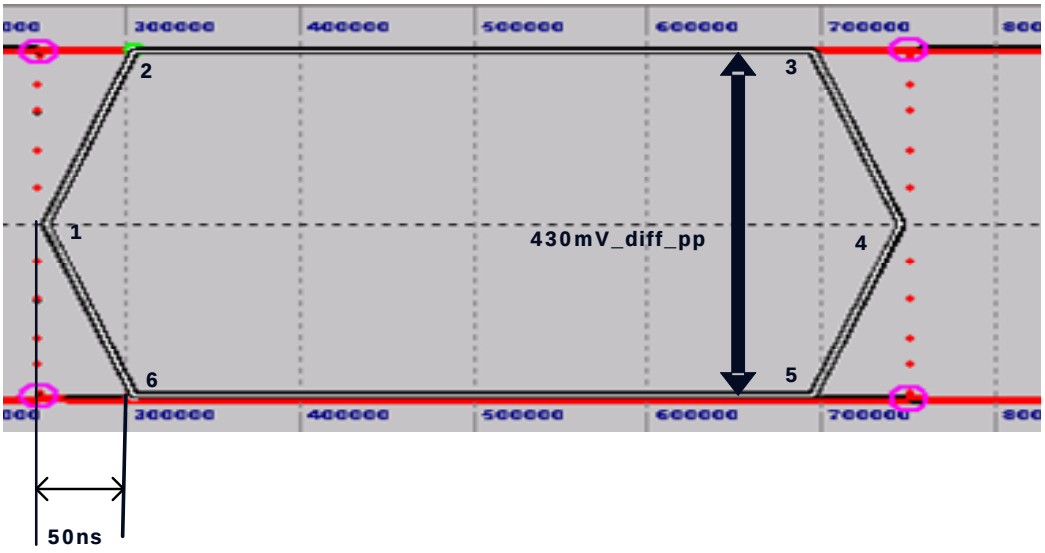


Figure 3-6: AUX CH EYE Mask at Transmitting Integrated Circuit Package Pins (INFORMATIVE)

Table 3-4: Mask Vertices for AUX CH at Transmitting IC Packages Pins (INFORMATIVE)

Point	Time: (UI)	Minimum voltage value at Six Vertices (mV)
1	0.01	0
2	0.11	215
3	0.89	215
4	0.99	- 215
5	0.89	- 215
6	0.11	0

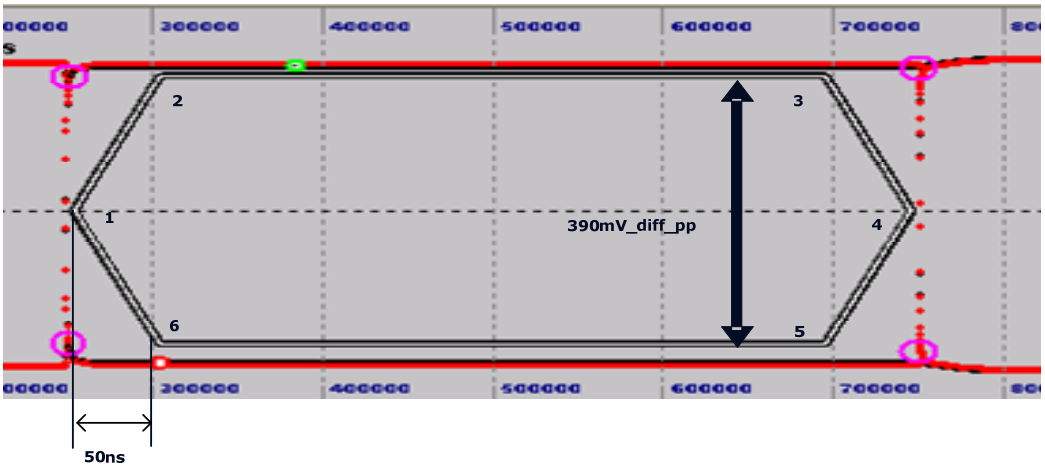


Figure 3-7: AUX CH EYE Mask at Connector Pins of Transmitting Device (NORMATIVE)

Table 3-5: Mask Vertices for AUX CH at Connector Pins of Transmitting Device (NORMATIVE)

Point	Time: (UI)	Minimum voltage value at Six Vertices (mV)
1	0.01	0
2	0.11	195
3	0.89	195
4	0.99	-195
5	0.89	-195
6	0.11	0

AUX CH EYE mask at the connector pins of the receiving device (normative) and its vertices values are shown in Figure 3-8 and Table 3-6, respectively.

AUX CH EYE mask at the receiving IC package pins and its vertices values (informative) are shown in Figure 3-9and

Table 3-7, respectively.

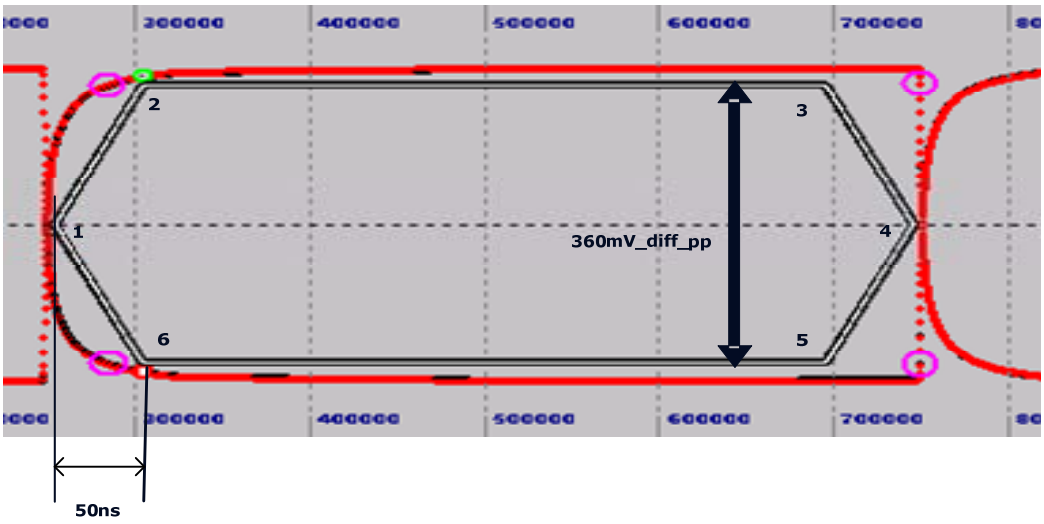


Figure 3-8: AUX CH EYE Mask at Connector Pins of Receiving Device (NORMATIVE)

Table 3-6: Mask Vertices for AUX CH at connector pins of receiving device (NORMATIVE)

Point	Time: (UI)	Minimum voltage value at Six Vertices (mV)
1	0.01	0
2	0.11	180
3	0.89	180
4	0.99	-180
5	0.89	-180
6	0.11	0

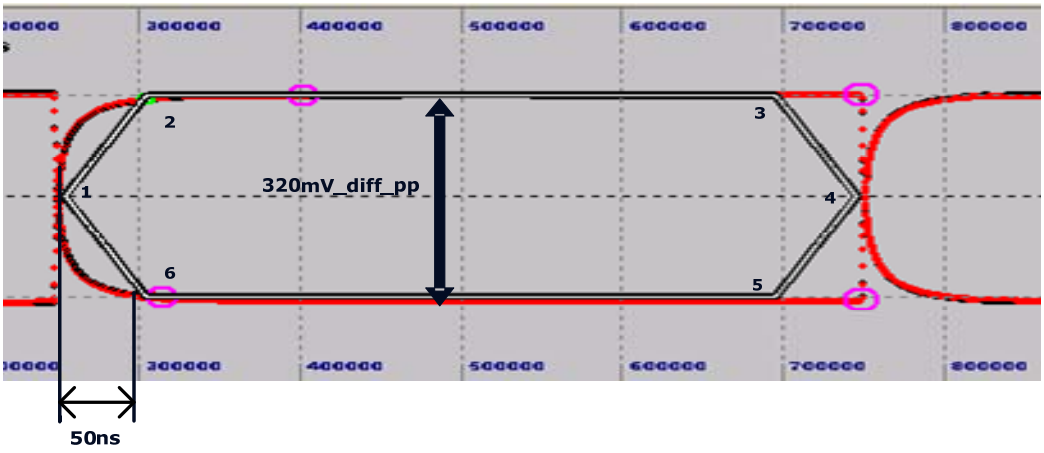


Figure 3-9: AUX CH EYE Mask at Receiving IC Package Pins (INFORMATIVE)

Table 3-7: Mask Vertices for AUX CH at Receiving IC Packages Pins (INFORMATIVE)

Point	Time: (UI)	Minimum voltage value at Six Vertices (mV)
1	0.01	0
2	0.11	160
3	0.89	160
4	0.99	-160
5	0.89	-160
6	0.11	0

3.5 Main Link

This section describes the functions of the DisplayPort Main Link Physical layer.

3.5.1 Main Link Logic Sub-block

The Logical Sub-block of DisplayPort Main Link Physical Layer performs the following functions:

- Scrambling and de-scrambling
- ANSI 8B/10B encoding / decoding
- Serialization and de-serialization
- Link Training and Link Status Monitor
- Drive current and pre-emphasis level control as needed
- Link Quality Measurement (Testability)

3.5.1.1 Scrambling

Scrambling of the Main Link data is performed for EMI reduction prior to ANSI 8B/10B encoding on the transmitter. De-scrambling of the data symbols is performed subsequent to ANSI 8B/10B decoding at the receiver. Utilization of scrambling should result in approximately 7dB reduction in peak spectrum.

Each of the Main Link lanes is scrambled and de-scrambled independently, each with a 16 bit LFSR as follows:

- $G(X) = X^{16} + X^5 + X^4 + X^3 + 1$

The Source Device must replace every 512^{th} BS symbol with a SR symbol. The SR symbol is used to reset the LFSR to FFFFh.

The data scrambling rules must be as follows:

- The LFSR advances on all symbols, both data symbols (D), and special symbols (K).
- Special symbols (K) are not scrambled.
- Data symbols, including “fill data” are scrambled.

Scrambling must be disabled during Link Training and Recovered Link Clock Quality Measurement.

3.5.1.2 Symbol Coding and Serialization/De-serialization

The DisplayPort interface uses the ANSI standard 8B/10B[1] as its channel coding scheme to provide symbol-level DC balancing. It also provides high transition density for link clock phase tracking at the receiver. Using this scheme, 8-bit data characters are treated as three bits and five bits mapped onto a four bit code group and a six bit code group, respectively.

The control bit in conjunction with the data character is used to identify when to encode one of the Special Symbols included in the 8B/10B transmission code.

These code groups are concatenated to form a 10-bit symbol.

As shown in Figure 3-10, ABCDE maps to abcdei and FGH maps to fghj.

After coding, the ANS 8B/10B symbols are serialized so that the least significant bit (lsb) is transported first, and the most significant bit (msb) last.

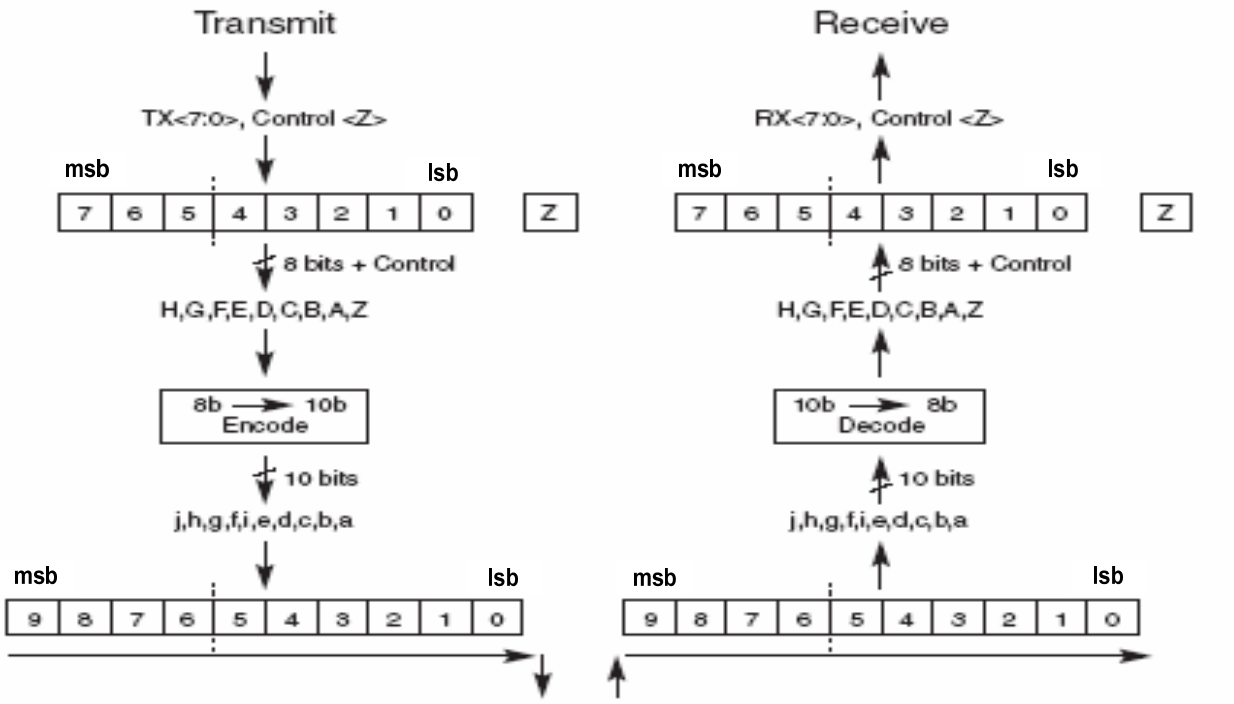


Figure 3-10: Character to Symbol Mapping

3.5.1.2.1 ANSI 8B/10B Special Characters used for DisplayPort Control Symbols

In the DisplayPort Specification, seven control symbols are defined in the Link Layer (refer to Section 2.2.1.1). Table 3-8 shows which ANSI 8B/10B special characters are used for those control symbols. Unused special characters are reserved for future use and must not be used by a DisplayPort compliant link.

[1] The 8B/10B coding scheme is as defined in ANSI X3.230-1994, clause 11 (and also 802.3z, 36.2.4).

Table 3-8: ANSI 8B/10B Special Characters for DisplayPort Control Symbols

Special Character	Symbol	Name
K28.5	BS	Blank Start
K27.7	BE	Blank End
K28.2	SS	Secondary-data Start
K29.7	SE	Secondary-data End
K30.7	FS	Fill Start
K23.7	FE	Fill End
K28.0	SR	Scrambler Reset
K28.1	CPBS	Content Protection BS
K28.3	CPSR	Content Protection SR
K28.4, K28.6, K28.7	Reserved in DisplayPort	

Note1: Refer to Section 2.2.1 for definitions of these control symbols.

3.5.1.3 Link Training

For an open, box-to-box connection, the DisplayPort Source Device configures the link through a link training sequence. One exception is when the DisplayPort Source Device is resuming a transmission. In this condition, the Source Device may skip the AUX CH handshake for the link training as described in Section 2.5.3.3.

For a closed, embedded connection, the DisplayPort transmitter and receiver may be set to pre-calibrated parameters without going through the full link training sequence. In this mode, the DisplayPort Source Device may start a normal operation without the AUX CH handshake for link training, as described in Section 2.5.3.3.

Link training consists of two distinct tasks which must be completed successfully in sequence to establish the link. These are:

- Clock Recovery: This stage locks the receiver CR (clock recovery) PLL to the repetition of D10.2 data symbols. This stage of Link Training determines the drive strength for the link.
- Channel Equalization / Symbol-Lock / Inter-lane Alignment: This stage optimizes the transmitter equalizer (also known as pre-emphasis). The receiver's equalizer (optional) may also be optimized. When successful, the Symbol-Lock and Inter-lane alignment must be achieved by the end of this sequence.

The training sequence is initiated by the Link Policy Maker in the Source Device after detecting a HPD event. When the Source Device detects a HPD low-going pulse that exceeds 2 ms in width, the Link Policy Maker must read the link capability field of the DPCD via the AUX CH. The Link Policy Maker must then, determine the link configuration based on the capability of DisplayPort Receiver and its own needs, write the configuration parameter to the link configuration field of DPCD, and start the Link Training by writing to 01h to the TRAINING_PATTERN_SET byte of the DPCD (DisplayPort Configuration Data) of the DisplayPort receiver via the AUX CH while instructing its transmitter PHY logic sub-layer to start transmitting training patterns.

The Link Policy Maker of the Source Device may choose any link count and link rate as long as they do not exceed the capabilities of the DisplayPort Receiver. Link Training starts when the DisplayPort transmitter writes the link configuration and sets the Link Training Pattern to the Link Configuration Field of the DPCD. Link training is expected to complete within 10 ms. Table 3-9 shows the link training symbol patterns.

Table 3-9: Symbol Patterns of Link Training

Pattern Number	Purpose	Name
1	For locking Clock Recovery Circuit of the DisplayPort receiver	Repetition of D10.2 characters without scrambling
2	For optimizing equalization, determining symbol boundary, and achieving inter-lane alignment	K28.5-, D11.6, K28.5+, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2 without scrambling

The link training sequence, regardless of whether there is an accompanying AUX CH handshake, must always start with negative disparity. Link Training Pattern must start with K28.5-.

The exact bit sequence of K28.5- and K28.5+ (lsb is left most bit and msb is right most bit) is:

- K28.5- : 0011111010
- K28.5+ : 1100000101

For a complete DisplayPort address mapping and definition for DPCD, refer to the DPCD Address Mapping in Table 2-52.

3.5.1.3.1 Clock-Recovery (CR) Sequence

Link training begins with the Clock-Recovery sequence. The link symbols transmitted in this sequence are a repetition of D10.2 data symbols with scrambling disabled. In this sequence, the transmitter must disable pre-emphasis, and start with the minimum differential voltage swing of 0.4 Vdiff_pp.

Note: The transmitter may start with non-minimum differential voltage swing and with pre-emphasis if the optimal setting is already known, for example, as is the case in embedded application.

The transmitter must wait for 100 µs before reading the LANEx_CR_DONE bits of the DPCD which are set by the receiver.

Once it achieves the CR lock, the receiver must set the LANEx_CR_DONE bit for each of (up to) four lanes in the DPCD. Otherwise, the receiver must keep the LANEx_CR_DONE bits cleared and request an increase of the differential voltage swing by updating the value in ADJUST_REQUEST_LANEx_x bytes.

If the receiver keeps the same value in ADJUST_REQUEST_LANEx_x bytes while LANEx_CR_DONE bits remain unset, the transmitter must loop four times with the same voltage swing. On the 5th time, the transmitter shall down-shift to the lower bit rate and must repeat the CR-lock training sequence.

Unless all the LANEx_CR_DONE bits are set, the transmitter must read the ADJUST_REQUEST_LANEx_x, increase the voltage swing according to the request, and update the TRAINING_LANEx_SET bytes to match the new voltage swing setting.

The transmitter must support differential voltage swings of (0.4, 0.6 and 0.8) Vdiff_pp (refer to Section 3.5.3.4).

If the maximum differential voltage swing (0.8 Vdiff_pp) fails to realize the CR lock, the transmitter must down-shift to the lower bit rate (as indicated to the receiver by an AUX CH write to the LINK_BW_SET byte of the DPCD), and repeat the bit-lock training sequence.

Once it reads CR_DONE_LANEx bits set for all lanes, the Link Policy Maker of the transmitter must move on to the next stage, namely, Channel Equalization.

If any of the CR_DONE_LANEx remains unset even at the reduced bit rate after all the voltage swing values have been tried, the transmitter must end the training (by clearing the TRAINING_PATTERN_SET byte to 00h in the DPCD) without establishing the link.

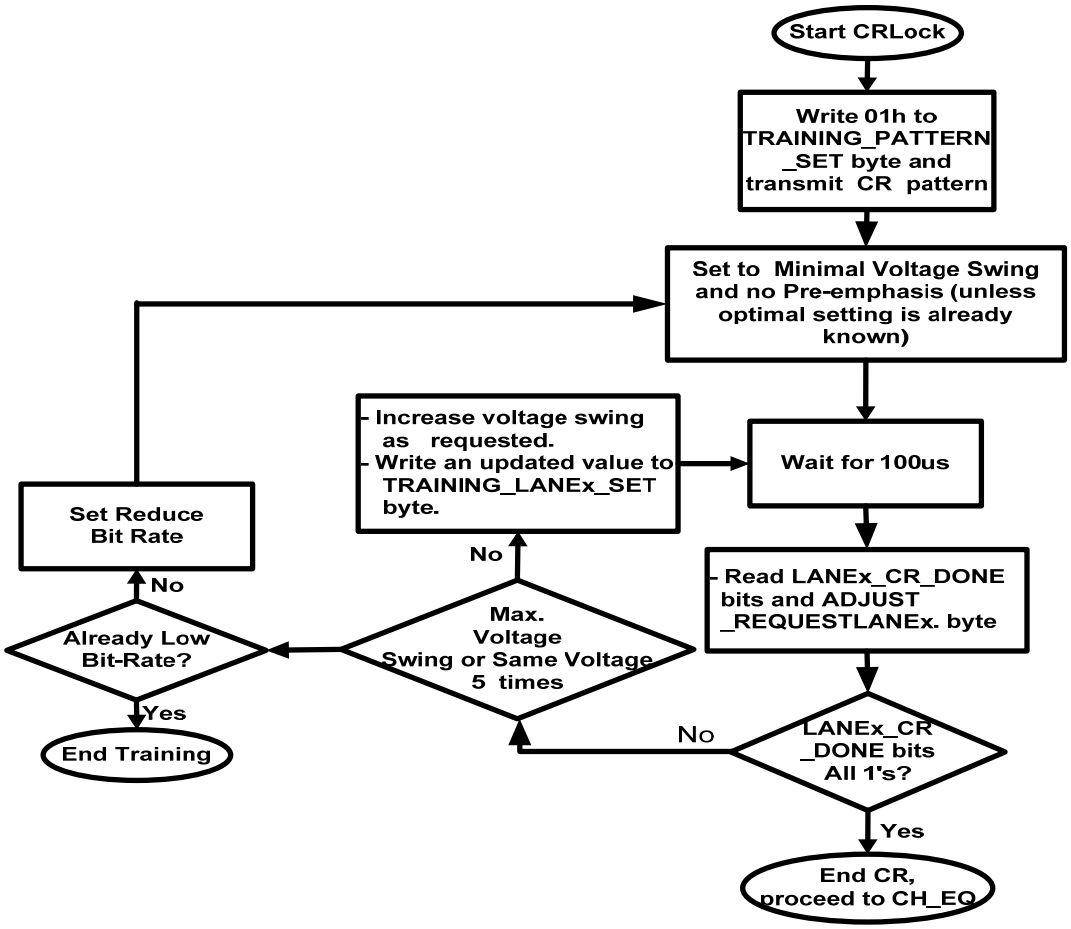


Figure 3-11: Clock Recovery Sequence of Link Training

3.5.1.3.2 Channel Equalization (EQ) Sequence

The Channel Equalization sequence starts with the differential voltage swing (Vdiff_pp) set in the Clock Recovery sequence, with pre-emphasis of the transmitter and equalizer of the receiver (optional) both disabled.

In the Channel Equalization (EQ) sequence, the transmitter writes 02h to the TRAINING_PATTERN_SET byte of DPCD, and transmits the following ten-symbol pattern repetitively, with scrambling disabled.

- K28.5-, D11.6, K28.5+, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2
  - K28.5- : 0011111010
  - K28.5+ : 1100000101

The bits are transported from the left most bit first (lsb) to the right most bit last (msb)

The transmitter must insert two-link-symbol inter-lane skew between adjacent lanes as shown in Figure 2-15.

The receiver must use the recognition of this training pattern to decide whether the channel equalization is successful or not. How to measure the equalization result is implementation specific.

The transmitter must support the pre-emphasis levels of 0 dB (no pre-emphasis), +3.5 dB (1.5x), and +6 dB (2x) as long as the pre-emphasized differential voltage swing (Vdiff_pre in Figure 3-14) does not exceed 1.2V. Support of +9.5 dB (3x) is optional. For example, when the differential voltage swing is set to 0.8V_diff_pp in the CR sequence, the maximum pre-emphasis level is limited to +3.5 dB (Refer to Section 3.5.3.4).

The receiver must indicate success by setting LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCKED, and INTERLANE_ALIGN_DONE bits in the LANEx_x_STATUS / LANE_ALIGNED_STATUS_UPDATED bytes.

The transmitter must read those bytes in the paragraph above and ADJUST_REQUEST_LANEx_x bytes. Unless all status bits are 1, the transmitter must then adjust the pre-emphasis level according to the request by the receiver, and write the new setting to TRAINING_LANEx_SET bytes.

The receiver with its own equalizer (optional) may adjust its equalizer setting(s) in each of the EQ training loop (as shown as the dotted-box in Figure 3-12).

It is recommended that the receiver not set LANEx_CHANNEL_EQ_DONE, LANEx_SYMBOL_LOCK_DONE, and INTERLANE_ALIGN_DONE bits right after the successful reception of training patterns. Rather, the receiver should either increase its own equalization level or request a stronger pre-emphasis. When such action results in loss of successful reception, the receiver must restore or request the last setting. The purpose of this methodology is to ensure the maximum operating margin.

The minimum loop count in this sequence is 1, while the maximum loop count in this sequence (refer to Figure 3-12) must be 5.

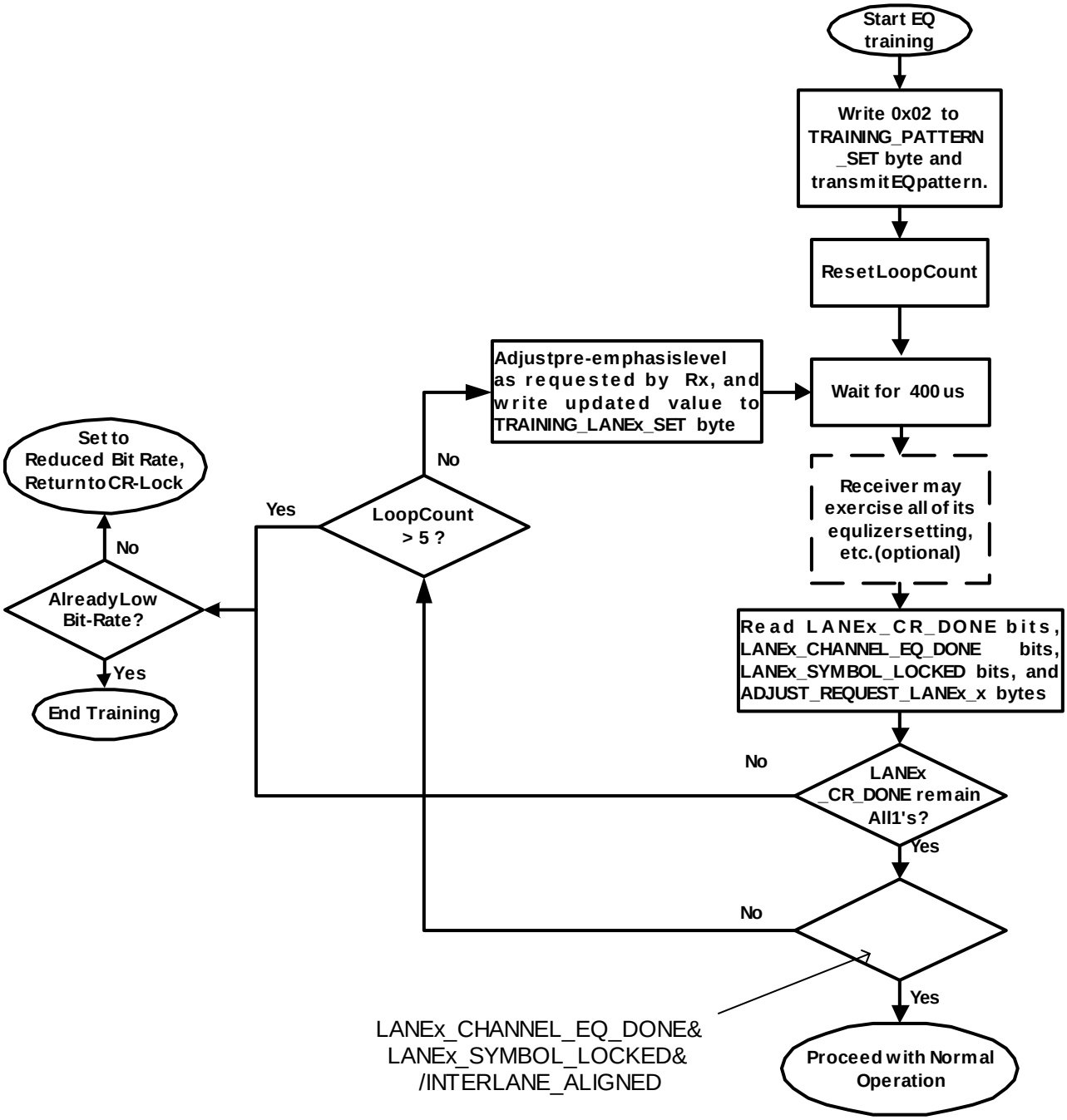


Figure 3-12: Channel Equalization Sequence of Link Training

Upon verifying that the Channel Equalization / Symbol-Lock / Inter-lane Alignment are all done, the transmitter must write 00h to the TRAINING_PATTERN_SET byte to indicate the end of training, and start transmission of stream data.

If the Clock Recovery circuit loses lock during the Channel Equalization sequence, the receiver must clear the CR_DONE_LANEx bit. If it is in the high bit-rate mode, the transmitter must then reduce the bit-rate and return to the CR training sequence. If it is already in the reduced bit-rate mode, then the transmitter must end the training by writing 00h to the TRAINING_PATTERN_SET byte without establishing the link.

3.5.1.4 Link Maintenance

The link status bits may be cleared by the receiver upon loss of clock recovery lock, symbol lock, or inter-alignment lock. The transmitter must check the link status whenever it detects a low-going IRQ HPD pulse during normal operation and perform re-training of the link as needed.

3.5.1.5 Link Quality Measurement (Testability)

The DisplayPort transmitter must be able to transmit test patterns for link quality measurement purpose as indicated in Section 2.5.3.5.

The DisplayPort receiver must support for the following:

- **Recovered Link Clock Quality Measurement:** Outputs the recovered link clock from a test pad when the DisplayPort Source Device writes to the RECOVERED_CLOCK_OUT_EN bit of the TRAINING_PATTERN_SET byte of the DPCD. The output clock frequency must be 1/40 of the link clock frequency.
  The purpose of this test output is to enable a simple EYE test for jitter measurements with minimal equipment for embedded applications using the recovered clock from the CDR circuits in the receiver. This output is not intended to be used for compliance purposes; such testing is specified in the DisplayPort compliance document.
  This test output must support a minimum of 10 pF of parasitic capacitance including that of the test probe. The test output must add no more than 11ps peak-to-peak jitter at the high bit rate and 18 ps peak-to-peak jitter at the reduced bit rate accumulated for a period of 250UI to facilitate 3% measurement accuracy (+/-1.5%); for example, if a single-ended output pad is desired, the test pad would need a minimum slew rate of 1.82 V / ns into the maximum expected capacitive load and can have no more than 20 mVp-p of total power supply noise. If the same pad can support 3.64 V/ns then 40 mVp-p power supply noise can be tolerated.
- **Link Symbol Error Rate Measurement:** Count of the number of unscrambled data symbols that are not 00h when the DisplayPort Source Device writes 08h to TRAINING_PATTERN_SET byte, and stores that count in SYMBOL_ERROR_COUNT_LANEx bytes of the DPCD. Link quality can be estimated using the procedure listed in Section 2.5.3.5.

3.5.2 Main Link Electrical Sub-Block

The electrical sub-block of a DisplayPort Main Link consists of up to four differential pairs. The DisplayPort Transmitter drives doubly-terminated, AC-coupled differential pairs as shown in Figure 3-13 in a manner compliant with the Main Link Transmitter electrical specification.

Note: The 50 Ω termination resistors may be integrated on the chip. The DisplayPort Receiver receives the incoming differential signals and extracts data with its link CDR (clock-and-data recovery) circuits.

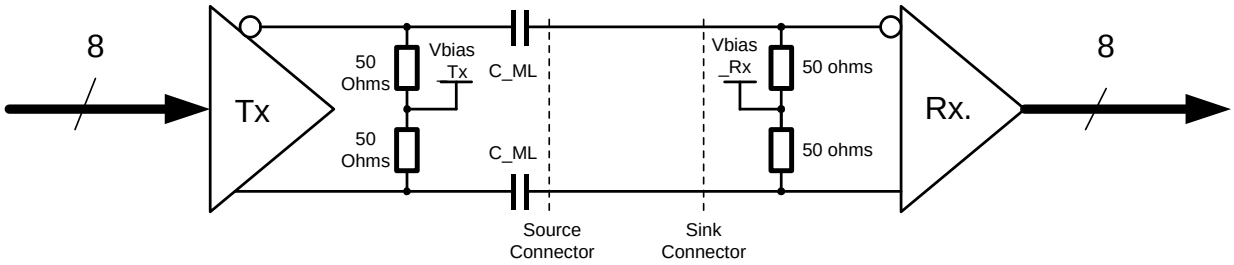


Figure 3-13: Main Link Differential Pair

3.5.2.1 Definition of Differential Voltage

A differential signal is defined by taking the voltage difference between two conductors. In this specification, a differential signal or differential pair is comprised of a voltage on a positive conductor, V_{D+}, and a negative conductor, V_{D-}. The differential voltage (V_{DIFF}) is defined as the difference of the positive and the negative conductor voltages ($V_{DIFF} = V_{D+} - V_{D-}$) as shown in Figure 3-14.

The Common Mode Voltage (V_{CM}) is defined as the average or mean voltage present on the same differential pair ($V_{CM} = [V_{D+} + V_{D-}]/2$).

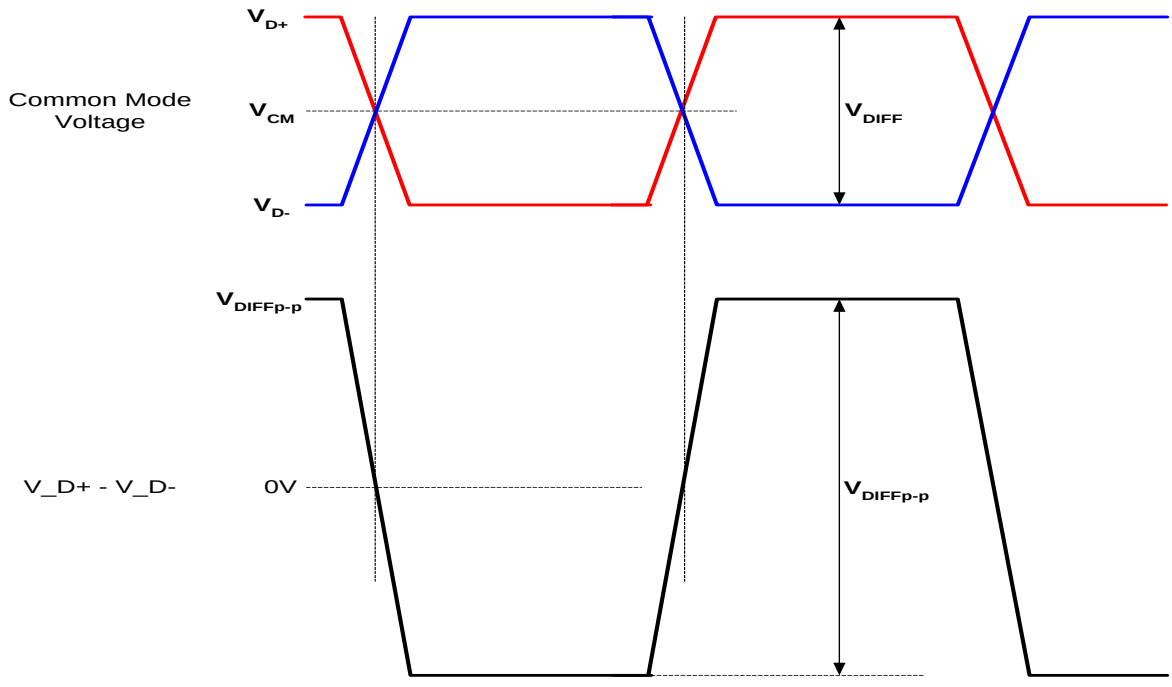


Figure 3-14: Definition of Differential Voltage and Differential Voltage Peak-to-Peak

This document's electrical specifications often refer to peak-to-peak measurements or peak measurements, which are defined by the following equations:

- Symmetrical Differential Swing
  - $V_{DIFFp-p} = (2 * \max |V_{D+} - V_{D-}|)$
- Asymmetrical Differential Swing
  - $V_{DIFFp-p} = (\max |V_{D+} - V_{D-}| \{V_{D+} > V_{D-}\} + \max |V_{D+} - V_{D-}| \{V_{D+} < V_{D-}\})$
- Common-Mode Voltage
  - $V_{CMp} = (\max |V_{D+} + V_{D-}| / 2)$

The definition equations only produce a single number (the number in the specification tables) and are not suitable for plotting a waveform.

3.5.3 Transmitter and Receiver Electrical Specifications

Table 3-10 and Table 3-11 show the Main Link transmitter and receiver electrical specifications (respectively).

Table 3-10: DisplayPort Main Link Transmitter (Main TX) Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI_High_Rate	Unit Interval for high bit rate (2.7 Gbps / lane)		370		ps	Range is nominal +/- 300ppm. UI does not account for down-spread dictated variations.
UI_Low_Rate	Unit Interval for low bit rate (1.62 Gbps / lane)		617		ps	
Down_Spread _Amplitude	Link clock down spreading	0		0.5	%	
Down_Spread _Frequency	Link clock down-spreading frequency	30		33	kHz	
$V_{TX-DIFFp-p-Level1}$	Differential Peak-to-peak Output Voltage Level 1	0.34	0.4	0.46	V	Refer to Figure 3-15 for definition of differential voltage. For embedded connection, support of programmable voltage swing levels is optional.
$V_{TX-DIFFp-p-Level2}$	Differential Peak-to-peak Output Voltage Level 2	0.51	0.6	0.68	V	
$V_{TX-DIFFp-p-Level3}$	Differential Peak-to-peak Output Voltage Level 3	0.69	0.8	0.92	V	
$V_{TX-DIFFp-p-Level4}$	Differential Peak-to-peak Output Voltage Level 4	1.02	1.2	1.38	V	
$V_{TX-PREEMP-RATIO}$	No Pre-emphasis	0.0	0.0	0.0	dB	Refer to Figure 3-15 for definition of differential voltage. Support of no pre-emphasis, 3.5 dB and 6.0 dB pre-emphasis is required. Support of 9.5 dB level is optional. For embedded connection, support of programmable pre-emphasis levels is optional.

Symbol	Parameter	Min	Nom	Max	Units	Comments
	3.5 dB Pre-emphasis Level	2.8	3.5	4.2	dB	
	6.0 dB Pre-emphasis Level	4.8	6.0	7.2	dB	
	9.5 dB Pre-emphasis Level	7.6	9.5	11.4	dB	
Tx Horizontal Eye Specification for High Bit Rate						
$T_{TX\text{-}EYE\_CHIP\_High\_Rate}$	Minimum TX Eye Width at Tx package pins	0.74			UI	
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER\_CHIP\_\_High\_Rate}$	Maximum time between the jitter median and maximum deviation from the median at Tx package pins			0.13	UI	
Tx Horizontal Eye Specification for Reduced Bit Rate						
$T_{TX\text{-}EYE\_CHIP\_Low\_Rate}$	Minimum TX Eye Width at Tx package pins	0.84			UI	
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER\ CHIP\ Low\_Rate}$	Maximum time between the jitter median and maximum deviation from the median at Tx package pins			0.08	UI	
$T_{TX\text{-}RISE\_CHIP}$, $T_{TX\text{-}FALL\_CHIP}$	D+/D- TX Output Rise/Fall Time at Tx package pins	50		130	ps	At 20-to-80
$V_{TX\text{-}DC\text{-}CM}$	TX DC Common Mode Voltage	0		VDD	V	Common mode voltage is equal to Vbias_Tx voltage shown in Figure 3-13. VDD is the output driver power supply voltage and 3.6V maximum.
$V_{TX\text{-}AC\text{-}CM}$	TX AC Common Mode Voltage			20	mV	Measured at 1.62 GHz and 2.7 GHz (if supported), within the frequency tolerance range. Frequency-domain measurement using a spectrum analyzer.
$I_{TX\text{-}SHORT}$	TX Short Circuit Current Limit			90	mA	Total drive current of the transmitter when it is shorted to its ground.
$RL_{TX\text{-}DIFF}$	Differential Return Loss at 0.675GHz			12	dB	Straight loss line between 0.675 GHz and 1.35 GHz
	Differential Return Loss at 1.35GHz			9	dB	
$L_{TX\text{-}SKEW\text{-}INTER\_PAIR}$	Lane-to-Lane Output Skew at Tx package pins			2	UI	
$L_{TX\text{-}SKEW\text{-}INTRA\_PAIR}$	Lane Intra-pair Output Skew at Tx package pins			20	ps	
$T_{TX\text{-}RISE\_FALL\_MISMATCH\_CHIPDIFF}$	Lane Intra-pair Rise-fall Time Mismatch at Tx package pins.			5	%	INFORMATIVE. D+ rise to D- fall mismatch and D+ fall to D- rise mismatch.
C_{TX}	AC Coupling Capacitor	75		200	nF	All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling

Symbol	Parameter	Min	Nom	Max	Units	Comments
						capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.
$F_{TX-REJECTION-BW}$	Clock Jitter Rejection Bandwidth			4	MHz	INFORMATIVE. Transmitter jitter must be measured at source connector pins using a signal analyzer that has a 2nd order PLL with tracking bandwidth of 20MHz (for D10.2 pattern) and damping factor of 1.428

Table 3-11: DisplayPort Main Link Receiver (Main RX) Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI_High_Rate	Unit Interval for high bit rate (2.7 Gbps / lane)		370		ps	Range is nominal +/-350ppm. DisplayPort link RX does not require local crystal for link clock generation.
UI_Low_Rate	Unit Interval for low bit rate (1.62 Gbps / lane)		617		ps	
Down_Spread _Amplitude	Link clock down spreading	0.5			%	0.5% downspread support is required. Modulation frequency range of 30 kHz to 33 kHz must be supported.
$V_{RX-DIFFp-p}$	Differential Peak-to-peak Input Voltage at package pins	120			mV	Refer to Figure 3-14 for definition of differential voltage.
Rx Horizontal Eye Specification for High Bit Rate						
T_{RX-EYE_CONN}	Minimum Receiver Eye Width at Rx-side connector pins	0.51			UI	
T_{RX-EYE_CHIP}	Minimum Receiver Eye Width at Rx package pins	0.47			UI	
$T_{RX-EYE-MEDIAN-to-MAX-ITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at Rx package pins			0.265	UI	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ

Symbol	Parameter	Min	Nom	Max	Units	Comments
Rx Horizontal Eye Specification for Reduced Bit Rate						
T_{RX-EYE_CONN}	Minimum Receiver Eye Width at Rx-side connector pins	0.46			UI	
T_{RX-EYE_CHIP}	Minimum Receiver Eye Width at Rx package pins	0.42			UI	(1- T_{RX-EYE_CONN}) specifies the allowable TJ.
$T_{RX-EYE-MEDIAN-to-MAX-ITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at Rx package pins			0.29	UI	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ
$V_{RX-DC-CM}$	RX DC Common Mode Voltage	0		VDD	V	Common mode voltage is equal to Vbias_Rx voltage shown in Figure 3-13. VDD is the receiver input power supply voltage and 3.6V maximum.
$I_{RX-SHORT}$	RX Short Circuit Current Limit			90	mA	Total drive current of the transmitter when it is shorted to its ground.
$RL_{RX-DIFF}$	Differential Return Loss at 0.675 GHz			12	dB	Straight loss line between 0.675 GHz and 1.35 GHz
	Differential Return Loss at 1.35 GHz			9	dB	
$R_{RX-HGIH-IMP-DC}$	Powered Down DC Input resistance	200k			Ω	
$L_{RX-SKEW-INTER\_PAIR}$	Lane-to-Lane Skew at RX package pins			5200	ps	Maximum skew limit between different RX lanes of a DisplayPort link.
Intra-pair Skew Specification for High Bit Rate						
$L_{RX-SKEW-INTRA\_PAIR\ High-Bit-Rate}$	Lane Intra-pair Skew at RX package pins			100	ps	Maximum skew limit between D+ and D- of the same lane.
Intra-pair Skew Specification for Reduced Bit Rate						
$L_{RX-SKEW-INTRA\_PAIR\ \_Reduced-Bit-Rate}$	Lane Intra-pair Skew at RX package pins			300	ps	Maximum skew limit between D+ and D- of the same lane.
$F_{RX-TRACKING-BW}$	Jitter Tracking Bandwidth	20			MHz	Minimum CDR tracking bandwidth at the receiver when the input is repetition of D10.2 symbols without scrambling

3.5.3.1 AC Coupling

Each lane of a DisplayPort link must be AC coupled. The minimum and maximum values for the capacitance are specified in Table 3-10. The requirement for the inclusion of AC coupling capacitors on the interconnect media is specified at the DisplayPort transmitter.

3.5.3.2 Termination

The DisplayPort Main Link transmitter must meet the impedance and return loss specifications specified in Table 3-10, whenever the link is active.

3.5.3.3 DC Common Mode Voltage

For the DisplayPort Main Link, the transmitter DC common mode voltage is held at the same value during all states unless otherwise specified. The range of allowable transmitter DC common mode values is specified in Table 3-10 ($V_{TX\text{-}DC\text{-}CM}$).

The DisplayPort transmitter shall pre-charge the bus to a common mode voltage for 10 μs or longer before starting the Link Training sequence. In the current revision of the Physical Layer specification, an abbreviated version of Link Training following a momentary Electrical Idle period (for example, turning off the link during the vertical blanking interval of a video stream) is not defined.

3.5.3.4 Voltage Swing and Pre-emphasis

The DisplayPort transmitter specification allows four non-transition voltage swing levels and four pre-emphasis levels. (Definition of pre-emphasis is shown in Figure 3-15.). Those levels are (0.2, 0.6, 0.8 and 1.2) Vdiff_pp and (0, 3.5, 6.0 and 9.5) dB, respectively (all are nominal values).

Certain combinations of these levels result in differential peak-to-peak voltages which are outside the allowable range of $0.4V_{TX\text{-}DIFFp\text{-}p}$ to $1.2V_{TX\text{-}DIFFp\text{-}p}$, and thus, are not allowed. Table 3-12 lists the allowable combinations of drive current and pre-emphasis settings.

Pre-emphasis, as used in this document, is defined as 20 multiplied by the $\log_{10}$ of the ratio of the peak-to-peak amplitude for the first T_{BIT} immediately following a transition divided by the peak-to-peak amplitude for the subsequent bits until the next transition ($20 \cdot \log$ (Vmax / Vmin)).

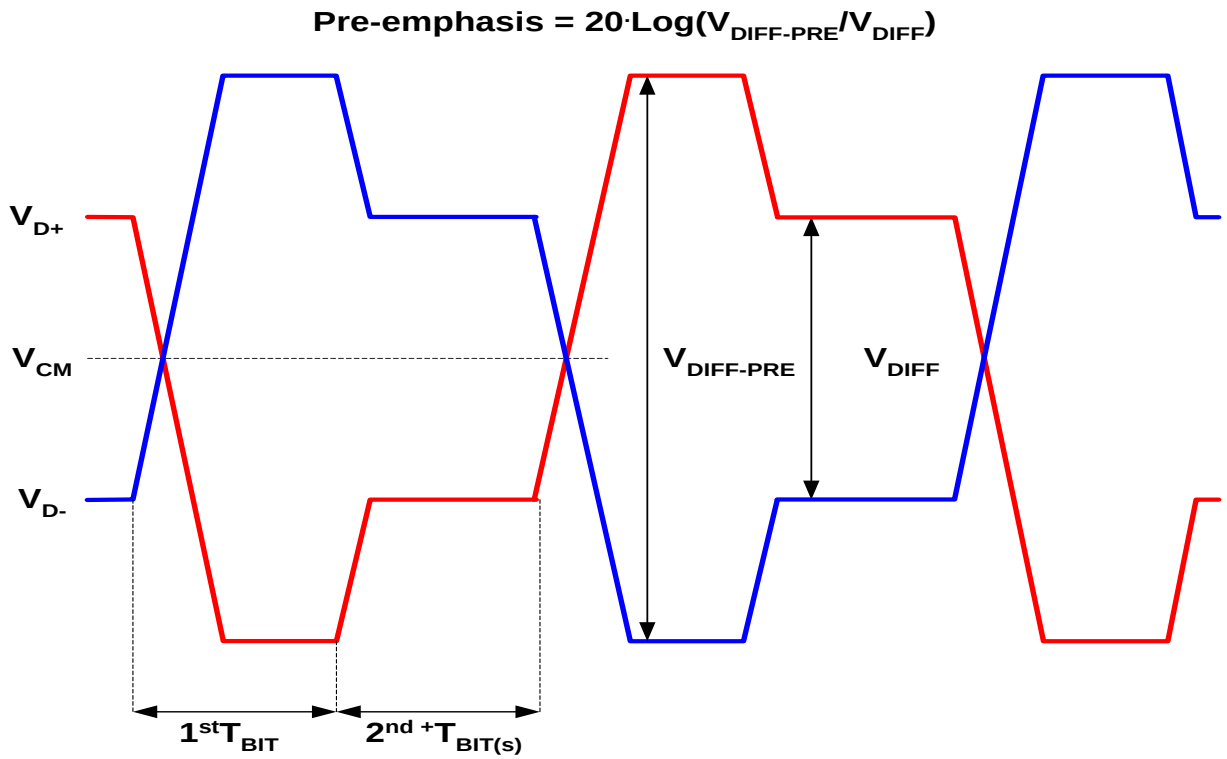


Figure 3-15: Definition of Pre-emphasis

Table 3-12: Allowed Vdiff_pp - Pre-emphasis Combinations

	Pre-emphasis Level (dB)			
	Required			Optional
	0 dB (1x)	3.5 dB (1.5x)	6 dB (2x)	9.5 dB (3x)
Vdiff_pp	Vdiff_pre_pp	Vdiff_pre_pp	Vdiff_pre_pp	Vdiff_pre_pp
0.4	0.4	0.6	0.8	1.2
0.6	0.6	0.9	1.2	Not allowed
0.8	0.8	1.2	Not allowed	Not allowed
1.2	1.2	Not allowed	Not allowed	Not allowed

Note: This table shows nominal values. For detailed specification, refer to Table 3-10 and Table 3-11..

3.5.3.5 Short Circuit Requirements

The driver and receiver circuits of the Main Link block must survive the worst-case short-circuit current of 90mA (3.6V over 40Ω).

3.5.3.6 Bandwidth of Transmitter / Receiver PLL's

No reference clock is required to be forwarded over the DisplayPort link. An accurate local time reference (for example, a local crystal) is optional for a Sink (receiving) Device. The Training Sequence must be used to establish the proper clock recovery by the DisplayPort receiver.

The DisplayPort specification requires that the Source Device link-clock generation PLL have a closed-loop bandwidth of no more than 4 MHz and that the Sink Device clock-recovery PLL have a closed-loop bandwidth of no less than 20 MHz (for the D10.2 pattern).

The 4 MHz Source Device PLL jitter rejection bandwidth in Table 3-10 was selected as a reasonable target based on existing designs of a similar nature. The factor of five margin was selected to accommodate the lowest dynamic clock recovery bandwidth during the longest ANSI 8B/10B run-lengths.

Note: The 4 MHz PLL jitter ejection bandwidth is an informative specification. Compliance to the Source Device jitter specification described in section 3.5.3.8 is measured at the source connector pins using a signal analyzer that has a 2nd order PLL with a tracking bandwidth of 20 MHz (for D10.2 pattern) and a damping factor of 1.428.

3.5.3.7 Down-spreading of Link Clock

Sink Devices compliant with DisplayPort specification version 1 revision 1 must support down-spreading of the link clock. The down-spread amplitude must be either disabled (0.0%) or 0.5% as written to the Link Configuration Field in the DPCD (DisplayPort Configuration Data) by the Source Device. The modulation frequency must be 30 kHz to 33 kHz.

3.5.3.8 DisplayPort Jitter Specifications

This section describes the jitter budget for Source and Sink Devices. Jitter specification compliance is measured at the Source connector pins (TP2) and Sink connector pins (TP3) as shown in Figure 3-16.

The jitter specifications at the transmitter and receiver integrated circuit package pins are informative.

A compliance test load that consists of a pair of 50Ω resistive loads as shown in Figure 3-17 is used during the measurement.

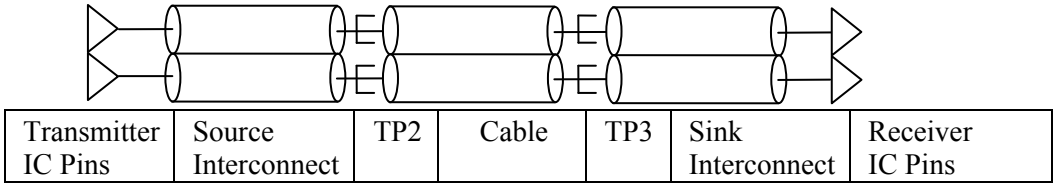


Figure 3-16: Compliance Measurement Points of the Channel

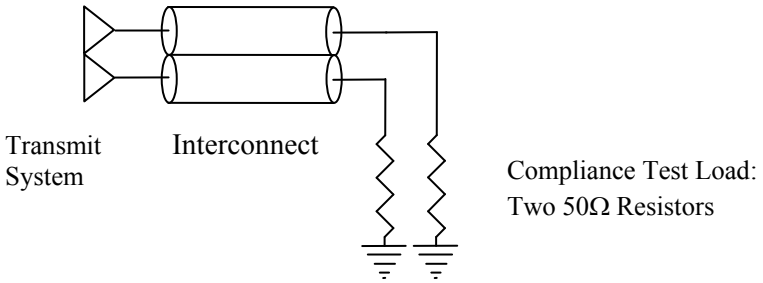


Figure 3-17: Compliance Test Load

3.5.3.8.1 Receiver Jitter Tolerance Masks

The DisplayPort spectral jitter at the Sink connector pins (TP3) must comply with the requirements as indicated in the receiver Jitter Tolerance Masks shown in Figure 3-18 (for high bit rate) and Figure 3-19 (for reduced bit rate). These masks are defined as follows:

$$s(f) := 2\cdot\pi\cdot f\cdot j \qquad \tau_z = 7.956\cdot 10^{-8} \qquad \tau_{p2} = 9.822\cdot 10^{-10} \qquad G = 1.272\cdot 10^{15}$$

$$G_o(f) := \frac{G}{s(f)^2}\cdot\frac{\left(s(f)\cdot\tau_z + 1\right)}{\left(s(f)\cdot\tau_{p2} + 1\right)} \qquad Hs(f) := \frac{G_o(f)}{1 + G_o(f)}$$

The High Bit Rate (HBR) jitter mask is calculated as follows:

$$JTHBRrx(f) := \left|\frac{0.504}{1 - Hs(f)}\right|$$

This measurement must be made with a signal analyzer emulating the jitter tracking of a receiver clock recovery PLL. The tracking bandwidth of the signal analyzer is the closed-loop bandwidth as defined by the equation Hs(f) above for Hs(20 MHz) = 0.7071 for a D10.2 clock pattern (20 MHz at 100% edge density).

The clock recovery emulation must also emulate the clock recovery characteristics of a receiver in that as edge density is reduced the effective bandwidth is also correspondingly reduced.

For example: For a K28.7 clock pattern the edge density is one-fifth and the corresponding effective bandwidth is 5.087 MHz.

At HBR, a compliant Sink (receiver) jitter tolerance must be at or above the JTHBRrx curve shown in Figure 3-18.

Table 3-13 which breaks up the total jitter (TJ) into ISI (inter-symbol interference) and non-ISI jitter.

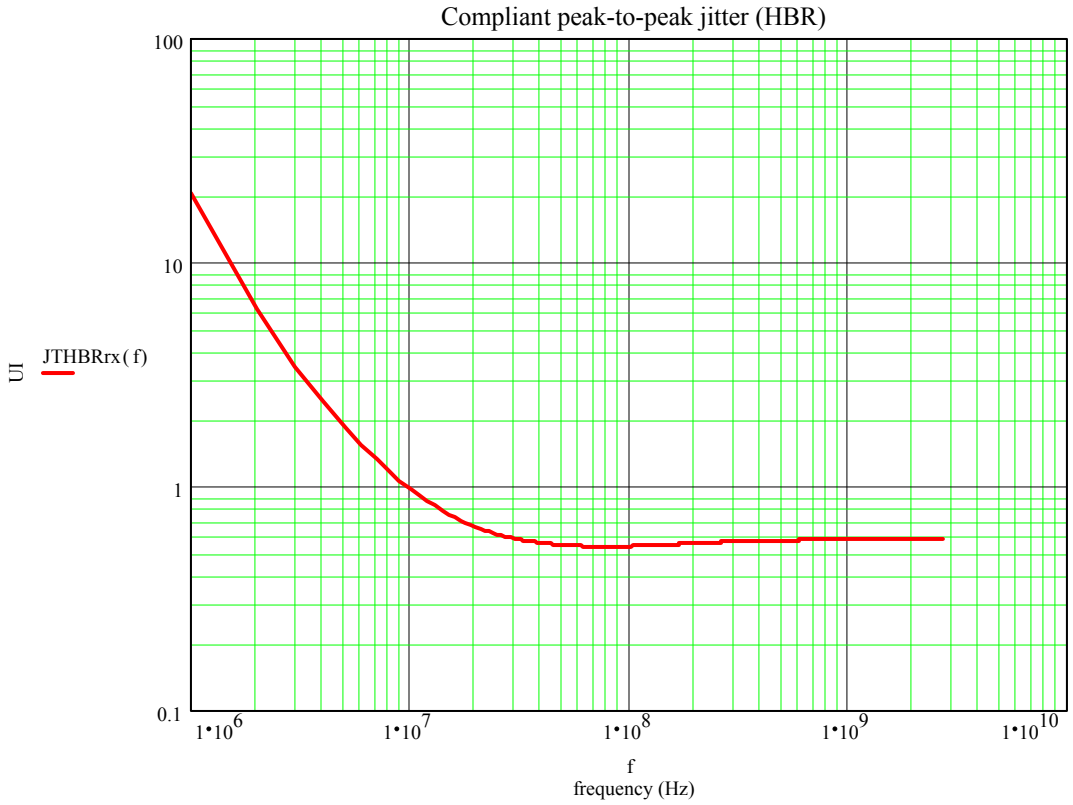


Figure 3-18: High Bit Rate Jitter Output / Input Tolerance Mask

The Reduced Bit Rate (RBR) jitter mask is calculated as follows:

$$JTRBRrx(f) := \left| \frac{0.554}{1 - Hs(f)} \right|$$

At RBR, a compliant Sink (receiver) jitter tolerance must be at or above the JTRBRrx curve (top) shown in Figure 3-19. Refer to Table 3-13Table 3-13 which breaks up the Total Jitter (TJ) into ISI (inter-symbol interference) and non-ISI jitter.

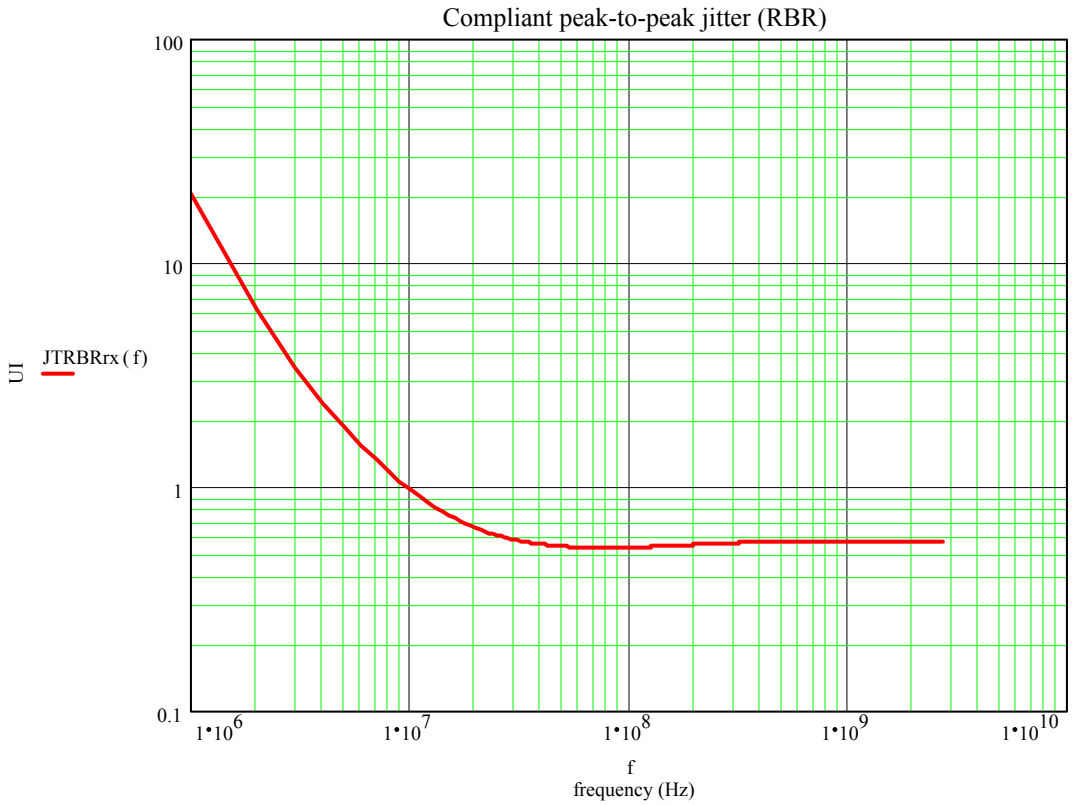


Figure 3-19: Reduced Bit Rate Jitter Output / Input Tolerance Mask

3.5.3.8.2 Differential Noise Budget

Jitter specifications relate to the phase relationship between an idealized reference clock and the data. Any phase error that results in the sample being improperly read (i.e. prior bit or following bit sampled) will result in a bit error.

These error components have been broken up into ISI (inter-symbol interference) and non-ISI jitter. The TJ (total jitter) is the total peak to peak phase variation in the zero volt differential crossing point of the data stream for a given BER, and is defined as DJ + (RJ * scale factor), where the scale factor is determined by the BER.

The DisplayPort interface jitter characteristics must comply with the jitter budget allocations in Table 3-13.

Table 3-13: Differential Noise Budget

	Transmitter Package Pins (INFORMATIVE)		Transmitter Connector (TP2) [NORMATIVE]		Receiver Connector (TP3) [NORMATIVE]		Receiver Package Pins (INFORMATIVE)		Notes
	Non-ISI	TJ	Non-ISI	TJ	Non-ISI	TJ	Non-ISI	TJ	
High-Bit Rate (2.7 Gbps per lane)									
$A_{,p-p}$	0.260	0.260	0.260	0.364	0.330	0.491	0.339	0.530	1, 2, 3
Reduced-Bit Rate (1.62 Gbps per lane)									
$A_{,p-p}$	0.160	0.160	0.160	0.223	0.442	0.539	0.465	0.580	1, 2, 3
f_{SSC}, Spread-Spectrum Modulation Frequency	30 / 33 kHz								
$SSC_{tol,}$ Spread-Spectrum Modulation Deviation	Minimum = 5000 ppm Maximum = 0 ppm								
$f_{tol,}$ TX Frequency Long Term Stability	Minimum = -350 ppm Maximum = 350 ppm								

Notes:

1. DisplayPort transmitter pre-emphasis must be enabled as needed in order to meet this budget specification.
2. A_{p-p} is the peak-to-peak jitter, in UI, required for the measurement points listed. The TP3 jitter properties are intended only for Sink test calibration and Hybrid-solution minimum signal consideration. This is not intended to be used as a cable qualification requirement.
3. Jitter must be measured with a second order type 2 tracking PLL configured to have a corner frequency of 20MHz (for D10.2 pattern) and damping factor of 1.428. The upper bound on this jitter measurement should be no less than the 5th harmonic of the data transmission rate.

3.5.3.9 The Dual Dirac Jitter Model (INFORMATIVE) [2]

It should be understood that although jitter can be described using a dual Dirac model, it should not be understood that the jitter in the system really is dual Dirac. Typically jitter will be distributed or structured, and the dual Dirac description is merely the linearization of the cdf (cumulative distribution function) at a particular BER. It should also be understood that the use of the dual Dirac model here and in the system budgeting is only a language to help define the jitter in the system, and does not imply that this should be the normative derivation methodology for the derivation of the jitter in the system.

[2] Referenced and reused with permission from Ransom Stevens on "What The Dual Dirac Model is and what it is not " available on www.jitter360.com

Three tools are needed to describe the Dual–Dirac model:

1st The **Dirac-delta** function:

$$\delta(x-x_0) \equiv \begin{cases} 0, & x \neq x_0 \\ \to \infty, & x = x_0 \end{cases} \quad \text{with} \quad \int \delta(x-x_0)dx = 1$$

2nd The RJ PDF is a **Gaussian:**

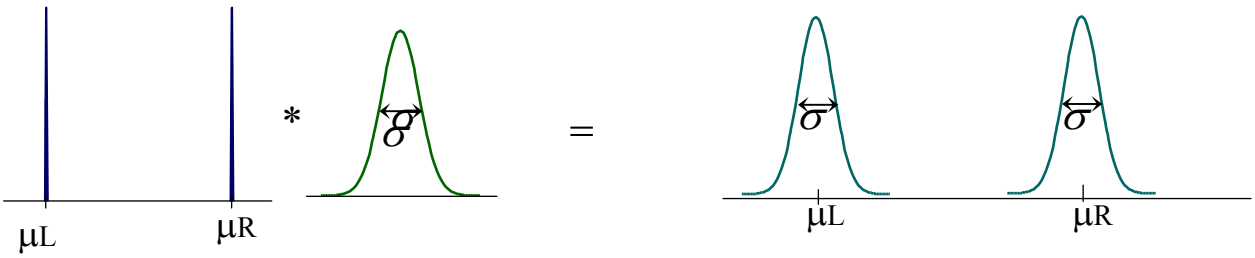
$$PDF_{RJ}(x) = \frac{1}{\sqrt{2\pi}\sigma}\exp\left[-\frac{x^2}{2\sigma^2}\right]$$

3rd The different jitter components combine through **convolution:**

$$\begin{aligned} \text{PDF}(x) &= \text{PDF}_{DJ}(x) * \text{PDF}_{RJ}(x) \\ &= \int \text{PDF}_{DJ}(u) * \text{PDF}_{RJ}(x-u)du \end{aligned}$$

The Dual-Dirac is made up form the following elements:

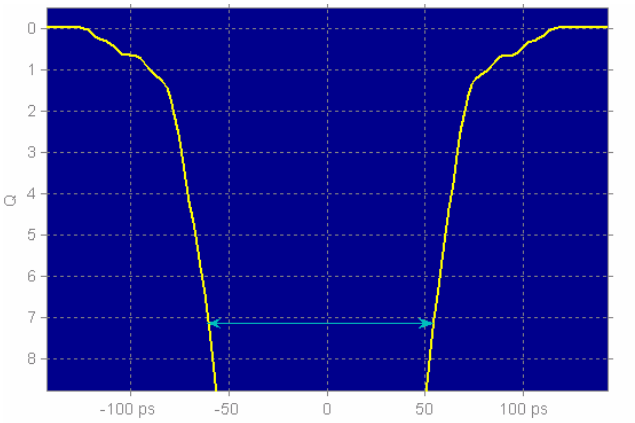
$$\left[\delta(x-\mu_L)+\delta(x-\mu_R)\right] * \frac{1}{\sqrt{2\pi}\sigma}\exp\left(-\frac{x^2}{2\sigma^2}\right) = \frac{1}{\sqrt{2\pi}\sigma}\left[\exp\left(-\frac{(x-\mu_L)^2}{2\sigma^2}\right)+\exp\left(-\frac{(x-\mu_R)^2}{2\sigma^2}\right)\right]$$



Dual-Dirac DJ `Gaussian RJ

DJ(p-p) = $\mu R - \mu L$ $RJ = \sigma$

The derivation of TJ(BER) in dual-Dirac: Generally we can define the bathtub plot,



$$\mathrm{BER}(x) = \rho_T \int_x^{\infty} \mathrm{PDF}(x')dx' + \rho_T \int_{-\infty}^{x} \mathrm{PDF}(x'-T)dx'$$

Plug in dual-Dirac:

$$\mathrm{BER}_{\delta\delta}(x) = \rho_T \left[\mathrm{erfc}\left(\frac{x-\mu_L}{\sqrt{2}\sigma} \right) + \mathrm{erfc}\left(\frac{(x-T)-\mu_R}{\sqrt{2}\sigma} \right) \right]$$

Evaluate the complementary error functions, erfc(x), and get:

$\underline{\mathrm{TJ(BER)} = 2Q_{BER} \times \mathrm{RJ}(\delta\delta) + \mathrm{DJ}(\delta\delta)}$

For BER = 10^{-9}, Q_{BER} = 6.15

The jitter model under these conditions would be 12.3Rj + Dj = Tj

3.5.3.10 Differential Voltage / Timing (EYE) Diagram

The EYE diagram is used to measure compliance of Source Device.

The polygon in Figure 3-20 represents the Source EYE Mask at the Source Connector pins (TP2). Table 3-14 and Table 3-15 contain the values to be used for the vertices of the mask for high bit rate and reduced bit rate, respectively.

The EYE diagram must be measured at TP2 (with a Compliance Test Load) using a signal analyzer with 2nd order tracking PLL configured to have a tracking bandwidth of 20MHz with a damping factor of 1.428.

The measured EYE must be equal to or larger than the EYE mask. The transmitted pattern must be PRBS7. Those Source Devices that support down-spreading of the link clock may measure the EYE with down-spreading enabled. The pre-emphasis may be enabled.

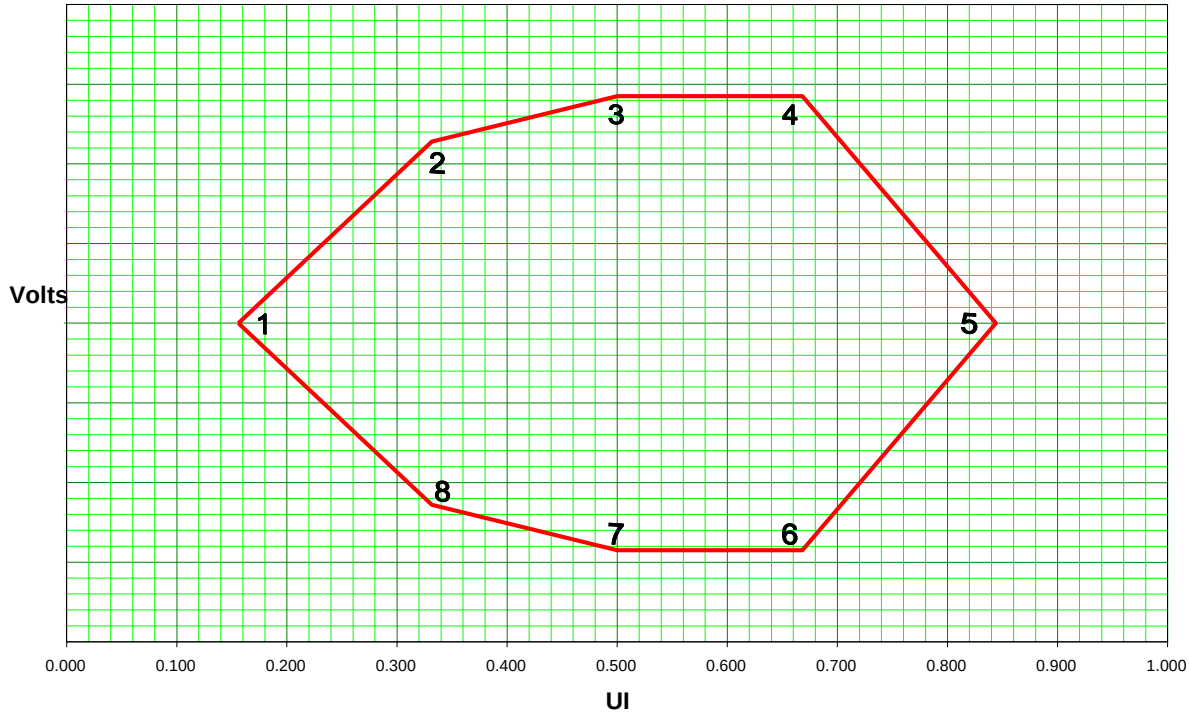


Figure 3-20: EYE Mask at Source Connector Pins

Table 3-14: Mask Vertices for High Bit Rate

Point	A_0	Voltage (Volts)
1	0.159	0.000
2	0.332	0.158
3	0.500	0.198
4	0.668	0.198
5	0.844	0.000
6	0.665	-0.198
7	0.500	-0.198
8	0.332	-0.158

Table 3-15: Mask Vertices for Reduced Bit Rate

Point	A_0, f_0	Voltage (Volts)
1	0.102	0.000
2	0.277	0.255
3	0.500	0.318
4	0.723	0.318
5	0.899	0.000
6	0.723	-0.318
7	0.500	-0.318
8	0.277	-0.255

The polygon in Figure 3-21 represents the minimum entry EYE into the Sink Device at TP3. Table 3-16 and

Table 3-17 contain the values to be used for the vertices of the mask for high bit rate and reduced bit rate, respectively. The EYE must be measured with a signal analyzer with 2nd order tracking PLL configured to have a tracking bandwidth of 20MHz with a damping factor of 1.428.

This EYE Mask is used for testing the jitter tolerance of Sink Device. A test pattern generator, while transmitting the PRBS7 bit stream, must be adjusted to realize the minimum EYE. The rise / fall time must be set to 130ps for 20-80% transition.

Once the test pattern generator is adjusted, the PRBS7 bit stream must be sent to the Sink connector pins (TP3) of the Sink Device. With this input, the Sink Device must realize a BER of $1E^{-9}$ or better.

For a Sink Device with a permanently tethered cable, the BER specification must be met with an input EYE to the plug connector that is equal to TP2 EYE mask.

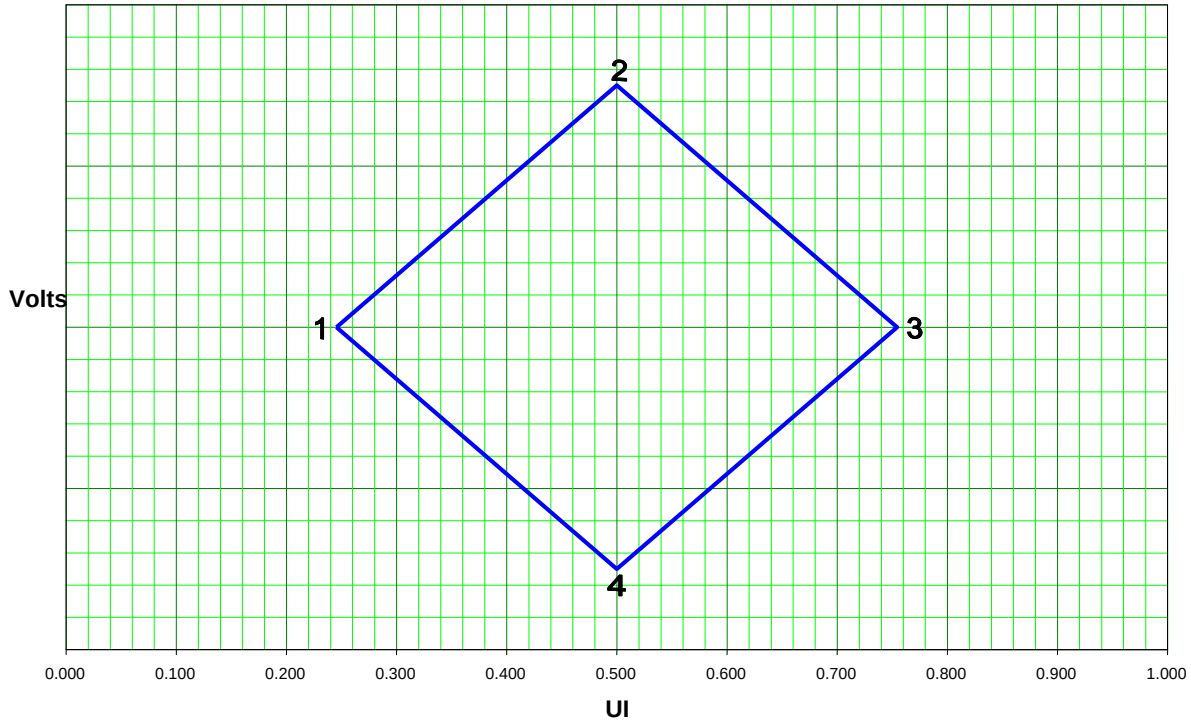


Figure 3-21: Mask at TP3

Table 3-16: Sink EYE Vertices for TP3 at High Bit Rate

Point	A_0, f_0	Voltage (Volts)
1	0.246	0.000
2	0.500	0.075
3	0.755	0.000
4	0.500	-0.075

Table 3-17: Sink EYE Vertices at TP3 for Reduced Bit Rate

Point	A_0, f_0	Voltage (Volts)
1	0.270	0.000
2	0.500	0.068
3	0.731	0.000
4	0.500	-0.068

3.5.3.11 Loss Over Source Interconnect

The Source interconnect is the trace route between the Main Link transmitter integrated circuit package pins and the Source connector pins (TP2).

The Source Device must generate an EYE at TP2 that is equal to or larger than that described in Table 3-14 for high-bit-rate operation and that in Table 3-15 for reduced-bit-rate operation.

The EYE must be measured with a signal analyzer with 2nd order tracking PLL configured to have a tracking bandwidth of 20 MHz (for D10.2 pattern) with a damping factor of 1.428. All Main Link lanes must be on and driving the PRBS7 test pattern with a two symbol (20 UI) skew between each lane and adjacent lane(s). Non-transitional bit voltage swing level and pre-emphasis level must be adjusted as needed to meet the TP2 EYE mask specification.

The impedance of the Source interconnect should be matched to the impedance of the connector and cable assembly so as to minimize return loss and maximize the transmitted signal. Failure to properly match the impedances will reduce the EYE opening decreasing the allowable Source interconnect trace length.

Protection devices should add no more than 1.5 pF parasitic load to each trace. Series protection resistors are not recommended. Losses are demonstrated by an EYE measurement at the Source connector (TP2).

Note: The approximate maximum length is 304.5mm (12 inches) using high volume manufacturing PCB materials. It is recommended that no more than three vias per trace be used.

3.5.3.12 Loss Over Sink Interconnect

The Sink interconnect is the trace route between the Sink connector pins and Main Link receiver integrated circuit package pins.

The impedance of the Sink interconnect should be matched to the impedance of the connector and cable assembly so as to minimize return loss and maximize the transmitted signal. Failure to properly match the impedances will reduce the eye opening decreasing the allowable Sink interconnect trace length.

Protection devices should add no more than 1.5 pF parasitic load to each trace. Series protection resistors are not recommended.

Note: The approximate maximum length is 50.8 mm (2 inches) using high volume manufacturing PCB materials. It is recommended that no more than two vias per trace be used.

3.5.4 ESD and EOS Protection

The DisplayPort based system must protect all potentially exposed interface signals and power pins to meet or exceed the EOS (electrical over stress) specification of IEC 61000-4-2, Level 4 (8kV contact) without damage. For repeatability of the contact test, the exposed input / output or power line must withstand a direct strike to each connector pin without contacting the ESD test gun to the connector shield.

All signal and power pins of associated DisplayPort components (transmitter IC, receiver IC, and associated I/O circuitry) must also withstand at least JEDEC JESD22-A114-B Class 2 (2kV Human Body Model, 200V Machine Model) strikes.

DisplayPort Devices implementing this specification may swing the I/O lines as high as ± 0.3V single-ended with respect the common mode bias reference level. The designer must carefully select clamping devices and clamping rail voltages such that ESD devices will not cause clipping of normal signals.

4 Mechanical

This chapter describes the mechanical specifications of a DisplayPort link. Cable assembly specification for external connection and connector specification are covered in this chapter[3]. Applications requiring a larger or longer "box to box" application space than supported by a passive cable assembly as defined in this section may be supported by the use of an active, Hybrid Device or any other such device as provided for under Section 2.1.4. The interfaces of these devices must meet the interface requirements of a source and sink respectively.

4.1 Cable-Connector Assembly Specifications (for box-to-box)

The cable assembly specification is divided into two categories reflecting the high bit rate (2.7 Gbps per lane) and the low bit rate (1.62 Gbps per lane), respectively.

The high bit rate specification generally has higher performance electrical requirements and is usually represented by one or more of the following: shorter lengths, larger wire gauges, lower dielectric loss insulation materials.

The low bit rate specification generally has lower performance electrical requirements and is usually represented by one or more of the following: longer lengths, smaller wire gauges, higher dielectric loss insulation materials.

Among the cable-connector assembly parameters, IL (insertion loss), RL (reflection loss), skew (both intra-pair and inter-pair), and Near End Noise (NEN) differ between high-bit-rate and low-bit-rate specifications.

Both categories represent the box-to-box application space sometimes referred to as external / desktop and consumer electronics (CE).

The embedded cable application space which is characterized by its inaccessibility to the end-user and is sometimes referred to as internal / mobile is not explicitly specified here. Instead, the system-integrator is required to meet the EYE mask requirements at the receiver pins by making appropriate trade-offs between circuit trace performance and cabling performance.

In general the high bit rate and low bit rate electrical specification presented below still apply to the internal / mobile cable assemblies given the same PCB traces at both ends of the channel except that the physical dimensions are much smaller.

4.1.1 Cable-Connector Assembly Definition

A DisplayPort Cable Assembly is comprised of two plug type connectors terminating both ends of a bulk cable as depicted in Figure 4-1.

[3] Masks for insertion loss, reflection loss, near-end noise, and far-end noise, and the impedance profile in this chapter were generated by Tyco Electronics. Channel simulations were run to verify that the worst-case cable-connector assembly as represented by those masks would meet receiver eye masks specified in this document.

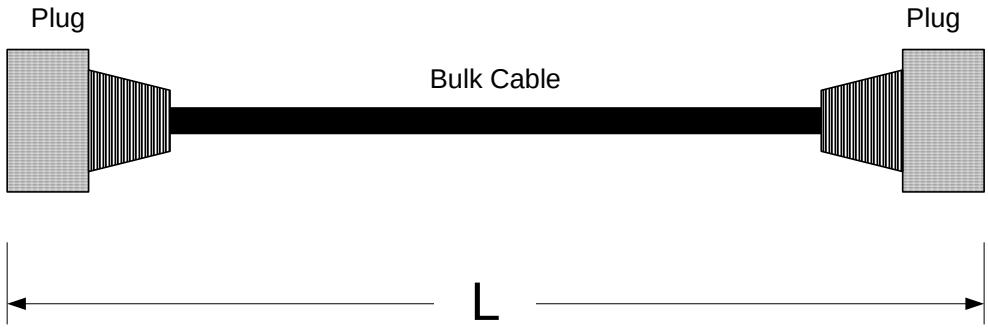


Figure 4-1: Cable Assembly

4.1.1.1 Cable Construction Guideline for EMI Reduction (INFORMATIVE)

The following recommendations for the construction of DisplayPort cable assemblies should be followed to prevent EMI issues:

- The intra-pair skew for differential pairs in the cable assembly should be made as small as possible and should meet the limits defined by the DisplayPort Specification version 1 revision 1.
- The termination of the cable shielding to the connector shield should cover a full 360^{o} around the cable and be of low impedance.
- The shielding between the device chassis, DisplayPort receptacle shield, DisplayPort plug shield, and cable shielding should form a unified low impedance link in order to maximize the efficiency of the shielding and minimize EMI. To facilitate this, the use of multiple grounding points and contact points between shield parts is recommended.
- As a general rule, unnecessary apertures in the shields may cause leakage. It is strongly recommended that the gaps between shielding components be eliminated. It is also strongly recommended that the shell cover as much of the connector as possible to yield the maximum EMI protection of the signal pins.
- As a recommendation, the shielding construction of the bulk cable should follow general high speed practices of including both a foil and braid shielding materials in its construction. A further recommendation is that the foil layer be a Al / Mylar wrap (spiral or longitudinal) with a minimum 20% overlap, and that the conductive braid should have a minimum 75% coverage over the inner foil layer to ensure effective EMI shielding.

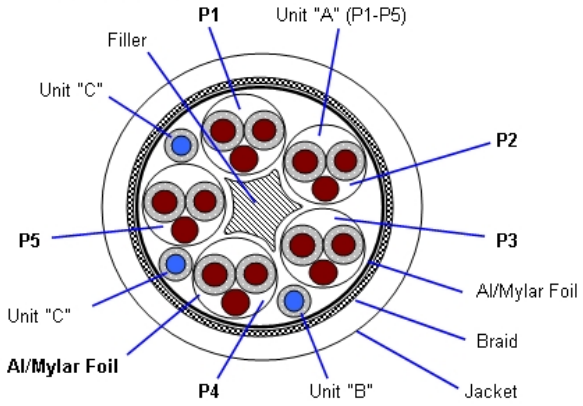
4.1.2 Type of Bulk Cable

The bulk cable must be chosen to meet or exceed all of the electrical and mechanical requirements described below. A reference construction is depicted in Figure 4-2 below.

DisplayPort Cable Mechanical Specifications

Cross Section

Cable construction:



Description

Rated Voltage (V)	30V DC
Rated Temperature (℃)	80 ℃
Product Standard Certification	
Flammability Test	VW-1
Tinned copper wire braiding shield	
PVC jacket	
Dielectric Withstanding Volta	300V AC

Mechanical Characteristics

Test Object	Jacket
Test Material	PVC
Before Tensile Strength (kg/mm2)	≧ 1.05
Aging Elongation (%)	≧ 100
Aging Condition	113±2℃ X 168 hrs
After	≧ 70% of original
Aging	≧ 65% of original
PVC JACKET: NON-MIGRATION (PS)	

Marking

DisplayPort™ Cable Exxxxx-x AWM STYLE 20276 80℃ 30V VW-1 **(Vendor Logo)**

50 mm ± 5

Figure 4-2: Bulk Cable Construction (INFORMATIVE - for reference purpose only)

The following is the description of the reference bulk cable construction. This description is for reference only.

- Overall shielded (braid) structure coated with jacket above
- Unit “A”: P1-P5 ‘STP’ or ‘Twinax’ # 30 AWG insulated stranded conductors, with # 30 AWG drain conductor
- Unit “B”: Unshielded, # 30 AWG single insulated stranded conductor.
- Unit “C”: Unshielded, # 28 or # 30AWG single insulated stranded conductor.

Examples of differences:

1) Wire gauge selection is implementation specific provided the cable specifications of sections 4.1.5 and 4.1.6 are met.
2) A cable that is permanently attached to a DisplayPort device may have less than four Main Link Lanes.

4.1.3 Impedance Profile

The impedance specification must be defined in the time domain. The impedance profile must be measured using a controlled impedance fixture and TDR with a differential sampling head. The fixture rise time must be 50 ps (20% - 80%) or faster while the readout of measurement must be filtered to tr = 130 ps (20% - 80%). Impedance values must conform to those listed in Table 4-1. **Figure 4-3** shows an example of measured data.

Table 4-1: Impedance Profile Values for Cable Assembly

Segment	Differential Impedance Value	Maximum Tolerance	Comment
Fixture	100 Ω	± 10%	Fixture shall have traces lengths of no more than 50 mm (2”)
Connector	100 Ω		
Wire Management	100 Ω		Transition from ± 10% to ± 5% shall have a slop of 5 Ω / 80ps
Cable	100 Ω	± 5%	

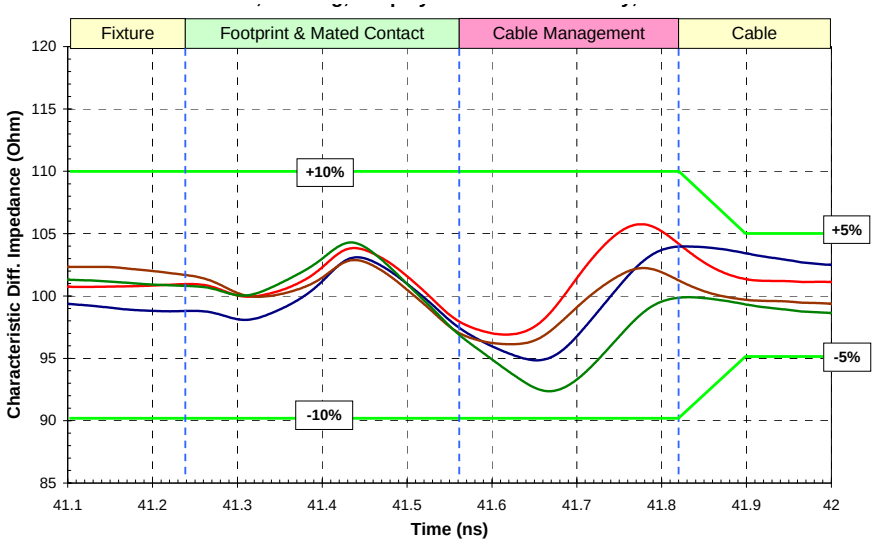


Figure 4-3: Differential Impedance Profile Measurement Data Example

4.1.4 Insertion Loss & Return Loss

Insertion Loss and Return Loss specified in this chapter are the mixed mode S-Parameters known as SDD21 and SDD11, respectively. Unlike Single Ended case, SDDij refers to differential stimulus and differential response as illustrated in the following matrix of all mixed modes in differential case as shown in Table 4-2:

Table 4-2: Mixed Mode Differential / Common relations of S-Parameters

		Stimulus			
		Differential		Common	
Response	Differential	SDD11	SDD12	SDC11	SDC12
		SDD21	SDD22	SDC21	SDC22
	Common	SCD11	SCD12	SCC11	SCC12
		SCD21	SCD22	SCC21	SCC22

4.1.5 High-bit-rate Cable-Connector Assembly Specification

4.1.5.1 Insertion Loss & Return Loss

The following equations represents the reference line that limits the 'Insertion Loss' and 'Return Loss' measured results.

4.1.5.1.1 Insertion Loss Lower Limit for High Bit Rate Cable Assemblies:

$$IL_{\min.}[dB] = \begin{cases} -8.7 \times \sqrt{\dfrac{f}{f_0}} & ; \quad 0.1 < f \le \dfrac{f_0}{3} \\ -4.9 \times \left(\dfrac{3f - f_0}{3} \right) - 5 & ; \quad \dfrac{f_0}{3} < f \le 7 \end{cases}$$

Where:

f is given in *GHz*

f_0 = 1.35 *GHz*

Figure 4-4 depicts the charts that represents the above equations 'Insertion Loss', and must be referenced as the lower limit. The cable assembly measured results must comply with this limit.

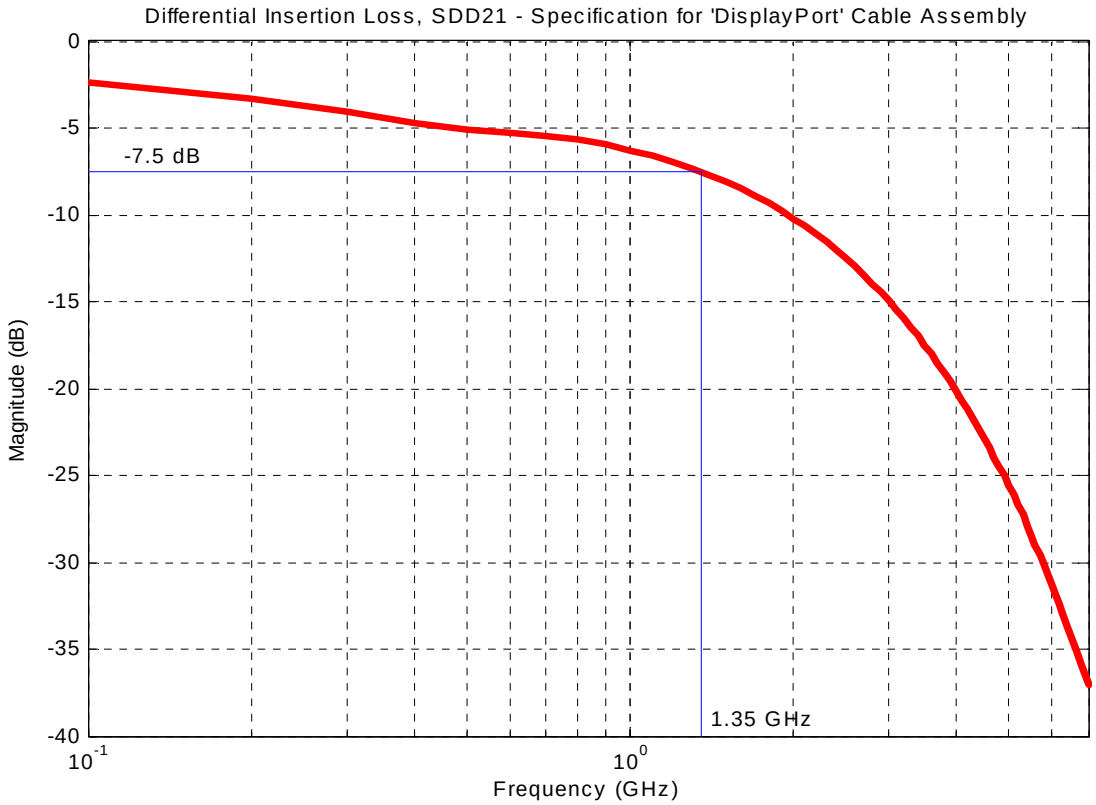


Figure 4-4: Mixed Mode Differential Insertion Loss for High Bit Rate Cable Assembly

4.1.5.1.2 Return Loss Upper Limit for High Bit Rate Cable Assemblies:

$$RL_{\max.}[dB] = \begin{cases} -15 & ; \quad 0.1 < f \le \frac{f_0}{2} \\ -15 + 12.3\, Log_{10}\left(\frac{f}{f_0}\right) & ; \quad \frac{f_0}{2} < f \le 7 \end{cases}$$

Where:

f is given in *GHz*

f_0 = 1.35 *GHz*

Figure 4-5 shows the chart that represents the above 'Return Loss' equation and must be referenced as the upper limit for 'Return Loss'.

The measured cable assembly results must comply with this limit.

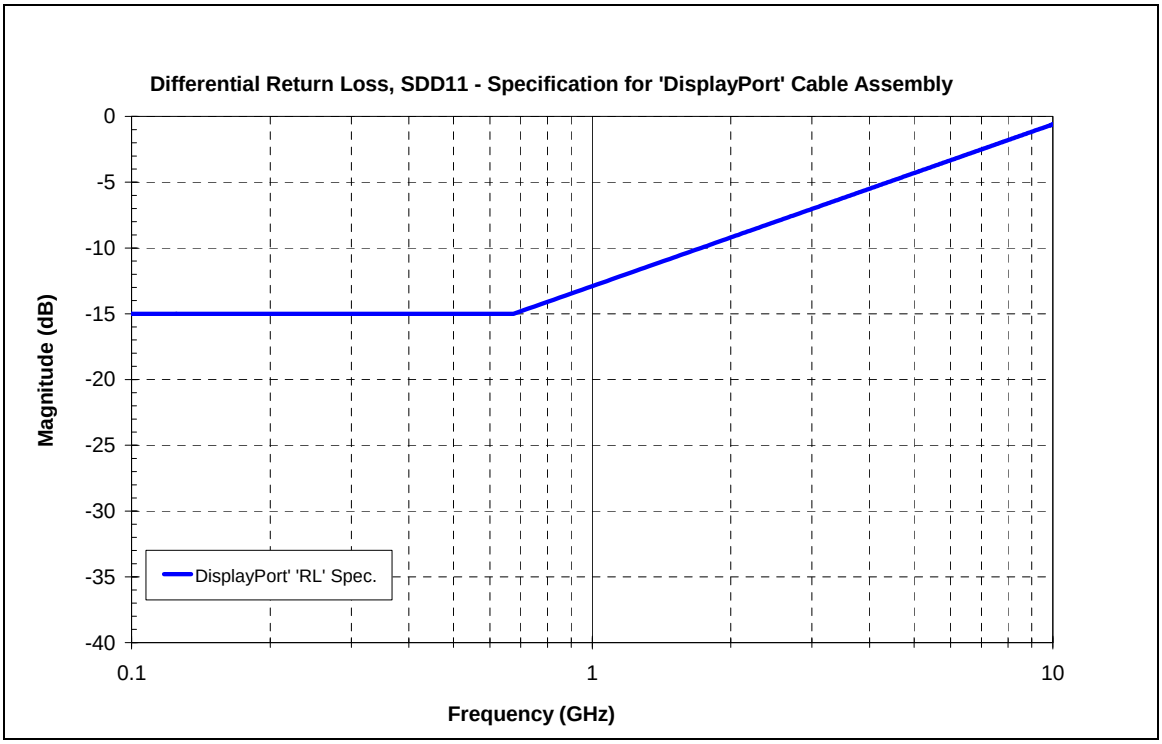


Figure 4-5: Mixed Mode Differential Return Loss for High-bit-rate Cable Assembly

4.1.5.2 Near End Noise (NEN)

Near End Noise (NEN) must be defined in the frequency domain and cover the bandwidth up to 7 GHz. The NEN must be lower than the upper limit in the Isolation equation and depicted in Figure 4-6 below:

Near End Noise - Upper Limit for High Speed Cable Assembly:

$$Isolation_{\max.}[dB] = \begin{cases} -26 & ; \quad 0.1 < f \le f_0 \\ -26 + 15\, Log_{10}\left(\frac{f}{f_0}\right) & ; \quad f_0 < f \le 7 \end{cases}$$

Where:

f is given in *GHz*

f_0 = 1.35 *GHz*

-30

-30

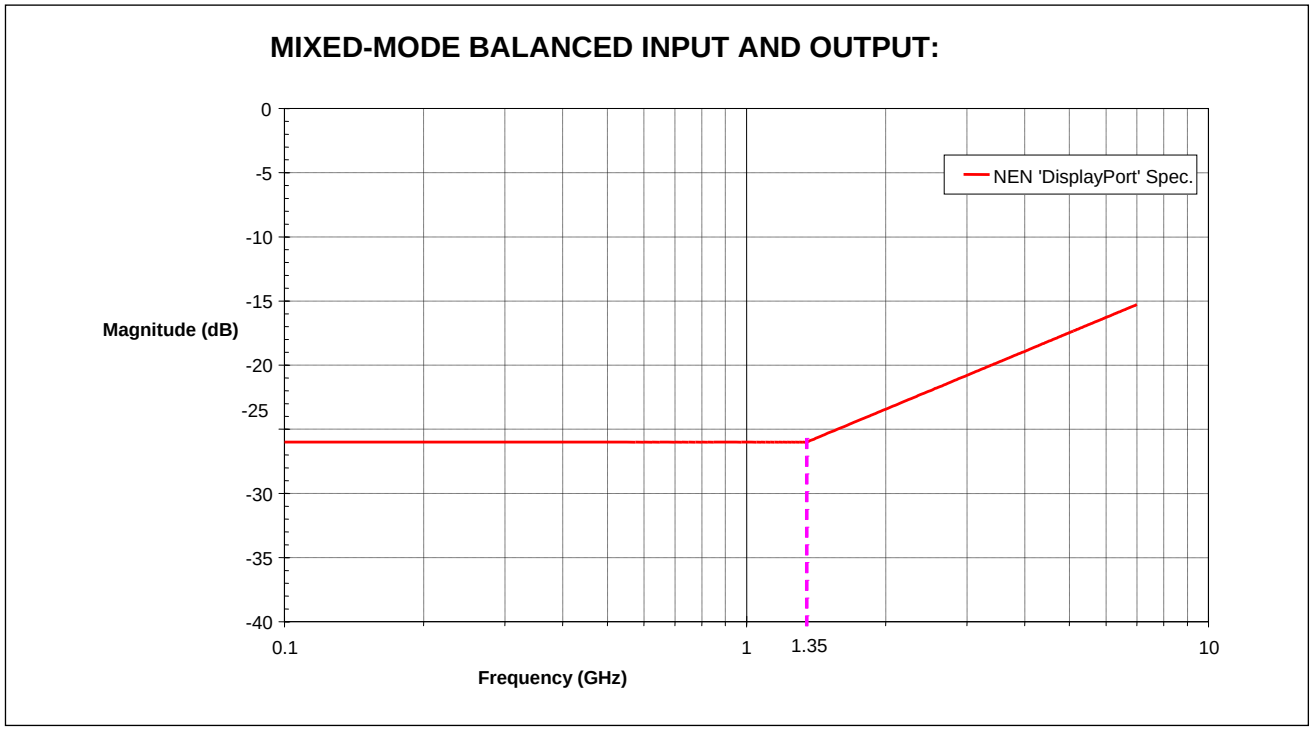


Figure 4-6: Near End Total Noise (peak) for High-bit-rate Cable Assembly

4.1.5.3 Far End Noise (FEN)

The Far End Noise must be lower than the upper limit as depicted in Figure 4-7 below:

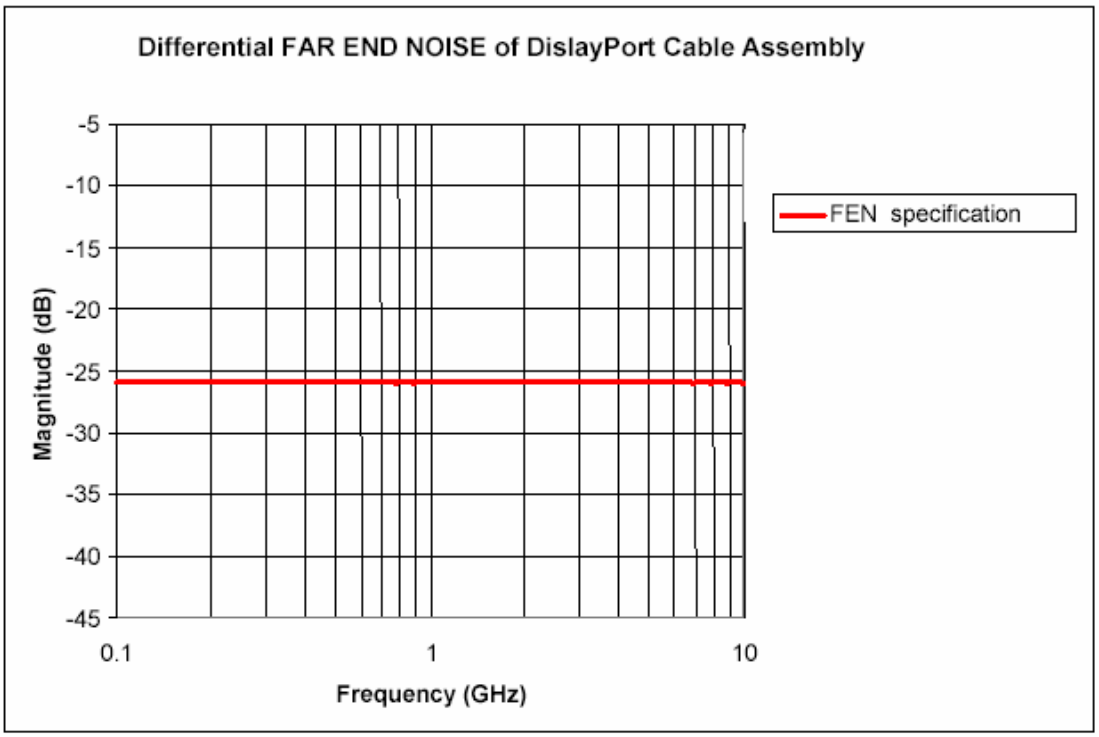


Figure 4-7: Far End Total Noise (peak) for High Bit Rate Cable Assembly

4.1.5.4 Intra and Inter Pair Skew

Both Intra-Pair and Inter-Pair skew are measured in the time domain with Differential TDR at the fixture rise / fall time, i.e. 50 ps measured (20% - 80%).

4.1.5.4.1 Intra-Pair Skew

Intra-Pair skew must be no more than 50 ps and measured as depicted in Figure 4-8 below:

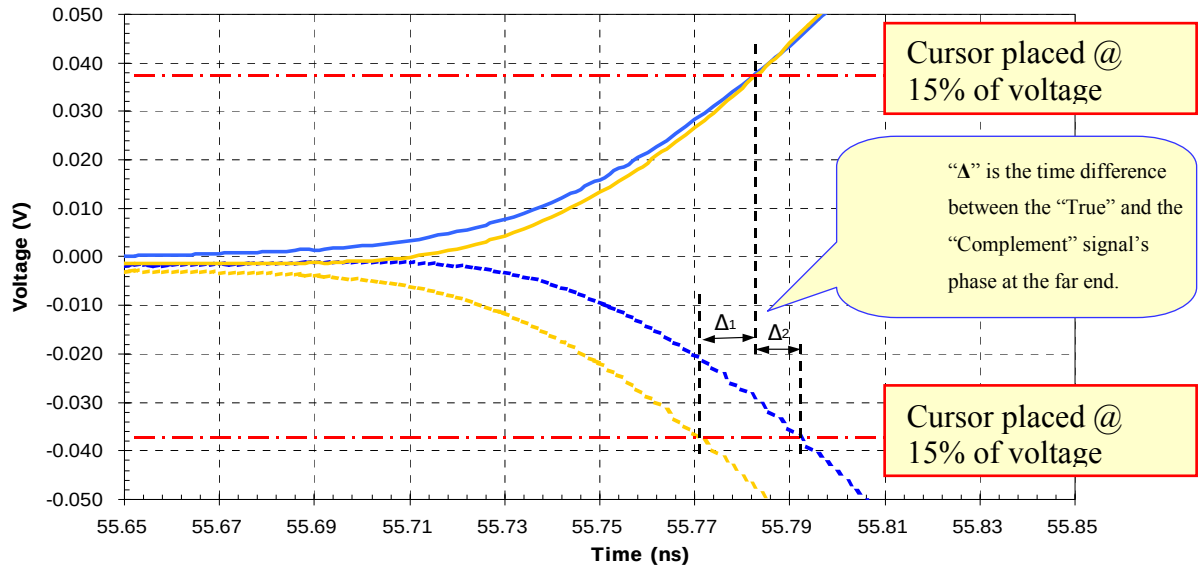


Figure 4-8: Intra-Pair Skew Measurement Method

4.1.5.4.2 Inter-Pair Skew

Inter-Pair skew must be no more than 4 ns and measured as depicted in Figure 4-9 below:

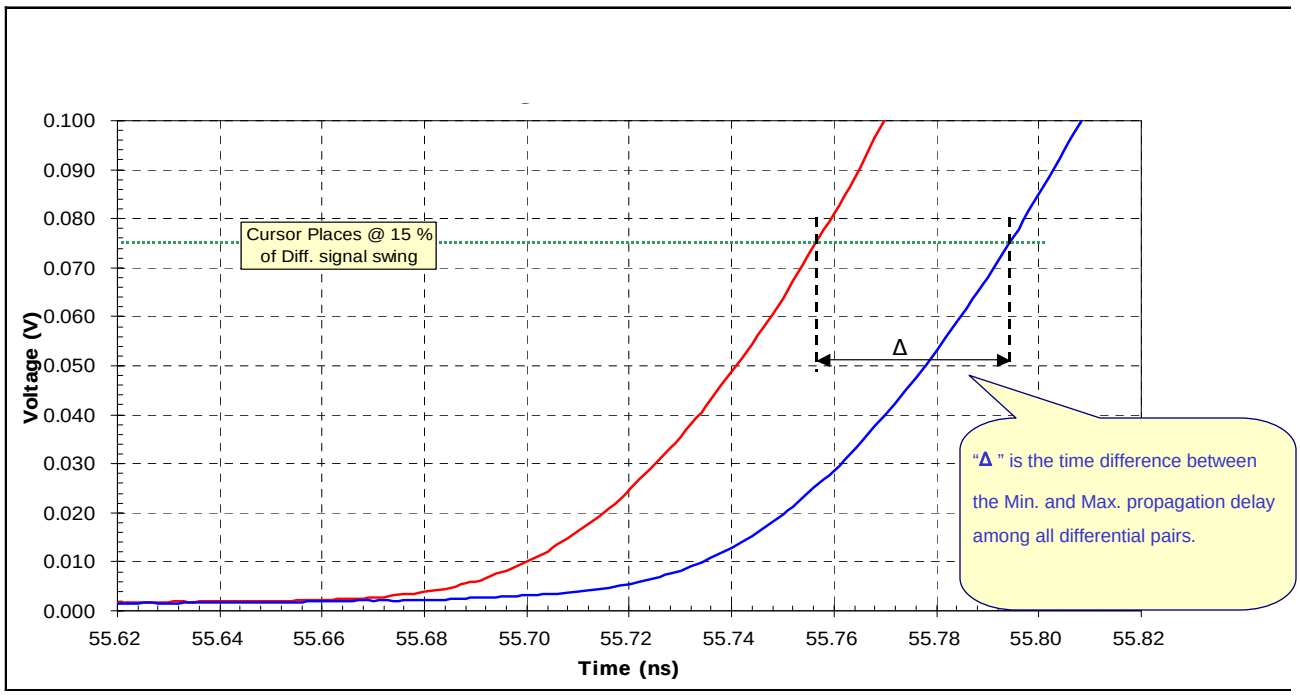


Figure 4-9: Inter-Pair Skew Measurement Method

4.1.6 Reuced Bit Rate Cable-Connector Assembly Specification

4.1.6.1 Insertion Loss & Return Loss

The following equations represents the reference line that limits the 'Insertion Loss' and 'Return Loss' measured results.

4.1.6.1.1 Insertion Loss Lower Limit for Reduced Bit Rate Cable Assembly:

$$IL_{\min.}[dB] = \begin{cases} -1 - 10 \times \sqrt{\frac{f}{f_0}} & ; \quad 0.01 < f \le \frac{f_0}{3} \\ -12 \times \left(\frac{3f - f_0}{3} \right) - 6.8 & ; \quad \frac{f_0}{3} < f \le 3 \end{cases}$$

Where:

f is given in *GHz*

$f_0 = 0.825$ *GHz*

Figure 4-10 shows the chart representing the above 'Insertion Loss' and must be referenced as the lower limit. The measured cable assembly results must comply with this limit.

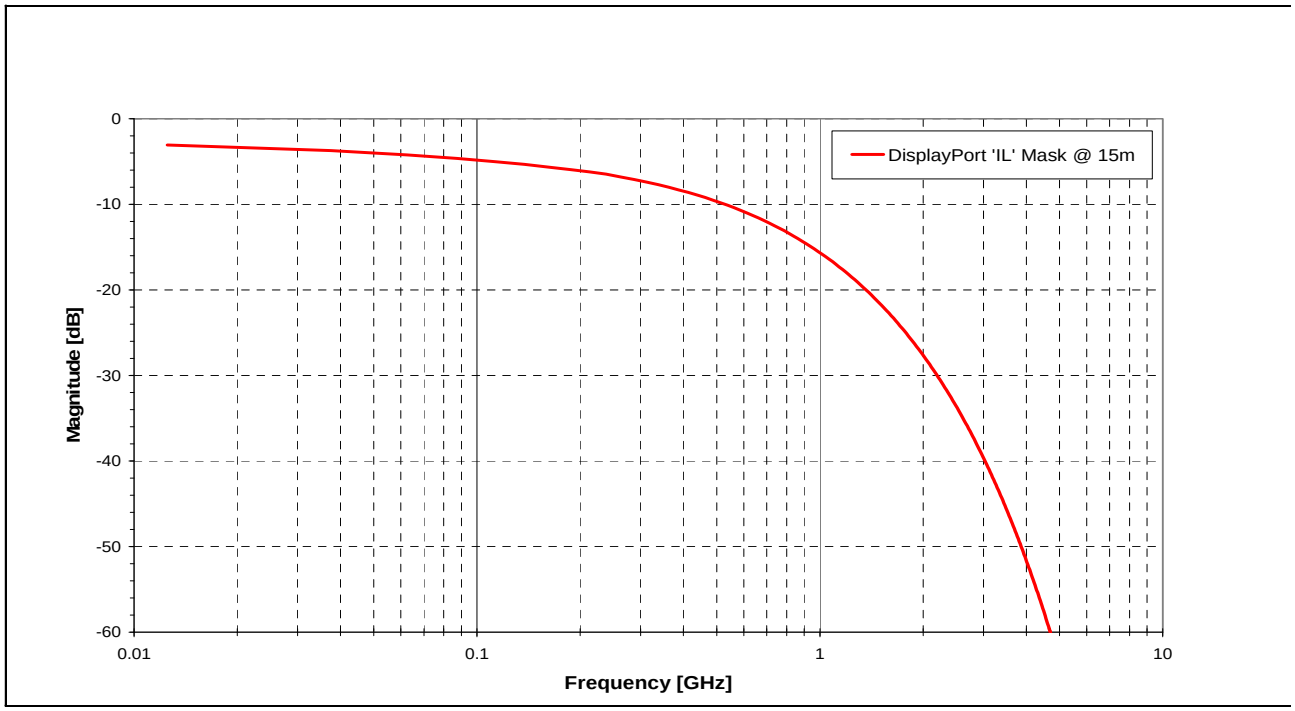


Figure 4-10: Mixed Mode Differential Insertion Loss (SDD21) Mask of Reduced Bit Rate Cable

4.1.6.1.2 Return Loss Upper Limit for Reduced Bit Rate Cable Assembly:

$$RL_{\max.}[dB] = \begin{cases} -20 & ; \quad f \le f_0 \\ -20 + 33\,Log_{10}\left(\frac{f}{f_0}\right) & ; \quad f_0 < f \le 2f_0 \\ -10 + 12.56\,Log_{10}\left(\frac{f}{f_0} \times 0.5\right) & ; \quad 2f_0 < f \le 4 \end{cases}$$

Where:

f is given in *GHz*

$f_0 = 0.8$ *GHz*

Figure 4-11 shows the chart representing the above 'Return Loss' and must be referenced as the upper limit. The cable assembly measured results must comply with these limits.

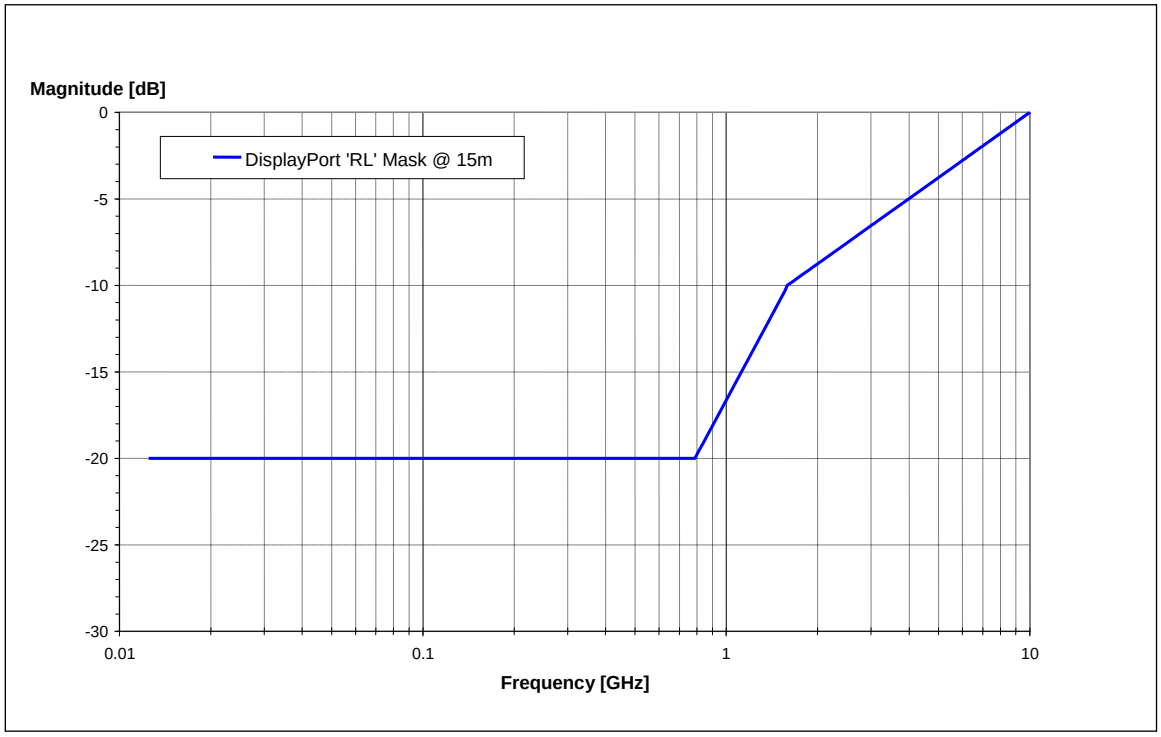


Figure 4-11: Mixed Mode Differential Return Loss (SDD11) of Reduced Bit Rate Cable

4.1.6.2 Near End Noise (NEN)

Near End Noise must be lower than the upper limit in the Isolation equation and depicted in Figure 4-12 below:

Near End Noise - Upper Limit for Reduced Bit Rate Cable Assembly:

$$Isolation_{\max.}[dB] = \begin{cases} -26 & ; \quad 0.1 < f \le f_0 \\ -26 + 15\,Log_{10}\left(\frac{f}{f_0}\right) & ; \quad f_0 < f \le 7 \end{cases}$$

Where:

f is given in GHz

$f_0 = 0.8\ GHz$

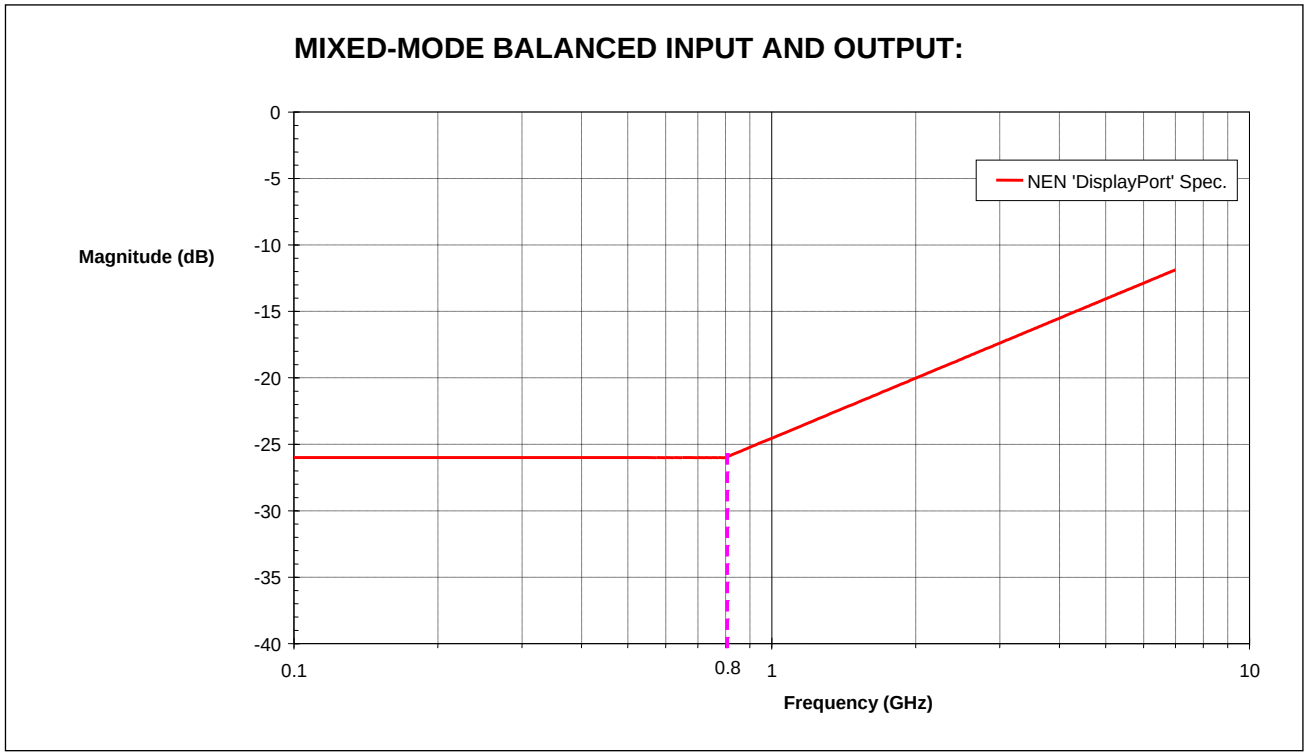


Figure 4-12: Near End Total Noise (peak) for Reduced Bit Rate Cable Assembly

4.1.6.3 Far End Noise (FEN)

Far End Noise must be lower than the upper limit depicted in Figure 4-13 below:

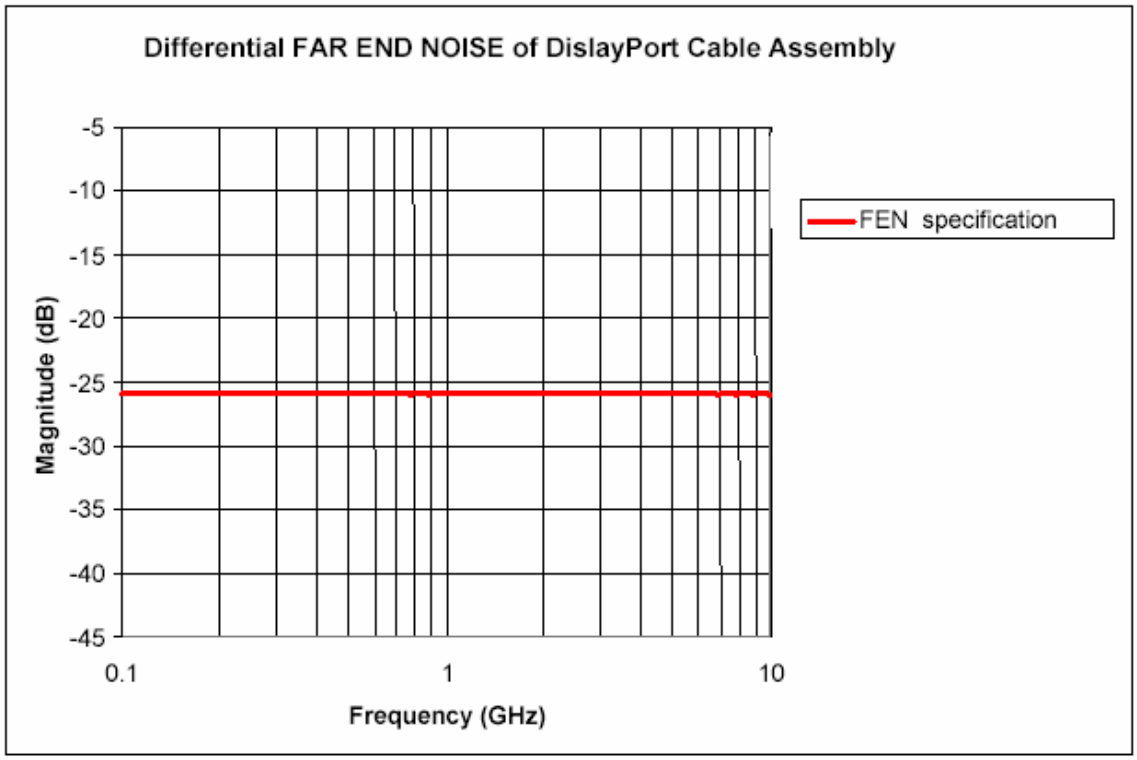


Figure 4-13: Far End Total Noise (peak) for Reduced Bit Rate Cable Assembly

4.1.6.4 Intra-Pair Skew

Intra-Pair Skew is measured in the time domain with Differential TDR at fixture rise / fall time, i.e. 50 ps measured (20% - 80%).

Intra-Pair skew must be no more than 250 ps.

Refer to Figure 4-8 for the measurement method.

4.2 Connector Specification

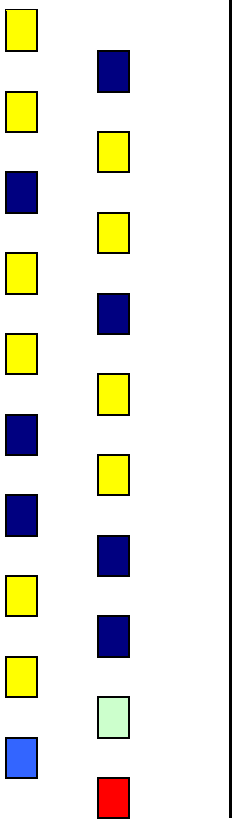
This section describes the specifications of the external and internal DisplayPort connectors.

4.2.1 External connector

4.2.1.1 Connector Pin Assignment

Table 4-3: and Table 4-4 show the pin assignments of the DisplayPort external connectors.

Table 4-3: Source-side Connector Pin Assignment

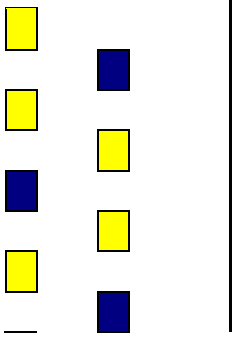
Pin Number	Signal Type	Pin Name	Mating Row Contact Location	Vertically Opposed Connector's Front View
1	Out	ML_Lane 0(p)	Top	
2	GND	GND	Bottom	
3	Out	ML_Lane 0 (n)	Top	
4	Out	ML_Lane 1 (p)	Bottom	
5	GND	GND	Top	
6	Out	ML_Lane 1 (n)	Bottom	
7	Out	ML_Lane 2 (p)	Top	
8	GND	GND	Bottom	
9	Out	ML_Lane 2 (n)	Top	
10	Out	ML_Lane 3 (p)	Bottom	
11	GND	GND	Top	
12	Out	ML_Lane 3 (n)	Bottom	
13	GND (see note 1)	GND	Top	
14	GND (see note 1)	GND	Bottom	
15	I/O	AUX CH (p)	Top	
16	GND	GND	Bottom	
17	I/O	AUX CH (n)	Top	
18	In	Hot Plug Detect	Bottom	
19	RTN	Return	Top	
20	PWR Out (see note 2)	DP_PWR	Bottom	

Notes:

1) Pins 13 and 14 may either be directly connected to ground or connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low impedance ground path from these pins.

2) Pin 20, PWR Out, must provide between 3.0 volts and +16.0V with a maximum current of 500 mA and a minimum power capability of 1.5 watts.

Table 4-4: Sink-side Connector Pin Assignment

Pin Number	Signal Type	Pin Name	Mating Row Contact Location	Vertically Opposed Connector's Front View
1	In	ML_Lane 3(n)	Top	
2	GND	GND	Bottom	
3	In	ML_Lane 3 (p)	Top	
4	In	ML_Lane 2 (n)	Bottom	
5	GND	GND	Top	
6	In	ML_Lane 2 (p)	Bottom	
7	In	ML_Lane 1 (n)	Top	
8	GND	GND	Bottom	

Pin Number	Signal Type	Pin Name	Mating Row Contact Location	Vertically Opposed Connector's Front View
9	In	ML_Lane 1 (p)	Top	
10	In	ML_Lane 0 (n)	Bottom	
11	GND	GND	Top	
12	In	ML_Lane 0 (p)	Bottom	
13	GND (see note 1)	GND	Top	
14	GND (see note 1)	GND	Bottom	
15	I/O	AUX CH (p)	Top	
16	GND	GND	Bottom	
17	I/O	AUX CH (n)	Top	
18	Out	Hot Plug Detect	Bottom	
19	RTN	Return	Top	
20	Power Out (see note 2)	DP_PWR	Bottom	

Notes:

1) Pins 13 and 14 may either be directly connected to ground or connected to ground through a pull-down device. External devices and cable assemblies must be designed to not rely on a low impedance ground path from these pins.

2) Pin 20, PWR Out, must provide +3.3 volts ± 5% with a maximum current of 500 mA and a minimum power capability of 1.5 watts.

Figure 4-14 shows the wiring of an external cable connector assembly. The standard external cable connector assembly must not have a wire on pin 20, DP_PWR.

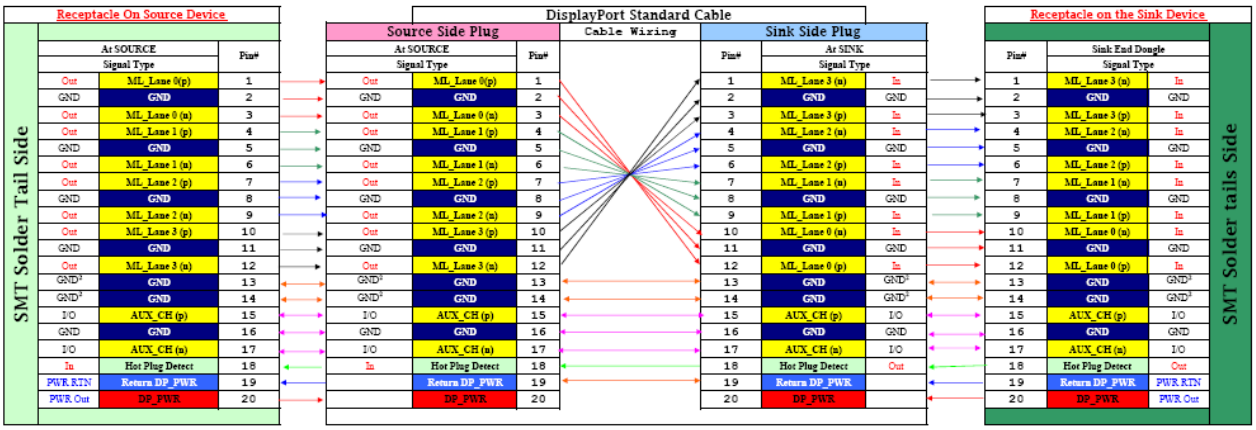


Figure 4-14: External Cable Connector Assembly Wiring

4.2.1.2 Contact Sequence

Table 4-5 shows the legend for signal name / type mating level.

Table 4-5: Mating Sequence Level

Signal Type			Level
Connector Shell			First Mate
DP_PWR	Return	GND	Second Mate
Auxiliary (+) / (-)	ML_Lane (i) (+) / (-)	Hot Plug Detect	Third Mate

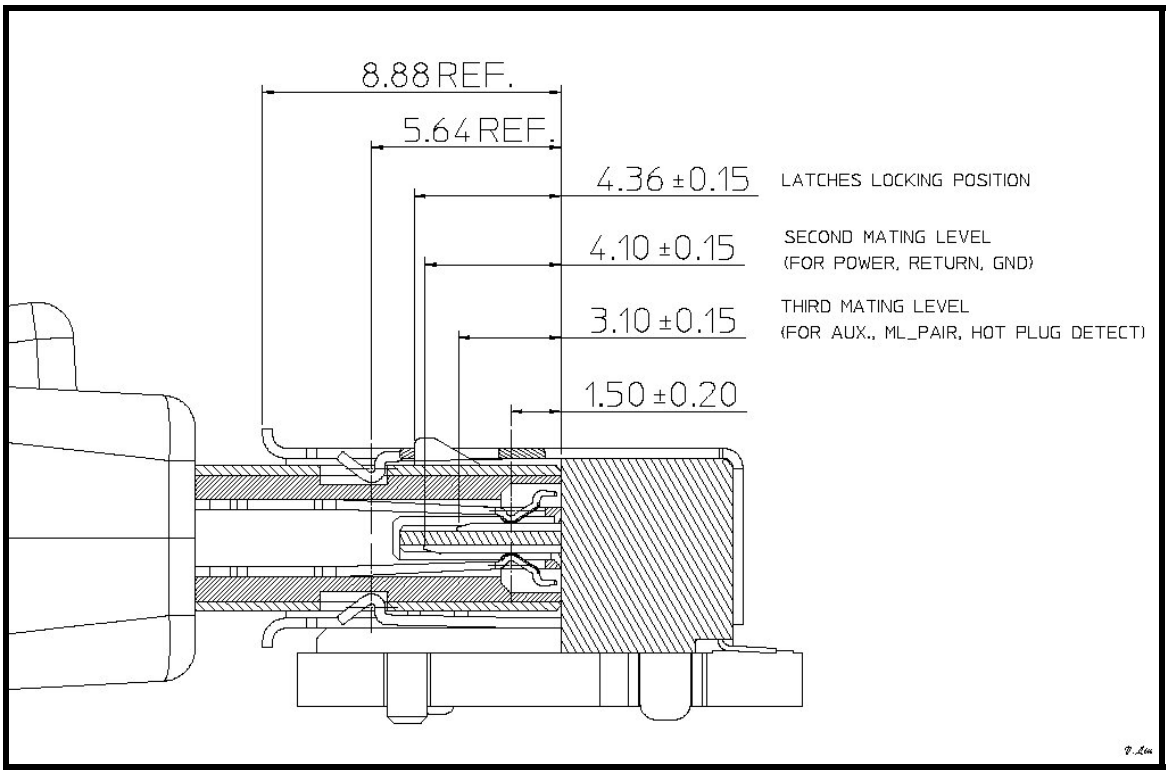


Figure 4-15: Connector Mating Levels

4.2.1.3 Connector Mechanical Performance

Table 4-6 below shows the mechanical performance requirements for a DisplayPort external connector.

Table 4-6: Connector Mechanical Performance

Item	Test Condition	Requirement	
Vibration	Amplitude: 1.52 mm P-P or 147 m/s^2 {15G} Sweep time: 50-2000-50Hz in 20 minutes. Duration: 12 times in each of X, Y, Z axes (Total of 36 times) Electrical load: DC 100 mA current must be conducted during the test. (ANSI/EIA-364-28 Condition III Method 5A)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value: 30 mΩ maximum. Shell Part: Change from initial value: 50 mΩ maximum.
		Discontinuity	1 µs maximum.
Durability	Measure contact and shell resistance after the following. Automatic cycling : 10,000 cycles at 100 ± 50 cycles per hour (ANSI/EIA-364-09)	Contact Resistance	Contact: Change from initial value: 30 mΩ maximum. Shell Part: Change from initial value: 50 mΩ maximum.
Insertion / Withdrawal Force (no latches)	Insertion and withdrawal speed: 25 mm / minute. (ANSI/EIA-364-13)	Withdrawal force	9.8 N {1.0kgf} minimum 39.2 N {4.0kgf} maximum
		Insertion force	44.1 N {4.5kgf} maximum
Latch Strength	Mate connectors, apply axial pull-out force at a rate of 13 mm / minute until the latch is disengaged or damaged. (ANSI/EIA-364-98)	Appearance	No damage on either part of connector
		Pull force	49.0 N {5.0kgf} minimum
Cable Flex	100 cycles in each of 2 planes. Dimension: X = 3.7 x Cable Diameter. (ANSI/EIA-364-41, Condition I)	Discontinuity	1 µs maximum.
		Dielectric Withstanding Voltage and Insulation Resistance.	Conform to item of dielectric withstanding voltage and insulation resistance

4.2.1.4 Connector Electrical Performance

Table 4-7 below shows the electrical performance requirements for a DisplayPort external connector.

Table 4-7: Connector Electrical Performance

Item	Test Condition	Requirement
Low Level Contact Resistance	Mated connectors, Contact: measured by dry circuit, 20 mVolts maximum, and 10mA. Shell: measured by open circuit, 5 Volts maximum, 100mA. (ANSI/EIA-364-23)	Contact: Change from initial value = 30 mΩ maximum Shell: Change from initial value = 50 mΩ maximum
Dielectric Strength	Unmated connectors, apply 500 Volts AC (RMS.) between adjacent terminal and ground. (ANSI/EIA 364-20,Method 301) Mated connector, apply 300 Volts AC (RMS.) between adjacent terminal and ground.	No Breakdown
Insulation Resistance	Unmated connectors, apply 500 Volts DC between adjacent terminal and ground. (ANSI/EIA 364-21,Method 302)	Unmated: 100 MΩ minimum
	Mated connectors, apply 150 Volts DC between adjacent terminal and ground.	Mated: 10 MΩ minimum
Contact Current Rating	55 °C, maximum ambient 85 °C, maximum temperature change (ANSI/EIA-364-70,TP-70)	0.5 A minimum
Applied Voltage Rating	40 Volts AC (RMS.) continuous maximum, on any signal pin with respect to the shield.	No Breakdown
Electrostatic Discharge	Test unmated connectors from 1 kVolt to 8 kVolts in 1 kVolt steps using 8mm ball probe. (IEC61000-4-2)	No evidence of discharge to contacts at 8kVolts

4.2.1.5 Connector Environment Performance

Table 4-8 below shows the environment performance requirements for a DisplayPort external connector.

Table 4-8: Connector Environment Performance

Item	Test Condition	Requirement	
Thermal Shock	10 cycles of: a) -55°Cfor 30 minutes b) +85°C for 30 minutes (ANSI/EIA-364-32, Condition I)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value: 30 mΩ maximum. Shell Part: Change from initial value: 50 mΩ maximum.
Humidity	A) Mate connectors together and perform the test as follows: Temperature : +25 to +85°C Relative Humidity : 80 to 95% Duration : Four cycles (96 hours) Upon completion of the test, specimens must be conditioned at ambient room conditions for 24 hours, after which the specified measurements must be performed. (ANSI/EIA-364-31)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value: 30 mΩ maximum. Shell Part: Change from initial value: 50 mΩ maximum.
	B) Unmate connectors and perform the test as follows: Temperature : +25 to +85°C Relative Humidity : 80 to 95% Duration : Four cycles (96 hours) Upon completion of the test, specimens must be conditioned at ambient room conditions for 24 hours, after which the specified measurements must be performed. (ANSI/EIA-364-31)	Appearance	No Damage
		Dielectric Withstanding Voltage and Insulation Resistance	Conform to item of Dielectric Withstanding Voltage and Insulation Resistance
Thermal Aging	Mate connectors and expose to (+105 ± 2)°C for 250 hours. Upon completion of the exposure period, the test specimens must be conditioned at ambient room conditions for one to two hours after which the specified measurements must be performed. (ANSI/EIA-364-17, Condition 4, Method A)	Appearance	No Damage
		Contact Resistance	Contact: Change from initial value: 30 mΩ maximum. Shell Part: Change from initial value: 50 mΩ maximum.

4.2.1.6 Connector Performance Test Sequence

To evaluate the connector performance, the test sequence must follow the test groups 1, 2, 3 and 7 in the ANSI/EIA Standard (EIA-364-1000.01).

4.2.1.7 Connector Drawings (Per Molex Connector P/N: 47272-0001)

Figure 4-16 below shows the DisplayPort external connector. All dimensions are in mm.

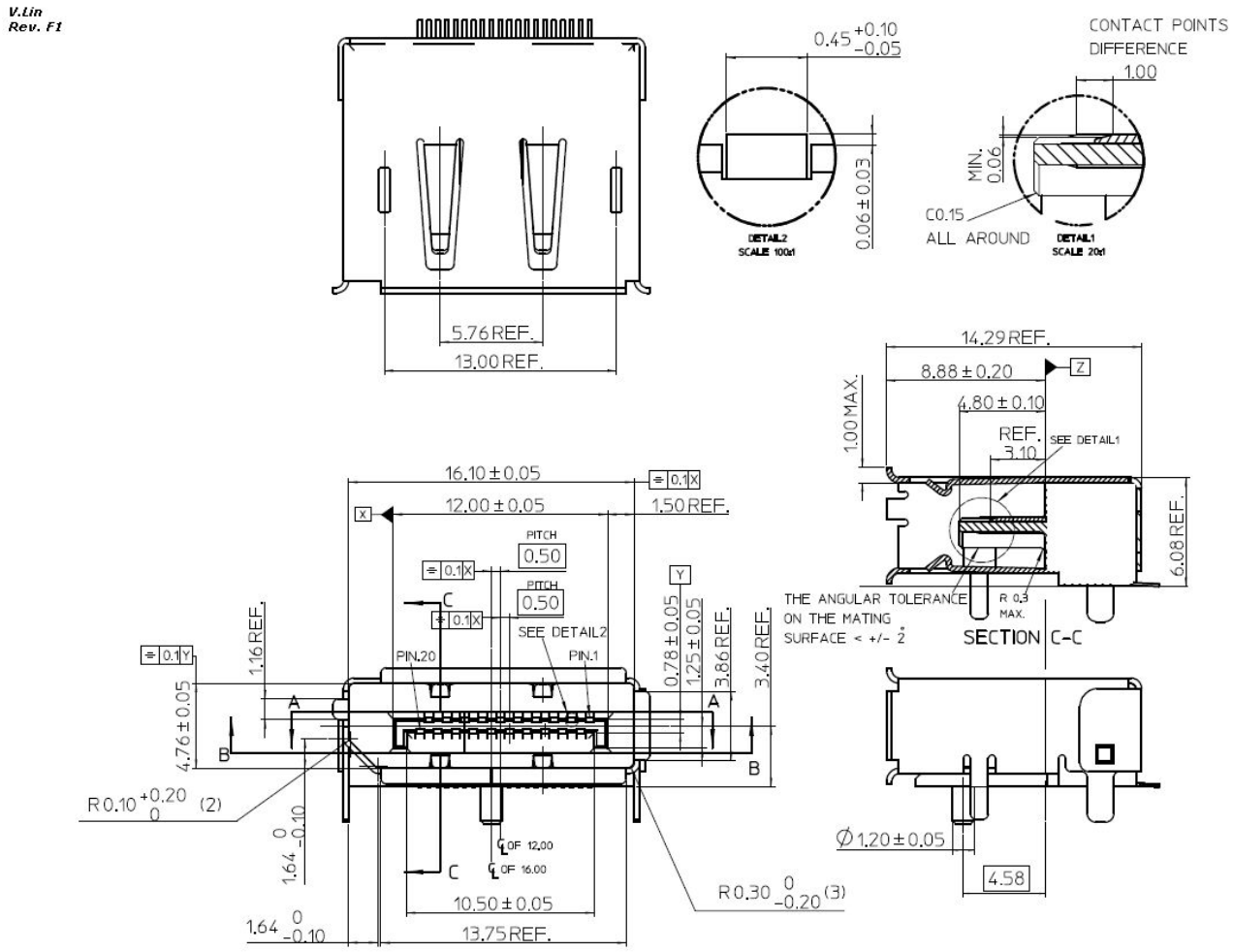


Figure 4-16: DisplayPort External Connector Drawings

*4.2.1.8 Cable Connector Drawings (Per Molex Connector P/N: 68783-****)*

Figure 4-17 below shows the DisplayPort external cable-connector assembly.

Recommendations for plug connector construction:

- Locate the thumb button on the opposite side to the interface chamfer corner.
- Provide the thumb button on the plug's top cover whether latches are fitted or not. This will provide the user with a good indicator of plug orientation.
- A plug without latches may have an alternate feature providing the same orientation indicator as the thumb button of the standard plug.

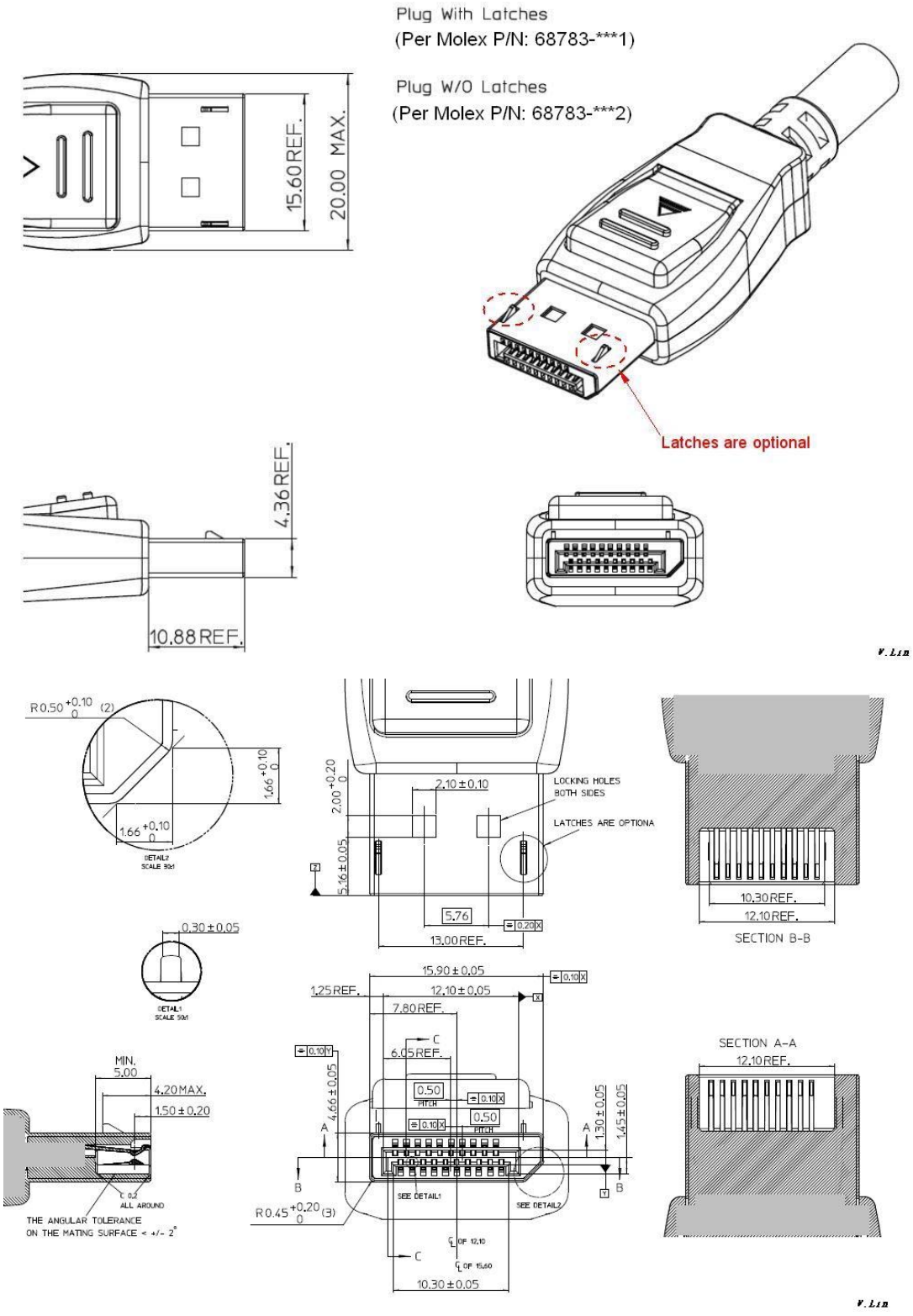


Figure 4-17: DisplayPort External Cable-Connector Assembly Drawings

Figure 4-18 shows the recommended orientations of the external connector.

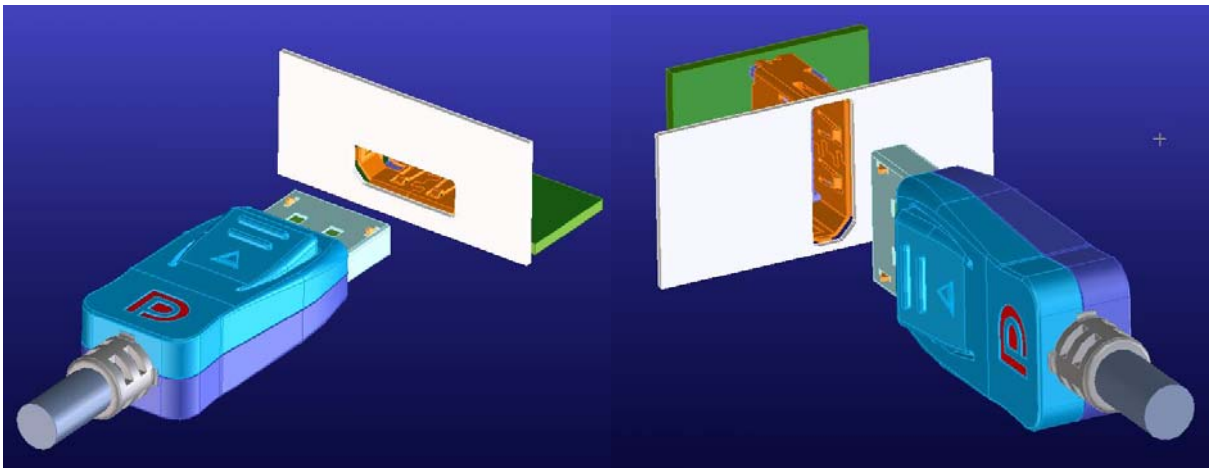


Figure 4-18: Recommended Orientation of External Connector

4.2.1.9 Plug Connector and Board Connector Full-mated Condition

Figure 4-19 below shows the fully mated condition of the plug and the board connectors.

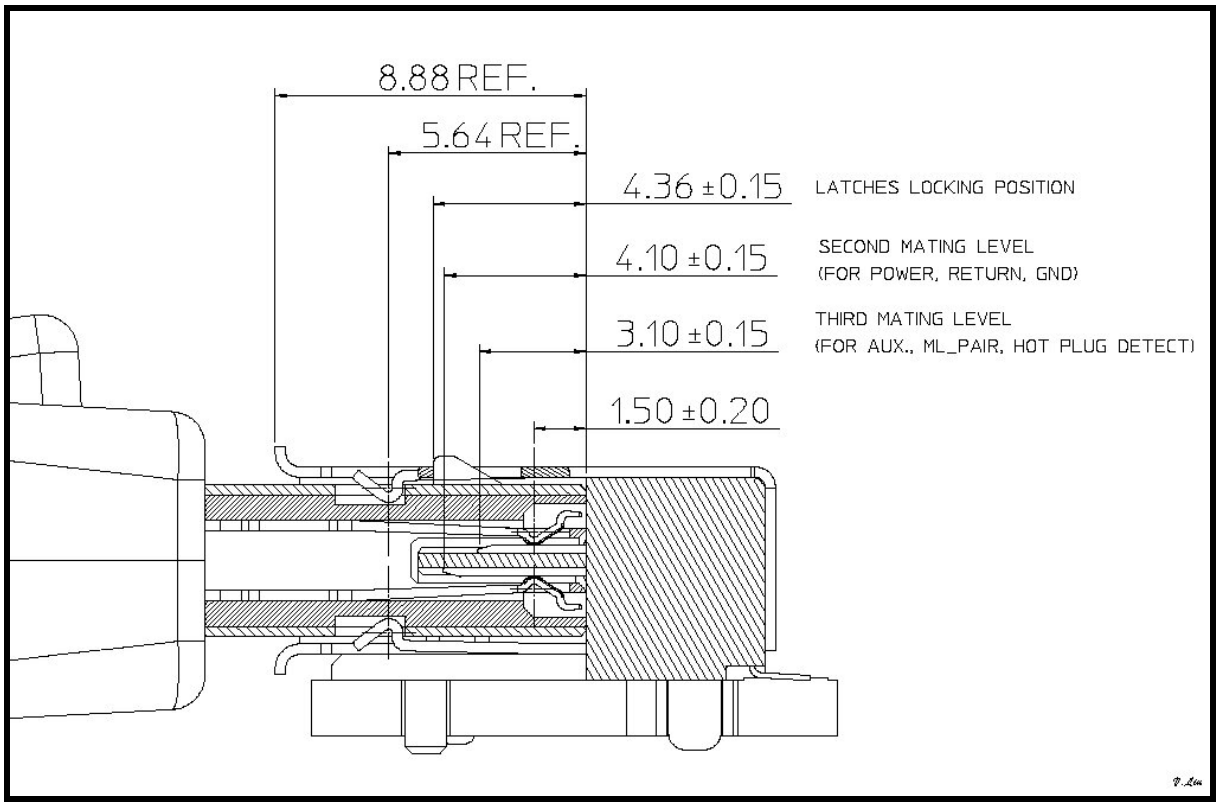


Figure 4-19: Fully-mated Condition for DisplayPort External Connectors

4.2.1.10 Recommended PCB Layout

Figure 4-20 below shows the DisplayPort external cable-connector assembly.

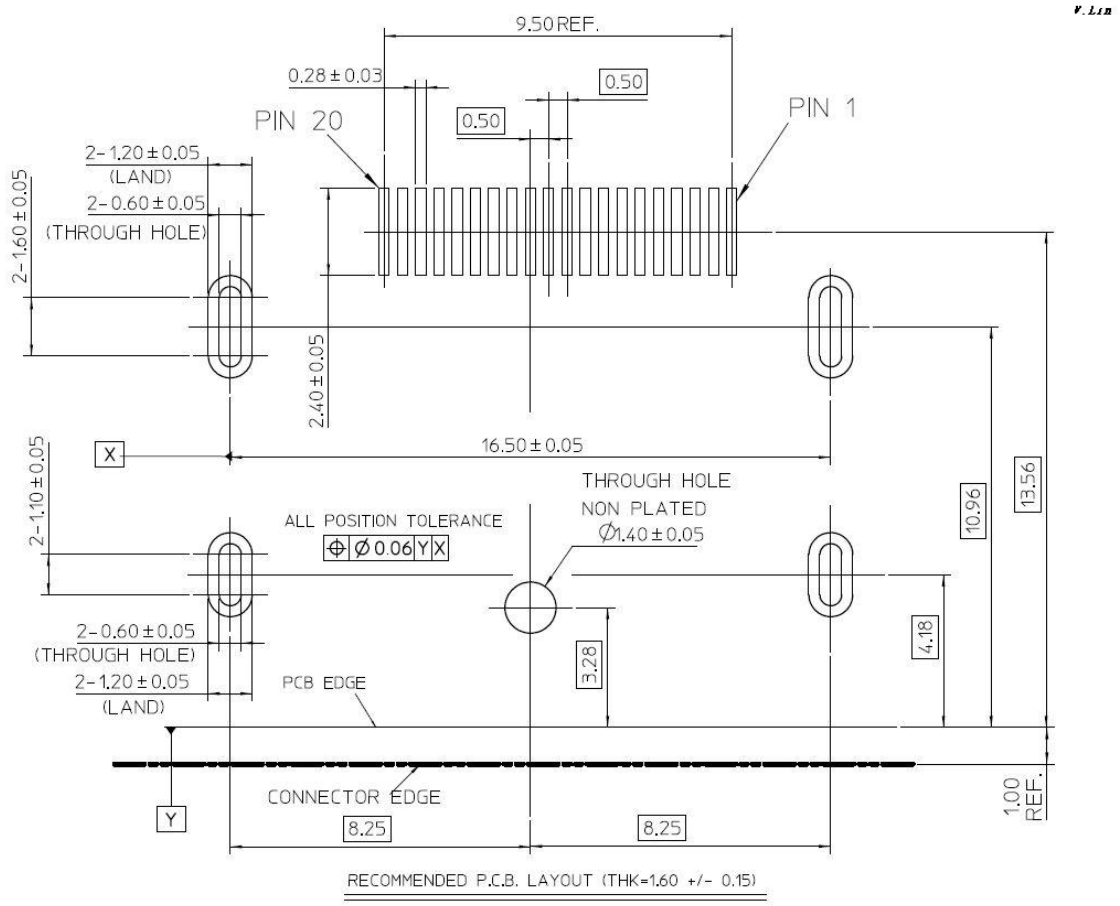


Figure 4-20: Recommended PCB Layout for DisplayPort External Connector

4.2.1.11 Reference Design for Four DisplayPort External Connectors on a PCI Card

Figure 4-21 is a reference application design for four external connectors on a standard PCI card.

Figure 4-22 shows the panel cut-out reference dimensions.

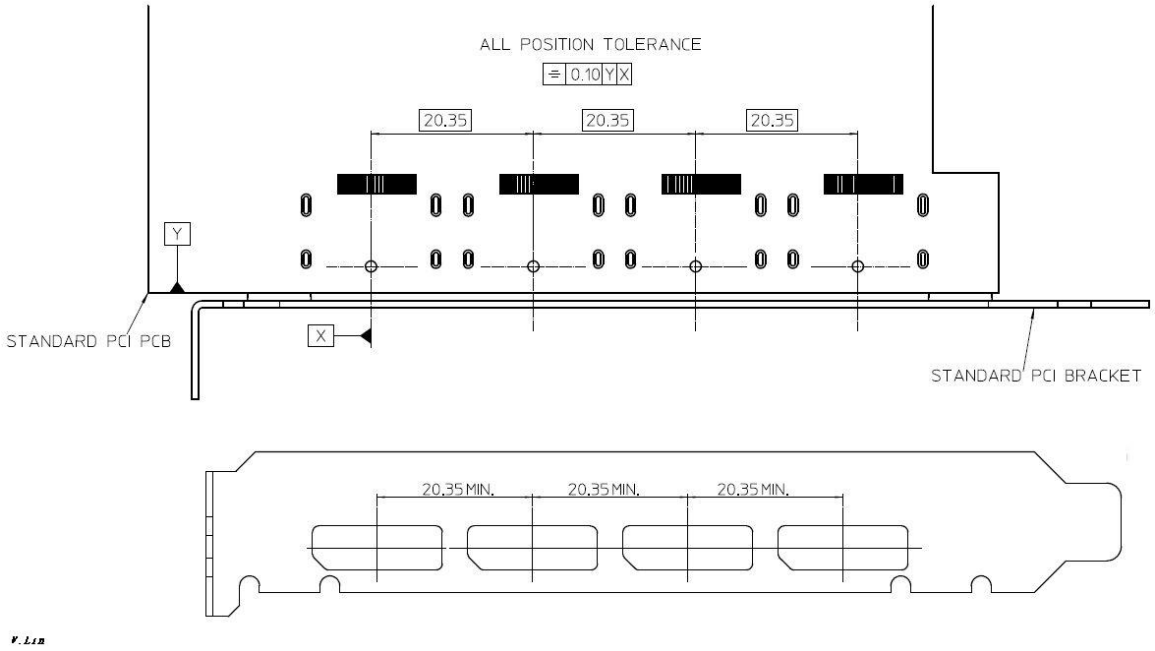


Figure 4-21: Reference Design for Four DisplayPort External Connectors on a PCI Card

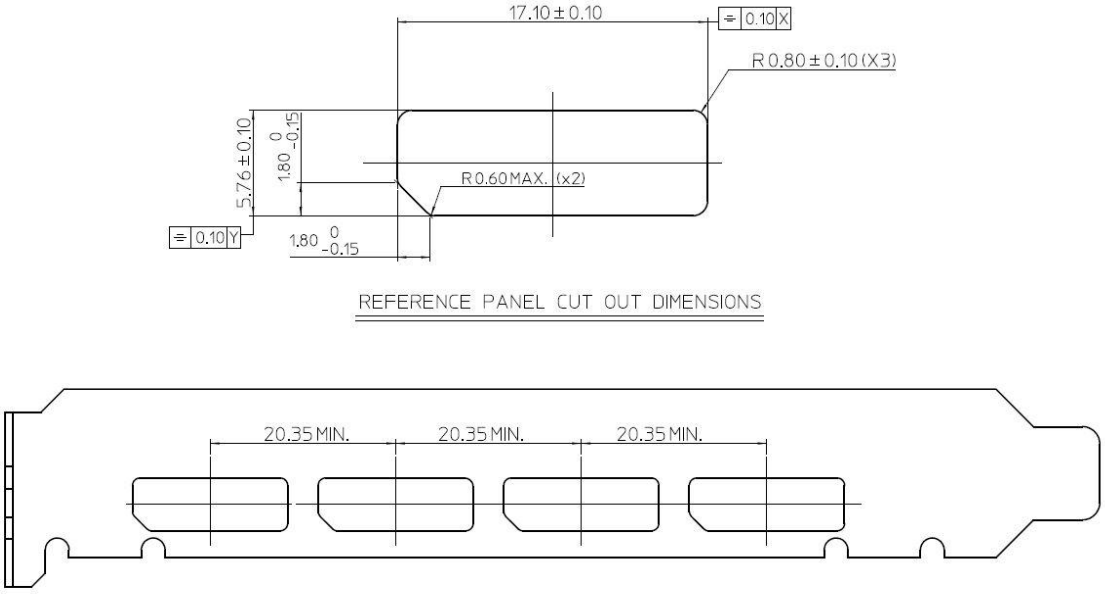


Figure 4-22: Panel Cut Out Reference Dimensions

4.2.2 Panel-side Internal Connector

This section covers the specifications for DispayPort panel-side internal connector.

The panel-side internal connector consist of a two piece, 30 position, low profile, cable-to-board, co-planar connector. One piece terminates the cable (Plug) and the other is attached to the PCB (Receptacle).

The connector supports up to four Main Link lanes (Lane 0 - Lane 3). In an embedded connection, the cable connector assembly may support one, two, or four lanes depending on the bandwidth requirement of the application.

For one lane and two lane Main Link configurations, the stuffing rule must be:

- When only two lanes are needed, Lane 0 and Lane 1 must be populated while Lane 2 and Lane 3 are unpopulated.
- When only one lane is needed, Lane 0 must be populated while Lane 1 to Lane 3 are unpopulated.

Only the panel TCON (timing controller) side of the connector is defined in this specification. While some cables may have the same connectors on both ends of the cable-connector assembly, others may have more pins for the Source Device side (that is, the side of graphics processor, LCD controller, etc.) for LCD backlight control, for instance.

4.2.2.1 Panel-side Internal Connector Pin Assignment

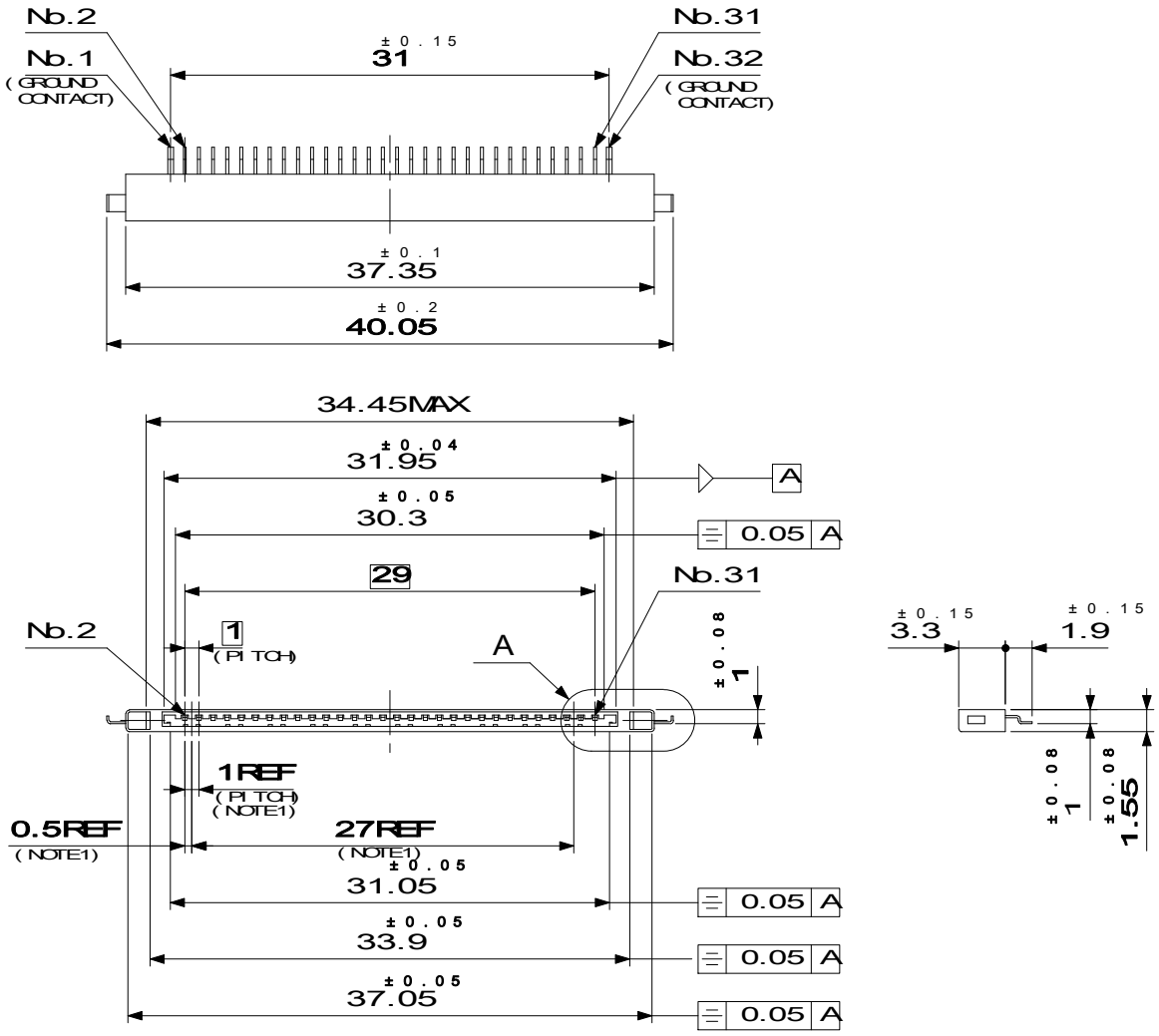
DisplayPort Panel-side Internal Connector Pin Assignment below shows the pin assignment of the DisplayPort panel-side internal connector. Pin assignment of those pins other than the DispayPort Main Link and AUX CH in Table 4-9 is for reference purpose only.

Table 4-9: DisplayPort Panel-side Internal Connector Pin Assignment

Pin #	Pin Name	Pin Definition
1		Optional (Outer shell connection - not a signal contact)
2	Reserved	
3	LCDVCC	Power to LCD panel. Controlled on graphics card and is removed when LCD is off.
4	LCDVCC	
5	LCDVCC	
6	LCDVCC	
7	GND	Power Return (Ground)
8	GND	
9	GND	
10	GND	
11	Hot Plug Detect	Hot Plug Detect
12	Reserved	
13	Reserved	
14	H_GND	High Speed (Main Link) Ground
15	ML_Lane 3(n)	'Complement' Signal-Main Link Lane 0
16	ML_Lane 3(p)	'True' Signal-Main Link Lane 0
17	H_GND	High Speed (Main Link) Ground
18	ML_Lane 2(n)	'Complement' Signal-Main Link Lane 0
19	ML_Lane 2(p)	'True' Signal-Main Link Lane 0
20	H_GND	High Speed (Main Link) Ground
21	ML_Lane 1(n)	'Complement' Signal-Main Link Lane 0
22	ML_Lane 1(p)	'True' Signal-Main Link Lane 0
23	H_GND	High Speed (Main Link) Ground
24	ML_Lane 0(n)	'Complement' Signal-Main Link Lane 0
25	ML_Lane 0(p)	'True' Signal-Main Link Lane 0
26	H_GND	High Speed (Main Link) Ground
27	AUX CH (p)	'True' Signal – Auxiliary channel
28	AUX CH (n)	'Complement' Signal – Auxiliary channel
29	H_GND	High Speed (Main Link) Ground
30	AUX_PWR	+3.3V "trickle" power to enable AUX CH for DPCD / EDID access
31	Reserved	
32		Optional (Outer shell connection - not a signal contact)

4.2.2.2 Panel-side Internal Receptacle Connector

Figure 4-23 (which straddles two pages) and Figure 4-24 show the DisplayPort panel-side internal PCB receptacle connector and the recommended footprint layout, respectively.



Note 1 : This dimension shows ground contact

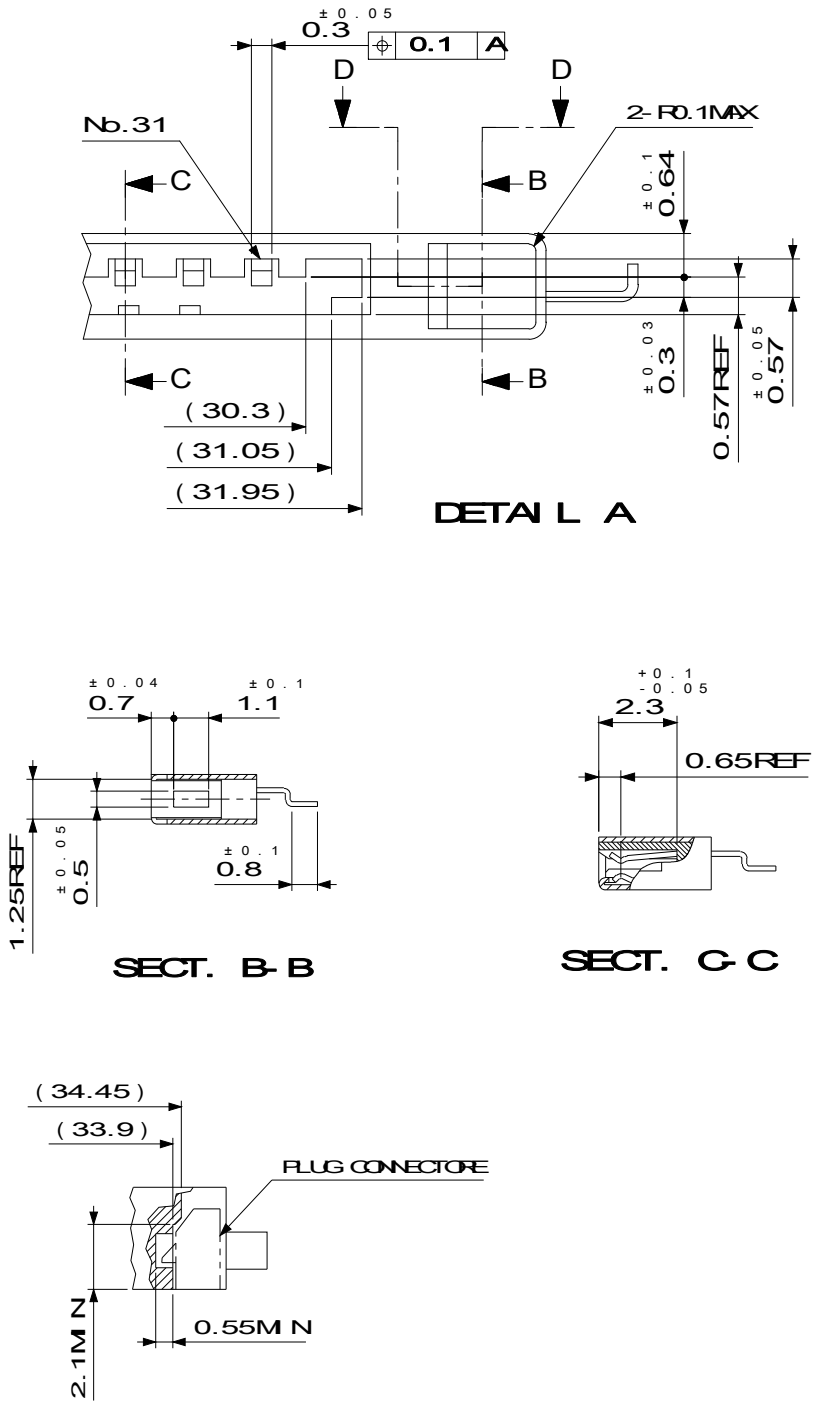


Figure 4-23: Panel-side Internal PCB Mount Receptacle Connector (in unit of mm)

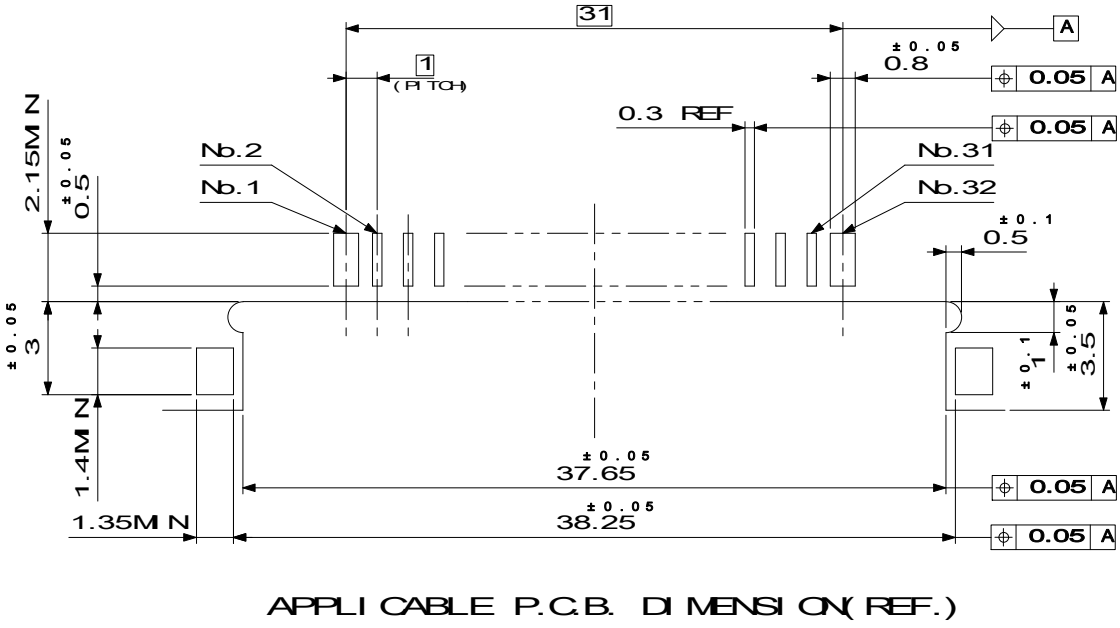


Figure 4-24: PCB mount Connector Recommended Footprint Layout (in unit of mm)

4.2.2.3 Panel-side Internal Plug Connector

Figure 4-25 shows the DisplayPort panel-side internal cable plug connector.

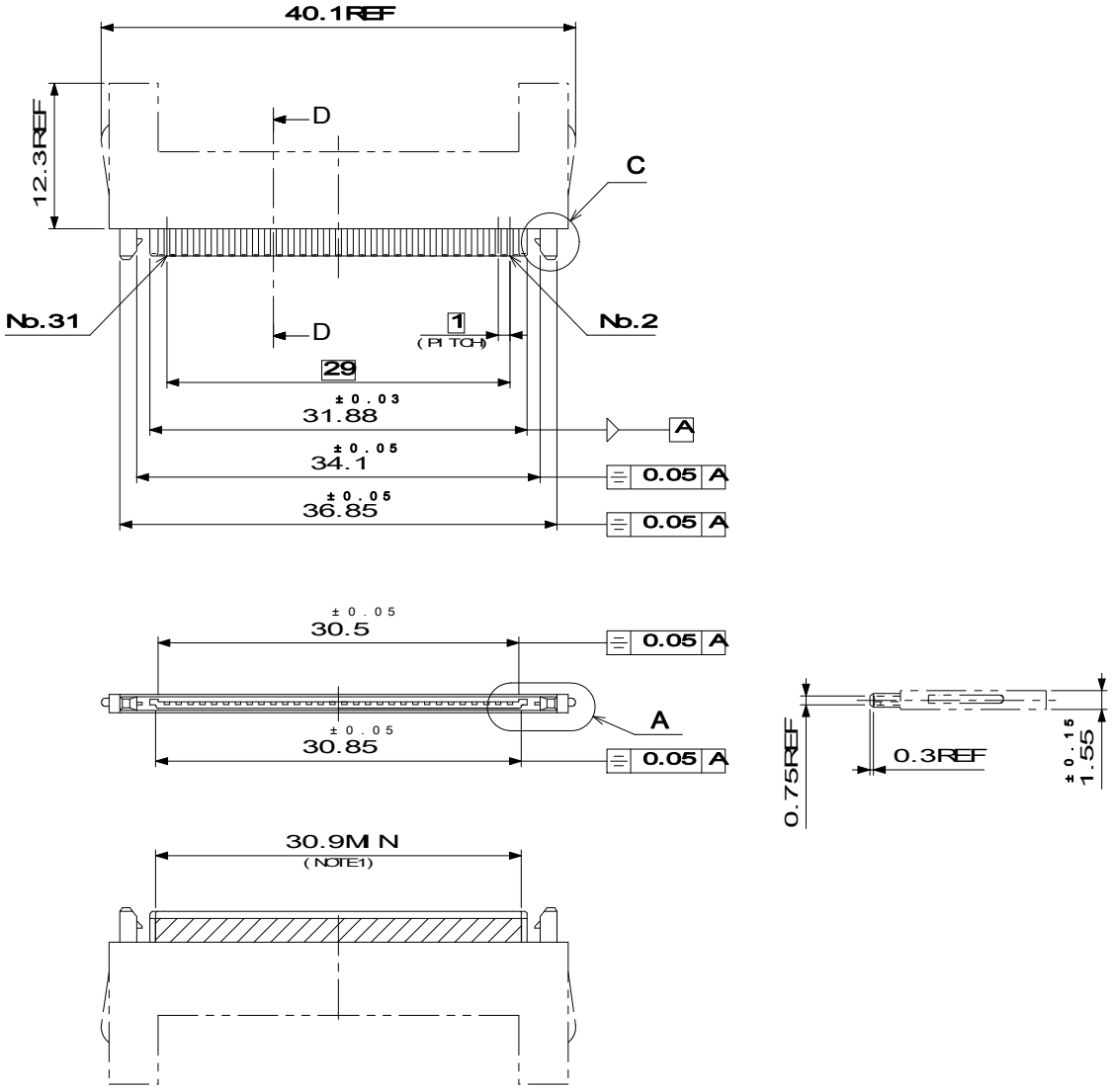
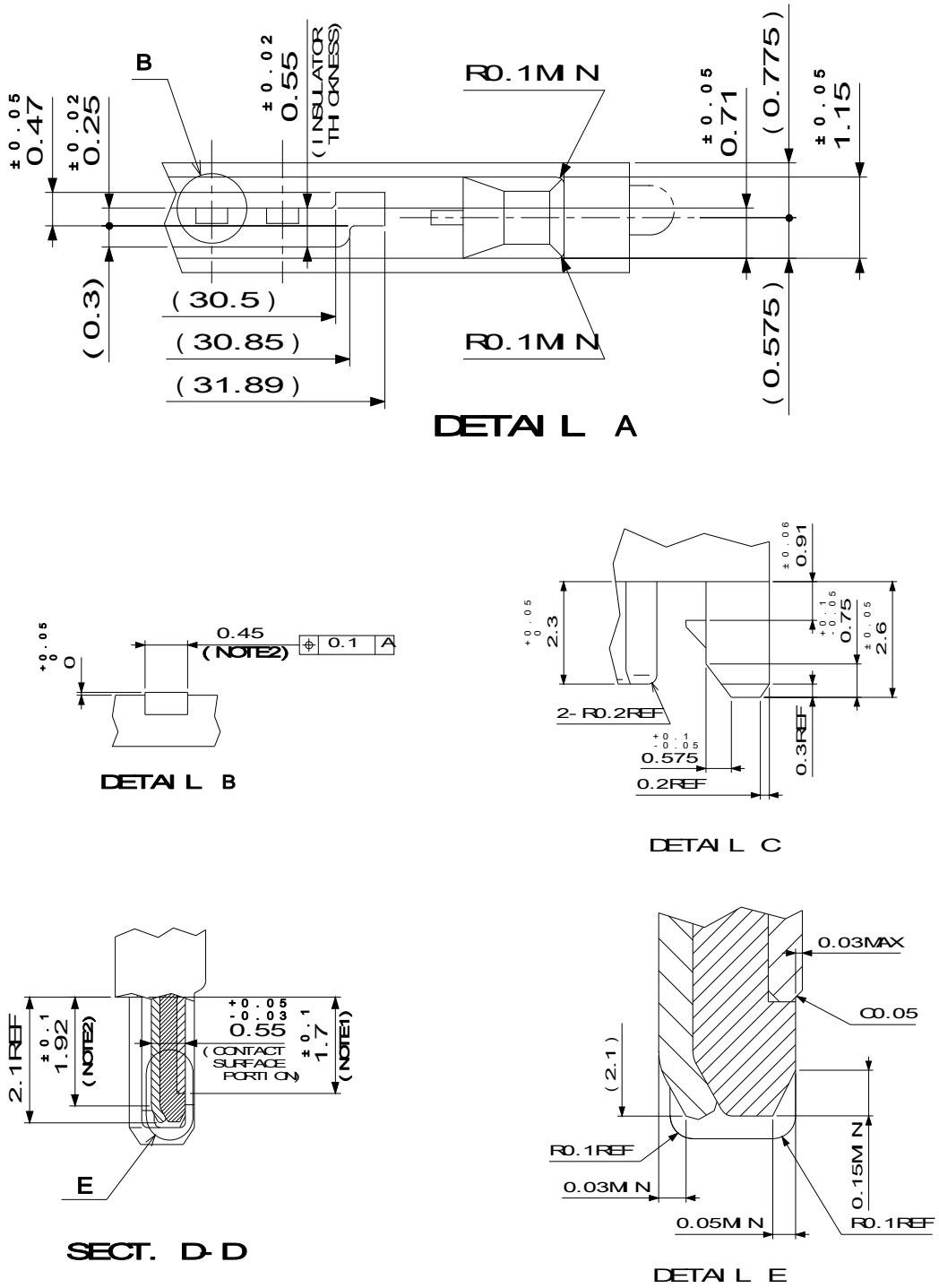


Figure 4-25: Panel-side Internal Cable Plug Connector (in unit of mm)

Note 1: This is ground area

4.2.2.4 Panel-side Internal Plug Connector – Contact and Mechanical Guide Details

Figure 4-26 and Figure 4-27 show the contact and mechanical guide details.



NOTE1. THIS AREA IS GROUND AREA
2. THIS AREA IS SIGNAL CONTACT AREA

Figure 4-26: Contact and Mechanical Guide Details (in unit of mm)

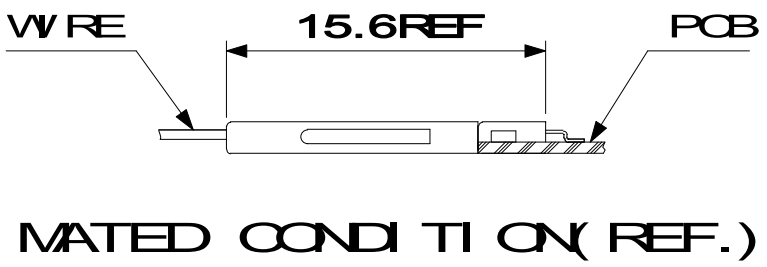


Figure 4-27: Mating Condition (Reference) of Panel Side Internal Cable Connector (in unit of mm)

4.2.2.5 Panel Side Connector Mechanical Requirements

Table 4-10 below shows the mechanical requirements of the panel-side connector.

Table 4-10: Panel-side Connector Mechanical Requirements

ITEM	TEST CONDITION	REQUIREMENT
Vibration (random)	Frequency: 10Hz to 2000Hz Acceleration Velocity: 30.38 m/s^2 (3.1G) RMS. Action direction: In each of 3 mutually perpendicular planes. Duration: 15 minutes each sample. EIA-364-28, Test condition VII, test condition D.	100mA applied with no electrical discontinuity greater than 1µs
Physical shock	Sample should be mounted on the test jig as mounted on the PCB. Aceleration velocity: 490 m/s^2 or 50G. Waveform: half sine Duration: 11 msec. Number of drops: Three drops each to normal and reversed directions of X,Y and Z axis. Total 18 drops. EIA-364-27B method A	No electrical discontinuity greater than 1 µs. must occur.
Durability (mating and unmating).	Number of cycles: 50 Automatic Cycling: 100 ± 50 cycles per hour EIA364-09C	R = 40 mΩ maximum (initially) ΔR = 20mΩ Maximum (final)
Durabilty (preconditioning)	Number of cycles: 20 EIA-364-09C	No Physical Damage.
Connector insertion force	Operation speed :12.5 mm/minute Measure the force required to mate the connector including the latching mechanism. EIA-364-13B	35 N maximum per connector (30 pin).
Connector withdrawal force	Operation speed :12.5mm/min Measure the force required to unmate the connector excluding the latching mechanism. EIA-364-13B	5 N minimum to 25N maximum per connector (30 pin).

4.2.2.6 Pane-side Connector Electrical Requirements

Table 4-11 below shows the electrical requirements of the panel-side connector.

Table 4-11: Panel-side Connector Electrical Requirements

ITEM	TEST CONDITION	REQUIREMENT
Dielectric withstanding voltage	0.25 kV AC for 1 minute. Test between adjacent circuits of unmated connectors. EIA364-20C	No creeping discharge or flashover must occur. Current leakage: 0.5 mA maximum
Insulation resistance	Impressed voltage 100 V DC Test between adjacent circuits of unmated connectors for two minutes. EIA-364-21C	100 MΩ minimum (initial) 50 MΩ minimum (final)
Low level contact resistance	Subject mated contacts assembled in housing measured by dry circuit 20mV maximum open circuit at 10 mA EIA-364-23B	R = 40 mΩ maximum (initial) ΔR = 40 mΩ maximum (final)
Temperature rise	Measure temperature rise by energizing current EIA-364-70A method 1	30ºC maximum ΔT over ambient at maximum rated current (0.50 A) per contact.

4.2.2.7 Panel-side Connector Environmental Requirements

Table 4-12 below shows the environmental requirements of the panel-side connector.

Table 4-12: Panel-side Connector Environmental Requirements

ITEM	TEST CONDITION	REQUIREMENT
Humidity and Temperature Cycling	Cycle Mated connector: 25ºC to 65ºC and 50% to 80% relative humidity 10 cycles and 10 cycles of cold shock at -10ºC per EIA-364-31B method 4	Mating Condition: Contact Resistance: R = 80 mΩ maximum (final) Unmating condition: Insulation resistance: R = 50MΩ maximum (final) ΔR = 50 MΩ maximum
Thermal Shock	Cycle mated connector from -55ºC for 30 minutes to 85ºC for 30 minutes repeat for 10 cycles. EIA-364-32	R = 40 mΩ minimum (initial) ΔR = 40 mΩ maximum (final)
Temperature Life (heat age)	Submit mated connector to 105ºC for 168 hours. EIA-364-17B	R = 40 mΩ minimum (initial) ΔR = 40 mΩ maximum (final)
Temperature Life (preconditioning)	Submit mated connector to 105ºC for 92 hours. EIA-364-17B	No physical damage

5 Source/Sink Device Interoperability

This chapter describes the requirements for DisplayPort devices and cable-connector assemblies to maximize the interoperability between Source and Sink Devices over "box-to-box" DisplayPort link(s).

5.1 Source Device

This section describes the Source Device requirements for "box-to-box" connections.

For embedded connection, it is the responsibility of the system integrator to ensure that the Source Device meets the requirement of a given application.

5.1.1 Stream Source Requirement

This subsection describes the requirements for the stream source in terms of video colorimetry, video timings, and audio formats.

The Stream Source is recommended to support parsing of EDID equivalent, VESA approved identification method in the Sink Device.

5.1.1.1 Video Colorimetry

DisplayPort Source Devices must support sourcing of both RGB and YCbCr colorimetry formats as shown in Table 5-1. A Source Device must indicate the colorimetry format (including the dynamic range) of the transmitted stream in the DisplayPort Main Stream Attributes as described in Section 2.2.4.

In determining the colorimetry format, the Source Device must check the capability of the Sink Device via an EDID read. When the Sink Device capability is unknown, for example due to the corruption of EDID, the Source Device must fall back to 18 bpp RGB, with full dynamic range (called "VESA range" as described in 5.1.1.1.1).

When a Source Device is transmitting a RGB stream with a video timing format called out in CEA-861C Section 5 (except 640 x 480p) as using CEA range RGB, it should use CEA range RGB.

When a Source Device is transmitting 640 x 480p 24 bit RGB, it will always use the full dynamic range.

Table 5-1: DisplayPort Colorimetry Format Support

Colorimetry Format	Bit-depth per Pixel (bpp)	Bit-depth per Component (bpc)	Dynamic Range, Coefficients	*Mandatory vs. Optional*
RGB	18	6	"VESA range" only	Mandatory. Used in "fall-back" modes when Sink Device capability are unknown.
	24	8	"VESA range" or "CEA range"	Mandatory.
	30	10		Optional
	36	12		
	48	16		
YCbCr 4:2:2	16	8	"CEA range". For CEA range, either 601 or 709 coefficients	Mandatory if YCbCr is supported on any other display interface
	20	10		Optional
	24	12		
	32	16		
YCbCr 4:4:4	24	8		Mandatory if YCbCr supported on any other display interface

Colorimetry Format	Bit-depth per Pixel (bpp)	Bit-depth per Component (bpc)	Dynamic Range, Coefficients	*Mandatory vs. Optional*
	30	10		Optional
	36	12		
	48	16		

Note: See the following sub-sections for definitions of VESA range and CEA range.

5.1.1.1.1 RGB Colorimetry

All DisplayPort Source Devices must support RGB colorimetry with pixel depths of 18 and 24 bpp. Support for 30, 36 and 48 bpp RGB is optional.

"VESA range" and "CEA range" are defined as follows:

- "VESA range" must have:
  - Nominal zero intensity level at code value zero
  - Maximum intensity level at maximum code value allowed for bit depth.
    i.e. 63 for 18 bpp RGB, 255 for 24 bpp RGB, 1023 for 30 bpp RGB, 4095 for 36 bpp RGB, and 65,535 for 48 bpp RGB.
- "CEA range" must have:
  - Nominal zero intensity level at 16 for 24 bpp, 64 for 30 bpp, 256 for 36 bpp, and 4,096 for 48 bpp.
  - Maximum intensity level at maximum code value allowed for bit depth, namely, 235 for 24 bpp RGB, 940 for 30 bpp RGB, 3760 for 36 bpp RGB, and 60160 for 48 bpp RGB.
    Note: The RGB CEA range is defined for 24, 30, 36, 48 bpp RGB only, not for 18-bpp RGB.

When a Source Device is transmitting a RGB stream with a video timing format called out in CEA-861C Section 5 as using CEA range RGB, it must use the CEA range RGB.

However, a Source Device may transmit all code values from zero to the maximum even when it declares the CEA range in the Main Stream Attributes. It is the responsibility of the Sink Device to limit the pixel value range as needed.

Note: The Source Device falls back to 18 bpp, VESA range RGB when the sink capability is unknown.

5.1.1.1.2 YCbCr Colorimetry

Support for YCbCr colorimetry is required for DisplayPort Source Devices that support YCbCr or YP_{bPr} on any other display interface, except where the Source Device would be required to convert RGB video to YCbCr in order to meet this requirement.

Source Devices that support YCbCr must support at least 24 bpp YCbCr 4:4:4 and 16 bpp YCbCr 4:2:2 in both 601 (defined in ITU-R BT.601-5 section 3.5 or EIA/CEA-770.2-C section 3.3) and 709 (defined by ITU-R BT.709-4 Part 1, Section 4 or EIA/CEA-770.3-C Sections 5.4 to 5.7).

In addition to the required minimum above, the pixel depth may optionally be 30, 36 and 48 bpp for YCbCr 4:4:4 and 20, 24 and 32 bpp for YCbCr 4:2:2.

YCbCr dynamic range is recommended to be as defined in CEA-861C Section 5 (CEA range):

- Y has nominal zero intensity level at 16 for 8 bits, 64 for 10 bits, 256 for 12 bits, 4,096 for 16 bits per component

- Y has nominal maximum intensity level at 235 for 8 bits, 940 for 10 bits, 3760 for 12 bits, and 60160 for 16 bits per component
- Cb and Cr have their zero levels at 128 for 8 bit, 512 for 10 bit, 2048 for 12 bits, and 32,768 for 16 bits per component
- Cb and Cr have nominal ranges of 16 to 240 for 8 bits, 64 to 960 for 10 bits, 256 to 3840 for 12 bits, and 4,096 to 61,440 for 16 bits per component.

However, a Source Device may transmit all code values from zero to the maximum value. It is the responsibility of the Sink Device to limit the pixel value range as needed.

5.1.1.2 Video Timing Format

In determining the video timing format, the stream source of the Source Device must check the capability of the Sink Device via an EDID read after the Hot Plug Detect signal goes active. When the Sink Device cannot handle the incoming stream, it must toggle the HPD signal to notify the Source Device of this condition. Upon detecting a HPD pulse, the Source Device must determine the Sink Device status by reading SINK_STATUS byte of the DPCD.

When the Sink Device capability is unknown, for example due to corruption of an EDID, the Source Device may fall back to a set of fall-back video timing formats its choice (except for the fail-safe mode). When none of the fall-back video timing formats is acceptable (as indicated by the Sink Device via the SINK_STATUS bit), the Source Device must fall back to the fail safe mode, which is 640 x 480 at 60Hz (as defined in the VESA DMT standard).

5.1.1.3 Audio Format

Audio support is optional for DisplayPort Source Devices. The Source Devices that support audio must support stereo (two channel) 16 bit per sample LPCM at one or more of 32 kHz, 44.1 kHz or 48 kHz.

It is optional for an audio capable Source Devices to support other sample rates, sample sizes or number of channels within the limits of the audio capability of the Sink Device indicated in its EDID.

The Source Device must check via EDID or the CEA Timing Extension to EDID which audio formats the Sink can support before sending any audio stream data.

The Source Device is recommended to find out whether the Sink Device is able to sink the audio stream by checking the SINK_STATUS bit of the Sink Device's DPCD and take corrective action as needed.

5.1.2 Source Device Link Configuration Requirement

The Source Device of a box-to-box DisplayPort connection must support the number of Main Link lanes that provides for sufficient bandwidth even at a reduced bit rate per lane.

For example, if a required application bandwidth is provided both with two lanes at a high bit rate and four lanes at a reduced bit rate, then the detachable Source Device is required to support four lanes.

Note: The Source Device for an embedded connection is not required to follow this rule.

Upon detecting an IRQ Hot Plug Detect signal toggle, the Source Link Policy Maker must read the Receiver Capability field in the DPCD of the Sink Device and configures the link accordingly, using Link Training procedure as described in Section 2.5.3.3 and Section 3.5.1.3.

After the link is configured, the Source Link Policy Maker must check the link status whenever it detects an IRQ HPD pulse. When it detects that the link has lost lock, the Source Link Policy Maker must re-train the link.

Upon detecting either the DOWNSTREAM_PORT_STATUS_CHANGED bit of LANE_ALIGN__STATUS_UPDATED byte in DPCD set or a low-going HPD pulse wider than 2 ms (Hot-plug-event HPD pulse), the Source Link Policy Maker must re-read the Receiver Capability field of the DPCD and take corrective action; For example, re-configure the link with reduced lane count, as needed.

A Source Device changes the Main Link lane count during normal operation following the procedure below:

- Lane count increase
  - Stop the transmission of symbols over the Main Link lanes.
  - Write the desired lane count to the link configuration field of the DPCD via AUX CH.
  - Perform link training. Source may use the known-good drive current and pre-emphasis level setting to accelerate the link training sequence.
  - Once all the lanes are trained, start the transmission of Idle Pattern or a stream.
- Lane count reduction
  - Switch the transmitted symbols to Idle Pattern on all active lanes.
  - Write the desired lane count to the link configuration field of the DPCD via AUX CH.
  - Stop the transmission of the Idle Pattern over the lanes that are to be disabled.
  - Verify that the DisplayPort receiver is symbol locked and inter-lane aligned (unless it is 1 lane configuration)
  - Start the transmission of a stream.

5.1.3 Source Device Behavior on Stream Timing Change

5.1.3.1 Video Stream Timing Change

Before changing the timing of the main video stream, the Source Device must transmit the "idle pattern" (BS symbol followed by VB-ID with NoVideoStream_Flag and VerticalBlanking_Flag both set to 1 every 2^{13} or 8192 LS_Clk cycles) until it is ready to insert the new Main Stream Attribute data during the vertical blanking period of the main video stream. At the very minimum, the Source Device must repeat the idle pattern five times before inserting the new Main Stream Attribute.

For embedded DisplayPort connections, the number of inserted idle patterns may be fewer than five.

If the Source Device chooses to stop the transmission of link symbols during the video timing change, it is required to run Link Training before starting the transport of the new main video stream.

Note: The Source Device is allowed to continue transmitting Audio_Stream packet framed by SS and SE symbols, even when it is no longer transmitting the main video stream. When the video stream is absent, the Source Device must transmit Audio_InfoFrame and Audio_TimeStamp packets after every 512th BS symbol set after SR symbol.

5.1.3.2 Audio Stream Format / Timing Change

As for audio format / timing change, the Source Device must set and keep VB-ID bit 2 (AudioMute_Flag) to 1 until after the new Audio InfoFrame and Audio_TimeStamp have been sent. Those packets may be sent as soon as the next frame boundary (when the main video stream is present) or after the next 512th BS symbol set (when the main video stream is absent).

5.1.4 Source Device Behavior upon HPD Pulse Detection

The HPD signal notifies the Source Device that one of the following events has occurred:

- **IRQ:** Sink Device wants to notify the Source Device that sink's status has changed so it toggles HPD line, forcing the Source Device to read its Link / Sink Status Receiver DPCD field via the AUX-CH
- **Unplug:** The Sink Device is no longer attached to the Source Device and the Source Device may then disable its Main Link as a power-saving measure
- **Plug/re-plug:** The Sink Device is now attached to the Source Device, forcing the Source Device to read its Receiver Capabilities and Link / Sink Status Receiver DPCD fields via the AUX-CH.

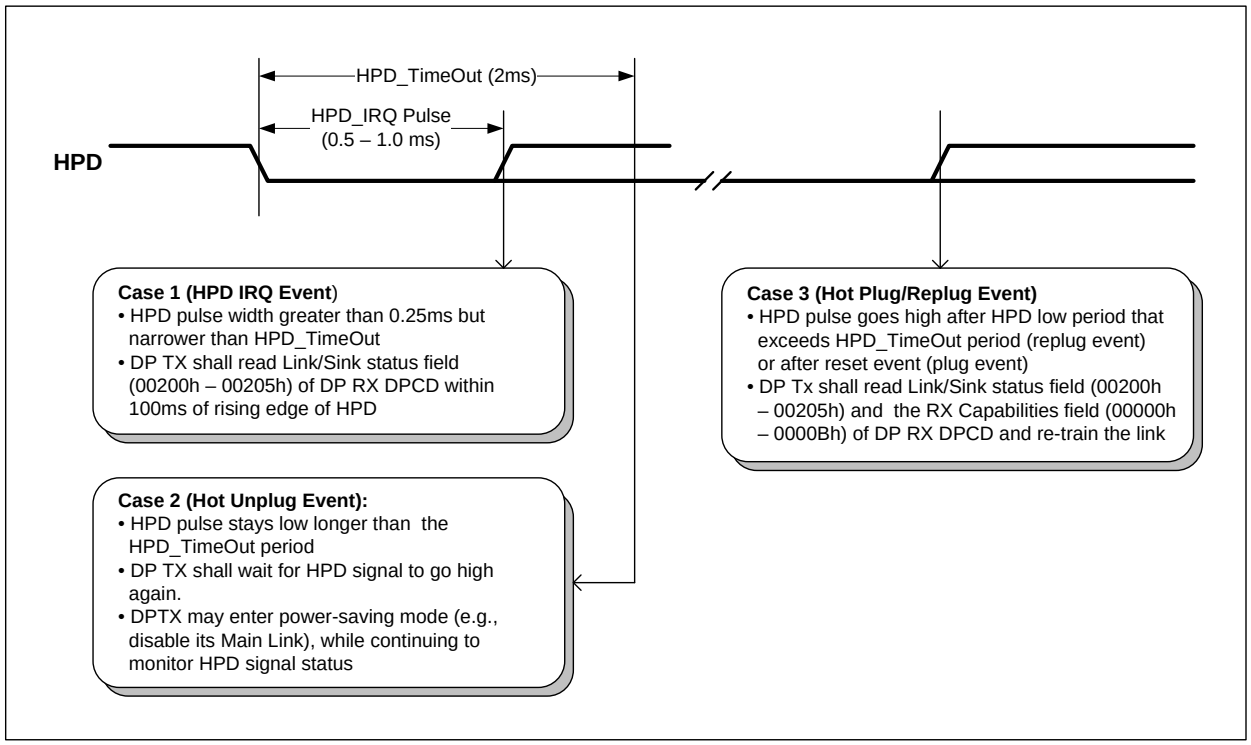


Figure 5-1: HPD Events

Figure 5-1 illustrates the different events signaled via the HPD signal.

Note: In the subsequent discussions the state of the Source Device is assumed to be ON, as the Source Device in the OFF state (for example, powered off or blocked waiting for user input) will obviously not be capable (or required) to respond to a HPD signal status changes.

The Source Device must respond to HPD IRQ events by starting to read the Link / Sink Status field (00200h – 00205h) of the sink's DisplayPort Receiver DPCD via the AUX-CH within 100 ms of the rising edge of the HPD signal. The Source Device must then perform the necessary corrective action based on the current link / sink status.

The Source Device is not required to have an explicit response to HPD unplug events. The source may choose to enter a power saving mode where it disables its Main Link after HPD has been de-asserted for longer than the HPD_TimeOut (2 ms).

Note: False events may occur due to signal bounce upon cable-assembly unplugging. In this condition, AUX-CH read operations will likely fail, and the HPD signal will eventually settle in a de-asserted state for an extended period of time, allowing accurate detection of the unplug event.

The Source Device must respond to HPD plug/re-plug events by first reading the Link / Sink status field of the sink's DisplayPort Receiver DPCD (00200h – 00205h) via the AUX-CH and, if the link is unstable, then reading the sink's Receiver Capabilities field (00000h – 0000Bh) to ascertain the appropriate information to train the link. The source must then initiate link training.

There is no mandatory time constraint on the Source Device's response to a plug / re-plug event, but a Source Device vendor may want to impose a voluntary constraint similar to that for HPD IRQ events (for example, 100 ms) to ensure a good user experience via prompt discovery and configuration of newly attached devices.

5.2 Sink Device

This section describes the requirements for the Sink Device for a "box-to-box" connection.

For embedded connections, it is the responsibility of the system integrator to ensure that the Sink Device meets the requirement of a given application.

5.2.1 Stream Sink Requirement

This subsection describes the requirements for the stream sink in terms of video colorimetry, video timings, and audio formats. A Sink Device must describe its capabilities (supported Video Colorimetry Formats, Video Timing Formats and Audio Formats) in the base EDID and / or the CEA-861 Timing Extension Block (optional). The Sink Device is recommended to support EDID equivalent, VESA approved identification method.

5.2.1.1 Video Colorimetry

DisplayPort Sink Devices support sinking of both RGB and YCbCr colorimetry formats as shown in Table 5-1. Sink Devices must read the colorimetry format of the transmitted stream from the DisplayPort Main Stream Attributes.

When receiving a CEA range video stream, the Sink Device should anticipate that all the code values may be used by the Source Device and clamp the dynamic range if needed.

5.2.1.2 Video Timing Format

A DisplayPort Sink Device must indicate whether it is able to sink the transmitted video stream by setting or clearing the SINK_STATUS bit of its DPCD.

All detachable DisplayPort Sink Devices must support 640 x 480 @ 60 Hz as the fail-safe mode. The sink is not required to scale 640 x 480 to full screen or center the image, but all pixels are required to be visible.

5.2.1.3 Audio Format

A DisplayPort Sink Device that outputs audio must support an audio input stream via DisplayPort link. The audio output may be sound waves (speakers) or electrical analog or digital audio output.

Sink Devices that support audio must support stereo 16 bit LPCM at 32 kHz, 44.1 kHz and 48 kHz. It is optional for all audio capable Sink Devices to support other sample rates, sample sizes or number of channels.

Sink Device must indicate via EDID or the CEA Timing Extension to EDID which audio formats are supported.

Note: As of this writing, only the CEA Timing Extension to EDID provides this information, but it is anticipated that future versions of VESA EDID may also specify audio capabilities of the Sink Device, and these would be acceptable to a DisplayPort Source Device.

As is the case with sinking video stream, the Sink Device must indicate whether it is able to sink the transmitted audio stream by setting or clearing the SINK_STATUS bit of its DPCD.

5.2.2 Sink Device Link Configuration Requirement

The Sink Device requirement for a supported link configuration depends on whether the device is a "lean-back" display or a "lean-in" display. A "lean-back" Sink Device is a display device that is meant to be viewed from more than 1.2 m (approximately 4 feet) away.

A "lean-back" Sink Device must support the number of Main Link lanes that provides for sufficient bandwidth even at a reduced bit rate per lane. This way, the lean-back display device can support a long cable length over which support of only a reduced bit rate is required.

Some examples of lean-back Sink Devices are TV displays and projectors. Table 5-2 and Table 5-3 show examples of the required lane counts for these lean-back display devices.

The Sink Device of an embedded DisplayPort connection is regarded as a "lean-in" Sink and is not required to follow the rule of the "lean-back" Sink describe above.

Table 5-2: Required Lane Count for Typical TV Timings at Reduced Bit Rate

Timing	Lane Count	*Remark*
Up to 480p /576p @ 50 / 60 Hz	One	
Up to 720p / 1080i @ 50 / 60 Hz	One @ 50 Hz, Two @ 60 Hz	 One @ 60Hz if 16 bpp YCbCr 4:2:2
Up to 1080p @ 50 / 60 Hz	Four	

Table 5-3: Required Lane Count for Typical Data Projector Timings at Reduced Bit Rate

Timing	Lane Count	*Remark*
Up to 1024 x 768	One	18 bpp
Up to 1680 x 1050 and 1600 x 1200	Two	18 bpp, 18 bpp, with reduced blanking
Up to 2048 x 1536	Four	18 bpp, with reduced blanking

A lean-in display device such as a desktop monitor may choose to minimize the lane count for lowest cost.

For example, a 1400 x 1050 desktop monitor may have only one Main Link lane.

Note: This example monitor cannot receive its native input resolution over the one lane at the reduced bit rate.

A Sink Device with a captive cable assembly is regarded as a lean-in device, and may choose to minimize the lane count.

5.2.3 Sink Device Behavior on Stream Timing Change

5.2.3.1 Main Video Stream Timing Change

As described in Section 5.1.3, the DisplayPort Source Device must insert the "idle pattern" (BS + VB-ID + Mvid 7:0 +Maud 7:0 with NoVideoStream_Flag and VerticalBlanking_Flag (bit 3 and bit 0) of VB-ID both set to 1 every 2^{13} or 8,192 LS_Clk cycles) at least five times before switching to a new video timing. Upon detecting this condition, a Sink Device must get ready to receive the new Main Stream Attribute and the main video stream data.

Note: The number of inserted idle patterns may be fewer than five for an embedded DisplayPort connection.

Whether to blank the display during this transition is implementation specific. Whatever method is selected, showing a visual image that is neither the incoming video stream nor a blank screen should be avoided.

5.2.3.2 Audio Stream Format / Timing Change

As for audio format / timing change, the Source Device should set and keep VB-ID bit 2 (AudioMute_Flag) to a '1' until after the new Audio InfoFrame and Audio_TimeStamp have been sent. An audio format change is caused by any of:

- A change between the compressed and non-compressed audio
- A change in the sampling rate
- A change in the number of channels

Those packets may be sent as soon as the next frame boundary (when the main video stream is present) or after the next 512th BS symbol set (when the main video stream is absent).

The Sink Device must mute the audio when the AudioMute_Flag is set, and should be ready to receive a new audio format upon detecting the change in Audio InfoFrame and Audio_TimeStamp packets.

5.2.4 Toggling of HPD Signal for Status Change Notification

When there is a change either in the link status (for example, loss of link synchronization) or the device status (for example, remote control command pending), the Sink Device must clear the HPD signal to low for (0.5 ms to 1 ms) before setting it to high again in order to notify the Source Device of the status change.

5.3 Branch Device

This section describes the requirement for DisplayPort Branch Devices. Branch Device types are summarized in Section 2.1.4.

5.3.1 EDID Access Handling Requirement

Branch Device must make sure that the stream transmitted by the Source Device can be sunk by at least one Sink Device in the link. Therefore, a Branch Device without its own local sink must forward the EDID access request from its upstream device to its downstream device.

When a Branch Device has multiple downstream ports, it has multiple choices regarding which downstream device(s) should receive the EDID access request.

The details of how to handle this situation are implementation specific. One example is for such a Branch Device to always choose the Sink Device connected to the lowest Downstream Port number. For instance, when Sink Devices are connected to Downstream Port 2 and Downstream Port 3, the EDID of the Sink Device connected to Downstream Port 2 is forwarded.

Note: DisplayPort Specification version 1 revision 1 does not define a mechanism through which the upstream device can read multiple EDID's of the Sink Devices connected to a Branch Device. The definition of such mechanism is deferred to the future revision of the specification.

5.3.2 Branch Device Link Configuration Requirements

DisplayPort repeaters (DisplayPort-in, DisplayPort-out) must support four Main Link lanes both for the receive and the downstream ports. DisplayPort repeaters must configure the downstream link in the same way (lane count, bit rate per lane, and down spread) as the upstream link is configured.

Once both the upstream and downstream links are configured, DisplayPort repeaters must transport all DisplayPort control and data stream symbols from input to output. Table 5-4 below lists all the DPCD parameters a Branch Device may update depending on the capability of its downstream links.

Table 5-4: DPCD Parameters Branch Device May Update

DisplayPort Address	Parameters
00000h	DPCD_REV DPCD revision number Bits 3:0 = Minor Revision Number Bits 7:4 = Major Revision Number 10h for DPCD Revision 1.0 **Note**: A Branch Device must update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common revision number must be used.
00001h	MAX_LINK_RATE Bits 4:0 = MAX_LINK_RATE Maximum link rate of Main Link lanes = Value x 0.27 Gbps per lane For DisplayPort, only two values are supported. All other values are reserved. 06h = 1.62 Gbps per lane 0Ah = 2.7 Gbps per lane Bits 7:5 = RESERVED. Read all 0's. **Note**: A Branch Device must update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common revision number must be used.
00002h	MAX_LANE_COUNT Bits 3:0 = MAX_LANE_COUNT Maximum number of lanes = Value For DisplayPort, only the following three values are supported. All other values are reserved. 1h = One lane 2h = Two lane 4h = Four lanes Bits 7:4 = RESERVED. Read all 0's. **Note**: A Branch Device must update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common revision number must be used.
00003h	MAX_DOWNSPREAD Bit 0 = MAX_DOWNSPREAD 0 = No spread supported 1 = 0.5% down spread Bits 7:1 = RESERVED. Read all 0's. **Note**: A Branch Device must update this value to comprehend the DPCD of the downstream DisplayPort receiver. The lowest common revision number must be used.

Converters (either from DisplayPort to Legacy or from Legacy to DisplayPort) may have fewer than four Main Link lanes as long as DisplayPort link provides for the sufficient bandwidth for the Legacy link. The converters must support the lane count that meets the bandwidth requirement at a reduced bit rate per lane.

5.3.2.1 Behavior of Branch Device upon Downstream Status Change

When a Branch Device detects a change in its downstream link through Hot Plug / Unplug detection (for example, a Sink Device gets plugged to one of the downstream ports), it must take the following actions within 25 ms after the detection of the HPD pulse:

- If the downstream link is DisplayPort, read the DPCD Receiver Capability field of the connected downstream DisplayPort Receiver and update the DPCD Receiver Capability field (MAX_LINK_RATE, MAX_LANE_COUNT, etc.) to comprehend the capability of the downstream DisplayPort Receiver.
- Increase the SINK_COUNT value as follows:
    - If the immediate downstream link is DisplayPort, increase the SINK_COUNT value by the SINK_COUNT value of the immediate downstream device.
    - If the immediate downstream link is Legacy, increase the SINK_COUNT by 1 when the downstream link is detected "loaded."

Note: If the immediate downstream is Legacy without "loaded" detection, always assume the Sink is connected.

After the action above, Branch Device must de-assert the HPD signal of its upstream port within 25ms. The HPD pulse width must be set as follows:

- HotPlug Event pulse when the Branch Device has changed its receiver capability field to match that of a newly plugged downstream device.
- IRQ_HPD pulse when forwarding the Device Service IRQ vector.

When the Branch Device generates a HotPlug Event pulse to its upstream port, it must wait for the upstream link to be trained, and then train the downstream link.

Note: The Branch Device HPD propagation latency requirement of 50 ms (25 ms for downstream and 25ms for upstream) does not apply to HDCP enabled Branch Devices. For the propagation latency requirement of a HDCP enabled Branch Device, refer to the HDCP Specification 1.3 Amendment for DisplayPort Revision 1.0.

5.3.2.2 Example of Actions upon Addition of a Sink Device (INFORMATIVE)

Figure 5-2 shows an example of actions upon addition of a Sink Device to a DisplayPort link.

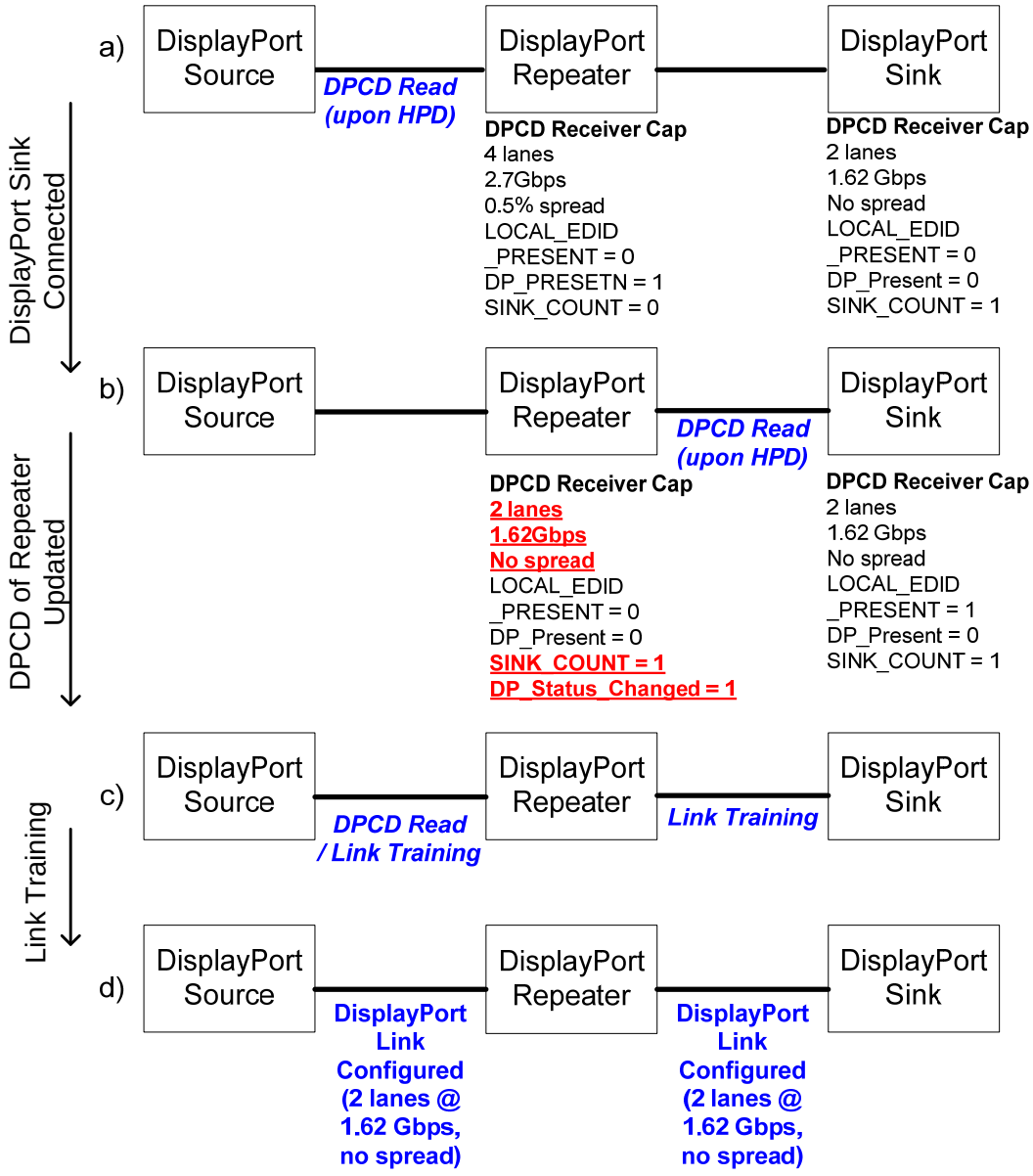


Figure 5-2: Action Flow upon Addition of Sink Device

5.4 Cable-Connector Assembly

This section describes the requirement for the cable-connector assembly.

5.4.1 Box-to-Box, End-user Detachable Cable Assembly

A box-to-box, detachable DisplayPort cable assembly must support four Main Link lanes.

Box-to-box, detachable DisplayPort cable assemblies of two meters or less must meet the high-bit-rate cable specification detailed in Section 4.1.4. All box-to-box, detachable DisplayPort cable assemblies must meet the low-bit-rate cable specification as detailed in Section 4.1.6.

The mating connectors of the box-to-box DisplayPort connection must meet the connector specification as detailed in Section 4.2.

5.4.2 Embedded and Captive Cable Assembly

An embedded or captive DisplayPort cable assembly may support fewer than four Main Link lanes as long as "sufficient" link bandwidth is provided for the design application with fewer lanes. For embedded and captive connections, it is the responsibility of the system integrator to select the cable assembly with sufficient bandwidth capacity.

6 Appendix A: Link Layer Extension for DPCP Support

DPCP (DisplayPort Content Protection) is an optional feature of DisplayPort and its specification is separate from the DisplayPort specification. This appendix briefly describes the Link Layer extension for supporting DPCP.

6.1 DPCP Bulk Encryption/Decryption Blocks

The bulk encryption is applied at the end of the Link Layer (just before the two Link Symbol inter-lane skew is inserted and scrambling is performed) while the bulk decryption is applied at the beginning of Link Layer (just after the de-scrambling and the two Link Symbol inter-lane de-skewing are performed) as shown in Figure 2-8 and Figure 2-9, respectively. When the link is encrypted, all the information transmitted on the link is encrypted (pixel data, sea of dummy symbols, and secondary-data packets)

DPCP uses two additional control symbols, CPBS and CPSR. These symbols replace BS and SR respectively when DPCP is enabled.

When DPCP is off, “DPCP bulk encryption” leaves all symbols (control and data) untouched but when DPCP is on, “DPCP bulk encryption”:

- Replaces BS with CPBS and SR with CPSR,
- Leaves other control symbol untouched,
- Encrypts all data symbols, namely, valid main video stream data, sea of dummy symbols, and secondary-data packets.

When DPCP is off, “DPCP bulk decryption” leaves all symbols (control and data) untouched but when DPCP is on, “DPCP bulk decryption”:

- Replaces CPBS with BS and SR with CPSR,
- Leaves any other control symbol untouched,
- Decrypts all data symbols.

When DPCP is off, “DPCP bulk decryption” leaves all symbols (control and data) untouched.

Source Device must replace every 512th of them with SR or CPSR, respectively in the transmitter. In the receiver of Sink Device, an SR or CPSR symbol must trigger a reset of the de-scrambler and be replaced with BS or CPBS, respectively.

6.2 AUX CH Transactions for DPCP

DPCP relies on the AUX CH for the content protection mutual authentication and the content protection information transport. The AUX CH is also used to introduce a redundancy for the DPCP synchronization secondary-data packet in the Main Link.

The AUX CH is also used both to reset DPCP and to query the DPCP status information.

DPCP is managed at the link level. Within the DPCD address space for link services, addresses 70000h - 7FFFFh are reserved for DPCP. Furthermore, within the device service address space, 80000h - 807FFh are also reserved for DPCP.

For DPCP control, native AUX CH transactions are used.

7 Appendix B: Audio Transport *(INFORMATIVE)*

Audio related secondary-data packets are covered in section 2.2.5. This appendix, intended to be read along with that section, aims to add clarification to the specification and to reduce ambiguity in order to improve on the interoperability between audio capable DisplayPort devices.

7.1 Audio stream components

An Audio stream consists of following components: Audio Stream Packets, Audio Time-stamp Packets; Audio Info Packets (as defined in CEA861-C Specification) and some portion of VB-ID. In the DisplayPort Specifications all audio related packets except VB-ID are transported as part of the secondary-data packet stream.

An Audio Stream Packet includes audio stream itself and some attribute information such as audio coding type and channel count. Depending on the coding type of Audio Stream Packet it may contain status information about parameters of the audio stream. For example, the existing format, which is similar to IEC60958 standard, transfers this information in serial format via block of samples. (Refer to IEC60958-1 and IEC60958-3 standards).

An Audio InfoFrame Packet is used for transferring attributes of the audio stream in a separate packet. Depending on the coding type of the Audio Stream Packet, there is some overlap between the information carried by Audio Stream Packet and that carried by Audio Info Frame Packet. Whenever there is an overlap, the information carried by the Audio Stream Packet takes precedence. As a matter of fact, the Audio Info Frame Packet must be referred to only for audio channel to speaker mapping in the DisplayPort Specification. When one or two channel audio is transported, the CEA861-C Specification defines only a single channel to speaker mapping. Therefore, the transmission of an Audio InfoFrame may be omitted altogether.

An Audio Time-stamp packet is used for the audio clock regeneration to restore the audio master clock frequency needed for further audio processing.

Additional signals such as “audio mute” signal for disabling audio are carried in the VB-ID byte transmitted next to each BS control symbol.

Section 7.2 describes how the time slot for Audio Stream Packet transmission must be scheduled. As far as the Audio Time-stamp Packet and Audio Info Frame Packet are concerned, they must be transmitted once per frame. It is recommended that they be transmitted during the main video stream vertical blanking period.

Note: The Audio Time-stamp Packet may be transferred more than once per frame. It is up to each DisplayPort transmitter implementation to decide how many times to transfer the Audio Time-stamp Packet.

7.2 Association of Three Packet Types via Packet ID

The transport of an audio stream over a DisplayPort link involves transmission of three packet types: Audio Stream Packet, Audio Time-stamp Packet, and Audio InfoFrame Packet. These three types of packets for a single audio stream are associated with one another by having the same Secondary-data Packet ID (00h) carried as HB0 (header byte 0) of each packet.

7.3 Scheduling of Audio Stream Packet Transmission

An audio stream is a continuous (that is, isochronous) stream of audio samples, each of which may contain several channels of audio signals at a pre-defined sample frequency (fs). The sample frequency is typically in the range of 32 kHz to 192 kHz.

The transmission scheduler for an Audio Stream Packet must wait for a time slot for audio transmission during which there are no main video stream, Main Stream Attribute Packet, and other higher priority

secondary-data packets in queue. Therefore, the DisplayPort transmitter and receiver are required to have some buffer space to hold the audio data while the Audio Stream Packet is waiting for its time slot.

Figure 7-1 shows how the Audio Stream Packets are transferred over the DisplayPort link when there is no video being transmitted. Figure 7-2 shows the Audio Stream Packet transfer with main video stream being transmitted. The transmission of Audio Stream Packets is withheld from BE symbol assertion till BS symbol assertion because the main video stream occupies the link during that period. Instead, the Audio Stream Packets are transmitted between BS and BE. During the vertical blanking period of the main video stream, the Audio Stream Packet transfer pattern will be similar to Figure 7-1.

Note: The presence or absence of main video stream is indicated in VB-ID bit 3.

As noted earlier, an Audio Stream Packets may be transmitted over the link any time as long as the time slot is available. Since the video line period of a given video format is constant throughout a video vertical frame period and so is the audio sample rate, the number of the audio samples transmitted over DisplayPort per a main video stream line period is roughly constant for the given video format. No special audio bandwidth allocation calculation is required to realize this scheduling control.

The higher the audio data rate (in Mbytes/second) and the longer the main video line period, the larger the buffer size requirement. An implementer should determine the buffer size by determining the maximum audio data rate and the longest main video line period that need to be supported.

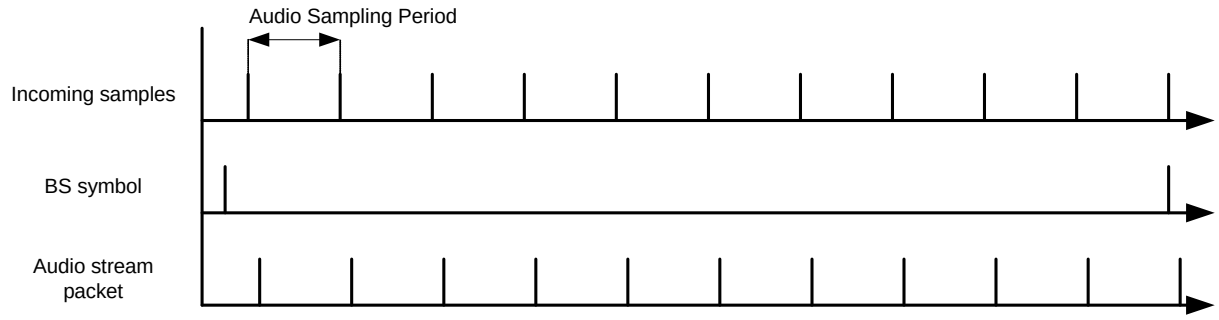


Figure 7-1: Audio Stream Packets Transfer with No Video or During Video Vertical Blanking

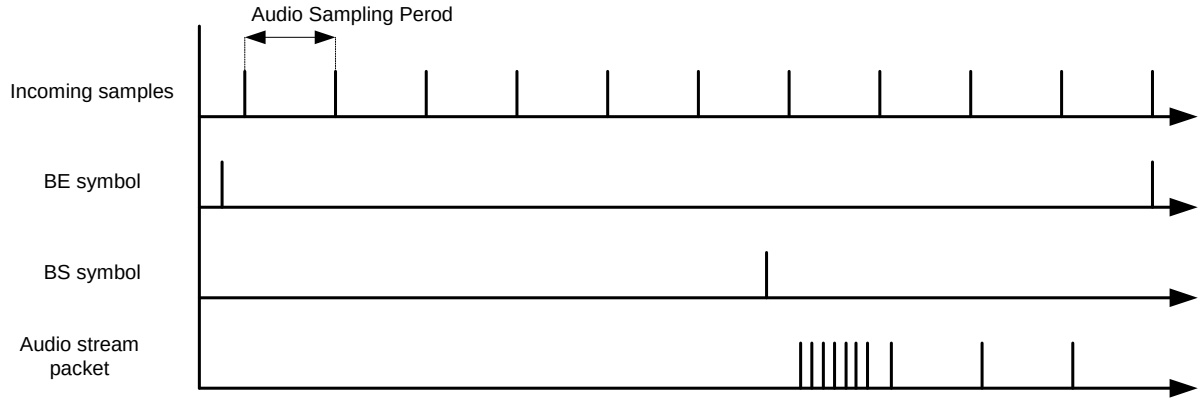


Figure 7-2: Audio Stream Packets Transfer Along with Video during Video Vertical Active Period

7.3.1 Handling of an Audio Format Change

The transported audio format may be changed at the any time. The DisplayPort transmitter should start sending an audio mute signal prior to the audio format change, by setting bit 4 (AudioMute_Flag) of VB-ID

which is sent once per main video stream line period (or once per 8192 link symbols when the main video stream is absent). An audio format change is caused by any of:

- A change between the compressed and non-compressed audio
- A change in the sampling rate
- A change in the number of channels

This signal indicates to the DisplayPort receiver that the audio system is in a transient process and the audio stream may be not valid at this time. When the AudioMute_Flag is '1', a DisplayPort receiver must disable its audio output while continuing to receive and process Audio Time-stamps.

The DisplayPort transmitter should clear the AudioMute_Flag to '0' only after finishing the transient process at the audio source input, finishing audio clock measurement with a correct and stable value and providing information about this change to the receiver. The DisplayPort transmitter should clear the audio mute signal only after transferring Audio Time-stamp and Audio Info packet (if needed).

Once the DisplayPort transmitter clears the AudioMute_Flag to '0', a DisplayPort receiver should enable its audio output only after the regenerated audio clock becomes stable and after it has collected enough audio status information.

7.4 Structure of Audio Stream Packet

The DisplayPort Specification defines only one audio coding type which is similar to IEC 60958 format, as specified in bits 7:4 of HB3 (header byte 3). However, other coding types are expected to be added in the future. Therefore, a DisplayPort receiver must check the coding type field to remain compatible with future revisions of the DisplayPort Specification.

ChannelCount field (bits 2:0 of header byte 3 (HB3)) carries information about the count of audio channels transmitted over the link. This field must have following values: 000 for one channel audio, 001 for two channel audio, up to 111 for eight channel audio.

The audio stream payload data structure has two configurations: One is for one or two channel audio and the other for three to eight channel audio. An Audio stream packet may have variable payload size. At the minimum, Audio Stream Packet size is as follows:

7.4.1 One or Two Channel Audio

Four header bytes protected by four ECC parity bytes, followed by 16 payload data bytes protected by four ECC parity bytes. The 16 payload data bytes consist of four 32 bit audio channel samples. Each of the 16 payload data bytes carries two audio samples, each consisting of 1st channel and 2nd channel audio samples. For one channel audio, the 2nd channel audio sample data must be zero padded.

7.4.2 Three to Eight Channel Audio

Four header bytes protected by four ECC parity bytes, followed by two sets of 16 payload data bytes, each protected by four ECC parity bytes (resulting in 32 data bytes plus 8 ECC parity bytes). As is the case with one or two channel audio, each of the 16 payload data bytes consists of four 32 bit audio samples. When the channel count is less than eight, unused audio channel sample data must be zero padded.

The DisplayPort transmitter may use one common Audio Stream packet's size for both one and two channel audio and three to eight channel audio modes. In this case, the packet payload configuration consisting of 32 data bytes plus 8 ECC parity bytes (the payload configuration for three to eight channel audio described in the previous paragraph) must be used.

The DisplayPort transmitter may concatenate multiple sets of minimum packet payload to form a long packet that has up to 256 data bytes for one or two channel audio and 1024 data bytes in case of three to eight channel audio.

Regardless of the payload size, each packet must be framed with SS and SE symbols and start with four header bytes protected by four ECC parity bytes and then body is present with sets of 16 bytes of data and four bytes of ECC parity.

Note: All the channels of data of one audio sample should be transferred in one packet. Dividing one sample into multiple Audio Stream Packets is not allowed.

Within the 32 bit audio channel data, the least significant 24 bits carry audio sample data while the most significant eight bits carry control, status and parity. The most significant bit (bit 7 of Byte 3), SP, indicates whether an audio sample is present. All the channels of one audio sample must have the same state of this flag.

For example, even when one channel audio is being transported and, therefore, all the 24 bits of the 2nd channel sample data are zero padded, the SP bit of this 2nd channel must be set to '1' whenever the SP bit of the 1st channel is '1'. The same situation applies to long packets (more then 32 bytes of data) when gaps between samples can be present marked by SP=0.

When one or two channel audio is transported, the 16 payload data bytes consist of two audio samples as noted earlier. Of these two samples, the second sample may have the SP bits cleared to '0'. For three to eight channel audio transport, the SP bits must be always 1.

Of the remaining seven control, status and parity bits, of note is the PR field (bits 5:4 of Byte 3). The PR field is inserted only for the 1st and 2nd channel data regardless of the channel count. The PR field is omitted from the rest of the channels.

7.5 Channel-to-Speaker Mapping

Channel position in the DisplayPort stream with more than two channels should exactly correspond to CEA861-C Specification. This means that gaps between channels can be present. Table 7-1 shows channel-placing for the one of the possible channel mappings described in CEA861-C Specification. This table describes transmission of three channels with CA set to 04h in byte 4 of the Audio InfoFrame Packet.

Table 7-1: Channel to Speaker Mapping of Three Channel Audio with CA = 04h

Four Lane Main Link			
Lane 0	**Lane 1**	**Lane 2**	**Lane 3**
SS	SS	SS	SS
HB0	HB1	HB2	HB3
PB0	PB1	PB2	PB3
S0_Ch1_B0	S0_Ch2_B0	00	00
S0_Ch1_B1	S0_Ch2_B1	00	00
S0_Ch1_B2	S0_Ch2_B2	00	00
S0_Ch1_B3	S0_Ch2_B3	0x80	0x80
PB4	PB5	PB6	PB7
S0_Ch5_B0	00	00	00
S0_Ch5_B1	00	00	00
S0_Ch5_B2	00	00	00
S0_Ch5_B3	0x80	0x80	0x80
PB8	PB9	PB10	PB11

Note: The most significant bit (bit 7 of byte 3) of the 32 bit audio sample data, the SP bit, indicates if an audio sample is present.

The channel to speaker mapping information is provided in an Audio InfoFrame Packet as described in Table 20 of the CEA861-C Specification. When one-channel audio is transported, it must use the FL channel (that is, Channel 1).

7.6 Transfer of Sample Frequency Information

Information about audio sampling frequency is transferred in an Audio Time-stamp Packet, which provides the audio clock frequency information (Maud and Naud) using the following formula:

- Maud / Naud = 512 * fs / f_LS_Clk

where fs is the sampling frequency of the audio stream being transported.

In accordance with the DisplayPort Specification, this information is transferred at least once per video frame (or following 512th BS symbol when the main video stream is not present). A DisplayPort transmitter is allowed to transmit it more frequently if it chooses to do so. In addition, the DisplayPort Specification allows for the transmission of the least significant eight bits of the Maud value once per line of main video stream line and it is up to the DisplayPort receiver to use or not this information.

How a DisplayPort receiver regenerates the audio sampling frequency is implementation specific and is beyond the scope of the DisplayPort Specification.

For example: Some implementations may use the Maud and Naud values to set the initial frequency of the audio clock recovery circuit and perform the fine frequency adjustment based on the audio FIFO fill rate. With this method, a DisplayPort receiver may ignore Maud 7:0 data from the VB-ID packet.

8 Appendix C: Sink Event Notification Example (INFORMATIVE)

This appendix describes a mechanism through which the DisplayPort Sink Device can notify the DisplayPort Source Device of a sink event such as a display orientation switch between portrait and landscape.

8.1 Mutual Identification by Source and Sink

Upon a Hot-Plug Event, the Source Device and Sink Device may identify each other by accessing the Source-specific field (Address 300h to 3FFh) and Sink-specific field (400h to 4FFh) of the DPCD. A Source Device that is interested in enabling its "Extension" feature should write its own 24 bit IEEE OUI (Organizational Unique ID) to Addresses 300h to 302h and read the 24 bit IEE OUI of the Sink Device from Addresses 400h to 402h. The Source Device may optionally write and read more than 3 bytes of IEEE OUI to exchange further identification information (for example, Chip ID and Revision ID). The "Extension" feature is enabled only when each device recognizes that the other device supports it.

8.2 IRQ_HPD Pulse and Sink-Specific IRQ

A Sink Device that supports the Sink Event notification feature indicates what sink event types are supporting by setting "Sink_Event_Type" byte(s) in the sink specific field. The Source Device, upon reading the Sink_Event_Type byte(s) via the AUX CH, enables certain sink events by writing to the Sink_Event_Mask byte(s) in the sink specific field. The address mapping of Sink_Event_Type byte(s) and Sink_Event_Mask byte(s) is implementation specific.

When the selected sink event (such as the display orientation switch) occurs, the Sink Device takes the following actions:

- Programs a set of parameters to a pre-defined address range of the Sink-specific field
- Sets Sink-Specific IRQ bit of DPCD (Bit 6 of Address 201h)
- Generates IRQ_HPD pulse on the HPD signal line

The Source Device, upon detecting the IRQ_HPD pulse, takes the following actions:

- Reads the Link / Sink Status field of DPCD and identifies that the cause of IRQ is Sink-Specific
- Reads a set of parameters from the pre-defined address range of the Sink-specific field
- Performs an operation according to the read parameters:
    - If the notified sink event is a display orientation change, it may change the orientation of the video data it is transmitting.

9 Appendix D: Summary of Features Related to Power Management (INFORMATIVE)

This appendix summarizes features related to power management in DisplayPort Specification version 1 revision 1.

9.1 AUX CH Request Transaction Readiness by Sink Device

While the Sink Device keeps its HPD signal asserted, it must be ready for an AUX CH request transaction by the Source Device. The Sink Device must make the best effort to reply to the request transaction within the Response time-out period of 300 μs.

A Sink Device may keep its HPD signal asserted while it is in a power-saving mode. Whether to de-assert the HPD signal in power-saving mode or not is a implementation-specific decision.

The Sink Device may enter into power-saving mode for various reasons. Some examples are listed below.

- Source Device has set Sink Device into D3 (power-saving) state by writing 02h to DPCD address 600h.
- Soft power button is pressed on the Sink Device.
- Source Device is detected as absent.

When the Sink Device receives the AUX CH request transaction while it is in a power save mode and has kept the HPD signal asserted, the Sink Device is not required to reply immediately. However, the Sink Device must monitor the presence of differential signal on AUX CH and must fully enable the AUX CH circuit within 1ms after detection of a differential signal so that it can reply to the request transaction retry by Source Device.

A Sink Device may disable the differential signal monitoring on the AUX CH lines when it de-asserts the HPD signal.

When a Source Device attempts to put the Sink Device back into normal operation state by writing 01h to DPCD address 600h, it should expect that the Sink Device may not reply within Reply Time-out period. In case there is no reply to AUX CH request transaction, the Source Device must retry at least three times.

9.2 Source Detection

It is optional for a Sink Device to monitor the presence of the Source Device by monitoring the DC voltage between the AC-coupling capacitors on the Source and Sink Devices.

How (or whether) to use Source Detection signal status for power management purpose is an implementation-specific decision of the Sink Device.

9.3 Link Training without AUX CH Handshake (Fast Link Training)

As long as the Source Device has monitored that the HPD signal has stayed asserted, it may initiate Link Training without an AUX CH handshake (Fast Link Training) using the last known-good link configuration if the Sink Device supports the feature. Whether the Sink Device supports the Fast Link Training is indicated in the Receiver Capability field of DPCD. In case of Fast Link Training failure, the Source Device must initiate full link training with an AUX CH handshake.

A Sink Device is not required to support Fast Link Training when it is in a power-saving mode.