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        ################################################
        #             ZeBu V6_1_1 Software             #
        # Installation - New Features - Limitations    #
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        #          Copyright (c) 2009                  #
        # Emulation and Verification Engineering  SA   #
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```

Installation:

- PCI Express interface
- Tcl 8.4
- If you are upgrading from ZeBu software V4_3_3, then new licenses are required (contact license@eve-team.com).
- Xilinx ISE 11.1i package for ZeBu is provided:
  - Specific licenses are required. Contact license@eve-team.com.
  - XST synthesizer is not included in the Xilinx ISE package for ZeBu.
- Diagnostics patches are delivered as separate packages.
- Sample configurations available for compilation:
  - 2-slot unit with 4C modules in slot 0 and 1
  - 2-slot unit with 8C modules in slot 0 and 1
  - 5-slot unit with 4C modules in slots 0 to 4.

  To compile for a different system (when targetting runtime), contact support for appropriate information.
- Includes the license package for Solaris and Linux.
- Does not include SynplifyZebu.
  (tests have been done with zFAST, XST and Synplify Pro 9.4 synthesizers).
- Tested Platforms:
  - Compilation: RHEL4 64-bit and RHEL5 64-bit
  - Runtime: RHEL4 64-bit (with kernel version 2.6.9) and Suse 10
- The documentation package will be released separately.
- No Release Note planned for V6_1_1.

New Features vs V6_1_0:

- Clustering control can now be set to 'Pre-existing Mapping', 'Automatic with Parameters' or 'Full Automatic'.
- 16C modules are now supported.
- Calibration of inter-FPGA communication at 300, 350, 400 and 450 MHz.
- Front-End 'quick' and 'optimized' modes in zCui.
- New compilation manual based on zCui usage.
- SVAs available when synthesizing with zFAST.

Known Limitations:

- Only primary clocks declared as zceiClockPort instantiations in the DVE file can be used by a module other than M0. Clocks coming from zClockPort or from a message port cannot be connected to such a module.
- In a multi-module configuration, only 10 primary clocks can be declared in the DVE file instead of 16.
- Panels with FPGA lists are no longer available in zCui (in particular to set FPGA Place & Route options).
- When design memories are mapped to LUTRAM resources, ISE sometimes maps them to memory resources which cannot be accessed at runtime.
  Hint: to avoid any mapping to LUTRAM, go to the 'Project -> Preferences -> Memory' panel in zCui and set the 'Ramlut vs BRAM Threshold' to 0%.
- In 5-slot units, SMARTICE port P4 does not have a clock.
  If user tries to use it, zRTB_FW will not exit in error.
- ngxBuild is not supported.
- ZeBu-Server multi-unit systems are not supported.
- Direct ICE interface is not supported.
- The zSpy tool is not available.
- In zNetgen, the 'write_verilog' command is no longer supported.
  edf2x tool should be used instead.
- Mapping to FK is not supported.
- Manual mapping of memory instances is not supported.
- The new runtime memory parser (introduced in V4_3_3) is not available.

* No temperature interrupts. Overheating will not be detected.
* SCEMI-1 is not supported.
* Advanced triggers are not supported.