Device Reliability Report

First Quarter 2013

UG116 (v9.4) May 13, 2013

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/09/2004	1.0	Initial release in new template.
05/10/2004	2.0	First quarter 2004 revision.
05/24/2004	2.1	Changed fit rate on page 7 for 0.5 µm from 89 to 8.
05/24/2004	2.2	Changes to Tables 1-1, 2-1, 2-15, 3-44, 3-46, 3-48, 3-50, and 3-52; also a heading on page 75.
08/18/2004	2.3	Added second quarter data.
01/04/2005	2.4	Added third quarter data.
03/01/2005	2.5	Changes in most tables to show the fourth-quarter test values. Removed packaging information from Chapter 1 and added a reference to the packaging website.
05/20/2005	2.6	Data corrections in tables 2-61 and 3-32.
08/19/2005	2.7	Changes in most tables to show the second-quarter test values.
11/17/2005	2.8	Updates most tables to include the third-quarter test data.
02/24/2006	2.9	Most tables updated to reflect the fourth-quarter test data.
05/05/2006	3.0	Changes in most tables to show the first-quarter test data.
06/20/2006	3.0.1	Corrected two transposed figures in Table 1-10.
08/11/2006	3.1	Changes in most tables to show the second-quarter test data.
08/29/2006	3.1.1	Changed typos in tables 2-91, 3-44, and 3-55.
10/06/2006	3.1.2	Corrected values in tables 1-12, 2-87, 2-90, and 2-91.

Date	Version	Revision *(Cont'd)*
12/01/2006	3.2	Changes in most tables to show the third-quarter test data.
02/12/2007	3.3	Changes in most tables to show the fourth-quarter test data.
02/20/2007	3.3.1	Correct typos in three tables.
03/28/2007	3.3.2	Correct typos in four tables.
06/04/2007	4.0	Changes in most tables to show the first-quarter test data.
08/24/2007	4.1	Changes in most tables to show the second-quarter test data.
09/18/2007	4.1.1	Corrected omission in this history table.
10/31/2007	4.2	Changes in most tables to show the third-quarter test data.
02/06/2008	4.3	Changes in most tables to show the fourth-quarter test data.
07/07/2008	5.0	Changes in most tables to show the first-quarter test data.
08/15/2008	5.1	Changes in most tables to show the second-quarter test data.
11/14/2008	5.2	Changes in most tables to show the third-quarter test data. Updated legal disclaimer.
02/11/2009	5.3	Changes in most tables to show the fourth-quarter test data. Added single event upset and soft error rate data. See Table 1-14, page 19. Note: Table number is accurate as of the version 5.3 printing.
05/07/2009	5.4	Changes in most tables to show the first-quarter, 2009 test data. Added second paragraph to SEU and Soft Error Rate Measurements, page 26.
06/15/09	5.5	Added SF363 (Lot 2) data to Table 3-62, page 102. Replaced Figure 3-1, page 103, Figure 3-2, page 103, and Figure 3-3, page 104. Revised FFG1704 data in Table 3-64, page 108. Note: Table and Figure numbers are accurate as of the version 5.5 printing.
08/03/2009	5.6	Changes in most tables to show the second-quarter, 2009 test data.
10/27/09	5.7	Added alpha particle FIT/Mb data for Spartan-6 and Virtex®-6 FPGAs to Table 1-14, page 19. Most tables updated to include third-quarter, 2009 test data. Note: Table number is accurate as of the version 5.7 printing.
03/15/2010	5.8	Changes in most tables to show the fourth-quarter, 2009 test data.
05/04/2010	5.9	Changes in most tables to show the first-quarter, 2010 test data.
08/10/2010	5.10	Changes in most tables to show the second-quarter, 2010 test data.
11/01/2010	5.11	Changes in most tables to show the third-quarter, 2010 test data.
02/01/2011	5.12	Changes in most tables to show the fourth-quarter, 2010 test data.
05/09/2011	6.0	Changes in most tables to show the first-quarter, 2011 test data.
06/17/2011	6.0.1	Revised last sentence in SEU and Soft Error Rate Measurements, page 26 for clarity.
08/02/2011	7.0	Changes in most tables to show the second-quarter, 2011 test data.

Date	Version	Revision *(Cont'd)*
11/07/2011	8.0	Changes in most tables to show the third-quarter, 2011 test data. Chapter 1, The Reliability Program: Updated Acceptance Criteria and added note 3 to Table 1-3. Chapter 2, Results by Product Family: Added XCV600E to Table 2-12. Added XC2VP7 to and deleted XC2VP80 from Table 2-15. Deleted XC3S2000 from Table 2-18. Deleted XC4VLX15 from Table 2-24. Added XC6VLX130T to Table 2-28. Added XC4VLX80 to Table 2-43. Added XC2V6000 to Table 2-77. Deleted XC4VFX100 and XC4VLX85T from Table 2-85. Added XC5VLX330T device to Table 2-86. Added XC6VLX195T device to Table 2-87. Added XC6SLX25T to Table 2-99. Added XCV100 to Table 2-123. Added XC6SLX16 to Table 2-136. Added XC4VLX80 to Table 2-137. Deleted XC17S150XL from Table 2-146. Deleted XCF128X from Table 2-148. Deleted XC17S30XL from Table 2-152. Deleted XCF01S, XCF04S, XCF08P, and XCF128X from Table 2-155. Deleted XC17S30XL from Table 2-163. Deleted XC17V16 from Table 2-164. Deleted XC17S30XL from Table 2-169. Deleted XC17V16 from Table 2-170. Deleted XCF01S, XCF04S, XCF08P, and XCF128X from Table 2-172. Deleted XC95216 from Table 2-174. Added XCR3256XL and deleted XCR384XL and XCR3512XL from Table 2-192. Added XCR3256XL and deleted XCR384XL and XCR3512XL from Table 2-201. Added XCR3256XL and deleted XCR3128XL XCR3512XL from Table 2-213. Chapter 3, Results by Package Type: Added HASTU to Table 3-11. Deleted HTS from Table 3-12. Deleted HASTU from Table 3-15. Deleted Temperature cycling –40 to +125°C row from Table 3-26. Added HASTU to Table 3-29. Added HTS to Table 3-43. Added HAST to Table 3-47. Added Temperature cycling -55 to +125°C row and HTS to Table 3-49. Added HTS to Table 3-66. Added Temperature humidity 85°C, 85% RH with bias row to Table 3-74. Note: Table numbers are accurate as of the version 8.0 printing.
01/27/2012	8.1	Updated Notice of Disclaimer. Changes in most tables to show the fourth-quarter, 2011 test data. Chapter 1, The Reliability Program: Added XCE6VxXxxx to Table 1-7. Added XC5VSX240T to Table 1-12. Chapter 2, Results by Product Family: Added XCE6VxXxxx to Table 2-1. Deleted XC2S150 from Table 2-8. Added XCV100 to Table 2-9. Added XC6SLX45 and XC6SLX100 to and deleted XC6SLX16 from Table 2-23. Added XC4VLX160 and XC4VFX12 and modified Note 1 in Table 2-24. Added Note 1 to Table 2-25 and Table 2-26. Inserted new table: Table 2-29. Added XC5VLX85T to table Table 2-45. Added XC6VLX365T to Table 2-46. Added XCS20XL to and deleted XCS10XL from Table 2-71. Added XC3S200AN to Table 2-84. Added XC6SLX4 to Table 2-85. Added XC2S100E to and deleted XC2S400E from Table 2-93. Added XCS20XL and XCSxxxX to Table 2-105. Added XC6SLX4 and XC6SLX9 to Table 2-117. Deleted XCR3064XL from Table 2-178. Added XC2C64 to Table 2-194. Added XCR3128XL to Table 2-214. Added XC2C64 to Table 2-215. Chapter 3, Results by Package Type: Added HTS to Table 3-3 and Table 3-47. Added HAST to Table 3-56. Note: Table numbers are accurate as of the version 8.1 printing.
05/08/2012	9.0	Changes in many tables to show the first-quarter, 2012 test data. Added Xilinx 7 series FPGAs.

Date	Version	Revision *(Cont'd)*
08/22/2012	9.1	Changes in many tables to show the second-quarter, 2012 test data. Chapter 1, The Reliability Program Added entries for the following devices: XC6SLX4, XC6SLX9 Removed obsolete reliability data for the following devices: XC4VSX25, XC4VSX55, XCV600E Chapter 2, Results by Product Family Added entries for the following devices: XC17S150A, XC3S250E, XC6VLX195T, XC7K410T, XC7VX485T, XC9536 Removed obsolete reliability data for the following devices: XC17(S)xxx, XC17(S)xxx(X)L, XC17(S)xxxE, XC1702L, XC17S15A, XC17S200A, XC17S50XL, XC17Sxxx, XC17SxxxA, XC17SxxxXL, XC17Vxxx, XC18V01, XC18V02, XC18V04, XC18V512, XC18Vxxx, XC2C64, XC2S100E, XC2S150E, XC2V1500, XC2V3000, XC2VP100, XC2VP70, XC2VPxxx, XC2Vxxx, XC3S1000, XC3S100E, XC3S1400AN, XC3S200A, XC3SD1800A, XC3SDxxxA, XC3SxxxA, XC3SxxxAN, XC4013XLA, XC4VLX15, XC4VLX200, XC4VLX80, XC4VSX25, XC4VSX55, XC4xxxXLA, XC5VLX50T, XC6SLX150T, XC6SLX45, XC6SLX45T, XC6VLX130T, XC6VLX760, XC95144XL, XC95144XV, XC95288XV, XC95xxxXL, XC95xxxXV, XCF01S, XCF04S, XCF08P, XCF16P, XCF32P, XCFxxx, XCFxxxP, XCFxxxS, XCS20, XCS40XL, XCSxxx, XCSxxxXL, XCV1000E, XCV1600E, XCV400, XCV400E, XCV405E, XCV600E, XCV812E, XCVxxx (shrink), XCVxxxE, XCVxxxE (shrink) Chapter 3, Results by Package Type Added entries for the following devices: XC7K410T, XC7VX485T Removed obsolete reliability data for the following devices: XC17256E, XC17S100A, XC17S100XL, XC17S200A, XC17S50A, XC18V01, XC2C128, XC2C256, XC2S300E, XC2V1000, XC2V250, XC2V500, XC2V6000, XC2V80, XC2VP100, XC2VP50, XC2VP70, XC3S1500, XC3S4000, XC3S5000, XC4085XLA, XC4VLX100, XC4VLX25, XC5215, XC5VLX50, XC6SLX150T, XC6SLX16, XC6SLX45, XC6SLX45T, XC6VLX130T, XC6VLX240T, XC6VLX475T, XC6VLX760, XCE2VP50, XCF01S, XCF02S, XCF04S, XCF08P, XCF16P, XCF32P, XCR3064XL, XCS40XL, XCV1000E (shrink), XCV1600E, XCV2000E, XCV2000E (shrink), XCV300E (shrink), XCV600, XCV600E

Date	Version	Revision *(Cont'd)*
02/12/2013	9.2	Changed many tables to show the third quarter, 2012 test data. Added Xilinx 7 series FPGAs. Chapter 1, The Reliability Program: Added XC7K160T, XC7K410T, XC7K420T, XC7K480T, XC7V585T, and XC7VX485T devices to Table 1-15 ESD and Latch-up Data for 7 Series FPGAs. Chapter 2, Results by Product Family: Added Table 2-34 THB Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-95 HAST Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-103 HASTU Test Results for Si Gate CMOS Device Type XC4xxxE, Table 2-110 HASTU Test Results for Si Gate CMOS Device Type XCVxxxE, Table 2-111 HASTU Test Results for Si Gate CMOS Device Type XCVxxxE (Shrink), Table 2-120 HASTU Test Results for Si Gate CMOS Device Type XCE4VxXxxx, Table 2-125 High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC4xxxXLA, Table 2-126 High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCSxxx, Table 2-141 High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCE4VxXxxx, and Table 2-160 Autoclave Test Results for Si Gate CMOS Device Type XCFxxxS/P. Chapter 3, Results by Package Type: Packages FF665, FF672, FF676, FFG665, FFG672, and FFG896 were added. Added Table 3-47 Test Results of Device Types XC5VLX30T and Table 3-56 Test Results of Device Type XC2V1000.
04/02/2013	9.3	Changed many tables to show fourth quarter, 2012 test data. Added Xilinx 7 series FPGAs and Zynq®-7000 All Programmable SoCs. Chapter 1, The Reliability Program: Added XC7A100T, XC7A200T, XC7K70T, and XC7Z020 devices to Table 1-15 ESD and Latch-up Data for 7 Series FPGAs. Failure rate data changed in Table 1-16 Summary of the Failure Rates. Text and data changed in SEU and Soft Error Rate Measurements, page 26. Chapter 2, Results by Product Family: Data in many tables was updated. Added Table 2-33 THB Test Results for Si Gate CMOS Device Type XCVxxx, Table 2-35 THB Test Results for Si Gate CMOS Device Type XC2Vxxx, Table 2-38 THB Test Results for Si Gate CMOS Device Type XC2SxxxE, Table 2-93 HAST Test Results for Si Gate CMOS Device Type XC4xxxE, and Table 2-104 HASTU Test Results for Si Gate CMOS Device Type XC4xxxXLA. Deleted Table 2-167, Summary of the Test Results for device XC2Cxxx/A from Temperature Humidity Test, page 76. Chapter 3, Results by Package Type: Data in many tables was updated. Added packages CS144, CS324, BGG575, FFG324 and their respective test results in Table 3-9 Test Results for Device Types XCV50, XC2V80, Table 3-11 Test Results for Device Types XC6SLX45, XC6SLX45T, Table 3-29 Test Results for Device Types XC2V1000, XC2V1500, and Table 3-49 Test Results of Device Types XC5VLX50.

Date	Version	Revision *(Cont'd)*
05/13/2013	9.4	Changed many tables to show first quarter, 2013 test data. Chapter 1, The Reliability Program: Added 7 series devices XC7VX330T, XC7VX415T, XC7VX550T, XC7VX690T and Zynq-7000 AP SoC devices XC7Z010, XC7Z030, and XC7Z045 to Table 1-15 ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 AP SoCs. Updated data for 0.25 µm, 0.35 µm, and 0.5 µm process technologies in Table 1-16 Summary of the Failure Rates. Updated data for 40 nm, 45 nm, and 28 nm technology nodes in Table 1-17 Real Time Soft Error Rates. Chapter 2, Results by Product Family: Data in many tables was updated. Removed duplicate Table 2-17 HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XCE2Vxxx. Deleted Table 2-69, Temperature Cycling Test Results for Si Gate CMOS Device Type XC4xxxXLA. Added Table 2-85 Temperature Cycling Test Results for Si Gate CMOS Device Type XCE4VxXxxx. Chapter 3, Results by Package Type: Data in many tables was updated. Added packages FFG1761 and FFG1927 and their test results.

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Chapter 3: Results by Package Type

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Chapter 1

The Reliability Program

Overview

Xilinx publishes this report to provide customers with insight regarding the reliability of Xilinx® products. Reliability is defined as product performance to specification over time in response to varied (specified) environmental stress conditions. The goal of the reliability program is to achieve continuous improvement in the robustness of each product being evaluated.

As part of this program, finished product reliability is measured periodically to ensure that the product performance meets or exceeds reliability specifications. Reliability programs are executed in response to internal programs.

The Reliability Program

The reliability qualifications of new devices, wafer processes, and packages are designed to ensure that Xilinx products satisfy internal requirements before transfer into production. The reliability qualification and monitoring requirements are outlined in Table 1-1 through Table 1-16. The reliability stress tests are conducted according to the conditions specified in JEDEC Solid State Technology Association' s reliability test methods for packaged devices, JESD22, except Group B and D tests in which it follows DSCC test methods, MIL-STD-883.

Product Qualification

Wafer Process

The reliability tests used for wafer process qualification are summarized in Table 1-1.

Table 1-1: **Wafer Process Qualification Tests**

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
High-temperature operating life (HTOL)	$T_J \geq 125°C$, V_{DD} Max	1,000 hours	3	77	200 FIT(1) 50 FIT(2)
THB(3) or High-accelerated stress test (HAST)(3)	85°C, 85% RH, V_{DD}	1,000 hours	3	25	0 failures
	130°C, 85% RH, V_{DD}	96 hours			
	110°C, 85% RH, V_{DD}	264 hours			

Table 1-1: **Wafer Process Qualification Tests *(Cont'd)***

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
Temperature humidity (TH)(3) or Unbiased high accelerated stress test (HASTU)(3)	85°C, 85% RH	1,000 hours	3	25	0 failures
	130°C, 85% RH	96 hours			
	110°C, 85% RH	264 hours			
Temperature cycling (TC)(3)(4)(5)(6)	–65°C to +150°C	500 cycles	3	25	0 failures
	–55°C to+125°C	1,000 cycles			
	–40°C to +125°C	1,000 cycles			
Data Retention Bake(7) or High Temperature Storage (HTS)	T_A = 150°C	1,000 hours	3	25	0 failures
Program Erase(8)	T_A = 25°C	10,000 cycles	1	32	0 failures

Notes:

1. Phase I production is released as the qualification data demonstrates, meeting the required 200 FIT failure rate and other test requirements.
2. Phase II production is released as the qualification data demonstrates, meeting the required 50 FIT failure rate and other test requirements.
3. Package preconditioning is performed prior to THB, HAST, temperature cycling, TH, and HASTU tests.
4. For plastic QFP packages: –65°C to +150°C and 500 cycles or –55°C to +125°C and 1,000 cycles.
5. For plastic BGA packages: –55°C to +125°C and 1,000 cycles.
6. For flip chip packages: –55°C to +125°C and 1,000 cycles or –40°C to +125°C and 1,000 cycles.
7. For CPLD and EPROM products.
8. This is not a mandatory test and only for CPLD and EPROM products.

Non-Hermetic and Hermetic Packages

Moisture sensitivity and reflow temperature information can be found in *Device Package User Guide* (UG112).

Package/Assembly

The non-hermetic package/assembly qualification is outlined in Table 1-2. However, for hermetic package qualification, a full group B and D test per MIL-STD-833, *Test Methods*, is required.

Table 1-2: **Non-Hermetic Package/Assembly Qualification**

Reliability Test	Conditions	Duration	Lot Quantity	Sample Size per Lot	Acceptance Criteria
THB(1) or HAST(1)	85°C, 85% RH, V_{DD}	1,000 hours	3	25	0 failures
	130°C, 85% RH, V_{DD}	96 hours			
	110°C, 85% RH, V_{DD}	264 hours			
Temperature cycling(1) (2)(3),(4)	–65°C to +150°C	500 cycles,	3	25	0 failures
	–55°C to +125°C	1,000 cycles			
	–40°C to +125°C	1,000 cycles			
Autoclave(1) or temperature humidity unbiased(1) or HASTU(1)	121°C, 100% RH	96 hours	3	25	0 failures
	85°C, 85% RH	1,000 hours			
	130°C, 85% RH or 110°C, 85% RH	96 hours or 264 hours			
High-Temperature Storage (HTS)	T_A=150°C	1,000 hours	3	25	0 failures

Notes:

1. Package preconditioning is performed prior to THB, HAST, temperature cycling, autoclave, TH, and HASTU tests.
2. For plastic BGA packages: –55°C to +125°C and 1,000 cycles.
3. For flip chip packages: –55°C to +125°C and 1,000 cycles or –40°C to +125°C and 1,000 cycles.
4. For plastic QFP packages: –65°C to +150°C and 500 cycles or –55°C to +125°C and 1,000 cycles.

Device

The qualification process for new devices is shown in Table 1-3.

Table 1-3: **Device Qualification**

Reliability Test	Conditions	Lot Quantity	Sample Size per Lot	Acceptance Criteria
ESD	HBM(1)	1	3	1,000V
ESD	CDM(2)	1	3	250V(3)
Latch-up	Current injection	1	3	200 mA

Notes:

1. HBM = Human Body Model.
2. CDM = Charge Device Model.
3. GT transceiver CDM level is specified per JEP157.

Reliability Monitor Program

Wafer Process

The wafer process reliability monitor program is based on the maturity of the wafer process, the number of device hours, and the FIT rate. All processes are divided into one of two classes to determine how often the process is monitored annually. Class 1 processes are monitored every quarter; Class 2 processes are monitored every other quarter. FIT Rate calculations for both classes are based on approximately one million device hours (at T_J = 125°C) per fab if the data is available. Processes that are four years old or less are monitored every quarter regardless of the FIT rate. Mature processes older than four years are monitored based on the FIT Rate. Table 1-4 summarizes the classification criteria and monitoring frequency for both classes.

Table 1-4: **Monitoring Process Classes**

	Class 1	Class 2
Classification Criteria	Process Age ≤ 4 years or FIT > 26 (for FPGAs) FIT > 55 (for Flash PROM)	Process Age > 4 years and FIT < 26 (for FPGAs) FIT < 55 (for Flash PROMs)
Monitor Frequency	4 times per year	2 times per year

The reliability tests used to monitor the wafer process are shown in Table 1-5.

Table 1-5: **Tests Used to Monitor Wafer Processes**

Reliability Test	Condition	Duration	Lot Quantity	Sample Size per Process per Family per Quarter
HTOL	T_j > 125°C, V_{DD} Max	1,000 hours	1	45
Data Retention Bake(1)	T_A = 150°C	1,000 hours	1	45

Notes:

1. For CPLD and PROM products.

Package/Assembly

The package reliability monitor program takes into consideration the following factors:

- Package construction (wire-bond lead frame, wire-bond BGA, or flip chip)
- Factory location (assembly site, or wafer fabrication site)
- Substrate vendor
- Die size
- Technology maturity
- Past history

Based on these factors and availability, representative packages are drawn from inventory for the stress tests defined in Table 1-6. These tests are typically conducted on a quarterly basis, but the number of tests can be reduced or eliminated based on the maturity of the

package technology, understanding of failure mechanisms, and their dependency on the stress test.

Table 1-6: **Tests Used by the Reliability Package Monitor Program**

Reliability Test	Stress Conditions	Stress Duration	Sample Size	Frequency
THB(1) or HAST(1)	85°C, 85% RH, V_{DD}	1,000 hrs	45	WBLF(2) every even quarter WBBGA(3) every odd quarter Flip Chip (4) every quarter
	130°C, 85% RH, V_{DD}	96 hrs		
	110°C, 85% RH, V_{DD}	264 hrs		
Temperature cycling(1)(5)	–55°C to +125°C or –40°C to +125°C	1,000 cycles	45	WBLF every quarter WBBGA every quarter Flip Chip every quarter
Autoclave(1)(5) or Temperature humidity unbiased(1)(5) or HASTU(1)(5)	121°C, 100% RH	96 hrs	45	WBLF every odd quarter WBBGA every even quarter
	85°C, 85% RH	1,000 hrs		
	130°C, 85% RH or 110°C, 85% RH	96 hrs or 264 hrs		
HTS(7)	T_A=150°C	1,000 hrs	45	WBLF every quarter WBBGA every quarter

Notes:

1. Package preconditioning is performed prior to THB, HAST, temperature cycling, autoclave, TH, and HASTU tests.
2. For matured WBLF packages (PLCCs, SOICs, and DIPs packages), reliability monitoring is performed once a year.
3. For matured WBBGA packages (S-BGA Cavity-down BGA), reliability monitoring is performed once a year.
4. For flip chip packages, THB testing is performed every quarter and replaces the need for temperature humidity testing.
5. For plastic QFP and BGA packages: –55°C to +125°C and 1,000 cycles; for flip chip packages: –55°C to +125°C and 1,000 cycles or 40°C/+125°C and 1,000 cycles.
6. Refer to the device-specific qualification report for complete autoclave, temperature humidity, and HASTU reliability test data.
7. HTS stress is not applicable with flip chip package because the technology has no wire-bond IMC interface degradation.

Process Technology Family

Table 1-7 lists the Xilinx devices that support various process technologies.

Table 1-7: **Wafer Process Technology Family**

Process Technology	Device
0.028 µm	7 series FPGAs
0.040 µm	XC6VxXxxx, XCE6VxXxxx
0.045 µm	XC6Sxxx
0.065 µm	XC5VxXxxx, XCE5VxXxxx
0.09 µm	XC3Sxxx, XC3SxxxA, XC3SxxxAN, XC3SxxxE,XC3SDxxxA, XC4VxXxxx, XCE4VxXxxx
0.13 µm	XC2VPxxx, XCE2VPxxx
0.15 µm	XC2Vxxx, XCE2Vxxx

Table 1-7: **Wafer Process Technology Family *(Cont'd)***

Process Technology	Device
0.15 µm	XC18Vxxx, XCFxxxS/P
0.18 µm/ 0.15 µm	XCVxxxE (shrink), XC2SxxxE
0.18 µm	XCVxxxE, XC2Cxxx
0.22 µm/ 0.18 µm	XC2Sxxx, XCVxxx (shrink)
0.22 µm	XCVxxx
0.25 µm	XC4xxxXLA, XCSxxxXL, XC95xxxXV
0.35 µm/ 0.25 µm	XC95xxxXL
0.35 µm	XC4xxxXL, XCSxxx, XCRxxxXL
0.35 µm	XC17Vxxx, XC17SxxxA
0.5 µm	XC4xxxE, XC95xxx
0.6 µm	XC4xxx/L/E
0.6 µm	XC17(S)xxx/(X)L/E

ESD and Latch-up Summary

ESD results are obtained according to specifications ANSI/ESDA/JEDEC JS-001-2010 and JEDEC JESD22-C101. Latch-up results are obtained by using specification EIA/JESD78. ESD tests are performed at 25°C. In general, the latch-up data for newer products such as 7 series FPGAs, Virtex®-4, Virtex-5, Virtex-6, Spartan®-3, and Spartan-6 devices are collected at 125°C unless specified otherwise.

ESD and latch-up data are summarized by family in these tables:

- Table 1-8: PROMs, CPLDs, and older FPGAs
- Table 1-9: Virtex-II Pro devices
- Table 1-10 and Table 1-11: Virtex-4 devices
- Table 1-12: Virtex-5 devices
- Table 1-13: Spartan-6 devices
- Table 1-14: Virtex-6 devices
- Table 1-15: 7 series FPGAs

Table 1-8: **Product ESD and Latch-up Data**

Device	Latch-up	Human Body Model	Charge Device Model
XC17xxxD/L	±200 mA	±2,000V	+2,000V(1)
XC17xxxE, XC17Sxxx	±210 mA	±2,000V	±1,000V(2)
XC17Vxxx	±200 mA	±2,000V	±500V
XC18Vxxx	±200 mA	±2,000V	±500V(3)
XC31xxx/A	±250 mA	±1,750V to ±8,000V	±1,000V(4)
XC3xxx/A	±220 mA	±4,000V to ±7,000V	±2,000V(5)
XC4xxx/A	±300 mA	±1,000V to ±8,000V	±2,000V(6)
XC4xxxE	±250 mA	±3,000V to ±8,000V	±2,000V(7)
XC4xxxEX	±250 mA	±3,000V to ±7,000V	±2,000V(8)
XC4xxxXL	±250 mA	±2,000V to ±8,000V	±1,000V(9)
XC4xxxXLA	±260 mA	±2,000V to ±7,000V	±500V (Core)/ ±1,000V (corner)(10)
XCVxxx	±200 mA	±1,000V to ±2,000V	±500V(11)
XCVxxxE	±210 mA	±1,000V to ±2,500V(12)	±300V(13)
XCVxxxE/XC2SxxxE	±210 mA	±2,000V to ±3,000V	±500V(14)
XCSxxx	±310 mA	±6,000V	±1,000V(15)
XCSxxxXL	±250 mA	±3,000V	±500V(16)
XC2Sxxx	±210 mA	±2,000V	±500V(17)
XC5xxx	±250 mA	±3,000V to ±7,000V	±2,000V(18)
XC95xxx	±200 mA	±2,000V to ±3,000V	±1,000V(19)
XC95xxxXL	±200 mA	±2,000V to ±3,000V	±1,000V(20)
XC95xxxXV	±200 mA	±2,000V to ±3,000V	±500V(21)
XCRxxxL	±200 mA	±2,000V to ±3,000V	±500V(22)
XC2Vxxx	±200 mA	±750V to 2,000V(23)	±500V
XC2Cxxx	±200 mA	±2,000V	±500V
XC3Sxxx	±200 mA	±2,000V	±500V
XC3SxxxE	±200 mA	±2,000V	±500V
XC3SxxxA	±200 mA	±2,000V	±500V

Table 1-8: **Product ESD and Latch-up Data *(Cont'd)***

Device	Latch-up	Human Body Model	Charge Device Model
XC3SxxxAN	±200 mA	±2,000V	±500V
XC3SDxxxA	±200 mA	±2,000V	±500V
XC18Vxxx(ST)	±200 mA	±2,000V	±500V
XCFxxxS/P	±200 mA	±2,000V	±500V

Notes:

1. Measured on XC1765D
2. Measured on XC17256E
3. Measured on XC18V04
4. Measured on XC3190/A
5. Measured on XC3090
6. Measured on XC4005
7. Measured on XC4005E
8. Measured on XC4010E
9. Measured on XC4028X
10. Measured on XC4062XLA
11. Measured on XCV800
12. Only XCV100E and XCV812E have ESD threshold below 2KV, (XCV100E passed at 1.5KV and XCV812E passed at 1KV)
13. Measured on XCV50E
14. Measured on XCV2600 (shrink) and XCV3200 (shrink)
15. Measured on XCS10 and XCS30
16. Measured on XCS30XL
17. Measured on XC2S200
18. Measured on XC5210
19. Measured on XC95108
20. Measured on XC9536XL
21. Measured on XC95288XV
22. Measured on XCR3064XL
23. Human body model data collected on XC2V40, XC2V80, XC2V250, XC2V500, XC2V1000, XC2V1500, XC2V2000, XC2V3000, XC2V4000, XC2V6000, and XC2V8000

    Using the human body model, these devices have a threshold below 2KV: The XC2V40 passes at 1.75KV. The XC2V4000 (from UMC 8D) passes at 1.5KV. The XC2V500 pass at 750V.

    Results do not include DXN and DXP temperature sensing pins.

    Results do not include VBATT pins for XC2VxxxX devices.

The ESD results in Table 1-9 do not include DXN and DXP temperature sensing pins.

Table 1-9: **ESD and Latch-up Data for XC2VPxxx**

Device	Latch-up ±200 mA	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		Regular I/O and Power	MGT	Regular I/O and Power	MGT
XC2VP2	Pass	±1,500V	±2,000V	±500V	±300V
XC2VP4	Pass	±2,000V	±1,500V	±500V	±300V
XC2VP7	Pass	±2,000V	±1,000V	±500V	±500V
XC2VP20	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP30	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP40	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP50	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP70	Pass	±2,000V	±2,000V	±500V	±300V
XC2VP100	Pass	±2,000V	±1,000V	±500V	±300V
XC2VPX20	Pass	±2,000V	±1,500V	±400V	±200V

Table 1-10: **ESD and Latch-up Data for XC4VFXxxx**

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		STDIO	MGT	STDIO	MGT
XC4VFX12	pass	±2,000V	N/A	±450V	N/A
XC4VFX60	pass	±2,000V	±1,000V	±500V	±300V
XC4VFX40	pass	±2,000V	±1,000V	±500V	±300V
XC4VFX20	pass	±2,000V	±1,000V	±500V	±300V
XC4VFX100	pass	±2,000V	±1,000V	±450V	±300V
XC4VFX140	pass	±2,000V	±1,000V	±500V	±300V

Table 1-11: **ESD and Latch-up Data for XC4VLXxxx and XC4VSXxxx**

Device	Latch-up	Human Body Model Passing Voltage	Charge Device Mode Passing Voltage
XC4VLX15	pass	±2,000V	±500V
XC4VLX25	pass	±2,000V	±450V
XC4VLX40	pass	±2,000V	±450V
XC4VLX60	pass	±2,000V	±400V
XC4VLX80	pass	±2,000V	±450V
XC4VLX100	pass	±2,000V	±350V
XC4VLX160	pass	±2,000V	±450V
XC4VLX200	pass	±2,000V	±350V
XC4VSX25	pass	±2,000V	±500V
XC4VSX35	pass	±2,000V	±450V
XC4VSX55	pass	±2,000V	±400V

Table 1-12: **ESD and Latch-up Data for XC5VxXxxx/T**

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		SelectIO(1)	GTP	SelectIO	GTP
XC5VLX20T	pass	±2,000V	±1,000V	±400V	±250V
XC5VLX30	pass	±2,000V	N/A	±400V	N/A
XC5VLX30T	pass	±2,000V	±1,000V	±400V	±250V
XC5VLX50	pass	±2,000V	N/A	±400V	N/A
XC5VLX50T	pass	±2,000V	±1,000V	±400V	±250V(2)
XC5VLX85	pass	±2,000V	N/A	±400V	N/A
XC5VLX85T	pass	±2,000V	±1,000V	±400V	±250V(2)
XC5VLX110	pass	±2,000V	N/A	±400V(3)	N/A

Table 1-12: **ESD and Latch-up Data for XC5VxXxxx/T**

Device	Latch-up	Human Body Model Passing Voltage		Charge Device Model Passing Voltage	
		SelectIO[1]	GTP	SelectIO	GTP
XC5VLX110T	pass	±2,000V	±1,000V	±400V[3]	±250V[2]
XC5VLX155	pass	±2,000V	N/A	±400V	N/A
XC5VLX155T	pass	±2,000V	±1,000V	±400V	±250V[4]
XC5VLX220	pass[5]	±2,000V	N/A	±400V	N/A
XC5VLX220T	pass[5]	±2,000V	±1,000V	±400V	±250V[4]
XC5VLX330	pass[6]	±2,000V	N/A	±400V	N/A
XC5VLX330T	pass[6]	±2,000V	±1,000V	±400V	±250V[2]
XC5VFX30T	pass	±2,000V	±1,000V	±400V	±250V
XC5VFX70T	pass	±2,000V	±1,000V	±400V	±250V
XC5VFX100T	pass	±2,000V	±1,000V	±400V	±250V
XC5VFX130T	pass	±2,000V	±1,000V	±400V	±250V
XC5VFX200T	pass	±2,000V	±1,000V	±400V	±250V
XC5VSX35T	pass	±2,000V	±1,000V	±400V	±250V
XC5VSX50T	pass	±2,000V	±1,000V	±400V	±250V[2]
XC5VSX95T	pass	±2,000V	±1,000V	±400V	±250V
XC5VSX240T	pass	±2,000V	±1,000V	±400V	±250V[2]
XC5VTX150T	pass	±2,000V	±1,000V	±400V	±250V
XC5VTX240T	pass	±2,000V	±1,000V	±400V	±250V

Notes:

1. Human body model passing voltage for VBATT pin is 1,000V. This data is updated based on the data collected after the HBM tester was upgraded to remove the HBM-ESD trailing pulse.
2. If an internal AC coupling capacitor is used in the GTP receiver input (RX) pin, charge device model passing voltage is 200V. Compliance to ANSI/ESD S20.20 (ESD Association standard for the electrostatic discharge control program) is necessary.
3. Charge device model passing voltage for VBATT pin is 300V.
4. If an internal AC coupling capacitor is used in the GTP receiver input (RX) pin, the CDM level is 150V. Compliance to ANSI/ESD S20.20 (ESD Association standard for the electrostatic discharge control program) is necessary.
5. The D_IN and CS_B pins on XC5VLX220 and XC5VLX220T devices pass at 150 mA.
6. The D_IN, CS_B, and RDWR_B pins on XC5VLX300 and XC5VLX330T devices pass at 150 mA.

Table 1-13: **ESD and Latch-up Data for XC6Sxxx**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO	GTP	SelectIO	GTP
XC6SLX4	Pass	±2,000V	N/A	±500V	N/A
XC6SLX9	Pass	±2,000V	N/A	±500V	N/A
XC6SLX16	Pass	±2,000V	N/A	±500V	N/A
XC6SLX25	Pass	±2,000V	N/A	±500V	N/A

Table 1-13: **ESD and Latch-up Data for XC6Sxxx *(Cont'd)***

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO	GTP	SelectIO	GTP
XC6SLX25T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX45	Pass	±2,000V	N/A	±500V	N/A
XC6SLX45T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX75	Pass	±2,000V	N/A	±500V	N/A
XC6SLX75T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX100	Pass	±2,000V	N/A	±500V	N/A
XC6SLX100T	Pass	±2,000V	±2,000V	±500V	±400V
XC6SLX150	Pass	±2,000V	N/A	±500V	N/A
XC6SLX150T	Pass	±2,000V	±2,000V	±500V	±450V

Table 1-14: **ESD and Latch-up Data for XC6VxXxxx**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC6VLX75T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX130T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX195T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX240T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX365T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX550T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VLX760	Pass	±2,000V(1)	N/A	±500V(2)	N/A
XC6VSX315T	Pass	±2,000V(1)	±1,000V	±500V(2)	±200V
XC6VSX475T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V
XC6VHX250T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V
XC6VHX255T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V
XC6VHX380T	Pass	±2,000V(1)	±1,000V	±500V(2)	±250V
XC6VHX565T	Pass	±2,000V(1)	±1,000V	±500V(2)(3)	±250V

Notes:

1. If the system monitor function is used, HBM passing voltage is: ±1,000V for all of the devices.
2. If the system monitor function is used, CDM passing voltage for the AVDD, AVSS, VN, VP, VREFN, VREFP, DXN and DXP pins is: ±200V for XC6VLX130T, XC6VLX195T, XC6VLX240T, XC6VSX315T, XC6VHX250T, XC6VHX255T, and XC6VHX565T devices; ±150V for XC6VLX75T, XC6VLX365T, XC6VLX550T, XC6VLX760, XC6VSX475T, and XC6VHX380Tdevices. The DXN and DXP pins can withstand CDM voltages up to 500V without impacting the temperature sensing function.
3. The CDM passing voltage for the CCLK pin of the XC6VSX475T, XC6VHX250T, XC6VHX255T, and XC6VHX565T devices is 450V.

Table 1-15: **ESD and Latch-up Data for 7 Series FPGAs and Zynq-7000 AP SoCs**

Device	Latch-Up	HBM Passing Voltage		CDM Passing Voltage	
		SelectIO and Special Functions	Transceiver	SelectIO and Special Functions	Transceiver
XC7A100T	Pass	±2,000V	±1,500V	±350V	±300V
XC7A200T	Pass	±2,000V	±1,500V	±350V	±250V
XC7K70T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K160T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K325T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K355T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K410T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K420T	Pass	±2,000V	±1,500V	±350V	±300V
XC7K480T	Pass	±2,000V	±1,500V	±350V	±300V
XC7V585T	Pass	±2,000V	±1,500V	±350V	±250V
XC7VX330T	Pass	±2,000V	±1,500V	±350V	±250V
XC7VX415T	Pass	±2,000V	±1,500V	±350V	±250V
XC7VX485T	Pass	±2,000V	±1,500V	±350V	±250V
XC7VX550T	Pass	±2,000V	±1,500V	±350V	±200V
XC7VX690T	Pass	±2,000V	±1,500V	±350V	±200V
XC7Z010	Pass	±2,000V	N/A	±350V	N/A
XC7Z020	Pass	±2,000V	N/A	±350V	N/A
XC7Z030	Pass	±2,000V	±1,500V	±350V	±300V
XC7Z045	Pass	±2,000V	±1,500V	±350V	±300V

Failure Rate Determination

The failure rate is typically defined in FIT units. One FIT equals 1 failure per 1 billion device hours. For example, 5 failures expected out of 1 million components operating for 1,000 hours have a failure rate of 5 FIT. The following is the failure rate calculation method:

$$\text{Failure Rate} = \frac{x^2 10^9}{2(\text{No. of Devices})(\text{No. of Hours})(\text{Acc. Factor})} \qquad \textit{Equation 1-1}$$

where:

x^2 = Chi-squared value at a desired confidence level and (2f + 2) degrees of freedom, where f is the number of failures.

The acceleration factor is calculated using the Arrhenius relationship:

$$A = \exp\left\{\frac{E_a}{k}\cdot\left(\frac{1}{T_{J1}} - \frac{1}{T_{J2}}\right)\right\} \qquad \textit{Equation 1-2}$$

where:

E_a = Thermal activation energy (0.7eV is assumed and used in failure rate calculation except EPROM in which 0.58 eV is used).

A = Acceleration factor

k = Boltzman's constant, 8.617164 x 10^{-5} eV/°K

T_{J1} = Use junction temperature in degrees Kelvin (°K = °C + 273.16)

T_{J2} = Stress junction temperature in degrees Kelvin (°K = °C + 273.16)

Failure Rate Summary

Table 1-16: **Summary of the Failure Rates**

Process Technology	Device Hours at T_J = 125°C	FIT(1)
0.028 µm	686,644	17
0.040 µm	1,582,458	16
0.045 µm	1,031,587	11
0.065 µm	2,953,609	9
0.09 µm	8,556,490	6
0.13 µm	2,326,476	5
0.15 µm (FPGA)	3,215,846	4
0.15 µm (EPROM)	2,110,352	12
0.18/0.15 µm	2,554,004	10
0.18 µm	3,774,429	14
0.22/0.18 µm	2,124,940	6
0.22 µm	1,960,000	6
0.25 µm	3,126,619	4
0.35 µm/0.25 µm	2,097,253	6
0.35 µm	4,347,370	12
0.35 µm (EPROM)	1,045,774	24
0.5 µm	2,120,647	12
0.6 µm	847,674	14
0.6 µm (EPROM)	1,069,748	23

Notes:

1. FIT is calculated based on 0.7 eV (0.58 eV for EPROM), 60% C.L. and T_J of 55°C.

SEU and Soft Error Rate Measurements

Table 1-17 shows the soft error rates caused by single event upsets (SEUs) affecting memory cells used as configuration memory and block RAM. Neutron cross-sections are determined from LANSCE beam testing according to JESD89A/89-3A. Soft error rates (in FIT/Mb) are determined from real time (system level) measurements in various locations and altitudes and corrected for New York City, according to JESD89A/89-1A. All data is current as of date of this report.

An upset in any configuration bit does not create a soft functional error per se. The bit has to be one that is critical to the function in order for a soft error to occur. The ratio of unused bits and non-critical bits reduces the soft error rate by what is known as the device vulnerability factor (DVF). The DVF for a typical design is 5% (one in 20 upsets, on average, cause a functional soft error). In the worst case, the DVF is never smaller than one in ten, or never more than 10% of the upsets cause a soft functional error.

The DVF is predicted by the Xilinx ISE tools, along with the non-essential (unused) bits. The tools also provide the predicted average soft error rate for the user's design (the DVF varies with individual designs from below 2% to as much as 10%). Detection, correction, testing, and mitigation of these soft errors are provided for by the Soft Error Mitigation (SEM) IP cores.

The SEM IP core can be found at the following link:
www.xilinx.com/products/intellectual-property/SEM.htm

Note: The actual SEU FIT rate of a design running in a Xilinx FPGA is far lower than what is predicted by direct calculation from the numbers in Table 1-17. This is because most FPGA routing resources are unused within any particular implementation.

Table 1-17: **Real Time Soft Error Rates**

Technology Node	Product Family	Neutron Cross-section per Bit(1)			FIT/Mb (Alpha Particle)(2)			FIT/Mb (Real Time Soft Error Rate)(3)		
		Config. Memory	Block	Error	Config. Memory	Block RAM	Error(4)	Config. Memory	Block RAM	Error(4)
250 nm	Virtex	9.90×10^{-15}	9.90×10^{-15}	±10%				160	160	±20%
180 nm	Virtex-E	1.12×10^{-14}	1.12×10^{-14}	±10%				181	181	±20%
150 nm	Virtex-II	2.56×10^{-14}	2.64×10^{-14}	±10%				405	478	±8%
130 nm	Virtex-II Pro	2.74×10^{-14}	3.91×10^{-14}	±10%				437	770	±8%
90 nm	Virtex-4	1.55×10^{-14}	2.74×10^{-14}	±10%				263	484	±11%
65 nm	Virtex-5	6.70×10^{-15}	3.96×10^{-14}	±10%				165	692	–13% +15%
40 nm	Virtex-6	1.26×10^{-14}	1.14×10^{-14}	±10%	16	54	-50% +100%	98	216	-17% +21%
90 nm	Spartan-3	2.40×10^{-14}	3.48×10^{-14}	±10%				190	373	–50% +80%

Table 1-17: **Real Time Soft Error Rates *(Cont'd)***

Technology Node	Product Family	Neutron Cross-section per Bit[1]			FIT/Mb (Alpha Particle)[2]			FIT/Mb (Real Time Soft Error Rate)[3]		
		Config. Memory	Block	Error	Config. Memory	Block RAM	Error[4]	Config. Memory	Block RAM	Error[4]
90 nm	Spartan-3E Spartan-3A	1.31×10^{-14}	2.73×10^{-14}	±10%				104	293	–80% +90%
45 nm	Spartan-6	1.00×10^{-14}	2.20×10^{-14}	±10%	135	180	–50% +100%	192	402	–13% +15%
28 nm	7 Series FPGAs	6.99×10^{-15}	6.32×10^{-15}	±10%	34	53	-50% +100%	86	78	-17% +21%

Notes:

1. Data from Los Alamos Neutron Science Center (LANSCE).
2. Spartan-6 and 7 series FPGAs data based on thorium foil testing and package alpha emissivity of 0.0015 counts/cm^2/hr. Virtex-6 FPGA alpha data estimated using Virtex-6 Real Time Soft Error Rate Results.
3. Data compiled from the Rosetta experiment which includes upsets from neutron secondaries and packaging alpha particles. See *Continuing Experiments of Atmospheric Neutron Effects on Deep Submicron Integrated Circuits* (WP286).
4. 90% confidence interval.
5. Configuration memory and block RAM memory utilization is reported by the ISE tools. For accurate soft error failure rate estimation, consult the tool reports.

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Chapter 2

Results by Product Family

FPGA Products

High-Temperature Operating Life (HTOL) Test

The HTOL test is conducted under the conditions of $T_J \geq 125°C$ temperature, maximum V_{DD}, and either dynamic or static operation. The FIT failure rate calculation in the following tables is based on the assumption of 0.7 eV activation energy and 60% confidence level (CL).

Summary

The failures listed in Table 2-1 are also listed in each family device table with failure analysis results in the footnotes.

Table 2-1: **Summary of HTOL Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC4xxx/E (0.6 µm)	14	0	639	374,844	847,676	14
XC4xxx/E (0.5 µm)	12	1	519	998,220	1,052,368	25
XC4xxxXL	26	3	1,067	1,443,697	2,230,289	24
XC4xxxXLA	13	0	569	1,062,445	1,080,033	11
XCSxxx	14	0	615	904,488	1,025,411	11
XCSxxxXL	13	0	584	991,557	1,011,248	12
XC2Sxxx	10	0	451	910,538	1,043,392	11
XCVxxx	20	0	870	1,326,750	1,960,000	6
XCVxxx (shrink)	12	0	486	959,922	1,081,545	11
XCVxxxE	31	3	1,240	1,768,713	2,741,592	20
XCVxxxE (shrink)	17	1	580	1,013,551	1,497,009	17
XC2SxxxE	15	0	781	845,263	1,056,995	11
XC2Vxxx	21	0	923	1,688,841	2,129,807	6

Table 2-1: **Summary of HTOL Test Results *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCE2Vxxx	9	0	395	792,767	1,086,039	11
XC2VPxxx	9	0	402	770,056	1,164,218	10
XCE2VPxxx	8	0	384	834,489	1,162,258	10
XC3Sxxx	10	0	445	802,610	1,017,942	12
XC3SxxxE	9	0	436	743,573	1,007,462	12
XC3SxxxA	10	0	469	895,817	1,068,403	11
XC3SxxxAN	9	0	435	830,832	1,103,223	11
XC3SDxxxA	7	0	293	565,731	1,020,458	12
XC6Sxxx	4	0	176	352,332	1,031,587	11
XC4VxXxxx	9	2	469	938,617	2,099,825	19
XCE4VxXxxx	9	1	405	609,952	1,239,177	21
XC5VxXxxx	9	1	539	1,042,053	2,322,729	11
XCE5VxXxxx	3	0	249	249,000	630,879	19
XC6VxXxxx	7	1	334	629,660	1,078,904	24
XCE6VxXxxx	3	0	240	240,000	503,554	23
7 Series FPGAs	4	0	320	559,916	686,644	17

Data

Table 2-2: **HTOL Test Results for 0.6 µm Si Gate CMOS Device Type XC4xxx/E**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC4005E	2	0	94	24,064	63,878	
XC4010E	9	0	411	202,494	539,467	
XC4013E	2	0	87	136,254	212,393	
XC4025E	1	0	47	12,032	31,939	
XC4xxx/E	14	0	639	374,844	847,676	14 FIT

Table 2-3: **HTOL Test Results of 0.5 µm, Si Gate CMOS Device Type XC4xxx/E**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC4006E	1	0	45	90,180	94,506	
XC4008E	1	0	45	90,585	90,585	
XC4010E	3	0	135	271,485	284,572	
XC4013E	7	1(1)	294	545,970	582,705	
XC4xxx/E	12	1	519	998,220	1,052,368	25 FIT

Notes:

1. Failure at post 2,006 hours. Failure analysis was not performed.

Table 2-4: **HTOL Test Results for 0.35 µm Si Gate CMOS Device Type XC4xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J > 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC4005XL	2	0	89	133,700	207,111	
XC4010XL	9	1(1)	398	653,141	888,820	
XC4020XL	2	0	93	186,000	334,904	
XC4028XL	4	0	150	144,132	302,705	
XC4036XL	4	0	183	145,252	218,721	
XC4044XL	2	0	63	126,840	133,009	
XC4062XL	3	2(2)	91	54,632	145,020	
XC4xxxXL	26	3	1,067	1,443,697	2,230,289	24 FIT

Notes:

1. The device failed at post 1,033 hours. No failure analysis was performed.
2. No defect was found at post 48 hours.

Table 2-5: **HTOL Test Results for 0.25 µm Si Gate CMOS Device Type XC4xxxXLA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC4020XLA	6	0	267	478,005	486,053	
XC4028XLA	2	0	89	157,000	160,343	
XC4044XLA	1	0	44	88,797	92,134	
XC4052XLA	1	0	42	84,000	86,860	
XC4085XLA	3	0	127	254,643	254,643	
XC4xxxXLA	13	0	569	1,062,445	1,080,033	11 FIT

Table 2-6: **HTOL Test Results for 0.35 µm Si Gate CMOS Device Type XCSxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at T_J > 125°C	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XCS05	1	0	39	78,351	78,351	
XCS20	4	0	173	258,723	347,399	
XCS30	4	0	181	340,038	357,228	
XCS40	5	0	222	227,376	242,433	
XCSxxx	14	0	615	904,488	11,025,411	11 FIT

Table 2-7: **HTOL Test Results for 0.25 µm Si Gate CMOS Device Type XCSxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XCS20XL	6	0	266	423,072	476,442	
XCS30XL	2	0	90	182,520	188,943	
XCS40XL	5	0	228	340,965	345,862	
XCSxxxXL	13	0	584	991,557	1,011248	12 FIT

Table 2-8: **HTOL Test Results for 0.22/0.18 µm Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XC2S100	2	0	89	178,088	204,672	
XC2S200	6	0	273	553,299	640,734	
XC2S30	2	0	89	179,151	197,985	
XC2Sxxx	10	0	451	910,538	1,043,391	11 FIT

Table 2-9: **HTOL Test Results for 0.22 µm Si Gate CMOS Device Type XCVxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCV50	5	0	225	410,580	438,147	
XCV100	1	0	45	90,090	97,778	
XCV150	2	0	90	180,360	194,470	
XCV200	3	0	138	277,263	318,260	
XCV300	5	0	284	309,695	822,081	
XCV800	2	0	44	28,402	38,484	
XCV1000	2	0	44	30,360	50,780	
XCVxxx	20	0	870	1,326,750	1,960,000	6 FIT

Table 2-10: **HTOL Test Results for 0.22/0.18 µm Si Gate CMOS Device Type XCVxxx (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCV300	2	0	90	180,315	202,304	
XCV400	3	0	118	216,351	238,202	
XCV600	4	0	171	348,867	401,968	
XCV800	2	0	62	124,209	135,267	
XCV1000	1	0	45	90,180	103,804	
XCVxxx	12	0	486	959,922	1,081,545	11 FIT

Table 2-11: **HTOL Test Results for 0.18 µm Si Gate CMOS Device Type XCVxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCV50E	2	0	84	126,630	336,137	
XCV100E	2	0	80	115,765	115,765	
XCV200E	3	0	165	215,436	571,872	
XCV600E	4	0	118	155,046	411,568	
XCV405E	4	1(1)	209	249,914	266,058	
XCV812E	4	0	159	266,663	284,177	
XCV1000E	2	0	97	98,080	98,081	
XCV1600E	5	1(2)	195	389,099	461,936	
XCV2000E	5	1(3)	133	156,080	195,998	

Table 2-11: **HTOL Test Results for 0.18 µm Si Gate CMOS Device Type XCVxxxE *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCVxxxE	31	3	1,240	1,768,713	2,741,592	20 FIT

Notes:

1. Functional failure at post 184 hours.
2. Marginal failure at post 501 hours.
3. No defect found at post 281 hours.

Table 2-12: **HTOL Test Results for 0.18/0.15 µm Si Gate CMOS Device Type XCVxxxE (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCV400E	2	0	90	181,800	223,121	
XCV1000E	7	0	234	359,873	580,352	
XCV2000E	6	0	211	402,274	623,932	
XCV2600E	1	1(1)	22	23,604	23,604	
XCV3200E	1	0	23	46,000	46,000	
XCVxxxE (shrink)	17	1	580	1,013,551	1,497,009	17 FIT

Notes:

1. No defect found at post 189 hours.

Table 2-13: **HTOL Test Results for 0.18/0.15 µm Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2S100E	6	0	275	278,162	415,349	
XC2S150E	1	0	45	91,665	110,293	
XC2S300E	7	0	416	384,671	416,410	
XC2S400E	1	0	45	95,765	114,943	
XC2SxxxE	15	0	781	845,263	1,056,995	11 FIT

Table 2-14: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2V40	4	0	179	341,438	419,193	
XC2V80	2	0	88	177,881	190,660	
XC2V250	1	0	45	68,400	79,796	
XC2V500	4	0	164	247,832	328,763	
XC2V1000	3	0	135	270,855	322,593	
XC2V1500	1	0	45	90,630	106,505	
XC2V3000	4	0	179	315,717	425,876	
XC2V4000	1	0	44	88,088	99,435	
XC2V6000	1	0	44	88,000	156,985	
XC2Vxxx	21	0	923	1,688,841	2,129,807	6 FIT

Table 2-15: **HTOL Test Results for 0.13 µm Si Gate CMOS Device Type XC2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J > 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2VP2	1	0	45	92,385	106,344	
XC2VP7	1	0	45	91,305	126,841	
XC2VP20	1	0	45	50,355	67,203	
XC2VP30	2	0	89	178,354	269,598	
XC2VP40	2	0	89	178,944	292,249	
XC2VP50	2	0	89	178,713	301,982	
XC2VPxxx	9	0	402	770,056	1,164,218	10 FIT

Table 2-16: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XCE2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J > 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCE2V1000	8	0	352	706,638	937,610	
XCE2V4000	1	0	43	86,129	148,429	
XCE2Vxxx	9	0	395	792,767	1,086,039	11 FIT

Table 2-17: **HTOL Test Results for 0.13 µm Si Gate CMOS Device Type XCE2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at T_J > 125°C	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XCE2VP7	2	0	134	399,152	399,152	
XCE2VP40	2	0	89	178,675	301,000	
XCE2VP50	3	0	139	234,662	410,490	
XCE2VP70	1	0	22	22,000	51,616	
XCE2VPxxx	8	0	384	834,489	1,162,258	10 FIT

Table 2-18: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XC3S400	4	0	175	306,035	374,236	
XC3S1000	4	0	180	361,080	463,462	
XC3S1500	2	0	90	135,495	180,244	
XC3Sxxx	10	0	445	802,610	1,017,942	12 FIT

Table 2-19: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XC3S250E	2	0	90	183,060	221,112	
XC3S500E	4	0	178	313,820	421,895	
XC3S700E	1	0	45	45,000	50,809	
XC3S1600E	2	0	123	201,693	313,646	
XC3SxxxE	9	0	436	743,573	1,007,462	12 FIT

Table 2-20: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at T_J = 125°C	Failure Rate at 60% CL and T_J = 55°C (FIT)
XC3S200A	2	0	49	49,629	53,551	
XC3S700A	1	0	54	108,000	129,608	
XC3S1400A	7	0	366	738,188	885,244	
XC3SxxxxA	10	0	469	895,817	1,068,403	11 FIT

Table 2-21: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC3S700AN	1	0	44	88,000	135,192	
XC3S1400AN	8	0	391	742,832	968,031	
XC3SxxxAN	9	0	435	830,832	1,103,223	11 FIT

Table 2-22: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC3SDxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC3SD1800A	2	0	90	180,135	276,987	
XC3SD3400A	5	0	203	385,596	743,471	
XC3SDxxxA	7	0	293	565,731	1,020,458	12 FIT

Table 2-23: **HTOL Test Results for 0.045 µm Si Gate CMOS Device Type XC6Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC6SLX100T	1	0	45	90,045	221,007	
XC6SLX45	2	0	86	172,287	382,566	
XC6SLX150T	1	0	45	90,000	428,013	
XC6Sxxx	4	0	176	352,332	1,031,587	11 FIT

Table 2-24: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC4VLX15	1	0	45	91,080	114,529	
XC4VLX40	1	0	80	160,000	233,235	
XC4VLX80	2	0	120	240,705	620,203	
XC4VLX160	2	2(1)	89	174,132	721,939	
XC4VFX20	1	0	45	92,475	139,875	
XC4VFX40	1	0	45	90,225	153,416	
XC4VFX12	1	0	45	90,000	116,627	
XC4VxXxxx	9	2	469	938,617	2,099,824	19 FIT

Notes:

1. Failure due to substrate defect. New process improvement has been implemented.

Table 2-25: **HTOL Test Results for 0.09 µm Si Gate CMOS Device Type XCE4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCE4VLX80	4	1(1)	181	249,075	700,578	
XCE4VLX40	2	0	89	179,302	283,169	
XCE4VSX25	3	0	135	181,575	255,431	
XCE4VxXxx	9	1	405	609,952	1,239,178	21 FIT

Notes:

1. Failure due to substrate defect. New process improvement has been implemented

Table 2-26: **HTOL Test Results for 0.065 µm Si Gate CMOS Device Type XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC5VLX155T	1	0	45	90,045	268,745	
XC5VLX110T	5	1(1)	327	617,753	1,090,246	
XC5VLX50T	2	0	125	250,045	615,887	
XC5VSX35T	1	0	42	84,210	347,851	

Table 2-26: **HTOL Test Results for 0.065 µm Si Gate CMOS Device Type XC5VxXxxx *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC5VxXxxx	9	1	539	1,042,053	2,322,729	11 FIT

Notes:

1. Failure due to substrate defect. New process improvement has been implemented.

Table 2-27: **HTOL Test Results for 0.065 µm Si Gate CMOS Device Type XCE5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCE05VL11	3	0	249	249,000	630,879	
XCE5VxXxxx	3	0	249	249,000	630,879	19 FIT

Table 2-28: **HTOL Test Results for 0.40 µm Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC6VLX130T	2	0	90	180,000	377,666	
XC6VLX240T	5	1(1)	244	449,660	701,238	
XC6VxXxxx	7	1	334	629,660	1,078,904	24 FIT

Notes:

1. One unit failed for configuration at post HTOL stress, but the root cause could not be identified during failure analysis.

Table 2-29: **HTOL Test Results for 0.040 µm Si Gate CMOS Device Type XCE6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCE06L24T	3	0	240	240,000	503,554	
XCE6VxXxxx	3	0	240	240,000	503,554	23 FIT

Table 2-30: **HTOL Test Results for 0.028 µm Si Gate CMOS Device Type 7 Series FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC7K325T	3	0	244	407,916	490,857	
XC7K410T	1	0	76	152,000	195,787	
7 Series FPGAs	4	0	320	559,916	686,644	17 FIT

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C and 85% RH and VDD bias. Package preconditioning is performed on the testing samples prior to the THB test.

The failures listed in Table 2-31 are also listed by device with failure analysis results in the footnotes.

Summary

Table 2-31: **THB Test Results for Si Gate CMOS Devices**

XC4xxxXLA	2	0	90	90,000
XCVxxx	1	0	45	45,000
XCVxxxE	1	0	34	34,000
XC2Vxxx	2	0	90	90,000
XC2VPxxx	5	0	165	165,000
XC2Sxxx	1	0	45	45,000
XC2SxxxE	3	0	135	135,000
XC3Sxxx	1	0	45	45,000
XC3SxxxE	8	0	359	359,000
XC4VxXxxx	9	0	343	343,000
XC5VxXxxx	5	0	224	224,900
XC6VxXxxx	7	0	275	275,540
7 Series FPGAs	6	0	150	150,000

Data

Table 2-32: **THB Test Results for Si Gate CMOS Device Type XC4xxxXLA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4020XLA	2	0	90	90,000
XC4xxxXLA	2	0	90	90,000

Table 2-33: **THB Test Results for Si Gate CMOS Device Type XCVxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV50	1	0	45	45,000
XCVxxx	1	0	45	45,000

Table 2-34: **THB Test Results for Si Gate CMOS Device Type XCVxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCVxxxE	1	0	34	34,000
XCVxxxE	1	0	34	34,000

Table 2-35: **THB Test Results for Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2V4000	1	0	45	45,000
XC2V6000F	1	0	45	45,000
XC2Vxxx	2	0	90	90,000

Table 2-36: **THB Test Results for Si Gate CMOS Device Type XC2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2VP20	1	0	45	45,000
XC2VP40	1	0	45	45,000
XC2VP50	3	0	75	75,000
XC2VPxxx	5	0	165	165,000

Table 2-37: **THB Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S30	1	0	45	45,000
XC2Sxxx	1	0	45	45,000

Table 2-38: **THB Test Results for Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S100E	1	0	45	45,000
XC2S150E	1	0	45	45,000
XC2S300E	1	0	45	45,000
XC2SxxxE	3	0	135	135,000

Table 2-39: **THB Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S400	1	0	45	45,000
XC3Sxxx	1	0	45	45,000

Table 2-40: **THB Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S100E	1	0	45	45,000
XC3S250E	2	0	90	90,000
XC3S500E	1	0	44	44,000
XC3S1200E	3	0	135	135,000
XC3S1600E	1	0	42	84,000
XC3SxxxE	8	0	359	359,000

Table 2-41: **THB Test Results for Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4VLX15	2	0	88	88,000
XC4VFX20	1	0	45	45,000
XC4VLX25	2	0	90	90,000
XC4VLX15	1	0	43	43,000
XC4VFX20	1	0	45	45,000
XC4VLX40	1	0	45	45,000
XC4VLX60	1	0	45	45,000
XC4VLX80	4	0	120	120,000
XC4VLX100	1	0	45	45,000
XC4VxXxxx	14	0	521	521,000

Table 2-42: **THB Test Results for Si Gate CMOS Device Type XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX85T	2	0	90	90,900
XC5VLX155T	3	0	134	134,000
XC5VxXxxx	5	0	224	224,900

Table 2-43: **THB Test Results for Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6VHX565T	1	0	45	45,540
XC6VLX195T	1	0	45	45,000
XC6VLX240T	4	0	140	140,000
XC6VLX365T	1	0	45	45,000
XC6VxXxxx	7	0	275	275,540

Table 2-44: **THB Test Results for Si Gate CMOS Device Type 7 Series FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7K325T	6	0	150	150,000
7 Series FPGAs	6	0	150	150,000

Temperature Humidity Test

The TH test is conducted under the conditions of 85°C and 85% RH Package preconditioning is performed on the testing samples prior to the TH test.

Summary

Table 2-45: **Summary of TH Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4xxxE	1	0	45	45,450
XC4xxxXLA	1	0	40	42,280
XCSxxx	1	0	20	20,100
XCSxxxXL	2	0	78	78,558
XCVxxx (shrink)	2	0	119	121,702
XCVxxxE	2	0	119	119,639
XCVxxxE (shrink)	5	0	219	220,626
XC2Sxxx	3	0	149	153,136
XC2SxxxE	2	0	122	122,089
XC2Vxxx	2	0	83	84,581
XC2VPxxx	2	0	79	79,896
XC3Sxxx	2	0	90	90,765
XC3SxxxE	1	0	45	45,315
XC3SxxxA	2	0	54	55,701
XC3SDxxxA	2	0	158	158,396
XC4VxXxxx	6	0	98	98,596
XC5VxXxxx	6	0	279	283,190
XC6VxXxxx	3	0	75	75,000
7 Series FPGAs	3	0	80	79,969

Data

Table 2-46: **TH Test Results for Si Gate CMOS Device Type XC4xxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4013E	1	0	45	45,450

Table 2-47: **TH Test Results for Si Gate CMOS Device Type XC4xxxXLA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4052XLA	1	0	40	42,280

Table 2-48: **TH Test Results for Si Gate CMOS Device Type XCSxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCS20	1	0	20	20,100

Table 2-49: **TH Test Results for Si Gate CMOS Device Type XCSxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCS40XL	2	0	78	78,558

Table 2-50: **TH Test Results for Si Gate CMOS Device Type XCVxxx (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV300	2	0	119	121,702

Table 2-51: **TH Test Results for Si Gate CMOS Device Type XCVxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV1600E	2	0	119	119,639

Table 2-52: **TH Test Results for Si Gate CMOS Device Type XCVxxxE (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV300E	2	0	90	90,675
XCV600E	1	0	40	40,280
XCVxxxE	1	0	45	45,315

Table 2-53: **TH Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S30	1	0	77	78,971
XC2S15	1	0	42	44,015

Table 2-53: **TH Test Results for Si Gate CMOS Device Type XC2Sxxx *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S200	1	0	30	30,150
XC2Sxxx	3	0	149	153,136

Table 2-54: **TH Test Results for Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S300E	2	0	122	122,809

Table 2-55: **TH Test Results for Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2V500	1	0	43	43,301
XC2V6000	1	0	40	41,280
XC2Vxxx	2	0	83	84,581

Table 2-56: **TH Test Results for Si Gate CMOS Device Type XC2VPxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2VP20	1	0	44	44,616
XC2VP40	1	0	35	35,280
XC2VPxxx	2	0	79	79,896

Table 2-57: **TH Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200	1	0	45	45,450
XC3S1500	1	0	45	45,315
XC3Sxxx	2	0	90	90,315

Table 2-58: **TH Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S500E	1	0	45	45,315
XC3SxxxE	1	0	45	45,315

Table 2-59: **TH Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1400A	2	0	54	55,701

Table 2-60: **TH Test Results for Si Gate CMOS Device Type XC3SDxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3SD3400A	2	0	158	158,396

Table 2-61: **TH Test Results for Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4VLX80	1	0	23	23,161
XC4VLX100	5	0	75	75,435
XC4VxXxxx	6	0	98	98,596

Table 2-62: **TH Test Results for Si Gate CMOS Device Type XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX50T	6	0	279	283,190

Table 2-63: **TH Test Results for Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6VLX240T	3	0	75	75,000
XC6VxXxxx	3	0	75	75,000

Table 2-64: **TH Test Results for Si Gate CMOS Device Type 7 Series FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7K325T	3	0	80	79,969
7 Series FPGAs	3	0	80	79,969

Temperature Cycling Test

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test.

Summary

Table 2-65: **Summary of Temperature Cycling Test Results(1)**

Device	Lot Quantity	Failures	Device on Test	Total Device Cycles
XC4xxxE	2	0	90	90,000
XC4xxxXL	1	0	45	45,000
XC4xxxXLA	2	0	90	90,000
XCSxxx	1	0	45	45,000
XCSxxxXL	4	0	180	180,000
XC2Sxxx	1	0	45	45,000
XC2SxxxE	3	0	135	135,000
XCVxxx	1	0	45	45,000
XCVxxx (shrink)	1	0	45	45,000
XCVxxxE (shrink)	3	0	135	137,250
XC2Vxxx	4	0	180	181,800
XC2VPxxx	7	0	273	273,000
XC3Sxxx	7	0	315	315,000
XC3SxxxE	18	0	789	803,210
XC3SxxxA	7	0	310	310,900
XC3SDxxxA	2	0	90	90,000
XC3SxxxAN	2	0	90	90,000
XC6Sxxx	10	0	449	448,000
XC4VxXxxx	15	0	550	550,900
XCE4Vxxx	1	0	45	45,000
XC5VxXxxx	15	0	494	494,000
XC6VxXxxx	24	1	777	776,000
7 Series FPGAs	27	0	760	760,653

Notes:

1. Failures listed in this table are also listed in each family device table with failure analysis results in the footnote.

Data

Table 2-66: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC4xxx/E**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC4013E	B: –55°C to +125°C	2	0	90	90,000

Table 2-67: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC4xxxXL**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC4005XL	B: –55°C to +125°C	1	0	45	45,000
XC4xxxXL	B: –55°C to +125°C	1	0	45	45,000

Table 2-68: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC4xxxXLA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC4020XLA	B: –55°C to +125°C	2	0	90	90,000
XC4xxxXLA	B: –55°C to +125°C	2	0	90	90,000

Table 2-69: **Temperature Cycling Test Results of Si Gate CMOS Device Type XCSxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCS10	B: –55°C to +125°C	1	0	45	45,000
XCSxxx	B: –55°C to +125°C	1	0	45	45,000

Table 2-70: **Temperature Cycling Test Results for Si Gate CMOS Device Type XCSxxxXL**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCS10XL	B: –55°C to +125°C	1	0	45	45,000
XCS20XL	B: –55°C to +125°C	2	0	90	90,000
XC2S30XL	B: –55°C to +125°C	1	0	45	45,000
XCS2xxXL	B: –55°C to +125°C	4	0	180	180,000

Table 2-71: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2S150	B: –55°C to +125°C	1	0	45	45,000
XC2Sxxx	B: –55°C to +125°C	1	0	45	45,000

Table 2-72: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2SxxxE**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2S50E	B: –55°C to +125°C	1	0	45	45,000
XC2S100E	B: –55°C to +125°C	1	0	45	45,000
XC2S150E	B: –55°C to +125°C	1	0	45	45,000
XC2SxxxE	B: –55°C to +125°C	3	0	135	135,000

Table 2-73: **Temperature Cycling Test Results for Si Gate CMOS Device Type XCVxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCV200	B: –55°C to +125°C	1	0	45	45,000
XCVxxx	B: –55°C to +125°C	1	0	45	45,000

Table 2-74: **Temperature Cycling Test Results for Si Gate CMOS Device Type XCVxxx (Shrink)**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCV400	B: –55°C to +125°C	1	0	45	45,000
XCVxxx (shrink)	B: –55°C to +125°C	1	0	45	45,000

Table 2-75: **Temperature Cycling Test Results for Si Gate CMOS Device Type XCVxxxE (Shrink)**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCV400E	B: –55°C to +125°C	1	0	45	45,000
XCV1000E	B: –55°C to +125°C	2	0	90	92,250
XCVxxxE	B: –55°C to +125°C	3	0	135	137,250

Table 2-76: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2Vxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2V80	B: –55°C to +125°C	1	0	45	45,900
XC2V4000	B: –55°C to +125°C	1	0	45	45,000
XC2V6000	B: –55°C to +125°C	2	0	90	90,900
XC2Vxxx	B: –55°C to +125°C and G: –40°C to +125°C	4	0	180	181,800

Table 2-77: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC2VPxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2VP20	B: –55°C to +125°C	2	0	90	90,000
XC2VP40	B: –55°C to +125°C	1	0	45	45,000
XC2VP50	B: –55°C to +125°C	3	0	93	93,000
XC2VP100	B: –55°C to +125°C	1	0	45	45,000
XC2VPxxx	B: –55°C to +125°C	7	0	273	273,000

Table 2-78: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S200	B: –55°C to +125°C	2	0	90	90,000
XC3S400	B: –55°C to +125°C	1	0	45	45,000
XC3S1000	B: –55°C to +125°C	2	0	90	90,000
XC3S1500	B: –55°C to +125°C	2	0	90	90,000
XC3Sxxx	B: –55°C to +125°C	7	0	315	315,000

Table 2-79: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S100E	B: –55°C to +125°C	2	0	90	90,000
XC3S250E	B: –55°C to +125°C	3	0	135	135,900
XC3S500E	B: –55°C to +125°C	5	0	225	225,000
XC3S1200E	B: –55°C to +125°C	5	0	205	218,310
XC3S1600E	B: –55°C to +125°C	3	0	135	135,900
XC3SxxxE	B: –55°C to +125°C	18	0	790	803,210

Table 2-80: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S200A	B: –55°C to +125°C	1	0	45	45,000
XC3S400A	B: –55°C to +125°C	1	0	45	45,900
XC3S1400A	B: –55°C to +125°C	5	0	220	220,000
XC3SxxxA	B: –55°C to +125°C	7	0	310	310,900

Table 2-81: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SDxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3SD3400A	B: –55°C to +125°C	2	0	90	90,000
XC3SDxxxA	B: –55°C to +125°C	2	0	90	90,000

Table 2-82: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S200AN	B: –55°C to +125°C	1	0	45	45,000
XC3S700AN	B: –55°C to +125°C	1	0	45	45,000
XC3SxxxAN	B: –55°C to +125°C	2	0	90	90,000

Table 2-83: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC6Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6SLX4	B: –55°C to +125°C	2	0	90	90,000
XC6SLX9	B: –55°C to +125°C	1	0	45	45,000
XC6SLX16	B: –55°C to +125°C	2	0	90	90,000
XC6SLX45T	B: –55°C to +125°C	2	0	90	90,000
XC6SLX150T	B: –55°C to +125°C	3	0	134	134,000
XC6Sxxx	B: –55°C to +125°C C: –65°C to +150°C	10	0	449	449,000

Table 2-84: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC4VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC4VFX20	B: –55°C to +125°C	1	0	45	45,000
XC4VLX15	B: –55°C to +125°C	1	0	44	44,000
XC4VLX25	B: –55°C to +125°C	1	0	45	45,000
XC4VLX40	B: –55°C to +125°C	1	0	45	45,000
XC4VLX60	B: –55°C to +125°C	4	0	120	120,000
XC4VLX80	B: –55°C to +125°C	1	0	45	45,000
XC4VLX100	B: –55°C to +125°C	6	0	206	206,000
XC4VxXxxx	B: –55°C to +125°C	15	0	550	550,000

Table 2-85: **Temperature Cycling Test Results for Si Gate CMOS Device Type XCE4VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCE4VLX100	B: –55°C to +125°C	1	0	45	45,000
XCE4VxXxxx	B: –55°C to +125°C	1	0	45	45,000

Table 2-86: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC5VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC5VLX50	B: –55°C to +125°C	1	0	45	45,000
XC5VLX85T	B: –55°C to +125°C	2	0	90	90,000
XC5VLX110	B: –55°C to +125°C	3	0	75	75,000
XC5VLX110T	B: –55°C to +125°C	1	0	45	45,000
XC5VLX155T	B: –55°C to +125°C	5	0	165	165,000
XC5VLX330T	B: –55°C to +125°C	3	0	74	74,000
XC5VXxXxxx	B: –55°C to +125°C	15	0	494	494,000

Table 2-87: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC6VxXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6VHX565T	B: –55°C to +125°C	2	0	70	70,000
XC6VLX130T	B: –55°C to +125°C	4	0	139	139,000
XC6VLX195T	B: –55°C to +125°C	1	0	44	44,000
XC6VLX240T	B: –55°C to +125°C	2	1(1)	90	89,000
XC6VLX365T	B: –55°C to +125°C	3	0	135	135,000
XC6VSX475T	B: –55°C to +125°C	12	0	299	299,000
XC6VxXxxx	B: –55°C to +125°C	24	1	777	776,000

Notes:

1. Substrate short caused by inter-layer copper particle. Process control improvements implemented.

Table 2-88: **Temperature Cycling Test Results for Si Gate CMOS Device Type 7 Series FPGAs**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC7K325T	B: –55°C to +125°C	9	0	270	272,214
XC7K410T	B: –55°C to +125°C	7	0	200	200,436
XC7VX485T	B: –55°C to +125°C	5	0	129	127,028
XC7VX690T	B: –55°C to +125°C	6	0	161	160,975
7 Series FPGAs	B: –55°C to +125°C	27	0	760	760,653

Autoclave Test

The autoclave test is conducted under the conditions of 121°C, 100% RH (unbiased), and 29.7 PSI. Package preconditioning is performed on the testing samples prior to the autoclave stress test.

Summary

Table 2-89: **Summary of Autoclave Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3Sxxx	2	0	89	8,544
XC3SxxxE	1	0	45	4,320

Data

Table 2-90: **Autoclave Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200	2	0	89	8,544

Table 2-91: **Autoclave Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S100E	1	0	45	4,320

High Accelerated Stress Test

The HAST test is conducted under the conditions of 130°C, 85% RH and V_{DD} bias or 110°C, 85% RH and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the HAST test.

Summary

Table 2-92: **Summary of HAST Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4xxxE	1	0	45	4,320
XC2SxxxE	4	0	155	14,880
XCVxxxE	2	0	90	8,640
XCVxxxE (shrink)	3	0	111	12,672
XC3Sxxx	1	0	45	4,320
XC3SxxxA	4	0	180	38,640
XC3SDxxxA	3	0	134	27,984
XC6Sxxx	6	0	270	48,600
XC4VxXxxx	1	0	45	11,880

Data

Table 2-93: **HAST Test Results for Si Gate CMOS Device Type XC4xxxE**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC4013E	130°C, 85% RH	1	0	45	4,320

Table 2-94: **HAST Test Results for Si Gate CMOS Device Type XC2SxxxE**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2S100E	130°C, 85% RH	1	0	45	4,320
XC2S150E	130°C, 85% RH	2	0	65	6,240
XC2S300E	130°C, 85% RH	1	0	45	4,320
XC2SxxxE	130°C, 85% RH	4	0	155	14,880

Table 2-95: **HAST Test Results for Si Gate CMOS Device Type XCVxxxE**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCV405E	130°C, 85% RH	1	0	45	4,320
XCV1000E	130°C, 85% RH	1	0	45	4,320
XCVxxxE	130°C, 85% RH	2	0	90	8,640

Table 2-96: **HAST Test Results for Si Gate CMOS Device Type XCVxxxE (Shrink)**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCV400E	130°C, 85% RH	1	0	45	4,320
XCV600E	130°C, 85% RH	1	0	45	4,320
XCV1000E	130°C, 85% RH	1	0	21	4,032
XCVxxxE	130°C, 85% RH	3	0	111	12,672

Table 2-97: **HAST Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S1500	130°C, 85% RH	1	0	45	4,320

Table 2-98: **HAST Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3S1400A	130°C, 85% RH	4	0	180	38,640
XC3SxxxA	130°C, 85% RH	4	0	180	38,640

Table 2-99: **HAST Test Results for Si Gate CMOS Device Type XC3SDxxxA**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC3SD3400A	110°C, 85% RH	3	0	134	27,984
XC3SDxxxxA	110°C, 85% RH	3	0	134	27,984

Table 2-100: **HAST Test Results for Si Gate CMOS Device Type XC6Sxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC6SLX16	110°C, 85% RH	1	0	45	11,880
XC6SLX25T	110°C, 85% RH	1	0	45	11,880
XC6SLX45	110°C, 85% RH	1	0	45	11,880
XC6SLX45T	130°C, 85% RH	1	0	45	4,320
XC6SLX150T	130°C, 85% RH	2	0	90	8,640
XC6Sxxx		6	0	270	48,600

Table 2-101: **HAST Test Results for Si Gate CMOS Device Type XC4VLXxxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC4VLX80	110°C, 85% RH	1	0	45	11,880

Unbiased High Accelerated Stress Test

The HASTU test is conducted under the conditions of 130°C, 85% RH or 110°C, 85% RH. Package preconditioning is performed on the testing samples prior to the HAST test.

Summary

Table 2-102: **HASTU Test Results for Si Gate CMOS Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4xxxE	1	0	45	4,320
XC4xxxXLA	1	0	45	4,320
XCSxxx	3	0	135	12,960
XCSxxxXL	5	0	270	25,920
XC2Sxxx	4	0	180	17,280
XC2SxxxE	1	0	45	4,320
XCVxxx	3	0	134	12,864
XCVxxxE	1	0	45	4,320
XCVxxxE (shrink)	2	0	90	8,640
XC2Vxxx	1	0	45	4,320
XC3Sxxx	7	0	315	30,240
XC3SxxxE	14	0	607	91,536
XC3SxxxA	4	0	174	52,992

Table 2-102: **HASTU Test Results for Si Gate CMOS Devices *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3SxxxAN	5	0	157	15,072
XC3SDxxxA	4	0	180	17,280
XC6Sxxx	5	0	157	15,072
XC4VxXxxx	2	0	90	8,640
XCE4VxXxxx	1	0	45	4,320
XC5VxXxxx	2	0	90	8,640

Data

Table 2-103: **HASTU Test Results for Si Gate CMOS Device Type XC4xxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4013E	1	0	45	4,320
XC4xxxE	1	0	45	4,320

Table 2-104: **HASTU Test Results for Si Gate CMOS Device Type XC4xxxXLA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4013XLA	1	0	45	4,320
XC4xxxXLA	1	0	45	4,320

Table 2-105: **HASTU Test Results for Si Gate CMOS Device Type XCSxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCS10	2	0	90	8,640
XCS20	1	0	45	4,320
XCSxxx	3	0	135	12,960

Table 2-106: **HASTU Test Results for Si Gate CMOS Device Type XCSxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCS05XL	1	0	90	8,640
XCS10XL	1	0	45	4,320
XCS20XL	2	0	90	8,640
XCS30XL	1	0	45	4,320
XCSxxxXL	5	0	270	25,920

Table 2-107: **HASTU Test Results for Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S15	1	0	45	4,320
XC2S50	1	0	45	4,320
XC2S150	2	0	90	8,640
XC2Sxxx	4	0	180	17,280

Table 2-108: **HASTU Test Results for Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S50E	1	0	45	4,320
XC2SxxxE	1	0	45	4,320

Table 2-109: **HASTU Test Results for Si Gate CMOS Device Type XCVxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV100	1	0	45	4,320
XCV200	2	0	89	8,544
XCVxxx	3	0	134	12,864

Table 2-110: **HASTU Test Results for Si Gate CMOS Device Type XCVxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV405E	1	0	45	4,320
XCVxxxE	1	0	45	4,320

Table 2-111: **HASTU Test Results for Si Gate CMOS Device Type XCVxxxE (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV600E	1	0	45	4320
XCV1000E	1	0	45	4,320
XCVxxxE	2	0	90	8,640

Table 2-112: **HASTU Test Results for Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2V80	1	0	45	4,320
XC2Vxxx	1	0	45	4,320

Table 2-113: **HASTU Test Results for Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S1000	2	0	90	8,640
XC3S200	2	0	90	8,640
XC3S400	1	0	45	4,320
XC3S1500	2	0	90	8,640
XC3Sxxx	7	0	315	30,240

Table 2-114: **HASTU Test Results for Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S100E	4	0	180	17,280
XC3S1200E	6	0	250	31,560
XC3S250E	1	0	45	4,320
XC3S500E	5	0	225	21,600
XC3S1600E	5	0	222	47,016
XC3SxxxE	21	0	922	121,776

Table 2-115: **HASTU Test Results for Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200A	1	0	45	4,320
XC3S400A	1	0	45	4,320
XC3S1400A	2	0	84	44,352
XC3SxxxA	4	0	174	52,992

Table 2-116: **HASTU Test Results for Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3SxxxAN	5	0	157	15,072

Table 2-117: **HASTU Test Results for Si Gate CMOS Device Type XC3SDxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3SD1800A	1	0	45	4,320
XC3SD3400A	3	0	135	12,960
XC3SDxxxA	4	0	180	17,280

Table 2-118: **HASTU Test Results for Si Gate CMOS Device Type XC6Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6SLX4	2	0	90	8,640
XC6SLX9	1	0	45	4,320
XC6SLX16	1	0	45	4,320
XC6SLX150T	1	0	45	4,320
XC6Sxxx	5	0	157	15,072

Table 2-119: **HASTU Test Results for Si Gate CMOS Device Type XC4Vxxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4VSX25	1	0	45	4,320
XC4VSX35	1	0	45	4,320
XC4VxXxxx	2	0	90	8,640

Table 2-120: **HASTU Test Results for Si Gate CMOS Device Type XCE4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCE4VLX100	1	0	45	4,320
XCE4VxXxxx	1	0	45	4,320

Table 2-121: **HASTU Test Results for Si Gate CMOS Device Type XC5Vxxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX30T	1	0	45	4,320
XC5VLX50T	1	0	45	4,320
XC5VxXxxx	2	0	90	8,640

High-Temperature Storage Life

The High-Temperature Storage Life test is conducted under the conditions of 150°C and with the device unbiased.

Summary

Table 2-122: **Summary of High-Temperature Storage Life Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4xxxE	2	0	90	90,000
XC4xxxXL	1	0	45	48,240
XC4xxxXLA	1	0	45	45,000
XCSxxx	1	0	45	45,000
XCSxxxXL	4	0	180	180,000
XCVxxx	1	0	45	45,000
XCVxxx (shrink)	1	0	45	45,000
XCVxxxE (shrink)	1	0	45	45,000
XC2Sxxx	2	0	90	90,000
XC2SxxxE	3	0	134	134,000
XC2Vxxx	1	0	45	45,000
XC3Sxxx	6	0	270	270,000
XC3SxxxE	17	0	725	737,500
XC3SxxxA	6	0	250	251,080
XC3SDxxxA	2	0	90	90,000
XC3SxxxAN	6	0	185	185,000
XC6Sxxx	7	0	314	315,080
XC4VxXxxx	2	0	50	50,000
XCE4VxXxxx	1	0	45	45,000
XC5VxXxxx	2	0	90	90,900
XC6VxXxxx	6	0	117	117,000
7 Series FPGAs	3	0	80	80,108

Data

Table 2-123: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC4xxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4013E	2	0	90	90,000

Table 2-124: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC4xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4005XL	1	0	45	48,240
XC4xxxXL	1	0	45	48,240

Table 2-125: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC4xxxXLA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4020XLA	1	0	45	45,000
XC4xxxXLA	1	0	45	45,000

Table 2-126: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCSxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCS10	1	0	45	45,000
XCSxxx	1	0	45	45,000

Table 2-127: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCSxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCS10XL	1	0	45	45,000
XCS20XL	2	0	90	90,000
XCS30XL	1	0	45	45,000
XCSxxxXL	4	0	180	180,000

Table 2-128: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCVxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV200	1	0	45	45,000
XCVxxx	1	0	45	45,000

Table 2-129: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCVxxx (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV400	1	0	45	45,000
XCVxxx (shrink)	1	0	45	45,000

Table 2-130: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCVxxxE (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCV1000E	1	0	45	45,000
XCVxxxE (shrink)	1	0	45	45,000

Table 2-131: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC2Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S30	1	0	45	45,000
XC2S150	1	0	45	45,000
XC2Sxxx	2	0	90	90,000

Table 2-132: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC2SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2S50E	1	0	45	45,000
XC2S100E	1	0	45	45,000
XC2S150E	1	0	44	44,000
XC2SxxxE	3	0	134	134,000

Table 2-133: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC2Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2V80	1	0	45	45,000
XC2Vxxxx	1	0	45	45,000

Table 2-134: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200	2	0	90	90,000
XC3S1000	2	0	90	90,000
XC3S1500	2	0	90	90,000
XC3Sxxx	6	0	270	270,000

Table 2-135: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3SxxxE**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S100E	2	0	90	90,000
XC3S250E	3	0	135	135,000
XC3S500E	5	0	225	225,000
XC3S1200E	5	0	185	197,500
XC3S1600E	2	0	90	90,000
XC3SxxxE	17	0	725	737,500

Table 2-136: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S200A	1	0	45	45,000
XC3S400A	1	0	45	45,000
XC3S1400A	4	0	160	161,080
XC3SxxxA	6	0	250	251,080

Table 2-137: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3SDxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3SD3400A	2	0	90	90,000
XC3SDxxxA	2	0	90	90,000

Table 2-138: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC3SxxxAN**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC3S400AN	3	0	84	84,000
XC3S1400AN	3	0	101	101,000
XC3SxxxAN	6	0	185	185,000

Table 2-139: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC6Sxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6SLX4	1	0	45	45,000
XC6SLX9	1	0	45	45,000
XC6SLX16	2	0	89	90,080
XC6SLX150T	2	0	90	90,000

Table 2-139: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC6Sxxx *(Cont'd)***

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6SLX45T	1	0	45	45,000
XC6Sxxx	7	0	314	315,080

Table 2-140: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC4VLX80	2	0	50	50,000
XC4VxXxxx	2	0	50	50,000

Table 2-141: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XCE4VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCE4VLX100	1	0	45	45,000
XCE4VxXxxx	1	0	45	45,000

Table 2-142: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC5VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC5VLX30T	1	0	45	45,900
XC5VLX50T	1	0	45	45,000
XC5VxXxxx	2	0	90	90,900

Table 2-143: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type XC6VxXxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC6VHX255T	3	0	72	72,000
XC6VLX115T	3	0	45	45,000
XC6VxXxxx	6	0	117	117,000

Table 2-144: **High-Temperature Storage Life Test Results of Si Gate CMOS Device Type 7 Series FPGAs**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC7K325T	3	0	80	80,108
7 Series FPGAs	3	0	80	80,108

Flash PROM Products

HTOL Test

The HTOL test is conducted under the conditions of $T_J \geq 125°C$ temperature, maximum V_{DD}, and either dynamic or static operation. The FIT failure rate calculation in the following tables is based on the assumption of 0.7 eV activation energy and 60% confidence level (CL).

Summary

Table 2-145: **Summary of HTOL Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC17(S)xxx/(X)L	10	0	445	898,995	1,069,747	23
XC17Vxxx/XC17SxxxA	12	0	536	1,000,247	1,045,774	24
XC18Vxxx	16	0	715	760,225	1,004,700	25
XCFxxxS/P	12	0	482	1,067,500	1,105,652	22

Data

Table 2-146: **HTOL Test Results for 0.6 µm Si Gate CMOS Device Type XC17(S)xxx/(X)L**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC1702L	3	0	135	270,900	279,527	
XC1704L	1	0	45	90,225	98,248	
XC17S30XL	4	0	175	355,035	439,466	
XC17S40XL	2	0	90	182,835	252,506	
XC17Sxx/XL	10	0	445	898,995	1,069,747	23 FIT

Table 2-147: **HTOL Test Results of 0.35 µm Si Gate CMOS Device Type XC17Vxx/XC17SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC17V04	5	0	223	363,015	377,803	
XC17V08	3	0	135	275,856	298,948	
XC17V16	2	0	89	183,112	190,759	
XC17S50A	1	0	45	90,000	90,000	
XC17S200A	1	0	44	88,264	88,264	
XC17Vxx/ XC17SxxxA	12	0	536	1,000,247	1,045,774	24 FIT

Table 2-148: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type 18Vxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC18V02	6	0	265	265,000	303,152	
XC18V04	9	0	405	405,000	609,828	
XC18V512	1	0	45	90,225	91,720	
XC18Vxxx	16	0	715	760,225	1,004,700	25 FIT

Table 2-149: **HTOL Test Results for 0.15 µm Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCF08P	2	0	90	90,000	90,000	
XCF16P	4	0	122	730,000	730,000	
XCF32P	5	0	225	225,000	263,152	
XCF128X	1	0	45	22,500	22,500	
XCFxxxS/P	12	0	482	1,067,500	1,105,652	22 FIT

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C, 85% RH, and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test.

Summary

Table 2-150: **Summary of THB Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCFxxxS/P	8	0	360	600,480

Data

Table 2-151: **THB Test Results of Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCF16P	1	0	45	75,060
XCF32P	7	0	315	525,420
XCFxxxS/P	8	0	360	600,480

Temperature Humidity Test

The TH test is conducted under the conditions of 85°C and 85% RH. Package preconditioning is performed on the testing samples prior to the TH test.

Summary

Table 2-152: **Summary of TH Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17Vxxx	1	0	44	44,812

Data

Table 2-153: **TH Test Results of Si Gate CMOS Device Type XC17Vxxx/XC17SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17S100A	1	0	44	44,812
XC17Vxxx/XC17SxxxA	1	0	44	44,812

Temperature Cycling Tests

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in an air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test.

Summary

Table 2-154: **Summary of Temperature Cycling Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC17(S)xxx/(X)L/E	2	0	90	90,000
XCFxxxS/P	6	0	270	441,180

Data

Table 2-155: **Temperature Cycling Test Results for Si Gate CMOS Device XC17(S)xxx/(X)L/E**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC17S150A	B: –55°C to +125°C	1	0	45	45,000
XC17S200A	B: –55°C to +125°C	1	0	45	45,000
XC17(S)xxx/(X)L/E	B: –55°C to +125°C	2	0	90	90,000

Table 2-156: **Temperature Cycling Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCF32P	C: –65°C to +150°C	6	0	270	441,180
XCFxxxS/P	C: –65°C to +150°C	6	0	270	441,180

Autoclave Test

The autoclave test is conducted under the conditions of 121°C, 100% RH (unbiased), and 29.7 PSI. Package preconditioning is performed on the testing samples prior to the autoclave stress test.

Summary

Table 2-157: **Summary of Autoclave Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17(S)xxx/(X)L/E	1	0	43	4,128
XC17Vxxx/XC17SxxxA	1	0	45	4,320
XCFxxxS/P	6	0	270	25,920

Data

Table 2-158: **Autoclave Test Results for Si Gate CMOS Device Type XC17(S)xxx/(X)L/E**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC1702L	1	0	43	4,128
XC17(S)xxx/(X)L/E	1	0	43	4,128

Table 2-159: **Autoclave Test Results for Si Gate CMOS Device Type XC17Vxxx/XC17SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17S15A	1	0	45	4,320
XC17Vxxx/XC17SxxxA	1	0	45	4,320

Table 2-160: **Autoclave Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCF32P	6	0	270	25,920
XCFxxxS/P	6	0	270	25,920

Unbiased High Accelerated Stress Test

The HASTU test is conducted under the conditions of 130°C, 85% RH or 110°C, and 85% RH. Package preconditioning is performed on the testing samples prior to the HASTU test.

Summary

Table 2-161: **Summary of HASTU Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17Vxxx/XC17SxxxA	3	0	135	12,960

Data

Table 2-162: **HASTU Test Results for Si Gate CMOS Device Type XC17SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17S150A	1	0	45	4,320
XC17S200A	2	0	90	8,640
XC17SxxxA	3	0	135	12,960

Program/Erase Endurance Test

The Program/Erase Endurance test is conducted under nominal voltage and room temperature.

Qualification Data

Table 2-163: **Program/Erase Endurance Test Results of Si Gate CMOS Device Type XC18Vxxx/XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC18V04	1	0	32	640,000
XCF08P	1	0	16	320,000
XCF16P	2	0	93	1,860,000
XCF32P	2	0	93	1,860,000

Data Retention Bake Test

The data retention bake test is conducted at 150°C ambient temperature. The devices are programmed prior to the bake test.

Summary

Table 2-164: **Summary of Data Retention Bake Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17Vxxx/XC17SxxxA	2	0	90	90,900
XCFxxxS/P	6	0	270	450,360

Data

Table 2-165: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC17Vxxx/XC17SxxxA**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC17S200A	2	0	90	90,900
XC17Vxxx/XC17SxxxA	2	0	90	90,900

Table 2-166: **Data Retention Bake Test Results for Si Gate CMOS Device Type XCFxxxS/P**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCF32P	6	0	270	450,360
XCFxxxS/P	6	0	270	450,360

CPLD Products

HTOL Tests

The HTOL test is conducted under the conditions of $T_J > 125°C$ temperature, maximum V_{DD}, and either dynamic or static operation. The FIT calculations in Table 2-167 through Table 2-172 are based on the assumption of 0.7 eV activation energy and 60% confidence level.

Summary

Table 2-167: **Summary of HTOL Test Results(1)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC95xxx	8	0	350	686,000	1,068,278	11
XC95xxxXL	19	0	1056	1,534,319	2,097,253	6
XC95xxxXV	14	0	746	982,430	1,028,282	11
XCRxxxXL	12	0	538	1,018,580	1,019,944	12
XC2Cxxx/A	12	0	523	1,028,517	1,032,838	11

Notes:

1. Failures listed in this table are also listed in each family device table with failure analysis results in the footnote.

Data

Table 2-168: **HTOL Test Results for 0.5 µm Si Gate CMOS Device Type XC95xxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC95108	3	0	135	254,700	445,167	
XC95288	1	0	45	90,045	149,871	
XC9572	4	0	170	341,255	473,240	
XC95xxx	8	0	350	686,000	1,068,278	11 FIT

Table 2-169: **HTOL Test Results of 0.35 µm Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC951288XL	1	0	45	90,630	231,398	
XC95144XL	5	0	254	391,868	503,890	
XC95288XL	8	0	472	611,310	821,688	
XC9572XL	5	0	285	440,691	540,276	
XC95xxxXL	19	0	1056	1,534,319	2,097,253	6 FIT

Table 2-170: **HTOL Test Results of 0.25 µm Si Gate CMOS Device Type XC95xxxXV**

Device	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC9572XV	1	0	76	38,000	38,000	
XC95144XV	4	0	210	346,478	346,478	
XC95288XV	9	0	460	597,952	643,804	
XC95xxxXV	14	0	746	982,430	1,028,282	11 FIT

Table 2-171: **HTOL Test Results of 0.35 µm Si Gate CMOS Device Type XCRxxxXL**

Devices	Lot Quantity	Failures	Device on Test	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XCR3128XL	3	0	135	270,855	271,487	
XCR3256XL	3	0	135	247,953	248,327	
XCR3384XL	4	0	176	355,416	355,774	
XCR3512XL	2	0	92	144,356	144,356	
XCRxxxXL	12	0	538	1,018,580	1,019,944	12 FIT

Table 2-172: **HTOL Test Results of 0.18 µm Si Gate CMOS Device Type XC2Cxxx/A**

Devices	Lot Quantity	Fail Quantity	Device Quantity	Actual Device Hours at $T_J \geq 125°C$	Equivalent Device Hours at $T_J = 125°C$	Failure Rate at 60% CL and $T_J = 55°C$ (FIT)
XC2C128	2	0	90	181,350	181,690	
XC2C256	6	0	268	516,987	518,736	
XC2C384	4	0	165	330,180	332,412	
XC2Cxxx/A	12	0	523	1,028,517	1,032,838	11 FIT

Temperature Humidity with Bias Test

The THB test is conducted under the conditions of 85°C, 85% RH, and V_{DD} bias. Package preconditioning is performed on the testing samples prior to the THB test.

Data

Table 2-173: **THB Test Results for Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C64A	2	0	85	85,000
XC2C128	2	0	90	90,000
XC2C256	3	0	133	133,000
XC2Cxxx/A	8	0	353	353,000

Temperature Humidity Test

The TH test is conducted under the conditions of 85°C and 85% RH. Package preconditioning is performed on the testing samples prior to the TH test.

Summary

Table 2-174: **Summary of TH Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95xxx	1	0	30	30,060
XC95xxxXL	3	0	135	135,990
XCRxxxXL	2	0	69	128,985
XC2Cxxx/A	3	0	120	120,915

Data

Table 2-175: **TH Test Results of Si Gate CMOS Device Type XC95xxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95144	1	0	30	30,060
XC95xxx	1	0	30	30,060

Table 2-176: **TH Test Results of Si Gate CMOS Device Type XC95xxxXL (Shrink)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9572XL	1	0	45	45,315
XC95144XL	2	0	90	90,675
XC95xxxXL	3	0	135	135,990

Table 2-177: **TH Test Results of 0.35 µm Si Gate CMOS Device Type XCRxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCR3256XL	2	0	69	69,690
XCRxxxXL	2	0	69	69,690

Table 2-178: **TH Test Results of Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C64A	2	0	90	135,990
XC2C256	1	0	30	30,240
XC2Cxxx/A	3	0	120	120,915

Temperature Cycling Test

The temperature cycling test is conducted under the conditions of predefined maximum and minimum temperatures and in air-to-air environment. Package precondition is performed on the testing samples prior to the temperature cycling test.

Summary

Table 2-179: **Summary of Temperature Cycling Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95xxx	2	0	90	90,000
XC95xxxXL	4	0	180	1,801,350
XCRxxxXL	3	0	135	135,000
XC2Cxxx/A	17	0	763	763,000

Data

Table 2-180: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC95xxx**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC9536	B: -55°C to +125°C	1	0	45	45,000
XC9572	B: -55°C to +125°C	1	0	45	45,000
XC95xxx	B: -55°C to +125°C	2	0	90	90,000

Table 2-181: **Temperature Cycling Test Results for Si Gate CMOS Device Type XC95xxxL**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC9572XL	B: -55°C to +125°C	3	0	135	136,350
XC95144XL	B: -55°C to +125°C	1	0	45	45,000
XC95xxxXL	B: -55°C to +125°C	4	0	180	1,801,350

Table 2-182: **Temperature Cycling Test Results of Si Gate CMOS Device Type XCRxxxXL**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCR3064XL	B: –55°C to +125°C	1	0	45	45,000
XCR3256XL	B: –55°C to +125°C	2	0	90	90,000
XCRxxxXL	B: –55°C to +125°C	3	0	135	135,000

Table 2-183: **Temperature Cycling Test Results of Si Gate CMOS Device Type XC2Cxxx/A**

Device	Stress Condition	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2C64A	B: -55°C to +125°C	3	0	135	135,000
XC2C32A	B: -55°C to +125°C	1	0	45	45,000
XC2C128	B: -55°C to +125°C	5	0	225	225,000
XC2C256	B: -55°C to +125°C	6	0	268	268,000
XC2C384	B: -55°C to +125°C	2	0	90	90,000
XC2Cxxx/A	B: -55°C to +125°C	17	0	763	763,000

Autoclave Test

The autoclave test is conducted under the conditions of 121°C, 100% RH (unbiased), and 29.7 PSI. Package preconditioning is performed on the testing samples prior to the autoclave stress test.

Summary

Table 2-184: **Summary of Autoclave Test Results**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95xxxXL	1	0	41	3,936
XC2Cxxx	1	0	42	4,032

Data

Table 2-185: **Autoclave Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9572XL	1	0	41	3,936

Table 2-186: **Autoclave Test Results for Si Gate CMOS Device Type XC2Cxxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C128	1	0	42	4,032

Unbiased High Accelerated Stress Test

The HASTU test is conducted under the conditions of 130°C and 85% RH or 110°C and 85% RH. Package preconditioning is performed on the testing samples prior to the HASTU test.

Summary

Table 2-187: **HASTU Test Results for Si Gate CMOS Devices**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95xxx	1	0	45	4,320
XC95xxxXL	4	0	180	17,280
XCRxxxXL	3	0	135	12,960
XC2Cxxx/A	13	0	584	63,624

Data

Table 2-188: **HASTU Test Results for Si Gate CMOS Device Type XC95xxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC9572	1	0	45	4,320
XC95xxx	1	0	45	4,320

Table 2-189: **HASTU Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95144XL	1	0	44	4,224
XC9572XL	3	0	135	12,960
XC95xxxXL	4	0	180	17,280

Table 2-190: **HASTU Test Results for Si Gate CMOS Device Type XCRxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XCR3064XL	1	0	45	4,320
XCR3256XL	2	0	90	8,640
XCRxxxXL	3	0	135	12,960

Table 2-191: **HASTU Test Results for Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC2C128	3	0	135	12,960
XC2C256	5	0	225	12,160
XC2C384	2	0	90	8,640
XC2C32A	1	0	44	4,224
XC2C64A	2	0	90	8,640
XC2Cxxx/A	13	0	584	63,624

Program/Erase Endurance Test

The Program/Erase Endurance test is conducted under nominal voltage and predefined temperature.

Qualification Data

Table 2-192: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxx; Test Condition at 55°C**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9536	1	0	29	290,000
XC95108	1	0	80	875,120
XC95xxx	2	0	109	1,165,120

Table 2-193: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxx; Test Condition at –40°C**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9536	2	0	64	5,088,000

Table 2-194: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxxXL; Test Condition at –40°C**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95144XL	1	0	21	420,000

Table 2-195: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxxXL; Test Condition at 70°C**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95144XL	1	0	32	320,000

Table 2-196: **Erase Endurance Test Results for Si Gate CMOS Device Type XC95xxxXV; Test Condition at 70°C**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC95144XV	1	0	32	320,000

Table 2-197: **Erase Endurance Test Results of Si Gate CMOS Device Type XCRxxx/XL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCR3128	1	0	10	10,000
XCR3032XL	2	0	57	684,000

Data Retention Bake Test

The Data Retention Bake Test is conducted at 150°C. The devices are programmed prior to the bake test.

Summary

Table 2-198: **Summary of Data Retention Bake Test Results(1)**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Cycles
XC95xxx	3	0	135	135,225
XC95xxxXL	3	0	134	134,000
XCRxxxXL	4	0	180	180,000
XC2Cxxx/A	20	0	900	877,725

Notes:

1. Failures listed in this table are also listed in each family device table with failure analysis results in the footnote.

Data

Table 2-199: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC95xxx**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9536	1	0	45	45,225
XC9572	2	0	90	90,000
XC95xxx	3	0	135	135,225

Table 2-200: **Data Retention Bake Test Results for Si Gate CMOS Device Type XC95xxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC9572XL	3	0	134	134,000
XC95xxxXL	3	0	134	134,000

Table 2-201: **Data Retention Bake Test Results of Si Gate CMOS Device Type XCRxxxXL**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XCR3064XL	1	0	45	45,000
XCR3128XL	1	0	45	45,000
XCR3256XL	2	0	90	90,000
XCRxxxXL	4	0	180	180,000

Table 2-202: **Data Retention Bake Test Results of Si Gate CMOS Device Type XC2Cxxx/A**

Device	Lot Quantity	Fail Quantity	Device Quantity	Total Device Hours
XC2C128	7	0	315	292,500
XC2C256	6	0	270	270,000
XC2C384	2	0	90	90,000
XC2C32A	1	0	45	45,225
XC2C64A	4	0	180	180,000
XC2Cxxx/A	20	0	900	877,725

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Chapter 3

Results by Package Type

Reliability Data for Non-Hermetic Packages

PD8

Table 3-1: **Test Results for Device Types XC17256E, XC17S200A, XC17S40XL, and XC17S10**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature humidity -55°C to +125°C	2	0	90	90,000
Temperature cycling 85°C, 85% RH with bias	1	0	45	45,000
HTS	2	0	90	90,000
HASTU	1	0	45	4,320

VO20 and VO48

Table 3-2: **Test Results for Device Types XCF08P, XCF32P, XC18V01, XC18V02, and XC18V04**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –65°C to +150°C	2	0	90	144,000
Temperature humidity 85°C, 85% RH with bias	2	0	90	150,120
PP	2	0	90	8,640
HTS	1	0	45	75,060

PC44, PC84, and PC20

Table 3-3: **Test Results for Device Types XC1704L, XC17V16, XC18V04, XC9572XL, XCR3064XL, XCS05, XCS10XL, and XC4006E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
HASTU	1	0	45	4,320
HTS	2	0	90	90,225

PQ100, PQ160, PQ208, PQ240

Table 3-4: **Test Results for Device Types XC3S200, XC2S300E, XC4013E, XC4010XL, XC3S1500, XC95144, XC95216, XC95288XL, XC95288XV, XCR3512XL, and XCR3384XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	5	0	229	229,000
Temperature humidity 85°C, 85% RH with bias	1	0	45	45,000
HAST	1	0	45	4,320
HASTU	2	0	90	8,640
HTS	4	0	180	180,000

TQ100, TQ144

Table 3-5: **Test Results for Device Types XC2C256, XC2C384, XC2S50E, XC2S100/E, XC3S50A, XC3S200, XC3S400, and XC95288XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	7	0	270	271,080
HASTU	4	0	179	17,184
HTS	8	0	315	318,240

VQ44, VQ100

Table 3-6: **Test Results for Device Types XC1702L, XC17V04, XC18V02, XC18V04, XC2C128, XCS30, XCS20XL, XC9572XL, XC3S200, and XC3S250E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	2	0	90	90,000
HTS	2	0	90	90,000
HASTU	3	0	180	17,280

HQ208, HQ240

Table 3-7: **Test Results for Device Types XCV400 (Shrink), XCV600 (Shrink), XCV600E, XC95216, XC95288, and XC4028EX**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH no bias	1	0	40	40,240
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

BG352, BG432, BG560

Table 3-8: **Test Results for Device Types XCV1000E, XC1600E, XC4052XLA, XC4062XLA, and XCV300**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	1	0	34	34,000
HAST	2	0	66	8,352
HASTU	1	0	45	4,320
HTS	1	0	45	45,000
Temperature humidity 85°C, 85% RH no bias	2	0	90	90,810

CS144

Table 3-9: **Test Results for Device Types XCV50, XC2V80**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature humidity -55°C to +125°C	1	0	45	45,900
Temperature cycling 85°C, 85% RH with bias	1	0	45	45,000
HTS	1	0	45	45,000

CS280

Table 3-10: **Test Results for Device Types XC95288XL, XC95288XV, XCR3256XL, and XCR3512XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

CS324

Table 3-11: **Test Results for Device Types XC6SLX45, XC6SLX45T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	2	0	90	90,900
HTS	2	0	90	90,000

FS48

Table 3-12: **Test Results for Device Types XCF08P, XCF16P, and XCF32P**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –65°C to +150°C	7	0	347	561,320
Temperature humidity 85°C, 85% RH with bias	8	0	424	707,232
PP	8	0	822	78,912
HTS	8	0	1120	1,868,160

FG324, FG456, FG484

Table 3-13: **Test Results of Device Types XC2V250, XC3S1000, XC3S1500, XC6SLX45T, XC6SLX150T, XC2S300E, and XCR3512XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	2	0	90	90,000
HAST	1	0	45	4,320
HASTU	1	0	45	4,320
HTS	2	0	90	90,000
THB	1	0	45	45,000

FG676

Table 3-14: **Test Results for Device Types XC2VP20, XC3S1400A, XC3S1500, XC3SD1800A, XC6SLX150T, XC3SD3400A, XCE2V2000, and XCV600E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	4	0	168	168,000
HAST	4	0	180	14,880
HASTU	3	0	135	12,960
HTS	4	0	177	177,000

FG680

Table 3-15: **Test Results for Device Types XCV2000E, and XCV1000E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	47,250
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

FT256

Table 3-16: **Test Results for Device Types XCR3512XL, XC2S150E, XC2S300E, XC2S400E, XC2C512, XC3S1000, XC3S400A, XC3S1200E, XC3S200AN, XC3S200, XC3S50A, and XC3S200A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	1	0	45	45,000
Autoclave 121°C, 100% RH	1	0	44	4,224
HAST	1	0	45	4,320
HASTU	1	0	45	4,320
Temperature humidity 85°C, 85% RH no bias	1	0	45	47,745
HTS	1	0	44	44,000

FF665, FF668, FF672, FF676

Table 3-17: **Test Results for Device Types XC4VLX25, XC4VLX60, XC4VFX20, XC4VLX40, and XC7K410T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	5	0	145	145,375
Temperature humidity 85°C, 85% RH with bias	2	0	90	90,360
HASTU	1	0	45	4,320
HTS	1	0	44	44,000

FF1136, FF1148, FF1152

Table 3-18: **Test Results for Device Types XC4VLX60, XC4VLX100, XC4VLX160, XC4VFX60, XC2VP20, XC2VP50, XC2V6000, XC2V8000, XC2V4000, XC5VSX95T, XC5VLX50T, and XC5VLX110T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	5	0	225	225,900
HAST	1	0	45	11,880
Temperature humidity 85°C, 85% RH with bias	3	0	135	135,000

FF1156

Table 3-19: **Test Results for Device Types XC6VSX475T, XC6VLX240T, XC6VLX115T(1), XC6VLX195T, and XC6VLX130T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	2	0	30	30,000
TCB	1	1(2)	44	44,000
TH	2	0	30	30,000
THB	1	0	45	45,000

Notes:

1. XC6VLX115T is an internal product qualification vehicle.
2. Substrate short caused by inter-layer copper particle. Process control improvements implemented.

FF1923

Table 3-20: **Test Results for Device Types XC6VHX565T, XC6VHX255T and XC6VHX380T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55°C to +125°C	9	1(1)	147	147,850
Temperature humidity 85°C, 85% RH with bias	3	0	74	74,000
Temperature humidity 85°C, 85% RH no bias	3	0	74	74,000
High temperature storage	3	0	72	72,000

Notes:

1. One unit failed at post temperature cycling stress was due to a solder particle at bump. Post bump cleaning improvement is being implemented.

FF1513, FF1517

Table 3-21: **Test Results for Device Types XC2V6000, XC2V8000, XC2VP50, XC2VP70, XC4VLX100, XC4VLX200, XC4VLX160, and XC4VLX200**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	1	0	45	45,000
HASTU	1	0	45	4,320
Temperature cycling –55°C to +125°C	1	0	45	45,000

Reliability Data for Hermetic Packages

Reliability Data for PGA Packages

Table 3-22: **Tests of Package Types PG84, PG120, PG132, PG156, PG175, PG191, PG223, PG299, and PG475**

Code	Test	Sample Quantity	Failures	Total Device Cycles
B2	Resistance to solvents	15	0	
B3	Solderability	15	0	
B5	Bond strength	24	0	
D1	Physical dimension	30	0	
D2	Lead integrity	30	0	
	Seal			
D3	Thermal shock	30	0	450
	Temperature cycle			
	Seal			
	Visual examination			
	End-point electrical			
	Parametrics			
D4	Mechanical shock	30	0	
	Vibration, variable frequency			
	Constant acceleration			
	Seal			
	Visual examination			
	End-point electrical parameters			

Table 3-22: **Tests of Package Types PG84, PG120, PG132, PG156, PG175, PG191, PG223, PG299, and PG475 *(Cont'd)***

Code	Test	Sample Quantity	Failures	Total Device Cycles
D5	Salt atmosphere	30	0	
	Seal			
	Visual examination			
D6	Internal water-vapor content	30	0	
D7	Adhesion of lead finish	30	0	
D8	Lid Torque	15	0	

Reliability Data for CB Packages

Table 3-23: **Tests of Package Types CB-100, CB164, CB196, and CB228**

Code	Test	Sample Quantity	Failures	Total Device Cycles
B2	Resistance to solvents	48	0	
B3	Solderability	27	0	
B5	Bond strength	36	0	
D1	Physical dimension	60	0	
D2	Lead integrity	60	0	
	Seal			
D3	Thermal shock	60	0	
	Temperature cycle			
	Seal			
	Visual examination			
	End-Point electrical			
	Parametrics			
D4	Mechanical shock	60	0	
	Vibration, variable frequency			
	Constant acceleration			
	Seal			
	Visual examination			
	End-point electrical parameters			

Table 3-23: **Tests of Package Types CB-100, CB164, CB196, and CB228 *(Cont'd)***

Code	Test	Sample Quantity	Failures	Total Device Cycles
D5	Salt atmosphere	60	0	
	Seal			
	Visual examination			
D6	Internal water-vapor content	60	0	
D7	Adhesion of lead finish	60	0	
D8-LID	Lid Torque	30	0	
HTOL	Life Test	45	0	

Reliability Data for DD8 Packages

Table 3-24: **Tests of Package Type DD8**

Code	Test	Sample Quantity	Failures	Total Device Cycles
B2	Resistance to solvents	9	0	
B3	Solderability	9	0	
B5	Bond strength	12	0	
D1	Physical dimension	30	0	
D2	Lead integrity	30	0	
	Seal			
D3	Thermal shock	30	0	225
	Temperature cycle			1,500
	Seal			
	Visual examination			
	End-point electrical			
	Parametrics			
D4	Mechanical shock	30	0	
	Vibration, variable frequency			
	Constant acceleration			
	Seal			
	Visual examination			
	End-point electrical parameters			

Table 3-24: **Tests of Package Type DD8 *(Cont'd)***

Code	Test	Sample Quantity	Failures	Total Device Cycles
D5	Salt atmosphere	30	0	
	Seal			
	Visual examination			
D6	Internal water-vapor content	30	0	
D7	Adhesion of lead finish	30	0	
D8	Lead torque	15	0	

Reliability Data for Chip Scale CC44 Package

Table 3-25: **Tests of Package Type Chip Scale CC44**

Code	Test	Sample Quantity	Failures	Total Device Cycles
B2	Resistance to solvents	9	0	
B3	Solderability	9	0	
B5	Bond strength	12	0	
D1	Physical dimension	15	0	
D2	Lead integrity	15	0	
	Seal			
D3	Thermal shock	30	0	675
	Temperature cycle			4,500
	Seal			
	Visual examination			
	End-point electrical			
	Parametrics			
D4	Mechanical shock	15	0	
	Vibration, variable frequency			
	Constant acceleration			
	Seal			
	Visual examination			
	End-point electrical parameters			
D5	Salt atmosphere	30	0	
	Seal			
	Visual examination			

Table 3-25: **Tests of Package Type Chip Scale CC44 *(Cont'd)***

Code	Test	Sample Quantity	Failures	Total Device Cycles
D6	Internal water-vapor content	20	0	
D7	Adhesion of lead finish	18	0	
D8	Lead torque	15	0	

Reliability Data for CF1144 Package

Table 3-26: **Tests of Package Type CF1144**

Code	Test	Sample Quantity	Failures	Total Device Hours/Cycles
D3	Thermal shock	15	0	225
	Parametrics			
D4	Mechanical shock	15	0	
	High temperature storage	22	0	2,112
	Temperature cycling 65 to +155°C	15	0	1,500
	HAST (130°C, 85% RH)	18	0	1,728
TCB	Temperature cycling -55 to +125°C	14	0	29,260

Reliability Data for CG717 Package

Table 3-27: **Tests of Package Type CG717**

Code	Test	Sample Quantity	Failures	Total Device Hours/Cycles
	Thermal shock	15	0	225
	Mechanical shock	15	0	
	Vibration	15	0	225
	High temperature storage	22	0	2,112
	Temperature cycling 65 to +155°C	15	0	1,500
	HTOL	44	0	44,000

Reliability Data for Pb-Free Packages

BGG352, BGG432, BGG560

Table 3-28: **Test Results for Device Types XCV300E (Shrink), XCV405E, XCV600E (Shrink), XCV1000E (Shrink), and XC4062XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
TCB	1	0	45	45,000
HAST	2	0	66	8,352
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

BGG575

Table 3-29: **Test Results for Device Types XC2V1000, XC2V1500**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
TCB	2	0	90	90,000
HTS	2	0	90	90,000
HASTU	2	0	90	8,640

CPG132

Table 3-30: **Test Results for Device Types XC2C256, XC2C128, XC3S50, XC3S250E, and XC3S500E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	7	0	313	313,000
Temperature humidity 85°C, 85% RH with bias	2	0	90	90,000
HASTU	5	0	225	21,600
HTS	8	0	360	337,500

CPG196

Table 3-31: **Test Results for Device Type XC6SLX16**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	135	135,000
HASTU	3	0	135	12,960
HTS	2	0	89	89,000

CSG144

Table 3-32: **Test Results of Device Types XC95144XL, XCR3128XL, and XCV200E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	2	0	90	90,000
HASTU	2	0	90	8,640
HTS	2	0	90	90,000

CSG280

Table 3-33: **Test Results of Device Types XC95288XV, XCR3512XL, and XCR3256XL**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000
HASTU	1	0	45	4,320
HTS	1	0	45	45,000
Temperature humidity 85°C, 85% RH no bias	1	0	24	24,240

CSG324

Table 3-34: **Test Results of Device Types XC6SLX16, XC6SLX45, and XC6SLX45T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	2	0	90	90,000
HAST	3	0	135	28,080
HTS	3	0	135	136,080

CSG484

Table 3-35: **Test Results of Device Type XC6SLX150T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000
HAST	1	0	44	4,224
HTS	1	0	45	45,000

FGG320

Table 3-36: **Test Results of Device Types XC3S200, XC3S400A, XC3S1200E and XC3S1600E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HASTU	2	0	70	6,720
Temperature humidity 85°C, 85% RH with bias	1	0	25	25,000
Temperature cycling –55 to +125°C	4	0	160	173,400
HTS	2	0	70	70,000

FGG400

Table 3-37: **Test Results of Device Type XC3S1600E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	4	0	179	179,810
HASTU	4	0	180	17,280
HTS	4	0	180	180,000

FGG324, FGG456, and FGG484

Table 3-38: **Test Results of Device Types XC2V250, XC2VP4, XC2S300E, XC3S1500, XC3S1600E, XC3S700AN, XC3S1400AN, XC6SLX45T, and XC6SLX150T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	6	0	265	265,000
Temperature humidity 85°C, 85% RH with bias	1	0	42	84,000
HASTU	4	0	176	25,040
HAST	1	0	45	4,320
HTS	5	0	205	205,000

FGG676

Table 3-39: **Test Results of Device Types XCV405E, XCV800, XCV600E, XC2V3000, XC2VP20, XC2VP30, XC2VP40, XC2S600E, XC3S1500, XC3S2000, XC3S1400A, XC3S1400AN, XC3SD1800A, XC6SLX150T, and XC3SD3400A**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	135	135,000
Temperature humidity 85°C, 85% RH with bias	1	0	43	43,000
HAST	2	0	90	6,240
HASTU	2	0	90	8,640
HTS	2	0	90	90,000

FGG900

Table 3-40: **Test Results of Device Type XC6SLX150T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	2	0	89	89,000
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

FTG256

Table 3-41: **Test Results for Device Types XCR3512XL, XC2C512, XC2S150E, XC3S250E, XC2S300E, XC2S400E, XC3S1000, XC3S50A, XC3S200A, XC3S400A, XCR3512XL, and XC3S200AN**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	10	0	450	450,000
Temperature humidity 85°C, 85% RH with bias	3	0	135	135,000
Temperature humidity 85°C, 85% RH no bias	1	0	45	47,745
HAST	5	0	200	42,960
HASTU	7	0	309	73,512
HTS	8	0	340	253,580

PQG160, PQG208

Table 3-42: **Test Results of Device Types XC95144, XC95216, XCS40XL, XC2S200, XC2S300E, XC3S400, and XC3S500E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	8	0	360	360,000
Temperature humidity 85°C, 85% RH with bias	3	0	134	134,000
Temperature humidity 85°C, 85% RH no bias	1	0	33	33,198
HASTU	5	0	225	21,600
HTS	8	0	360	260,000

PCG44, PCG84

Table 3-43: **Test Results for Device Types XC9572XL, XCS05, XC18V02, and XC1702L**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	1	0	45	45,000

SOG20

Table 3-44: **Test Results for Device Types XC17S50A, XC17S100A, and XC18V01**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000
HTS	1	0	45	45,000

VQG44, VQG64, VQG100

Table 3-45: **Test Results of Device Types XCS30XL, XC18V02, XC18V04, XC2C64A, XC2C128, XC2C256, XC9572XL, XC3S200, XC3S250E, and XC3S100E**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	10	0	450	450,000
Temperature humidity 85°C, 85% RH with bias	3	0	135	135,000
Temperature humidity 85°C, 85% RH no bias	2	0	62	64,115
HASTU	8	0	360	34,560
HTS	11	0	494	494,000

TQG100, TQG144

Table 3-46: **Test Results of Device Types XC2S100, XC95144XL, XC95288XL, XC2C384, XC3S50A, XC3S200, XC3S400, XC3S100E, XC3S250E, XC4010XL, and XC3S50AN**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	11	0	495	496,250
Temperature humidity 85°C, 85% RH with bias	3	0	135	135,000
Temperature humidity 85°C, 85% RH no bias	2	0	75	75,600
HASTU	10	0	450	43,200
HTS	12	0	540	540,000

FFG665

Table 3-47: **Test Results of Device Types XC5VLX30T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	2	0	90	90,000
HTS	2	0	90	90,900
HASTU	2	0	90	8,640

FFG668, FFG672

Table 3-48: **Test Results of Device Types XC4VLX60**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	4	0	120	120,000
Temperature humidity 85°C, 85% RH with bias	2	0	90	90,360
HASTU	1	0	45	4,320
HTS	1	0	45	45,000

FFG324

Table 3-49: **Test Results of Device Types XC5VLX50**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000

FFG484, FFG784

Table 3-50: **Test Results of Device Types XC6VLX130T and XC6VLX240T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	2	0	50	50,000

FFG1136, FFG1148, FFG1152

Table 3-51: **Test Results of Device Types XC2V8000, XC2VP20, XC2VP50, XC4VLX60, XC4VLX100, XC4VLX160, XC4VFX60, XC4VSX95T, XC5VLX50T, and XC5VLX110T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	2	0	50	50,000
HTS	2	0	50	50,000

FFG1759, FFG1760

Table 3-52: **Test Results of Device Types XC6VSX475T, XC6VLX760 and XC6VLX240T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	6	0	149	149,000

FFG1156

Table 3-53: **Test Results of Device Types XC6VLX115T[1], XC6VLX130T, XC6VLX365T, XC6VSX475T, XC6VLX195T, and XC6VLX240T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
HTS	3	0	45	45,000
Temperature cycling –55 to +125°C	10	0	329	329,000
Temperature humidity 85°C, 85% RH no bias	3	0	75	75,000
Temperature humidity 85°C, 85% RH with bias	5	0	185	185,000

Notes:

1. XC6VLX115T is an internal product qualification vehicle.

FFG1923

Table 3-54: **Test Results of Device Types XC6VHX565T, XC6VHX255T and XC6VHX380T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	10	1[1]	329	329,000
Temperature humidity 85°C, 85% RH with bias	5	0	185	185,000
Temperature humidity 85°C, 85% RH no bias	3	0	75	75,000
High temperature storage	3	0	72	72,000

Notes:

1. One unit failed at post temperature cycling stress was due to a solder particle at bump. Post bump cleaning improvement is being implemented.

FFG676

Table 3-55: **Test Results of Device Type XC7K325T, XC7K410T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	7	0	175	175,375

FFG896

Table 3-56: **Test Results of Device Type XC2V1000**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000
HASTU	1	0	45	4,320
High temperature storage	1	0	45	45,000

FFG900

Table 3-57: **Test Results of Device Type XC7K325T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	6	0	155	157,214
Temperature humidity 85°C, 85% RH with bias	6	0	150	150,000
Temperature humidity 85°C, 85% RH no bias	3	0	80	79,969
High temperature storage	3	0	80	80,108

FFG1158

Table 3-58: **Test Results of Device Type XC7VX485T, XC7VX690T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	6	0	159	159,188

FFG1738

Table 3-59: **Test Results of Device Types XC5VLX330T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	74	74,000

FFG1761

Table 3-60: **Test Results of Device Types XC7VX485T, XC7VX690T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	2	0	52	50,245

FFG1927

Table 3-61: **Test Results of Device Types XC7VX485T, XC7VX690T**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	3	0	79	78,570

SFG363

Table 3-62: **Test Results of Device Types XC4VLX25**

Reliability Test	Lot Quantity	Failures	Device on Test	Total Device Hours/Cycles
Temperature cycling –55 to +125°C	1	0	45	45,000
Temperature humidity 85°C, 85% RH with bias	2	0	90	90,000
Temperature humidity 85°C, 85% RH no bias	1	0	45	45,000

Board-Level Reliability Tests, SnPb Eutectic

FG676, FG680, FG900, FG1156, BF957, FF672, FF896, FF1152, FF1704, SF363, and CF1144

Table 3-63: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FG676	27 x 27	676	1.00	0.60	0.46	SMD	17.8 x 17.8 x 0.3	0.56 thick, 4-layer
FG680	40 x 40	680	1.00	0.60	0.46	SMD	20.3 x 20.3 x 0.3	0.98 thick, 3-layer
FG900	31 x 31	900	1.00	0.60	0.46	SMD	17.0 x 17.0 x 0.3	0.56 thick, 4-layer

Table 3-63: **Package Details (All Dimensions in mm) *(Cont'd)***

Package	Size	I/O	Pitch	Ball/ Column Size	Pad Opening	Pad Type	Die Size	Substrate
FG1156	35 x 35	1,156	1.00	0.60	0.46	SMD	23 x 21 x 0.3	0.56 thick, 4-layer
BF957	40 x 40	957	1.27	0.75	0.61	SMD	22 x 20 x 0.7	1.152 thick, 6-layer
FF672	27 x 27	672	1.00	0.60	0.53	SMD	12 x 10 x 0.7	1.152 thick, 6-layer
FF896	31 x 31	896	1.00	0.60	0.53	SMD	10 x 10 x 0.7	1.152 thick, 6-layer
FF1152	35 x 35	1,152	1.00	0.60	0.53	SMD	22 x 20 x 0.7	1.152 thick, 6-layer
FF1704	42.5 x 42.5	1,704	1.00	0.60	0.53	SMD	26 x 22 x 0.7	1.152 thick, 6-layer
SF363	17 x 17	363	0.8	0.50	0.40	SMD	10 x 10 x 0.3	0.60 thick, 4-layer
CF1144	35 x 35	1,144	1.00	0.52	0.80	SMD	22 x 20 x 0.7	1.59 thick, 10-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.3622 mm size, HASL finish
- 0.5 mm pad diameter/0.65 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power/GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.1524 mm laser cut stencil, 0.50 mm aperture, alpha metals WS609 paste

Test Condition

- 0°C – 100°C, 10 minutes dwells, 5 minutes ramps, 2 cycles/hour

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- **OPEN**: Resistance of net > threshold resistance (300Ω)
- **FAIL**: At least 2 opens within one cycle, log 15 failures for each net

Table 3-64: **Summary of Test Results**

Package	Cycles Completed	# Tested	# Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FG676	7,027	30	30	4,686	6,012
FG680	4,000	30	0	NA	NA
FG900	7,027	28	28	4,405	5,344
FG1156	5,000	32	25	2,786	4,892
BF957	4,145	35	35	1,958	3,662
FF672	5,840	30	30	3,764	4,881
FF896	7,027	12	10	5,607	6,783
FF1152	4,158	30	30	2,668	3,822
FF1704	4,150	35	35	3,003	3,389

Table 3-64: **Summary of Test Results *(Cont'd)***

Package	Cycles Completed	# Tested	# Failed	First Failure (Cycle)	Characteristic Life (Cycle)
SF363 (Lot 1)	2,370	24	21	1,642	2,048
SF363 (Lot 2)	2,288	24	24	1,555	1,999
CF1144	5,000	21	0	NA	NA

Weibull Plots

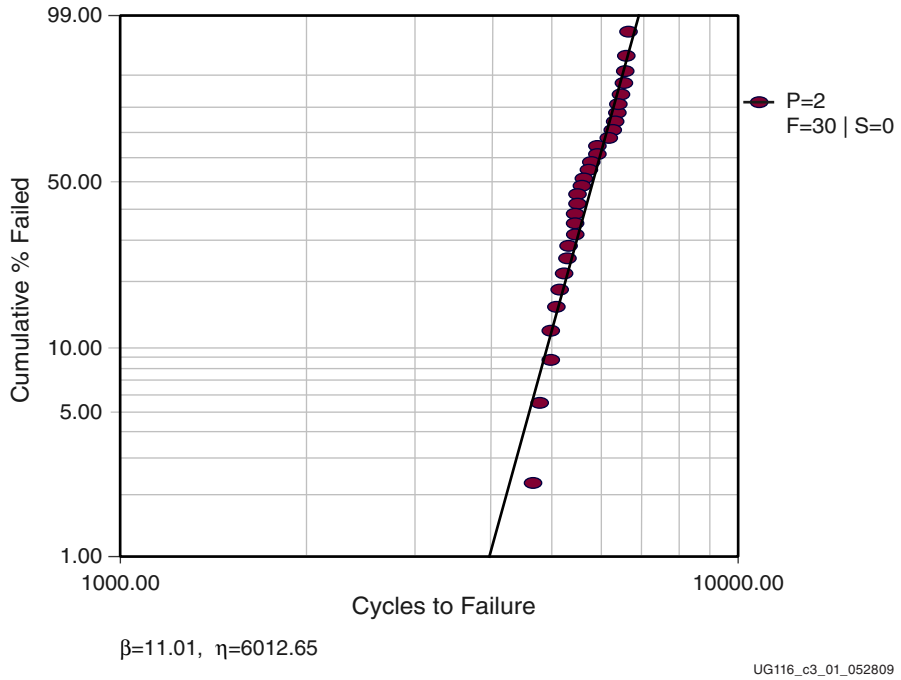

Figure 3-1: **Cycles to Failure in the Second-Level Reliability Tests for FG676**

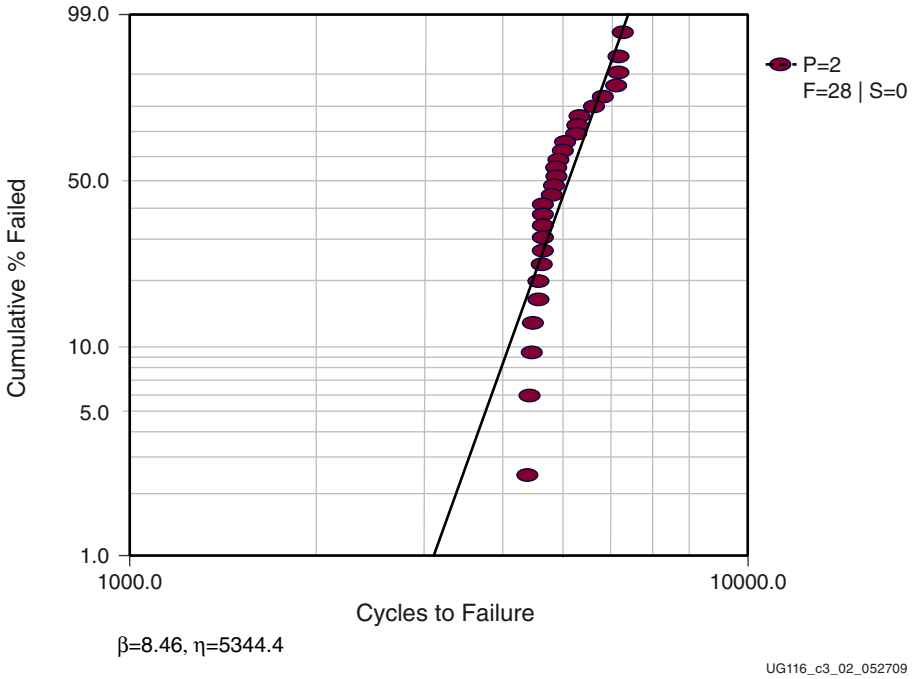

Figure 3-2: **Cycles to Failure in the Second-Level Reliability Tests for FG900**

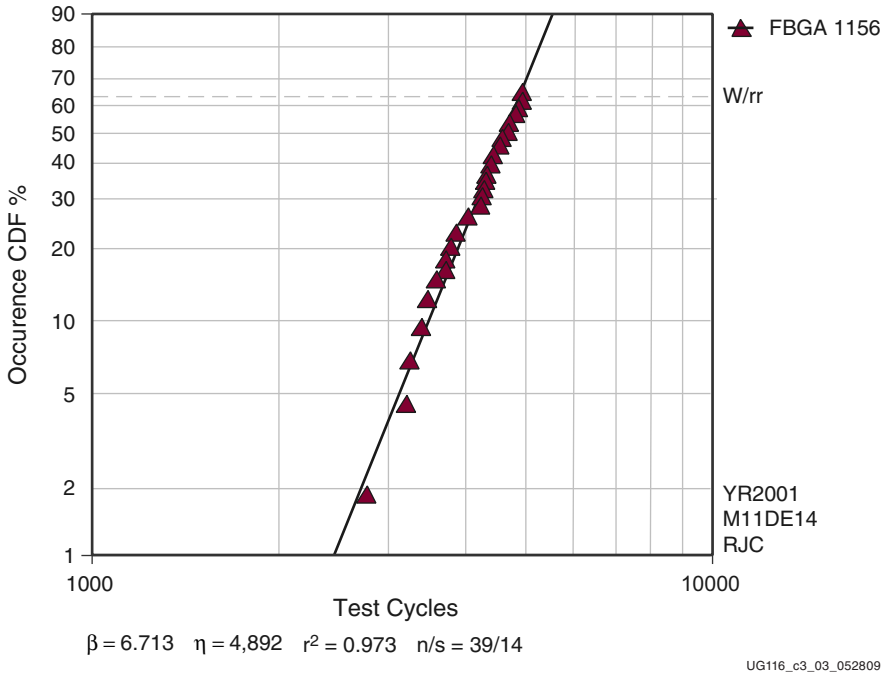

Figure 3-3: **Cycles to Failure in the Second-Level Reliability Tests for FG1156**

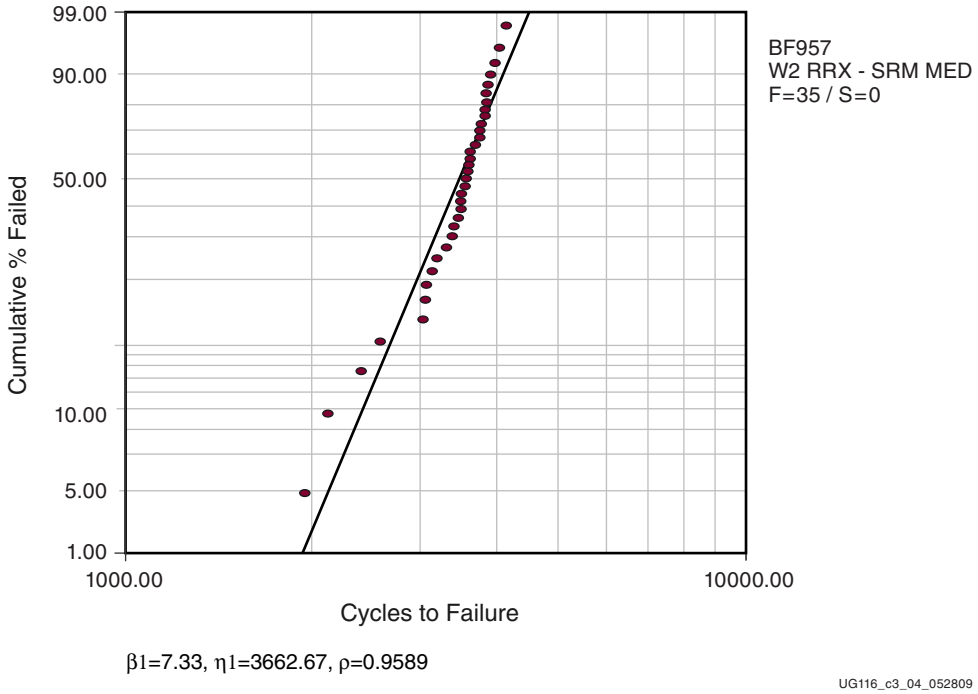

Figure 3-4: **Cycles to Failure in the Second-Level Reliability Tests for BF957**

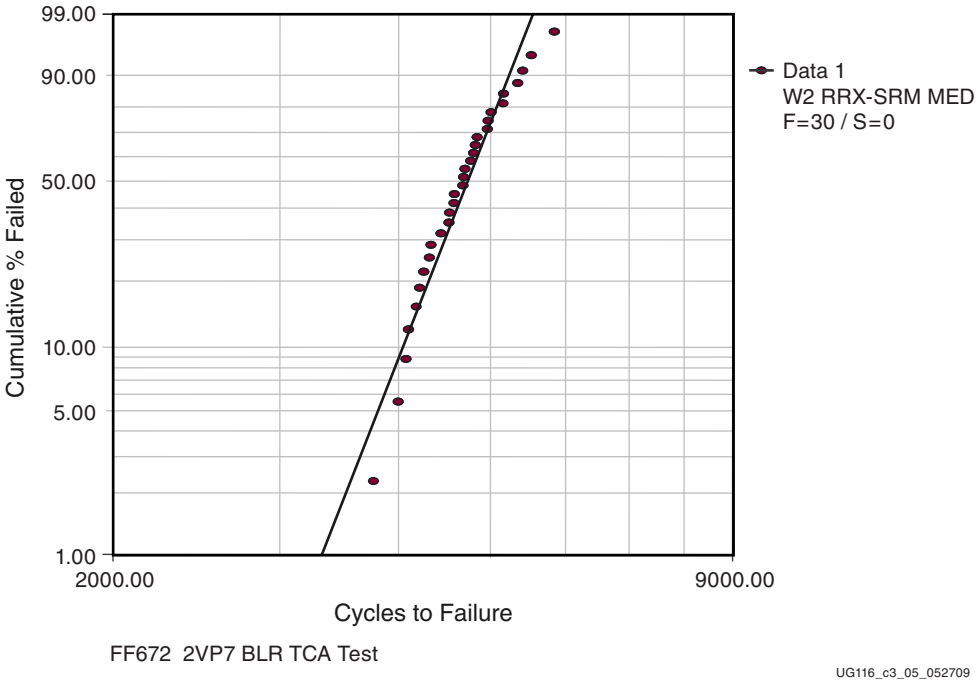

Figure 3-5: **Cycles to Failure in the Second-Level Reliability Tests for FF672**

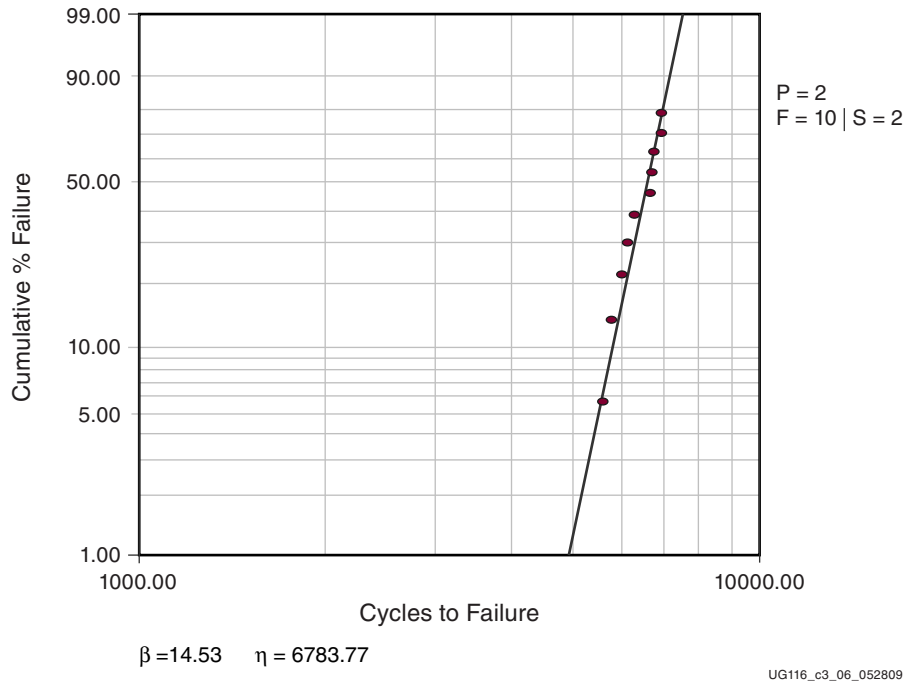

Figure 3-6: **Cycles to Failure in the Second-Level Reliability Tests for FF896**

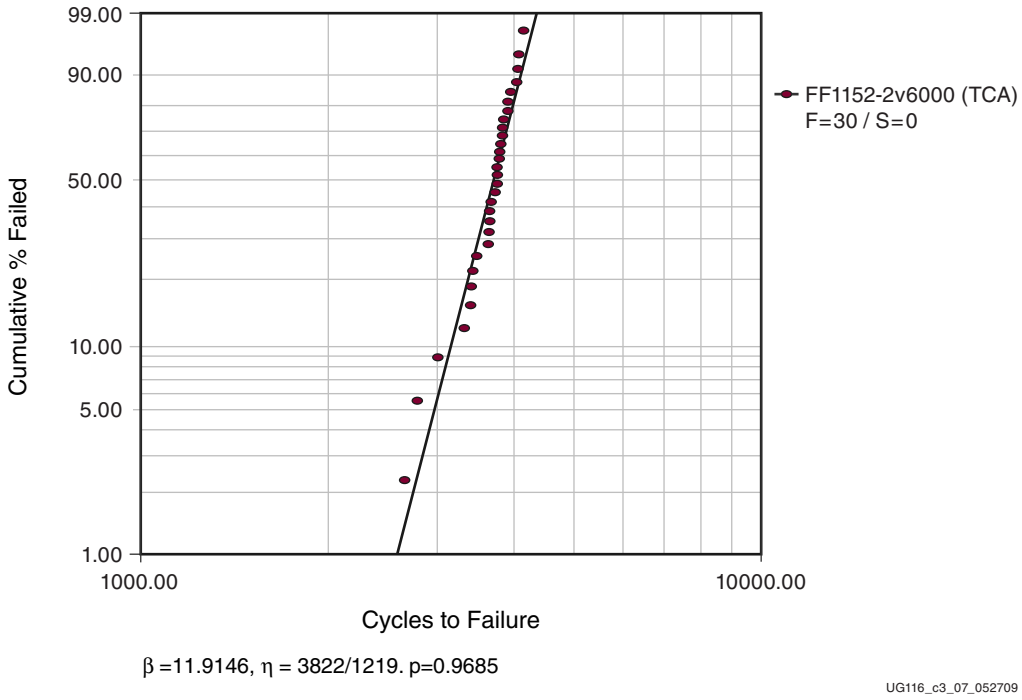

Figure 3-7: **Cycles to Failure in the Second-Level Reliability Tests for FF1152**

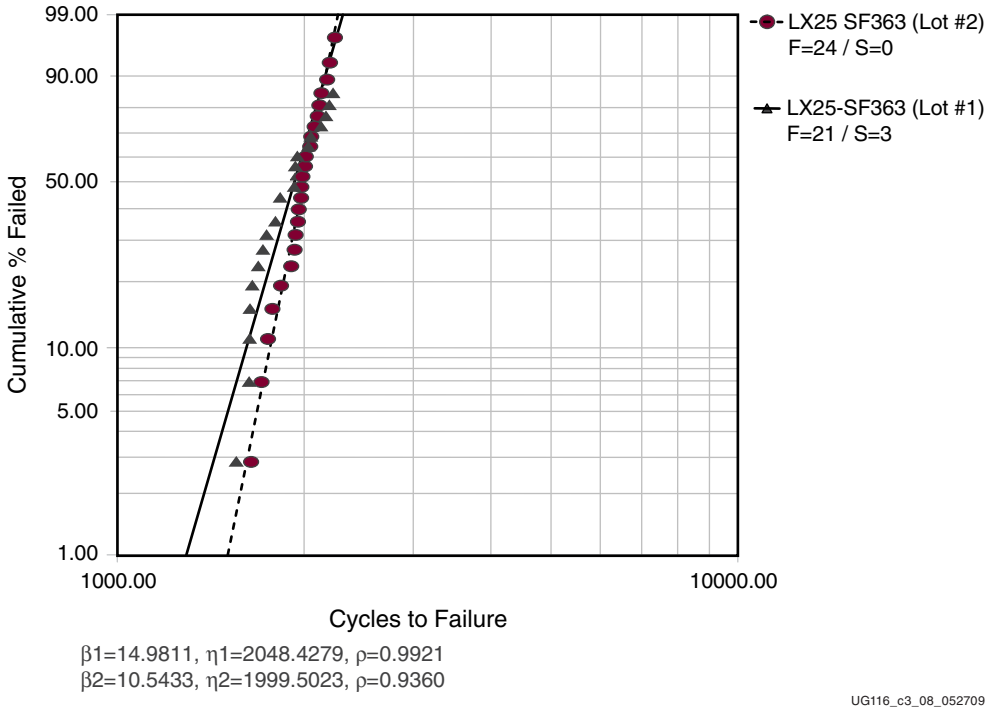

Figure 3-8: **Cycles to Failure in the Second-Level Reliability Tests for SF363**

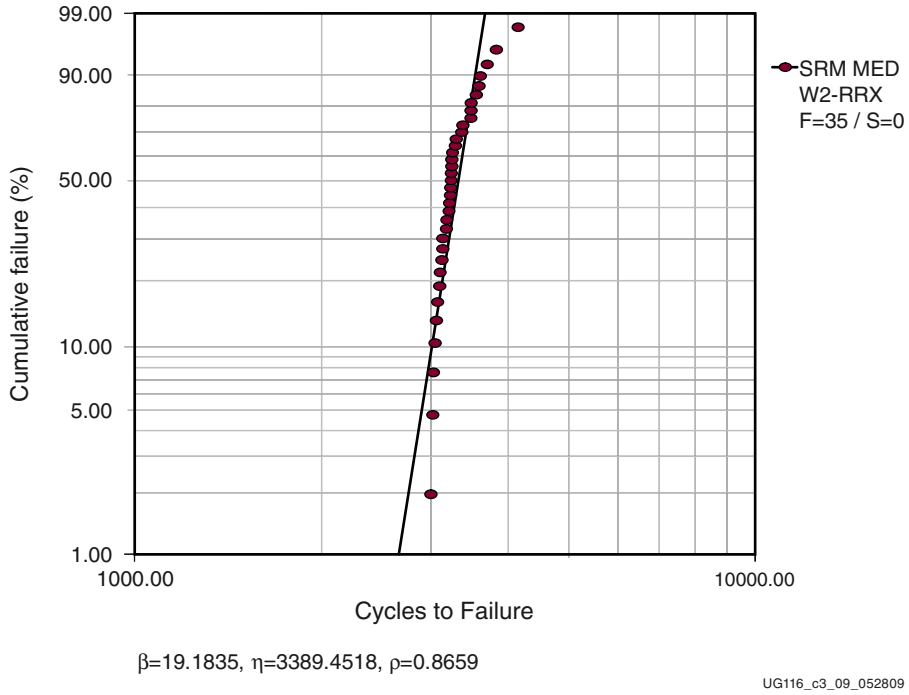

Figure 3-9: **Cycles to Failure in the Second-Level Reliability Tests for FF1704**

Board-Level Reliability Tests, Pb-Free

FGG676, FFG1152

Table 3-65: **Package Details (All Dimensions in mm)**

Package	Size	I/O	Pitch	Ball/Column Size	Pad Opening	Pad Type	Die Size	Substrate
FGG676	27 x 27	676	1.00	0.60	0.46	SMD	17.8 x 17.8 x 0.3	0.56 thick, 4-layer
FFG1704	42.5 x 42.5	1,704	1.00	0.60	0.53	SMD	23 x 23	1.152 thick 6-layer
FFG1152	35 x 35	1,152	1.00	0.60	0.53	SMD	22 x 20 x 0.7	1.152 thick, 6-layer

Mother Board Design and Assembly Details

- 8-layer, FR-4, 220 x 140 x 2.3622 mm size, OSP finish
- 0.5 mm pad diameter/0.65 mm solder mask opening (NSMD pads)
- Board layer structure: signal/GND/signal/power/signal/GND/signal/power
- Power, GND layer has 70% metal. Internal signal layer has 40% metal.
- 0.1524 mm laser cut stencil, 0.50 mm aperture, alpha metals WS609 paste

Test Condition

- FGG676: 0°C – 100°C, 40-minute thermal cycle, 10 minutes dwells, 10°C/minute ramp rate
- FFG1152: 0°C – 100°C, 10 minutes dwells, 5 minutes ramps, 2 cycles/hour

Failure Criteria

- Continuous scanning of daisy chain nets (every 2 minutes)
- **OPEN**: resistance of net > threshold resistance (300Ω)
- **FAIL**: At least 2 opens within one cycle, log 15 failures for each net

Table 3-66: **Summary of Test Results**

Package	Cycles Completed	# Tested	# Failed	First Failure (Cycle)	Characteristic Life (Cycle)
FGG676	7,027	35	27	4,390	5,974
FFG1704	5,000	32	0	NA	NA
FFG1152	4,640	28	26	3,186	4,121

Weibull Plots

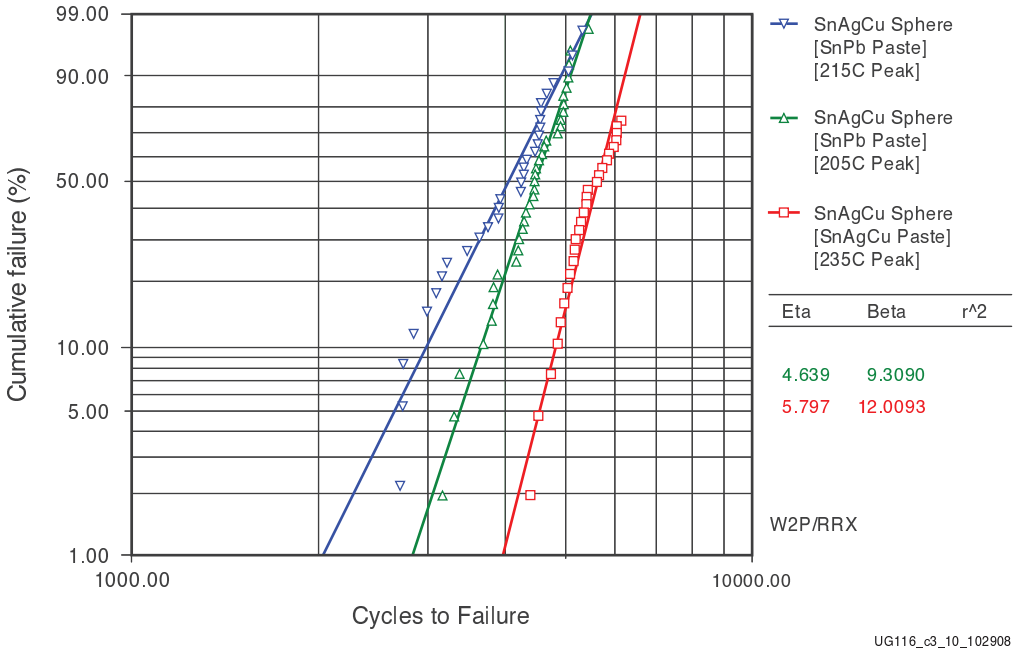

Figure 3-10: **Cycles to Failure in the Second-Level Reliability Tests for FGG676**

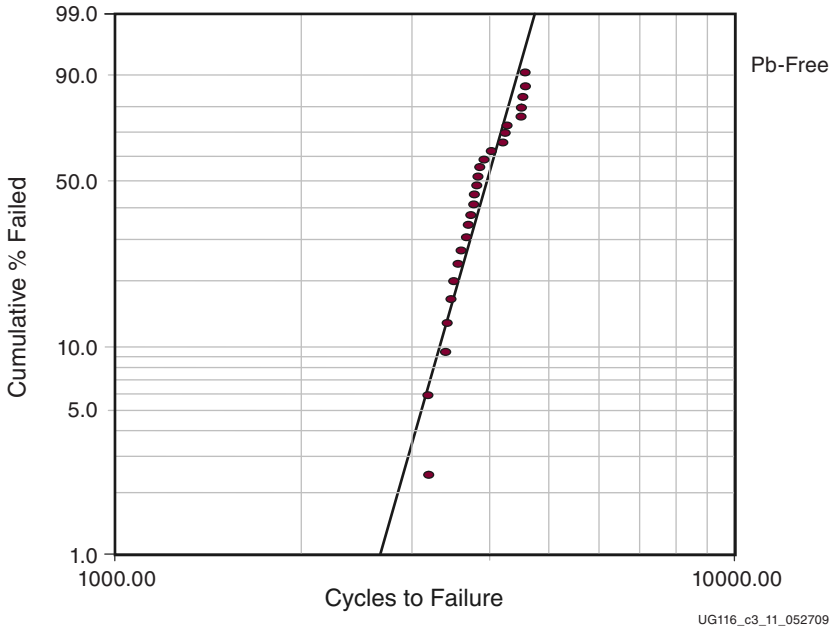

Figure 3-11: **Cycles to Failure in the Second-Level Reliability Tests for FFG1152**