ARM CoreSight
Debug Access Port (DAP) Lite

r1p2

Release Note

CoreSight DAP Lite r1p2 Release Notes

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Contents

1 PRODUCT DELIVERABLES

1.1 Product Release Status

This is a full release of the CoreSight Debug Access Port (DAP) Lite, revision r1p2.

These deliverables are being released under the terms of the agreement between ARM and each licensee (the "Agreement"). Use by recipient of the deliverables is subject to the terms and conditions of the Agreement.

1.2 About CoreSight DAP Lite

The DAP-Lite is a feature-reduced version of the CoreSight DAP supplied with the CoreSight Design Kit products. It does not contain a JTAG access port, or any others access ports to directly access the system bus. For more information on the additional features provided by the DAP, see the *CoreSight Design Kit Technical Reference Manual.*

The CoreSight DAP-Lite release bundles the following components:
- CoreSight Serial Wire & JTAG Debug Port (**DAPSWJDP**)
- CoreSight APB Access Port (**DAPAPBAP**)
- CoreSight APB Multiplexer (**DAPAPBMUX**)
- CoreSight ROM Table (**DAP ROM**)

Refer to Table 1 for the list of parts provided as part of this release.

1.3 About the CoreSight DAP Lite release note

Table1 lists the ARM part numbers for the individual deliverables that form part of the delivery for this ARM product. All the parts are provided under the TM940-BU-00000-r1p2-00rel0 bundle.

PART A – TECHNICAL REFERENCE MANUALS

Section 1 Technical Reference Manuals

Part number	Description	Revision	Format
TM940-DA-03001	CoreSight DAP Lite TRM –PDF	r1p2-00rel0	PDF
TM940-DA-00001	CoreSight DAP Lite TRM –FrameMaker	r1p2-00rel0	FrameMaker
TM940-DC-06002	CoreSight DAP-Lite Release Note (this document)	r1p2-00rel0	PDF

PART B – IMPLEMENTATION & INTEGRATION MANUALS

Part number	Description	Revision	Format
TM093-DC-70014	CoreSight Components Implementation Guide	r1p3-00rel0	PDF

PART C – ARM CORE SYNTHESIZABLE SOURCE

Section 1- CoreSight Debug

Part number	Description	Revision
TM940-MN-22100	CoreSight DAP Lite Verilog RTL	r1p1-01rel0
TM945-MN-22100	Serial Wire JTAG Dual Mode Debug Port Verilog RTL	r0p2-00rel0
TM918-MN-22100	APB Access Port Verilog RTL	r0p1-01rel0
TM919-MN-22100	APBMUX for DAP Lite Verilog RTL	r0p1-00rel0

Section 2 – Synthesis Scripts

Part number	Description	Revision
TM940-MN-01001	CoreSight DAP Lite Synthesis Scripts	r1p1-01rel0
TM940-DE-70002	CoreSight DAP Lite LEC Formality	r1p1-01rel0
TM940-DE-70003	CoreSight DAP Lite LEC Conformal	r1p1-01rel0

PART D – FUNCTIONAL TEST VECTORS

Part number	Description	Revision
TM940-VE-70000	CoreSight DAP Lite Functional CRF	r1p1-01rel0

Table 1: ARM part numbers for CoreSight DAP Lite

2 INSTALLATION

2.1 Introduction

Intellectual Property (IP) deliverables are collectively delivered as a single UNIX zipped tar file which has been security encrypted.

These installation instructions cover the following platform/operating system:

- UNIX

It is highly recommended that you use the GNU tar tool, version 1.13 or higher to avoid any confusion over the contents of your download.

The downloaded file has been TAR'ed and compressed using 'gzip'.

To recreate the files use:

```
gunzip FILENAME.tgz
```

Followed by:

```
gtar –xvf FILENAME.tar
```

2.1.1 What do you get?

Once the product extracted, under the directory **TM940-BU-00000-r1p2-00rel0** you will find the file **TM940-BU-00000-r1p2-00rel0.lst** This file describes the content of the bundle and for each part lists the files associated to the part.

Under **TM940-BU-00000-r1p2-00rel0/coresight** you will find

- **-** the CoreSight DAP Lite release note, **CoreSight_DAP_Lite_r1p2_Release_Note.pdf**
- README files
- the **docs** directory that contains all the CoreSight documentation associated with this product
- the **logical** directory under which the RTL for the DAP-Lite component is stored.
- the **implementation** directory under which the implementation scripts and replay vectors are localised.

Figure 1 shows the generic directory structure for a CoreSight component.
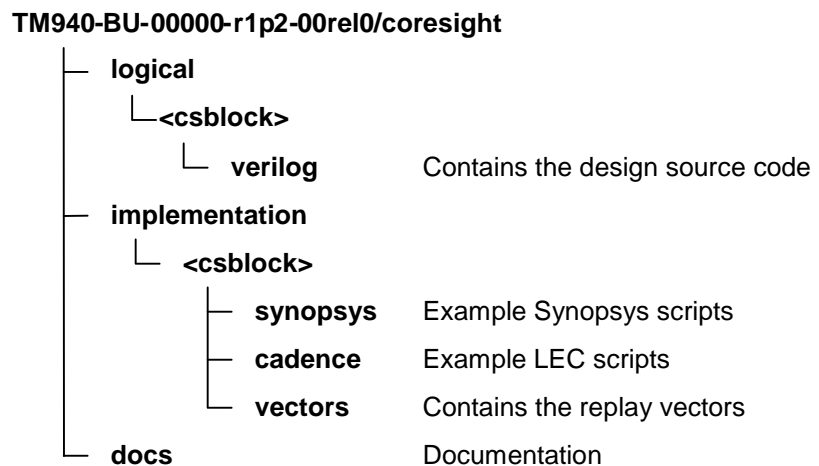
TM940-BU-00000-r1p2-00rel0/coresight

```
├── logical
│   └──<csblock>
│          └── verilog          Contains the design source code
├── implementation
│   └── <csblock>
│              ├── synopsys      Example Synopsys scripts
│              ├── cadence       Example LEC scripts
│              └── vectors       Contains the replay vectors
└── docs                        Documentation
```

Figure 1: CoreSight Development Environment Directory Structure

Under logical and implementation you will find a dedicated directory for each of the CoreSight components, refer to the **CoreSight DAP Lite Technical Reference Manual** delivered with this product for details of the components.

2.1.2 Installation of the reference cell library

The development and test of the CoreSight components has been done using the Standard Cell, Artisan Sage-HS, TSMC 0.13μm G (FSG) Version 2003q1v1 libraries (not provided). The logs provided with this release have been generated when targeting this library.

3 DOCUMENTATION

3.1 Documents Supplied

The following documents are supplied as part of the CoreSight DAP Lite release.
The document files are located in the **docs** directory, see Figure 1

CoreSight DAP-Lite r1p2 Technical Reference Manual ARM DDI 0316D

The technical reference manual provides details for programming and interfacing to the CoreSight DAP Lite component.

CoreSight Components Implementation Guide ARM DDI 0143 E

The Implementation Guide provides details for using the implementation scripts provided as part of the deliverables; the implementation flow of a typical CoreSight Sub System is also discussed.

3.2 README Files

In some of the directories you will find README files. ARM recommends users to read all the README files provided in this release.

4 RTL CONFIGURATION PARAMETERS ('DEFINE)

As specified contractually, the RTL deliverables contains "Verilog Defines" that are expected to be amended by partners, refer to the CoreSight Components Implementation Guide for details on these parameters.

For the DAP Lite product only the ROM table parameters are relevant.

5 TRIAL TESTING

5.1 Product Maturity

This product release is a full release. All known errata have been fixed, information about errata in previous releases is available in the DAP-Lite errata document, part number : TM940-DC-11001-r1p2-00rel0.

5.2 Technical data summary

The following is a summary of the key technical points from testing of the DAP Lite component.

Cell library	Standard Cell, Artisan Sage-HS, TSMC 0.13µm G (FSG) Version 2003q1v1
Debug Access Port (DAP) Lite	**Verilog RTL**
Total cell area, scan inserted, sq um	DAP Lite : 48934 sq.um
Total cell area, scan inserted, NAND-2 equivalents	DAP : 7.8 K gates
Clock frequency used	PCLKDBG : 200 MHz; PCLKSYS : 200 MHz; SWCLKTCK: 100 MHz

Table 2: CoreSight DAP Lite Technical Data Summary

Tools used to develop the CoreSight DAP-Lite EAC release	
Simulators	Synopsys VCS 2006.06-7 (RH_Linux86, SunOS5) ModelTech ModelSim 6.0c (RH_Linux86, SunOS5) Cadence Incisive 5.5 (RH_Linux86, SunOS5)
Code Coverage Metrics	Synopsys VCS 2006.06-7
Synthesis and scan test tools and version	Synopsys Design Compiler 2006.06-SP5 (RH_Linux86) Synopsys Physical Compiler 2006.06-SP5 (RH_Linux86) Design Ware Foundation Library 2006.06-SP5 (RH_Linux86) Synopsys DFT Compiler 2006.06-SP5 (RH_Linux86) Synopsys TetraMAX 2006.06-SP5 (RH_Linux86) Synopsys JupiterXT 2006.06-SP5 (RH_Linux86)
Equivalence Checking	Synopsys Formality 2006.06 (RH_Linux86) Cadence Conformal LEC 6.2 (RH_Linux86)
Command Line Tools	Perl 5.8

Table 3: CoreSight DAP Lite Technical data summary and Tools used

Notes: The performance provided in this table for the CoreSight DAP Lite component have been obtained using Synopsys Design Compiler and a NAND2 (drive of 1) as reference cell. For reference a NAND-2 gate area for Sage-HS is 6.24 sq um.

5.3 Validation

- SWJ-DP, APB-MUX and APB-AP have been extensively validated within their own block level testbenches, this validation environment is not delivered with this release.
- DAP Lite has been validated together with the SWJ-DP, APB-MUX and APB-AP sub-components, a subset of these tests are supplied as vectors with this release.

6 DIFFERENCES FROM PREVIOUS REVISIONS

- Improvements in Clock Domain Crossing (CDC) tools have highlighted issues where asynchronous clocks are used in the design, these issues have been resolved with this release. Some issues have been classified as errata, details of these can be found in the DAP-Lite errata document, part number : TM940-DC-11001-r1p2-00rel0.

  Note that the RTL has only changed in the following two components:

  | TM945-MN-22100 | Serial Wire JTAG Dual Mode Debug Port Verilog RTL | r0p2-00rel0 |
  | TM919-MN-22100 | APBMUX for DAP Lite Verilog RTL | r0p1-00rel0 |

  The other components, including the DAP Lite RTL and the Synthesis and LEC scripts, have **NOT** changed since the last release. However, as the logs delivered with the DAP Lite scripts have been updated to reflect changes in the sub-components all DAP Lite deliverables have had a minor revision update (see Table 1).

- The CoreSight DAP-Lite Reference Manual (DDI 0316D) has been updated to reflect the release revision.

7 LIMITATIONS OF THIS RELEASE

- The DAP Lite release is supplied with the CoreSight Implementation Guide, this document is a generic document that is supplied with other CoreSight releases. Therefore it describes RAM integration and an example CoreSight sub-system (CSSYS), which are not applicable to this release.

8 KNOWN ISSUES

None

9 REVISION HISTORY

Date	Revision - Version	Description
05/08/05	r0p0-00bet0	Beta Release r0p0
17/01/06	r0p0-00rel0	Early Access Release
20/12/06	r1p0-00rel0	Maintenance Release, see section 6 for changes.
19/10/07	r1p1-00rel0	Maintenance Release, see section 6 for changes.
9/5/08	r1p2-00rel0	CDC Maintenance Release, see section 6 for changes.