ECE 385: Digital Systems Laboratory

Fall 2022

Experiment #1

Introductory Experiment

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1 Introduction

In this lab, the phenomenon of Static Hazards is studied with the example of an 2 to 1 MUX. To begin with, a naïve version of the 2 to 1 MUX is implemented using only the 7400 NAND gate chips. This implementation possess the weakness of potential static-1 hazard ("glitch"). Then the circuit is re-designed to include redundancy in K-map terms to avoid a state transfer between adjacent minterms, which eliminates the possibility of any glitch.

2 Circuit Operation Description

In both parts of the prelab, the target of the circuits is to implement a 2 to 1 MUX with two inputs (A, C), one output (Z) and select (B) with NAND gates. The basic functionality is that when the select B is at a logical high ("1"), the output Z should be directly outputting the value of A; and when B is at a logical low ("0"), the output Z should be outputting that of C.

The K-map can be drawn as in Figure 1

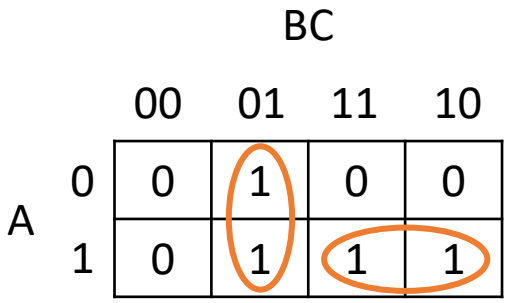

Figure 1: The K-map for the output Z in the part A circuit. The two orange circles, which are adjacent to each other, represent the chosen minterm implementations. The adjacency implies a potential static hazard.

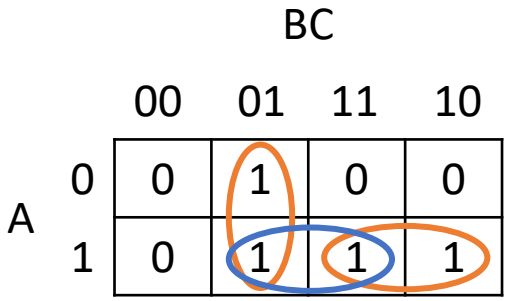

Figure 2: The K-map for the the output Z in the part B circuit. In addition to the two orange circles, one redundant blue circle is added to cover the state transfer between two adjacent minterms. This modification eliminates the static hazard.

3 Component Layout Sheet

4 Circuit Diagrams

5 Lab Documentations

5.1 Pre-lab Part A Truth Table

5.2 Pre-lab Question Answers

5.3 Pre-lab Part B Truth Table

5.4 Oscilloscope Printout

6 Post-lab question answers

7 General Guide question answers

8 Conclusion