Rev. 1.1, Sep. 2017

K9AFGD8H0A

256Gb A-die Toggle NAND Flash

Multi-Level-Cell (3bit/Cell)

datasheet *WF biz Only*

SAMSUNG

Revision History

Revision No.	History	Draft Date	Remark	Edited by	Reviewed by
1.0	1. Initial issue	May. 19, 2017	Target	H.K.Kim	I.S.Han
1.1	1. tR is changed from 45ms to 65us. 2. tBERS is changed from 1.2ms to 5ms. 3. tPROG is changed from 0.7ms to 0.2ms. 4. Chapter 2.7 DC Operating Characteristics revised. 5. Chapter 2.11 Input/Output Capacitance revised. 6. Figures 55. Set Offset Value for Read Retry (Edge MLC) revised.	Sep. 26, 2017	Target	H.K.Kim	S.J.Kim

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1.0 INTRODUCTION

1.1 Features

• Voltage Supply
- V_{CC} : 3.3V (2.7V ~ 3.6V)
- $V_{CC}Q$: 1.8V(1.7~1.95V)

• Organization
- Page Size : (16K + 2K) x 8bit
- Data Register : (16K + 2K) x 8bit
- Block Size : (12M + 1536K) bytes
- Unit Device capacity : (12M + 1536K) x 2852

• Products
- K9AFGD8H0A : Unit device x 1

• Automatic Program and Erase
- Page Program : (16K + 2K)Byte
- Block Erase : (12M + 1536K)Byte

• Page Read Operation
- Random Read : 4/8/16KB = 65μs (Typ.)
- Data Transfer Rate : up to 533Mbps or 266Mhz ($V_{CC}Q$: 1.8V)

• Write Cycle Time
- Page Program Time : 1.2 ms (Typ.)
- Block Erase Time : 5ms (Typ.)

• Command/Address/Data Multiplexed DQ Port

• Toggle Mode DDR Data Interface

• Hardware Data Protection
- Program/Erase Lockout During Power Transitions

• Reliable CMOS charge trap flash Technology
- ECC Requirement : 240bit / 2KB

• Command Driven Operation

• Scalable DQ Driver

• Randomizer function is required by controller

1.2 Product List

Part Number	Density	Interface	Organization	V_{CC} Range	$V_{CC}Q$ Range	PKG Type
K9AFGD8H0A	256Gb	Toggle mode	x8	2.7V~ 3.6V	1.7~1.95V	Wafer

1.3 General Description

Toggle DDR is a NAND interface for high performance applications which support data read and write operations using bidirectional DQS.

Toggle DDR NAND has implemented 'Double Data Rate' without a clock. It is compatible with functions and command which have been supported in conventional type NAND(i.e. SDR NAND) while providing high data transfer rate based on the high-speed Toggle DDR Interface and saving power with separated DQ voltage. For applications that require high capacity and high performance NAND, Toggle DDR NAND is the most appropriate.

Toggle DDR2.0 NAND supports the interface speed of up to 266 Mhz(533Mbps), which is 2 times faster than the data transfer rate offered by Toggle DDR 2.0 NAND (533Mbps). Toggle DDR NAND transfers data at high speed by using DQS signal that behaves as a clock, and DQS shall be used only when data is transferred for optimal power consumption.

1.4 Toggle DDR Interface according to Data Transfer Rate

Feature		~ 200Mbps	~ 400Mbps	~ 533Mbps
$V_{CC}Q$		1.8V	1.8V	1.8V
I/O Type	CMOS (Single-ended without $V_{REF}Q$)	Support	Not support	Not support
	Single-ended with $V_{REF}Q$[1)]	Support	Support	Support
	Differential signaling for DQS and $\overline{RE}$ (optional)[2)]	Support	Support	Support
ZQ calibration[3)]		Support	Support	Support

NOTE :
1) To use high speed over 200Mbps, $V_{REF}Q$ shall be supplied before High-speed setting.The device can be used on under 200Mbps without $V_{REF}Q$.
2) Differential signal may be required depending on vendors
3) ZQ calibration is highly recommended when the device runs on over 400Mbps.

1.5 Definitions and Abbreviations

DDR
Acronym for double data rate.

Address
The address is comprised of a column address with 2 cycles and a row address with 3 cycles. The row address identifies the page, block and LUN to be accessed. The column address identifies the byte within a page to access. The least significant bit of the column address shall always be zero.

Column
The byte location within the page register.

Row
Refer to the block and page to be accessed.

Page
The smallest addressable unit for the Read and the Program operations.

Block
Consists of multiple pages and is the smallest addressable unit for the Erase operation.

Page register
Register used to transfer data to and from the Flash Array.

Defect area
The defect area is where factory defects are marked by the manufacturer. Refer to the section 3.2.

Device
The packaged NAND unit. A device may contain more than a target.

LUN (Logical Unit Number)
The minimum unit that can independently execute commands and report status. There are one or more LUNs per $\overline{CE}$.

Target
An independent NAND Flash component with its own $\overline{CE}$ signal.

SR[x] (Read Status)
SR refers to the status register contained within a particular LUN. SR[x] refers to bit x in the status register for the associated LUN.
Refer to Chapter 5.2.13 for the definition of bit meanings within the status register.

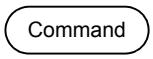
$V_{REF}Q$
input reference voltage.

V_{TT}
Termination voltage for output AC timing and DC level measurement.

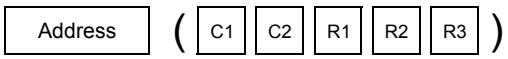
1.6 Diagram Legend

Diagrams in the Toggle DDR2.0 datasheet use the following legend:

This legend shows the command data. Refer to the Table 30 for more information about the command data.

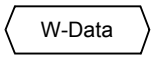


This legend shows the Address data. The address are comprised of 2 cycles column address and 3 cycles row address.

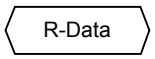


C1 : Column address 1
C2 : Column address 2
R1 : Row address 1
R2 : Row address 2
R3 : Row address 3

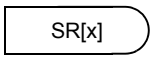
This legend shows Host writing data(data input) to the device.



This legend shows Host reading data(data output) from the device.



This legend shows Host reading the status register within a particular LUN.



2.0 PHYSICAL INTERFACE

2.1 Pin Description

Pin Name	Pin Function
DQ[7:0]	**DATA INPUTS/OUTPUTS** The DQ pins are used to input command, address and data, and to output data during read operations. The DQ pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the DQ ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{RE}$, (RE) or RE_t, (RE_c)	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active, drives the data onto the DQ bus. Data is valid after t_{DQSRE} of rising edge & falling edge of $\overline{RE}$, which also increments the internal column address counter by each one. The Read Enable $\overline{RE}$ is paired with differential signal RE to provide differential pair signaling to the system during reads.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the DQ port. Commands, addresses are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled. R/$\overline{B}$ shall be tied to $V_{CC}Q$.
DQS, ($\overline{DQS}$) or DQS_t, (DQS_c)	**DATA STROBE** Data output is aligned with DQS falling/rising edge, and data inputs at DQS falling/rising. The data strobe DQS is paired with differential signal $\overline{DQS}$ to provide differential pair signaling to the system during reads and writes.
V_{CC}	**POWER** V_{CC} is the power supply for device.
$V_{CC}Q$	**DQ POWER** The $V_{CC}Q$ is the power supply for input and/or output signals.
V_{SS}	**GROUND**
$V_{REF}Q$	**REFERENCE VOLTAGE**
RZQ_x	**REFERENCE PIN FOR ZQ CALIBRATION** This is used on ZQ calibration and RZQ ball shall be connected to V_{SS} through 300ohm resistor.
V_{PP}	**EXTERNAL HIGH VOLTAGE**
N/U	**Not Usable** A pin that is not to be used in normal applications and that may or may not have an internal connection.
N/C	**NO CONNECTION** A pin that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of wiring) does not exceed the highest supply voltage rating of the circuit.
RFU	**RESERVED FOR USE** Nothing should be connected with it.

NOTE :
Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
Do not leave V_{CC} or V_{SS} disconnected.

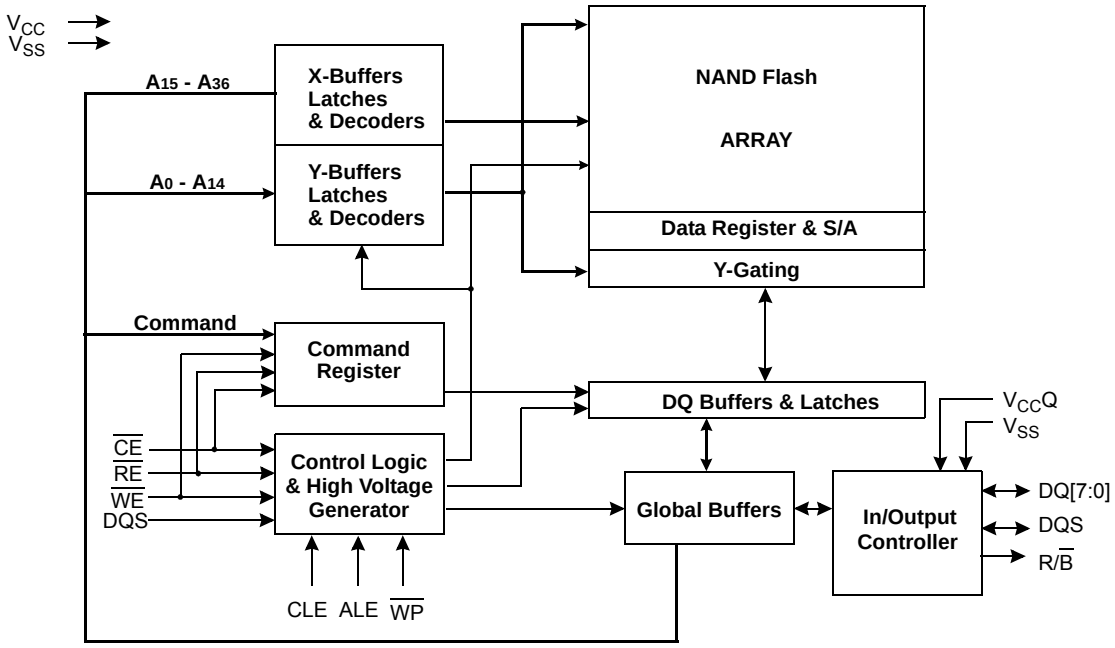


Figure 1. Functional Block Diagram

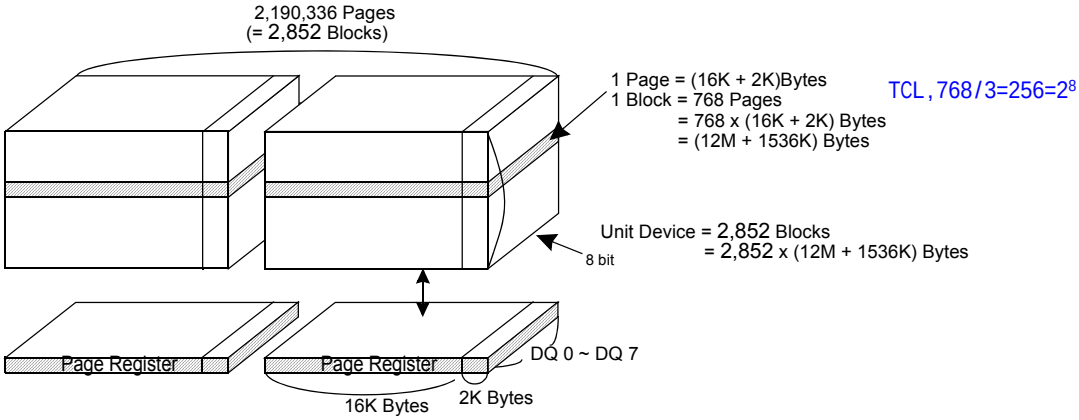


Figure 2. Array Organization of Unit Device

[Table 1] Address Mapping Table

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7	
1st Cycle	A0(1)	A1	A2	A3	A4	A5	A6	A7	**Column Address**
2nd Cycle	A8	A9	A10	A11	A12	A13	A14	*L	
3rd Cycle	A15	A16	A17	A18	A19	A20	A21	A22	**Row Address;**
4th Cycle	A23	A24	A25	A26	A27	A28	A29	A30	**Page Address : A15 - A24**
5th Cycle	A31	A32	A33	A34	A35	A36	**A37	*L	**Plane address : A25** **Block Address : A26 - A36**

NOTE :

1) A0 must be set to "Low"
2) Data input/output unit should be 2-byte(16bit).
Column Address : Starting Address of the Register.
* When unused address bits shall be set to "Low".
* The device ignores any additional input of address cycles than required.
** A37 is used for DDP with a single CE.
** A37 must be set to "Low" for SDP.

2.2 Valid Block

[Table 2] The Number of Valid Block per a $\overline{CE}$

Parameter	Symbol	Min	Typ.	Max	Unit
K9AFGD8H0A	N_{VB}	2762	-	2852	Blocks

NOTE :
1) The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2) The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

2.3 Absolute Maximum DC Rating

Stresses greater than those listing in Table 3 may cause permanent damage to the device. This is a stress rating only. Operation beyond the operating conditions specified in Table 3 is not recommended. Extended exposure beyond these conditions may affect device reliability.

[Table 3] Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to +4.6	V
	$V_{CC}Q$	-0.3 to +2.4	
	V_{IN}	-0.3 to $V_{CC}Q$ + 0.3(<2.4)	
	$V_{I/O}$		
	V_{PP}	-0.6 to +16	
Storage Temperature	T_{STG}	-65 to +100	°C

NOTE :
Maximum DC voltage on input and I/O pins is $V_{CC}Q$+0.3V which, during transition, may have overshoot that is defined in Table 7.

2.4 Operating Temperature Condition

[Table 4] Operating Temperature Condition

Symbol	Parameter	Rating	Unit
T_{OPER}	Operating Temperature Range for Commercial	0 to +70	°C

NOTE :
1) Operating Temperature(T_{OPER}) is the case surface temperature on the center/top side of the NAND.
2) The Normal Temperature Range specifies the temperatures where all NAND specifications will be supported. During operation, the NAND case temperature must be maintained between 0-70°C for commercial under all operating conditions.

2.5 Recommended Operating Conditions

[Table 5] Recommended Operating Condition

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Ground Voltage	V_{SS}	0	0	0	V
Supply Voltage for 1.8V I/O signaling	$V_{CC}Q$	1.7	1.8	1.95	V
External high Voltage	V_{PP}	11	12	13	V

NOTE :
1) V_{CC} and $V_{CC}Q$ may be distinct and unique voltages. The device shall support one of the following V_{CC}/ $V_{CC}Q$ combinations,
V_{CC} = 3.3V, $V_{CC}Q$ = 1.8V
All parameters, timing modes and other characteristics are related to the supported voltage combination.
2) From External V_{PP} source, up to 3mA can be consumed by each NAND device when more than 20nF power capacitor is supported.

2.6 AC Overshoot/Undershoot Requirements

The device may have AC overshoot or undershoot from $V_{CC}Q$ and V_{SS} levels. Table 7 defines the maximum values that the AC overshoot or undershoot may attain.

[Table 6] AC Overshoot/Undershoot Specification (1.8V)

Parameter	Maximum Value		Unit
	~200Mhz	~266Mhz	
Max. peak amplitude allowed for overshoot area	1		V
Max. peak amplitude allowed for undershoot area	1		V
Max. overshoot area above $V_{CC}Q$	0.75	0.56	V*ns
Max. undershoot area above $V_{SS}Q$	0.75	0.56	V*ns

NOTE :
1) This specification is intended for devices with no clamp protection and is guaranteed by design.

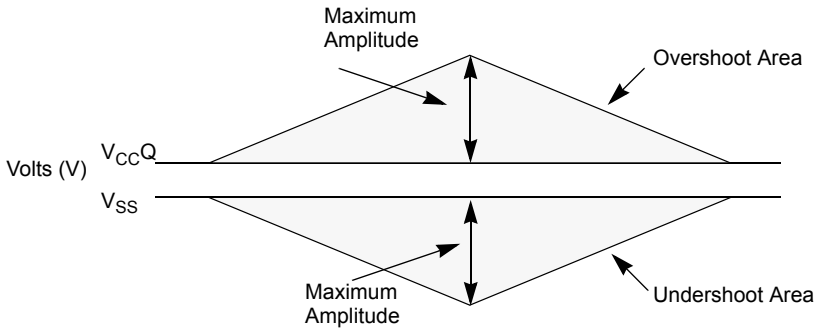


Figure 3. Overshoot/Undershoot Diagram

2.7 DC Operating Characteristics

[Table 7] DC & Operating Characteristics for $V_{CC}Q$=1.8V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Operation Current	$I_{CC}1$	-	-	-	50	mA
Page Program Operation Current	$I_{CC}2$	-	-	-		
Erase Operation Current	$I_{CC}3$	-	-	-		
DQ Burst Read Current	$I_{CC}4R$	$\overline{CE}$=V_{IL}, Half data switching C_{LOAD}=0pF (I_{OUT}=0mA) $\overline{CE}$=V_{IL}, Half data switching tRC=3.75ns(266Mhz)	-	-	75	
	$I_{CC}Q4R$		-	-	90	
DQ Burst Write Current	$I_{CC}4W$	$\overline{CE}$=V_{IL}, Half data switching tDSC=3.75ns(266Mhz)	-	-	75	
	$I_{CC}Q4W$		-	-	12	
Bus Idle Current	$I_{CC}5$	DQ[7:0]=00h/FFh	-	-	20	
Stand-by Current(CMOS)	I_{SB}	$\overline{CE}$=$V_{CC}Q$-0.2, $\overline{WP}$=0V/$V_{CC}Q$	-	-	50	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to VccQ(max)	-	-	±10	
Output Leakage Current	I_{LO}	V_{UOT}=0 to VccQ(max)	-	-	±10	
Output High Voltage Level	V_{OH}	I_{OH}=-100µA	$V_{CC}Q$-0.1	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL}= 100µA	-	-	0.1	
Output Low Current(R/$\overline{B}$)	I_{OL}(R/$\overline{B}$)	V_{OL}=0.2V	3	4	-	mA

NOTE :

1) Typical value is measured at V_{CC}=3.3V, T_A=25°C. Not 100% tested.
VOH and VOL should be available on these two conditions; Output Strength is nominal and $V_{CC}Q$=1.8V, Rpd/Rpu are all $V_{CC}Q$x0.5. If the driver strength settings are supported.

2) Table 14 shall be used to derive the output driver impedance values.

3) The value of I_{CC} max @ Cache Read is $I_{CC}1$+ $I_{CC}4$.

2.8 AC & DC Input Measurement Levels

[Table 8] Single Ended without $V_{REF}Q$ AC & DC input level

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}(DC)$	0.7 x $V_{CC}Q$	$V_{CC}Q$ + 0.3	V
DC input logic low	$V_{IL}(DC)$	- 0.3	0.3 x $V_{CC}Q$	
AC input logic high	$V_{IH}(AC)$	0.8 x $V_{CC}Q$	-	
AC input logic low	$V_{IL}(AC)$	-	0.2 x $V_{CC}Q$	

NOTE :
1) V_{IL} can undershoot to -0.3V and VIH can overshoot to $V_{CC}Q$ +0.3V for durations of 20ns or less.
2) $V_{REF}Q$ shall be used at high interface speed above 200Mbps.

[Table 9] Single Ended with $V_{REF}Q$ AC & DC input level

Parameter	Symbol	Min	Max	Unit
DC input logic high	$V_{IH}(DC)$	$V_{REF}Q$ + 0.15	$V_{CC}Q$ + 0.3	V
DC input logic low	$V_{IL}(DC)$	- 0.3	$V_{REF}Q$ - 0.15	
AC input logic high	$V_{IH}(AC)$	$V_{REF}Q$ + 0.3	-	
AC input logic low	$V_{IL(AC)}$	-	$V_{REF}Q$ - 0.3	
Reference Voltage	$V_{REF}Q_{(DC)}$	0.49 x $V_{CC}Q$	0.51 x $V_{CC}Q$	

NOTE :
$V_{REF}Q$ is used only for 1.8$V_{CC}Q$.

2.9 $V_{REF}Q$ Tolerances

The DC-tolerance and AC-noise limits for the reference voltages. Figure 4 shows a valid reference voltage $V_{REF}Q(t)$ as a function of time.
$V_{REF}Q(DC)$ is the linear average of $V_{REF}Q(t)$ over a very long period of time (e.g. 1sec). This average has to meet the min/max requirements in Table 9.
$V_{REF}Q(t)$ may temporarily deviate from $V_{REF}Q(DC)$ by no more than +/- 1% $V_{CC}Q$.
The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on $V_{REF}Q$.
"$V_{REF}Q$" shall be understood as $V_{REF}Q(DC)$, as defined in Figure 4.

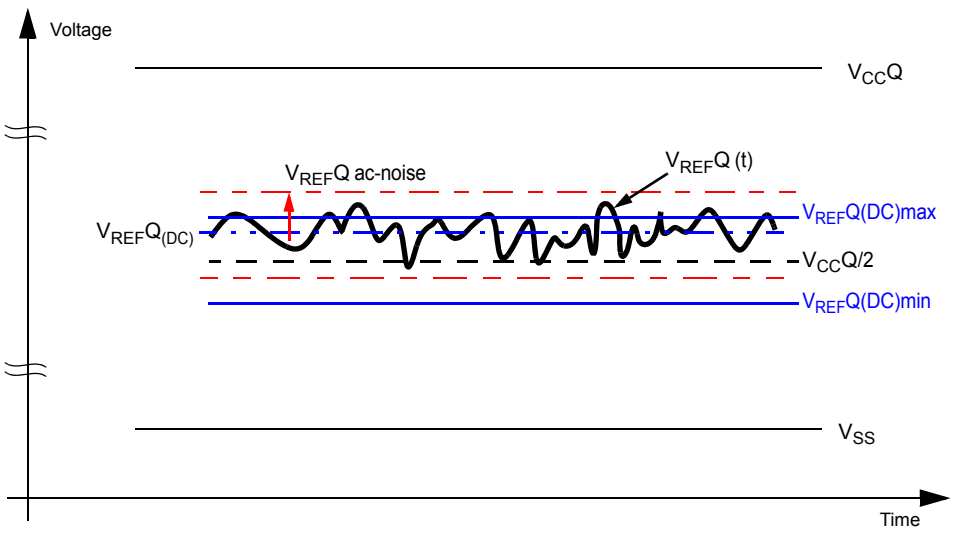


Figure 4. $V_{REF}Q(DC)$ Tolerance and $V_{REF}Q$ AC-Noise Limits

2.10 Differential Input/Output AC Characteristics

[Table 10] Differential AC/DC Input Logic Level

Parameter	Symbol	Min	Max	Units
AC differential input voltage[1)]	V_{ID}(AC)	0.6	$V_{CC}Q$ + 0.6	V
DC differential input voltage	V_{ID}(DC)	0.3	$V_{CC}Q$ + 0.3	V
AC differential cross point voltage[2)]	V_{IX}(AC)	0.5 * $V_{CC}Q$ - 0.175	0.5 * $V_{CC}Q$ + 0.175	V

NOTE :

1) V_{ID}(AC) specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the "true" input signal and V_{CP} is the "complementary" input signal. The minimum value is equal to V_{IH}(AC) - V_{IL}(AC).

2) The typical value of V_{IX}(AC) is expected to be about 0.5 * $V_{CC}Q$ of the transmitting device and V_{IX}(AC) is expected to track variations in $V_{CC}Q$. V_{IX}(AC) indicates the voltage at which differential input signals must cross.

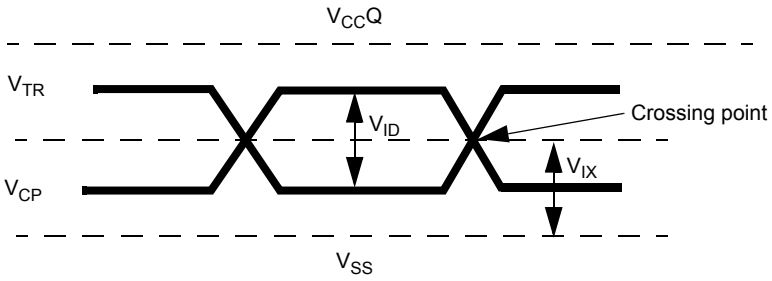


Figure 5. Differential Signal Levels

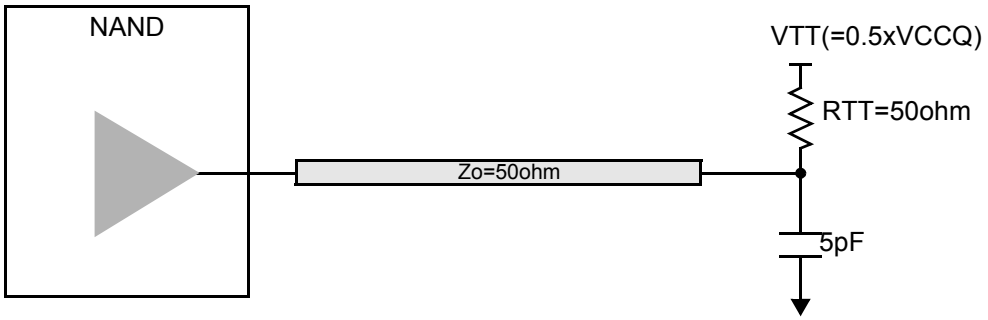


Figure 6. Measurement condition

2.11 Input/Output Capacitance (T_A=25°C, $V_{CC}Q$=1.8V, f=100Mhz)

[Table 11] Input/Output Capacitance

Item	Symbol	Test Condition	K9AFGD8H0A		Unit
			Wafer		
			Min	Max	
Input/Output Capacitance	C_{DQ}	V_{IL}=0V	-	2	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	1.5	pF

NOTE :

1) Capacitance is periodically sampled and not 100% tested.

2.12 DQ Driver Strength

The device may be configured with multiple driver strengths with 'SET FEATURE' command.
The Toggle DDR supports all two driver strength settings. Devices that support driver strength settings shall comply with the output driver requirements in this section. A device is only required to meet driver strength values for 1.8V $V_{CC}Q$.

[Table 12] DQ Driver Strength Settings

Setting	Driver Strength	$V_{CC}Q$
Nominal	1.0x = RZQ/8 Ohms	1.8 V
Underdrive1	0.75x = RZQ/6 Ohms	

The impedance values corresponding to several different $V_{CC}Q$ values are defined in Table 14 for 1.8V $V_{CC}Q$. The test conditions that shall be used to verify the impedance values are specified in Table 13. The terms T_{OPER}(Min) and T_{OPER}(Max) are in reference to the minimum and maximum operating temperature defined for the device.

[Table 13] Testing Conditions for Impedance Values

Condition	Temperature	$V_{CC}Q$	Process
Minimum Impedance	T_{OPER} (Min) degrees Celsius	1.95 V	Fast - fast
Nominal Impedance	25 degrees Celsius	1.8 V	Typical
Maximum Impedance	T_{OPER} (Max) degrees Celsius	1.7 V	Slow-slow

[Table 14] Output Driver Strength Impedance Values

Output Strength	Rpd/Rpu	V_{OUT} to V_{SS}	Minimum	Nominal	Maximum	Units
			$V_{CC}Q$(1.8V)	$V_{CC}Q$(1.8V)	$V_{CC}Q$(1.8V)	
Nominal	Rpd	$V_{CC}Q \times 0.2$	15.0	27.0	62.5	ohms
		$V_{CC}Q \times 0.5$	18.0	37.5	66.5	ohms
		$V_{CC}Q \times 0.8$	22.0	52.0	88.0	ohms
	Rpu	$V_{CC}Q \times 0.2$	22.0	52.0	88.0	ohms
		$V_{CC}Q \times 0.5$	18.0	37.5	66.5	ohms
		$V_{CC}Q \times 0.8$	15.0	27.0	62.5	ohms
Underdrive1	Rpd	$V_{CC}Q \times 0.2$	21.5	39.0	90.0	ohms
		$V_{CC}Q \times 0.5$	26.0	50.0	95.0	ohms
		$V_{CC}Q \times 0.8$	31.5	66.5	126.5	ohms
	Rpu	$V_{CC}Q \times 0.2$	31.5	66.5	126.5	ohms
		$V_{CC}Q \times 0.5$	26.0	50.0	95.0	ohms
		$V_{CC}Q \times 0.8$	21.5	39.0	90.0	ohms

[Table 15] Output Driver Strength Impedance Values and mismatch

Output Strength	V_{OUT} to V_{SS}	Minimum	Nominal	Maximum	Units
Ron = RZQ/8	$V_{CC}Q \times 0.5$	0.85	1.0	1.15	RZQ/8
Ron = RZQ/6	$V_{CC}Q \times 0.5$	0.85	1.0	1.15	RZQ/6
Mismatch between pull-up and pull-down	$V_{CC}Q \times 0.5$	-15.0	-	+15.0	%

NOTE :
1) Across entire operating temperature range, after calibration
2) RZQ is 300ohm
3) Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5*VCCQ
4) Measurement definition for mismatch between pull-up and pull-down, MMPUPD: Measure RONPU and RONPD, both at 0.5*VCCQ

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

2.13 Input / Output Slew Rate

The input slew rate requirements that the device shall comply with are defined in Table 16 and Table 17. The output slew rate requirements that the device shall comply with are defined in Table 19. The testing conditions that shall be used to verify the input slew rate are listed in Table 18 and Table 20.

[Table 16] Derating Factor

Input slew rate	200Mbps	400Mbps		533Mbps		Unit
	1.8V$_{CC}$Q	1.8V$_{CC}$Q	Small swing	1.8V$_{CC}$Q	Small swing	
1.0V/ns	0	0	0	0	0	ps
0.8V/ns	100	100	50	100	50	
0.6V/ns	267	267	133	267	133	
0.5V/ns	400	N/A	N/A	N/A	N/A	
0.4V/ns	600	N/A	N/A	N/A	N/A	
0.3V/ns	933	N/A	N/A	N/A	N/A	

NOTE :
1) Derating factor is required when DQ slew rate is lower than minimum slew rate while the slew rate of DQS meets the minimum slew rate.

[Table 17] Input Slew Rate

V$_{CC}$Q	V$_{IL}$	V$_{IH}$	Min		
			200Mbps	400Mbps	533Mbps
1.8V	0.2 x V$_{CC}$Q	0.8 x V$_{CC}$Q	1.0V/ns	1.0V/ns	1.0V/ns
Small swing	V$_{REF}$Q -300mV	V$_{REF}$Q +300mV	-	1.0V/ns	1.0V/ns

[Table 18] Testing Conditions for Input Slew Rate

Parameter	Value
Positive Input Transition	V$_{IL}$ (DC) to V$_{IH}$ (AC)
Negative Input Transition	V$_{IH}$ (DC) to V$_{IL}$ (AC)

[Table 19] Output Slew Rate Requirements

Parameter	Minimum	Maximum	Unit
Nominal	1.05	4.0	ohms
Underdrive 1	0.90	3.5	ohms

NOTE :
1) Measured with a test load of 5pF connected to V$_{SS}$.
2) The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

[Table 20] Testing Conditions for Output Slew Rate

Parameter	Value
V_{OL} (AC)[1)]	V_{TT} - 0.1* $V_{CC}Q$
V_{OH} (AC)[1)]	V_{TT} + 0.1* $V_{CC}Q$
Positive Output Transition	V_{OL} (AC) to V_{OH} (AC)
Negative Output Transition	V_{OH} (AC) to V_{OL} (AC)
tRISE[1)]	Time during Rising Edge from V_{OL} (AC) to V_{OH} (AC)
tFALL[1)]	Time during Falling Edge from V_{OH} (AC) to V_{OL} (AC)
Output Slew Rate Rising Edge	(V_{OH} (AC) - V_{OL} (AC)) / tRISE
Output Slew Rate Falling Edge	(V_{OH} (AC) - V_{OL} (AC)) / tFALL
Output Capacitive Load	C_L = 5pF

NOTE :
1) Output termination described in Figure 6 is used.
2) Refer to Figure 7.
3) Output slew rate is verified by design and characterization. It may not be subject to production test. The minimum slew rate is the minimum of the rising edge and the falling edge slew rate. The maximum slew rate is the maximum of the rising edge and the falling edge slew rate.

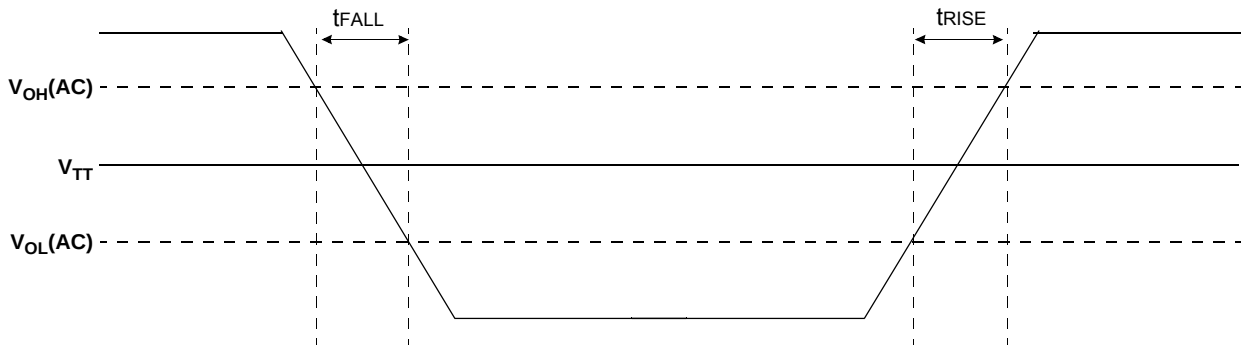


Figure 7. tRISE and tFALL Definition for Output Slew Rate

2.14 R/$\overline{B}$ and SR[6] Relationship

R/$\overline{B}$ represents the status of the selected target. R/$\overline{B}$ goes busy when only a single LUN is busy while rest of LUNs on the same target are idle.

2.15 Write Protect

When $\overline{WP}$ is enabled, Flash array is blocked from any program and erase operations. This signal shall only be transitioned when a target is idle. The host shall be allowed to issue a new command after tWW once $\overline{WP}$ is enabled.

Figure 8 describes the tWW timing requirement, shown with the start of a Program command. And Figure 9 shows with the start of a Erase command.

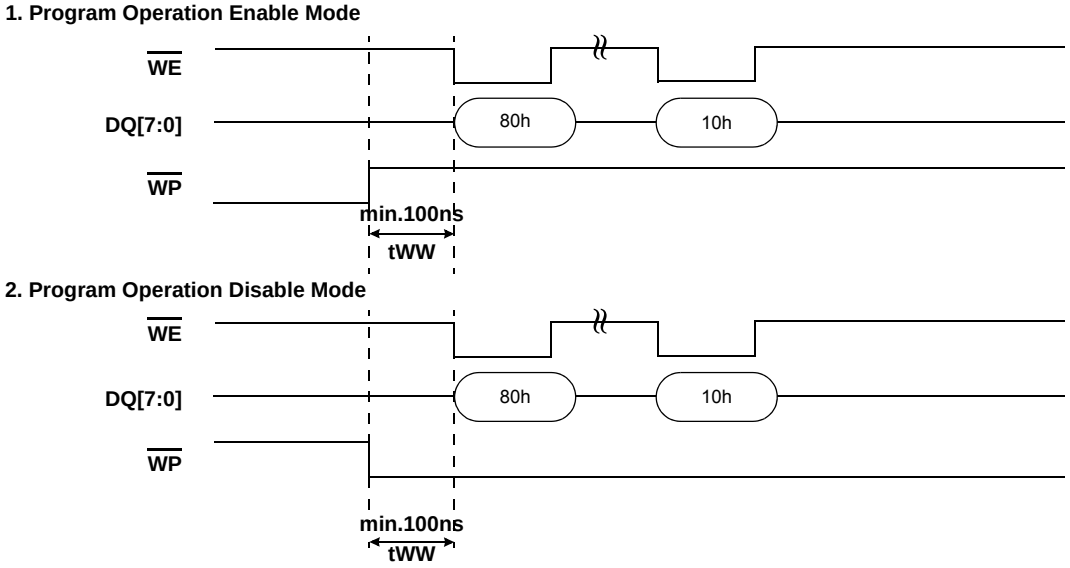


Figure 8. Write Protect Sequence Requirements of the Program Operation

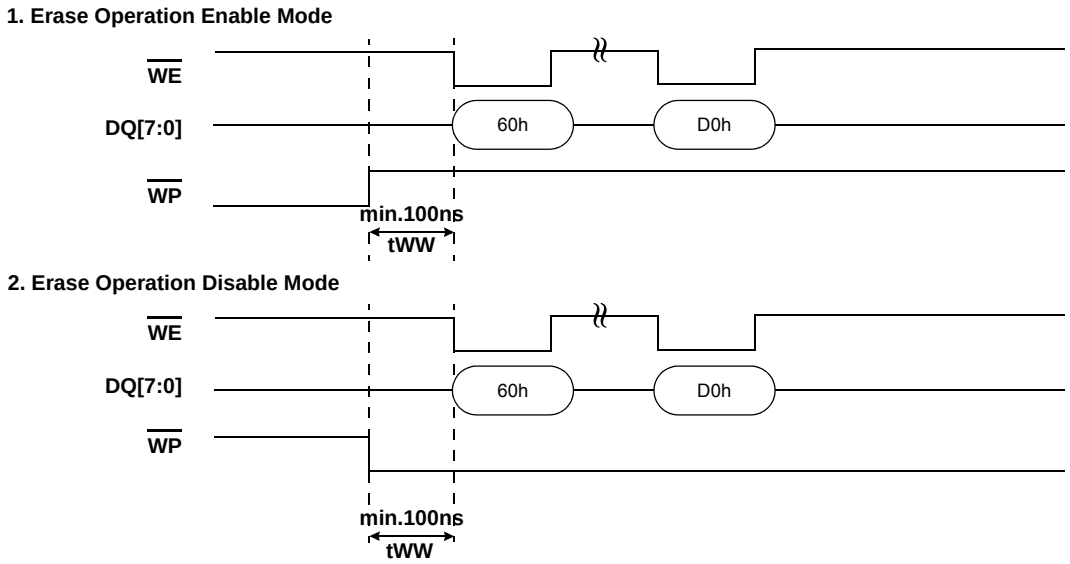


Figure 9. Write Protect Sequence Requirements of the Erase Operation

3.0 MEMORY ORGANIZATION

A device contains one or more targets. A target is controlled by one $\overline{CE}$ signal. A target is organized into one or more logical units (LUNs).

A logical unit (LUN) is the minimum unit that can independently execute commands and report status. Specifically, separate LUNs may operate on arbitrary command sequences in parallel. For example, it is permissible to start a Page Program operation on LUN 0 and then prior to the operation's completion to start a Read command on LUN 1. A LUN contains at least one page register and a Flash array. The number of page registers is dependent on the number of plane operations supported for the LUN. The Flash array contains a number of blocks.

A block is the smallest erasable unit of data within the Flash array of a LUN. There is no restriction on the number of blocks within the LUN. A block contains a number of pages.

A page is the smallest addressable unit for read and program operations.

Each LUN shall have at least one page register. A page register is used for the temporary storage of data before it is moved to a page within the Flash array or after it is moved from a page within the Flash array.

The byte location within the page register is referred to as the column.

3.1 Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into the page. The least significant bit of the column address shall always be zero for a DDR interface, i.e. an even number of bytes is always transferred. The row address is used to address pages, blocks, and LUNs.

When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses shall not be issued.

For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero.

The row address structure is shown in Figure 10 with the least significant row address bit to the right and the most significant row address bit to the left.

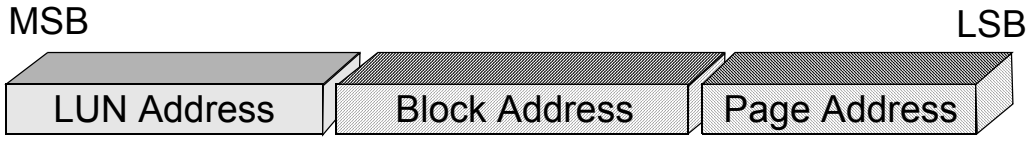


Figure 10. Row Address Layout

The page address is set by the least significant row address bits, and the LUN address is set by the most significant row address bit(s). The block address is between a page address and a LUN address.

A host shall not access an address of a page or block beyond maximum page address or block address.

3.1.1 Plane Addressing

The plane address comprises the lowest order bits of the block address as shown in Figure 11. The plane address is used when performing a Two-Plane command sequence on a particular LUN:

The plane address bit(s) shall be different within address setting sequences for the Two-Plane-related operation, while the page address shall stay the same within address setting sequences for the Two-Plane-related operation.

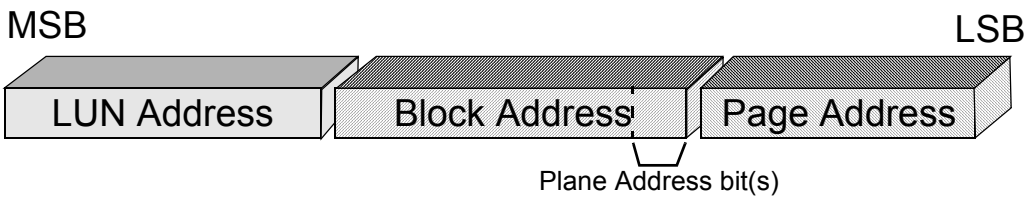


Figure 11. Position of Plane Address

3.2 Factory Defect Mapping

The Flash array is not presumed to be pristine, and a number of defects that makes the blocks unusable may be present. Invalid blocks shall be sorted out from normal blocks by software.

3.2.1 Device Requirements

If a block is defective, the manufacturer shall mark the block as defective by setting the Defective Block Marking, as shown in Figure 12, of the 1st page of the defective block to a value of non-FFh. The Defective Block Marking is located on the first byte of user data area or the first byte of spare data area in the pages within a block.

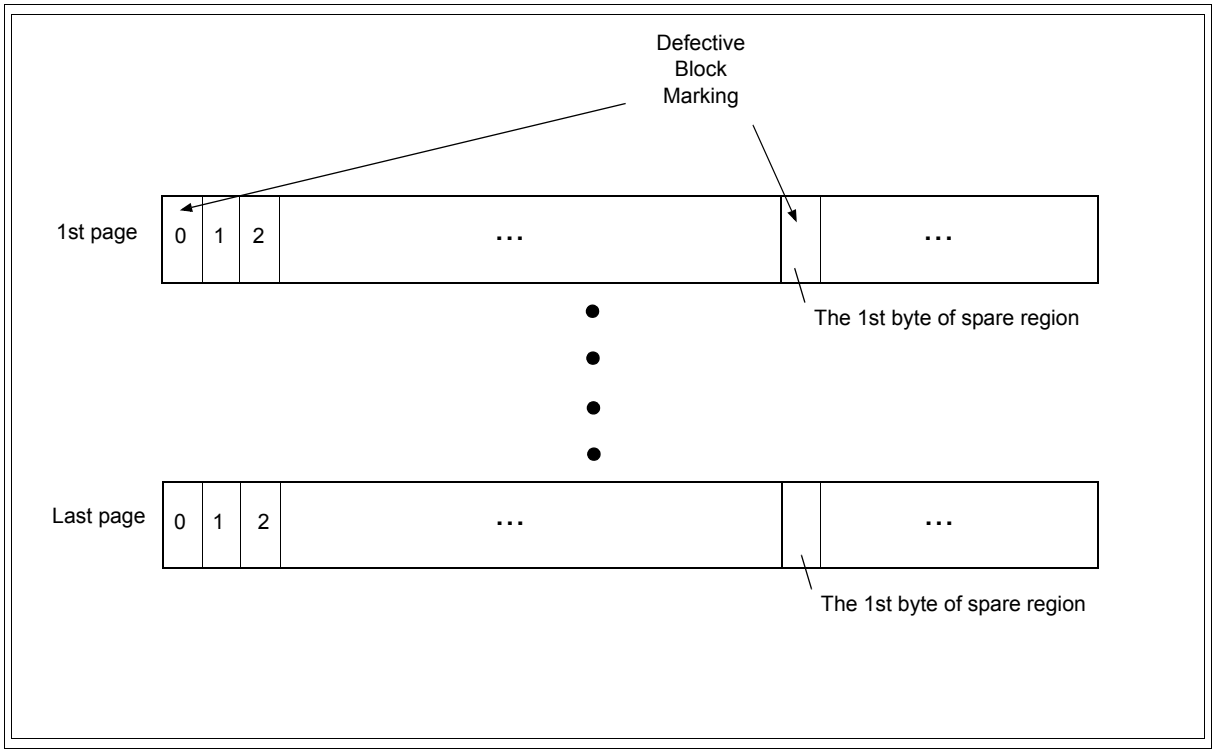


Figure 12. Area marked in first or last page of block indicating defect

3.2.2 Host Requirements

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results.

Figure 13 outlines the flow chart how to create an initial invalid block table. It should be performed at SLC mode by the host to create the initial bad block table prior to performing any erase or programming operations on the target. The 1st byte of main or spare region in non-defective blocks are read FFh with ECC enabled on the controller. A defective block is indicated by the majority of bits being read non-FFh in the Defective Block Marking location of either the first page or last page of the block. The host shall check the Defective Block Marking location of both the first and last past page of each block to verify the block is valid prior to any erase or program operations on that block.

NOTE :
Over the lifetime use of a NAND device, the Defective Block Marking of defective blocks may encounter read disturbs that cause bit changes. The initial defect marks by the manufacturer may change value over the lifetime of the device, and are expected to be read by the host and used to create a bad block table during initial use of the part.

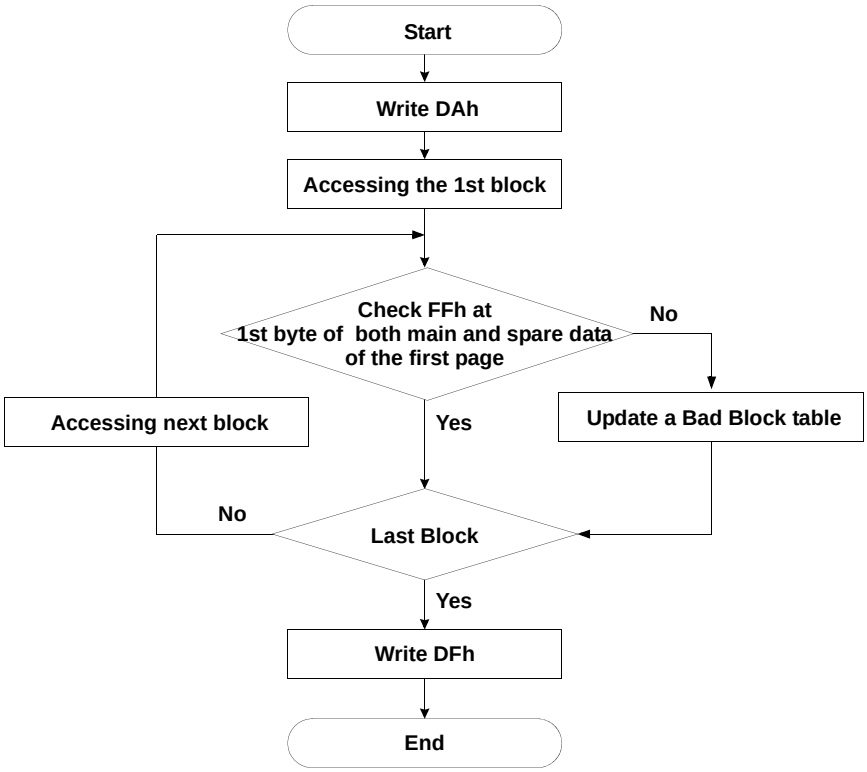


Figure 13. Flow chart to create initial invalid block table

3.3 Error in Write or Read Operation

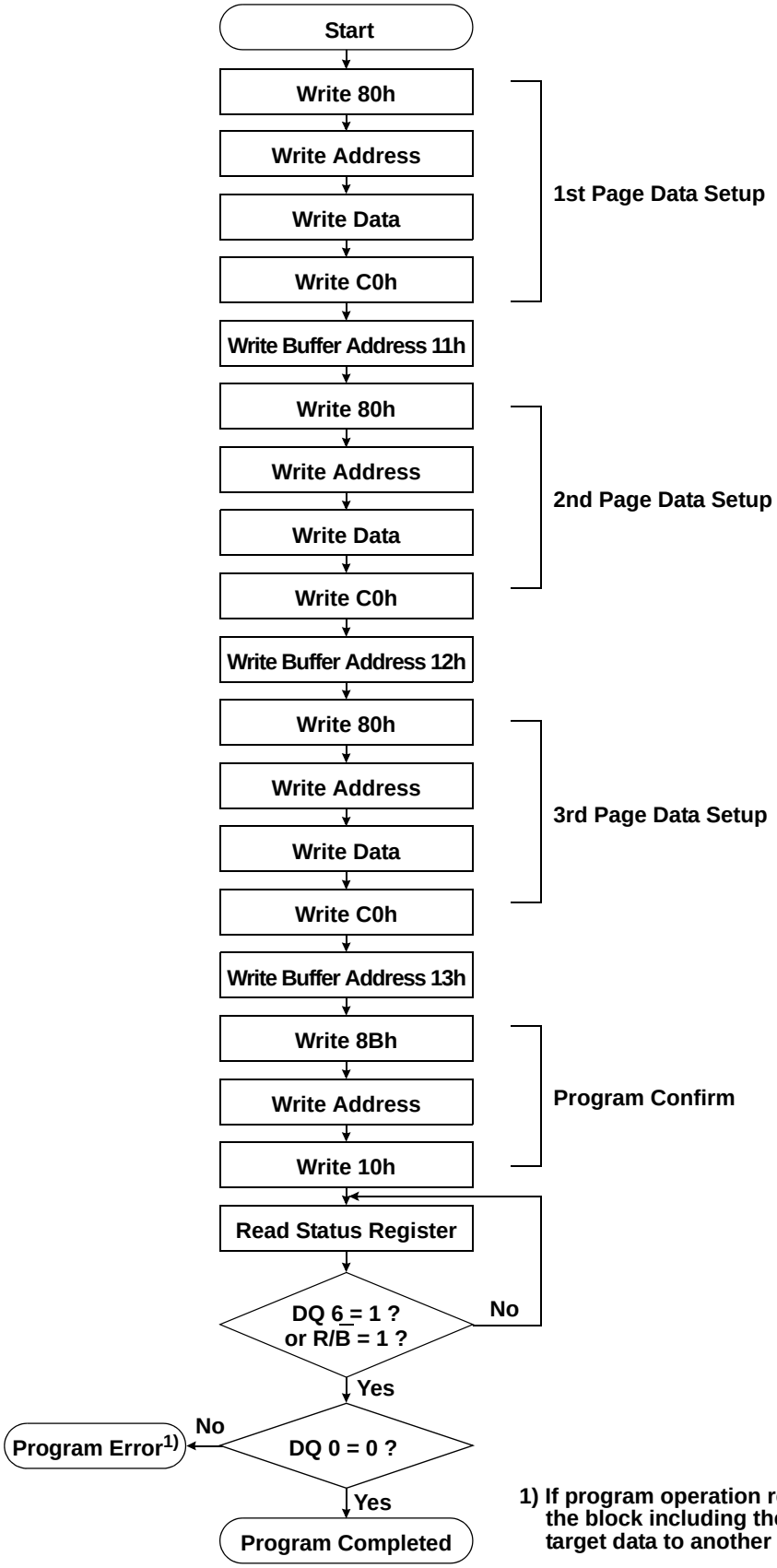
Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

[Table 21] Failure cases

Failure Mode		Detection and Countermeasure sequence
Write	Program Failure	Read Status after Program --> Block Replacement
Erase	Erase Failure	Read Status after Erase --> Block Replacement
Read	Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code

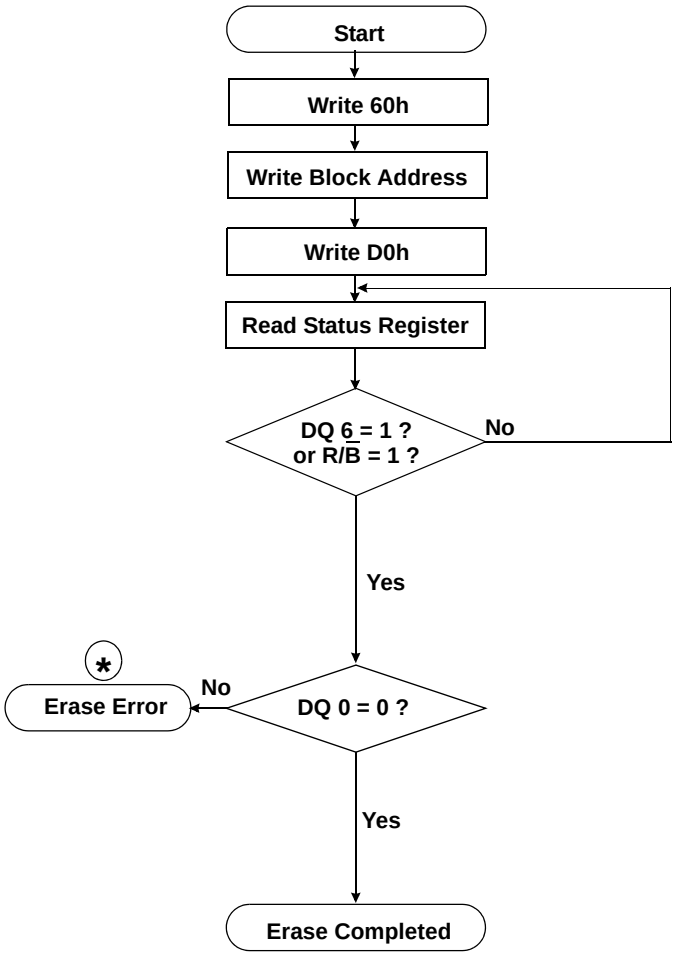
TLC Program Flow Chart



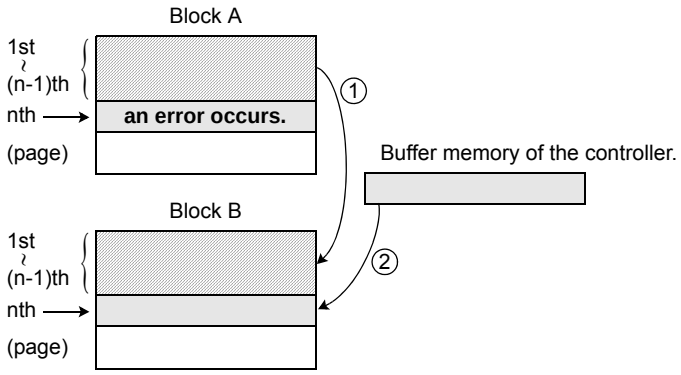
1) If program operation results in an error, map out the block including the page in error and copy the target data to another block.

(*) : If erase operation results in an error, map out the failing block and replace it with another block.

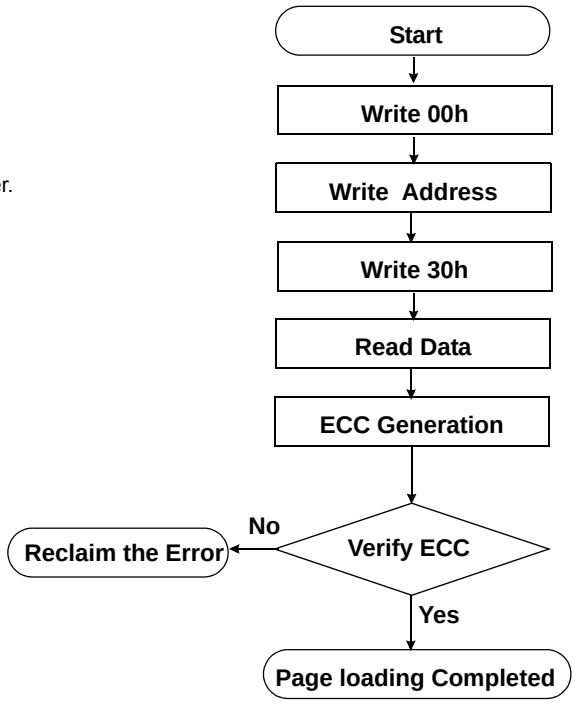
Erase Flow Chart



Block Replacement



Read Flow Chart



*Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

3.4 Addressing For Program Operation

3bit/cell NAND has the following programming characteristics. The fine programming to one WL consists of 3 steps of program operation. 3 pages' data, LSB, CSB and MSB, has to be stored for each program operation to make 8 program states at the same time.

[Table 22] TLC HSP Addressing

Group A	Group B	Group C	Group D
0x00	0x01	0x02	0x03
0x04	0x05	0x06	0x07
0x08	0x09	0x0A	0x0B
0x0C	0x0D	0x0E	0x0F
0x10	0x11	0x12	0x13
0x14	0x15	0x16	0x17
0x18	0x19	0x1A	0x1B
0x1C	0x1D	0x1E	0x1F
0x20	0x21	0x22	0x23
0x24	0x25	0x26	0x27
0x28	0x29	0x2A	0x2B
0x2C	0x2D	0x2E	0x2F
0x30	0x31	0x32	0x33
0x34	0x35	0x36	0x37
0x38	0x39	0x3A	0x3B
0x3C	0x3D	0x3E	0x3F
0x40	0x41	0x42	0x43
0x44	0x45	0x46	0x47
0x48	0x49	0x4A	0x4B
0x4C	0x4D	0x4E	0x4F
0x50	0x51	0x52	0x53
0x54	0x55	0x56	0x57
0x58	0x59	0x5A	0x5B
0x5C	0x5D	0x5E	0x5F
0x60	0x61	0x62	0x63
0x64	0x65	0x66	0x67
0x68	0x69	0x6A	0x6B
0x6C	0x6D	0x6E	0x6F
0x70	0x71	0x72	0x73
0x74	0x75	0x76	0x77
0x78	0x79	0x7A	0x7B
0x7C	0x7D	0x7E	0x7F
0x80	0x81	0x82	0x83
0x84	0x85	0x86	0x87
0x88	0x89	0x8A	0x8B
0x8C	0x8D	0x8E	0x8F
0x90	0x91	0x92	0x93
0x94	0x95	0x96	0x97
0x98	0x99	0x9A	0x9B
0x9C	0x9D	0x9E	0x9F
0xA0	0xA1	0xA2	0xA3
0xA4	0xA5	0xA6	0xA7
0xA8	0xA9	0xAA	0xAB
0xAC	0xAD	0xAE	0xAF
0xB0	0xB1	0xB2	0xB3
0xB4	0xB5	0xB6	0xB7
0xB8	0xB9	0xBA	0xBB
0xBC	0xBD	0xBE	0xBF

Group A	Group B	Group C	Group D
0xC0	0xC1	0xC2	0xC3
0xC4	0xC5	0xC6	0xC7
0xC8	0xC9	0xCA	0xCB
0xCC	0xCD	0xCE	0xCF
0xD0	0xD1	0xD2	0xD3
0xD4	0xD5	0xD6	0xD7
0xD8	0xD9	0xDA	0xDB
0xDC	0xDD	0xDE	0xDF
0xE0	0xE1	0xE2	0xE3
0xE4	0xE5	0xE6	0xE7
0xE8	0xE9	0xEA	0xEB
0xEC	0xED	0xEE	0xEF
0xF0	0xF1	0xF2	0xF3
0xF4	0xF5	0xF6	0xF7
0xF8	0xF9	0xFA	0xFB
0xFC	0xFD	0xFE	0xFF
0x100	0x101	0x102	0x103
0x104	0x105	0x106	0x107

[Table 23] TLC Read Addressing

Group A			Group B			Group C			Group D		
LSB	CSB	MSB	LSB	CSB	MSB	LSB	CSB	MSB	LSB	CSB	MSB
	0x00	0x01		0x02	0x03		0x04	0x05		0x06	0x07
0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	0x10	0x11	0x12	0x13
0x14	0x15	0x16	0x17	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F
0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27	0x28	0x29	0x2A	0x2B
0x2C	0x2D	0x2E	0x2F	0x30	0x31	0x32	0x33	0x34	0x35	0x36	0x37
0x38	0x39	0x3A	0x3B	0x3C	0x3D	0x3E	0x3F	0x40	0x41	0x42	0x43
0x44	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C	0x4D	0x4E	0x4F
0x50	0x51	0x52	0x53	0x54	0x55	0x56	0x57	0x58	0x59	0x5A	0x5B
0x5C	0x5D	0x5E	0x5F	0x60	0x61	0x62	0x63	0x64	0x65	0x66	0x67
0x68	0x69	0x6A	0x6B	0x6C	0x6D	0x6E	0x6F	0x70	0x71	0x72	0x73
0x74	0x75	0x76	0x77	0x78	0x79	0x7A	0x7B	0x7C	0x7D	0x7E	0x7F
0x80	0x81	0x82	0x83	0x84	0x85	0x86	0x87	0x88	0x89	0x8A	0x8B
0x8C	0x8D	0x8E	0x8F	0x90	0x91	0x92	0x93	0x94	0x95	0x96	0x97
0x98	0x99	0x9A	0x9B	0x9C	0x9D	0x9E	0x9F	0xA0	0xA1	0xA2	0xA3
0xA4	0xA5	0xA6	0xA7	0xA8	0xA9	0xAA	0xAB	0xAC	0xAD	0xAE	0xAF
0xB0	0xB1	0xB2	0xB3	0xB4	0xB5	0xB6	0xB7	0xB8	0xB9	0xBA	0xBB
0xBC	0xBD	0xBE	0xBF	0xC0	0xC1	0xC2	0xC3	0xC4	0xC5	0xC6	0xC7
0xC8	0xC9	0xCA	0xCB	0xCC	0xCD	0xCE	0xCF	0xD0	0xD1	0xD2	0xD3
0xD4	0xD5	0xD6	0xD7	0xD8	0xD9	0xDA	0xDB	0xDC	0xDD	0xDE	0xDF
0xE0	0xE1	0xE2	0xE3	0xE4	0xE5	0xE6	0xE7	0xE8	0xE9	0xEA	0xEB
0xEC	0xED	0xEE	0xEF	0xF0	0xF1	0xF2	0xF3	0xF4	0xF5	0xF6	0xF7
0xF8	0xF9	0xFA	0xFB	0xFC	0xFD	0xFE	0xFF	0x100	0x101	0x102	0x103
0x104	0x105	0x106	0x107	0x108	0x109	0x10A	0x10B	0x10C	0x10D	0x10E	0x10F
0x110	0x111	0x112	0x113	0x114	0x115	0x116	0x117	0x118	0x119	0x11A	0x11B
0x11C	0x11D	0x11E	0x11F	0x120	0x121	0x122	0x123	0x124	0x125	0x126	0x127
0x128	0x129	0x12A	0x12B	0x12C	0x12D	0x12E	0x12F	0x130	0x131	0x132	0x133
0x134	0x135	0x136	0x137	0x138	0x139	0x13A	0x13B	0x13C	0x13D	0x13E	0x13F
0x140	0x141	0x142	0x143	0x144	0x145	0x146	0x147	0x148	0x149	0x14A	0x14B
0x14C	0x14D	0x14E	0x14F	0x150	0x151	0x152	0x153	0x154	0x155	0x156	0x157
0x158	0x159	0x15A	0x15B	0x15C	0x15D	0x15E	0x15F	0x160	0x161	0x162	0x163
0x164	0x165	0x166	0x167	0x168	0x169	0x16A	0x16B	0x16C	0x16D	0x16E	0x16F
0x170	0x171	0x172	0x173	0x174	0x175	0x176	0x177	0x178	0x179	0x17A	0x17B
0x17C	0x17D	0x17E	0x17F	0x180	0x181	0x182	0x183	0x184	0x185	0x186	0x187
0x188	0x189	0x18A	0x18B	0x18C	0x18D	0x18E	0x18F	0x190	0x191	0x192	0x193
0x194	0x195	0x196	0x197	0x198	0x199	0x19A	0x19B	0x19C	0x19D	0x19E	0x19F
0x1A0	0x1A1	0x1A2	0x1A3	0x1A4	0x1A5	0x1A6	0x1A7	0x1A8	0x1A9	0x1AA	0x1AB
0x1AC	0x1AD	0x1AE	0x1AF	0x1B0	0x1B1	0x1B2	0x1B3	0x1B4	0x1B5	0x1B6	0x1B7
0x1B8	0x1B9	0x1BA	0x1BB	0x1BC	0x1BD	0x1BE	0x1BF	0x1C0	0x1C1	0x1C2	0x1C3
0x1C4	0x1C5	0x1C6	0x1C7	0x1C8	0x1C9	0x1CA	0x1CB	0x1CC	0x1CD	0x1CE	0x1CF
0x1D0	0x1D1	0x1D2	0x1D3	0x1D4	0x1D5	0x1D6	0x1D7	0x1D8	0x1D9	0x1DA	0x1DB
0x1DC	0x1DD	0x1DE	0x1DF	0x1E0	0x1E1	0x1E2	0x1E3	0x1E4	0x1E5	0x1E6	0x1E7
0x1E8	0x1E9	0x1EA	0x1EB	0x1EC	0x1ED	0x1EE	0x1EF	0x1F0	0x1F1	0x1F2	0x1F3
0x1F4	0x1F5	0x1F6	0x1F7	0x1F8	0x1F9	0x1FA	0x1FB	0x1FC	0x1FD	0x1FE	0x1FF
0x200	0x201	0x202	0x203	0x204	0x205	0x206	0x207	0x208	0x209	0x20A	0x20B
0x20C	0x20D	0x20E	0x20F	0x210	0x211	0x212	0x213	0x214	0x215	0x216	0x217
0x218	0x219	0x21A	0x21B	0x21C	0x21D	0x21E	0x21F	0x220	0x221	0x222	0x223
0x224	0x225	0x226	0x227	0x228	0x229	0x22A	0x22B	0x22C	0x22D	0x22E	0x22F

Group A			Group B			Group C			Group D		
LSB	CSB	MSB	LSB	CSB	MSB	LSB	CSB	MSB	LSB	CSB	MSB
0x230	0x231	0x232	0x233	0x234	0x235	0x236	0x237	0x238	0x239	0x23A	0x23B
0x23C	0x23D	0x23E	0x23F	0x240	0x241	0x242	0x243	0x244	0x245	0x246	0x247
0x248	0x249	0x24A	0x24B	0x24C	0x24D	0x24E	0x24F	0x250	0x251	0x252	0x253
0x254	0x255	0x256	0x257	0x258	0x259	0x25A	0x25B	0x25C	0x25D	0x25E	0x25F
0x260	0x261	0x262	0x263	0x264	0x265	0x266	0x267	0x268	0x269	0x26A	0x26B
0x26C	0x26D	0x26E	0x26F	0x270	0x271	0x272	0x273	0x274	0x275	0x276	0x277
0x278	0x279	0x27A	0x27B	0x27C	0x27D	0x27E	0x27F	0x280	0x281	0x282	0x283
0x284	0x285	0x286	0x287	0x288	0x289	0x28A	0x28B	0x28C	0x28D	0x28E	0x28F
0x290	0x291	0x292	0x293	0x294	0x295	0x296	0x297	0x298	0x299	0x29A	0x29B
0x29C	0x29D	0x29E	0x29F	0x2A0	0x2A1	0x2A2	0x2A3	0x2A4	0x2A5	0x2A6	0x2A7
0x2A8	0x2A9	0x2AA	0x2AB	0x2AC	0x2AD	0x2AE	0x2AF	0x2B0	0x2B1	0x2B2	0x2B3
0x2B4	0x2B5	0x2B6	0x2B7	0x2B8	0x2B9	0x2BA	0x2BB	0x2BC	0x2BD	0x2BE	0x2BF
0x2C0	0x2C1	0x2C2	0x2C3	0x2C4	0x2C5	0x2C6	0x2C7	0x2C8	0x2C9	0x2CA	0x2CB
0x2CC	0x2CD	0x2CE	0x2CF	0x2D0	0x2D1	0x2D2	0x2D3	0x2D4	0x2D5	0x2D6	0x2D7
0x2D8	0x2D9	0x2DA	0x2DB	0x2DC	0x2DD	0x2DE	0x2DF	0x2E0	0x2E1	0x2E2	0x2E3
0x2E4	0x2E5	0x2E6	0x2E7	0x2E8	0x2E9	0x2EA	0x2EB	0x2EC	0x2ED	0x2EE	0x2EF
	0x2F0	0x2F1		0x2F2	0x2F3		0x2F4	0x2F5		0x2F6	0x2F7
		0x2F8			0x2F9			0x2FA			0x2FB
		0x2FC			0x2FD			0x2FE			0x2FF

[Table 24] SLC Program Addressing = SLC Read Addressing

Group A	Group B	Group C	Group D
0x00	0x01	0x02	0x03
0x04	0x05	0x06	0x07
0x08	0x09	0x0A	0x0B
0x0C	0x0D	0x0E	0x0F
0x10	0x11	0x12	0x13
0x14	0x15	0x16	0x17
0x18	0x19	0x1A	0x1B
0x1C	0x1D	0x1E	0x1F
0x20	0x21	0x22	0x23
0x24	0x25	0x26	0x27
0x28	0x29	0x2A	0x2B
0x2C	0x2D	0x2E	0x2F
0x30	0x31	0x32	0x33
0x34	0x35	0x36	0x37
0x38	0x39	0x3A	0x3B
0x3C	0x3D	0x3E	0x3F
0x40	0x41	0x42	0x43
0x44	0x45	0x46	0x47
0x48	0x49	0x4A	0x4B
0x4C	0x4D	0x4E	0x4F
0x50	0x51	0x52	0x53
0x54	0x55	0x56	0x57
0x58	0x59	0x5A	0x5B
0x5C	0x5D	0x5E	0x5F
0x60	0x61	0x62	0x63
0x64	0x65	0x66	0x67
0x68	0x69	0x6A	0x6B
0x6C	0x6D	0x6E	0x6F
0x70	0x71	0x72	0x73
0x74	0x75	0x76	0x77
0x78	0x79	0x7A	0x7B
0x7C	0x7D	0x7E	0x7F
0x80	0x81	0x82	0x83
0x84	0x85	0x86	0x87
0x88	0x89	0x8A	0x8B
0x8C	0x8D	0x8E	0x8F
0x90	0x91	0x92	0x93
0x94	0x95	0x96	0x97
0x98	0x99	0x9A	0x9B
0x9C	0x9D	0x9E	0x9F
0xA0	0xA1	0xA2	0xA3
0xA4	0xA5	0xA6	0xA7
0xA8	0xA9	0xAA	0xAB
0xAC	0xAD	0xAE	0xAF
0xB0	0xB1	0xB2	0xB3
0xB4	0xB5	0xB6	0xB7
0xB8	0xB9	0xBA	0xBB
0xBC	0xBD	0xBE	0xBF
0xC0	0xC1	0xC2	0xC3
0xC4	0xC5	0xC6	0xC7
0xC8	0xC9	0xCA	0xCB
0xCC	0xCD	0xCE	0xCF

Group A	Group B	Group C	Group D
0xD0	0xD1	0xD2	0xD3
0xD4	0xD5	0xD6	0xD7
0xD8	0xD9	0xDA	0xDB
0xDC	0xDD	0xDE	0xDF
0xE0	0xE1	0xE2	0xE3
0xE4	0xE5	0xE6	0xE7
0xE8	0xE9	0xEA	0xEB
0xEC	0xED	0xEE	0xEF
0xF0	0xF1	0xF2	0xF3
0xF4	0xF5	0xF6	0xF7
0xF8	0xF9	0xFA	0xFB
0xFC	0xFD	0xFE	0xFF

4.0 FUNCTION DESCRIPTION

4.1 Data Protection and Power Transition Sequence

4.1.1 Data Protection

The device is designed to offer protection from any involuntary program/erase during power transitions. An internal voltage detector disables all internal program/erase circuits when V_{CC} is below about 2V. $\overline{WP}$_n pin provides hardware protection and is recommended to be kept at V_{IL} during power transitions. Although two step command sequence for program/erase provides protection from any operations by unintentional command input, keeping CLE and ALE at V_{IL} prevents any spurious commands asserted during power transitions.

It is highly recommended to keep $\overline{CE}$ at VIH to prevent unnecessary current consumption during power transitions.

4.1.2 Power Up Sequence

For NAND devices that support $V_{CC}Q$ for I/O power supply, $V_{CC}Q$ must not exceed V_{CC} during power up. The host must wait for R/$\overline{B}$ to be valid High before issuing Reset command (FFh) to initialize any targets that share same $\overline{CE}$. The R/$\overline{B}$_n signal becomes valid after 100us since both V_{CC} and $V_{CC}Q$ reach 1.7V. The RESET command (FFh) must be issued to all targets as the first command after the NAND device is powered up and R/$\overline{B}$_n becomes valid. Each target ($\overline{CE}$_n) will be busy for a maximum of 5ms after the RESET command (FFh) is issued. The RESET busy time can be monitored by polling R/$\overline{B}$ or issuing the READ STATUS(70h) command. Each NAND LUN(i.e. die) may draw less than 10mA over 1ms prior to the execution of the first RESET command (FFh) after the device is powered on. During the power up sequence including the RESET busy time, each LUN consumes a maximum current of 50mA.

4.1.3 Power Down Sequence

During power-down, $V_{CC}Q$ shall not exceed V_{CC}.

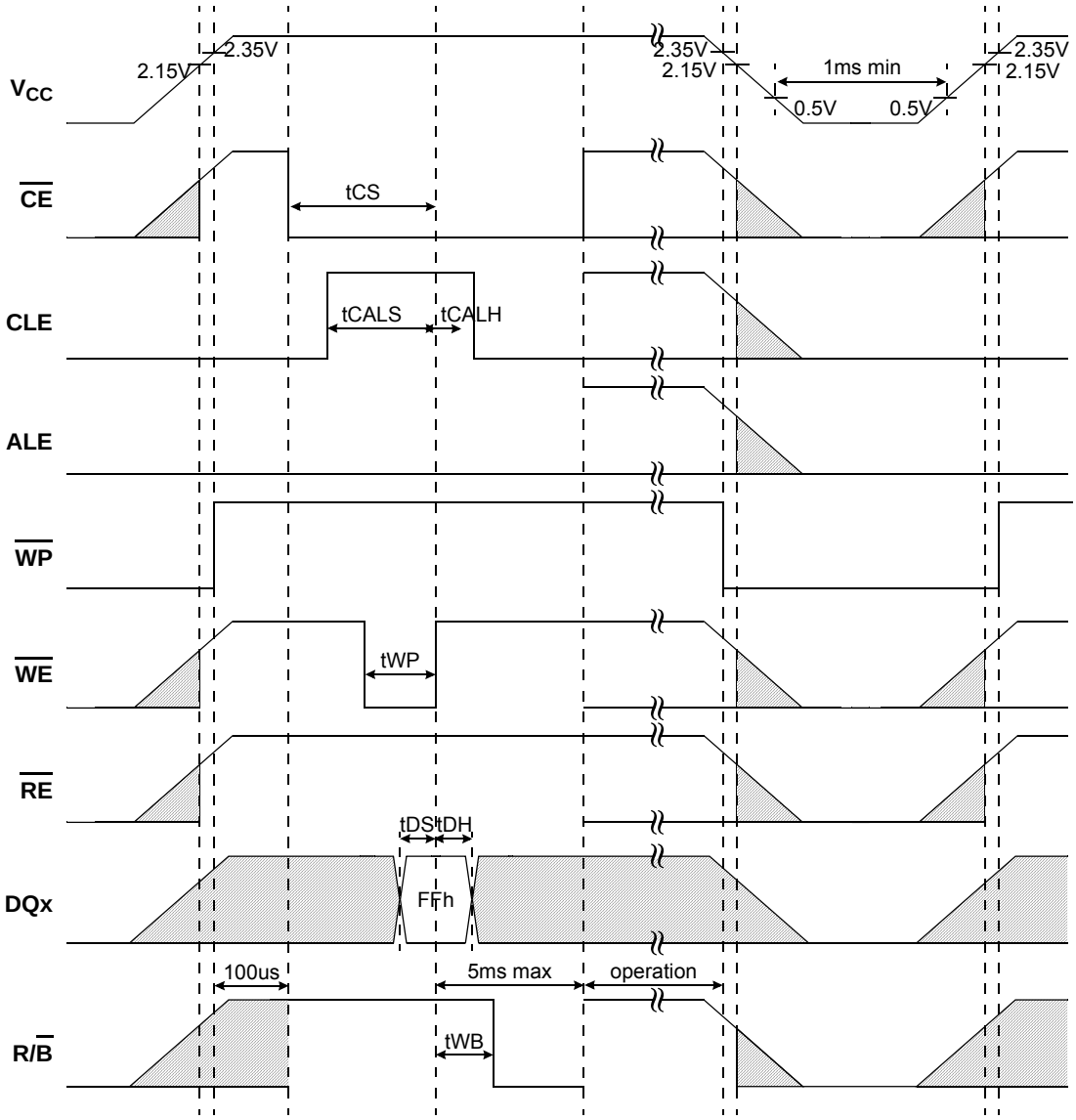


Figure 14. Initialization Timing

NOTE :
1) V_{CC} shall be same or 0.2V higher than $V_{CC}Q$. ($V_{CC}Q+0.2V < V_{CC}$)
2) Once V_{CC} drops under 2.15V, V_{CC} is recommended that it should be driven down to 0.5V and stay low under 0.5V for at least 1ms before V_{CC} powered up.
3) Maximum DC voltage on input and I/O pins is $V_{CC}Q+0.3V$ which, during transition, may have overshoot that is defined in Table 8.

4.2 Mode Selection

Table 25 describes the bus state for the Toggle DDR. Commands, addresses and data is all written through DQ's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the DQ pins.
Host reads or writes data to the device using DQS signal. And data is latched on the falling and rising both edge of DQS on data input.

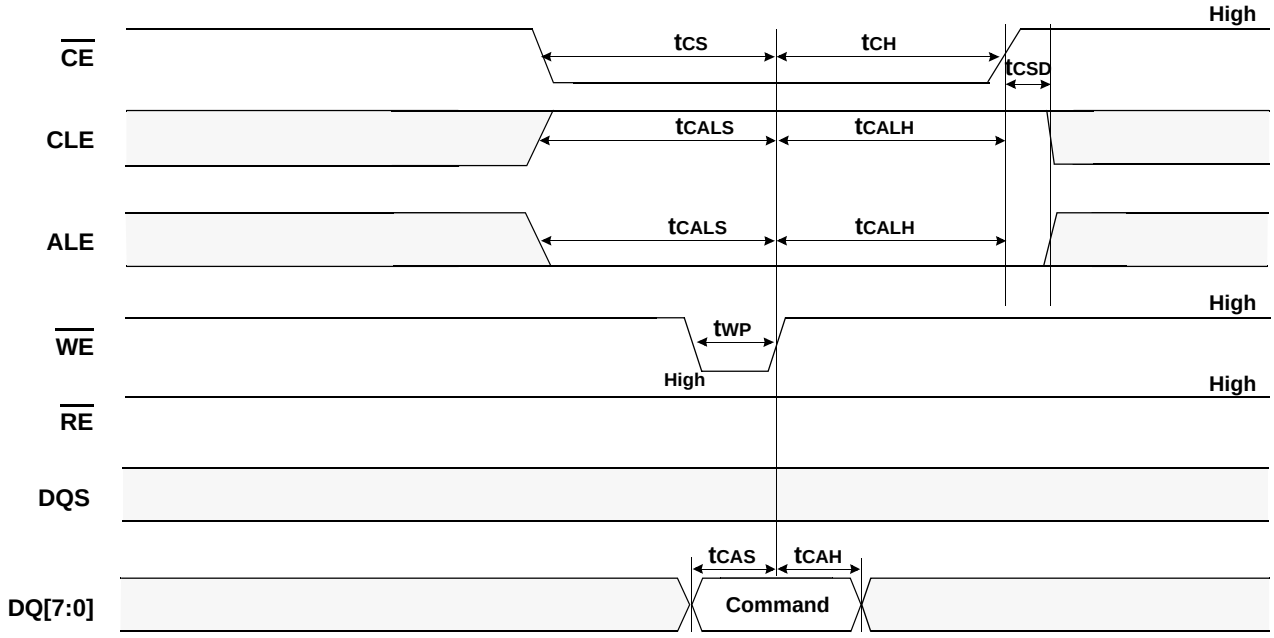
[Table 25] Mode Selection

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	DQS	$\overline{WP}$	Mode	
H	L	L		H	X[1)]	X	Read Mode	Command Input
L	H	L		H	X	X		Address Input(5 cycles)
H	L	L		H	X	H	Write Mode	Command Input
L	H	L		H	X	H		Address Input(5 cycles)
L	L	L	H	H		H	Data Input	
L	L	L	H			X	Data Output	
X	X	X	X	H	X	X	During Read(Busy)	
X	X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	X	H	During Erase(Busy)	
X	X	X	X	X	X	L	Write Protect	
X	X	H	X	X	X	0V/V_{CC}[2)]	Stand-by	

NOTE :
1) X can be V_{IL} or V_{IH}.
2) $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.
3) Data input by DQS transition in the middle of command input(e.g. 80h/81h/85h) and address input(e.g. 5 cycle of column address and row address) sequence is prohibited.

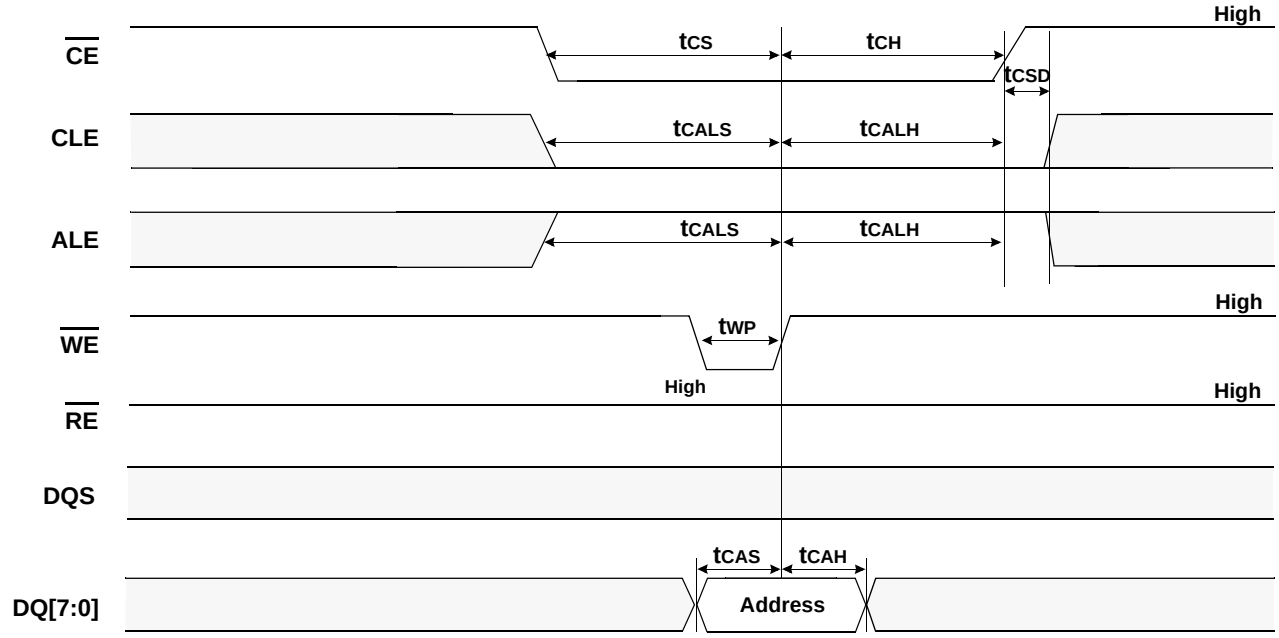
4.3 General Timing

4.3.1 Command Latch Cycle



NOTE :
1) Command information is latched by $\overline{WE}$ going 'High' when $\overline{CE}$ is 'Low', CLE is 'High', and ALE is 'Low'.

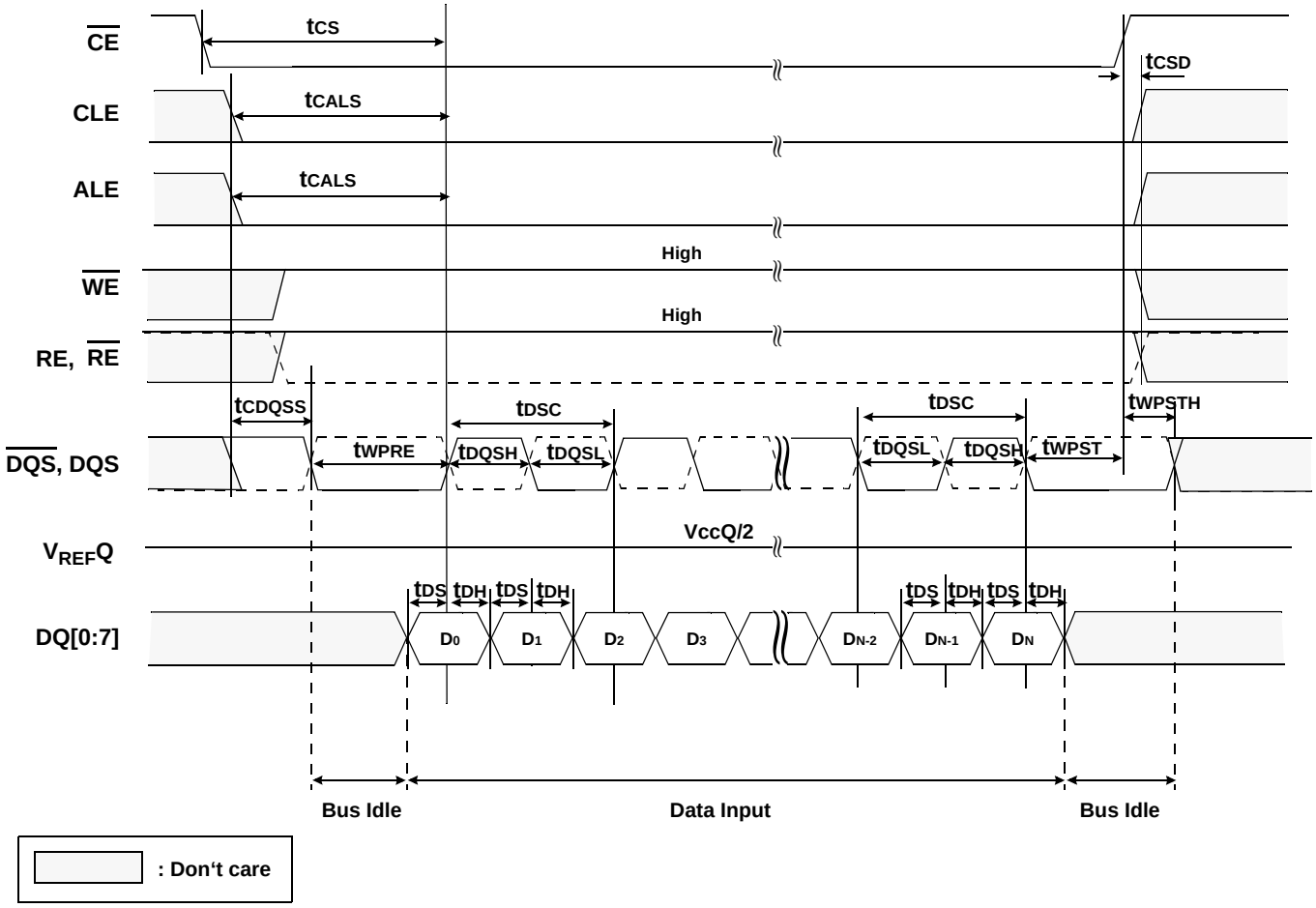
4.3.2 Address Latch Cycle



: Don't care

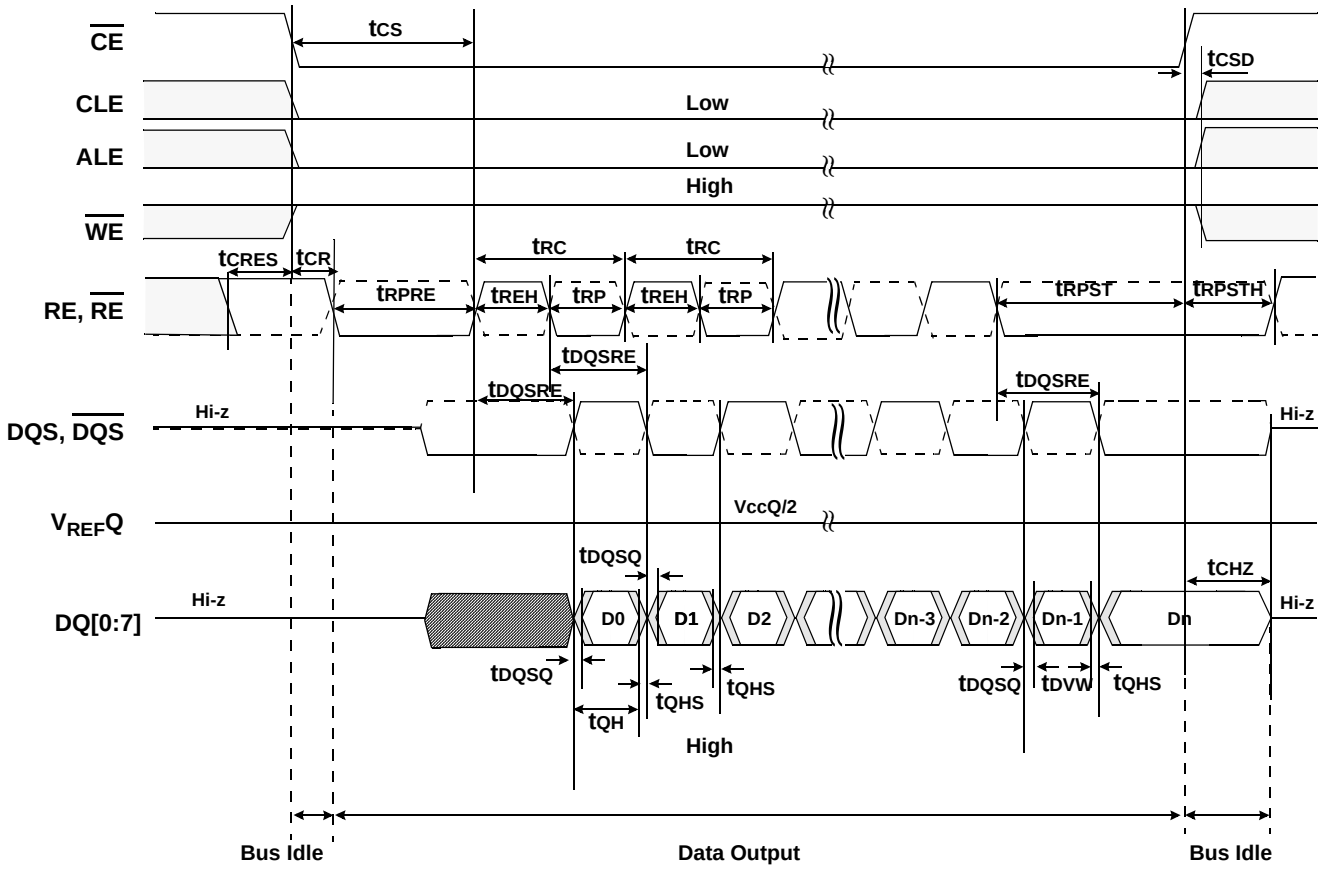
NOTE :
1) Address information is latched by $\overline{WE}$ going 'High' when $\overline{CE}$ is 'Low', CLE is 'Low', and ALE is 'High'.

4.3.3 Basic Data Input Timing



NOTE :
1) DQS, $\overline{DQS}$ and Data input buffers are turned-on when $\overline{CE}$ and DQS goes 'Low' and Data inputs begin with DQS, $\overline{DQS}$ toggling simultaneously.
2) ALE and CLE should not toggle during tWPRE period and during tCALS.
3) DQS and Data input buffers are turned-off if either CLE or $\overline{CE}$ goes 'High'.
4) tCDQSS is defined from the last data input condition of the control signals such as $\overline{CE}$, CLE and ALE.
5) DQS can be high or low during tCDQSS.

4.3.4 Basic Data Output Timing

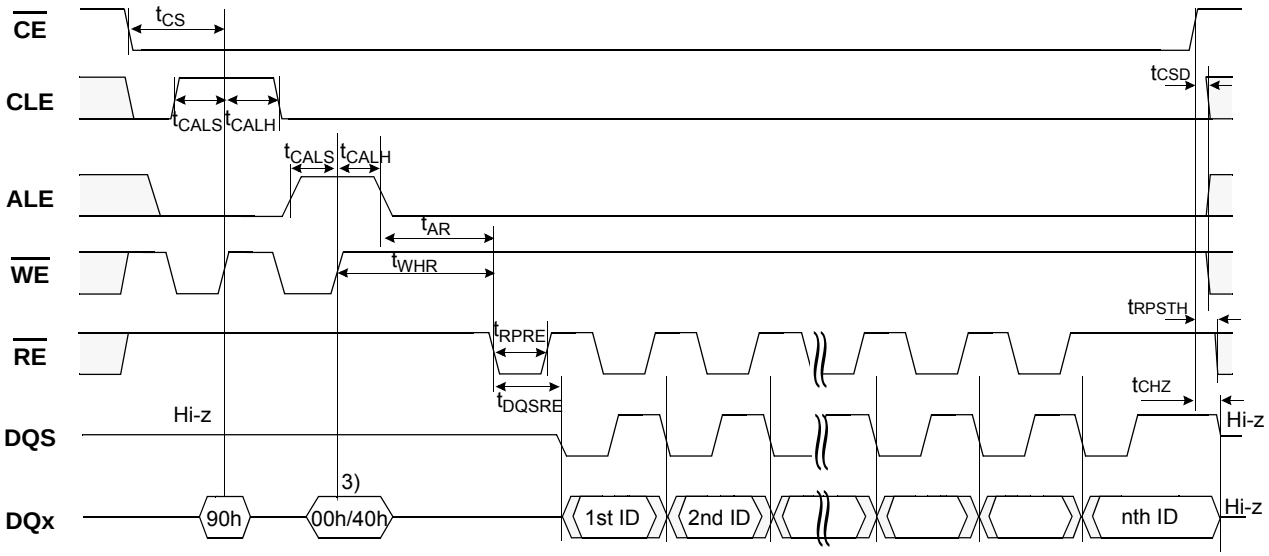


: Don‘t care

: Undefined(Driven by NAND)

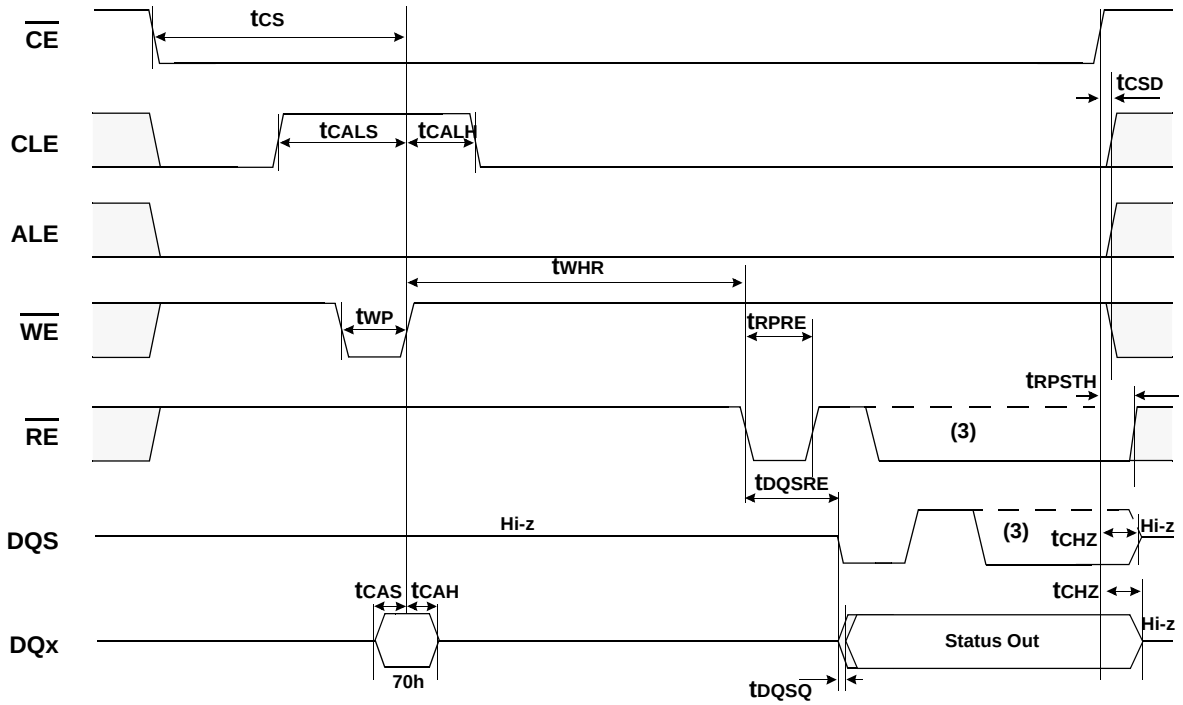
NOTE :
1) DQS, DQS and DQ drivers are turned-on when CE and RE goes Low for data out operation.
2) ALE and CLE should not toggle during tRPRE period regardless of tCALS.
3) DQS and DQ drivers turn from valid value to high-z if either CLE or CE goes high.
4) The least significant bit of the column address shall always be zero.
5) RE shall be high during tCRES.

4.3.5 Read ID Operation



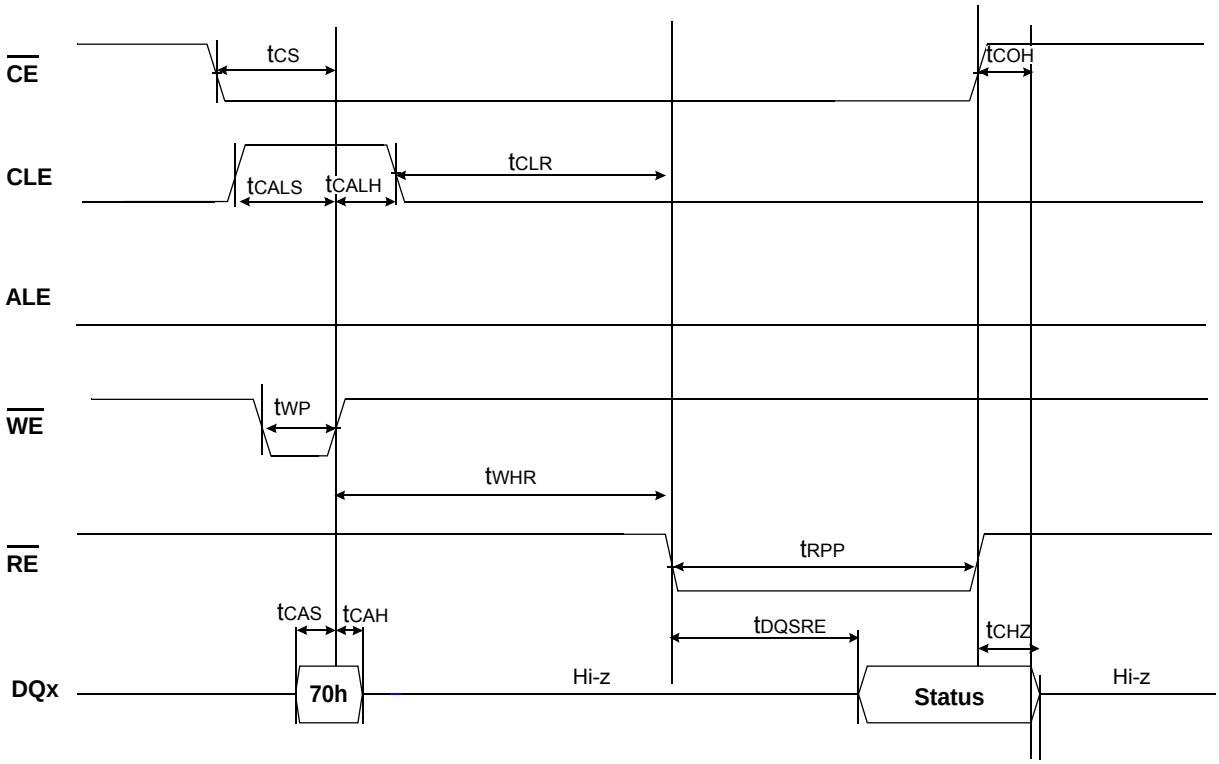
NOTE :
1) Even though toggle-mode NAND uses both low- and high-going edges of DQS for reads, ID read operation repeates each data byte twice, so that ID read timing becomes identical to that of conventional NAND.
2) DQS and DQ drivers turn from valid value to high-z when $\overline{CE}$ or CLE goes High.
3) Address 00h is for Samsung conventional and 40h is for new JEDEC ID information.

4.3.6 Read Status Cycle



NOTE :
1) Even though toggle-mode NAND uses both low and high-going edges of DQS for reads, Read Status operation7 same output until device status changes.
2) DQS and Data out buffers turn from valid value to high-z when $\overline{CE}$ or CLE goes High.
3) $\overline{RE}$ can toggle more than once.

4.3.6.1 Read Status Cycle before Toggle DDR Setting at Initialization Sequence by FFh Command



4.3.7 Set Feature

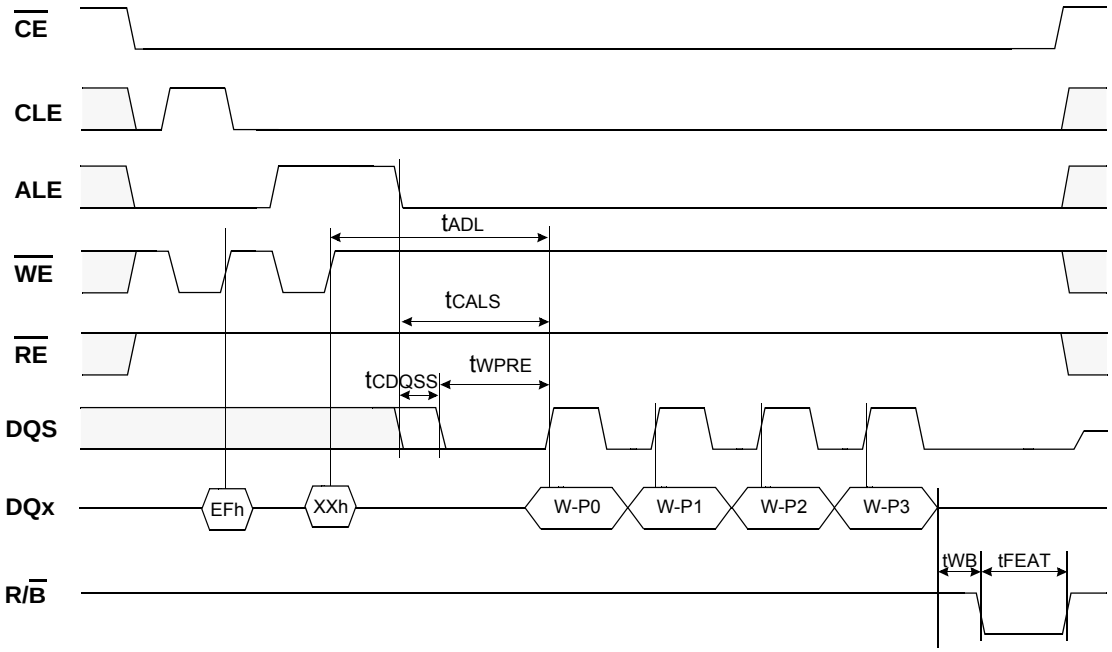


Figure 15. Set Feature(EFh) Timing

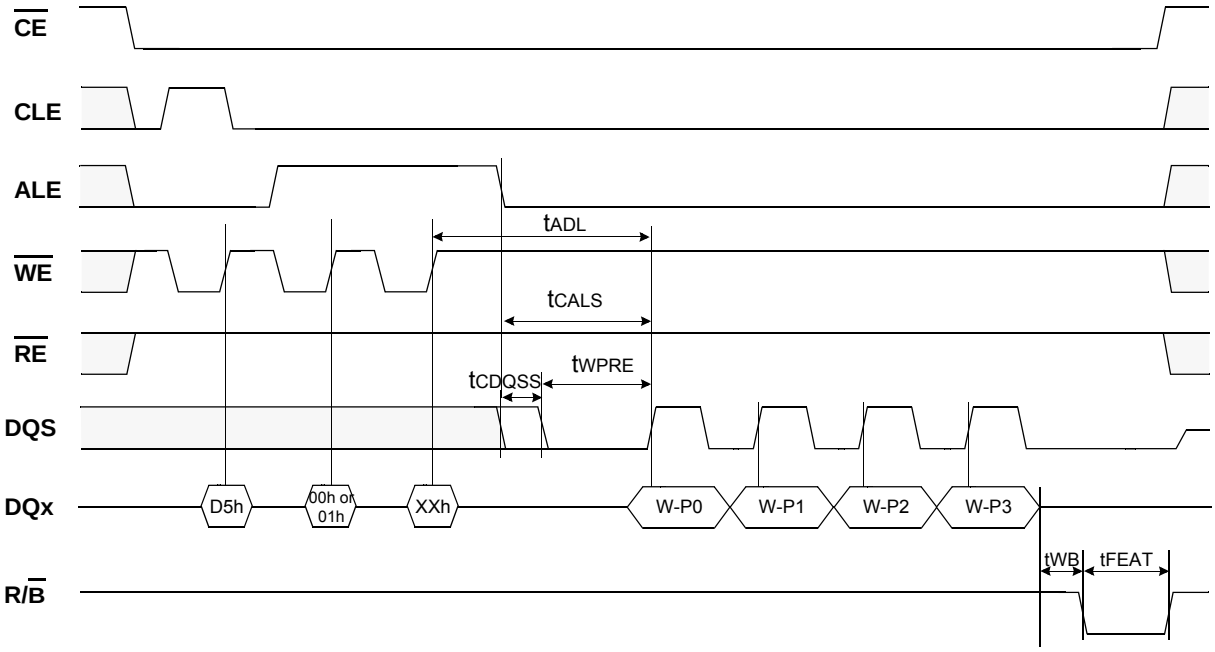


Figure 16. Set Feature(D5h) with LUN Control within 1CE Timing

4.3.8 Get Feature

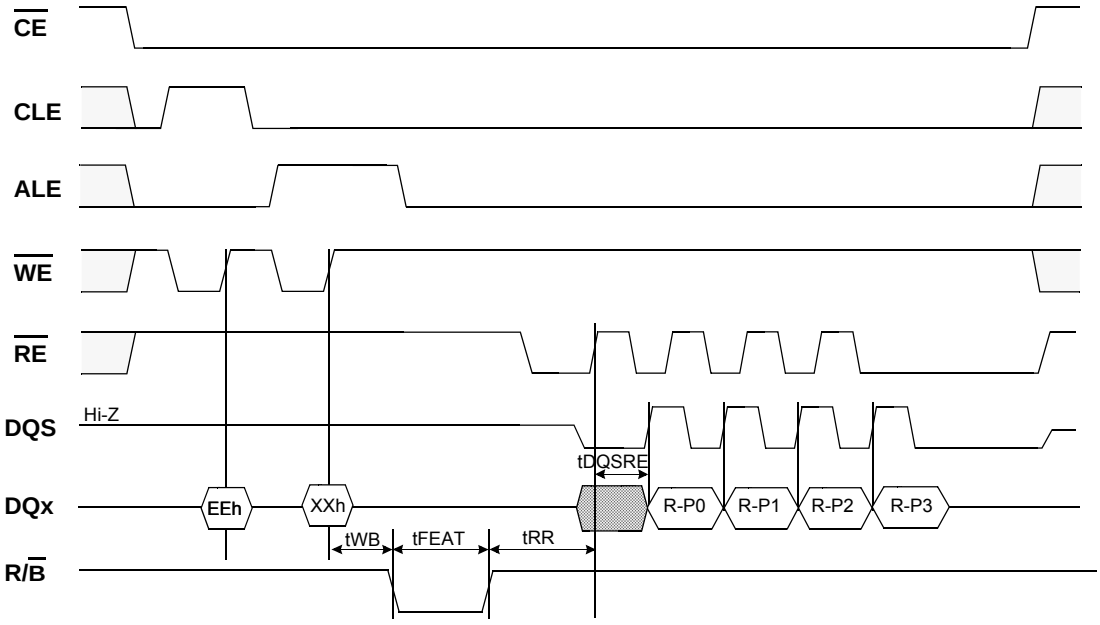


Figure 17. Get Feature(EEh) Timing

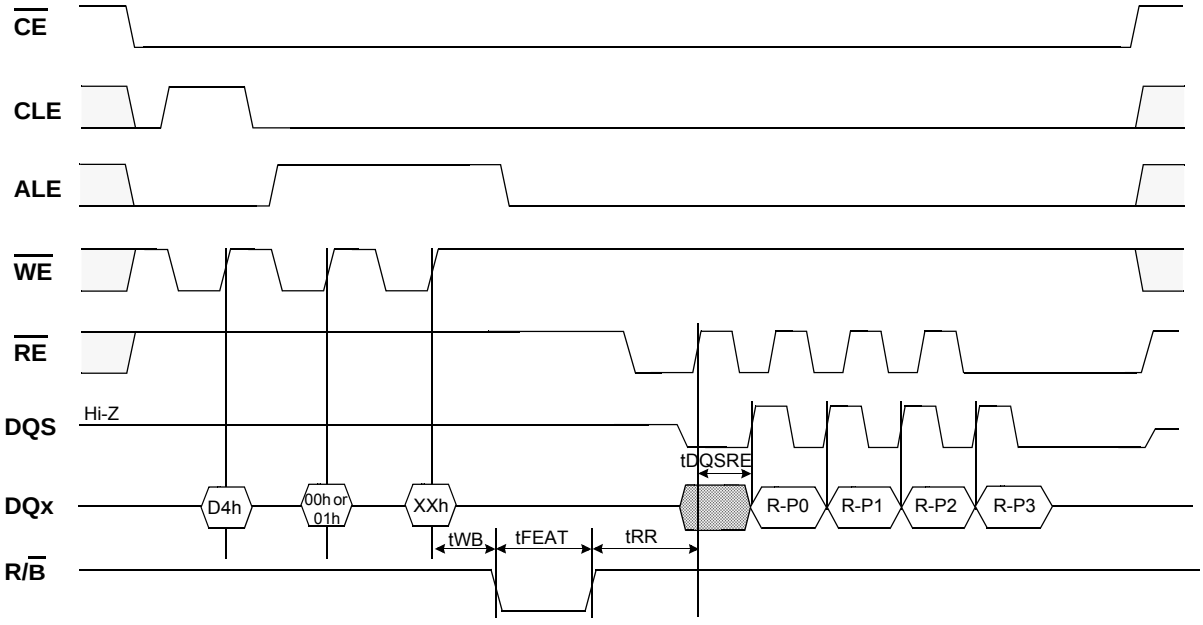
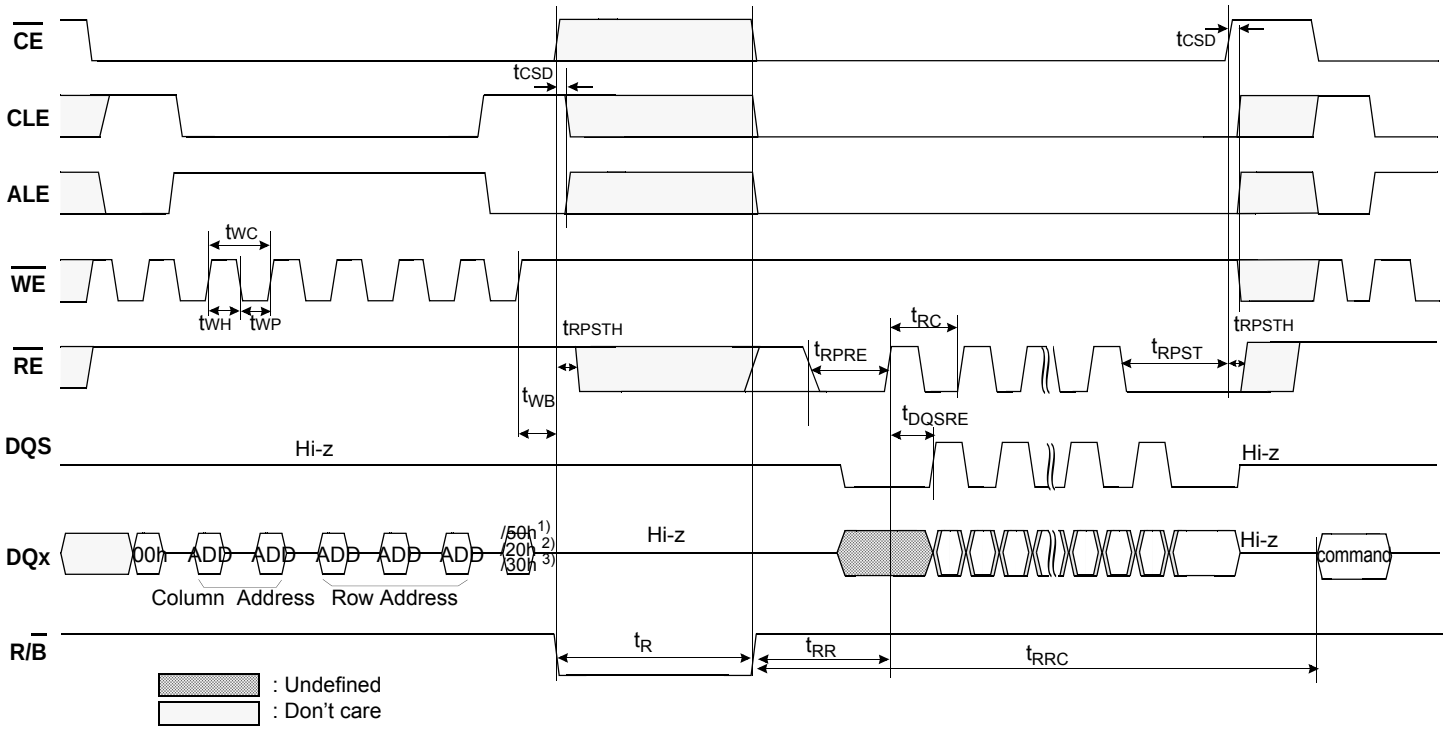


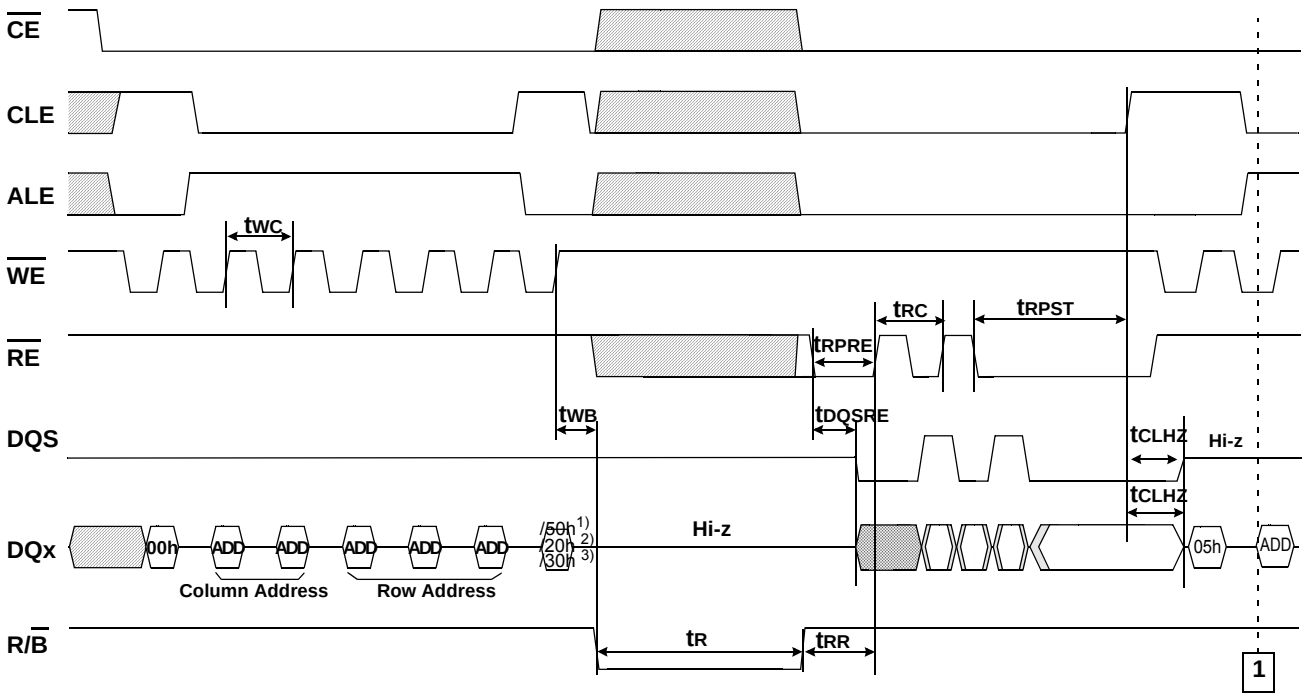
Figure 18. Get Feature(D4h) with LUN Control within 1$\overline{CE}$ Timing

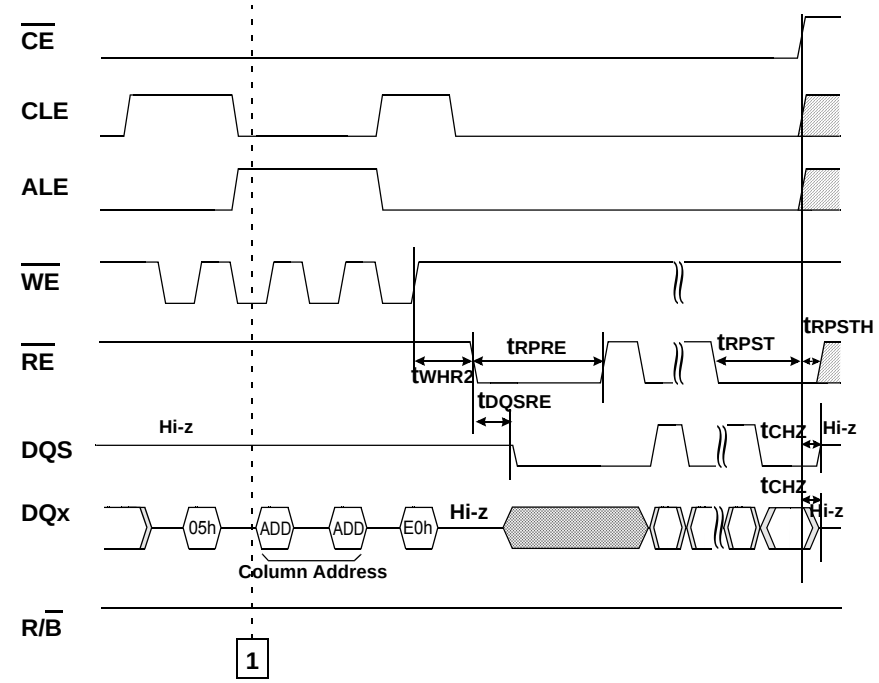
4.3.9 Page Read Operation : 4KB/8KB/16KB



NOTE :
1) 4KB Read Command.
2) 8KB Read Command.
3) 16KB Read Command.
4) $\overline{CE}$ is once deasserted, it shall stay high over at least 35ns before it is asserted again.

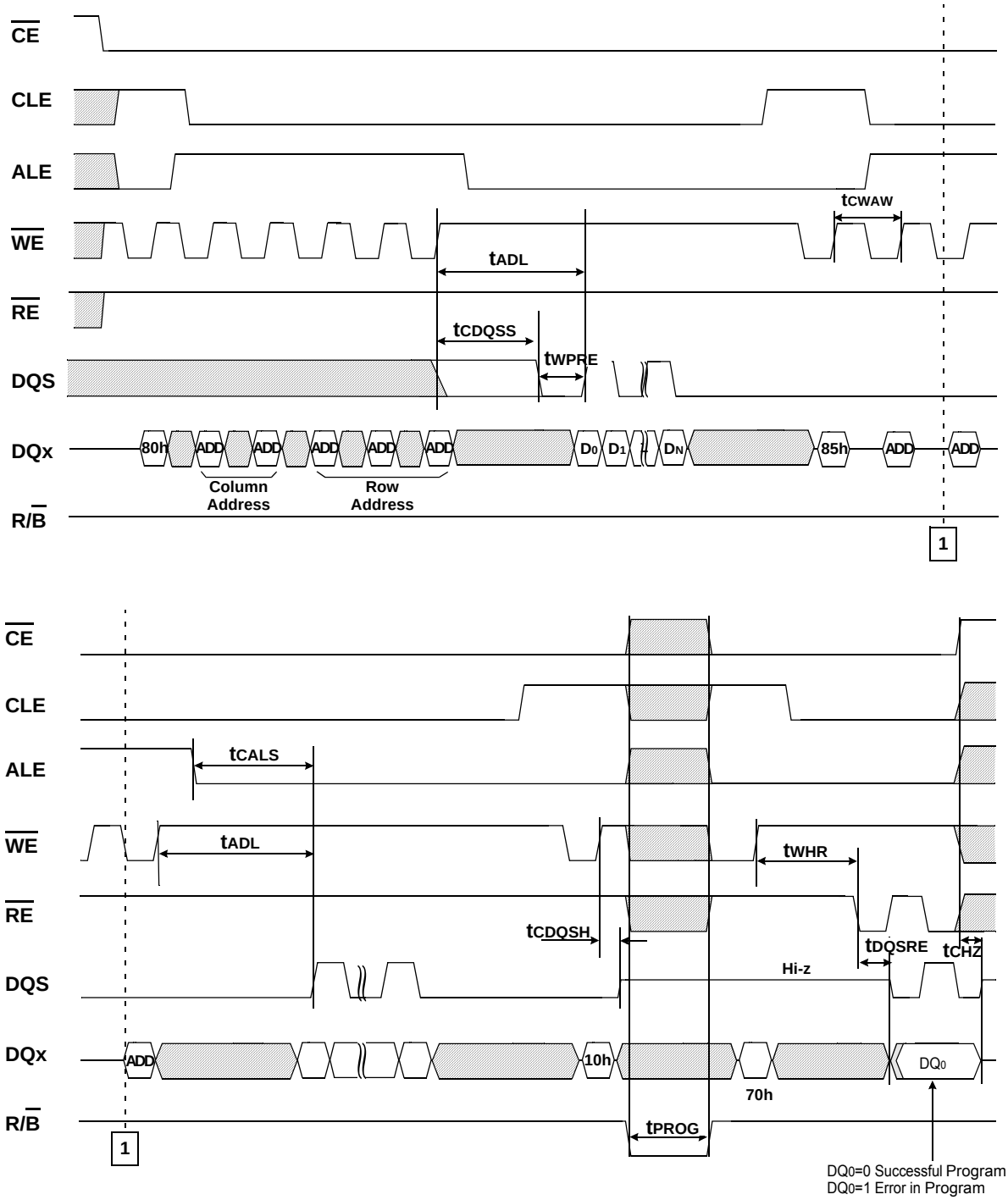
4.3.10 Page Read Operation with Random Data Output Operation





: Undefined
: Don't care

4.3.11 Page Program Operation with Random Data Input Operation



4.4 AC Test Condition

[Table 26] AC Test Condition

Parameter	K9AFGD8H0A
Input Pulse Levels	V_{IL} to V_{IH}
Input Rise and Fall Times	1.0V/ns
Input and Output Timing Levels	$V_{CC}Q/2$
Output Load	C_L = 5pF

4.5 AC Timing Characteristics

4.5.1 Timing Parameters Description

[Table 27] Toggle DDR Timing Parameters Description

Parameter	Description
tR	Data Transfer from Flash array to Register
tPROG	Program Time
tBERS	Erase Time
tADL	Address to Data Loading Time
tAR	ALE Low to $\overline{RE}$ Low
tCALH	CLE/ALE Hold Time
tCALS	CLE/ALE Setup Time
tCAH	Command/Address Hold Time
tCAS	Command/Address Setup Time
tCH	$\overline{CE}$ Hold Time
tCDQSH	DQS Hold Time for data input finish
tCDQSS	DQS Setup Time for data input start
tCHZ	$\overline{CE}$ High to Output Hi-Z
tCLHZ	CLE High to Output Hi-Z
tCLR	CLE to $\overline{RE}$ Low
tCOH	Data Hold Time after $\overline{CE}$ disable
tCR	$\overline{CE}$ Low to $\overline{RE}$ Low
tCRES	$\overline{RE}$ Set up Time
tCS	$\overline{CE}$ Setup Time
tCSD	$\overline{CE}$ Disable to signal (CLE, ALE, $\overline{WE}$) don't care
tCWAW	Command Write Cycle to Address Write Cycle Time for Random Data Input and Register Read Out mode
tDH	Data Hold Time
tDQSH	DQS Input High Pulse Width
tDQSL	DQS Input Low Pulse Width
tDQSQ	Output skew among data output and corresponding DQS
tDQSRE	$\overline{RE}$ to DQS and DQ delay
tDSC	Data Strobe Cycle Time
tDS	Data Setup Time
tDVW	Output data valid window
tFEAT	Busy time for Set Feature and Get Feature
tQH	Output hold time from DQS
tQHS	DQS hold skew factor
tRC	Read Cycle Time
tREH	$\overline{RE}$ High pulse width
tRP	$\overline{RE}$ Low pulse width
tRPP	$\overline{RE}$ Low width for Read Status at power-up
tRPRE	Read Preamble
tRPST	Read Postamble
tRPSTH	Read Postamble Hold Time

Parameter	Description
tRR	Ready to $\overline{RE}$ High
tRST	Device Resetting Time(Read/Program/Erase)
tWB	$\overline{WE}$ High to Busy
tWC	Write Cycle Time
tWH	$\overline{WE}$ High pulse width
tWHR	$\overline{WE}$ High to $\overline{RE}$ Low
tWHR2	$\overline{WE}$ High to $\overline{RE}$ Low for Random data out
tWP	$\overline{WE}$ Low pulse Width
tWPRE	Write Preamble
tWPST	Write Postamble
tWPSTH	Write Postamble Hold Time
tWW	$\overline{WP}$ High/Low to $\overline{WE}$ low
tDBSY	Dummy Busy Time for Two-Plane Program
tDBSY2	Dummy Busy Time for Data setup
tCBSY	Dummy Busy Time for Cache Program
tDCBSYR	Cache Busy in Cache Read
tRRC	Time from Read Ready to new Command (refer to Table 30/Table 52)
tDBSY3	Dummy Busy Time for Data Out

4.5.2 Timing Parameters Table

[Table 28] AC Timing Characteristics

Parameter	Symbol		100Mhz		133Mhz		166Mhz		200Mhz		266Mhz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Address to Data Loading Time	tADL		300	-	300	-	300	-	300	-	300	-	ns
ALE Low to $\overline{RE}$ Low	tAR		10	-	10	-	10	-	10	-	10	-	ns
CLE/ALE Hold Time	tCALH		5	-	5	-	5	-	5	-	5	-	ns
CLE/ALE Setup Time	tCALS		15	-	15	-	15	-	15	-	15	-	ns
Command/Address Hold Time	tCAH		5	-	5	-	5	-	5	-	5	-	ns
Command/Address Setup Time	tCAS		5	-	5	-	5	-	5	-	5	-	ns
DQS Hold Time for data input finish	tCDQSH		100	-	100	-	100	-	100	-	100	-	ns
DQS Setup Time for data input start	tCDQSS		100	-	100	-	100	-	100	-	100	-	ns
$\overline{CE}$ Hold Time	tCH		5	-	5	-	5	-	5	-	5	-	ns
$\overline{CE}$ High to Output Hi-Z	tCHZ		-	30	-	30	-	30	-	30	-	30	ns
CLE High to Output Hi-Z	tCLHZ		-	30	-	30	-	30	-	30	-	30	ns
CLE to $\overline{RE}$ Low	tCLR		10	-	10	-	10	-	10	-	10	-	ns
Data Hold Time after $\overline{CE}$ disable	tCOH		5	-	5	-	5	-	5	-	5	-	ns
$\overline{CE}$ Low to $\overline{RE}$ Low	tCR		10	-	10	-	10	-	10	-	10	-	ns
$\overline{RE}$ Set up time	tCRES		10	-	10	-	10	-	10	-	10	-	ns
$\overline{CE}$ Setup Time	tCS		25	-	25	-	25	-	25	-	25	-	ns
$\overline{CE}$ Disable to signal don't care	tCSD		10	-	10	-	10	-	10	-	10	-	ns
Command Write cycle to Address Write cycle Time for Random data input and Register Read Out mode	tCWAW		300	-	300	-	300	-	300	-	300	-	ns
Data Hold Time	tDH		0.9	-	0.75	-	0.55	-	0.4	-	0.4	-	ns
DQS Input High Pulse Width	tDQSH		0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	ns
DQS Input Low Pulse Width	tDQSL		0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	ns
Output skew among data output and corresponding DQS	tDQSQ		-	0.8	-	0.6	-	0.5	-	0.4	-	0.4	ns
$\overline{RE}$ to DQS and DQ delay	tDQSRE		5	25	5	25	5	25	5	25	5	25	ns
Data Strobe Cycle Time	tDSC		10	-	7.5	-	6	-	5	-	3.75	-	ns
Data Setup Time	tDS		0.9	-	0.75	-	0.55	-	0.4	-	0.4	-	ns
Output data valid window	tDVW		tDVW = tQH - tDQSQ										ns
Busy time for Set Feature and Get Feature	tFEAT		-	1	-	1	-	1	-	1	-	1	µs
Output hold time from DQS	tQH		tQH = min[tREH, tRP] - tQHS										ns
DQS hold skew factor	tQHS		-	0.8	-	0.6	-	0.5	-	0.4	-	0.4	ns
Read Cycle Time	tRC		10	-	7.5	-	6	-	5	-	3.75	-	ns
$\overline{RE}$ High pulse width	tREH		0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	ns
$\overline{RE}$ Low pulse width	tRP		0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	0.45* tRC	-	ns
$\overline{RE}$ Low width for Read Status at power-up	tRPP		30	-	30	-	30	-	30	-	30	-	ns
Read Preamble	tRPRE		15	-	15	-	15	-	15	-	15	-	ns
Read Postamble	tRPST		tDQSRE+ 0.5xtRC	-	tDQSRE+ 0.5xtRC	-	tDQSRE+ 0.5xtRC	-	tDQSRE+ 0.5xtRC	-	tDQSRE+ 0.5xtRC	-	ns
Read Postamble Hold Time	tRPSTH		25	-	25	-	25	-	25	-	25	-	ns
Ready to $\overline{RE}$ High	tRR		20	-	20	-	20	-	20	-	20	-	ns
Device Resetting Time (Read/Program/Erase)	tRST(1)		20 /30 /200										µs
Read Ready to New Command2)	tRRC	4KB /8KB /16KB	5	-	5	-	5	-	5	-	5	-	µs

Parameter	Symbol	100Mhz		133Mhz		166Mhz		200Mhz		266Mhz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$\overline{WE}$ High to Busy	tWB	-	100	-	100	-	100	-	100	-	100	ns
Write Cycle Time	tWC	25	-	25	-	25	-	25	-	25	-	ns
$\overline{WE}$ High pulse width	tWH	11	-	11	-	11	-	11	-	11	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	tWHR	120	-	120	-	120	-	120	-	120	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low for Random data out	tWHR2	300	-	300	-	300	-	300	-	300	-	ns
$\overline{WE}$ Low pulse Width	tWP	11	-	11	-	11	-	11	-	11	-	ns
Write Preamble	tWPRE	15	-	15	-	15	-	15	-	15	-	ns
Write Postamble	tWPST	6.5	-	6.5	-	6.5	-	6.5	-	6.5	-	ns
Write Postamble Hold Time	tWPSTH	25	-	25	-	25	-	25	-	25	-	ns
$\overline{WP}$ High/Low to $\overline{WE}$ low	tWW	100	-	100	-	100	-	100	-	100	-	ns
Write Postamble Hold Time	t_{WPSTH}	25	-	25	-	25	-	25	-	25	-	ns
$\overline{WP}$ High/Low to $\overline{WE}$ low	t_{WW}	100ns	-	100ns	-	100ns	-	100ns	-	100ns	-	ns
Dummy busy Time for Set up	tDBSY2	-	10	-	10	-	10	-	10	-	10	µs
Dummy busy Time for Data Out	tDBSY3	-	10	-	10	-	10	-	10	-	10	µs
Initial ZQ calibration	t_{ZQCL}	-	-	-	-	-	-	-	1	-	1	µs
Run-time ZQ calibration	t_{ZQCS}	-	-	-	-	-	-	-	0.3	-	0.3	µs

NOTE :
1) If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 10us.
2) Refer to Table 30/Table 52.

4.5.3 Read / Program / Erase Characteristics

[Table 29] NAND Read/Program/Erase Characteristics

Parameter	Symbol		Min	Typ	Max	Unit
Data Transfer from Flash array to Register	tR	4KB	-	65	-	µs
		8KB	-	65	-	
		16KB	-	65	-	
Program Time	tPROG		-	1.2	-	ms
Dummy Busy Time for Two-Plane setting	tDBSY			0.5	1	µs
Dummy Busy Time for Cache Program	tCBSY		-	-	tPROG	ms
Cache Busy in Cache Read	t_{DCBSYR}	4KB	-	-	tR	µs
		8KB	-	-	tR	µs
		16KB	-	-	tR	µs
Number of Partial Program Cycles in the Same Page	Nop		-	-	1	cycle
Block Erase Time	tBERS		-	5	20	ms

NOTE :
1) Typical program time is measured at V_{CC}=3.3V, T_A=25°C. Not 100% tested.
2) Typical program time is defined as the time within which more than 50% of the whole pages are programed at 3.3V V_{CC} and 25°C temperature.
3) tCBSY depends on the timing between internal programming time and data in time.

5.0 COMMAND DESCRIPTION AND DEVICE OPERATION

5.1 Basic Command Sets

Toggle DDR NAND Flash Memory has addresses multiplexed into 8 I/Os. Command, address and data is all written through DQ[7:0] by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the DQ[7:0] pins. Commands which apply to a specific page or block typically have a second command and ones that apply to a target or a LUN have a first command only.

Table 30 below defines the basic command sets.

[Table 30] Basic Command Sets

Mode	Function	Primary	1st Set	Address Cycles	2nd Set	Acceptable while Accessed LUN is Busy
Common	4KB Read	Primary	00h	5	50h	
	8KB Read	Primary	00h	5	20h	
	16KB Read	Primary	00h	5	30h	
	16KB Sequential Cache Read	-	31h	-	-	
	Read start for last Page Random 4KB cache		5Fh	-	-	
	Read start for last Page Random 8KB cache		2Fh	-	-	
	Read start for last Page Random 16KB cache	-	3Fh	-	-	
	4KB Random Cache Read	-	00h	5[4)]	51h	
	8KB Random Cache Read	-	00h	5[4)]	21h	
	16KB Random Cache Read	-	00h	5[4)]	31h	
	Read for Copy-Back	Primary	00h	5[4)]	35h	
	Block Erase	Primary	60h	3	D0h	
	Random Data Input [1)]	Primary	85h	2	-	
	Random Data Output [2)]	Primary	05h	2	E0h	
	Set Feature - Common	Primary	EFh	1	-	
	Get Feature - Common	Primary	EEh	1	-	
	Read ID	Primary	90h	1	-	
	Read Status [2)]	Primary	70h	-	-	Y
	Reset [2)]	Primary	FFh	-	-	Y
	Reset LUN[3)]	-	FAh	3	-	Y
	Set Feature LUN Control with in1$\overline{CE}$	-	D5h	2	-	-
	Get Feature LUN Control with in1$\overline{CE}$	-	D4h	2	-	-
TLC	Program Data In	Primary	80h	5[4)]	-	
	Latch Dump for Data In	-	C0h	1	-	
	Program Confirm	-	8Bh	5[4)]	10h	
	Copy-Back Program Data In	Primary	85h	5[4)]	-	
	Cache Program Confirm	-	8Bh	5[4)]	15h	
SLC	16KB Program[5)]	Primary	80h	5[4)]	10h	
	16KB Read	Primary	00h	5[4)]	30h	
	Copy-Back Program[5)]	Primary	85h	5[4)]	10h	
	SLC Mode Access	-	DAh	-	-	
	SLC Mode Abort	-	DFh	-	-	
	Cache Program Confirm[5)]	-	80h	5[4)]	15h	

NOTE :
1) Random Data Input/Output can be executed in a page.
Random Data input size has to be at least over 1KB.
2) Commands in are only allowable in tRRC.
3) To minimize peak current during initialization, each LUN in a target can be selectively initialized by FAh(Reset LUN) command.
4) SLC Mode must be applied to Table 24.
TLC Mode must be applied to Table 22/Table 23.
5) Page Program/Cache Program/Copy-back Program must be executed at SLC mode.
6) TLC mode program command input (8Bh) is not allowed after SLC mode access.

Caution :
Any undefined command inputs are prohibited except for above command set.

5.2 Basic Operation

5.2.1 Page Read Operation

The Page Read function reads a page of data identified by row address for the selected LUN. The page of data is made available to be read from the page register starting at the specified column address. Figure 19 defines the Page Read behavior and timings. Reading beyond the end of a page results in indeterminate values being returned to the host.

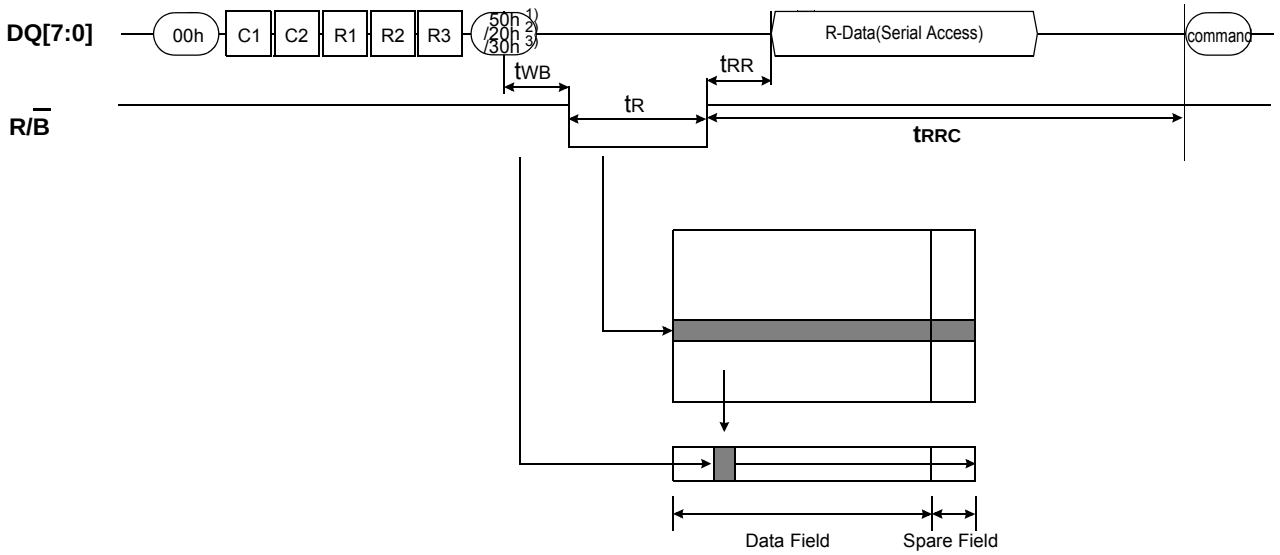


Figure 19. 4KB/ 8KB/ 16KB Page Read Sequence

NOTE :
1) 4KB Read Command.
2) 8KB Read Command.
3) 16KB Read Command.

5.2.1.1 Fast 4KB Read

The Fast 4KB Read function transfers (i.e.4KB+512B) data in NAND array to page register. This function helps applications maximize random read or write throughput. Since Fast 4KB Read function transfers 1/4 page, to transfer other side of the page data, another Fast 4KB Read operations are required.

Target 4KB data shall be determined by latched address between 00h and 50h command. When the address between 0000h and 11FFh is set, the first 4KB data shall be transferred and when the address between 1200h and 23FFh is set, the second 4KB data shall be transferred. Figure 20 represents the page layout when Fast 4KB Read is used.

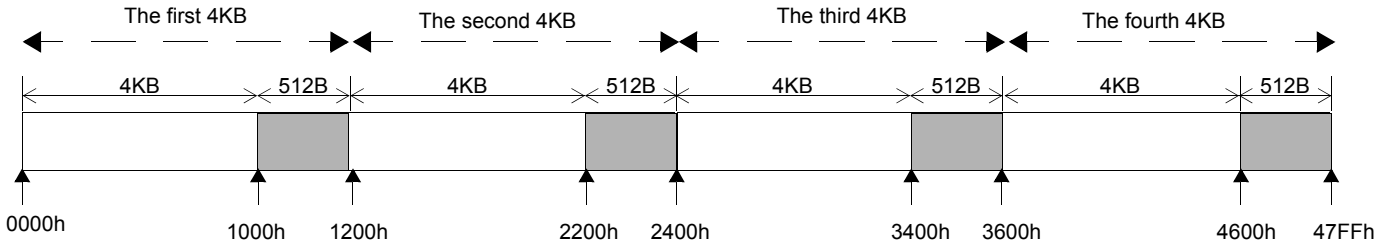


Figure 20. Page Layout for Fast 4KB Read

5.2.1.2 Fast 8KB Read

The Fast 8KB Read function transfers (i.e. 8KB+1024B) data in NAND array to page register. This function helps applications maximize random read or write throughput. Since Fast 8KB Read function transfers 1/2 page, to transfer other side of the page data, another Fast 8KB Read operations are required.

Target 8KB data shall be determined by latched address between 00h and 20h command. When the address between 0000h and 23FFh is set, the first 8KB data shall be transferred and when the address between 2400h and 47FFh is set, the second 8KB data shall be transferred. Figure 21 represents the page layout when Fast 8KB Read is used.

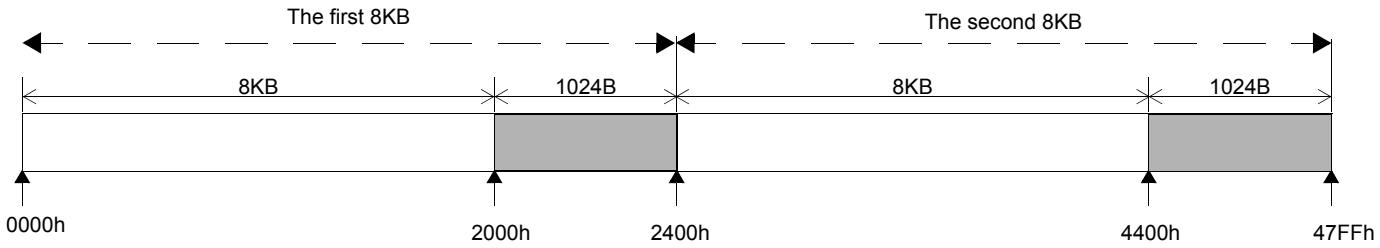


Figure 21. Page Layout for Fast 8KB Read

5.2.1.3 Page Read Operation with Random Data Output Operation

The Random Data Output function changes the column address from which data is being read in the page register for the selected LUN. The Random Data Output command shall only be issued when the LUN is in a read idle condition. Figure 22 defines the Random Data Output behavior and timings. The host shall not read data from the LUN until tWHR2(ns) after the second command (i.e. E0h) is written to the LUN.

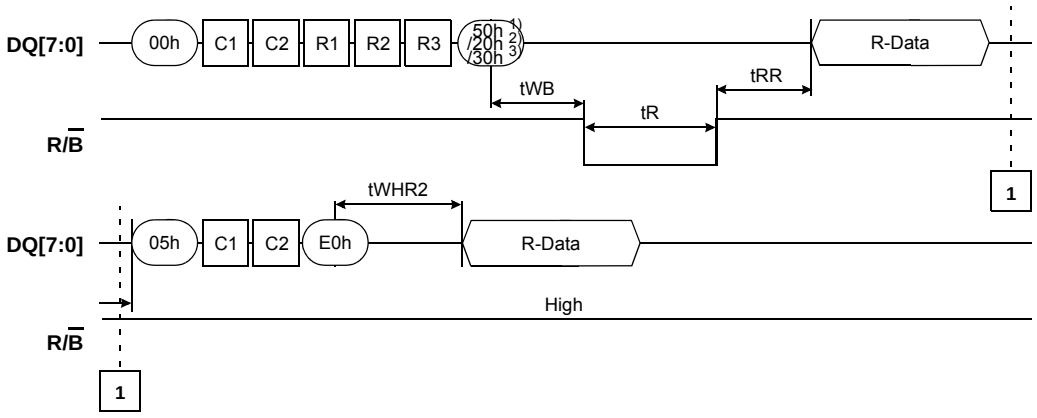


Figure 22. 4KB/8KB/16KB Page Read with Random Data Output Sequence

NOTE :
1) 4KB Read Command.
2) 8KB Read Command.
3) 16KB Read Command.

5.2.1.4 Data Out after Read Status Operation

While monitoring the read status to determine when the tR (transfer from Flash array to a page register) is complete, the host shall re-issue the 00h command to start reading data. Issuing the 00h command will cause data to be returned starting at the selected column address.

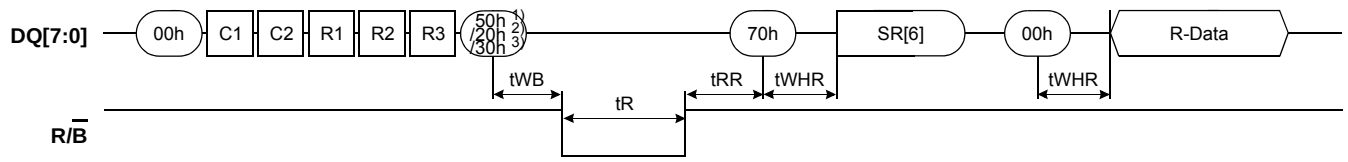


Figure 23. Data Out After 4/8/16KB Read Status Sequence

NOTE :
1) 4KB Read Command.
2) 8KB Read Command.
3) 16KB Read Command.

5.2.2 Latch Dump for Data In Operation

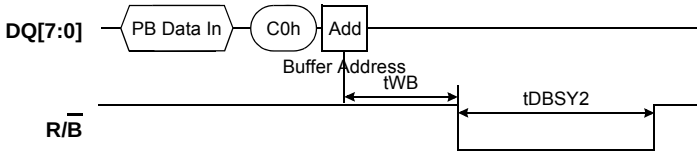


Figure 24. Dump Up (C0h)

5.2.3 16KB Sequential Cache Read Operation

The Sequential Cache Read offers loading page ahead operation, that is a page to be loaded from the Flash array while already loaded page is read by a host. A Read Page command shall be issued prior to the initial Sequential Cache Read command in a cache read sequence. A Sequential Cache Read command (i.e. 31h) shall be issued until the Sequential Cache Read Operation is completed by the Read Start for Last Page Cache Read command(i.e. 3Fh).

The Sequential Cache Read command may be issued after the Read function is complete (i.e. SR[6] is set to one). Data output always begins at column address 00h. When the Sequential Cache Read command(i.e. 31h) is issued, SR[6] is cleared to zero (i.e. busy). After the operation finishes, SR[6] turns to one (i.e. ready) and the host may begin to read the data loaded by the previous Sequential Cache Read operation. The data loaded by a Sequential Cache Read command from Flash array to a page register is copied to a cache register by a following Sequential Cache Read command. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS or READ STATUS ENHANCED table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Sequential Cache Read operation except RESET and READ STATUS commands are prohibited. And the data of a final page loaded onto a page register is transferred to a cache register by 3Fh command. The host shall not issue a Sequential Cache Read command(31h) after the last page of a block is read.

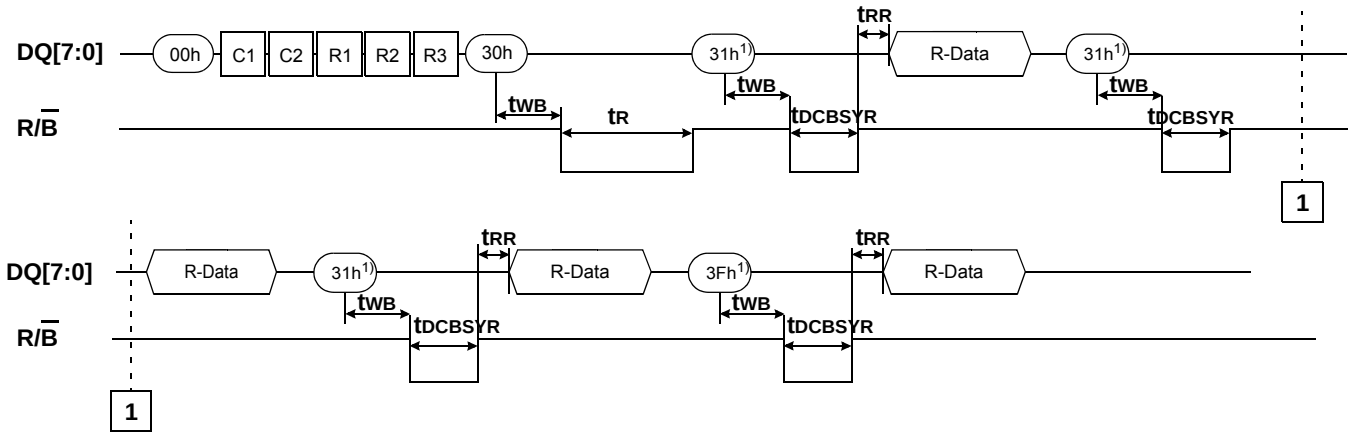


Figure 25. 16KB Sequential Cache Read Sequence

NOTE :
1) 16KB Read Command.

5.2.4 Random Cache Read(4KB/8KB/16KB) Operation

A Read Page command shall be issued prior to the initial Random Cache Read command in a cache read sequence like the Sequential Cache Read operation. Column address shall be fixed to 00h during 16KB Random Cache Read operation(30h/31h). 5Fh(4KB)/2F(8KB)/3F(16KB) command is required to finish the sequence and read the final cached page. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS or READ STATUS ENHANCED table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Random Cache Read operation except RESET and READ STATUS commands are prohibited. The page and block address can be accessed in a random manner while the plane address shall stay the same. Figure 26 defines the Random Cache Read behavior and timings.

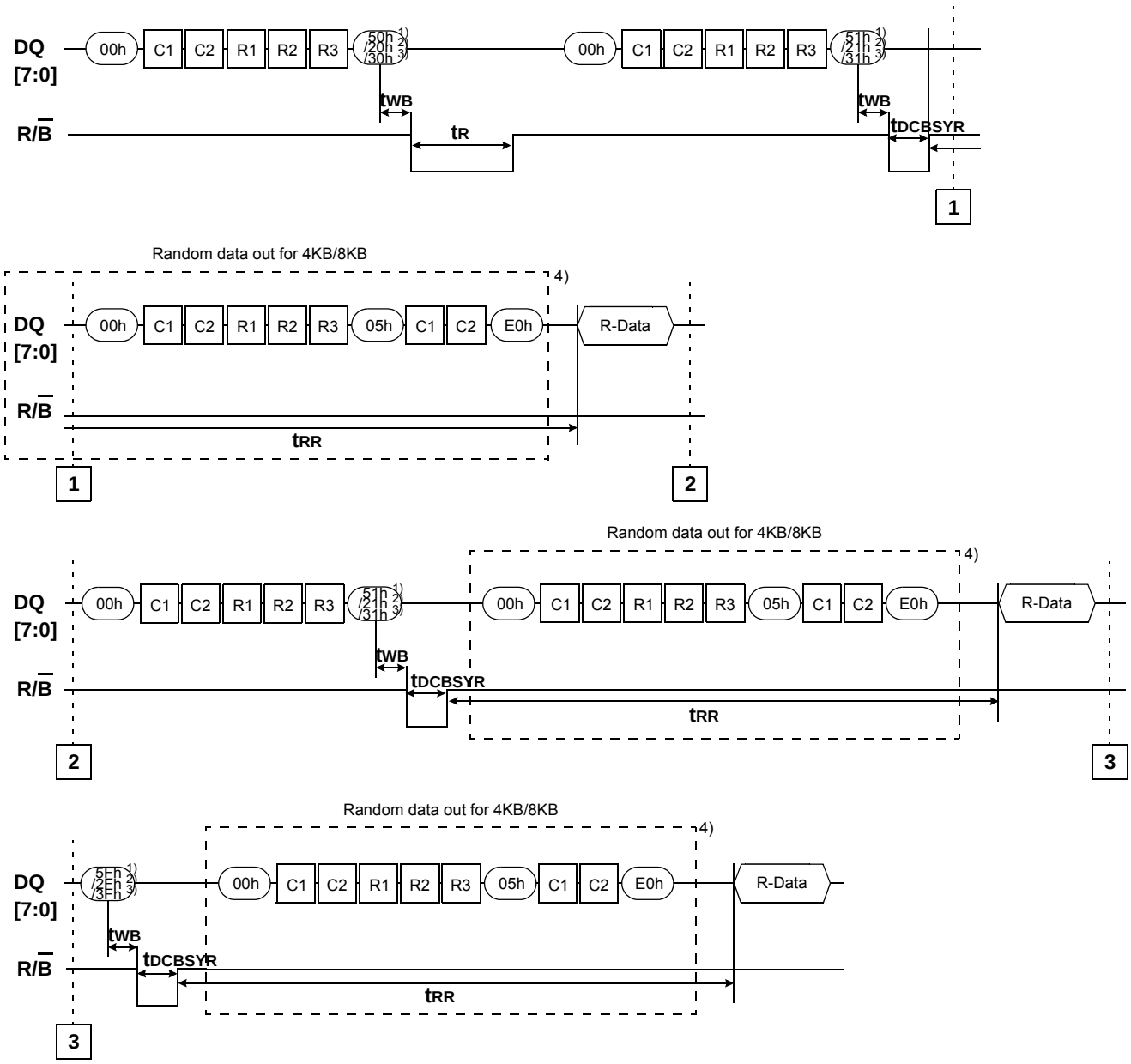


Figure 26. 4KB/8KB/16KB Random Cache Read Sequence

NOTE :
4KB/8KB Random Cache Read operation required the essential random data out.
1) 4KB random cache read command.
2) 8KB random cache read command.
3) 16KB random cache read command.
4) Must be applied to 4/8KB Random Cache Read.
The 4KB/8KB Random Cache Read is required to Random data-out.

5.2.5 Page Program Operation

The device is programmed basically on a page basis(48KB in TLC, 32KB in MLC, 16KB in SLC), and each page shall be programmed only once before being erased. The addressing order shall be sequential within a block. The contents of the page register are programmed into the Flash array specified by row address. SR[0] is valid for this command after SR[6] transitions from zero to one until the next transition of SR[6] to zero. Figure 27 defines the Page Program behavior and timings. Writing beyond the end of the page register is undefined.

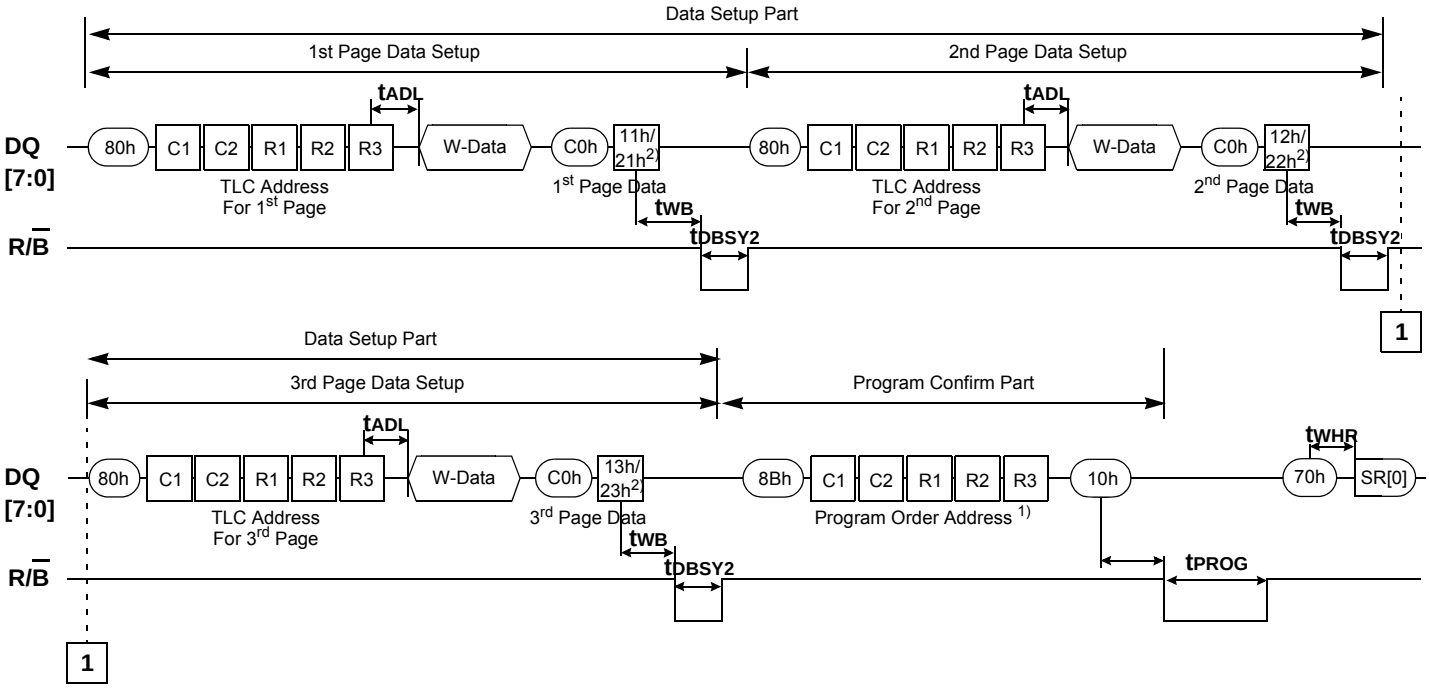


Figure 27. 48KB Page Program Operation (TLC)

NOTE :
1) The first Raw Address (R1) is required to refer Program order address in Table 22.
2) Refer to buffer address Table 31.

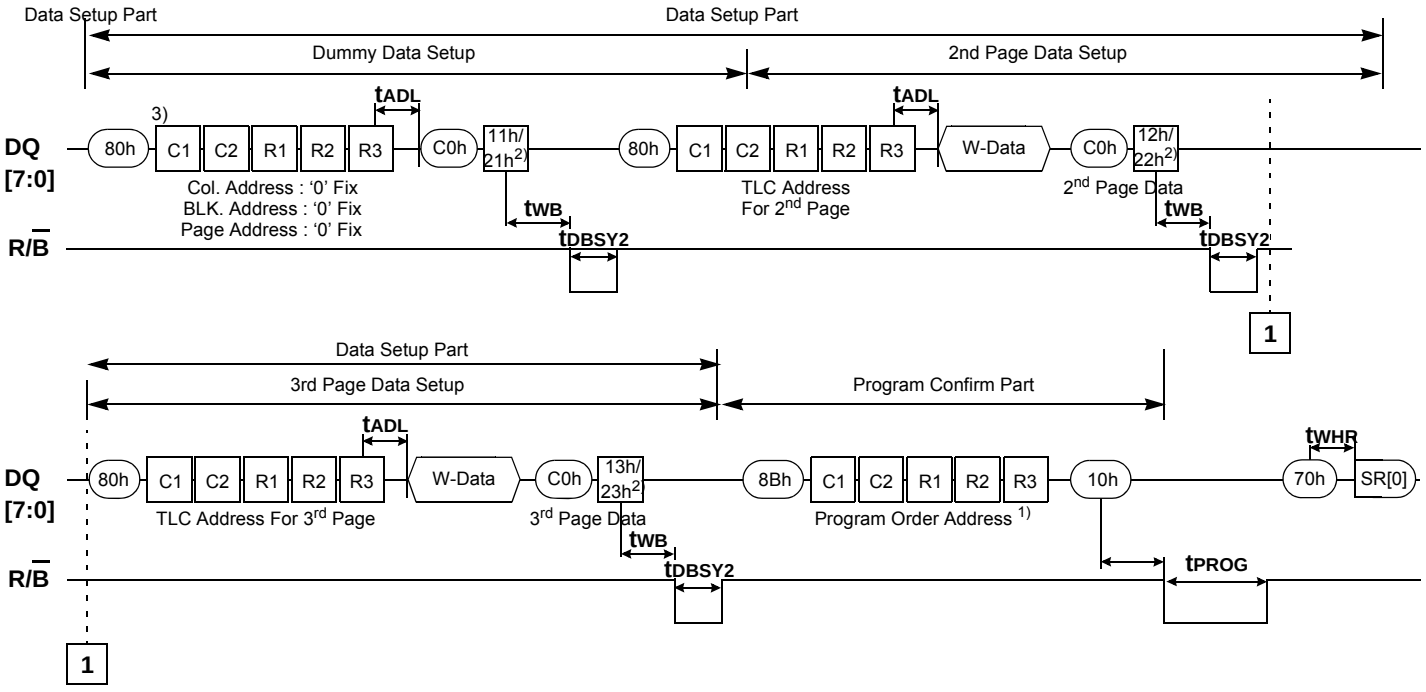


Figure 28. Page Program Operation (Edge MLC)

NOTE :
1) The first Raw Address (R1) is required to refer Program order address in Table 22.
2) Refer to buffer address Table 31.
3) No actual data loading (page address, block address, column address "0" fix in dummy data setup.

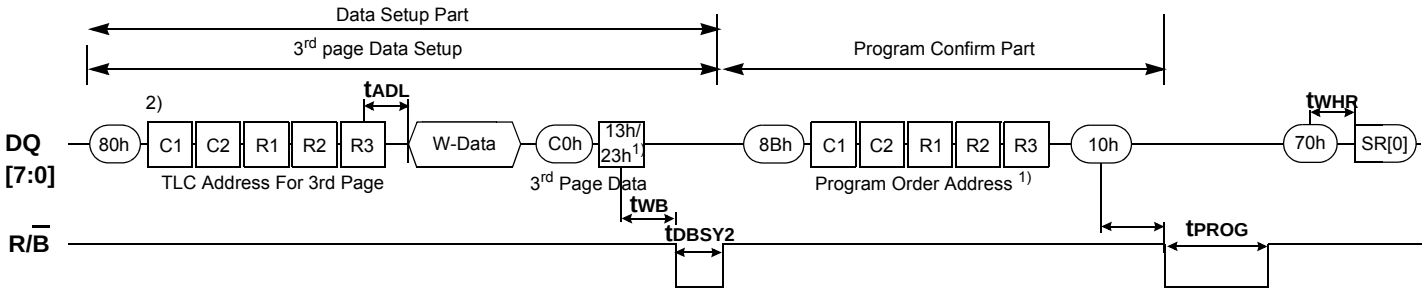


Figure 29. Page Program Operation (Edge SLC)

NOTE :
1) The first Raw Address (R1) is required to refer Program order address in Table 24.

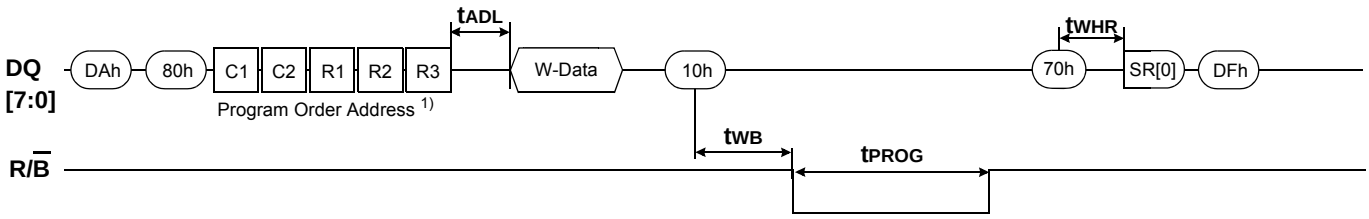


Figure 30. 16KB Page Program Operation (SLC)

NOTE :
1) The first Raw Address (R1) is required to refer Program order address in Table 24.

[Table 31] Buffer Address

	LSB	CSB	MSB
Plane0	11h	12h	13h
Plane1	21h	22h	23h
Plane0 & Plane1	31h	32h	33h

NOTE :
1) 3pages Data which are LSB, CSB and MSB has to be stored in each Program operation.
2) After C0h Command, buffer address is needed for definition of LSB or CSB or MSB page.
3) After 8Bh Command, 5 address cycles shall be inputted in sequence of the Program Order Address Information refer to Table 22.

5.2.5.1 Program Operation with Random Data Input Operation

The device supports random data input in a page. The column address for the next data, which will be written, may be changed to the address using Random data input command(i.e. 85h). Random data input may be operated multiple times without limitation.

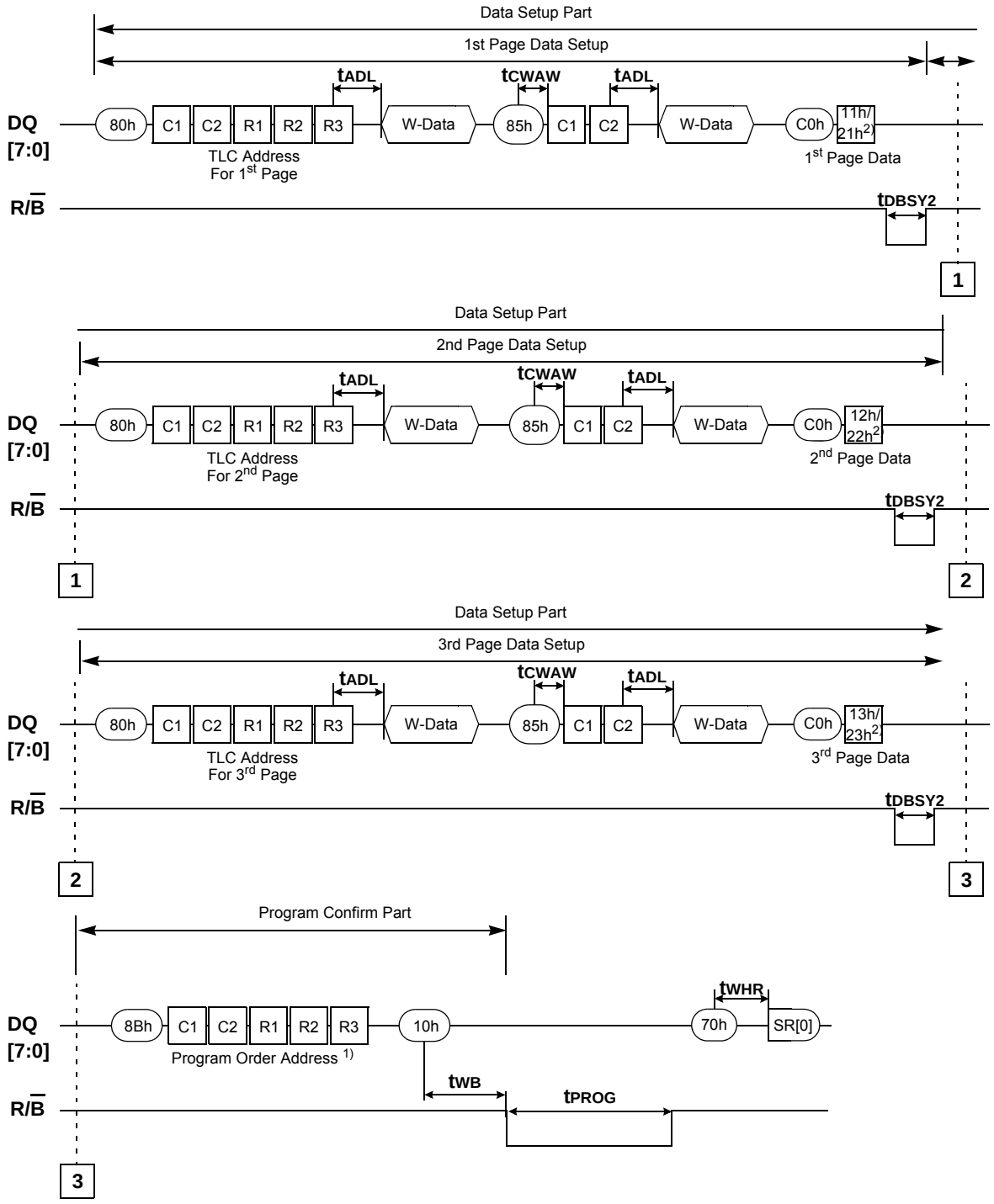


Figure 31. 48KB Program Operation with Random Data Input Sequence (TLC)

NOTE :
1) The first Raw Address (R1) is required to refer Program order address in Table 22.
2) Refer to buffer address Table 31.

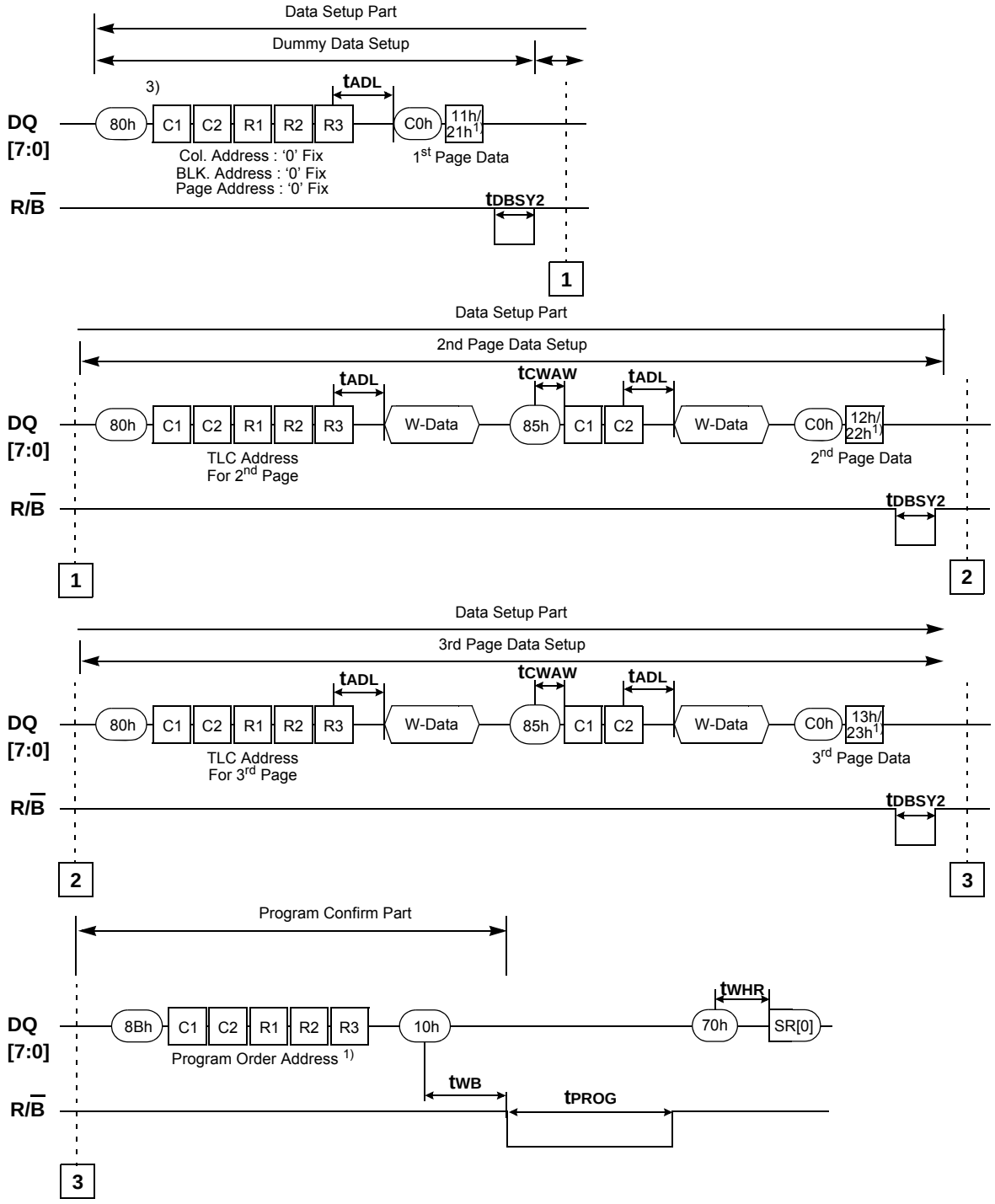


Figure 32. Program Operation with Random Data Input Sequence (Edge MLC)

NOTE :
1) The first Raw Address (R1) is required to refer Program order address in Table 22.
2) Refer to buffer address Table 31.
3) No actual data loading (page address, block address, column address "0" fix in dummy data setup.

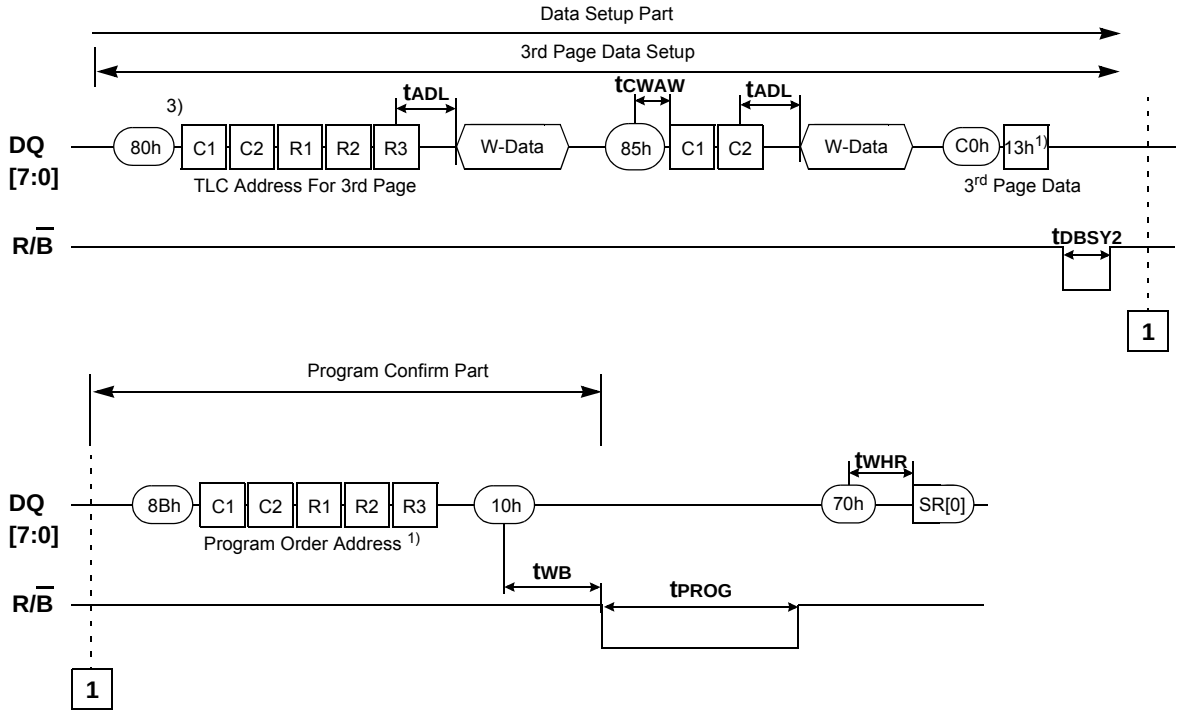


Figure 33. Program Operation with Random Data Input Sequence (Edge SLC)

NOTE :
1) The first Raw Address (R1) is required to refer Program order address in Table 24.
2) Refer to buffer address Table 31.

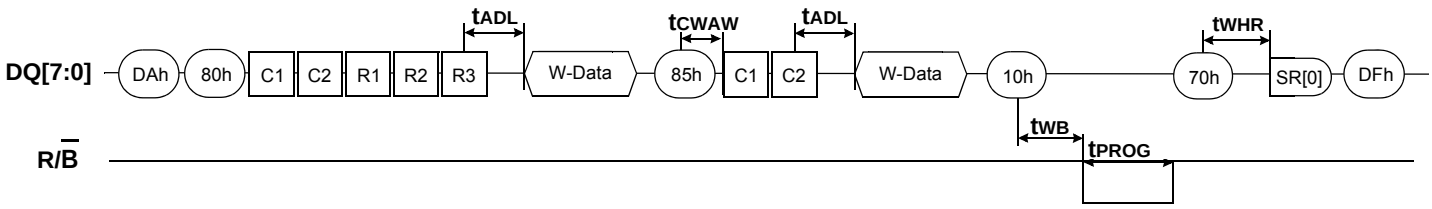


Figure 34. 16KB Program Operation with Random Data Input Sequence (SLC)

5.2.6 Copy-Back Program Operation

The Copy-Back Program with Read for Copy-Back is configured to efficiently rewrite data stored in a dual page without data re-loading when no error within the page is found. Since the time-consuming re-loading cycles are removed, copy-back operation helps the system performance improve. The benefit is especially obvious when a part of a block is updated and the rest of the block also needs to be copied to the newly assigned free block.
The Copy-Back operation consists of 'Read for Copy-Back' and 'Copy-Back Program'. A host reads a page of data from a source page using 'Read for Copy-Back' and copies read data back to a destination page on the same LUN by 'Copy-Back Program' command. Figure 35 defines the Copy-Back Program behavior and timings.

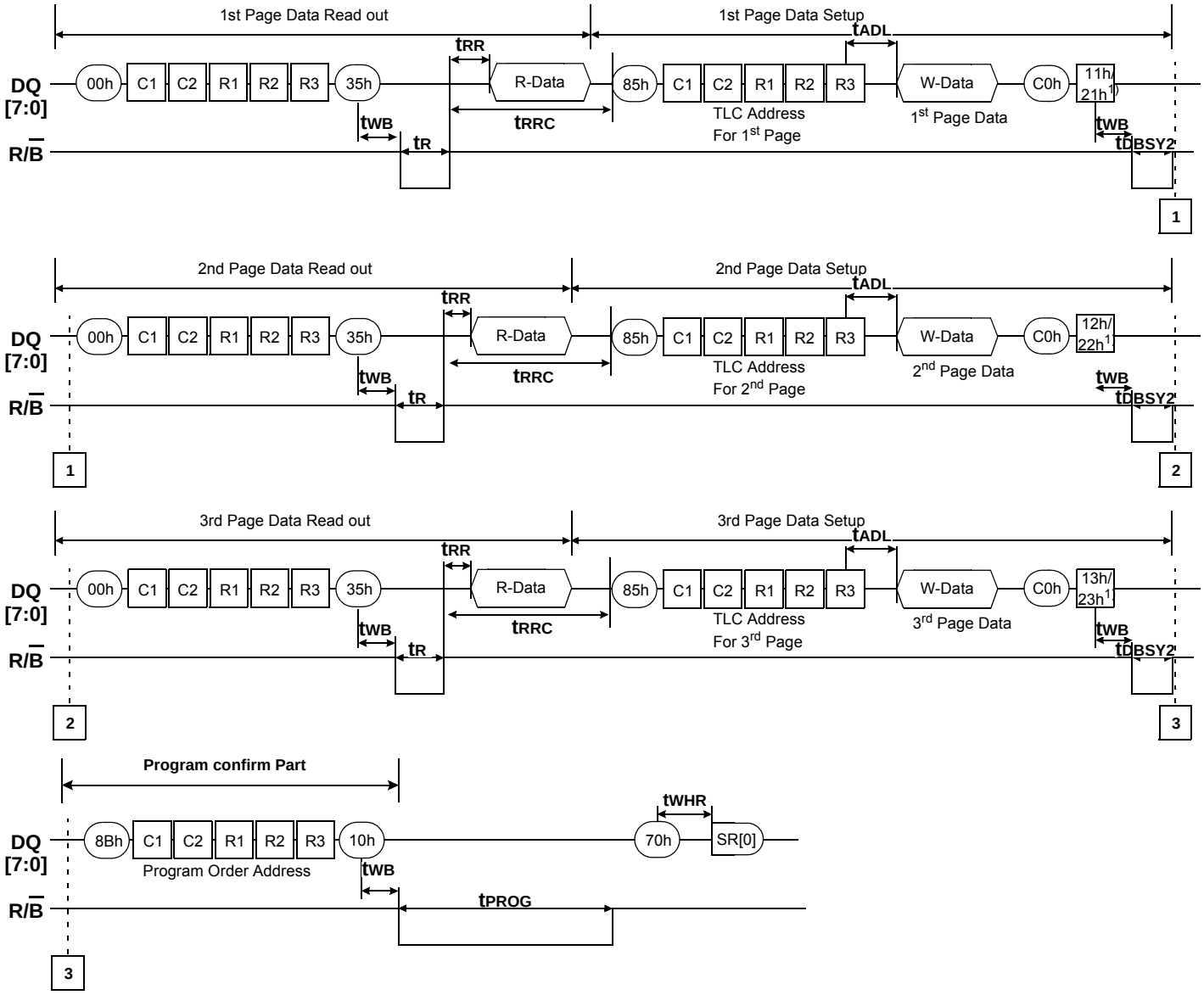


Figure 35. Copy-Back Program Sequence (TLC)

NOTE :
1) Refer to buffer address Table 31.

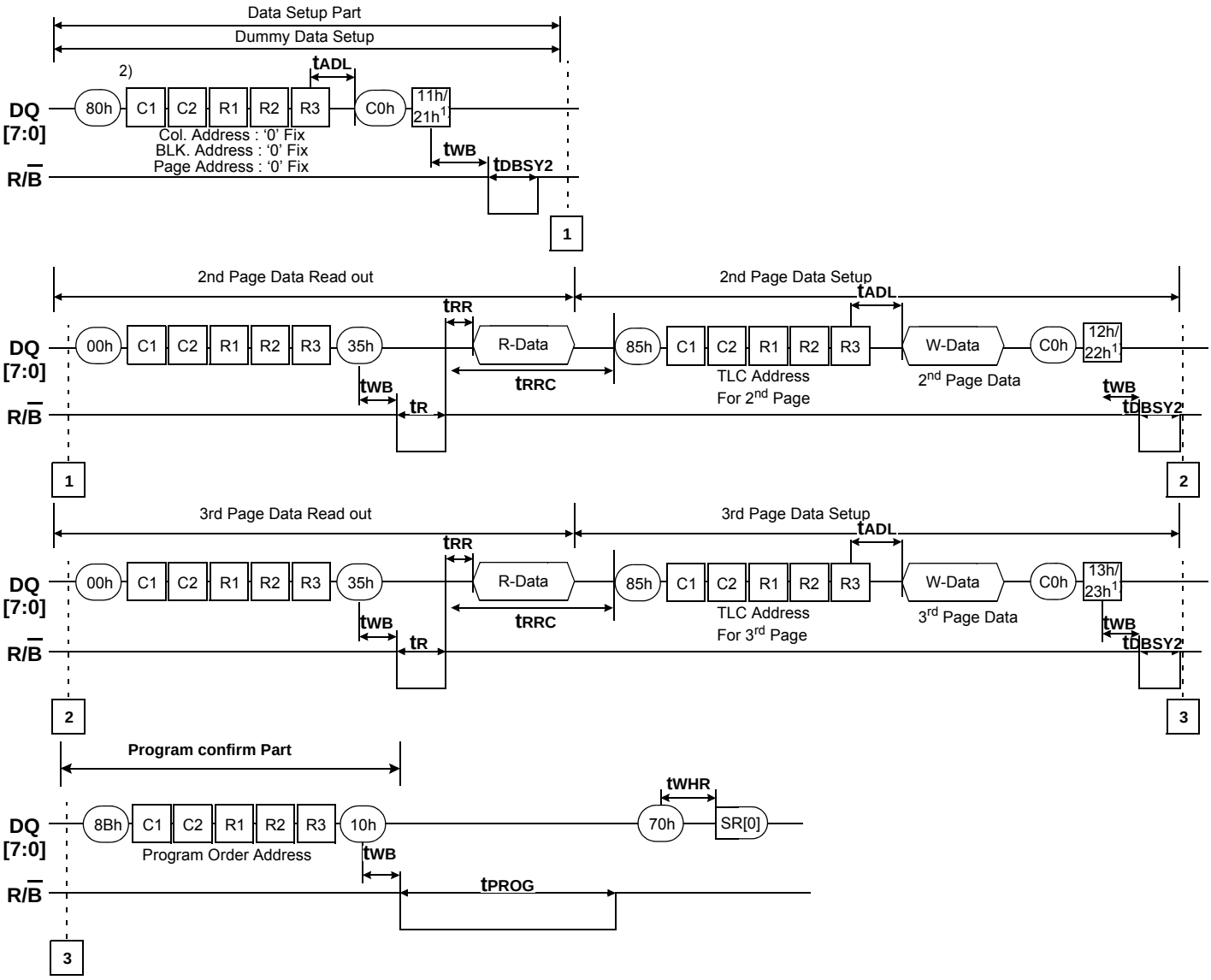


Figure 36. Copy-Back Program Sequence (Edge MLC)

NOTE :
1) Refer to buffer address Table 31.
2) No actual data loading (page address, block address, column address "0" fix in dummy data setup.

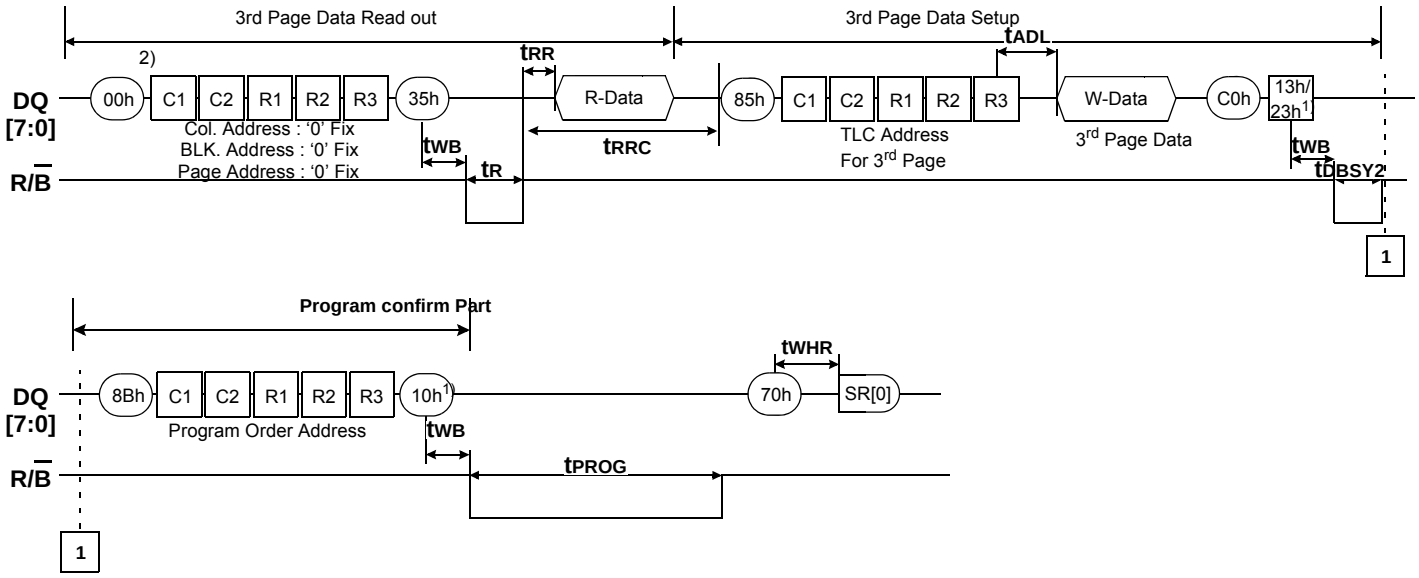


Figure 37. Copy-Back Program Sequence (Edge SLC)

NOTE :
1) Refer to buffer address Table 31.

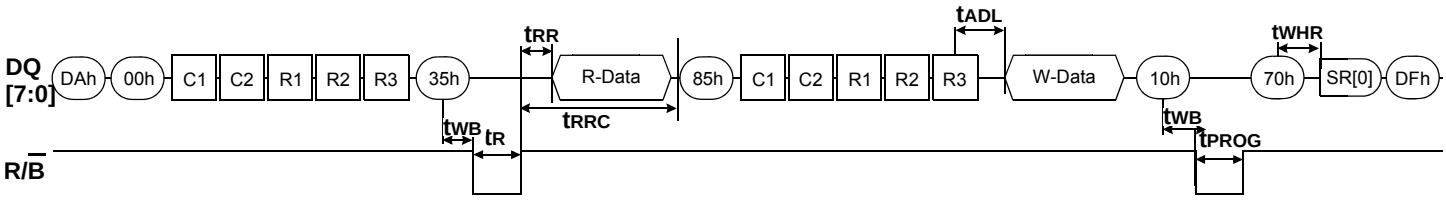


Figure 38. Copy-Back Program Sequence (SLC)

5.2.6.1 Copy-Back Program Operation with Random Data Input Operation

After a host completes to read data from a page register, the host may modify data using Random Data Input command if required. Figure 39 and Figure 42 define the Copy-Back Program with Random Data Input behavior and timings.

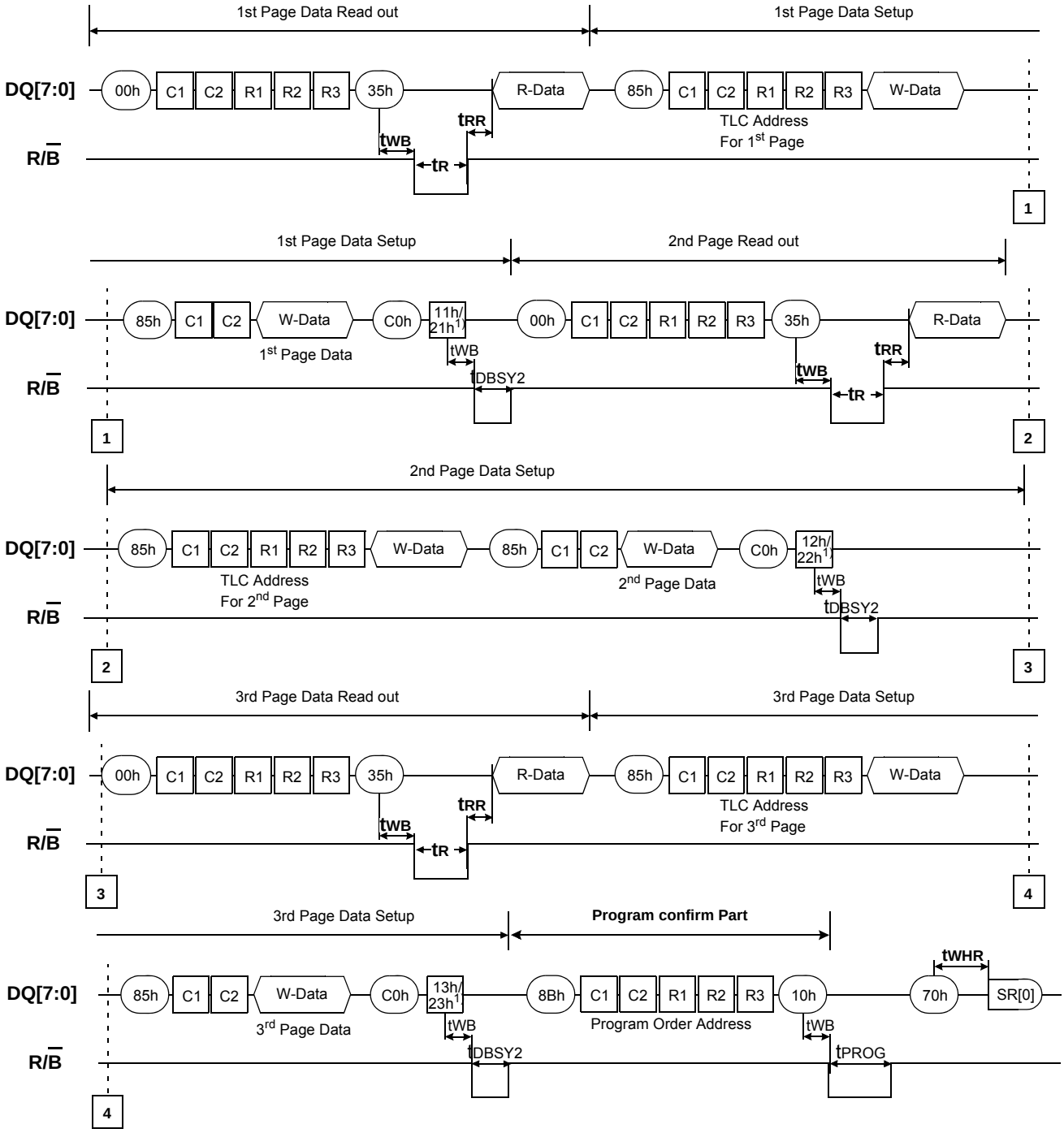


Figure 39. Copy-Back Program with Random Data Input Sequence (TLC)

NOTE :
1) Refer to buffer address Table 31.

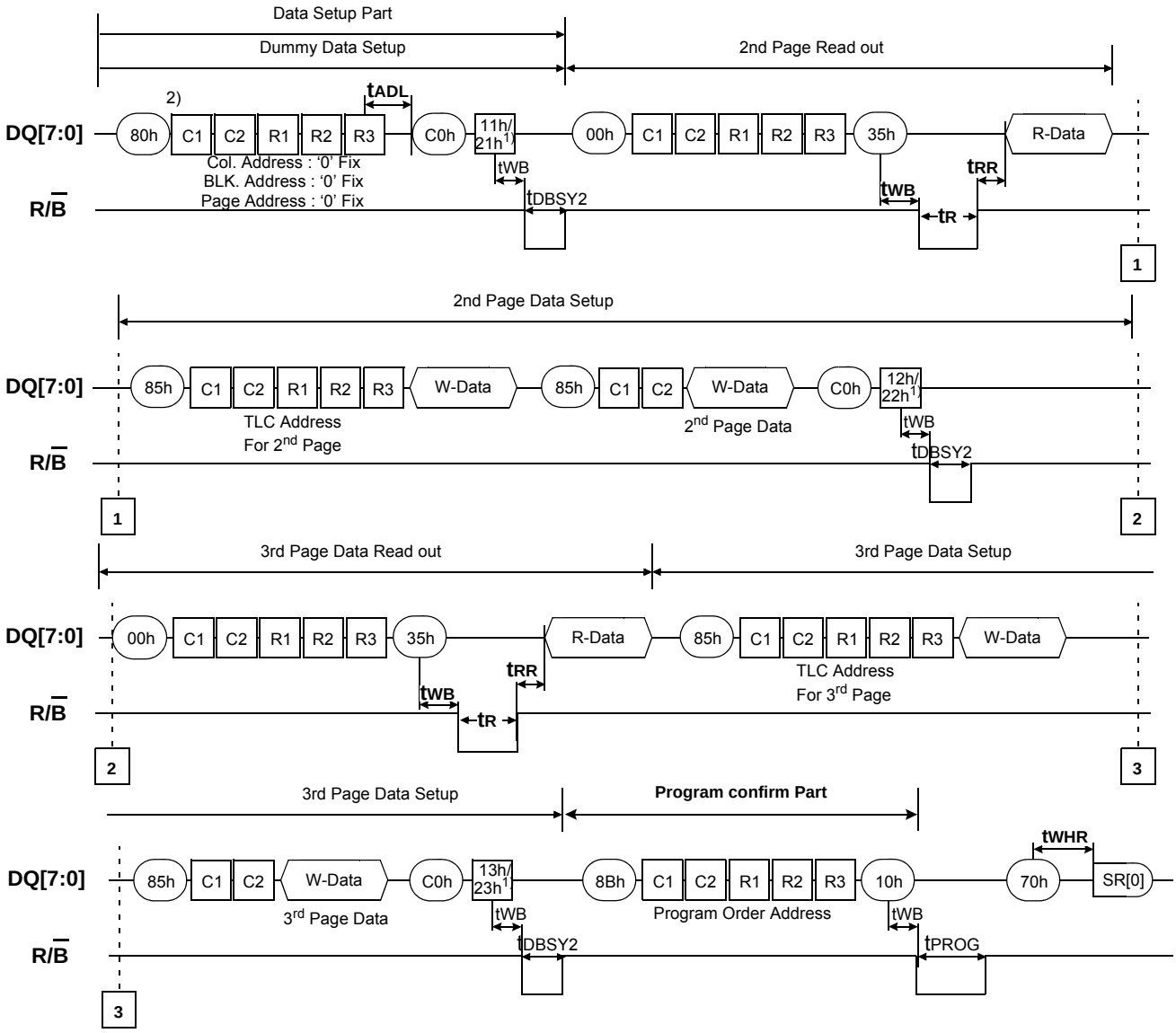


Figure 40. Copy-Back Program with Random Data Input Sequence (Edge MLC)

NOTE :
1) Refer to buffer address Table 31.
2) No actual data loading (page address, block address, column address "0" fix in dummy data setup.

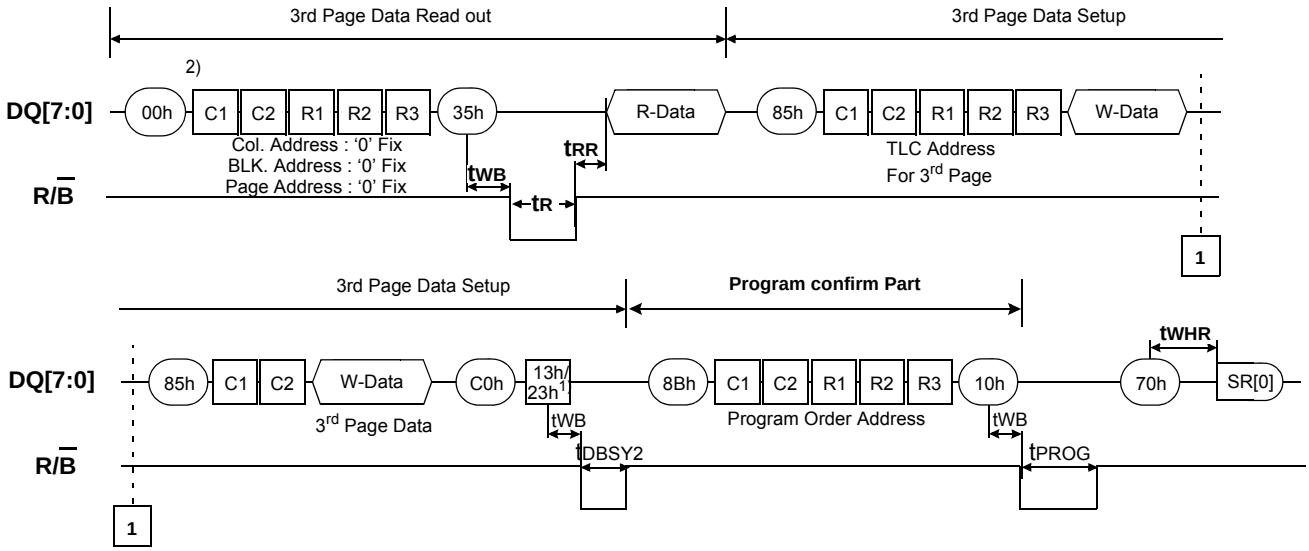


Figure 41. Copy-Back Program with Random Data Input Sequence (Edge SLC)

NOTE :
1) Refer to buffer address Table 31.

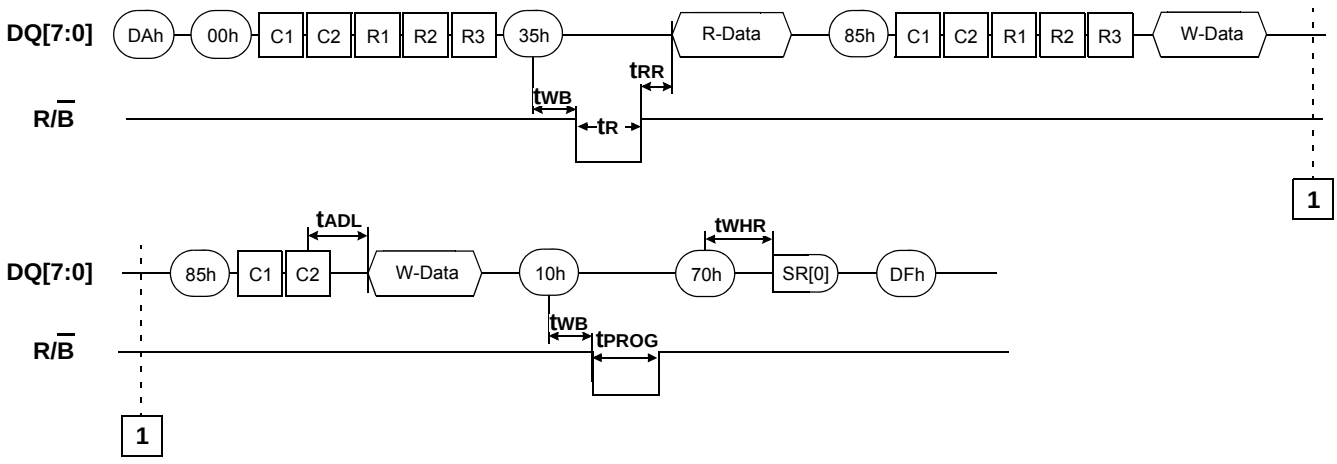


Figure 42. Copy-Back Program with Random Data Input Sequence (SLC)

5.2.7 Cache Program Operation

The Cache Program function allows the host to write the next data for another page to the page register while a page of data to be programmed to the Flash array for the selected LUN. When command 15h is issued, R/$\overline{B}$ returns high (i.e. ready) when a cache register is ready to be written after data in the cache register is transferred to a page register. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS or READ STATUS ENHANCED table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Cache Program operation except RESET and READ STATUS commands are prohibited.
When command 10h is issued for the final page, R/$\overline{B}$ turns to high after outstanding program operation performed by previous Cache Program command and the program operation for the final page is completed. SR[0] is valid for this command after SR[5] transitions from zero to one until the next transition. SR[1] is valid for this command after SR[6] transitions from zero to one, and it is invalid after the first Cache Program Command completion since there is no previous Cache Program operation. Cache Program operation shall work only within a block. Figure 46 defines the Cache Program behavior and timings. Note that tPROG at the end of the caching operation may be longer than typical as this time also includes completing the programming operation for the previous page. Writing beyond the end of the page register is undefined.

1st/2nd/3rd Page Cache Program Operation

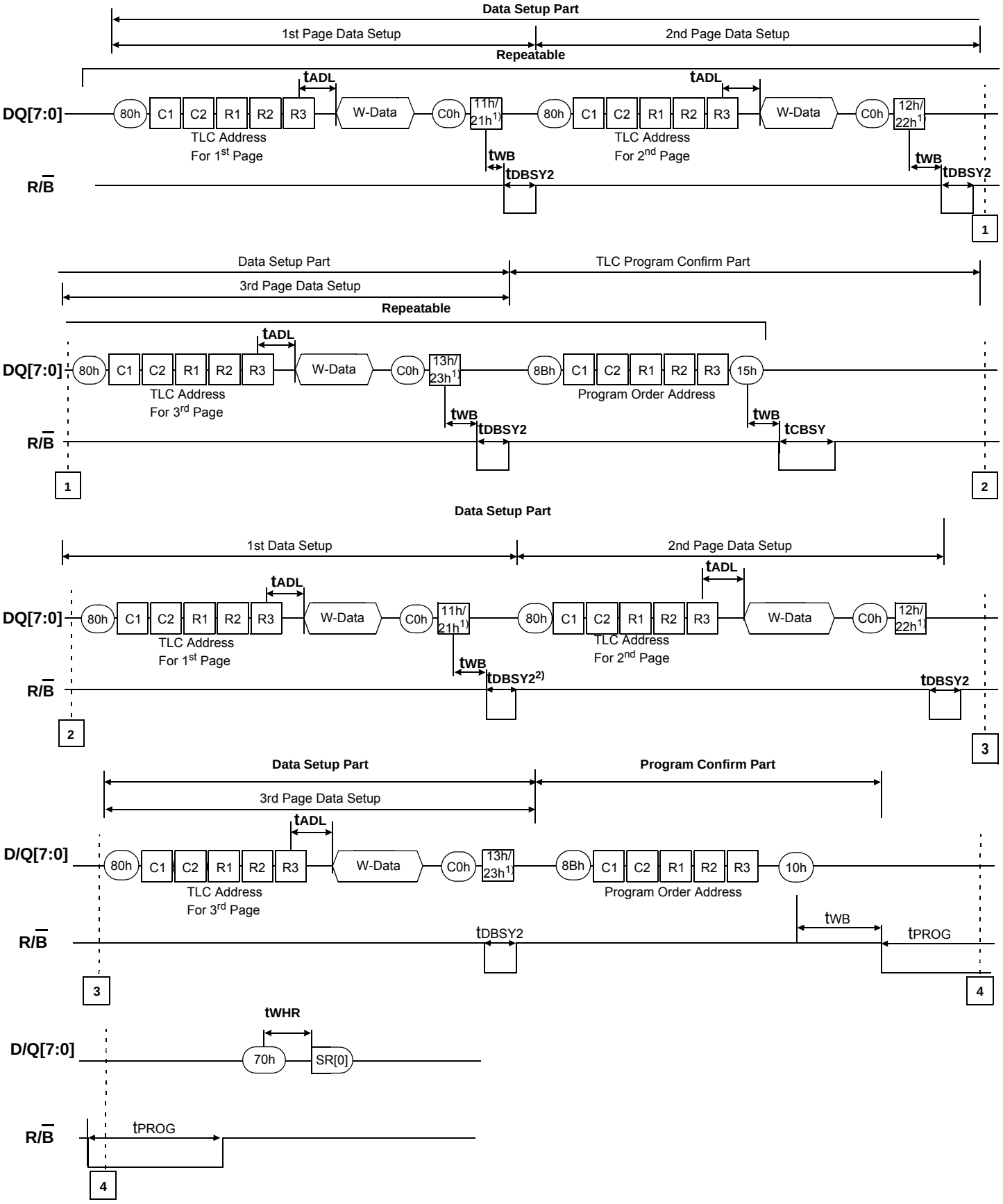


Figure 43. Page Cache Program Operation (TLC)

NOTE :
1) Refer to buffer address Table 31.
2) tDBSY2' = tCBSY (Dummy busy time for Cache Program) + tDBSY2.

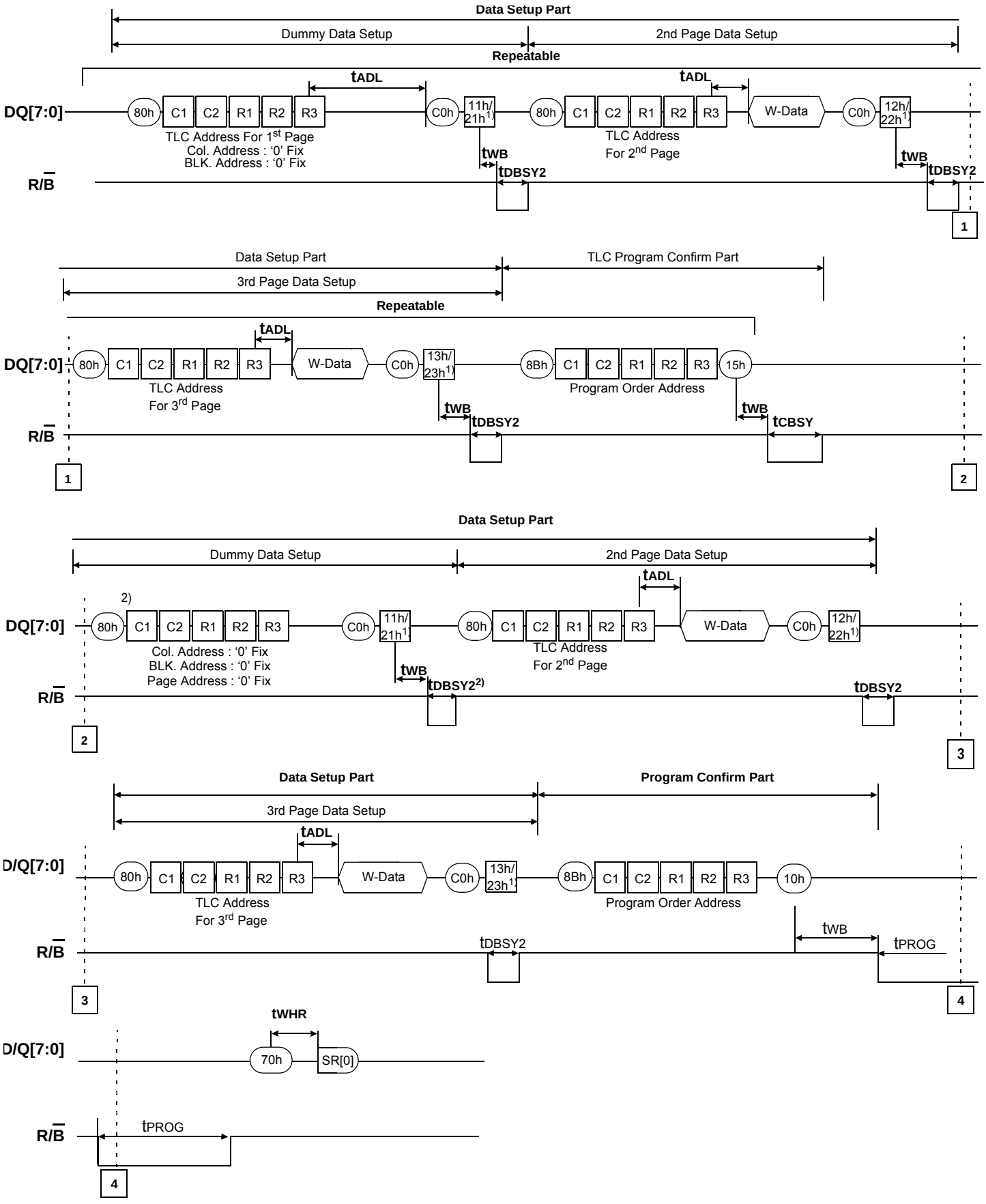


Figure 44. Page Cache Program Operation (Edge MLC)

NOTE :
1) Refer to buffer address Table 31.
2) No actual data loading (page address, block address, column address "0" fix in dummy data setup.

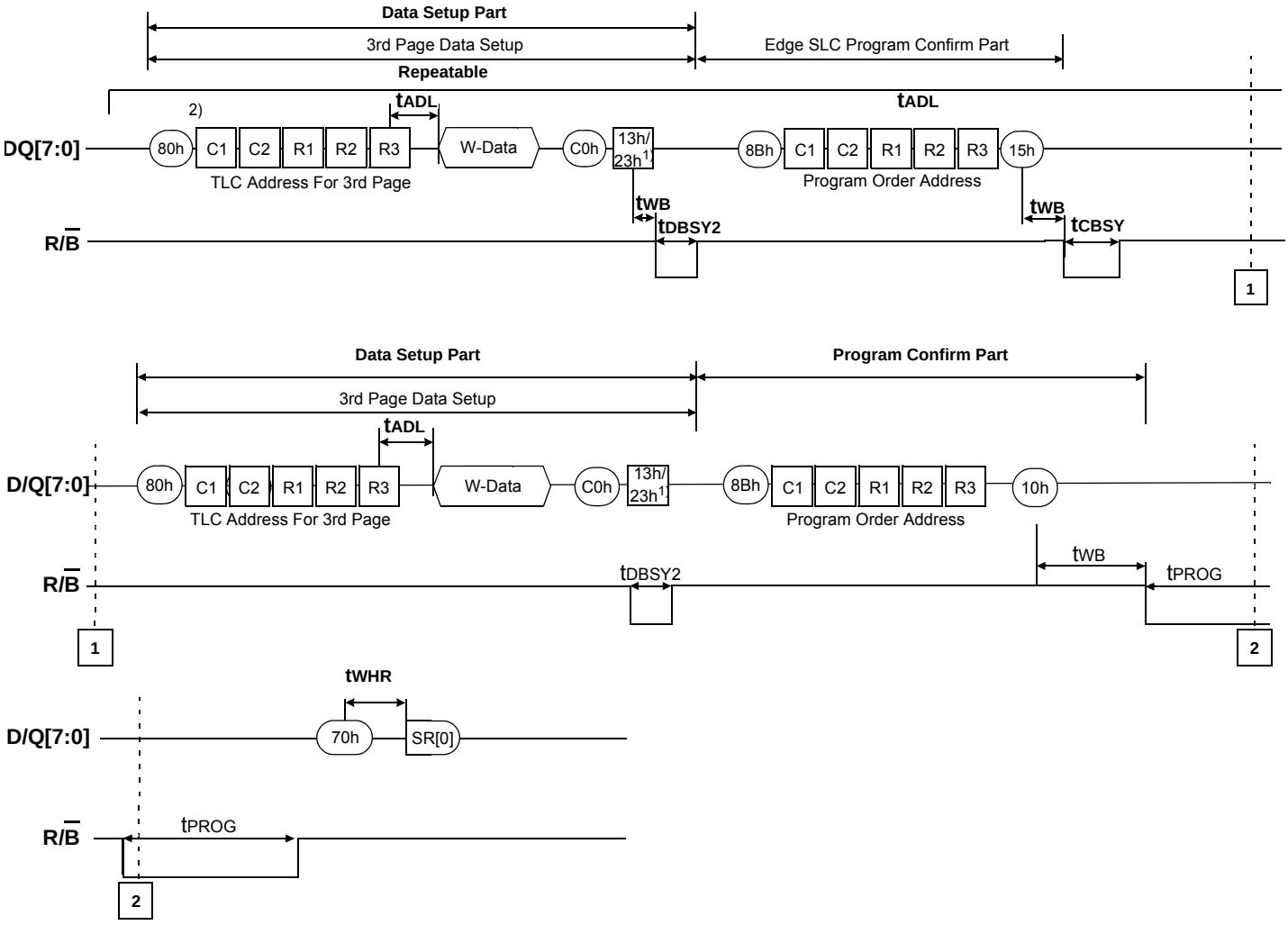


Figure 45. Page Cache Program Operation (Edge SLC)

NOTE :
1) Refer to buffer address Table 31.

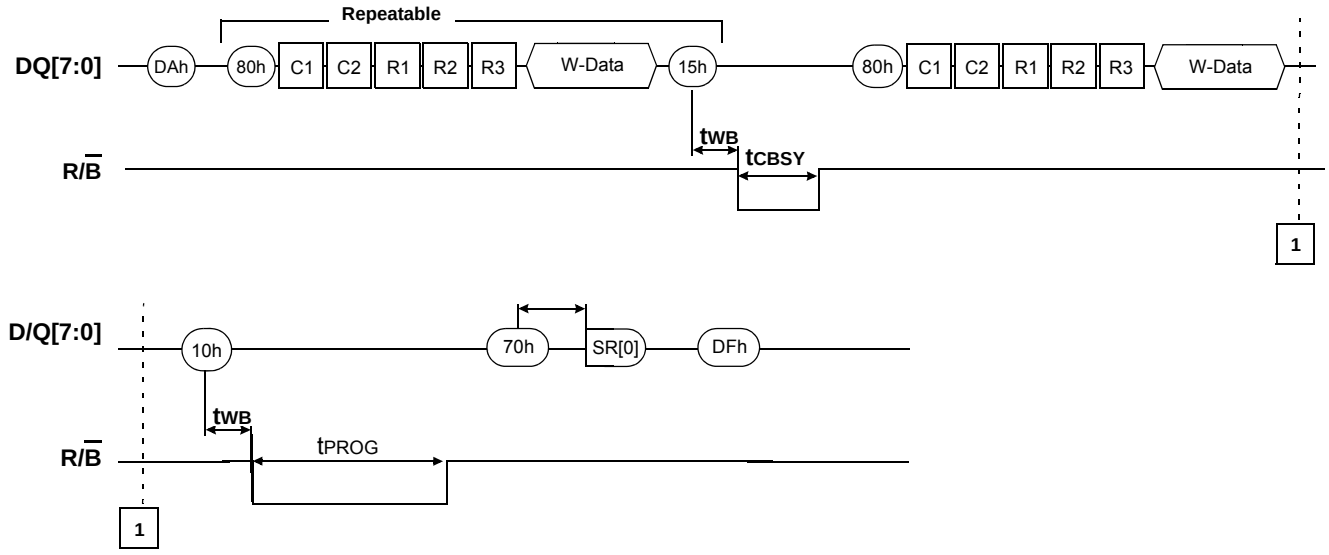


Figure 46. SLC Page Cache Program Operation (SLC)

5.2.8 Block Erase Operation

The Block Erase operation is done on a block basis. Only three cycles of row addresses are required for Block Erase operation and a page address within the cycles is ignored while block address is valid.
After Block Erase operation passes, all bits in the block shall be set to one. SR[0] is valid for this command after SR[6] transitions from zero to one(i.e. the selected LUN is ready) until the LUN goes in busy state by a next command. Figure 47 defines the Block Erase behavior and timings.

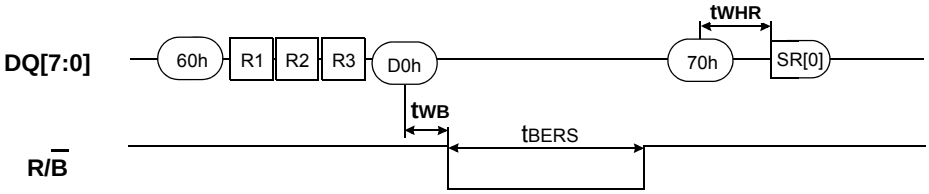


Figure 47. Block Erase Sequence

5.2.9 Reset Operation

Toggle DDR NAND offers a reset function by command FFh. When the device is in 'Busy' state during any operation, the Reset operation will abort these operations except during power-on when Reset shall not be issued until R/B# is set to one (i.e. ready). The contents of memory cells being programmed are no longer valid, as the data will be partially programmed or erased. Although the device is already in process of reset operation, a new reset command will be accepted. Figure 48 defines the Reset behavior and timings.

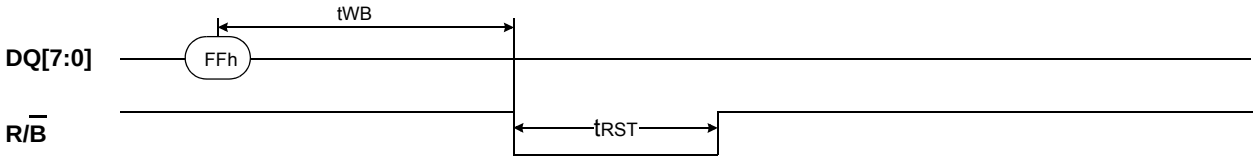


Figure 48. Reset Sequence

5.2.10 Set Feature Operation

Users may set particular features using 'Set Feature' operation. Once a feature is set by users, it shall not be changed until the device is powered off or setting is changed by users. Figure 49 defines the Set Features behavior and timings and Table 32 defines features that users can change.

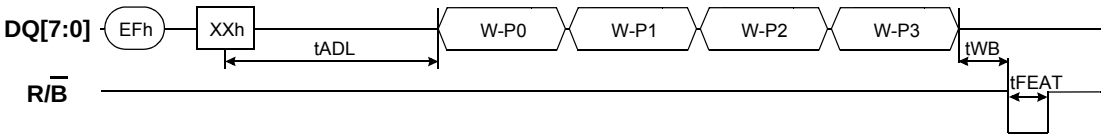


Figure 49. Set Feature Sequence (EFh)

[Table 32] Set Feature (EFh) Addresses

Feature Address	Description
02h	Toggle 2.0 specific setting
10h	Driver strength setting
30h	External V_{PP} setting

Set Feature with LUN control within 1$\overline{CE}$

Features such as Read retry and Erase information for Erase resume should be configurable for Each LUN.

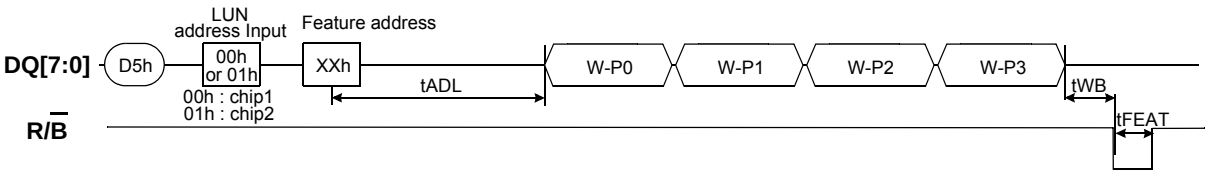


Figure 50. Set Feature Sequence (D5h)

[Table 33] Set Feature (D5h) Addresses

LUN Address	Feature Address	Description
00h / 01h	89h	Read Retry setting
	8Ah	
	8Dh	

5.2.10.1 Toggle 2.0 Specific Setting (02h)

This setting is required in order to use reference voltage and complementary signal. DQS latency cycle can also be configured by this SET FEATURE operation to read the first valid data correctly.
When $V_{REF}Q$ signal or complementary signals are set, those signals shall be applied before SET FEATURE sequence.
The setting is done at the rising edge of R/$\overline{B}$, thus the signals are used to check ready by READ STATUS operation.

[Table 34] Toggle 2.0 specific setting assignment

P0	**I/O7**	**I/O6**	**I/O5**	**I/O4**	**I/O3**	**I/O2**	**I/O1**	**I/O0**
	N/A				Reserved	RE	$\overline{DQS}$	$V_{REF}Q$
P1	**I/O7**	**I/O6**	**I/O5**	**I/O4**	**I/O3**	**I/O2**	**I/O1**	**I/O0**
	# of Latency DQS cycle for WRITE				# of Latency DQS cycle for READ			

NOTE :
1) P2 and P3 are reserved.
2) P2, P3, N/A, and reserved shall be written with 00h.
3) When differential signaling (i.e. RE and $\overline{DQS}$) is used, $V_{REF}Q$ shall be set to be enabled for DQ.

[Table 35] Definition of Toggle 2.0 Specific Setting

	Description
$V_{REF}Q$	0 : Disabled (default) 1 : Enabled
$\overline{DQS}$	0 : Disabled (default) 1 : Enabled
RE	0 : Disabled (default) 1 : Enabled
# of Latency DQS Cycle (Write)	0000 : No latency DQS cycle (default) 0001 : One latency DQS cycle 0010 : Two latency DQS cycle 0011 : Four latency DQS cycle
# of Latency DQS Cycle (Read)	0000 : No latency DQS cycle (default) 0001 : One latency DQS cycle 0010 : Two latency DQS cycle 0011 : Four latency DQS cycle

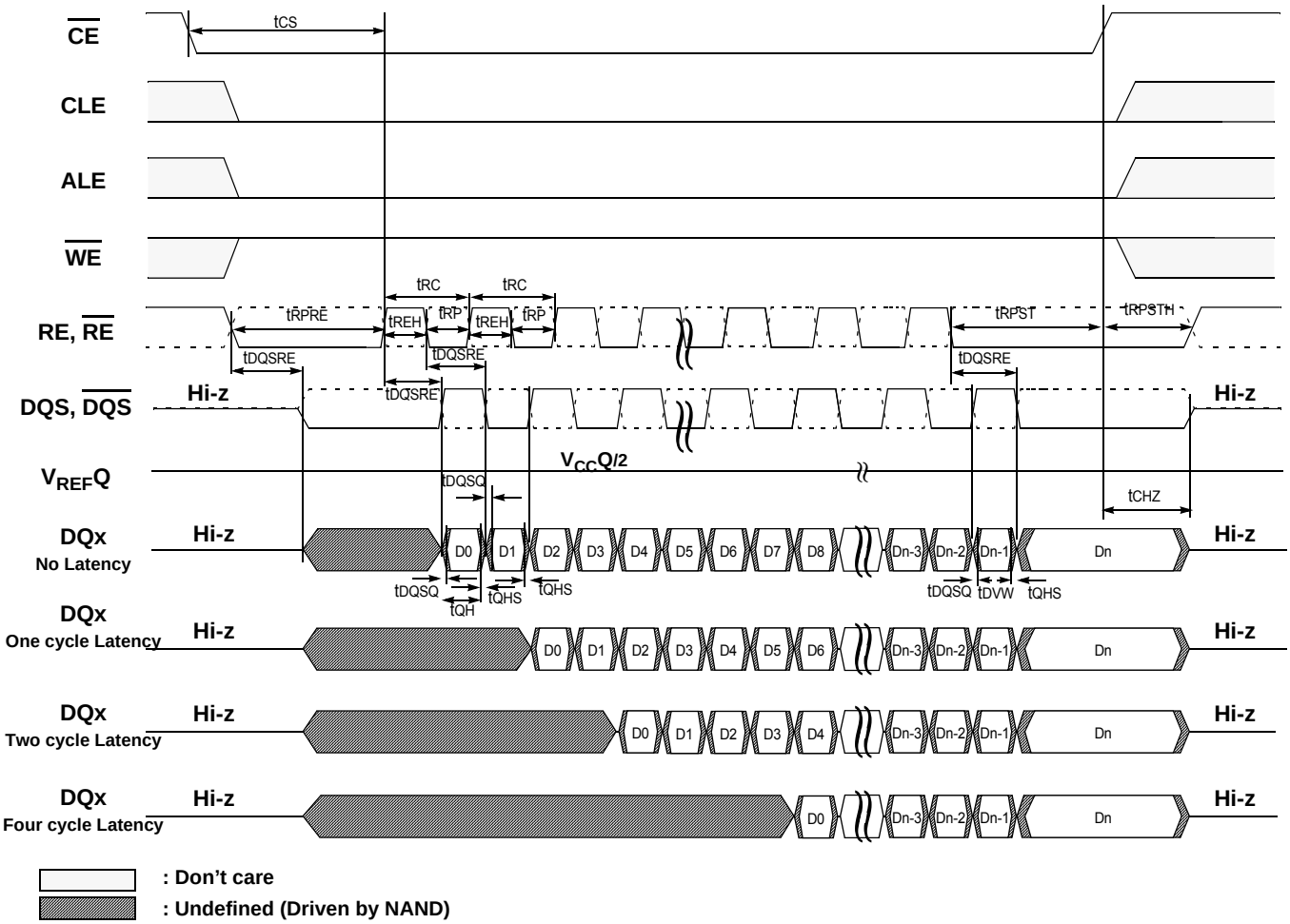
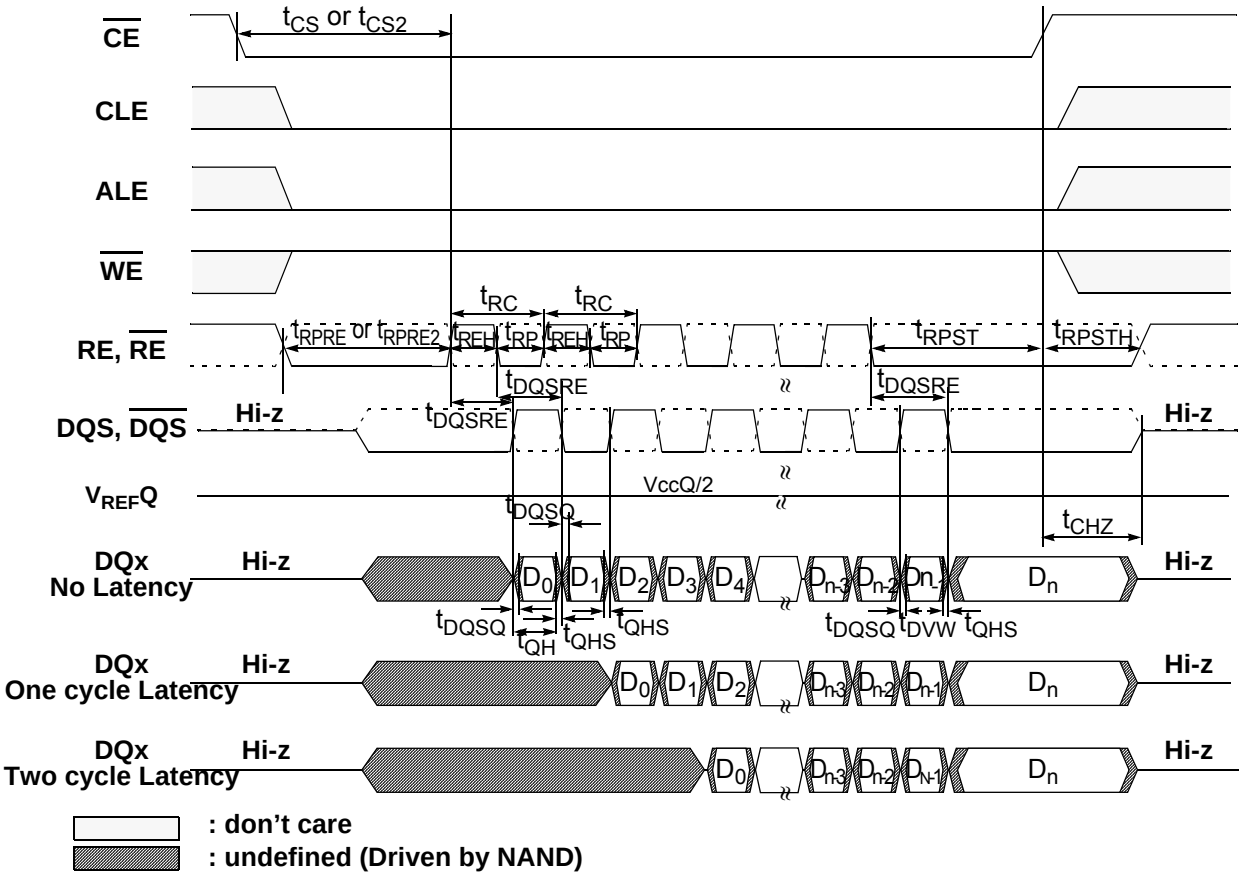


Figure 51. Example of DQS Latency (Read)


CE
CLE
ALE
WE
RE, RE
DQS, DQS
VREFQ
DQx
No Latency
DQx
One cycle Latency
DQx
Two cycle Latency
tCS or tCS2
tRC
tRC
tRPRE or tRPRE2
tREH
tRP
tREH
tRP
tRPST
tRPSTH
tDQSRE
tDQSRE
tDQSRE
Hi-z
Hi-z
VccQ/2
tDQSQ
tCHZ
Hi-z
Hi-z
D0
D1
D2
D3
D4
Dn-3
Dn-2
Dn-1
Dn
tDQSQ
tQH
tQHS
tQHS
tDQSQ
tDVW
tQHS
Hi-z
Hi-z
D0
D1
D2
Dn-3
Dn-2
Dn-1
Dn
Hi-z
Hi-z
D0
Dn-3
Dn-2
Dn-1
Dn
Hi-z
: don't care
: undefined (Driven by NAND)

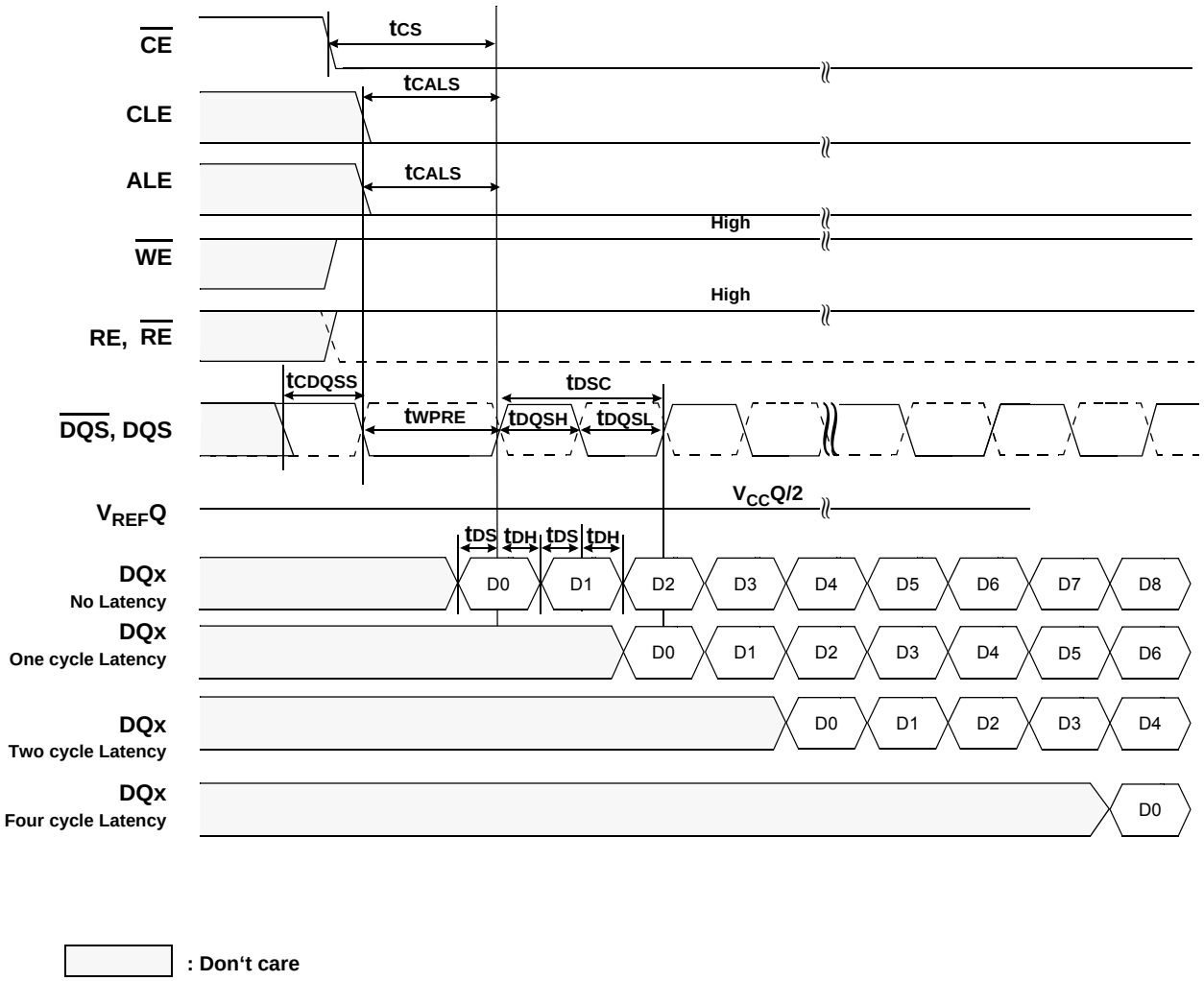


Figure 52. Example of DQS Latency (Write)

5.2.10.2 Driver Strength Setting (10h)

Driver strength is configured according to the P0 value.

[Table 36] Definition of Driver Strength Setting

P0 Value	Description
00h	Reserved
01h	Reserved
02h	Driver Multiplier : Underdriver(x0.75)
03h	Reserved
04h	Driver Multiplier : 1 (default)
05h	Reserved
06h	N/A
07h	Reserved
08h	N/A
09h ~ FFh	Reserved

NOTE :
P1, P2 and P3 are reserved and shall be written with 00h.

5.2.10.3 External V_{PP} (30h)

(WARNING : SAMSUNG RECOMMENDS THE USER TO CONTACT AND CONSULT SAMSUNG BEFORE ENABLING THIS FUNCTION. ENABLING THIS FUNCTION MAY CAUSE MALFUNCTION, INCLUDING BUT NOT LIMITED TO PERMENANT DAMAGE TO THE CHIP).
External high voltage(i.e. typical 12V) feature offers power saving on program and read operations. The external high voltage shall be supplied prior to the feature setting and it shall persist within 11V to 13V until it is set to defalut(i.e. off). The maximum external V_{PP} supply current per LUN is 5mA.

[Table 37] Definition of External V_{PP}

P0 Value	Description
00h	OFF (default)
01h	ON
02h ~ FFh	Reserved

NOTE :
P1, P2 and P3 are reserved and shall be written with 00h.

5.2.10.4 Read Retry Setting (89h, 8Ah, 8Dh)

Read Retry feature can relieve fail bit by reading again when read error occurs. If read operation is fail, read level should be set through set feature-read retry (89h). Read operation at read level newly set can relieve fail bit.

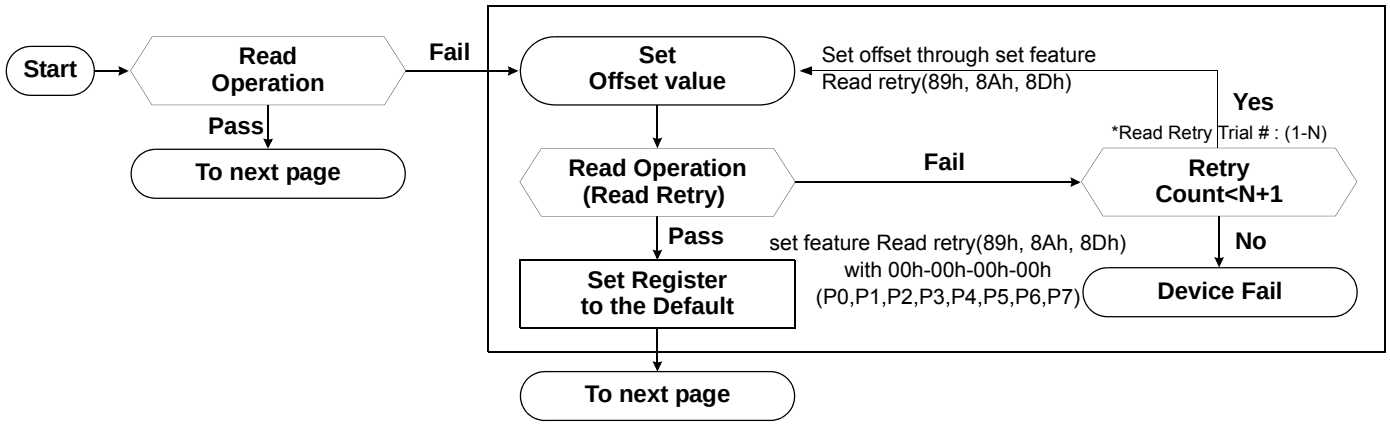


Figure 53. Read Retry sequence

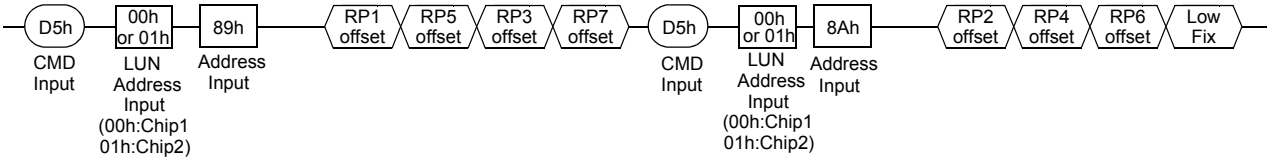


Figure 54. Set offset value for Read Retry (TLC)

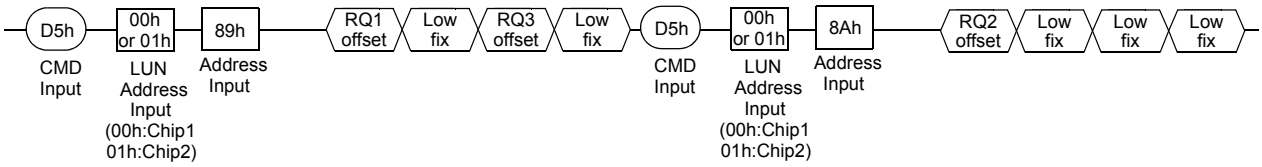


Figure 55. Set Offset Value for Read Retry (Edge MLC)

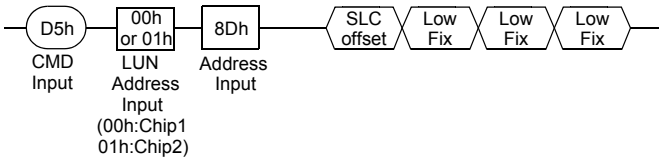


Figure 56. Set Offset Value for Read Retry(SLC/Edge SLC)

[Table 38] Description of Setting Data for MLC Read Retry(89h/8Ah)

W-P0	W-P1	W-P2	W-P3	Description
00h	00h	00h	00h	Read Retry off (default)
RQ1 ≠ 00h	00h	RQ3 ≠ 00h	00h	MLC Read Retry Offset Setting(89h)
RQ2 ≠ 00h	00h	00h	00h	MLC Read Retry Offset Setting(8Ah)

[Table 39] Description of Setting Data for TLC Read Retry

W-P0	W-P1	W-P2	W-P3	Description
00h	00h	00h	00h	Read Retry off (default)
RP1 ≠ 00h	RP5 ≠ 00h	RP3 ≠ 00h	RP7 ≠ 00h	TLC Read Retry Offset Setting(89h)
RP2 ≠ 00h	RP4 ≠ 00h	RP6 ≠ 00h	00h	TLC Read Retry Offset Setting(8Ah)

[Table 40] Specific Data of Read Retry

RP1/RP2/RP3/RP4/RP5/RP6/ RP7 value	Definition	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
0h	default	0	0	0	0	0	0	0	0
1h	+ΔmV	0	0	0	0	0	0	0	1
2h	+2ΔmV	0	0	0	0	0	0	1	0
3h	+3ΔmV	0	0	0	0	0	0	1	1
4h	+4ΔmV	0	0	0	0	0	1	0	0
:	:								
:	:								
FCh	-4ΔmV	1	1	1	1	1	1	0	0
FDh	-3ΔmV	1	1	1	1	1	1	0	1
FEh	-2ΔmV	1	1	1	1	1	1	1	0
FFh	-ΔmV	1	1	1	1	1	1	1	1

[Table 41] Related RVs According to the TLC Operations

Mode	Program Sequence	RV(s)	Input Address
TLC Block - TLC WLs	LSB Page	RP1 / RP5	0x89
	CSB Page	RP2 / RP4 / RP6	0x8A
	MSB Page	RP3 / RP7	0x89
TLC Block - SLC WLs	SLC Page	SLC	0x8D
TLC Block - MLC WLs	LSB Page	RQ2	0x8A
	MSB Page	RQ1 / RQ3	0x89
SLC		SLC	0x8D

5.2.11 Get Feature Operation

Users find how the target is set through 'Get Feature' command. The function shall return the current setting information. If a host starts to read the first byte of data (i.e. P0 value), the host shall complete reading all four bytes of data before issuing another command (including Read Status or Read Status Enhanced). Figure 57 defines the Get Features behavior and timings.

If Read Status (or Read Status Enhanced) is used to monitor whether the tFEAT time is complete, the host shall issue Read command (i.e. 00h) to read P0-P1-P2-P3.

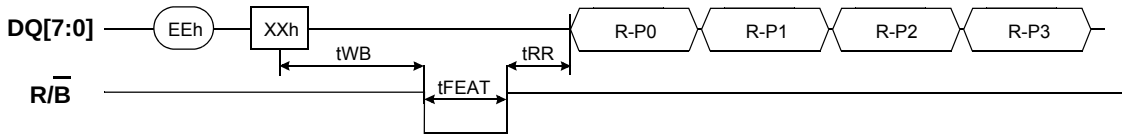


Figure 57. Get Feature Sequence

[Table 42] Get Feature(EEh) Addresses

Feature Address	Description
02h	Toggle 2.0 specific setting
10h	Driver strength setting
30h	External V_{PP} setting

Get Feature with LUN control within 1$\overline{CE}$(D4h)

Features such as Read retry and Erase information for Erase resume shall be configurable for Each LUN. The current setting information for the two features shall return through D4h Command, Get Feature with LUN control within 1$\overline{CE}$.

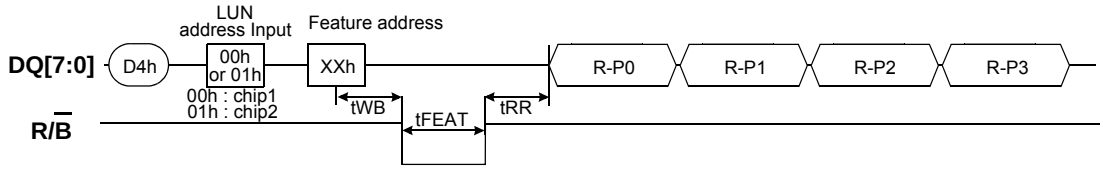


Figure 58. Get Feature Sequence (D4h)

[Table 43] Get Feature(D4h) Addresses

LUN Address	Feature Address	Description
00h / 01h	89h	Read Retry setting
	8Ah	
	8Dh	

5.2.12 Read ID Operation

The ID of a target is read by command 90h followed by 00h or 40h address. Read ID operation shall work on lower than 66MHz. Figure 59 defines Read ID operation behavior and timings.

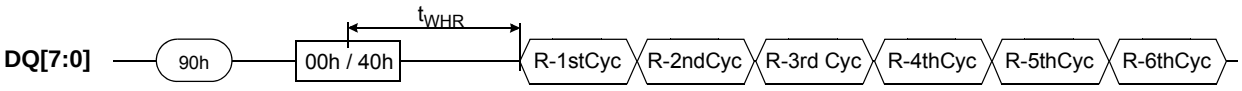


Figure 59. Read ID Sequence

5.2.12.1 00h Address ID Definition

Users can read six bytes of ID containing manufacturer code, device code and architecture information of the target by command 90h followed by 00h address. The command register remains in Read ID mode until another command is issued.

5.2.12.1.1 00h Address ID Cycle

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9AFGD8H0A	ECh	1Ch	98h	3Fh	84h	CBh

[Table 44] 00h Address ID Definition Table

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc.
4th Byte	Page Size, Block Size, Redundant Area Size.
5th Byte	Plane Number, ECC Level, Organization.
6th Byte	Device Technology, EDO, Interface.

[Table 45] 3rd ID Data

	Description	DQ7	DQ6	DQ5 DQ4	DQ3 DQ2	DQ1 DQ0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleaving operation between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

[Table 46] 4th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Page Size (w/o redundant area)	Reserved							0	0
	Reserved							0	1
	8KB							1	0
	16KB							1	1
Block Size (w/o redundant area)	4.5MB	0		0	0				
	6MB	0		0	1				
	9MB	0		1	0				
	12MB	0		1	1				
	1.5MB	1		0	0				
	8MB	1		0	1				
	3MB	1		1	0				
	4MB	1		1	1				
Spare area size (byte / Page Size)	768KB		0			0	0		
	896KB		0			0	1		
	1792B		0			1	0		
	2KB		0			1	1		
	1536B		1			0	0		
	512B		1			0	1		
	640B		1			1	0		
	1KB		1			1	1		

[Table 47] 5th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Plane Number	1					0	0	0	
	2					0	1	0	
	3					0	1	1	
	4					1	0	0	
	6					1	0	1	
	8					1	1	0	
	16					1	1	1	
ECC Level	1bit	0	0	0	0				
	2bit	0	0	0	1				
	4bit	0	0	1	0				
	8bit	0	0	1	1				
	16bit	0	1	0	0				
	24bit	0	1	0	1				
	40bit	0	1	1	0				
	60bit	0	1	1	1				
	LDPC	1	0	0	0				
	70bit	1	0	0	1				
	48bit	1	0	1	0				
Reserved									0

[Table 48] 6th ID Data

	Description	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Device Version	V1					0	1	1	1
	V2					1	0	0	0
	V3					1	0	0	1
	V4					1	0	1	1
EDO	Not Support		0						
	Support		1						
Interface	SDR	0							
	Toggle DDR	1							
Reserved				0	0				

5.2.12.2 40h Address ID Definition

Toggle DDR NAND also provide a six bytes of JEDEC standard signature ID. Users can read the ID by command 90h followed by 40h address. Any data returned after the six bytes of JEDEC standard signature is considered reserved for future use.

[Table 49] 40h Address ID Cycle

1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
4Ah	45h	44h	45h	43h	02h

[Table 50] 40h Address ID Definition

Cycle	Description	IDQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
1st	J	0	1	0	0	1	0	1	0
2nd	E	0	1	0	0	0	1	0	1
3rd	D	0	1	0	0	0	1	0	0
4th	E	0	1	0	0	0	1	0	1
5th	C	0	1	0	0	0	0	1	1
6th	Conventional Asynchronous SDR	0	0	0	0	0	0	0	1
	Toggle DDR	0	0	0	0	0	0	1	0
	Synchronous DDR	0	0	0	0	0	1	0	0

5.2.13 Read Status Operation

In the case of non-Two-Plane operations, the Read Status function retrieves a status value for the last operation issued. If multiple Two-Plane operations are in progress on a single LUN, then Read Status returns the composite status value. Specifically, Read Status shall return the combined status value of the independent status register bits according to Table 51. Figure 60 defines the Read Status behavior and timings.

[Table 51] Read Status Definition

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Reserved	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Page Program	Pass/Fail	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Ready for New Command*: '0' Ready For New command*: '1'	Busy/Ready	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Busy/Ready for Host	Write Protect

NOTE :
New Commands are allowable command referring to NOTE2 of Table 30.

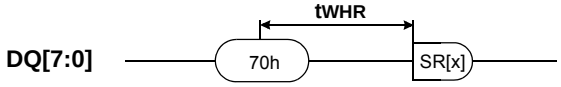


Figure 60. Read Status Sequence

5.2.14 Reset LUN Operation

A certain LUN within a target can be reset by command FAh followed by row addresses. Row addresses are required to set a LUN to be reset. Figure 61 defines the Reset LUN behavior and timings.

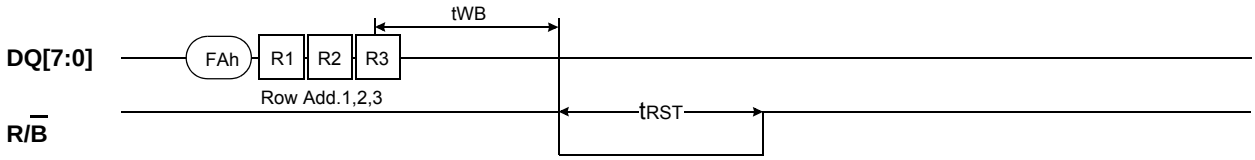


Figure 61. Single Chip Reset Sequence

5.3 Extended Operation

5.3.1 Extended Command Sets

Table 52 defines the Extended Command Sets. Primary is also categorized in the table. Primary Commands is recommended to use when a particular function is implemented for backward compatibility.

[Table 52] Extended Command Sets

Mode	Function	1st Set	Address Cycles for 1st Set	2nd Set	Address Cycles for 2nd Set
Common	4KB Two-Plane Page Read	00h--32h	5	00h--50h	5
	8KB Two-Plane Page Read	00h--32h	5	00h--20h	5
	16KB Two-Plane Page Read	00h--32h	5	00h--30h	5
	16KB Two-Plane Random Cache Read	00h--32h	5	00h--31h	5
	16KB Sequential Cache Read	31h	-	-	-
	Read start for last Page Random 16KB cache	3Fh	-	-	-
	16KB Two-Plane Read for copy back	00h--32h	5	00h--35h	5
	Two-Plane copy back Program	85h--11h	5	81h	5
	Two-Plane Random Data Output [1) 3)]	00h	5	05h--E0h	2
	Two-Plane Block Erase	60h	3	D0h	-
	Read status enhanced[3)]	78h	3	-	-
	ZQ calibration	F9h, D9h	1	-	-
	Device Identification Table Read	ECh	1	-	-
TLC	Two-Plane Page Program	8Bh--11h	5[4)]	8Bh--10h	5
	Two-Plane Cache Program	8Bh--11h	5[4)]	8Bh - 15h	5
SLC	Two-Plane Page Program	80h--11h	5	81h - 10h	5
	Two-Plane Cache Program	80h--11h	5	81h - 15h	5

NOTE :
1) Two-Plane Random Data out must be used after Two-Plane Page Read or Two-Plane Cache Read operation.
2) Any command between 11h and 80h/81h/85h is prohibited except 70h/78h and FFh and FAh.
3) Allowable Command in tRRC.
4) Must be applied to program order address Table 22.

5.3.2 ZQ calibration

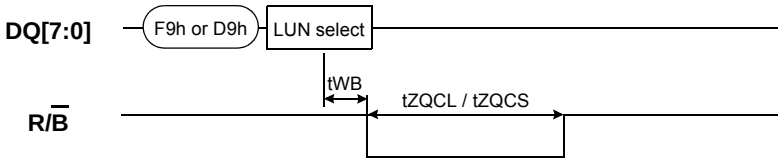
ZQ calibration is highly recommended to use NAND Flash device with over 400Mbps speed. ZQ calibration shall be performed after the driver strength setting and it shall be re-calibrated when the driver strengths are changed. ZQ calibration shall be done when the target device doesn't perform any other operation. If $V_{REF}Q$ is used, $V_{REF}Q$ shall be also enabled before ZQ calibration performs.

F9h is used for an initial ZQ calibration and D9h is for a run-time ZQ calibration which is an optional feature. The initial ZQ calibration takes 1us as maximum and the run-time ZQ calibration does 0.3us as maximum. RZQ ball of the BGA package shall be connected to Vss through 300ohm resistor (300 ohm +/- 1% tolerance external resistor).

Commands for ZQ calibration is followed by one cycle of LUN selection. 00h for LUN select points LUN0 and 01h does LUN1.

and Chapter 62 illustrates the timng of ZQ calibration.

On-Die termination shall be disabled and all devices connected to the DQ bus should be high impedance during the calibration procedure.



[Figure 62] ZQ calibration Sequence

5.3.3 Two-Plane Page Read Operation(4KB/8KB/16KB)

The Two-Plane Page Read operation is an extension of the Page Read operation. The device supporting Two-Plane page read operation also allows multiple Random data-output from each plane(i.e. Two-Plane Random Data Output) once multi-pages from each plane are loaded to page registers.
With the primary command, R/$\overline{B}$ returns to ready in a short time(i.e. tDBSY) after the first command 32h since it does not load data from a selected page, and the selected page data of each plane are transferred to the cache registers via page registers in less than tR after command 30h. When setting page addresses of each plane, the page addresses shall be identical although block addresses differ.
The Two-Plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Two-Plane Page Read Operation. Starting plane address shall be plane0.
Once the data is loaded into the cache registers, the data on the first plane can be read out by issuing the Two-Plane Random Data Output command. The data on the other plane can be also read out using the identical command sequences. Figure 63 defines Two-Plane Page Read and Two-Plane Random Data Output behavior and timings. Page Read out is only possible when the 3rd page program of Two-Plane operation.

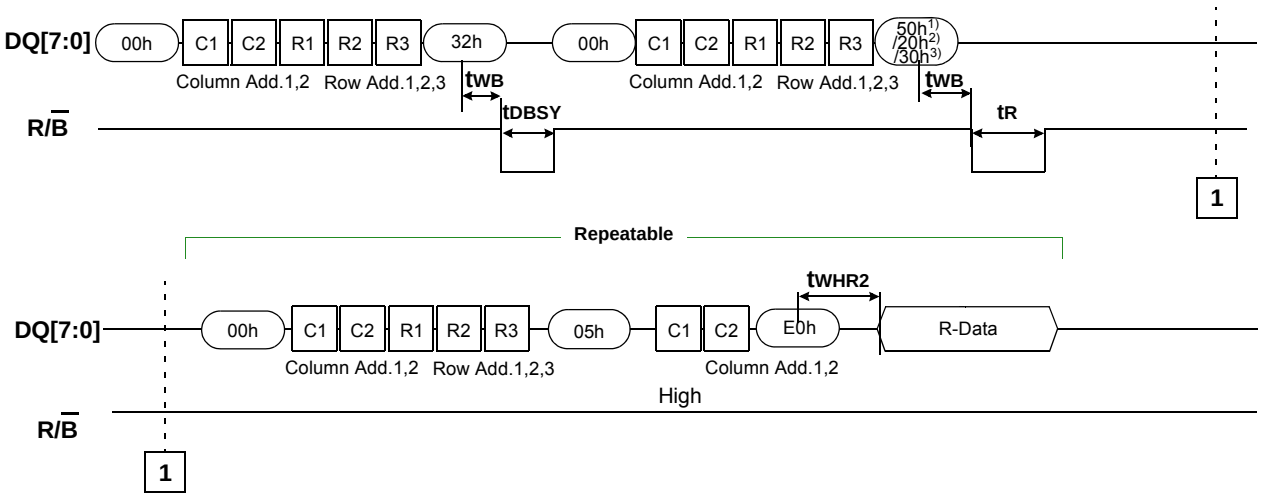


Figure 63. Example Sequence with Two-Plane Page Read

NOTE :
1) 4KB Read Command.
2) 8KB Read Command.
3) 16KB Read Command.
4) The data in the same location(i.e. the first 4KB or the second 4KB out of a page, the first 8KB or the second 8KB out of a page) of plane0 and plane1 shall be read.

5.3.4 Unaligned Two-Plane Operation

Multi-page Read / Program operation is supported in unaligned block addresses, as long as page addresses are same in all planes.

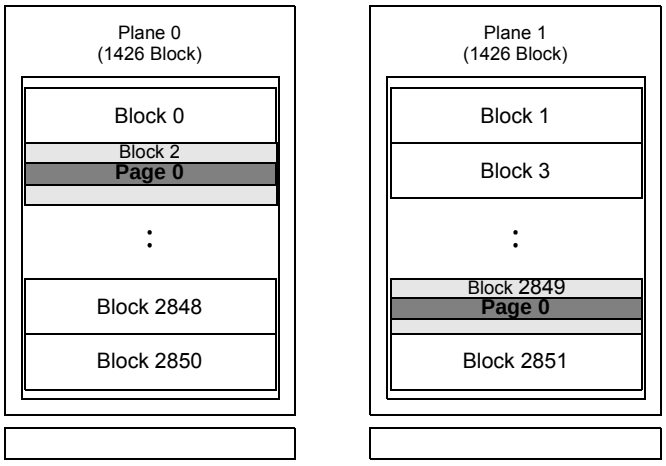


Figure 64. Example of Unaligned Two-Plane Operation

5.3.5 Two-Plane Page Program Operation

Two-Plane Page Program function extends an effective programmable page size using multiple planes.
When a host moves on a plane for loading another data, 80h--11h command set shall be used for the first plane in 2-plane page program operation. After the last page loading, 81h command set shall be used. After command 10h, all loaded data in each plane starts to be programmed to Flash array simultaneously.
The Two-Plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Two-Plane Page Program Operation. Starting plane address shall be plane0.

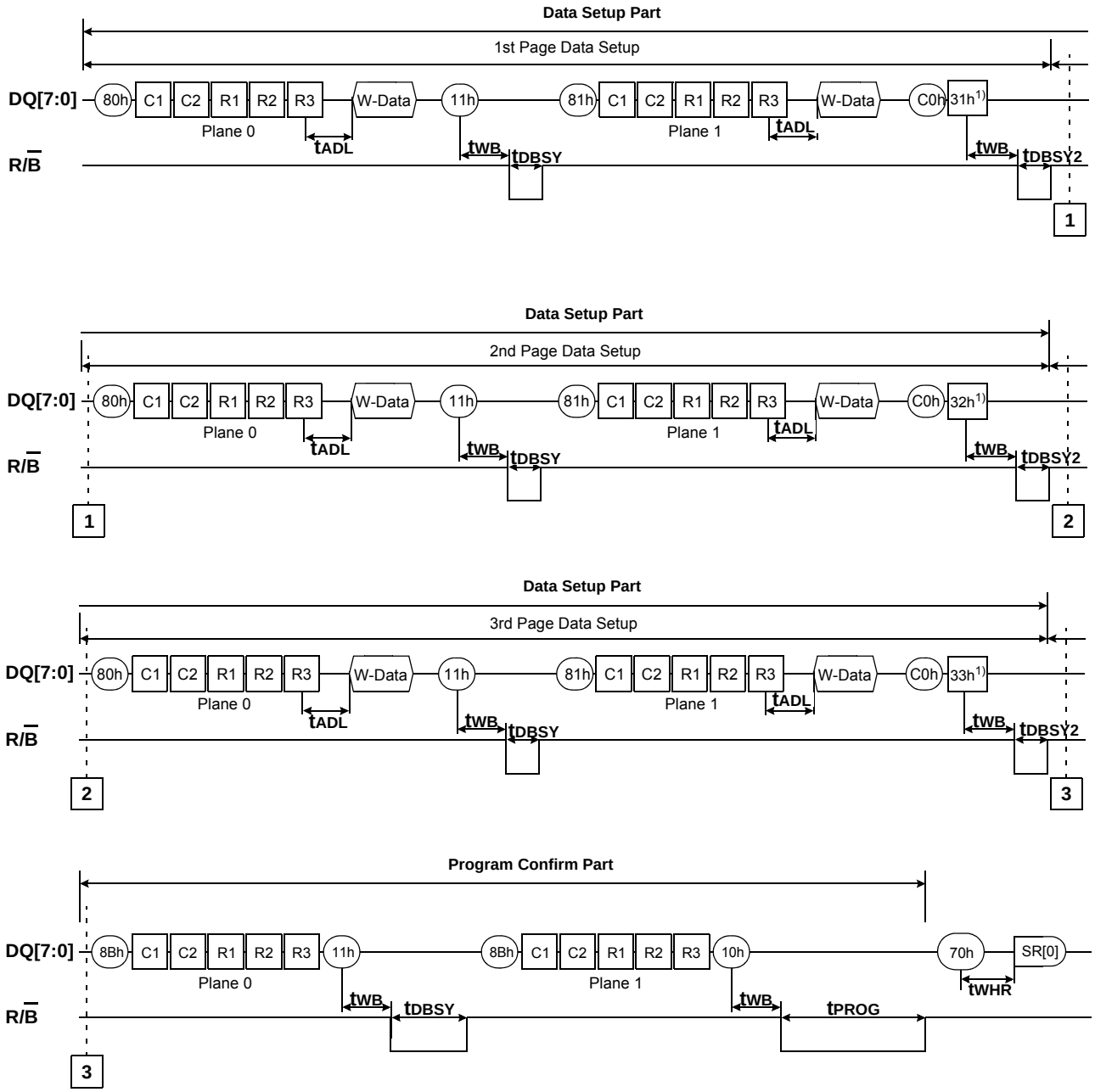


Figure 65. Example Sequence with Two-Plane Page Program (TLC)

NOTE :
1) Refer to buffer address Table 31.

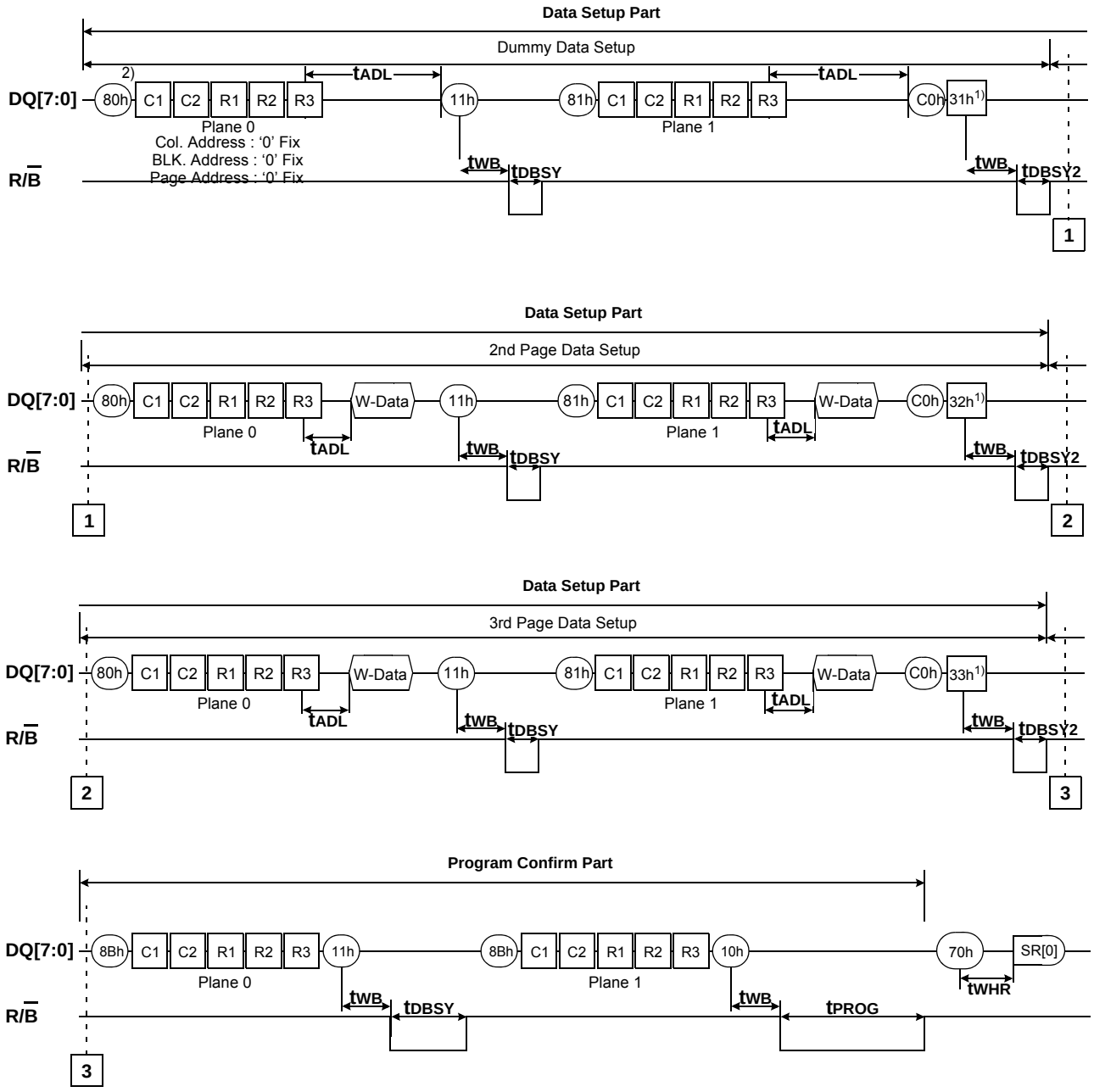


Figure 66. Example Sequence with Two-Plane Page Program (Edge MLC)

NOTE :
1) Refer to buffer address Table 31.
2) No actual data loading (page address, block address, column address "0" fix in dummy data setup.

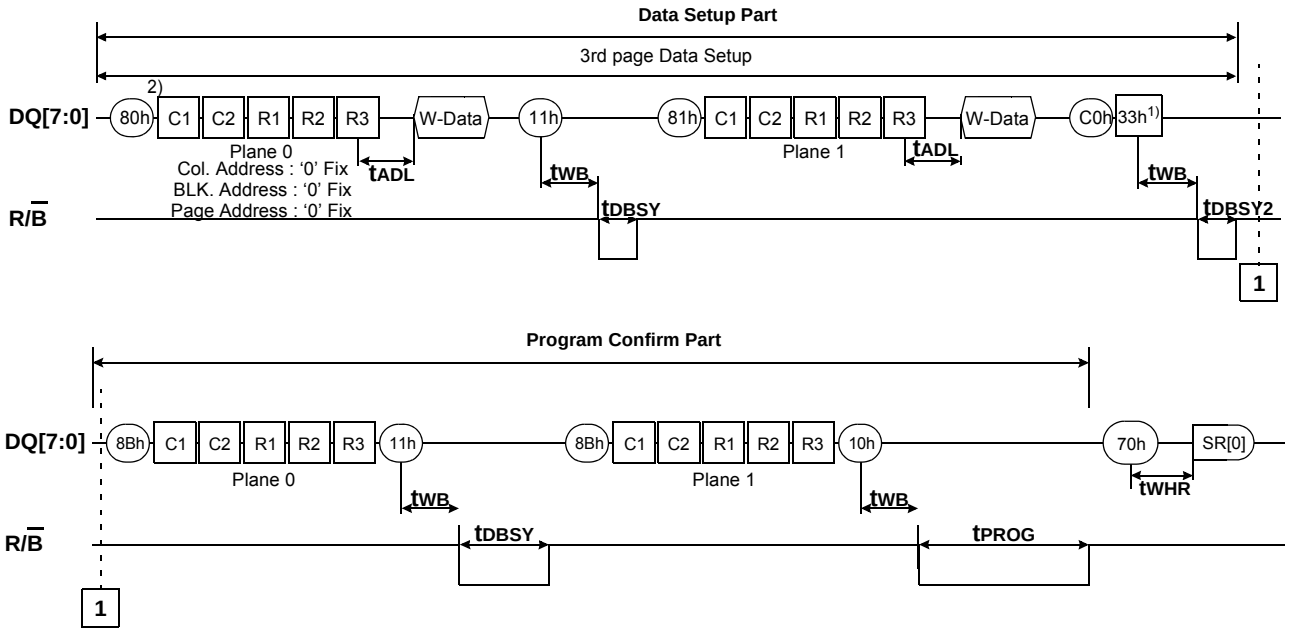


Figure 67. Example Sequence with Two-Plane Page Program (Edge SLC)

NOTE :
1) Refer to buffer address Table 31.

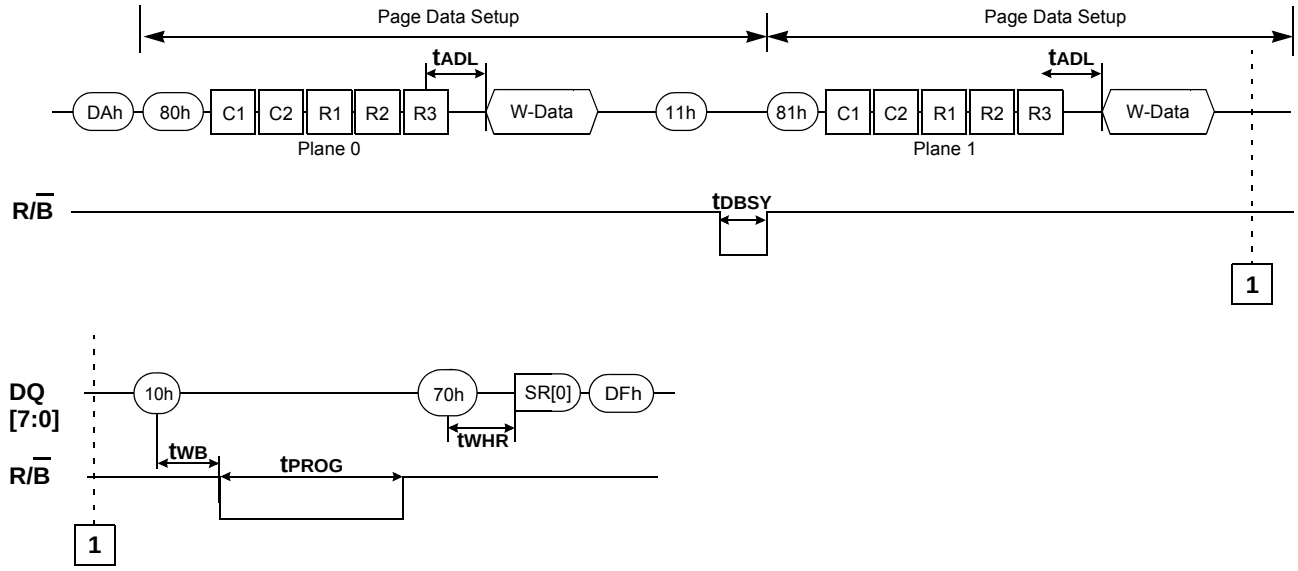
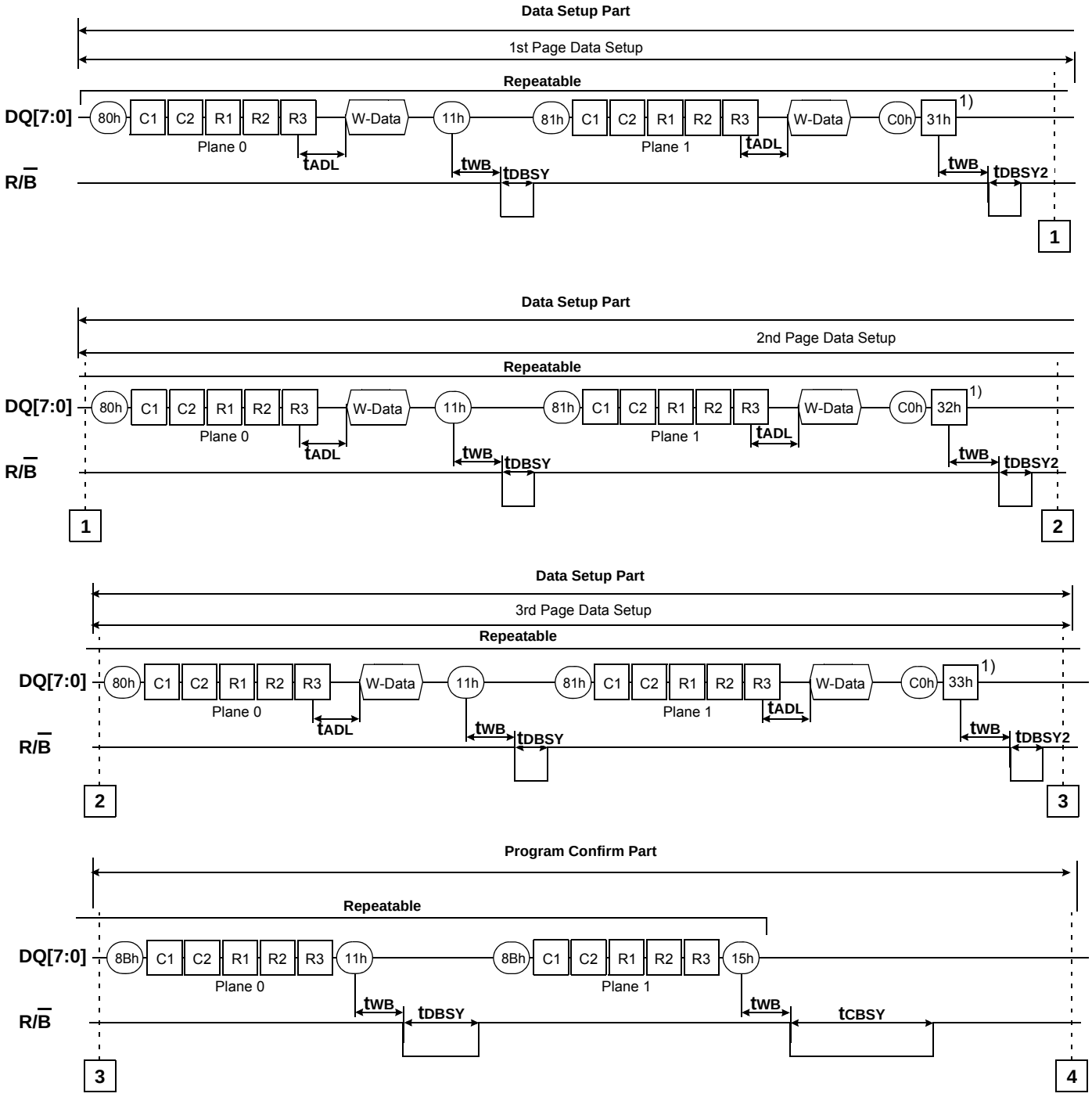


Figure 68. Example Sequence with Two-Plane Page Program (SLC)

NOTE :
The first Raw Address (R1) is required to refer Program order address in Table 24.

5.3.6 Two-Plane Cache Program Operation(1/2)

The Two-Plane Cache Program is an extension of the Cache Program. 81h-11h command set is required for the second plane in 2-Plane Cache Program Operation. 8Bh-15h command set is needed for the last plane in Two-Plane Cache Program operation. After command 15h, R/$\overline{B}$ returns high once transferring data from cache register to page register is completed. Internal program operation is in progress after R/$\overline{B}$ returns while other pages is loaded by a host. To check internal cache operation progress, ready/busy for Flash array (i.e. SR[5]) from READ STATUS or READ STATUS ENHANCED table shall be referenced. During 'busy for Flash array' period, illegal commands which is not related to Two-Plane Cache Program operation except RESET and READ STATUS commands are prohibited. At the last page loading for the entire Two-Plane Cache Program, command 10h is required to finalize the operation and R/$\overline{B}$ stays busy as long as tPROG.
The Two-Plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Two-Plane Cache Program Operation. Starting plane address shall be even ones such as plane0 and the number of planes which are set for Two-Plane Page Read Operation shall be even. The activated planes for the first Two-Plane Cache Program shall be kept using in the next address sequence until the Two-Plane Cache Program operation is completed by command 10h.
Figure 69 defines Two-Plane Cache Page Program behavior and timings.



5.3.7 Two-Plane Cache Program Operation(2/2)

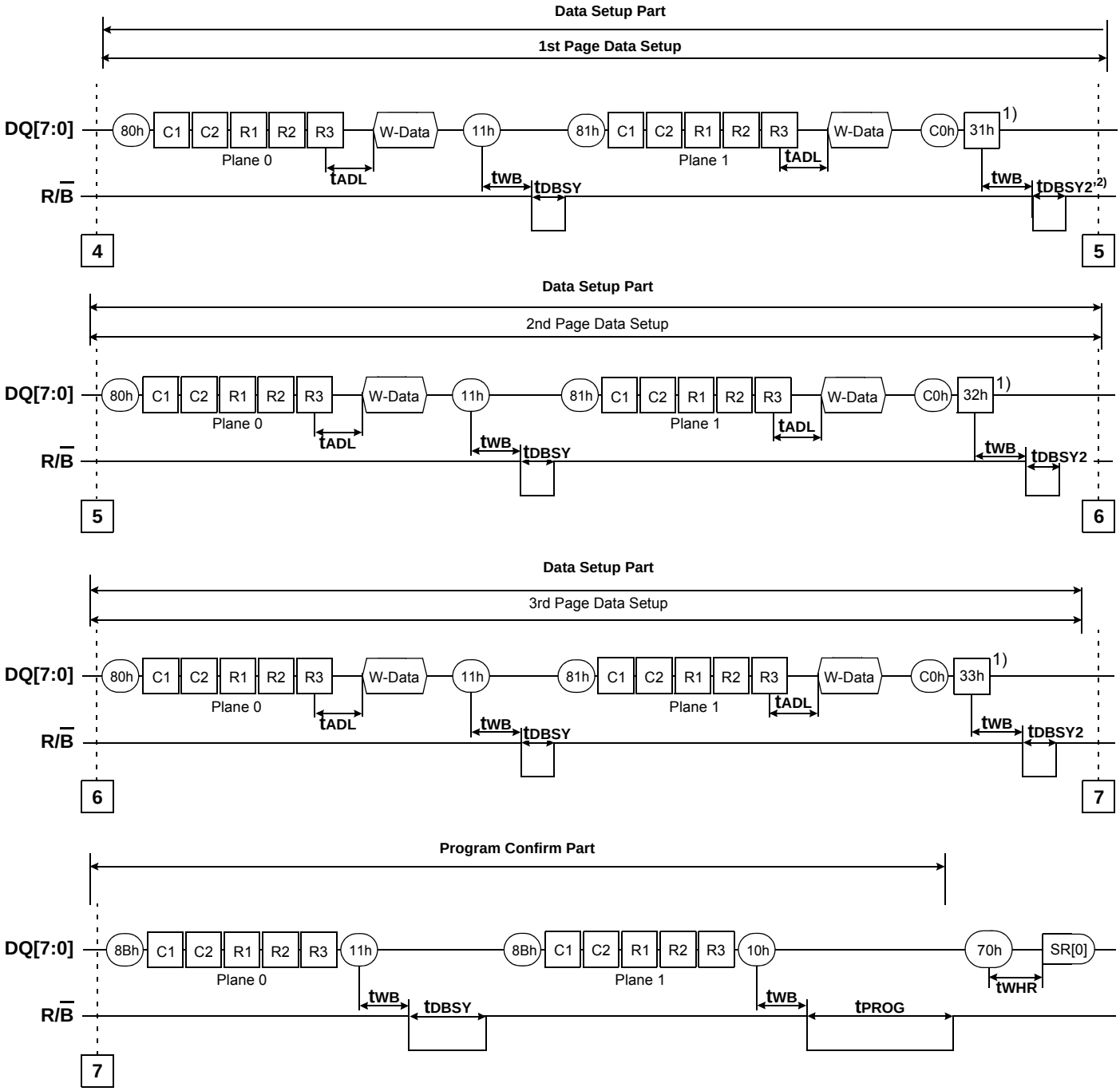
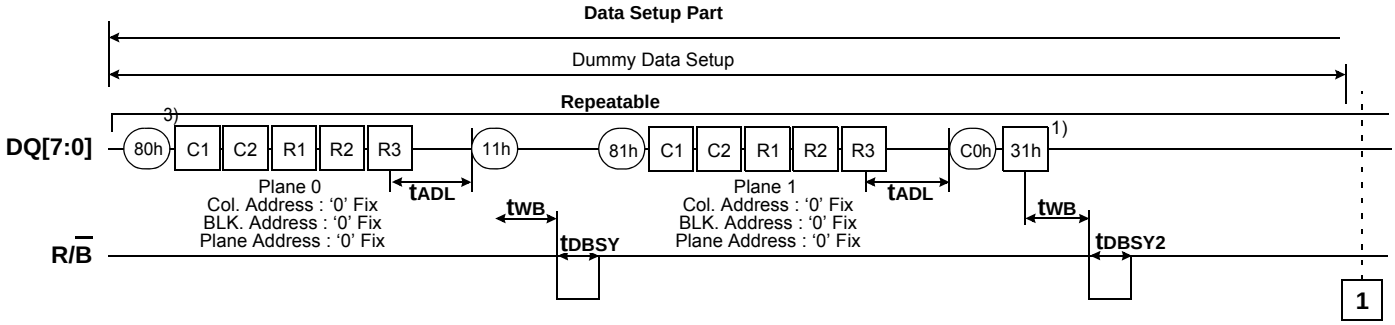
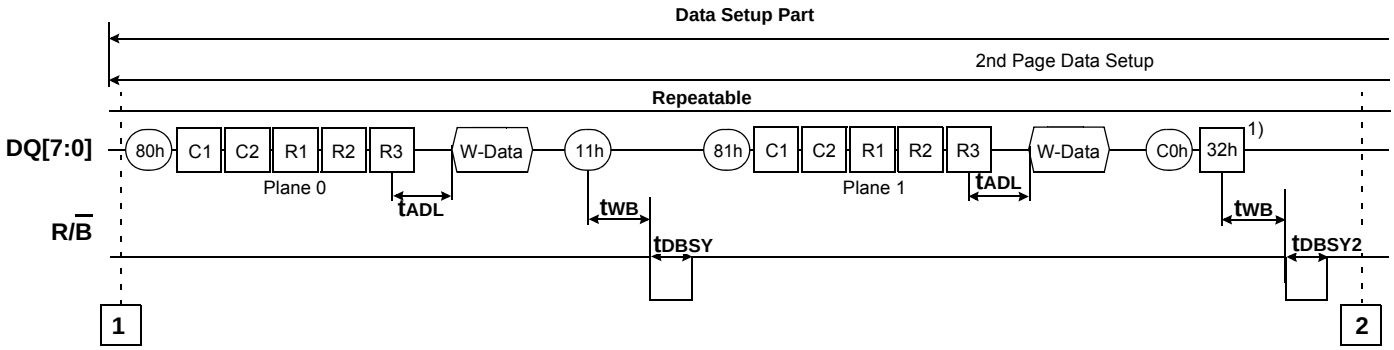
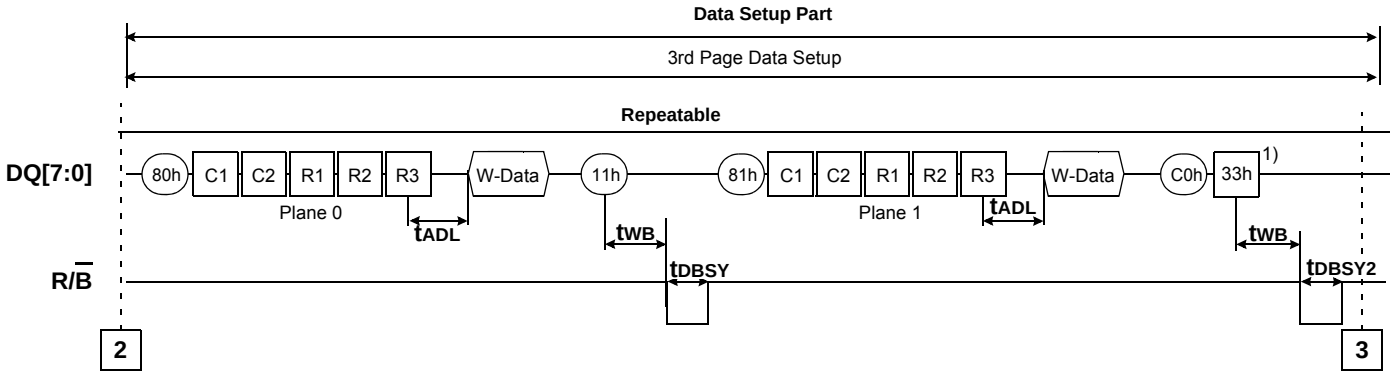


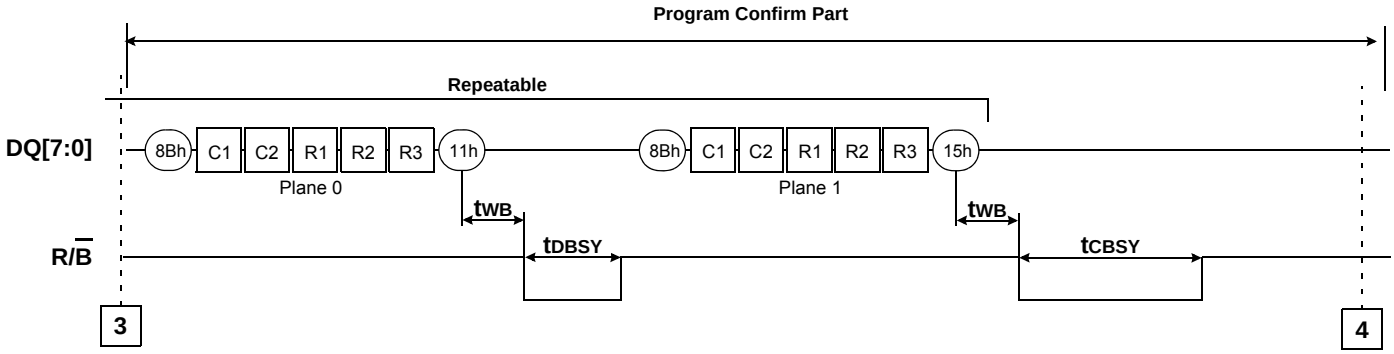
Figure 69. Example Sequence with Two-Plane Cache Program (TLC)

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 31.
2) tDBSY2' = tCBSY (Dummy Busy time for Cache Program) + tDBSY2.


Data Setup Part
Dummy Data Setup
Repeatable
DQ[7:0]
R/B
3)
80h
C1
C2
R1
R2
R3
11h
81h
C0h
31h
1)
Plane 0
Col. Address : '0' Fix
BLK. Address : '0' Fix
Plane Address : '0' Fix
Plane 1
Col. Address : '0' Fix
BLK. Address : '0' Fix
Plane Address : '0' Fix
tADL
tWB
tDBSY
tDBSY2
1


Data Setup Part
2nd Page Data Setup
Repeatable
DQ[7:0]
R/B
80h
C1
C2
R1
R2
R3
W-Data
11h
81h
C0h
32h
1)
Plane 0
Plane 1
tADL
tWB
tDBSY
tDBSY2
1
2


Data Setup Part
3rd Page Data Setup
Repeatable
DQ[7:0]
R/B
80h
C1
C2
R1
R2
R3
W-Data
11h
81h
C0h
33h
1)
Plane 0
Plane 1
tADL
tWB
tDBSY
tDBSY2
2
3


Program Confirm Part
Repeatable
DQ[7:0]
R/B
8Bh
C1
C2
R1
R2
R3
11h
15h
Plane 0
Plane 1
tWB
tDBSY
tCBSY
3
4

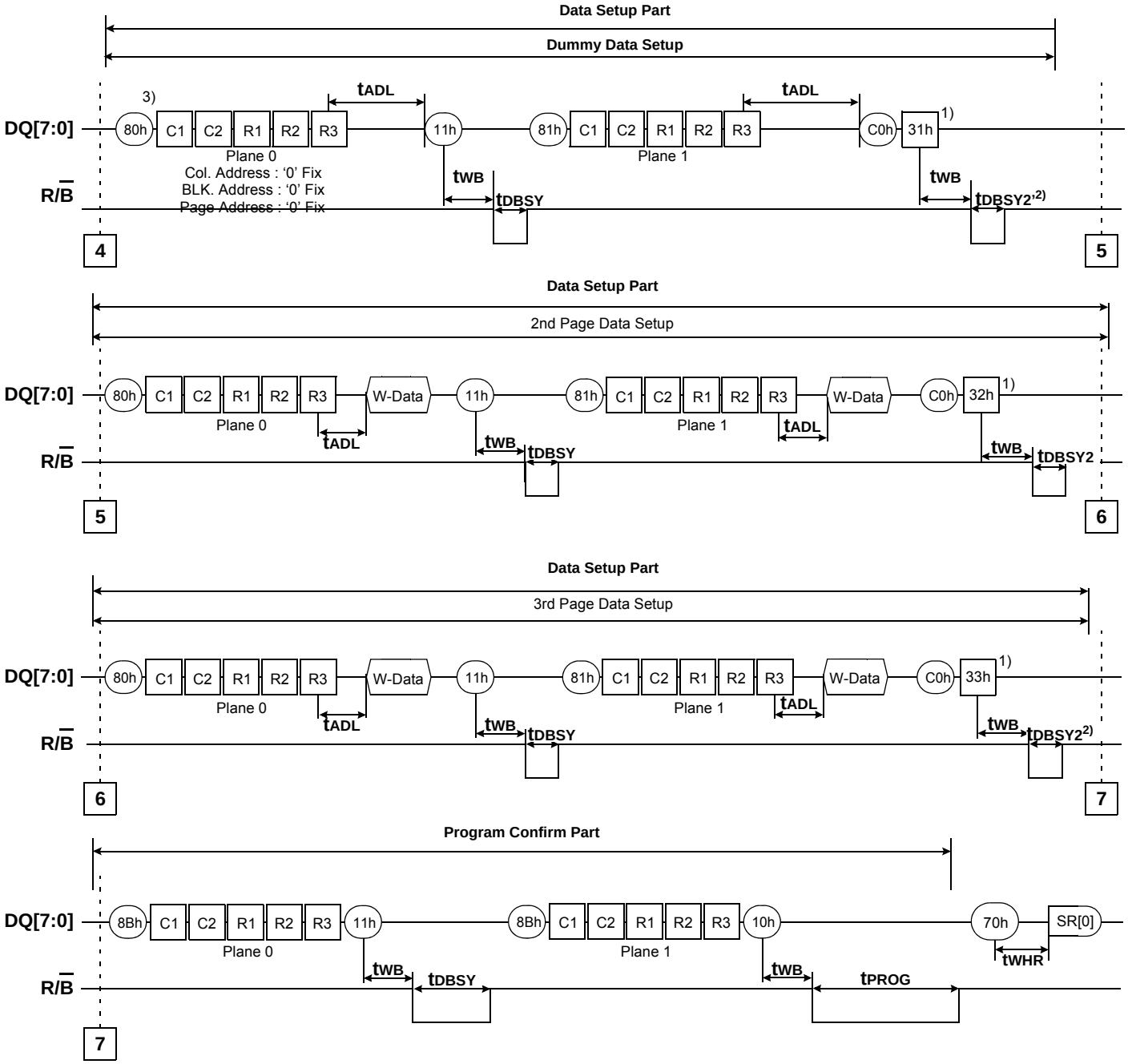


Figure 70. Example Sequence with Two-Plane Cache Program (Edge MLC)

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 31.
2) tDBSY2' = tCBSY (Dummy Busy time for Cache Program) + tDBSY2.
3) No actual data loading (page address, block address, column address "0" fix in dummy data setup.

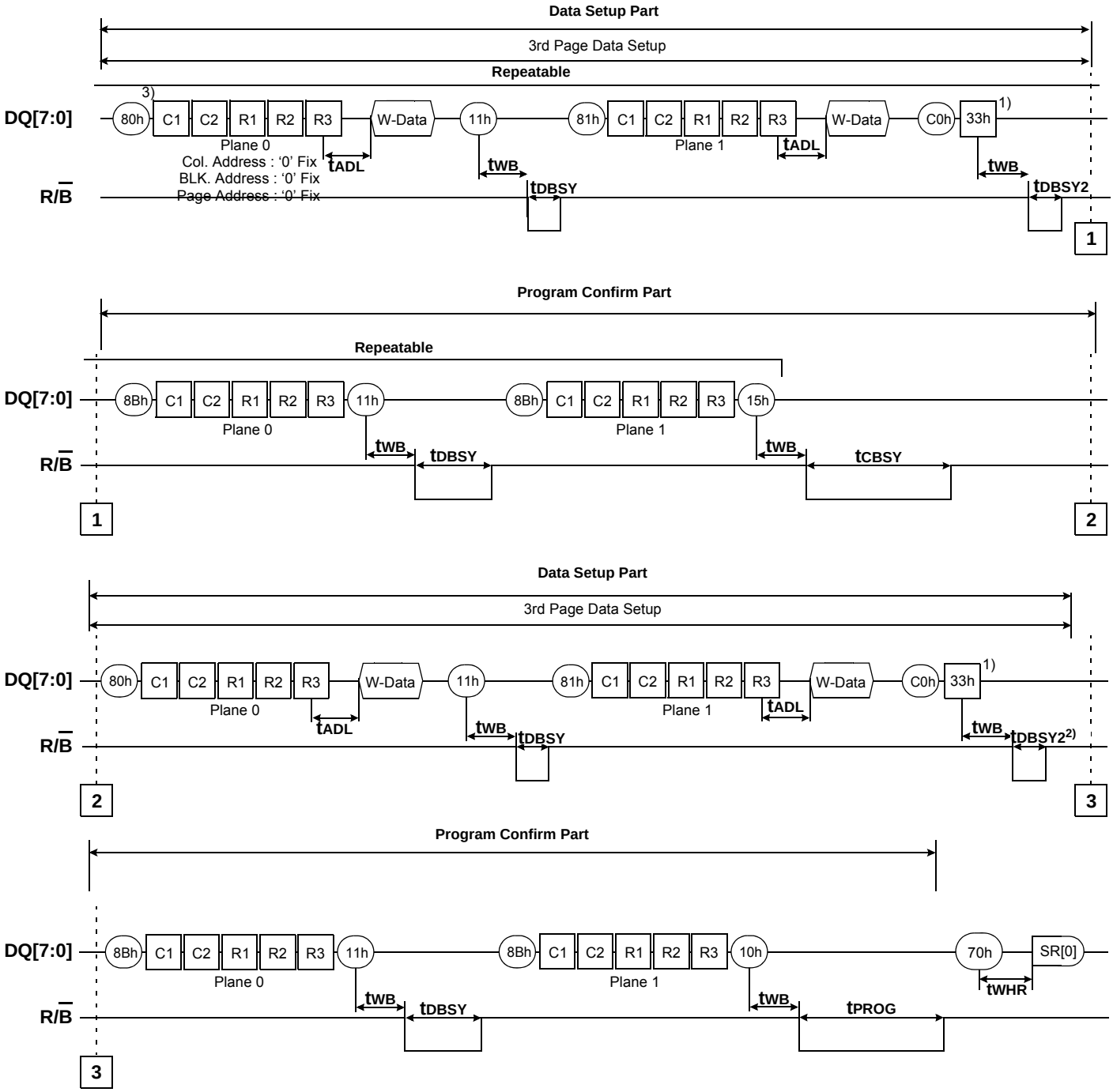


Figure 71. Example Sequence with Two-Plane Cache Program (Edge SLC)

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 31.
2) tDBSY2' = tCBSY (Dummy Busy time for Cache Program) + tDBSY2.

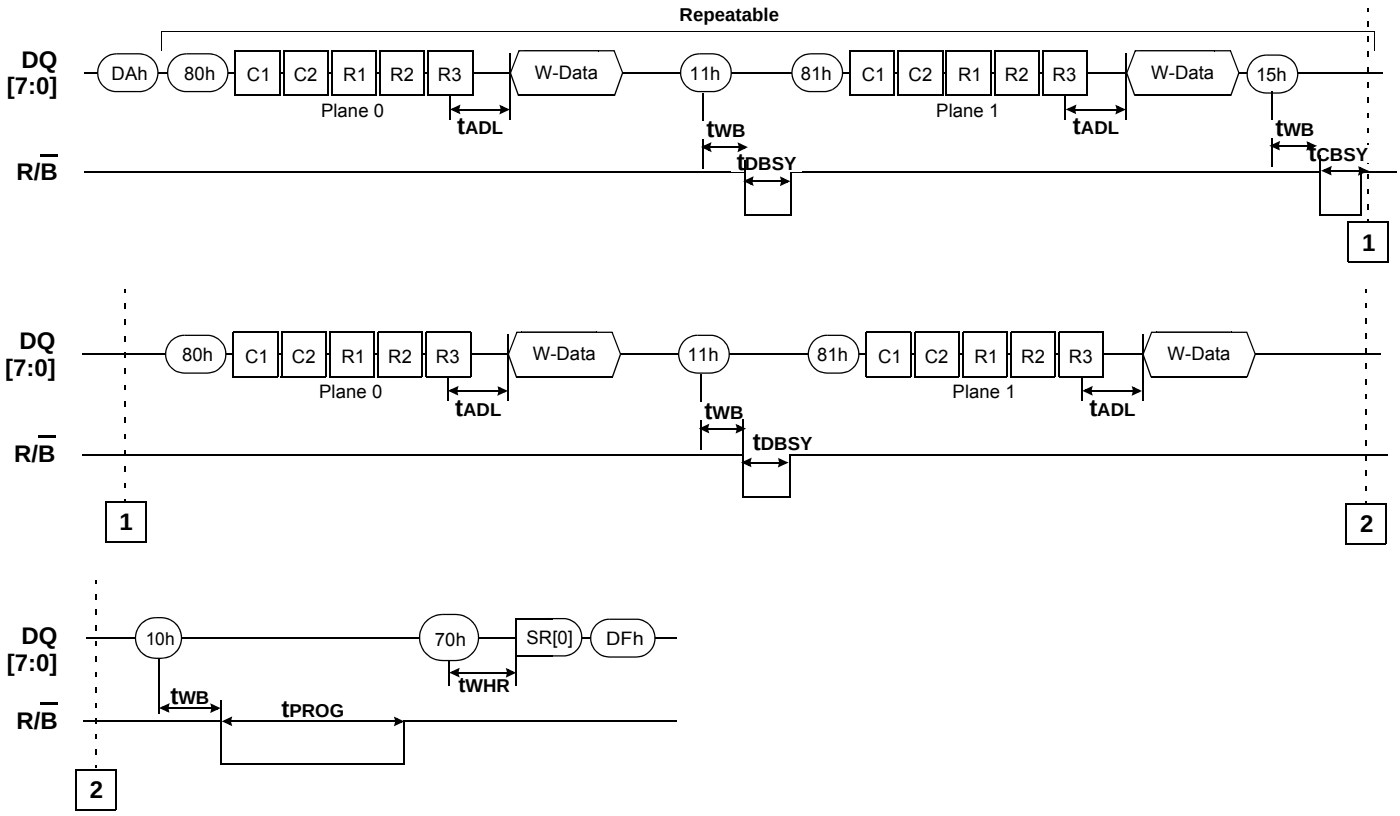


Figure 72. Example Sequence with Two-Plane Cache Program (SLC)

NOTE :
The first Raw Address (R1) is required to refer Program order address in Table 24.

5.3.8 16KB Two-Plane Random Cache Read Operation

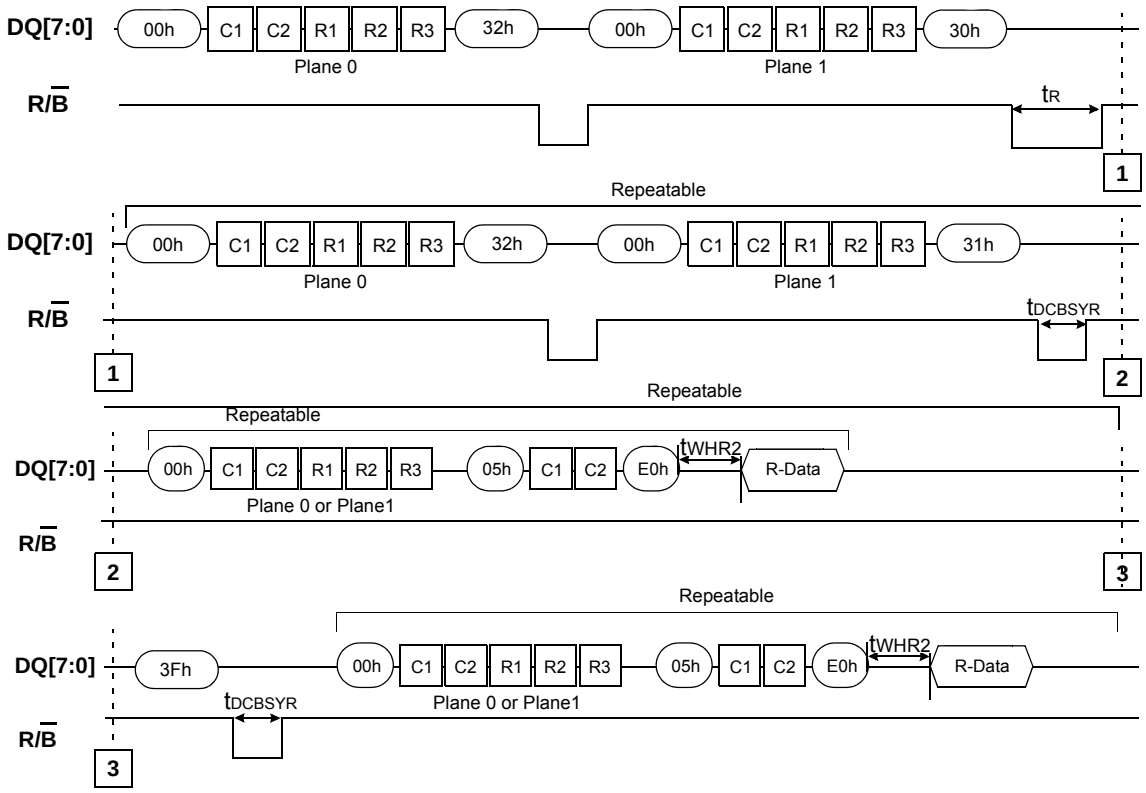


Figure 73. 16KB Two-Plane Random Cache Read

5.3.9 16KB Two-Plane Sequential Cache Read Operation

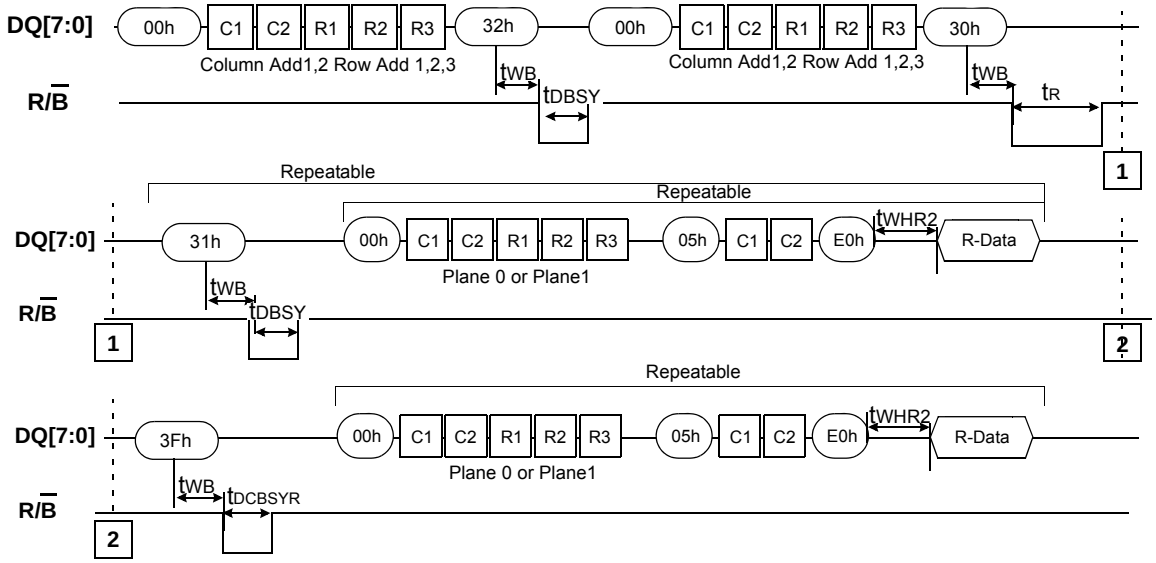
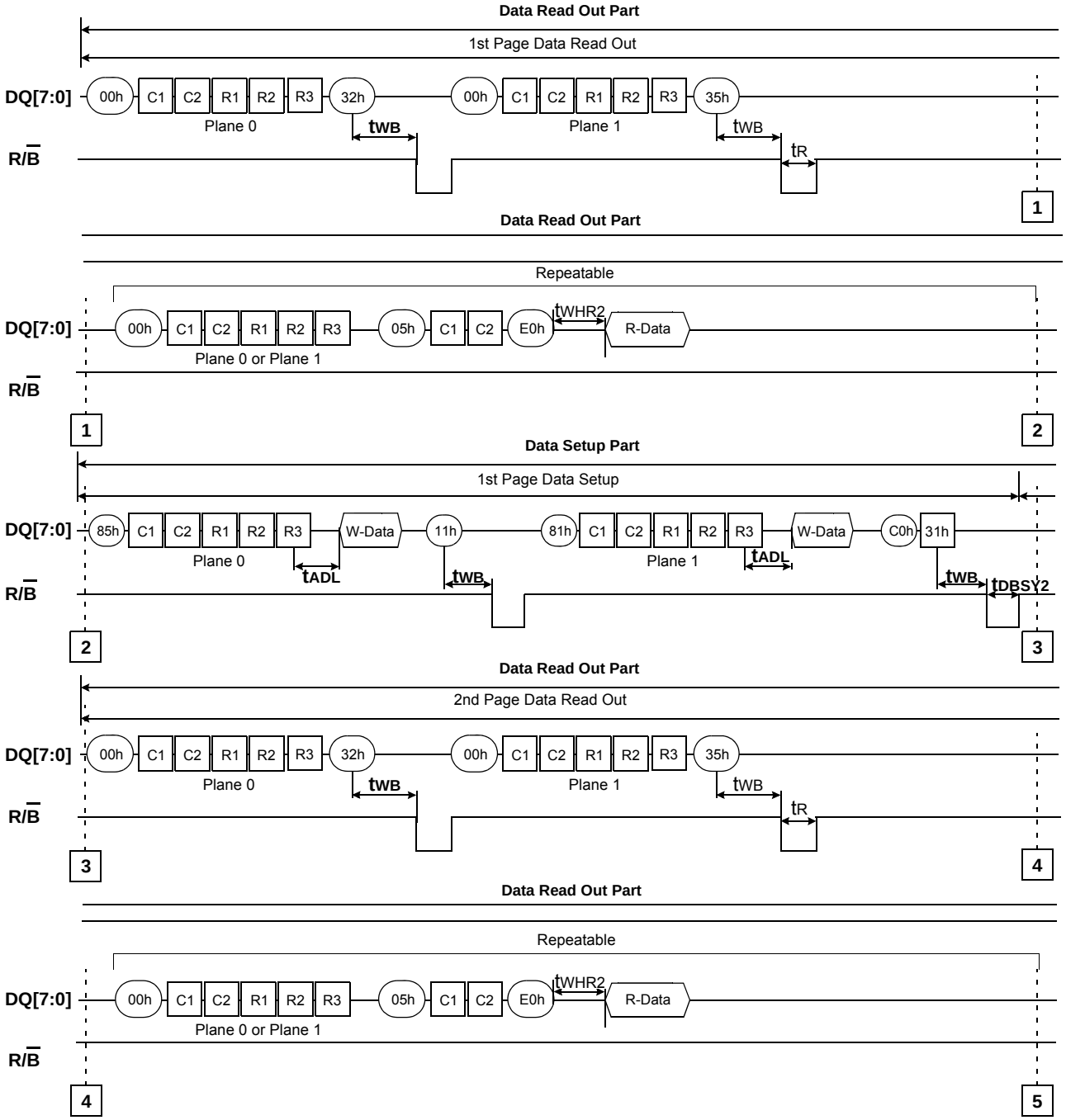


Figure 74. 16KB Two-Plane Sequential Cache Read

5.3.10 Two-Plane Copy-Back Program Operation



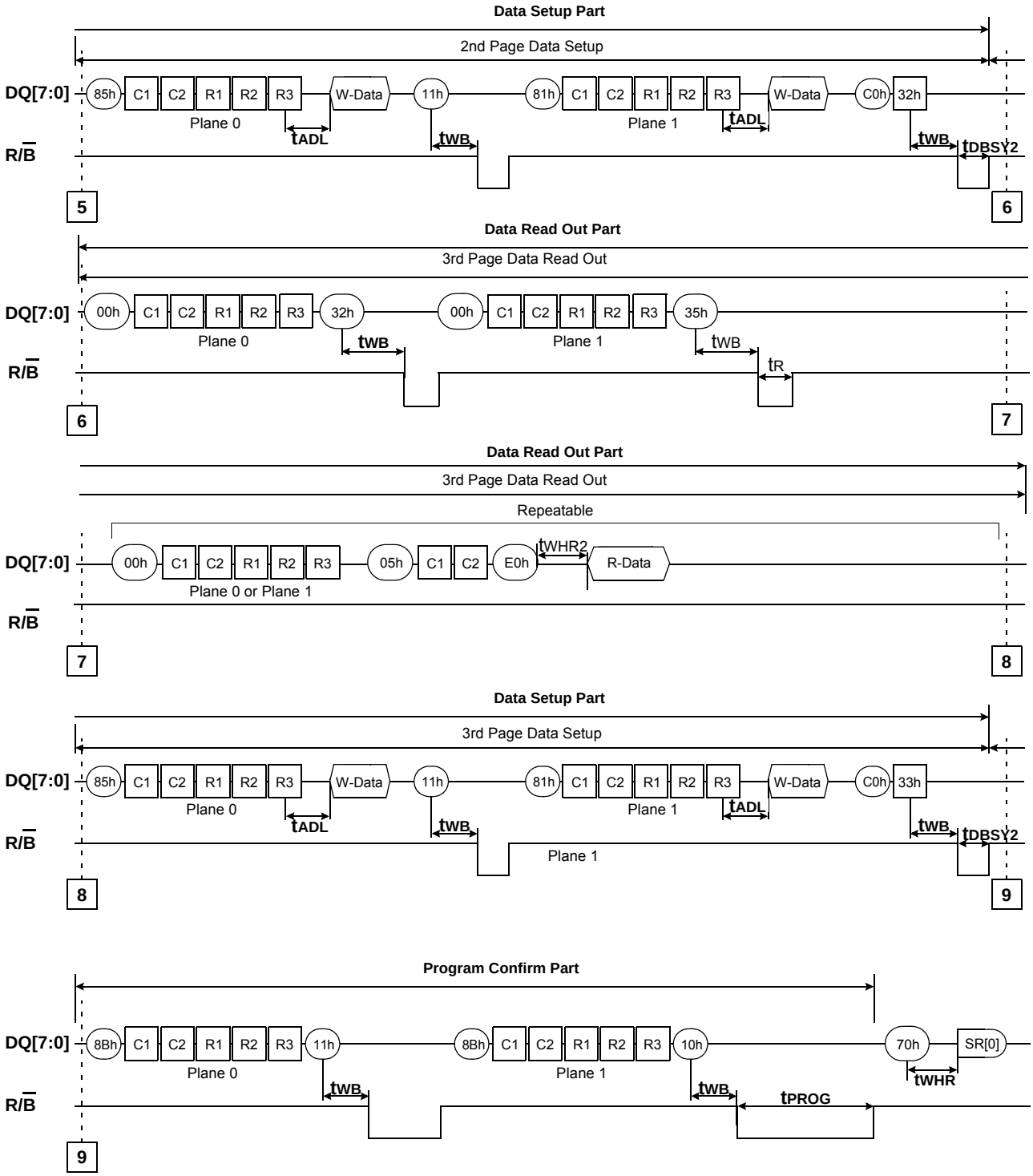
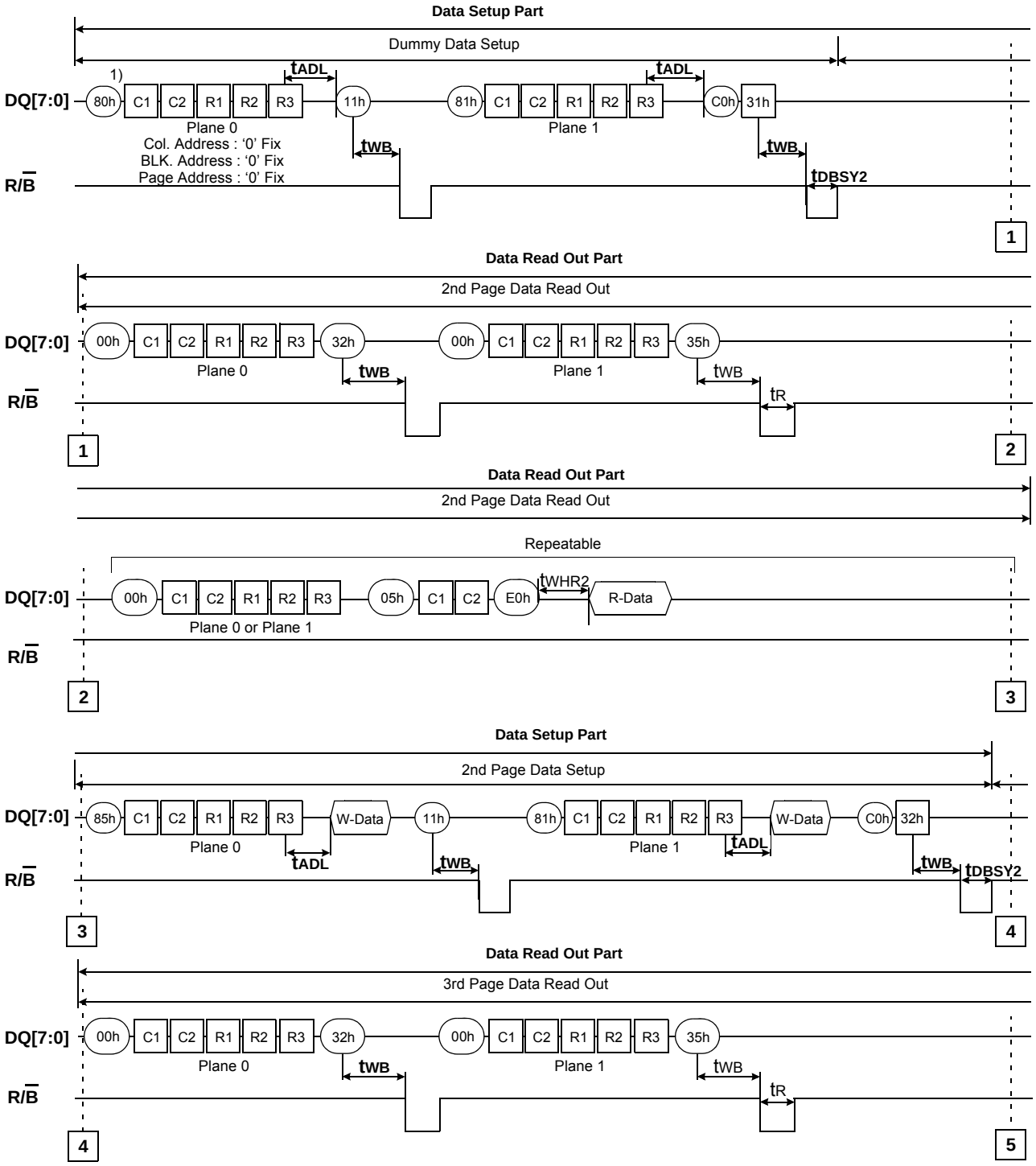


Figure 75. Example Sequence with Two-Plane Copy-Back Program (TLC)


Data Setup Part
Dummy Data Setup
1)
tADL
tADL
DQ[7:0]
80h
C1
C2
R1
R2
R3
11h
81h
C1
C2
R1
R2
R3
C0h
31h
Plane 0
Col. Address : '0' Fix
BLK. Address : '0' Fix
Page Address : '0' Fix
Plane 1
tWB
tWB
R/B
tDBSY2
1
Data Read Out Part
2nd Page Data Read Out
DQ[7:0]
00h
C1
C2
R1
R2
R3
32h
00h
C1
C2
R1
R2
R3
35h
Plane 0
tWB
Plane 1
tWB
R/B
tR
1
2
Data Read Out Part
2nd Page Data Read Out
Repeatable
DQ[7:0]
00h
C1
C2
R1
R2
R3
05h
C1
C2
E0h
tWHR2
R-Data
Plane 0 or Plane 1
R/B
2
3
Data Setup Part
2nd Page Data Setup
DQ[7:0]
85h
C1
C2
R1
R2
R3
W-Data
11h
81h
C1
C2
R1
R2
R3
W-Data
C0h
32h
Plane 0
tADL
tWB
Plane 1
tADL
tWB
tDBSY2
R/B
3
4
Data Read Out Part
3rd Page Data Read Out
DQ[7:0]
00h
C1
C2
R1
R2
R3
32h
00h
C1
C2
R1
R2
R3
35h
Plane 0
tWB
Plane 1
tWB
R/B
tR
4
5

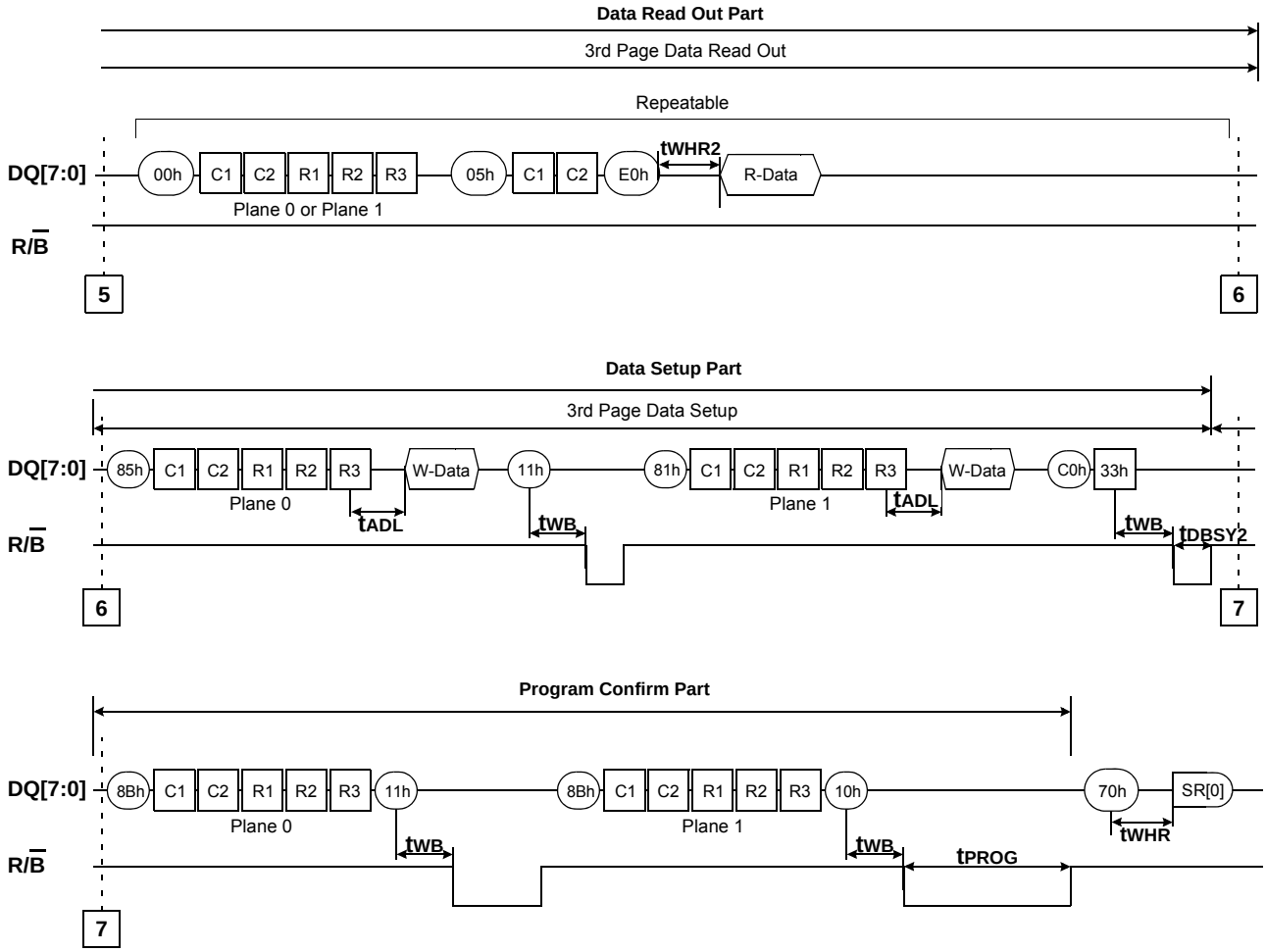


Figure 76. Example Sequence with Two-Plane Copy-Back Program (Edge MLC)

NOTE :
1) No actual data loading (page address, block address, column address "0" fix in dummy data setup.

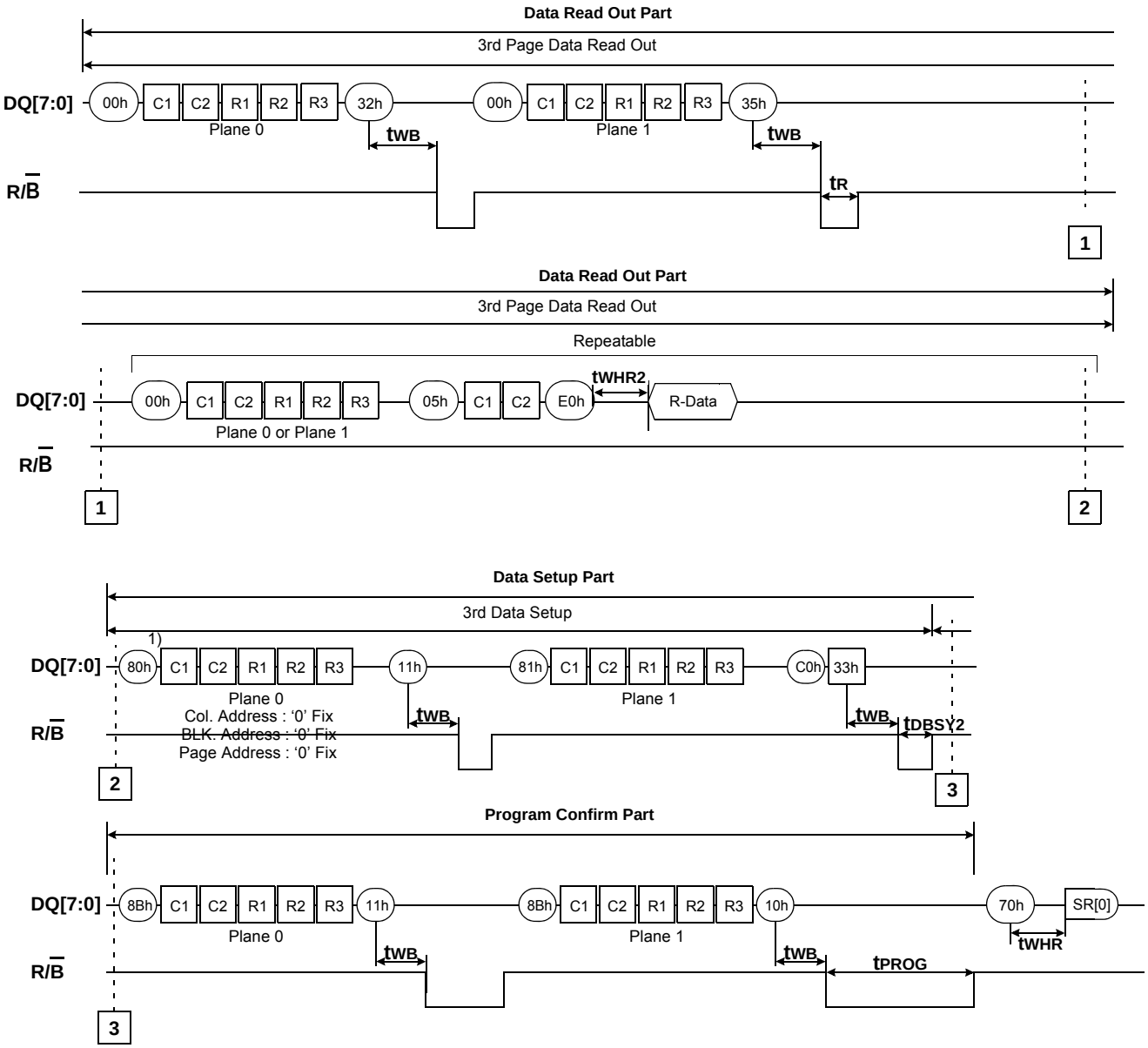


Figure 77. Example Sequence with Two-Plane Copy-Back Program (Edge SLC)

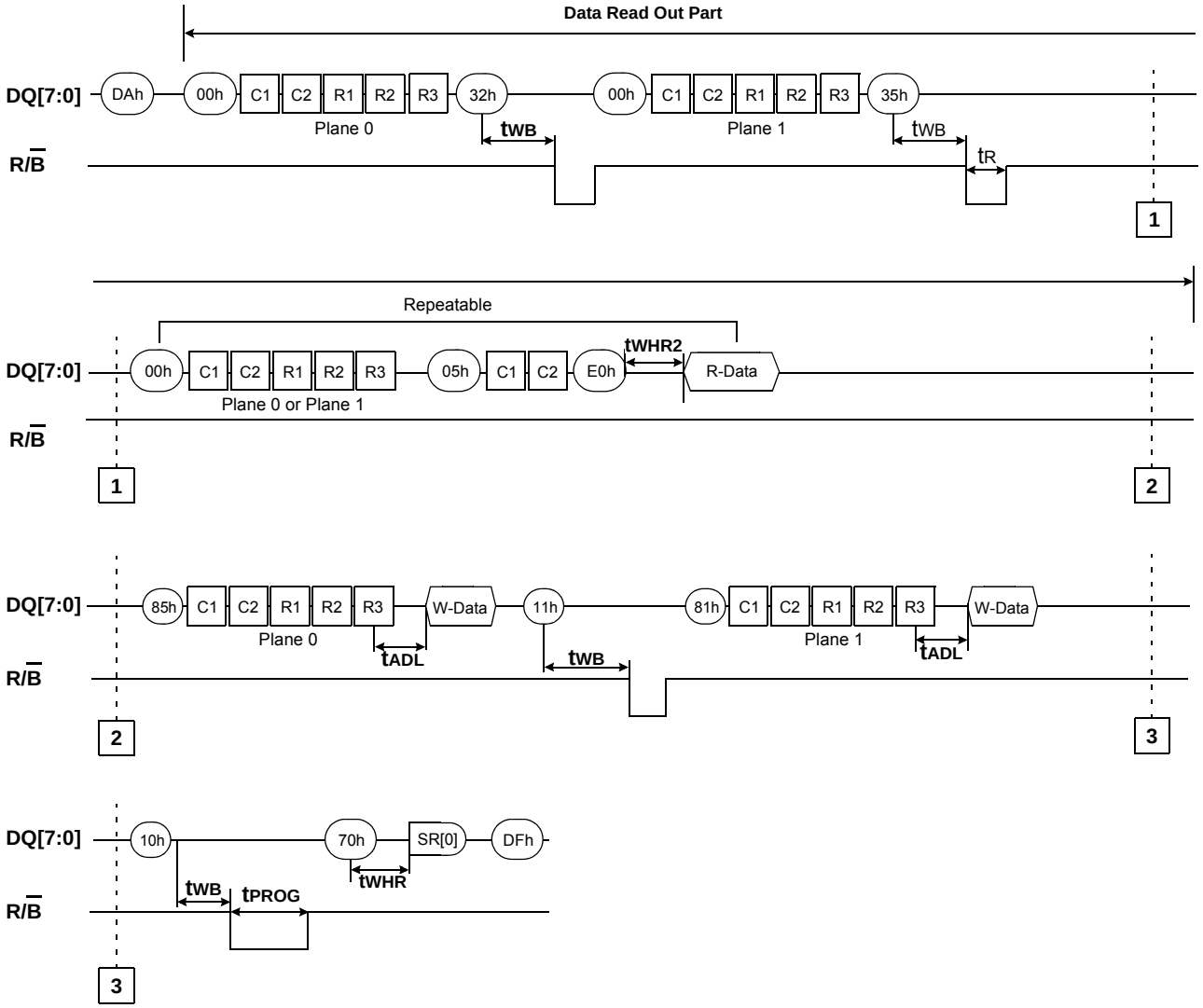


Figure 78. Example Sequence with Two-Plane Copy-Back Program (SLC)

5.3.11 Two-Plane Block Erase Operation

Two-Plane Block Erase allows users to erase multiple blocks comprising a block of each plane simultaneously.
The Two-Plane addresses shall be set in a consecutive manner from a lower address plane to a higher address plane and the same plane address shall not be set twice within a set of address setting sequence for the Two-Plane Block Erase Operation. Starting plane address shall be plane0. Figure 79 defines Two-Plane Block Erase behavior and timings.

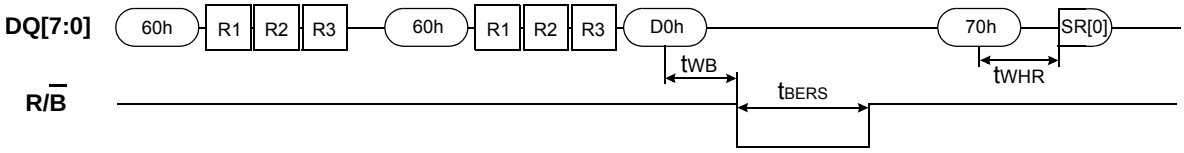


Figure 79. Example Sequence with Two-Plane Block Erase

5.3.12 Device Identification Table Read Operation

The device shall return a JEDEC standard formatted parameter page during the data out phase of the READ PARAMETER PAGE command when address 40h is inputted. The READ PARAMETER PAGE command is a ECh value for the command cycle and a 40h value for the address cycle, and the bytes of the parameter page are returned in the data output (DOUT) cycles.

After the command ECh address 40h is received by the NAND device, it will go busy for a period of time (tR in the figure) after which, the parameter page can be read from the device. The length and contents of the parameter page is to be determined. The timing associated with the bus cycles for the READ PARAMETER PAGE command is defined elsewhere in the JEDEC standard.

The Device Identification Table Read is used by the controller to identify the device that is attached. This command is used by the controller to gather information about the target flash device. Figure 80 defines the behavior and timings.

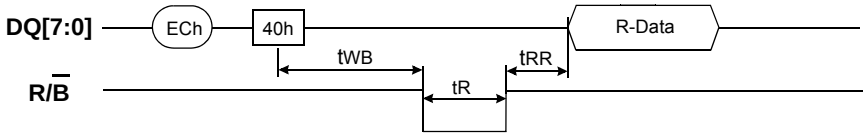


Figure 80. Device Identification Table Read Sequence

5.3.12.1 Device Identification Table Definition

Table 53 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.
Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the target will return how many data bytes are in a page.
All optional parameters that are not implemented shall be cleared to 00h by the target.

[Table 53] Parameter Page Definitions

Byte	O/M	Description
Revision information and features block		
0-3	M	Parameter page signature Byte 0: “J” (= 4Ah) Byte 1: “E” (= 45h) Byte 2: “S” (= 53h) Byte 3: “D” (= 44h)
4-5	M	Revision number 2-15: Reserved (0) 1: 1 = supports revision 1.0 0: Reserved (0)
6-7	M	Features supported 0-15 Reserved (0) <To be defined based on feature discussions.>
8-10	M	Optional commands supported 0-23: Reserved (0) <To be defined based on command set discussions.>
11-31		Reserved (0)
Manufacturer information block		
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64-69	M	JEDEC manufacturer ID (6 bytes)
70-71	TBD	TBD
72-79		Reserved (0)
Memory organization block		
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
TBD-TBD	TBD	TBD
Memory organization block		
101	M	Number of address cycles 4-7: Column address cycles 0-3: Row address cycles
102	M	Number of bits per cell
103	M	Number of programs per page
104	M	Multi-Plane addressing 4-7: Reserved (0) 0-3: Number of plane address bits
105	M	Multi-Plane operation attributes 3-7: Reserved (0) 2: Address restrictions for cache operations 1: 1= read cache supported 0: 1 = program cache supported
106-143		Reserved (0)
Electrical parameters block		

144	O	0:1 = supports 100ns speed grade(~10Mhz) 1:1 = supports 50ns speed grade(~20Mhz) 2:1 = supports 35ns speed grade(~28Mhz) 3:1 = supports 30ns speed grade(~33Mhz) 4:1 = supports 25ns speed grade(~40Mhz) 5:1 = supports 20ns speed grade(~50Mhz) 6:7 = Reserved
145	O	8-15 : Reserved(0)
146-147	O	Toggle DDR speed grade 10-15: Reserved (0) 9: 1 = supports 3 ns speed grade (~333 Mhz) 8: 1 = supports 3.75 ns speed grade (~266 Mhz) 7: 1 = supports 5 ns speed grade (~200 Mhz) 6: 1 = supports 6 ns speed grade (~166 Mhz) 5: 1 = supports 7.5 ns speed grade (~133 Mhz) 4: 1 = supports 10 ns speed grade (~100 Mhz) 3: 1 = supports 12 ns speed grade (~83 Mhz) 2: 1 = supports 15 ns speed grade (~66 Mhz) 1: 1 = supports 25 ns speed grade (40 Mhz) 0: 1 = supports 30 ns speed grade (~33 Mhz)
148-149	O	0-15: Reserved (0)
150	O	0:1 = supports 100ns speed grade(~10Mhz) 1:1 = supports 50ns speed grade(~20Mhz) 2:1 = supports 35ns speed grade(~28Mhz) 3:1 = supports 30ns speed grade(~33Mhz) 4:1 = supports 25ns speed grade(~40Mhz) 5:1 = supports 20ns speed grade(~50Mhz) 6:7= Reserved (0)
151	O	Toggle DDR features 0-7: Reserved (0)
152	O	0-7: Reserved (0)
153-154	M	tPROG Maximum page program time (µs)
155-156	M	tBERS Maximum block erase time (µs)
157-158	M	tR Maximum page read time (µs)
159-160	O	tR Maximum Multi-Plane page read time (µs)
161-162	O	tCCS Minimum change column setup time (ns)
163-164	M	I/O pin capacitance, typical
165-166	M	Input pin capacitance, typical
167-168	O	Reserved
169	M	Driver strength support 3-7: Reserved (0) 2: 1 = supports Overdrive 2 driver strength 1: 1 = supports Overdrive 1 driver strength 0: 1 = supports driver strength settings
170-207		Reserved (0)
ECC and endurance block		
208	M	Guaranteed valid blocks at beginning of target
209-210	M	Block endurance for guaranteed valid blocks
211-218	M	ECC and endurance information block 0 Byte 211: Number of bits ECC correctability Byte 212: Codeword size Byte 213-214: Bad blocks maximum per LUN Byte 215-216: Block endurance Byte 217-218: Reserved (0)
219-226	O	ECC and endurance information block 1 Byte 219: Number of bits ECC correctability Byte 220: Codeword size Byte 221-222: Bad blocks maximum per LUN Byte 223-224: Block endurance Byte 225-226: Reserved (0)

227-234	O	ECC and endurance information block 2 Byte 227: Number of bits ECC correctability Byte 228: Codeword size Byte 229-230: Bad blocks maximum per LUN Byte 231-232: Block endurance Byte 233-234: Reserved (0)
235-242	O	ECC and endurance information block 3 Byte 235: Number of bits ECC correctability Byte 236: Codeword size Byte 237-238: Bad blocks maximum per LUN Byte 239-240: Block endurance Byte 241-242: Reserved (0)
243-271	Reserved (0)	
Reserved		
272-419		Reserved (0)
Vendor specific block		
420-421	M	Vendor specific Revision number
422-509		Vendor specific
CRC for Parameter Page		
510-511	M	Integrity CRC
Redundant Parameter Pages		
512-1023		Value of bytes 0-511
1024-1535		Value of bytes 0-511
1536+		Additional redundant parameter pages

Byte 0-3: Parameter page signature
This field contains the parameter page signature.
When two or more bytes of the signature are valid, then it denotes that a valid copy of the parameter page is present.

Byte 0 shall be set to 4Ah.
Byte 1 shall be set to 45h.
Byte 2 shall be set to 53h.
Byte 3 shall be set to 44h.

Byte 4-5: Revision number
This field indicates the revisions of the standard that the target complies to.
The target may support multiple revisions of the standard.
This is a bit field where each defined bit corresponds to a particular specification revision that the target may support.

Bit 0 shall be cleared to zero.
Bit 1 when set to one indicates that the target supports revision 1.0.
Bits 2-15 are reserved and shall be cleared to zero.

Byte 6-7: Features supported
This field indicates the optional features that the target supports.

<TBD based on feature discussions.>

Byte 8-10: Optional commands supported
This field indicates the optional commands that the target supports.

<TBD based on command discussions.>

Byte 32-43: Device manufacturer
This field contains the manufacturer of the device.
The content of this field is an ASCII character string of twelve bytes.
The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

There is no standard for how the manufacturer represents their name in the ASCII string.
If the host requires use of a standard manufacturer ID, it should use the JEDEC manufacturer ID.

Byte 44-63: Device model
This field contains the model number of the device.
The content of this field is an ASCII character string of twenty bytes.
The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

Byte 64-69: JEDEC manufacturer ID
This field contains the JEDEC manufacturer ID for the manufacturer of the device.

Byte 70-71: TBD

Byte 80-83: Number of data bytes per page
This field contains the number of data bytes per page.
The value reported in this field shall be a power of two.
The minimum value that shall be reported is 512 bytes.

Byte 84-85: Number of spare bytes per page
This field contains the number of spare bytes per page. There are no restrictions on the value.

<TBD: Recommendations should be developed based on ECC strength needed.>

Byte 86-89: Number of data bytes per partial page
This field contains the number of data bytes per partial page.
The value reported in this field shall be a power of two.
The minimum value that shall be reported is 512 bytes.

Byte 90-91: Number of spare bytes per partial page
This field contains the number of spare bytes per partial page.
There are no restrictions on the value.

Byte 92-95: Number of pages per block
This field contains the number of pages per block.

<TBD: Should reference address format.>

Byte 96-99: Number of blocks per logical unit
This field contains the number of blocks per logical unit.
There are no restrictions on this value.

<TBD: Should reference address format.>

Byte 100: Number of logical units (LUNs)
This field indicates the number of logical units the target supports.
Logical unit numbers are sequential, beginning with a LUN address of 0.
This field shall be greater than zero.

<TBD: Should reference address format.>

Byte 101: Number of Address Cycles
This field indicates the number of address cycles used for row and column addresses.
The reported number of address cycles shall be used by the host in operations that require row and/or column addresses (e.g. Page Program).

Bits 0-3 indicate the number of address cycles used for the row address. This field shall be greater than zero.
Bits 4-7 indicate the number of address cycles used for the column address. This field shall be greater than zero.

NOTE :
Throughout this standard examples are shown with 2-byte column addresses and 3-byte row addresses. However, the host is responsible for providing the number of column and row address cycles in each of these sequences based on the values in this field.

Byte 102: Number of bits per cell
This field indicates the number of bits per cell in the Flash array.
This field shall be greater than zero.

Byte 103: Number of programs per page
This field indicates the maximum number of times a portion of a page may be programmed without an erase operation.
After the number of programming operations specified have been performed, the host shall issue an erase operation to that block before further program operations to the affected page.
This field shall be greater than zero.

Byte 104: Multi-Plane addressing
This field describes parameters for Multi-Plane addressing.
Bits 0-3 indicate the number of bits that are used for plane addresses.
This value shall be greater than 0h when Multi-Plane operations are supported.
Bits 4-7 are reserved.

Byte 105: Multi-Plane operation attributes
This field describes attributes for Multi-plane operations.
This byte is mandatory when Multi-plane operations are supported as indicated in the Features supported field.

Bit 0 indicates whether program cache is supported with Multi-plane programs.
If set to one then program cache is supported for Multi-plane program operations.
If cleared to zero then program cache is not supported for Multi-plane program operations.
Note that program cache shall not be used with Multi-plane copyback program operations.
See bit 2 for restrictions on the plane addresses that may be used.

Bit 1 indicates whether read cache is supported with Multi-plane reads.
If set to one then read cache is supported for Multi-plane read operations.
If cleared to zero then read cache is not supported for Multi-plane read operations.
Note that read cache shall not be used with Multi-plane copyback read operations.
Bit 2 indicates whether plane addresses may change during either:
a) a program cache sequence between 15h commands, or b) a read cache sequence between 31h commands.
If set to one and bit 0 is set to one, then the host may change the number and value of plane addresses in the program cache sequence.
If set to one and bit 1 is set to one, then the host may change the number and value of plane addresses in the read cache sequence.
If cleared to zero and bit 0 is set to one, then for each program cache operation the plane addresses and number of plane addresses issued to the LUN shall be the same.
If cleared to zero and bit 1 is set to one, then for each read cache operation the plane addresses and number of plane addresses issued to the LUN shall be the same.
Bits 3-7 are reserved.

Byte 144-145: Asynchronous SDR speed grade.
Bit 0 when set to one indicates that the target supports the 100 ns Asynchronous SDR speed grade (~10 MHz).
Bit 1 when set to one indicates that the target supports the 50 ns Asynchronous SDR speed grade (~20 MHz).
Bit 2 when set to one indicates that the target supports the 35 ns Asynchronous SDR speed grade (~28 MHz).
Bit 3 when set to one indicates that the target supports the 30 ns Asynchronous SDR speed grade (~33 MHz).
Bit 4 when set to one indicates that the target supports the 25 ns Asynchronous SDR speed grade (~40 MHz).
Bit 5 when set to one indicates that the target supports the 20 ns Asynchronous SDR speed grade (~50 MHz).
Bits 6-15 are reserved.

Byte 146-147: Toggle DDR speed grade
This field indicates the Toggle DDR speed grades supported. The target shall support an inclusive range of speed grades.

Bit 0 when set to one indicates that the target supports the 30 ns speed grade (~33 MHz).
Bit 1 when set to one indicates that the target supports the 25 ns speed grade (40 MHz).
Bit 2 when set to one indicates that the target supports the 15 ns speed grade (~66 MHz).
Bit 3 when set to one indicates that the target supports the 12 ns speed grade (~83 MHz).
Bit 4 when set to one indicates that the target supports the 10 ns speed grade (~100 MHz).
Bit 5 when set to one indicates that the target supports the 7.5 ns speed grade (~133 MHz).
Bit 6 when set to one indicates that the target supports the 6 ns speed grade (~166 MHz).
Bit 7 when set to one indicates that the target supports the 5 ns speed grade (~200 MHz).
Bit 8 when set to one indicates that the target supports the 3.75 ns speed grade (~266 MHz).
Bit 9 when set to one indicates that the target supports the 3 ns speed grade (~333 MHz).
Bits 10-15 are reserved and shall be cleared to zero.

Byte 148-149: Reserved

Byte 150: Asynchronous SDR speed grade.
Bit 0 when set to one indicates that the target supports the 100 ns Asynchronous SDR speed grade (~10 MHz).
Bit 1 when set to one indicates that the target supports the 50 ns Asynchronous SDR speed grade (~20 MHz).
Bit 2 when set to one indicates that the target supports the 35 ns Asynchronous SDR speed grade (~28 MHz).
Bit 3 when set to one indicates that the target supports the 30 ns Asynchronous SDR speed grade (~33 MHz).
Bit 4 when set to one indicates that the target supports the 25 ns Asynchronous SDR speed grade (~40 MHz).
Bit 5 when set to one indicates that the target supports the 20 ns Asynchronous SDR speed grade (~50 MHz).
Bits 6-7 are reserved.

Byte 151: Toggle DDR features
This field describes features and attributes for Toggle DDR operation.
This byte is mandatory when the Toggle DDR data interface is supported.
Bits 0-7 are reserved.

Byte 152: Reserved

Byte 153-154: Maximum page program time
This field indicates the maximum page program time (tPROG) in microseconds.
Byte 155-156: Maximum block erase time
This field indicates the maximum block erase time (tBERS) in microseconds.

Byte 157-158: Maximum page read time
This field indicates the maximum page read time (tR) in microseconds.

Byte 159-160: Maximum Two-Plane page read time
This field indicates the maximum page read time (tR) for Two-Plane page reads in microseconds.
Two-Plane page read times may be longer than single page read times.
This field shall be supported if the target supports Two-Plane reads as indicated in the Features supported field.

Byte 161-162: Minimum change column setup time.
This field indicates the minimum change column setup time (tCCS) in nanoseconds.
This parameter is used for the asynchronous SDR and synchronous DDR data interfaces.

After issuing a Change Read Column command, the host shall not read data until a minimum of tCCS time has elapsed.
After issuing a Change Write Column command including all column address cycles, the host shall not write data until a minimum of tCCS time has elapsed.
The value of tCCS shall always be longer than or equal to tWHR and tADL when the Toggle DDR or synchronous DDR data interface is supported.

Byte 163-164: I/O pin capacitance, typical
This field indicates the typical I/O pin capacitance for the target. This field is specified in 0.1 pF units.
For example, a value of 31 corresponds to 3.1 pF.
The variance from this value is less than +/- 0.5 pF per LUN. As an example, if two LUNs are present than the total variance is less than +/- 1 pF.

Byte 165-166: Input pin capacitance, typical
This field indicates the typical input pin capacitance for the target.
This value applies to all inputs except the following: $\overline{CE}$ and $\overline{WP}$ signals.
This field is specified in 0.1 pF units. For example, a value of 31 corresponds to 3.1 pF.
The variance from this value is less than +/- 0.5 pF per LUN.
As an example, if two LUNs are present than the total variance is less than +/- 1 pF.

Byte 167-168: Reserved

Byte 169: Driver strength support
This field describes if the target supports configurable driver strengths and its associated features.

Bit 0 when set to one indicates that the target supports configurable driver strength settings as defined in Table TBD.
If this bit is set to one, then the device shall support both the Nominal and Underdrive settings.
If this bit is set to one, then the device shall power-on with a driver strength at the Nominal value defined in Table TBD.

If this bit is cleared to zero, then the driver strength at power-on is undefined.
This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.

Bit 1 when set to one indicates that the target supports the Overdrive 1 setting in Table TBD for use in the I/O Driver Strength setting.
This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.

Bit 2 when set to one indicates that the target supports the Overdrive 2 setting in Table TBD for use in the I/O Driver Strength setting.
This bit shall be set to one for devices that support the synchronous DDR or Toggle DDR data interface.
Bits 3-7 are reserved.

Byte 208: Guaranteed valid blocks at beginning of target
This field indicates the number of guaranteed valid blocks starting at block address 0 of the target.
The minimum value for this field is 1h.
The blocks are guaranteed to be valid for the endurance specified for this area when the host follows the specified number of bits to correct in ECC information block 0.

Byte 209-210: Block endurance for guaranteed valid blocks
This field indicates the minimum number of program/erase cycles per addressable page/block in the guaranteed valid block area.
This value requires that the host is using at least the minimum ECC correctability reported in ECC information block 0. This value is not encoded.
If the value is 0000h, then no minimum number of cycles is specified, though the block(s) are guaranteed valid from the factory.

Byte 211-218: ECC information block 0
This block of parameters describes a set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.

Byte 211: Number of bits ECC correctability.
This field indicates the number of bits that the host should be able to correct per codeword.
The codeword size is reported in byte 212. With this specified amount of error correction by the host, the target shall achieve the block endurance specified in bytes 215-216.
When the specified amount of error correction is applied by the host and the block endurance is followed, then the maximum number of bad blocks specified in bytes 213-214 shall not be exceeded by the device.
All used bytes in the page shall be protected by ECC including the spare bytes if the ECC requirement reported in byte 211 has a value greater than zero. When this value is cleared to zero, the target shall return valid data.

Byte 212: Codeword size. The number of bits of ECC correctability specified in byte 211 is based on a particular ECC codeword size.
The ECC codeword size is specified in this field as a power of two.
The minimum value that shall be reported is 512 bytes (a value of 9).

Byte 213-214: Bad blocks maximum per LUN.
This field contains the maximum number of blocks that may be defective at manufacture and over the life of the device per LUN.
The maximum rating assumes that the host is following the block endurance requirements and the ECC requirements reported in this ECC and endurance information block.

Byte 215-216: Block endurance.
This field indicates the maximum number of program/erase cycles per addressable page/block.
This value assumes that the host is using the ECC correctability reported in byte 211.
The block endurance is reported in terms of a value and a multiplier according to the following equation: value x $10^{multiplier}$. Byte 215 comprises the value. Byte 216 comprises the multiplier.
For example, a block endurance of 75,000 cycles would be reported as a value of 75 and a multiplier of 3 (75 x 10^3).
The value field shall be the smallest possible; for example 100,000 shall be reported as a value of 1 and a multiplier of 5 (1 x 10^5).

Byte 219-226: ECC information block 1
This block of parameters describes an additional set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.
The layout is and definition for this block is equivalent to ECC information block 0.
If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 227-234: ECC information block 2
This block of parameters describes an additional set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.
The layout is and definition for this block is equivalent to ECC information block 0.
If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 235-242: ECC information block 3
This block of parameters describes an additional set of ECC and endurance information.
The parameters are related, and thus the parameters are specified as a set.
The layout is and definition for this block is equivalent to ECC information block 0.
If this set of parameter is not specified, the block shall be cleared to 0h.

Byte 420-421: Vendor specific Revision number
This field indicates a vendor specific revision number.
This field should be used by vendors to indicate the supported layout for the vendor specific parameter page area and the vendor specific feature addresses. The format of this field is vendor specific.

Byte 422-509: Vendor specific
This field is reserved for vendor specific use.

Byte 510-511: Integrity CRC
The Integrity CRC (Cyclic Redundancy Check) field is used to verify that the contents of the parameter page were transferred correctly to the host.
The CRC of the parameter page is a word (16-bit) field. The CRC calculation covers all of data between byte 0 and byte 509 of the parameter page inclusive.
The CRC shall be calculated on byte (8-bit) quantities starting with byte 0 in the parameter page.
The bits in the 8-bit quantity are processed from the most significant bit (bit 7) to the least significant bit (bit 0).

The CRC shall be calculated using the following 16-bit generator polynomial:
G(X) = X16 + X15 + X2 + 1
This polynomial in hex may be represented as 8005h.

The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Byte 512-1023: Redundant Parameter Page 1
This field shall contain the values of bytes 0-511 of the parameter page. Byte 512 is the value of byte 0.
The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-511. The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

Byte 1024-1535: Redundant Parameter Page 2
This field shall contain the values of bytes 0-511 of the parameter page. Byte 1024 is the value of byte 0.

The redundant parameter page is used when the integrity CRC indicates that there was an error in bytes 0-511 and in the first redundant parameter page.
The redundant parameter page shall be stored in non-volatile media; the target shall not create these bytes by retransmitting the first 512 bytes.

Byte 1536+: Additional Redundant Parameter Pages
Bytes at offset 1536 and above may contain additional redundant copies of the parameter page.
There is no limit to the number of redundant parameter pages that the target may provide.
The target may provide additional copies to guard against the case where all three mandatory copies have invalid CRC checks.

The host should determine whether an additional parameter page is present by checking the first Dword.
If at least two out of four bytes match the parameter page signature, then an additional parameter page is present.

5.3.13 Read Status Enhanced

Read Status Enhanced function is used to check status of selected plane of a LUN. Thus, the function requires row address setting steps before reading status value. Table 54 defines status values of each operation and Figure 81 defines Read Status Enhanced behavior and timings.

[Table 54] Read Status Enhanced Definition

	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7
Definition of value	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Pass : "0" Fail : "1"	Reserved	Busy : "0" Ready : "1"	Busy : "0" Ready : "1"	Protected : "0" Not Protected : "1"
Block Erase	Pass/Fail	Not Use	Pass/Fail	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Page Program	Pass/Fail	Not Use	Pass/Fail	Not Use	Not Use	Not Use	Ready/Busy	Write Protect
Cache Program	Pass/Fail for the current page	Pass/Fail for the previous page	Pass/Fail for the current page	Pass/Fail for the previous page	Not Use	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect
Read	Not Use	Not Use	Not Use	Not Use	Not Use	Not Ready for New Command[1]: '0' Ready For New command[1]: '1'	Ready/Busy	Write Protect
Cache Read	Not Use	Not Use	Not Use	Not Use	Not Use	Busy/Ready for Flash array	Ready/Busy for Host	Write Protect

NOTE :
DQ0 & DQ1 provides status of plane selected. DQ2 & DQ3 provides LUN(Chip) status for Block Erase, Page Program and Cache Program.
1) New Commands are allowable command referring to NOTE2 of Table 30.

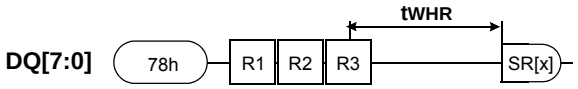


Figure 81. Read Status Sequence

5.3.14 Register Read Out Mode 1

At program operation, loaded data to the register can be read out before program confirm command(10h). The sequence is as follows. To continue program operation after reading data, Copy-back Program operation (i.e. 85h- Address(5cycle) - Data - 10h) is required.

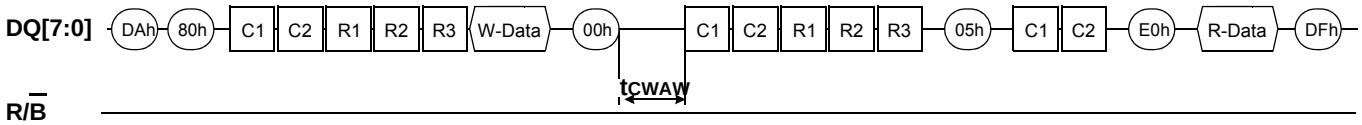


Figure 82. Register Read Out with SLC Operation

NOTE :
Register read out operation is prohibited during cache program operation.

5.3.15 Register Read Out Mode 2

At program operation, loaded data to the register can be read out before page buffer latch dump command(C0h) during data setup part. The sequence is as follows. To continue program operation after reading data, 85h- Address(5cycle) - Data - C0h - Address(1cycle) and insert next program command sequence is required.

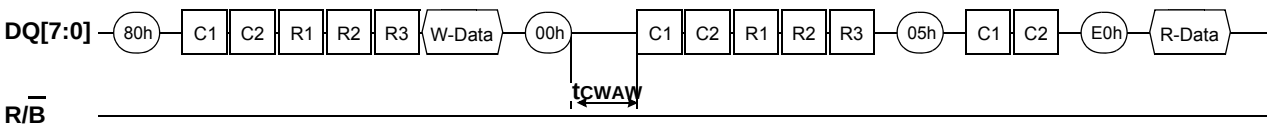


Figure 83. Register Read Out with TLC Operation

NOTE :
Register read out operation is prohibited during cache program operation.

5.3.16 Two-Plane Register Read Out Mode 1

At Two-Plane program operation, loaded data to the register can be read out before program confirm command(10h). The sequence is as follows.To continue Two-Plane program operation after reading data, Two-Plane Random Data Copy-back Program sequence is required.

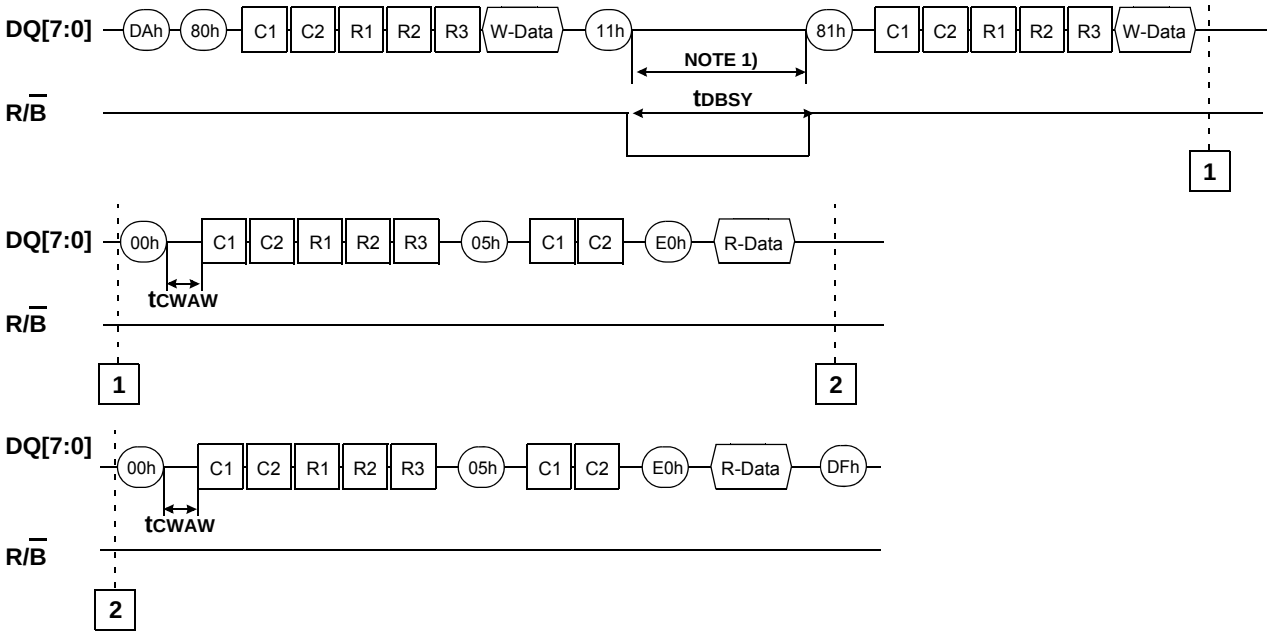


Figure 84. Two-Plane Register Read Out Mode with SLC Operation

NOTE :
1) Any command between 11h and 81h is prohibited except 70h/78h and FFh and FAh.
2) Register read out operation is prohibited during cache program operation.

5.3.17 Two-Plane Register Read Out Mode 2

At Two-Plane program operation, loaded data to the register can be read out before page buffer latch dump command(C0h) during data setup part. The sequence is as follows.To continue Two-Plane program operation after reading data, 85h- Address(5cycle) - Data - 11h- 81h - Address(5cycle) - Data - C0h - Address(1cycle) and insert next program command sequence is required.

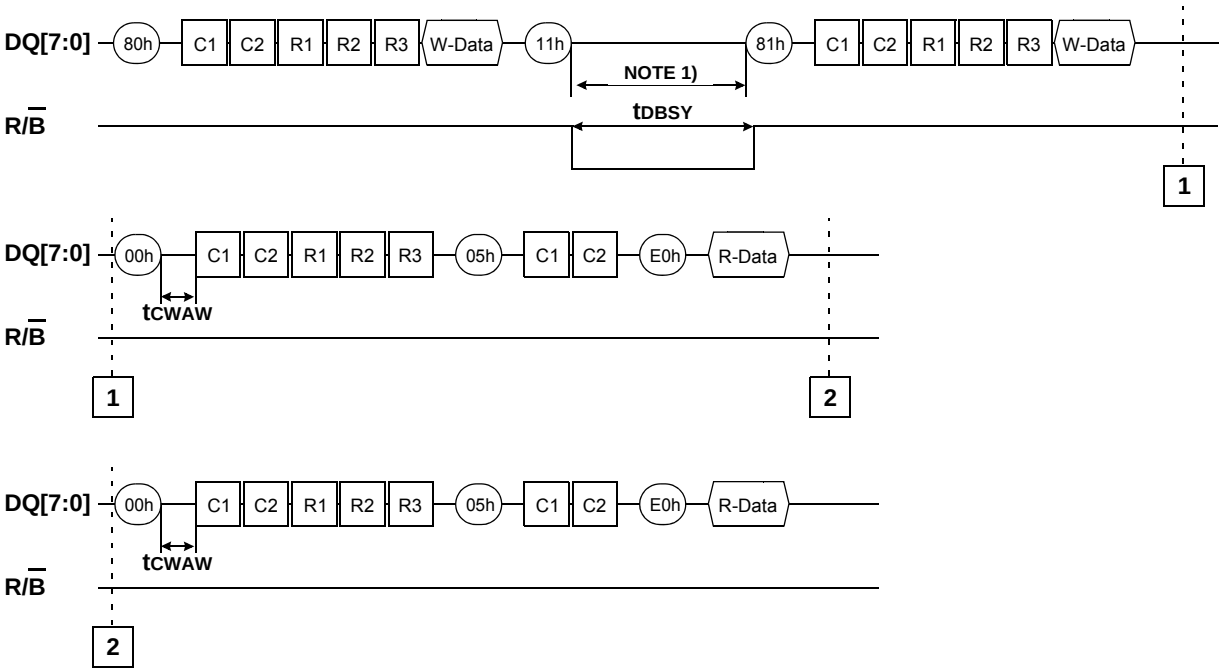


Figure 85. Two-Plane Register Read Out Mode with TLC Operation

NOTE :
1) Any command between 11h and 81h is prohibited except 70h/78h and FFh and FAh.
2) Register read out operation is prohibited during cache program operation.

5.4 Interleaving Operation

When multiple LUNs share a common $\overline{CE}$, it provides interleaving operation between LUNs.

At first, the host issues a operation command to one of the LSB chips, say (LUN #0). Due to DDP device goes into busy state. During this time, MSB chip (LUN #1) is in ready state. So it can execute the operation command issued by the host.

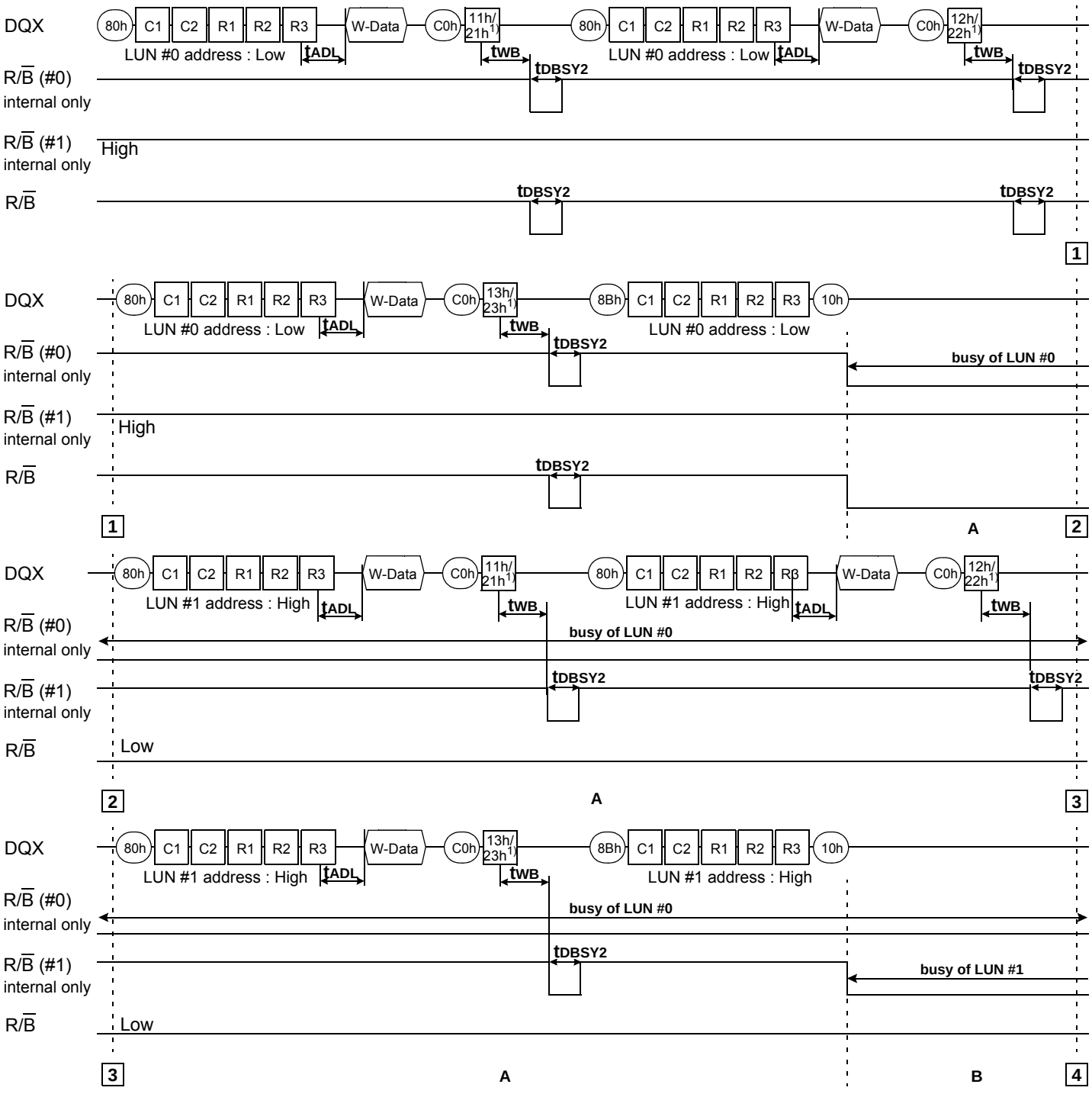
After the execution of operation by LSB chip (LUN #0), it can execute another operation regardless of MSB chip (LUN #1). Before that the host needs to check the status of LSB chip (LUN #0) by issuing 78h command. Only when the status of LSB chip (LUN #0) becomes ready status, host can issue another operation command. If LSB chip (LUN #0) is in busy state, the host has to wait for LSB chip (LUN #0) to get into ready state.

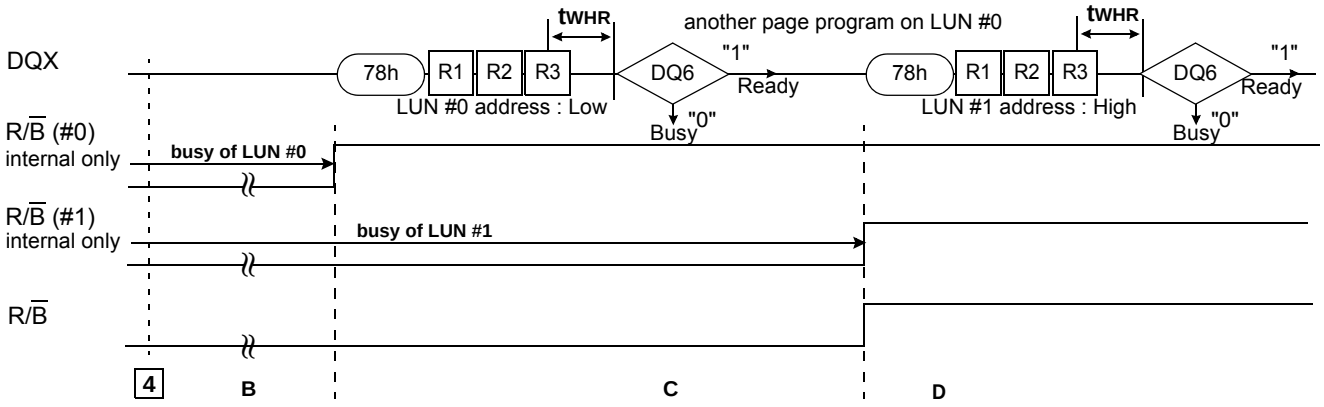
Similarly, MSB chip (LUN #1) can execute another operation after the completion of the previous operation. The host can monitor the status of MSB chip (LUN #1) by issuing 78h command. When MSB chip (LUN #1) goes ready state, host can issue another operation command to MSB chip (LUN #1).

This interleaving operation helps the system improve the system throughput.

NOTE :
During interleave operations, 70h command is prohibited and 78h command is used to check the status.
Interleaving operation must be executed between the blocks in the same status. It means that TLC to SLC and SLC to TLC interleaving operations are prohibited.

5.4.1 Interleaving Page Program Operation



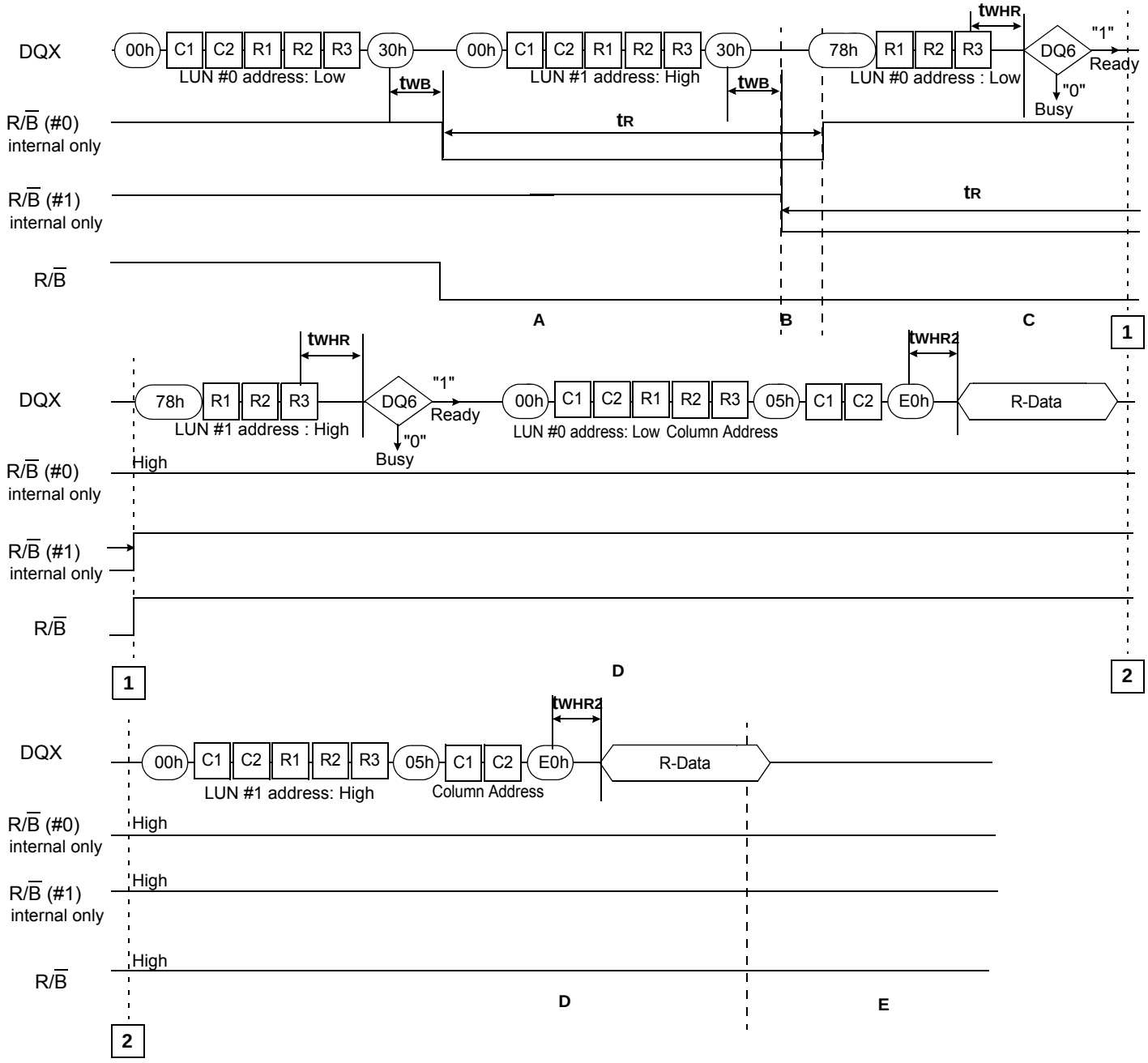


State A : LUN #0 is executing page program operation and LUN #1 is in ready state. So the host can issue page program command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing page program operation.
State C : Page program on LUN #0 is completed, but page program on LUN #1 is still ongoing. And the system should issue 78h command to detect the status of LUN #0. If LUN #0 is ready, status I/O6 is "1" and the system can issue another page program command to LUN #0.
State D : Both of LUN #0 and LUN #1 are ready.

Depending on the above process, the system can operate page program on LUN #0 and LUN #1 alternately.

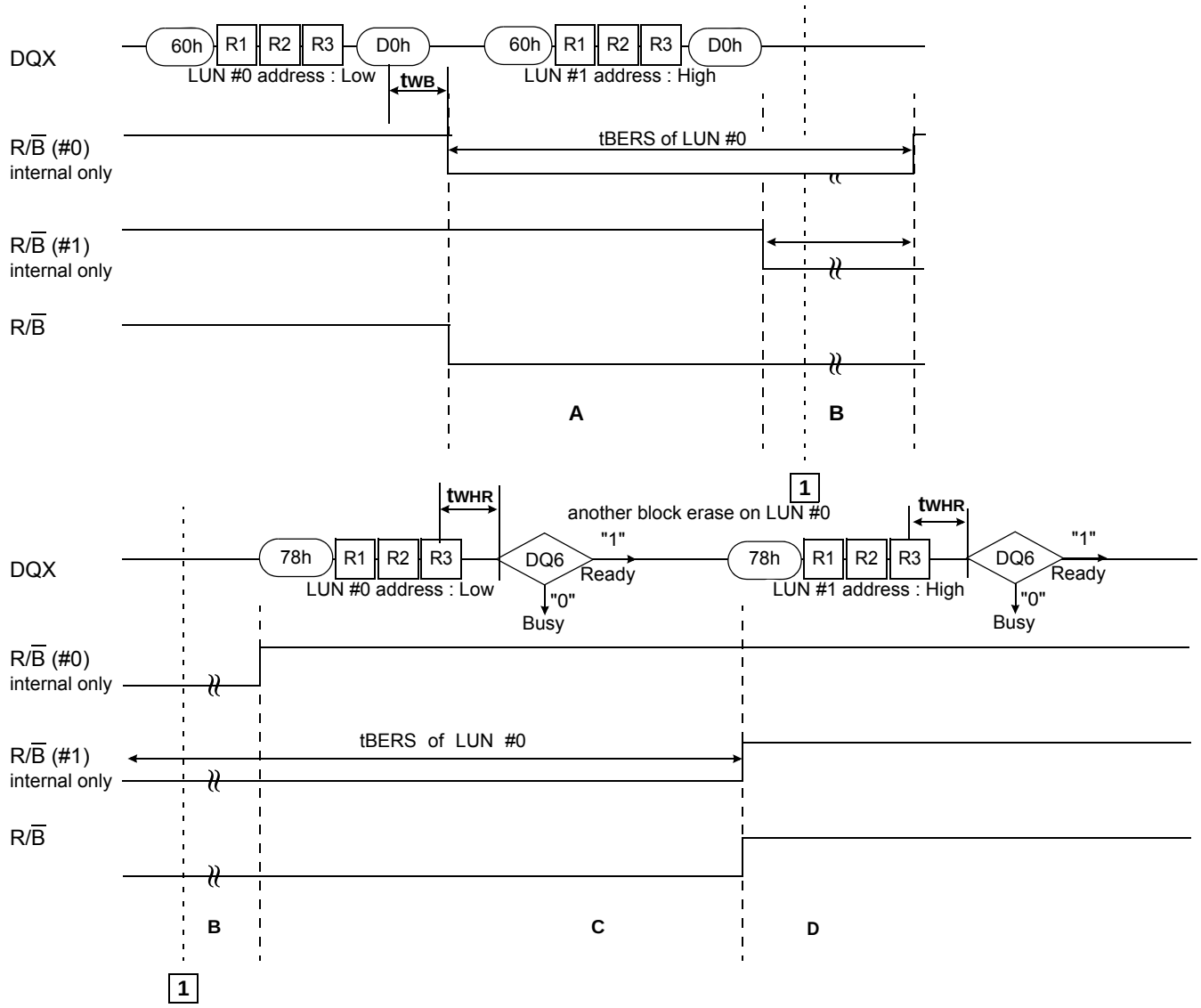
NOTE :
1) For address followed by C0h command, refer to the buffer address Table 31.

5.4.2 Interleaving Page Read Operation



State A : LUN #0 is executing page read operation, and LUN #1 is in ready state. So the host can issue page read command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing page read operation.
State C : Page read on LUN #0 is completed and LUN #1 is still executing page read operation.
State D : Before the host read the data, the host should check the Ready/Busy status for both LUNs by 78h commands.
State E : LUN #0 and LUN #1 are ready.

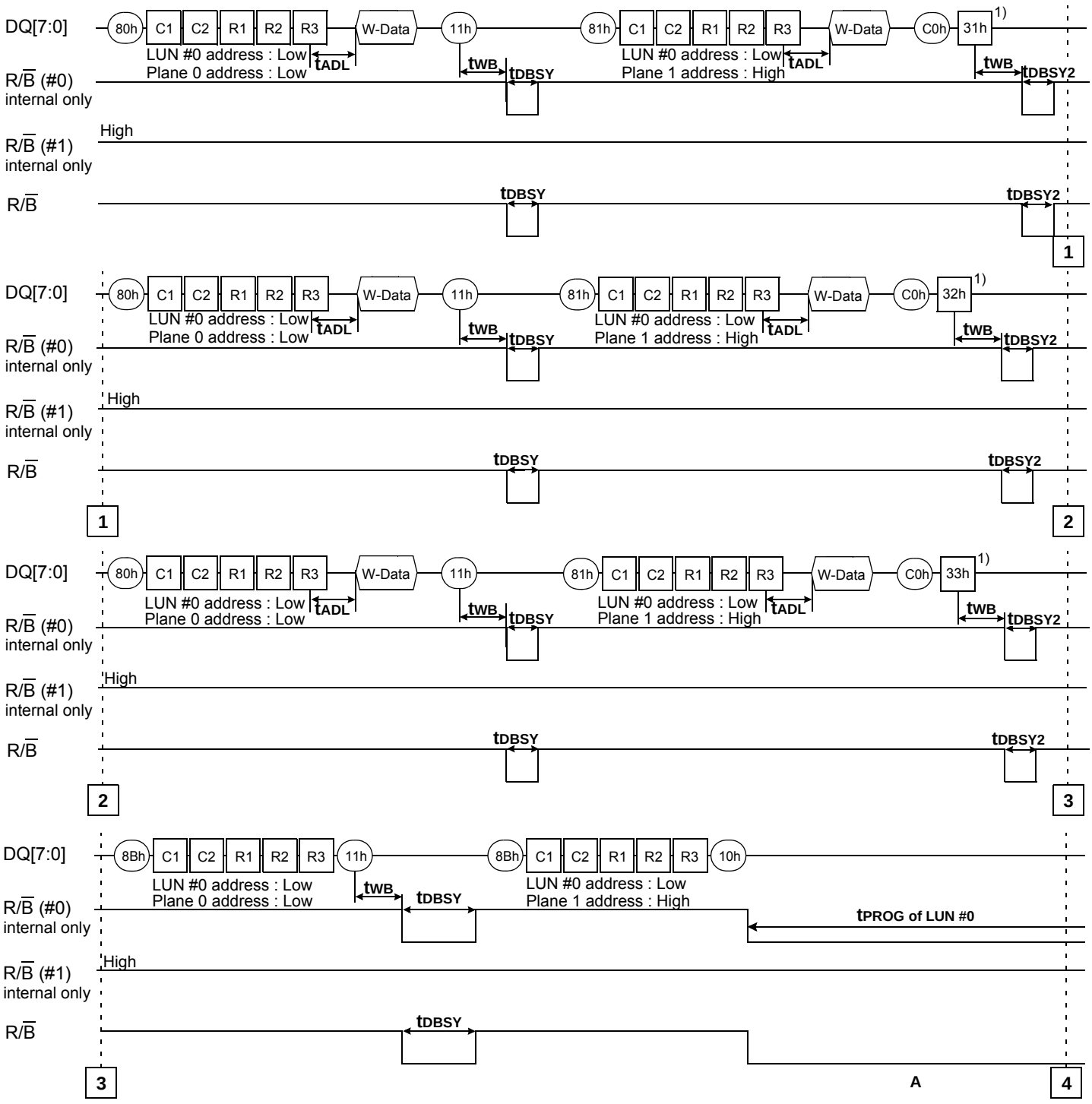
5.4.3 Interleaving Block Erase Operation



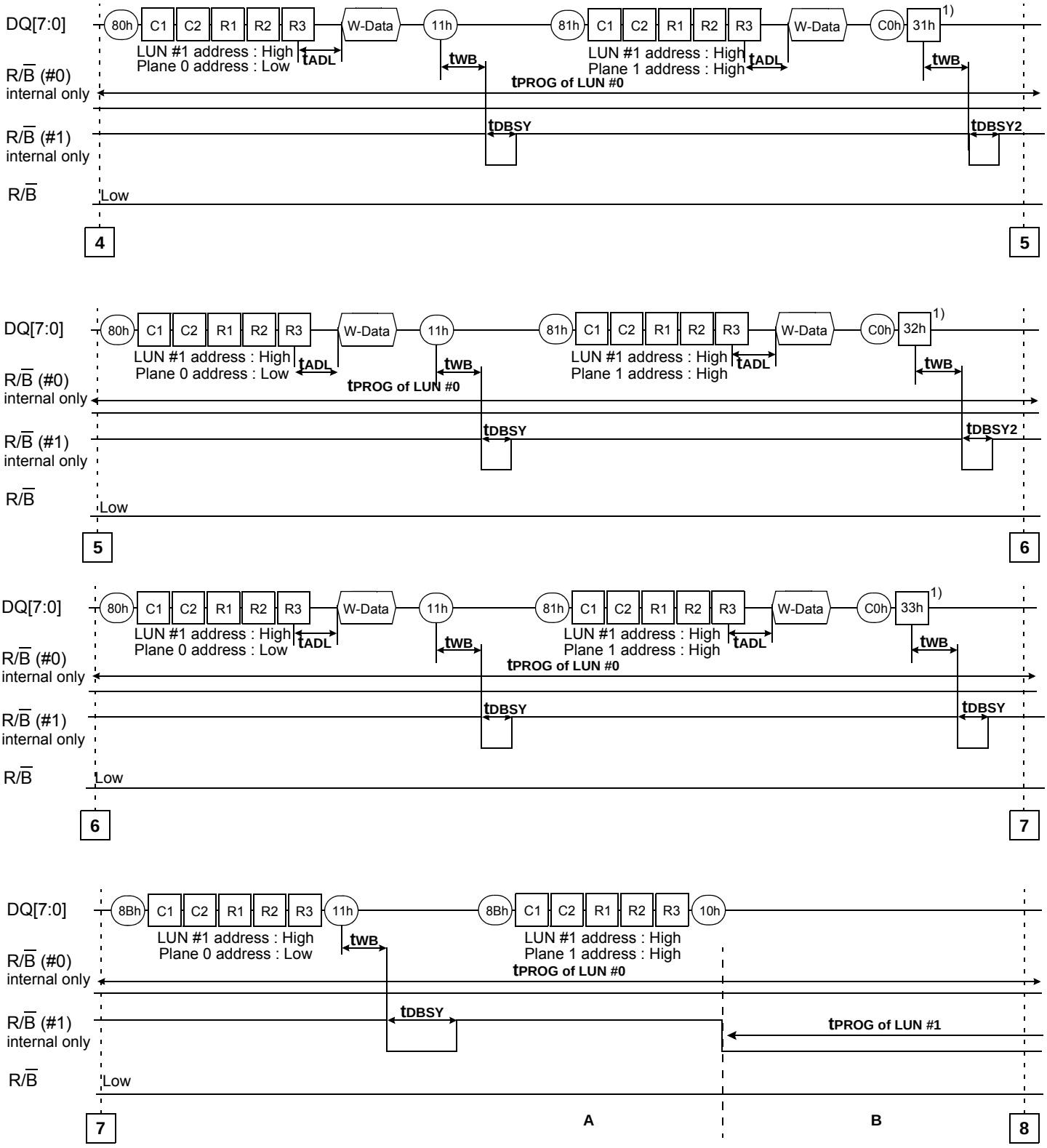
State A : LUN #0 is executing block erase operation, and LUN #1 is in ready state. So the host can issue block erase command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing block erase operation.
State C : Block erase on LUN #0 is terminated, but block erase on LUN #1 is still operating. And the system should issue 78h command to detect the status of LUN #0. If LUN #0 is ready, status I/O6 is "1" and the system can issue another block erase command to LUN #0.
State D : LUN #0 and LUN #1 are ready.

Depending on the above process, the system can operate block erase on LUN #0 and LUN #1 alternately.

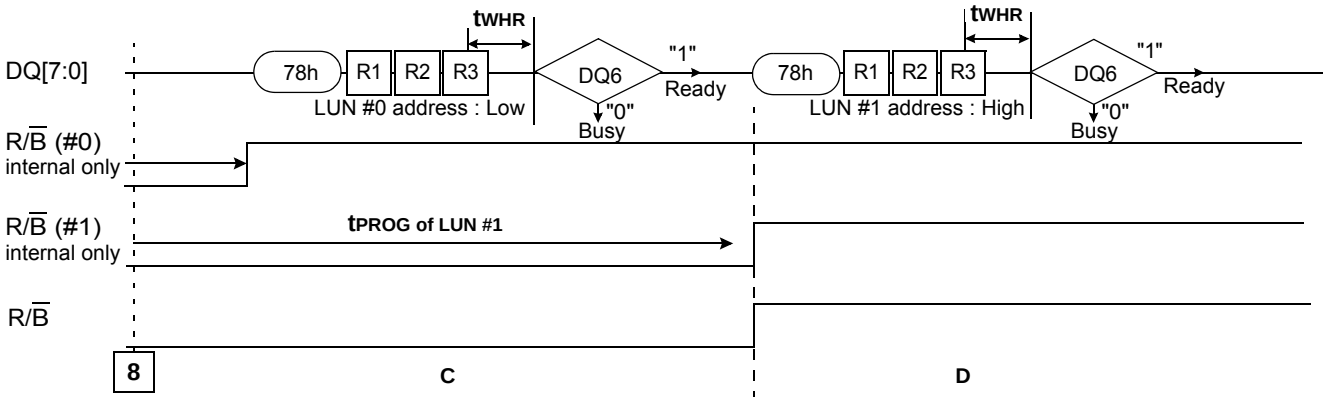
5.4.4 Interleaving Two-Plane Page Program Operation (1/3)



5.4.5 Interleaving Two-Plane Page Program Operation (2/3)



5.4.6 Interleaving Two-Plane Page Program Operation (3/3)

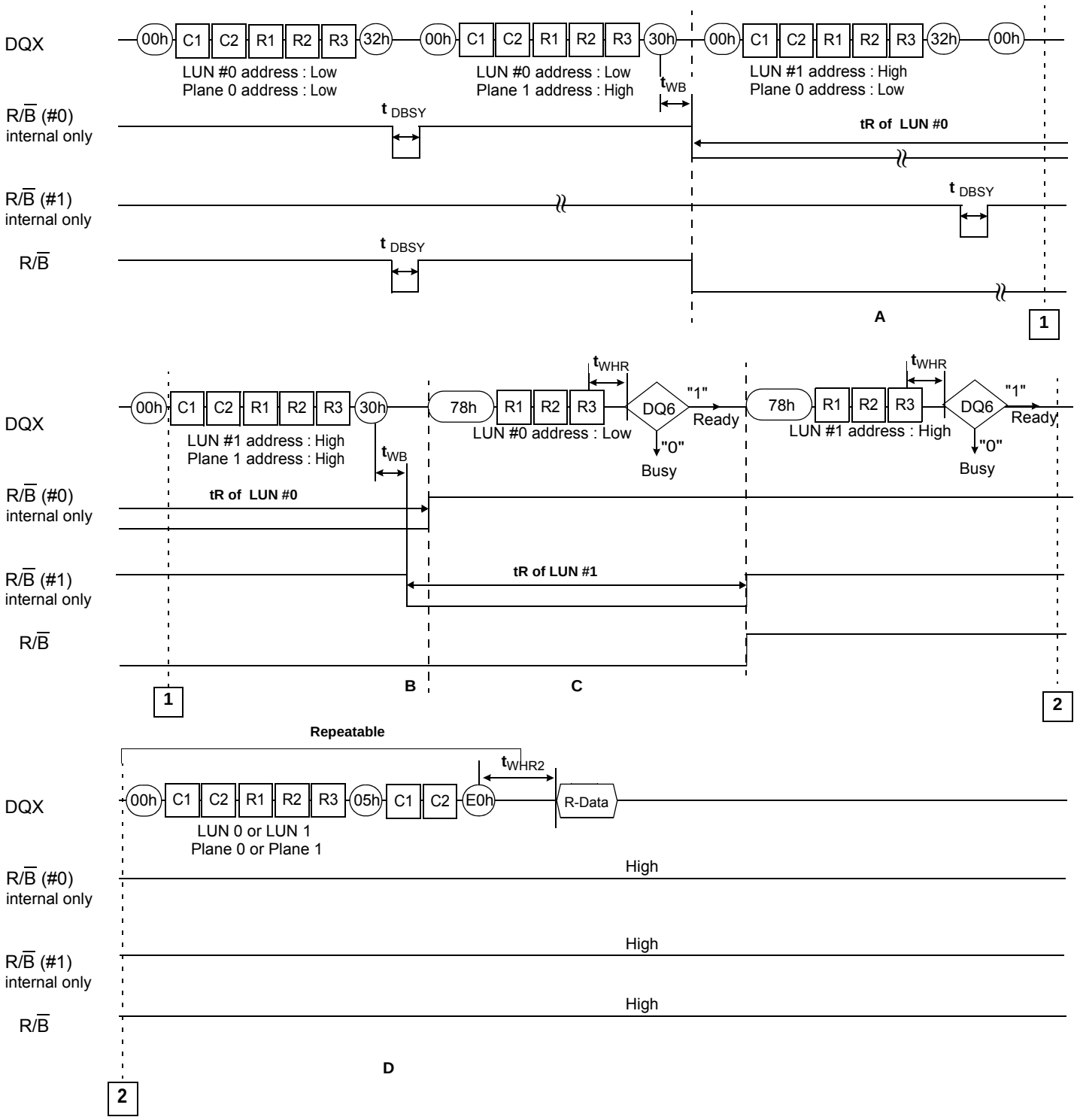


State A : LUN #0 is executing Two-plane page program operation, and LUN #1 is in ready state. So the host can issue Two-plane page program command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing Two-plane page program operation.
State C : Two-plane page program on LUN #0 is completed and LUN #0 is ready for the next operation. LUN #1 is still executing Two-plane page program operation.
State D : Both LUN #0 and LUN #1 are ready.

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 31.

Depending on the above process, the system can operate Two-plane page program on LUN #0 and LUN #1 alternately.

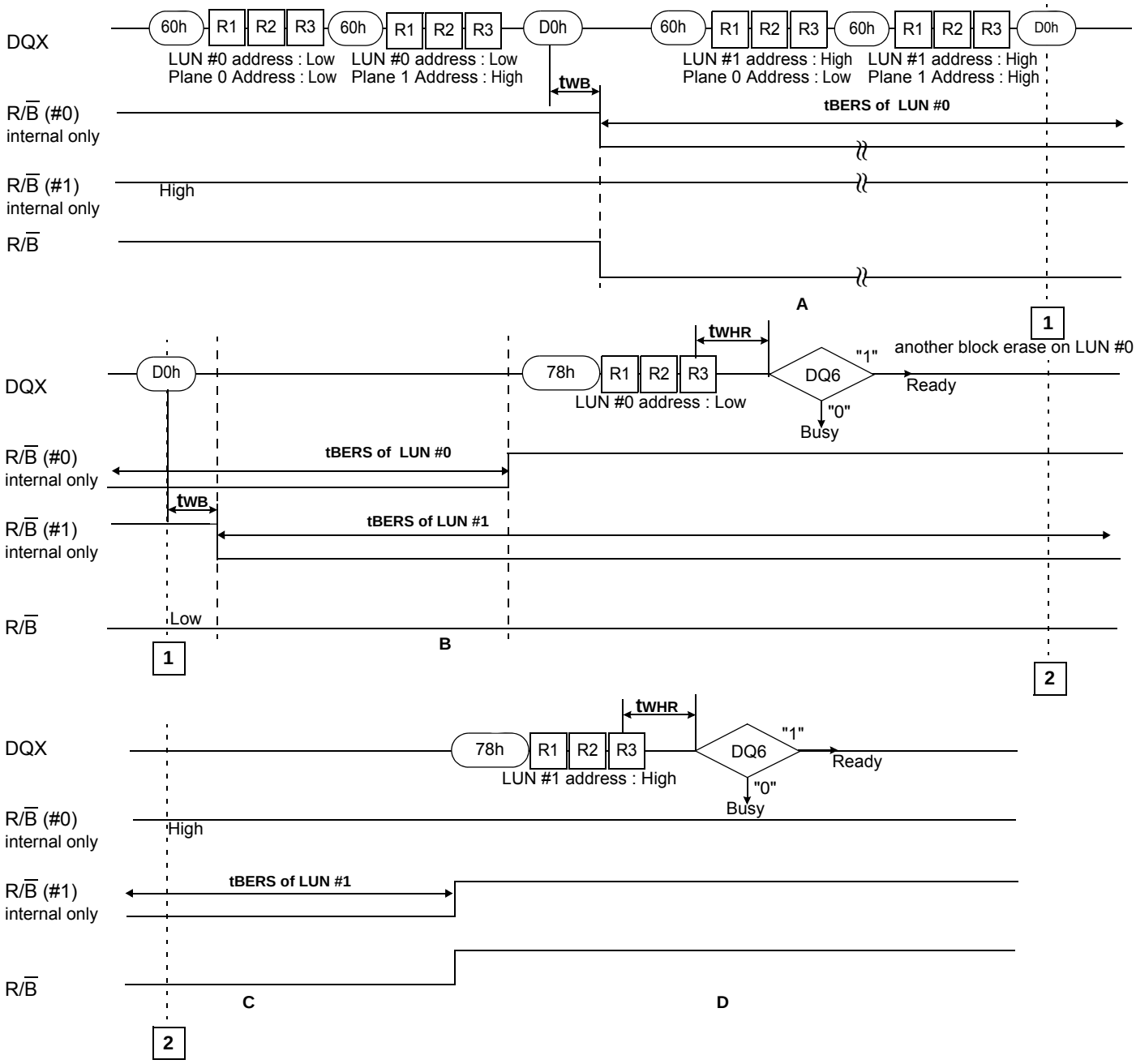
5.4.7 Interleaving Two-Plane Page Read Operation



State A : LUN #0 is executing Two-plane page read operation, and LUN #1 is in ready state. So the host can issue Two-plane page read command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing Two-plane page read operation.
State C : Two-plane page read on LUN #0 is completed and LUN #0 is ready for the next operation. LUN #1 is still executing Two-plane page read operation.
State D : Both LUN #0 and LUN #1 are ready.

NOTE :
78h command shall be required to check the Read status of LUN #0 and LUN #1.
Depending on the above process, the system can operate Two-plane page read on LUN #0 and LUN #1 alternately.

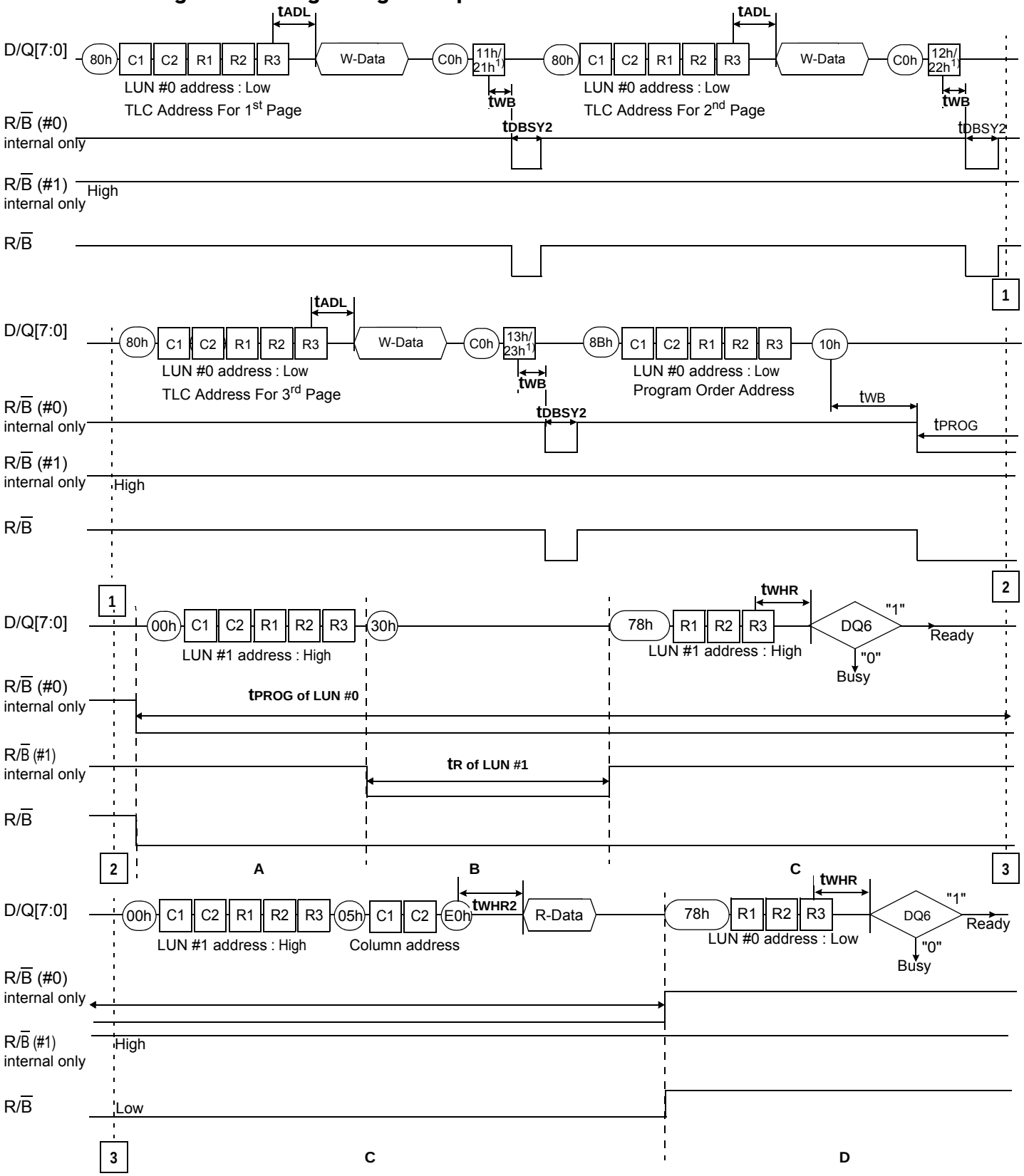
5.4.8 Interleaving Two-Plane Block Erase Operation



State A : LUN #0 is executing Two-plane block erase operation, and LUN #1 is in ready state. So the host can issue Two-plane block erase command to LUN #1.
State B : Both LUN #0 and LUN #1 are executing Two-plane block erase operation.
State C : Two-plane block erase on LUN #0 is completed and LUN #0 is ready for the next operation. LUN #1 is still executing Two-plane block erase operation.
State D : Both LUN #0 and LUN #1 are ready.

According to the above process, the system can operate Two-plane block erase on LUN #0 and LUN #1 alternately.

5.4.9 Interleaving Read to Page Program Operation

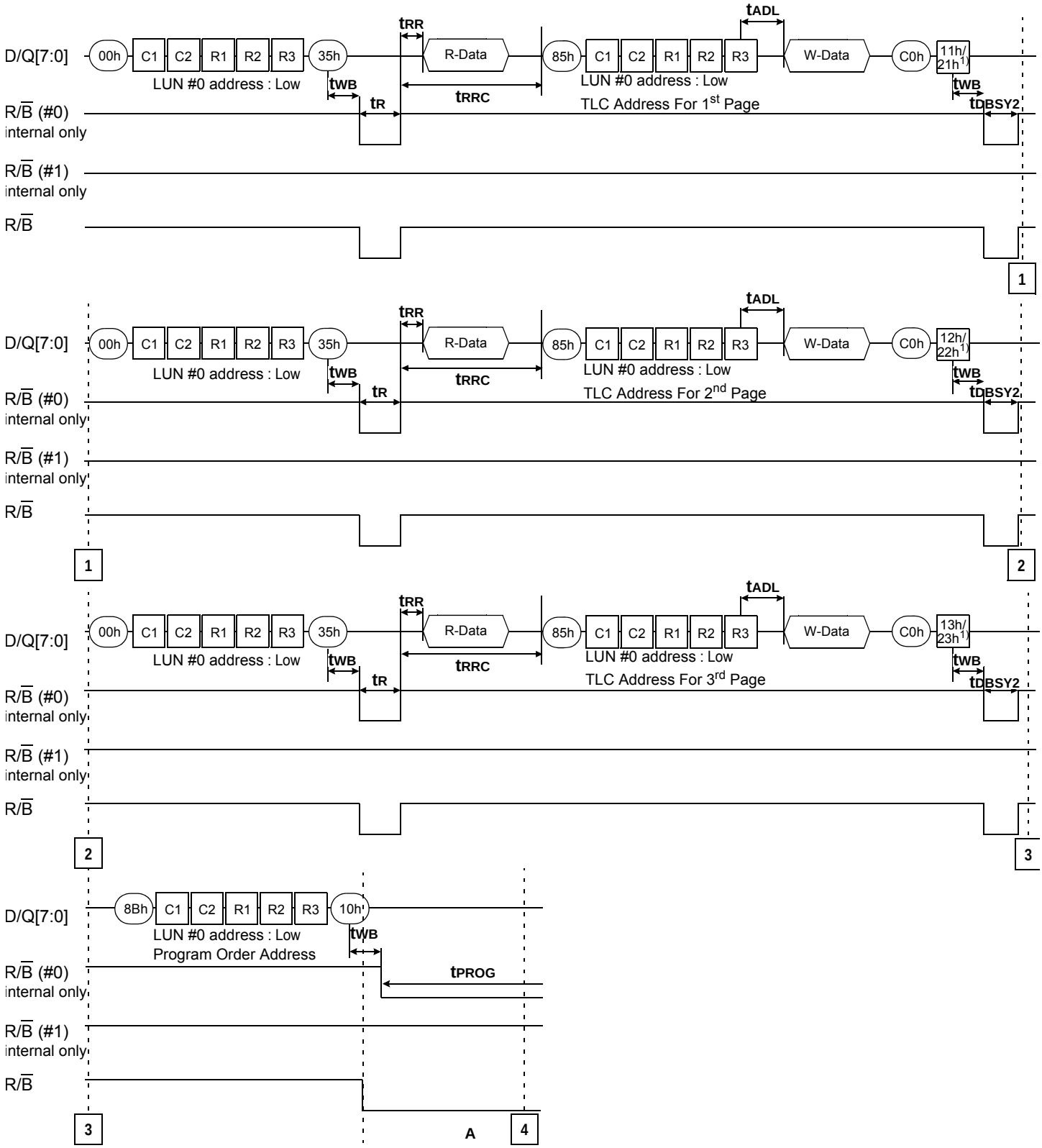


State A : LUN #0 is executing page program operation, and LUN #1 is in ready state. So the host can issue read command to LUN #1.
State B : Both LUN #0 is executing page program operation and LUN #1 is executing read operation.
State C : Read operation on LUN #1 is completed and LUN #1 is ready for the next operation. LUN #0 is still executing page program operation.
State D : Both LUN #0 and LUN #1 are ready.

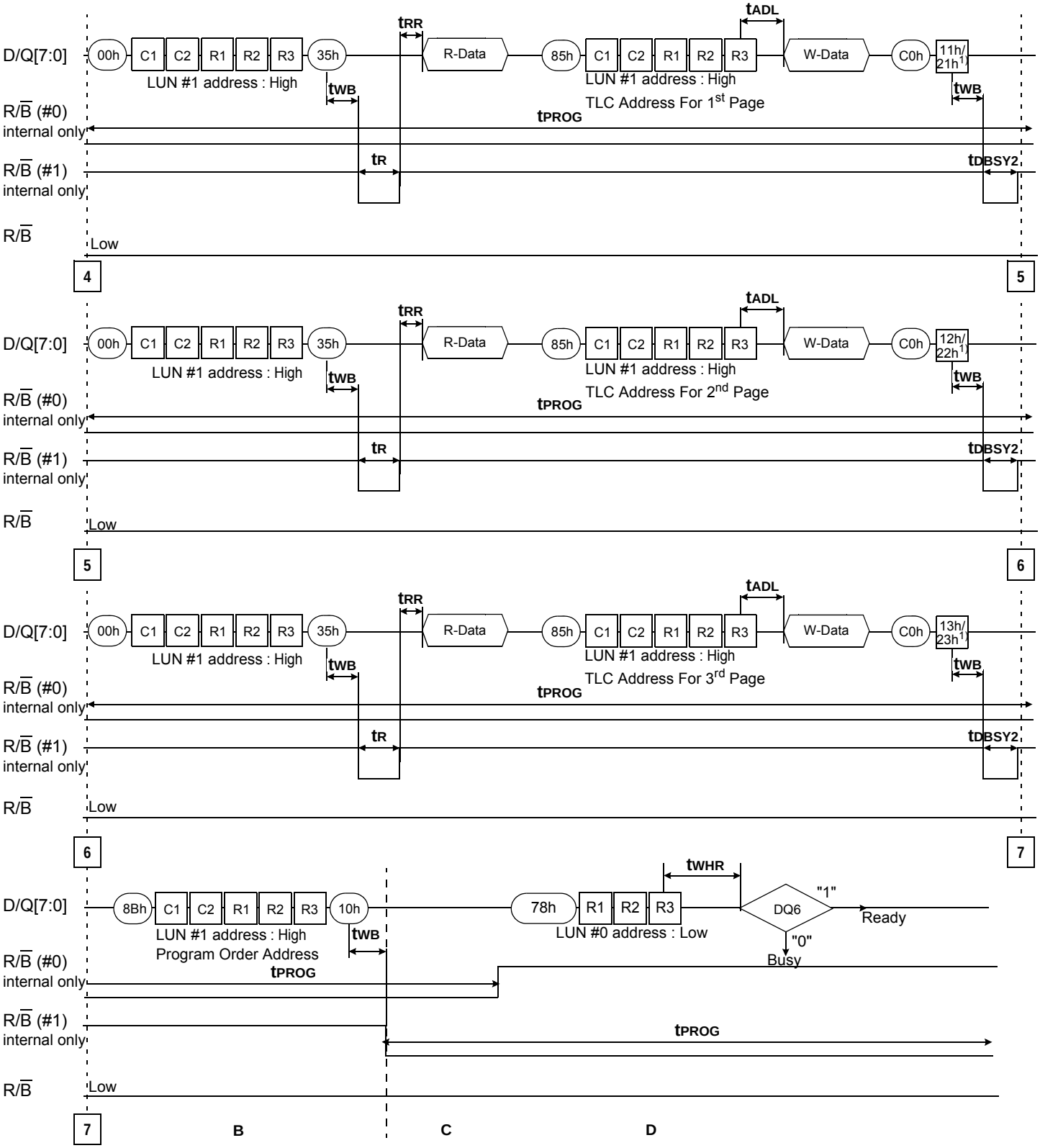
As the above process, the system can operate Interleave read to page program on LUN #0 and LUN #1 alternatively.

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 31.

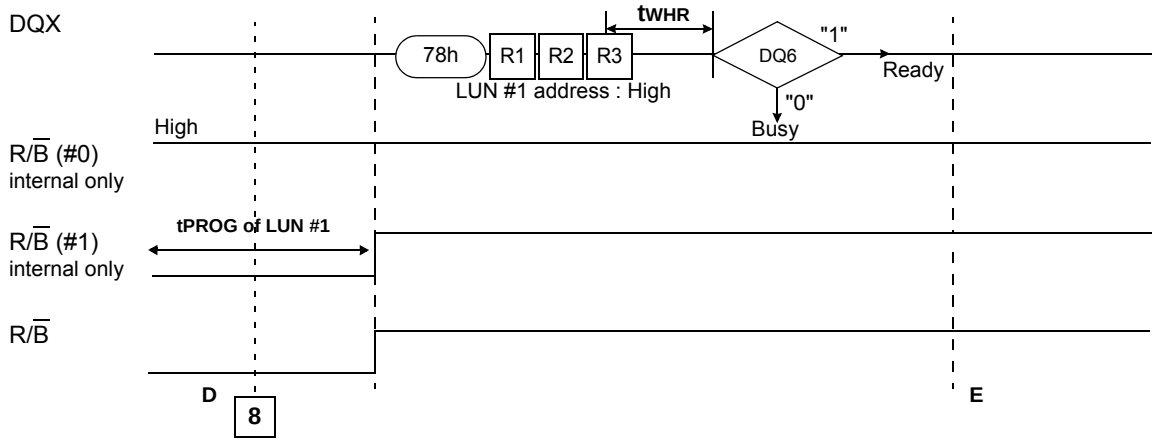
5.4.10 Interleaving Copy-Back Program Operation (1/3)



5.4.11 Interleaving Copy-Back Program Operation (2/3)



5.4.12 Interleaving Copy-Back Program Operation (3/3)

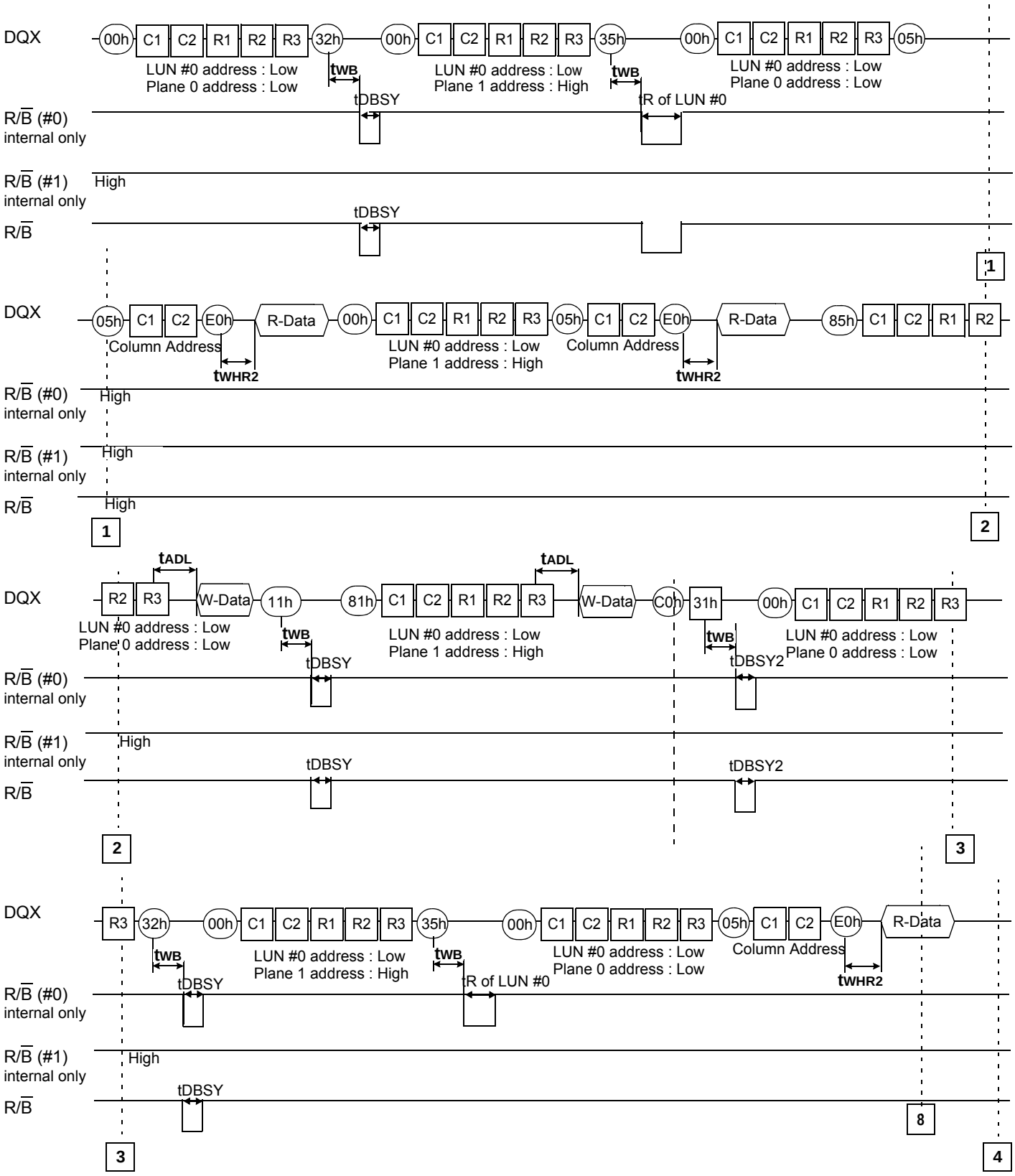


State A : LUN #0 is executing copy-back program operation, and LUN #1 is in ready state. So the host can issue read for copy-back command to LUN #1.
State B : Read for copy-back operation on LUN #1 is completed and LUN #1 is ready for the next operation. LUN #0 is still executing copy-back program operation.
State C : Both LUN #0 and LUN #1 are executing copy-back program operation.
State D : LUN #1 is still executing a copy-back program operation, and LUN #0 is in ready for the next operation.
State E : Both LUN #0 and LUN #1 are ready.

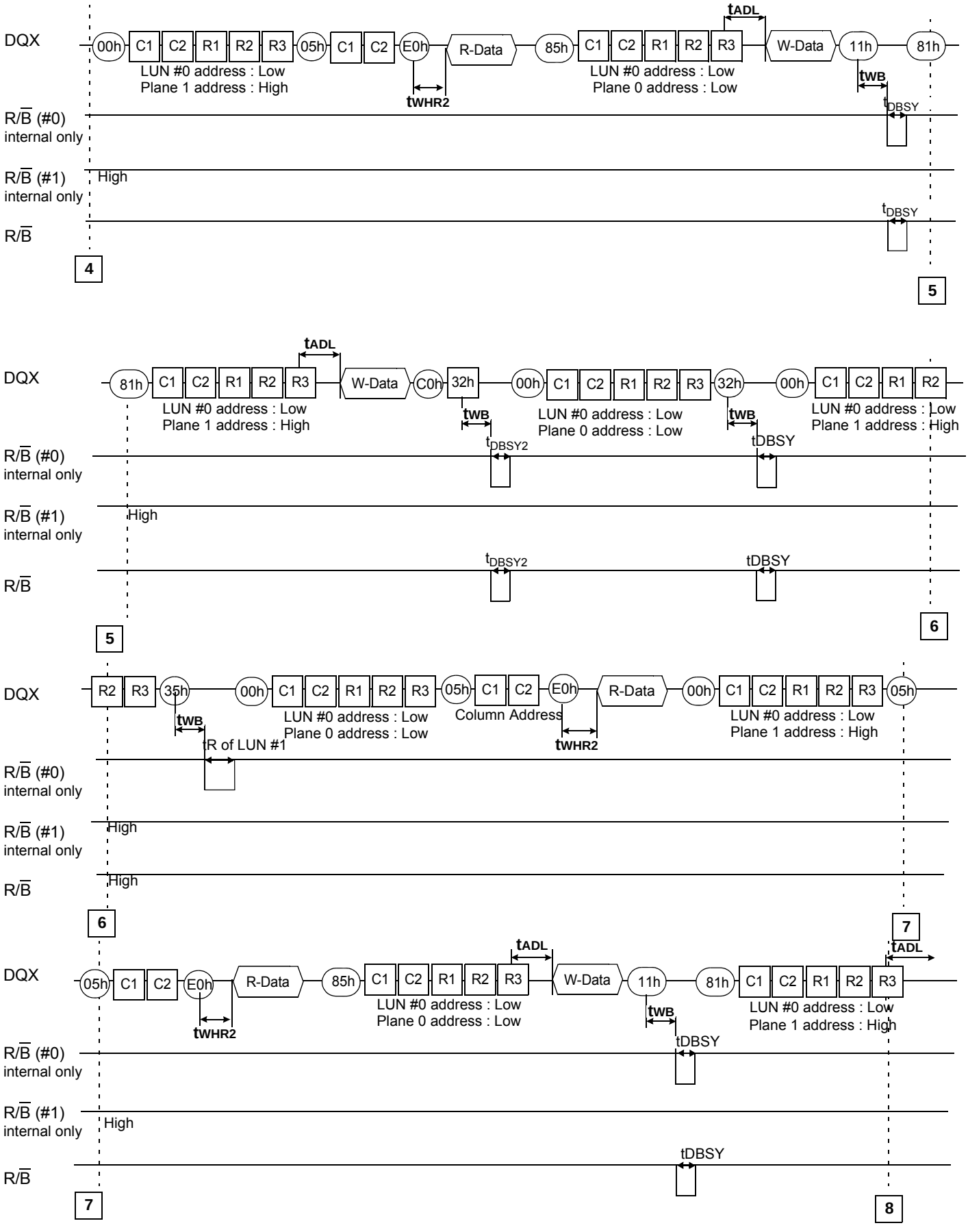
Depending on the above process, the system can operate Interleave copy-back program on LUN #0 and LUN #1 alternatively.

NOTE :
1) For address followed by C0h command, refer to the buffer address Table 31.

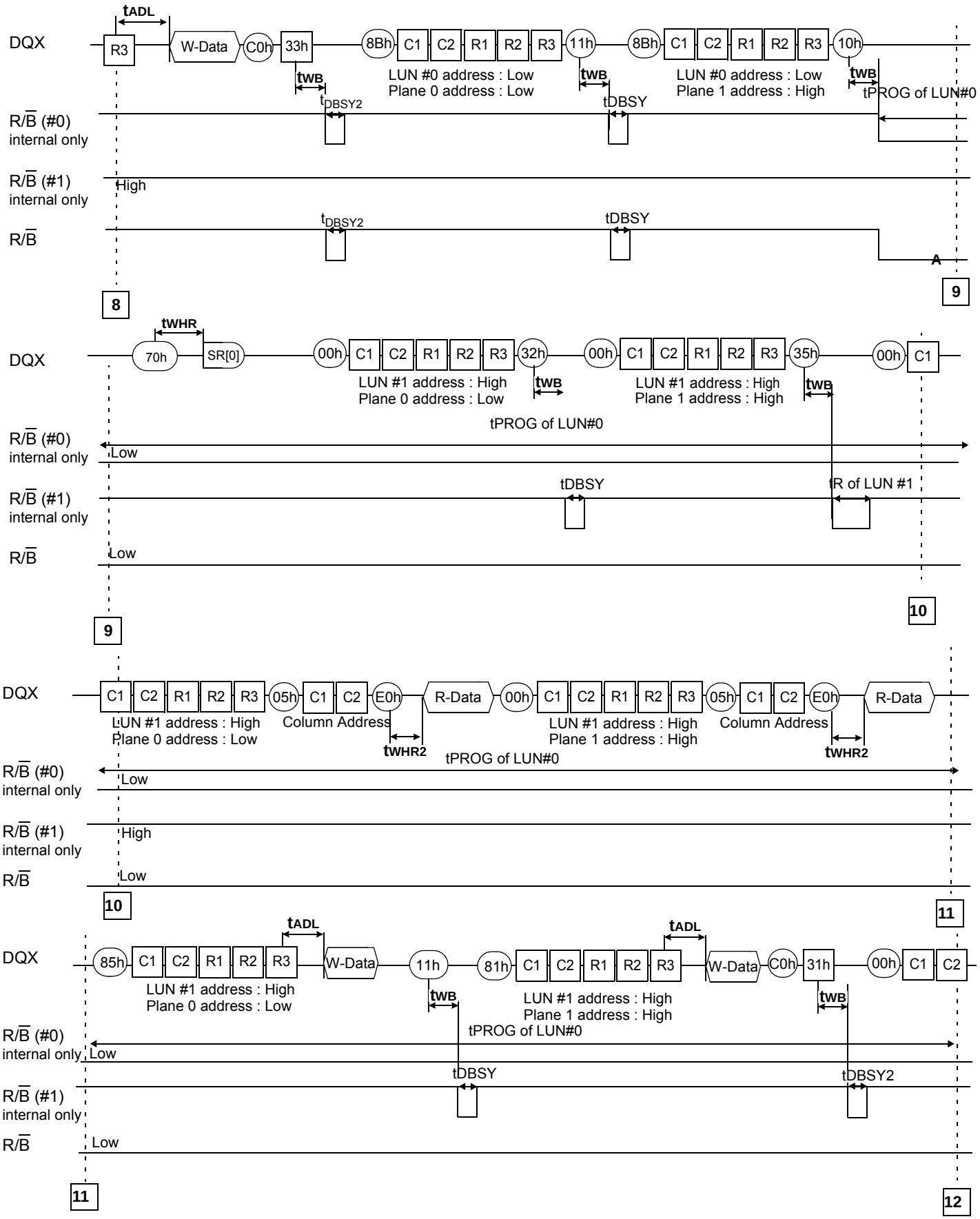
5.4.13 Interleaving Two-Plane Copy Back Program Operation (1/5)



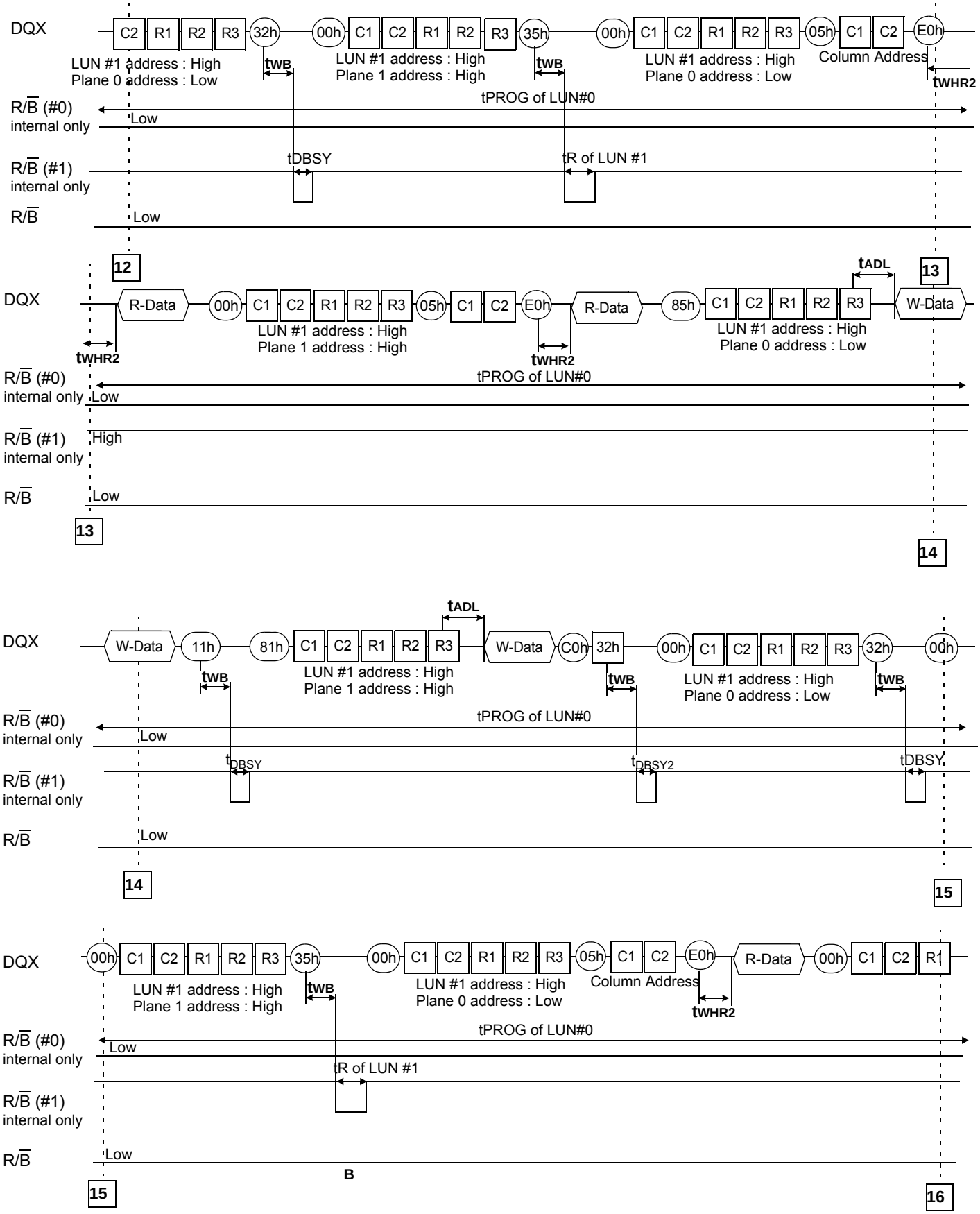
5.4.14 Interleaving Two-Plane Copy Back Program Operation (2/5)



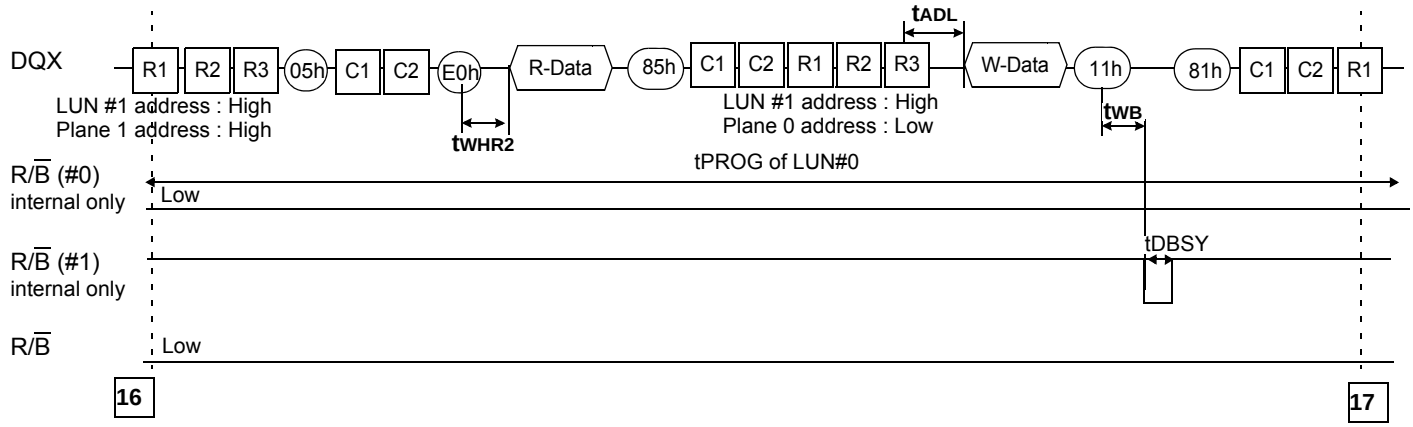
5.4.15 Interleaving Two-Plane Copy Back Program Operation (3/5)

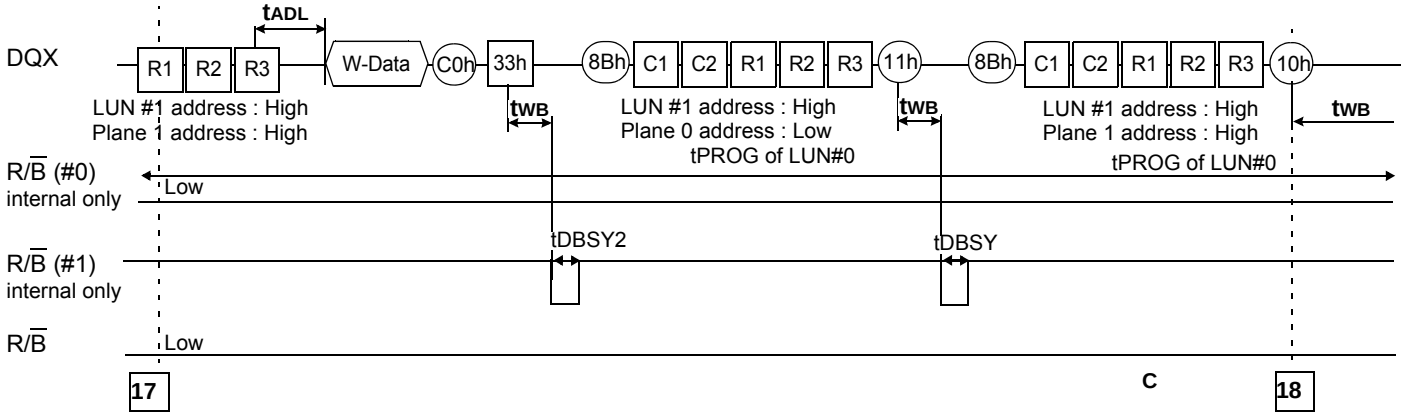


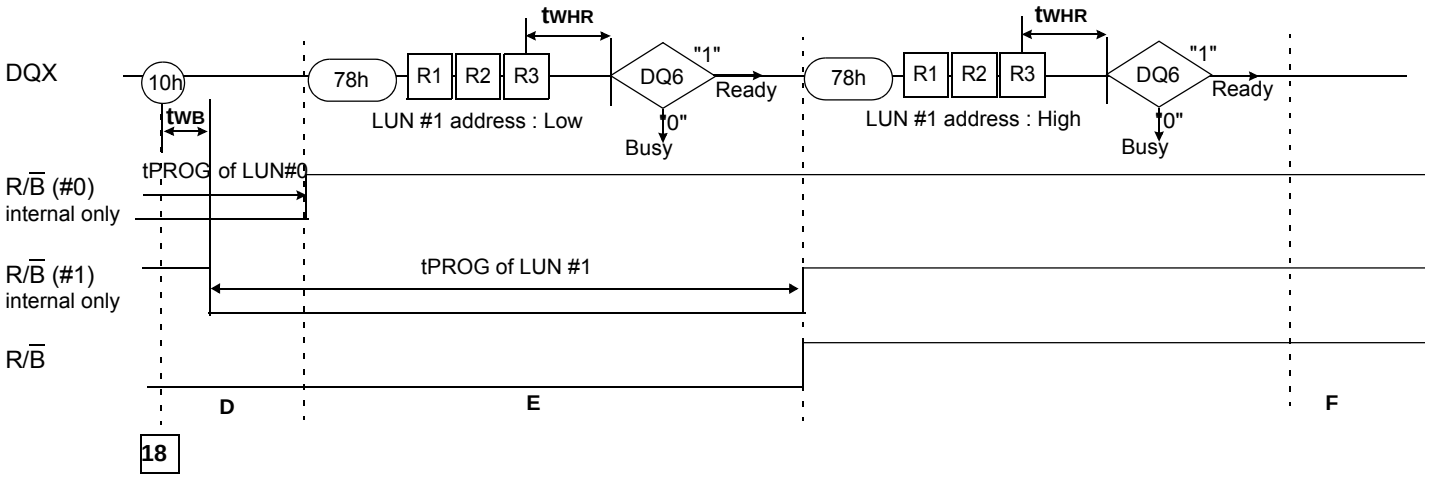
5.4.16 Interleaving Two-Plane Copy Back Program Operation (4/5)



5.4.17 Interleaving Two-Plane Copy Back Program Operation (5/5)





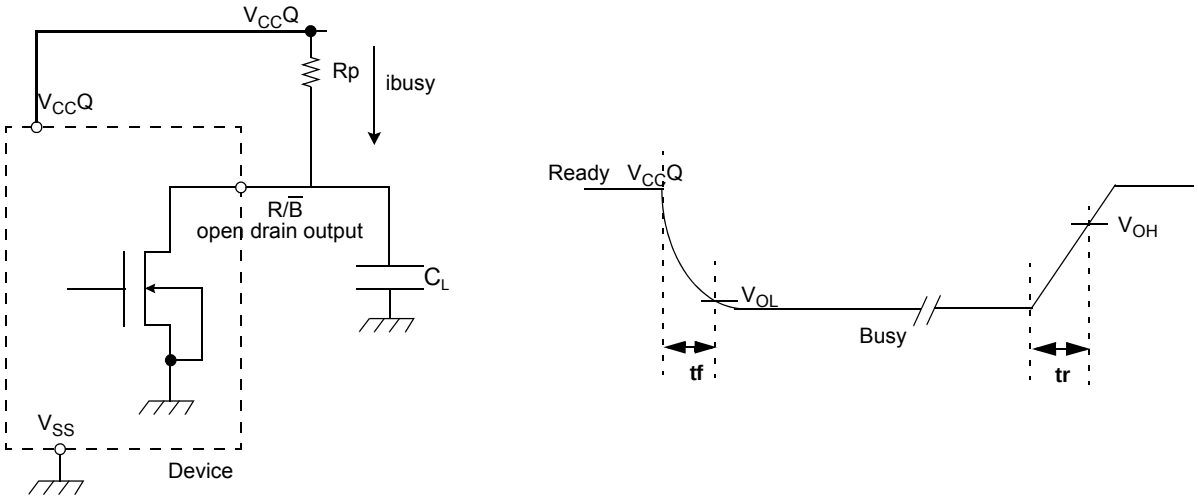


State A : LUN #0 is executing Two-plane copy-back program operation, and LUN #1 is in ready state. So the host can issue Two-plane read for copy-back command to LUN #1.
State B : LUN #0 is executing Two-plane copy-back program operation and LUN #1 is executing Two-plane read for copy-back operation.
State C : Two-plane read for copy-back operation on LUN #1 is completed and LUN #1 is ready for the next operation. LUN #0 is still executing Two-plane copy-back program operation.
State D : Both LUN #0 and LUN #1 are executing Two-plane copy-back program operation.
State E : LUN #1 is still executing a Two-plane copy-back program operation, and LUN #0 is in ready for the next operation.
State F : Both LUN #0 and LUN #1 are ready.

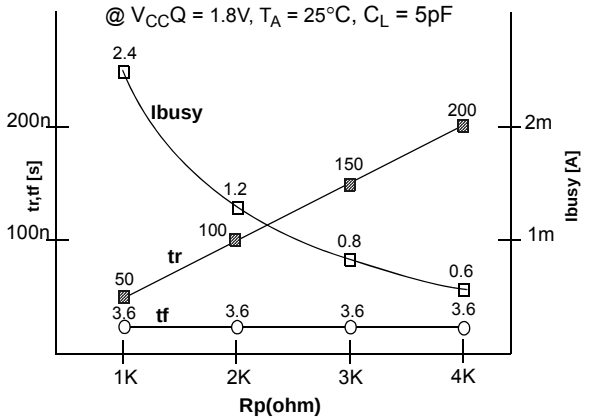
Depending on the above process, the system can operate Interleave Two-plane copy-back program on LUN #0 and LUN #1 alternatively.

5.5 Ready/$\overline{\text{Busy}}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy), an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.



Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

$$Rp(min, 1.8V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

Where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr.