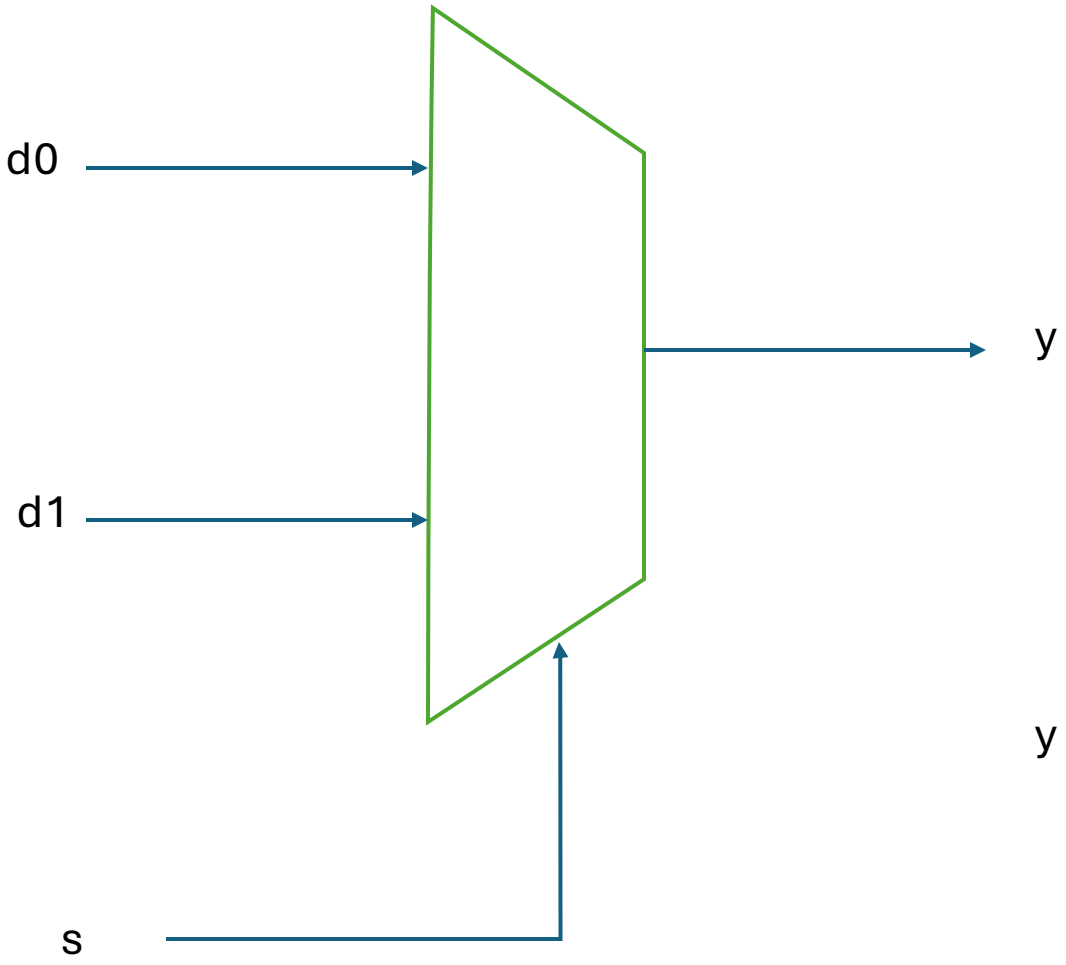
Multiplexer

VHDL modeling



s	y
0	d0
1	d1

y = ((NOT s) AND d0) OR (s AND d1))

$$y = (\bar{s}.d0) + (s.d1)$$

Types of VHDL description

- Behavioral
- Dataflow
- Structural

- Behavioral (check)

y = ((NOT s) AND d0) OR (s AND d1))

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- Behavioral
- Dataflow
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- Dataflow (check)

```
y <= ((NOT s) AND d0) OR  (s AND d1);
```

Types of VHDL description

- Behavioral
- Dataflow
- **Structural**

- structural

y = ((NOT s) AND d0) OR (s AND d1))