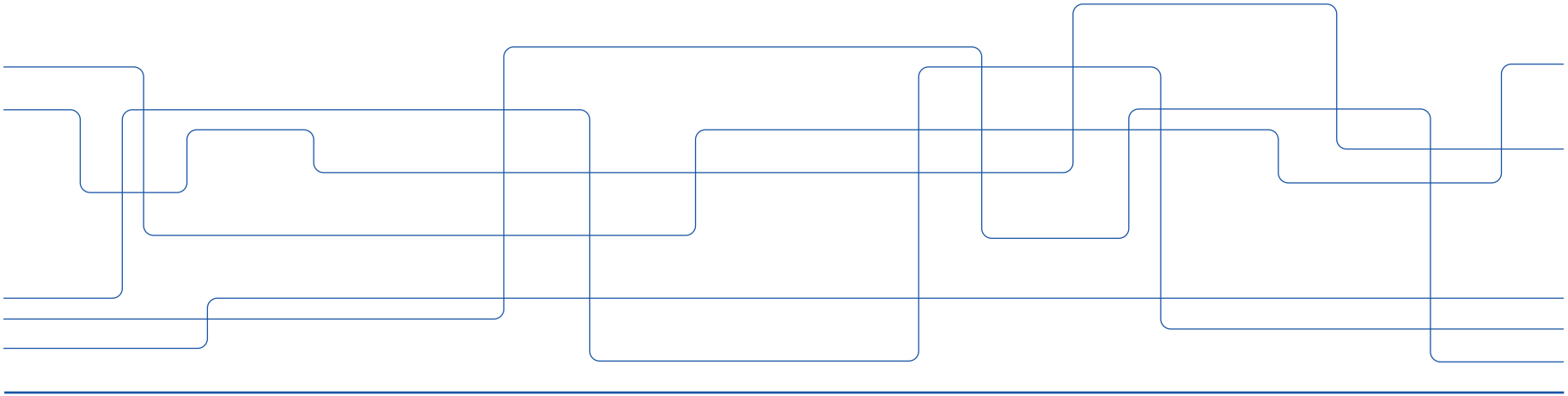
KTH ROYAL INSTITUTE OF TECHNOLOGY

Embedded Hardware Design in ASIC and FPGA

Project – Synthesis of the DRRA Fabric

Autum Semester, Period 1, 2024

Nov 14, 2024



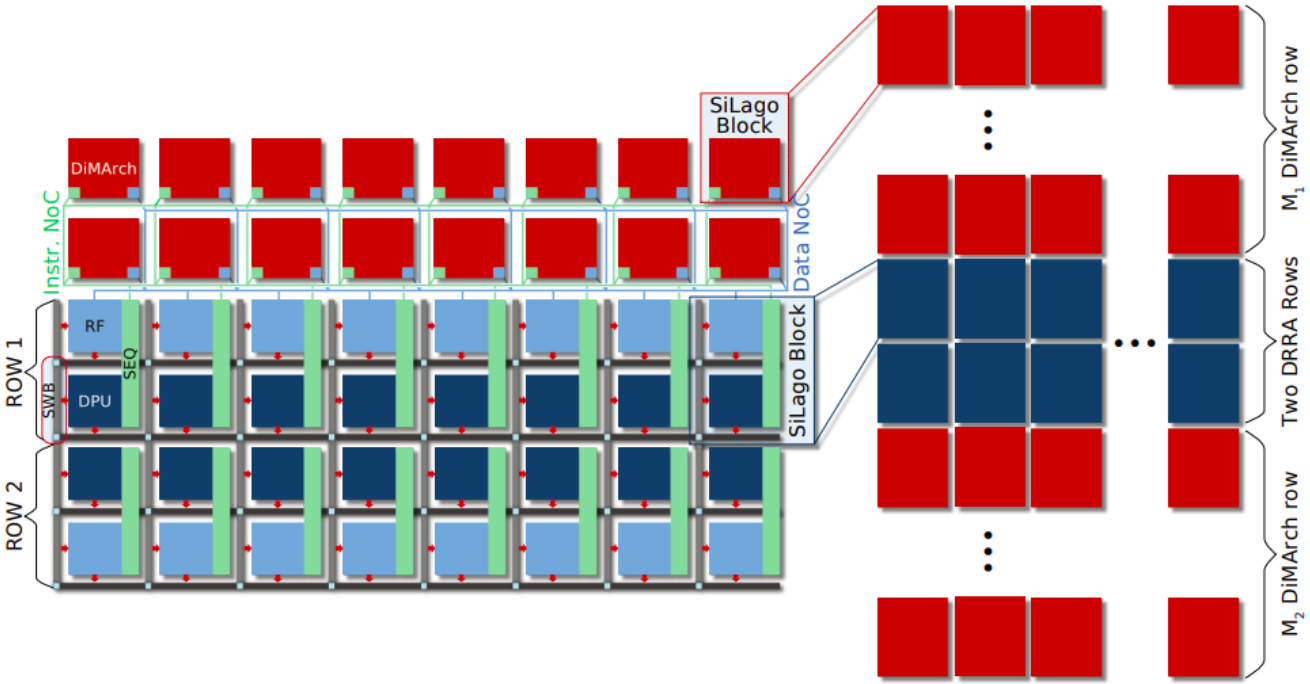
About the project

- ***Simulate*** a given RTL design in Questasim.
- ***Logic synthesis*** of the design in t*wo different styles*.
- ***Physical implementation*** of the netlist *in two different styles*.
- All tasks should be completed to pass.
- Teams of four students. Please join a group in Canvas.

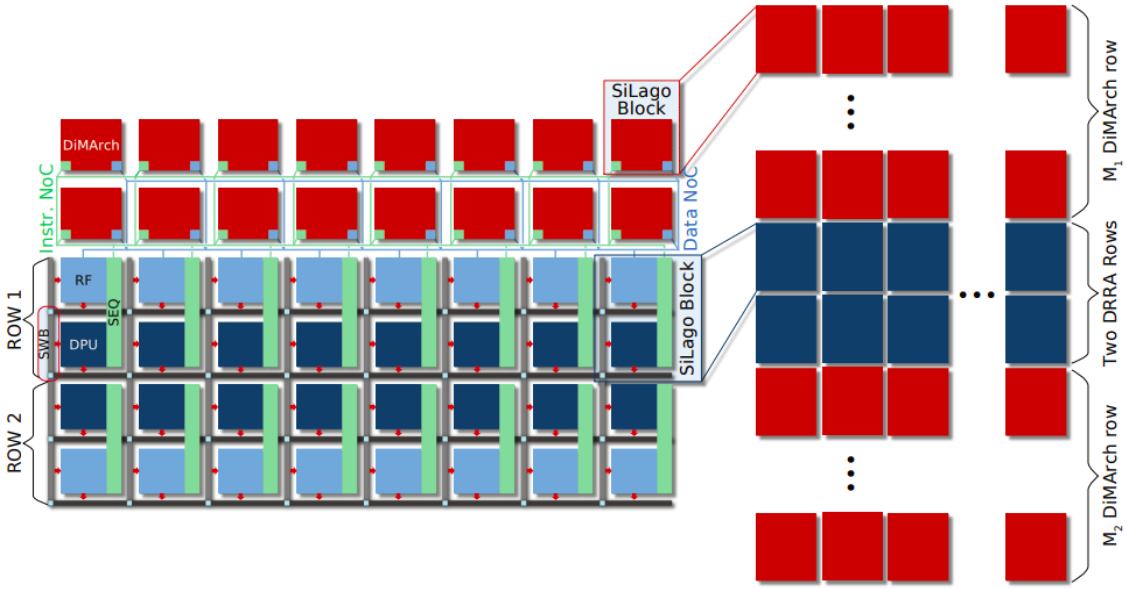
The design - DRRA and DiMArch Fabric

- DRRA stands for Dynamically Reconfigurable Resource Array.
- DRRA serves the computational need of the design.
- DiMArch stands for Distributed Memory Architecture.
- DiMArch serves as the scratchpad memory.
- You will simulate the RTL for DRRA and DiMArch.
- You will do logic synthesis and physical implementation of only DRRA.

DRRA and DiMArch Fabric

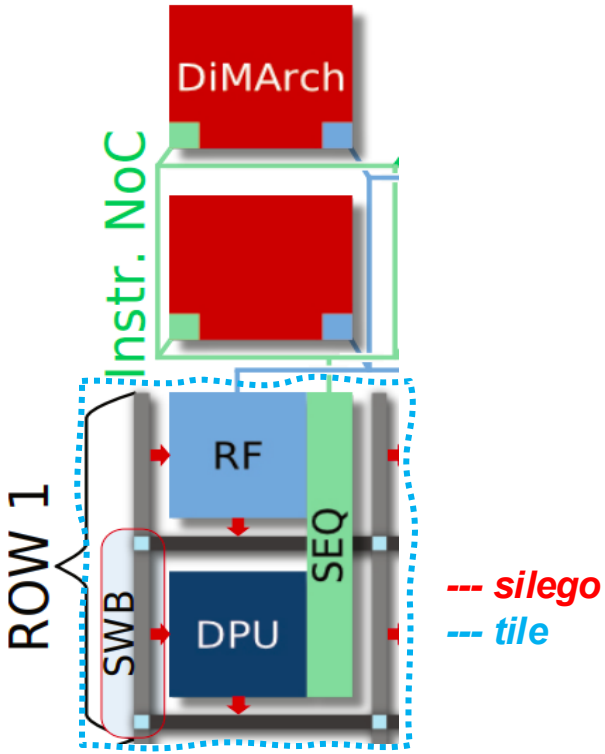


DRRA and DiMArch Fabric



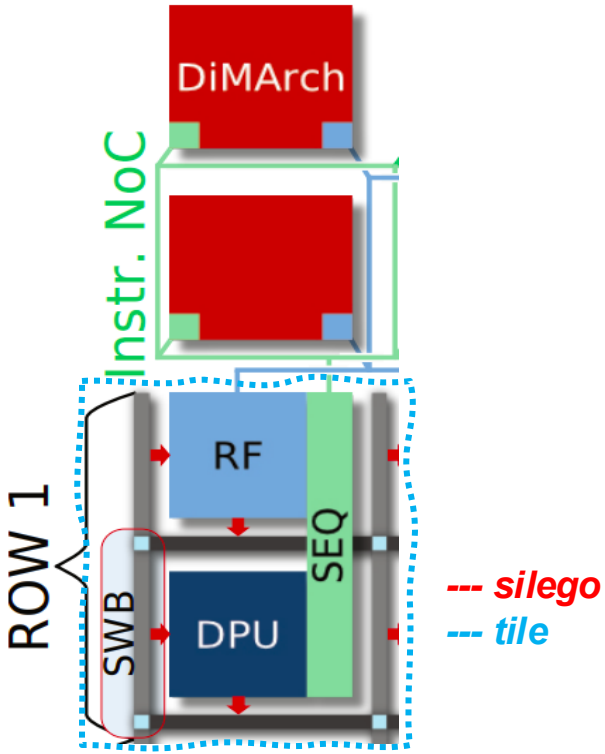
- Two rows of DRRA tiles.
- Two rows of DiMArch tiles.
- Each row has 8 tiles.

Zooming in...



- All tiles share a common module, ***silego***.
- **silego** consists of:
  - **SEQ** ***(Sequencer)***
    - Stores instructions.
    - Instructions configure the data path settings of each tile for data movement and computation.
  - **RF** ***(Register File)***
    - Bank of registers inside a tile for temp storage.
  - **DPU** ***(Data Processor Unit)***
    - Perform standard computation functions like, add, sub, mac, etc
  - **SWB** ***(SwitchBox)***
    - Configures the connections.

Zooming in...



- Depending on the location of each tile, ***silego*** has a tile wrapper.
- E.g, the DRRA tile in the top left corner does not have connections in the west. The tile wrapper wraps the common module silego with the connectivity associated with each tile location.
- There are six distinct DRRA tiles inside an overall ***DRRA wrapper***:
  - *DRRA_tile_top_left_corner*
  - *DRRA_tile_bot_left_corner*
  - *DRRA_tile_top_right_corner*
  - *DRRA_tile_bot_right_corner*
  - *DRRA_top*
  - *DRRA_bot*
- DiMArch follows similar design style.

A note on folder organization

- /rtl folder contains design files, including hierarchy files for silego, DRRA wrapper, and the complete design.
- /tb contains testbench.
- /syn for logic synthesis files.
- /phy for physical synthesis files.

Task 1 – Simulation of RTL design

- Goal - Demonstrate an understanding of inferring and simulating large designs.
- Testbench (available in the tb/ folder) – simple vector addition by the DPU of top_left tile.
- Compile ***the complete design in Questa,***
- Hierarchy file to use: rtl/silagonn_hierarchy.txt
- Simulate the design.
- Check the output waveforms of DPU<0,0> of the tile.

Task 2 – Flat logic synthesis

- Goal - Logic synthesis.
- Synthesise ***DRRA_wrapper with DC***.
- Hierarchy file to use: rtl/drra_wrapper_hierarchy.txt
- Since this is a big design, synthesis is slow, and it may test your patience :)
- Start with a large clock for fast synthesis. Reduce the clock once you are sure your script is clean.
- Assess PPA of the design with different clock periods. Understand design trade-offs.
- You may ignore warnings however be careful of the errors that halt the synthesis.

Task 3 – Bottom-Up logic synthesis

- Goal - Bottom-up logic synthesis.
- Synthesise ***DRRA_wrapper with DC*** following a bottom-up approach.
- Hierarchy file to use: rtl/silego.txt
- Assess PPA of the design with different clock periods to understand trade-offs. Why/why not is it different from the flat synthesis?

Task 4 - Flat Physical synthesis

- Goal - Flat physical synthesis.
- Physical synthesis of ***DRRA_wrapper with Innovus***.
- In flat physical synthesis, the design is not explicitly partitioned.
- Assess PPA of the design for one clock period. Why/why not is it different from logic synthesis results?

Task 5 - Floorplaning

- Goal - Floorplanning in physical synthesis.
- Physical synthesis of ***DRRA_wrapper with Innovus***.
- Decide locations of blocks.
- Identical blocks can be compiled once and reused by placing at several locations.

Task 6 - Hierarchical Physical synthesis

- Goal - Hierarchical physical synthesis.
- Hierarchical Physical synthesis of ***DRRA_wrapper with Innovus***.
- After fixing location, compile the partitions hierarchically.
- These partitions are assembled at the top level.
- Assess PPA of the design for one clock period. Why/why not is it different from logic synthesis and flat implementation?

Presentation

- Each group has a slot of 1 hour.
  - Book slots in Canvas. Slots available on week 03 and week 04, 2026.
  - 20 mins presentation. All members should participate.
  - 40 mins for questions and checking the scripts.
- We welcome creative analysis and insights on top of the Task requirements.

Grading

- Grades will be assessed on individual basis, *all group members are expected to contribute to the project*.
- Students are expected to have an understanding of all the tasks in the project, although they may divide the tasks individually.