컴퓨터 구조 2 번째 과제

2019040164 정지오

<Problem 3.1>

Device 5: 0003, location 940: 0002, Device 6: 0000

1. 3005 -> IR
2. 3 -> AC
3. 5940 -> IR
4. 3+2 = 5 -> AC
5. 7006 -> IR
6. AC -> Device 6

<Problem 3.3>

a. Opcode = 8 bit, Operand = 24 bit

➔ 2^24 = 2^20 x 16 = 1M x 16 = 16Mbytes.

b. 1)

local address bus: 32 bits -> whole address can be transferred at once and decoded in memory

local data bus: 16 bits -> require 2 cycles to fetch 32 bit instruction

2)

Local address bus: 16 bits -> can't access the whole referenced word of memory. So more complex memory interface control is needed to latch the first part of the address and then the second part.

Local data bus: 16 bits -> require 2 cycles to fetch 32 bit instruction

c. pc: 24 bits, ir: 32 bits

<Problem 3.4>

16 bit address, 16 bit data bus

a. 2^16 = 64KBytes (address is 16 bit)

b. 2^16 = 64Kbytes (address is 16 bit)

c. one more output pin is needed to carry I/O signals. Because it is different from the memory signals that is generated during the execution for memory instructions.

(I/O 시그널을 전송하려면 하나의 출력 핀이 더 필요하다. 왜냐하면 이 시그널은 메모리 명령 실행 중에 생성되는 메모리 신호와는 다르기 때문이다)

<Problem 3.14>

a. the instruction requires 16 bus clock cycles(4+3+3+3+3). there is four memory accesses. So 8 wait states will be required. So 16 + 8 = 24 clock cycles will be needed. First, it is needed only 16 clock cycles. Now it is needed 24 clock cycles, so duration of the instruction increase 50%.

b. Three bus clock cycles to add 1 to operand → 13 bus clock cycles to add 1 to operand.

   The instruction will be needed 26 bus cycles. So instruction needs 26 + 8 = 34 bus cycles.

<Problem 3.15>

a. Clock period is 125ns. So on read cycle is required 125 x 4 = 500 ns = 05 μs. Data transfer rate = 1/0.5 = 2MB/s

b. Bus read cycle will be increased 125ns. So, one read cycle is required 125 x 5 = 625 ns = 0.625 μs. Data transfer rate = 1/0.625 = 1.6MB/s