컴퓨터 구조 4번째 과제

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[Review]

5.3)

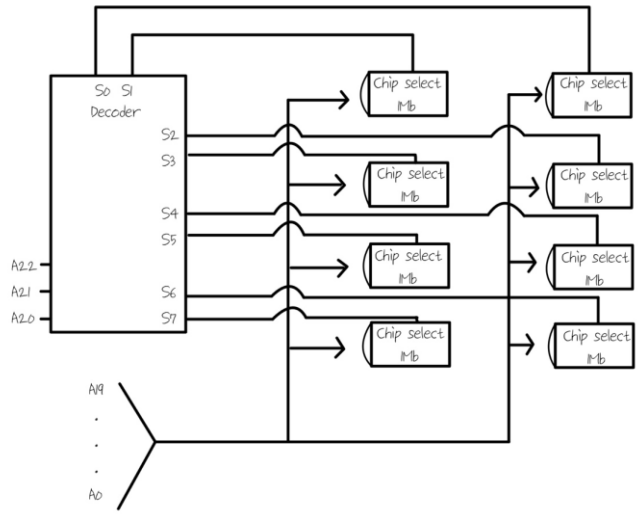
SRAM is used for cache memory (both on and off chip), and DRAM is used for main memory.

5.4)

SRAMs generally have faster access times than DRAMs. DRAMs are less expensive and smaller than SRAMs.

[problems]

5.4)



5.10)

The stored word is 001101001111, as shown in Figure 5.10. Now suppose that the only error is in C8, so that the fetched word is 001111001111. Then the received block results in the following table.

Poistion	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	D6	D5	C8	D4	D3	D2	C4	D1	C2	C1
Block	0	0	1	1	1	1	0	0	1	1	1	1
Codes			1010	1001		0111				0011		

원래 k값: 0111

K'값: 1111

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Syndrome = 1000 → The nonzero result detects and error and indicates that the error is in bit position 8, which is check bit C8.

5.11)

Poistion	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	D6	D5	C8	D4	D3	D2	C4	D1	C2	C1
Block	1	1	0	0		0	0	1		0		
Codes	1100	1011						0101				

C1= D1+D2+D4+D5+D7= 0+1+0+0+1= 0

C2= D1+D3+D4+D6+D7= 0+0+0+0+1= 1

C4= D2+D3+D4+D8= 1+0+0+1= 0

C8= D5+D6+D7+D8= 0+0+1+1 = 0

So, check bits are 0 0 1 0.

5.12)

Bit number:

12	11	10	9	8	7	6	5	4	3	2	1
0	0	1	1	0	1	0	0	1	1	1	1

Check bits are calculated to be 1101(=K').

K = 0111

K′ = 1101

———————

Syndrome = 1010 -> position number 10 error occurs

→ data word read from memory was 00011001

5.14)

data= 0101000000111001

C1= D1+D2+D4+D5+D7+D9+D11+D12+D14+D16= 1+0+1+1+0+0+0+0+0+0= 1

C2= D1+D3+D4+D6+D7+D10+D11+D13+D14= 1+0+1+1+0+0+0+1+0= 0

C4= D2+D3+D4+D8+D9+D10+D11+D15+D16= 0+0+1+0+0+0+0+1+0= 0

C8= D5+D6+D7+D8+D9+D10+D11= 1+1+0+0+0+0+0= 0

C16= D12+D13+D14+D15+D16= 0+1+0+1+0= 0

K= 00001

In D5, Error occurs

→ C16= 0, C8= 1, C4= 0, C2= 0, C1= 0 → K′= 01000

K = 00001

K′= 01000

———————

Syndrome number = 01001 → error occurs in position 9(D5).