컴퓨터 구조 5번째 과제

2019040164 정지오

[Review]

7.3) I/O module의 major function

Control and timing, processor communication, device communication, data buffering and error detection.

7.5) difference between memory-mapped I/O and isolated I/O

Memory-mapped I/O: there is a single address space for memory location and I/O devices. The processor treats the status and data registers of I/O modules as memory locations and uses the same machine instructions to access both memory and I/O devices.

Isolated I/O: The command line specifies whether the address refers to a memory location or an I/O device. The full range of addresses may be available for both. Address space for I/O is isolated from that for memory.

[Problems]

7.1)

For the first I/O instruction format, we have 8 bits for port addressing, therefore, the number of port addressed can be calculated as 2^8= 256 ports.

For the second instruction format, we have 16 bits for addressing, therefore, the number of ports addressed can be calculated as 2^16= 65536 ports.

Opcode selection allows us to change between the first and second instruction format, an opcode allows one input or output operation at a time.

7.2)

In direct addressing mode, an instruction can address up to 2^16= 64K ports. In indirect addressing mode, the port address resides in a 16-bit registers, so again, the instruction can address up to 2^16= 64K ports.

7.3)

2^16= 64KB

7.6)

a. The printing rate is slowed to 5 cps.

b. The situation must be treated differently with input devices such as the keyboard. It is necessary to scan the buffer at a rate of at least once per 60 ms. Otherwise, there is the risk of overwriting characters in the buffer.

7.9)

a. The processor scans the keyboard 10 times per second. In 8 hours, the number of times the keykoard is scanned is 10 x 60 x 60 x 8 = 288,000.

b. Only 60 visits would be required. The reduction is 1-(60/288000) = 0.999 -> 99%

7.11)

a. 8KB/s → 8 x 1024 = 8192B/s → for 1B= 1/8192sec → 1B/122μs(밀리세컨드). If each interrupt comsumes 122 μs, then the fraction of processor time consumed is 100/122= 0.8196 = 0.82

b. In this case, the time interval between interrupts is 16 × 122 = 1952 μs. Each interrupt now requires 100 μs for the first character plus the time for transferring each remaining character, which adds up to 8 × 15 = 120 μs, for a total of 220 μs. The fraction of processor time consumed is 220/1952 = 0.11

c. each interrupt requires 100 μs for the first byte

plus 2 x 15 = 30 μs for the remaining bytes, for a total of 130 μs. The fraction of processor time consumed is 130/1952= 0.06