Q.131) Differentiate between DRAM and SRAM.

Ans.

DRAM	SRAM
(i) Higher access time	(i) Lower access time.
(ii) Uses capacitors and very few transistors.	(ii) Uses transistors and latches.
(iii) Has the characteristics of off-chips memory.	(iii) Is in the form of on-chip memory.
(iv) High density devices	(iv) Low density devices.
(v) Used in main memories.	(v) Used in cache memories.
(vi) It is cheaper	(vi) It is expensive

Q.133) Write down the working principle of SRAM cell.

Ans. A typical SRAM cell is made up of six MOSFETS, Each bit in an SRAM is stored on 4 transistors (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 1 and 0. Two additional access transistors serve to control the access to a storage cell during read and write operation.

Q.135) How many external connections are required to design 32m X 32 memory chip ?

Ans. No of data lines = $32m \times 32 = 2^5 \times 2^{20} = 2^{25}$

Size of address lines = 25 bits

Data lines = 32

Q.137) What is the difference between memory access time and memory cycle time.

Ans.

Memory Access Time	Memory Cycle Time
Amount of time it takes the processor to read data, instructions, and information from memory.	Time that is measured in nanoseconds, the time between one RAM access of time the rest Random Access Memory RAM access start.

Q.139) A computer uses RAM chips of 256X4 capacity. Design a memory capacity of 1 KB by using available chip.

Ans. capacity of RAM chips = 256X4

So, to get 1KB = 1 * 8 (k-bits)

= 1 * 8 * 2^{10} bits

= 2^{13} bits

We need, $\frac{2^{13}}{256X4} = \frac{2^{13}}{2^8 X 2^2} = \frac{2^{13}}{2^{10}} = 2^3 = 8$

Q.141) How many 128X8 RAM chips are needed to provide a memory capacity of 2048 bytes?

Ans. capacity of RAM chips = 128 * 8

So, to get 2048 bytes = 2048 * 8 bits

= 2^{11} * 2^3 bits

= 2^{14} bits

We need, $\frac{2^{14}}{128X8} = \frac{2^{14}}{27X2^3} = \frac{2^{14}}{2^{10}} = 2^4 = 16$

Q.143) What is the need of locality of reference? Explain about the different types of locality of reference.

Ans. Locality of references is important because it is the tendency of the CPU to repeatedly execute instructions in localized areas of the program.

Different types of locality of reference are :

i) Temporal locality of reference : Recently executed instructions is likely to be executed again very soon.

ii) Spatial locality of reference : Instruction with address close to a recent instruction more likely to be executed soon.

Q.145) A cache consists of a total of 128 blocks. The main memory contains 2K blocks, each consisting of 32 words.

i) How many bits are there in each of the TAG, SET and WORD field in case of 4-way set associative mapping

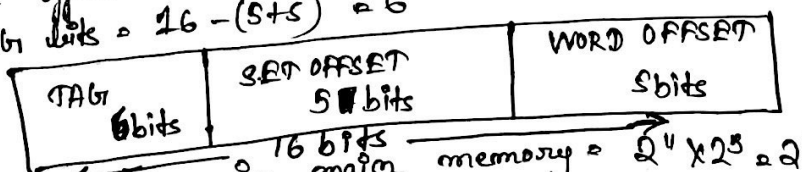
ii) How many bits are there in each of the TAG, BLOCK SET and WORD field in case of direct mapping.

Ans. Size of main memory = 2K × 32 words
Size of cache memory = 128 × 32 words

i) Cache memory = 128 blocks
4way i.e., 4 blocks present in 1

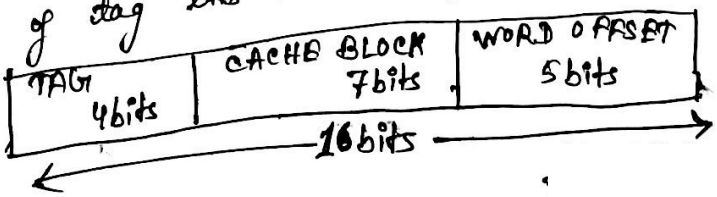
$$\frac{128}{4} = \frac{2^7}{2^2} = 2^5 = 32$$

Set offset = 5
Word offset = 5
TAG bits = 16 − (5+5) = 6



Size of main memory = $2^4 \times 2^5 = 2^{16}$

ii) No. of data bus in main memory = 16
∴ No. of bits = 16
Word offset = $\log_2 32$ = 5 bits
Cache memory offset = $\log_2(128)$ = 7 bits
∴ No. of tag bits = 16 − (5+7) = 4 bits



Q.147) Specify the use of tag bit in memory mapping function:

Ans. The TAG BIT is kept to allow the cache to translate from a cache address to a unique CPU address.

Q.149) Explain the importance of valid bit associated with cache memory.

Ans. Valid bit is a bit of information that indicates whether the data in a block is valid (1) or not (0). When data is loaded into a particular cache block, the corresponding valid bit is set to 1.

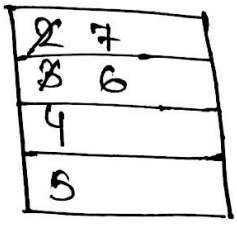
Q.151) What is difference between write through and write back protocol?

Ans.

Write - through METHOD	Write - Back METHOD
(i) Main memory is updated with every memory write operation as well as cache memory is updated in parallel if it contains the word at the specified address.	(i) Only cache location is updated during write operation
(ii) Main memory always contains same data as cache.	(ii) Main memory and cache memory may have difference data
(iii) No. of main write operation in a typical program is more	(iii) Number of memory write operation in a typical program is less
(iv) When I/O device communicate through DMA would recieve most recent data	(iv) When I/O device communicate through DMA would not recieve most recent data
(v) It is a process of writing cache and main memory simultaneously.	(v) Process of writing cache and data is removed from cache, first copied to main memory.

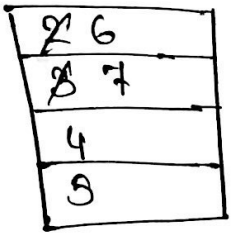
Q.154) Calculate the number of hits and miss in a 4-blocked cache for the LRU and FIFO policy if the sequence of block reference by CPU is given like 2,2,3,4,2,5,6,4,7,5.

Ans. LRU



Hit = 4
Miss = 6

FIFO

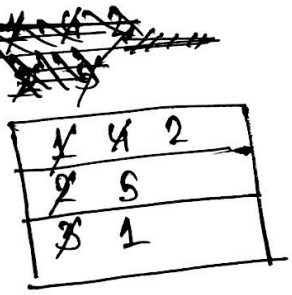


Hit = 4
Miss = 6

Q.155) Implement the LRU algorithm on the following data. Assume cache size is 3 block.

1, 1, 2, 3, 3, 4, 5, 1, 2, 5

Ans. LRU



Hits = 3
Miss = 7

Q.157) Find the average cache access time if the hit ratio is 60%, one cache access time is 2ms and miss penalty is 10ms.

Ans. $T_{avg} = hc + (1-h)M$

$\Rightarrow x = (0.6x) \times 2 + (1-0.6x)\, 10$

$\Rightarrow x = 1.2x + 10 - 6x$

$\Rightarrow 7x - 1.2x = 10 \quad \Rightarrow 5.8x = 10$

$\Rightarrow x = 1.724$

Q.158) Can it be possible to have 100% hit in a cache, justify your answer.

Ans. Yes, it is possible to have 100% hit in a cache. This happens when all the elements to be inserted are the same.

Q.159) In a cache organisation if the cache memory has an access time of 8 msec and hit rate as 0.98, then find out Average Memory Access Time (AMAT) for the whose arrangement. Assume the access time of main memory is 0.1 msec.

Ans. Hit rate = 0.98
Miss rate = (1 − 0.98)
= 0.02

Access time = 8 msec
Miss Penalty = 0.1 msec
$= 10^5$ msec

∴ Average Memory Access Time
= Hit Rate × Access Time + Miss Rate × Miss Penalty

$= 0.98 \times 8 + 0.02 \times 10^5$
$= 2007.84$ msec

Q.160) What is the hit rates of a cache memory if cache memory access time is 30 ns and main memory access time is 15 ns and average access time is 42 ns?

Ans. Let Hit Rate = x
Miss Rate = (1 − x)

c = 30 ns
M = 15 ns

Average access time = x × c + (1 − x) M
$\Rightarrow 42 = x \times 30 + (1-x) \times 15$
$\Rightarrow 42 = 30x + 15 - 15x$
$\Rightarrow 27 = 15x$
$\Rightarrow x = 1.8$

∴ Hit rate = x = 1.8
Miss rate = (1 − x) = (1 − 1.8)

$$\therefore \text{Hit ratio} = \frac{\text{Hit rate}}{\text{Hit rate} + \text{Miss rate}}$$

$$= \frac{1.8}{1.8(1-1.8)} = \frac{1.8}{1} = \frac{9}{5}$$

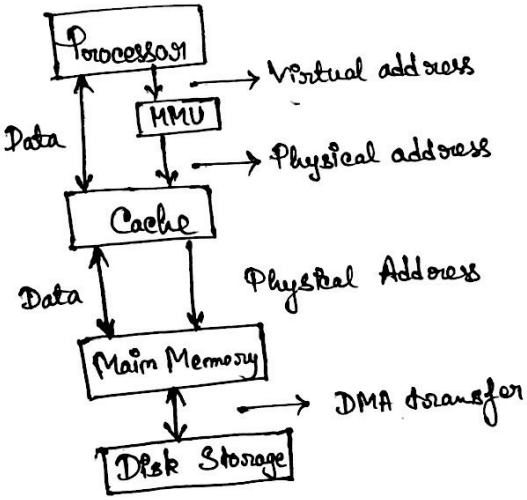
Hit Ratio = 9:5 (Ans.)

Q.166) What is virtual memory? Discuss the virtual memory organisation.

Ans. Virtual memory is an architectural solution to increase the effective size of the memory system.

Virtual Memory Organisation

- Memory Management Unit (MMU) translates virtual address into physical addresses.
- If the desired data as instructions are in the main memory they are fetched as described previously.
- If the desired data or instructions are not in the main memory, they must be transferred from secondary storage to the main memory.
- MMU causes the operating system to loading the data from the secondary storage into the main memory.



Q.167) Illustrate the address translation mechanism in virtual memory. Explain the role of TLB.