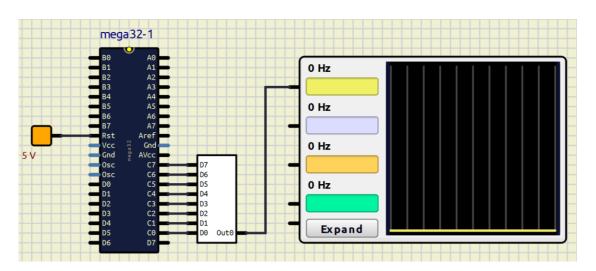
Embedded Systems Lab Experiment 5

Waveform Generation in ATMega 32 microcontroller

Program an ATMega32 to output different waveforms using DAC

Jitbitan Baroi 2-29-2024

INDIAN INSTITUTE OF TECHNOLOGY		
DATE · Waveform ger gh DAC and Z	nusation by ATMega 32 M 358	SHEET NO. 1
Objectives: To progran different waveforms i		
· Apparatus regd:		
Name	Speci fication	Rad Quanti
1. S.T. Mega. p. C	<u> </u>	1
2. DAC	DA C 08808	1
3. Oscillorage		1
6		



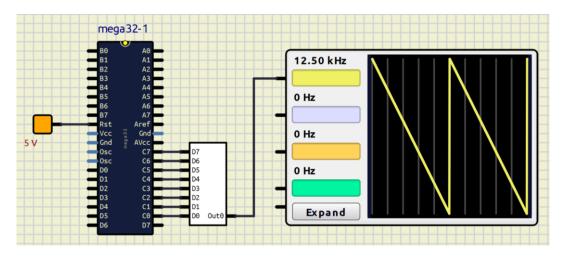
Schematic used for Assignment 1,2,3

DATE	SHEET NO 2
Assignment 1:	
1 Flow chart:	tart
	164-0255
	norte = r46
a Code:	
11# basic imports; Idi 116, 0xff	r16 conff
main: +16	porte as output main label.
outper porte, r16	> or16; > partc = r16.
jmp main	mesucli tional jung to mains

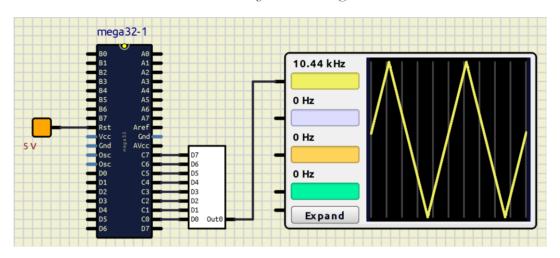
DATE	SHEET NO. 3
Assignment 2:	1
Designment 2: Thew chart: Start	
7164	
dec	ves ves
	No B.
	c rt6
i Cade:	
11 basic imports Adi +16, Oaff	
out ddre, r 16	porte asoutput.
aut parte, n/6	parte ~ r H
brus clean	~ m/6++
jup incr	-> if not overflow, decrement -> else jup increment.

SHEET NO. 4 DATE decr: decr out parts, r16-- portce + r16 dec n 16breg incr if r 16 == 0 => in crement jup deen-- else de crement. · Assignment 3: start @ Flewchart: stall sine wal in cons mein loc, Dato: mes loc-man tidx = 0parte = mem [idx ++] + ida (loc-max (is) Code: 11 basic imports Adi + 16, Onff out ddre, + 16

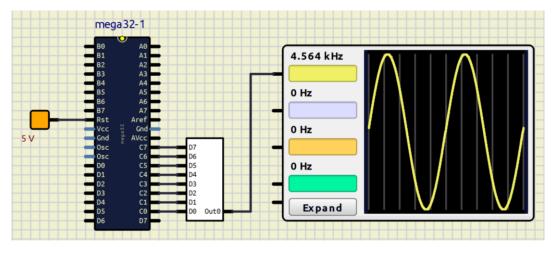
DATE	SHEET NO 5
Adi 188	ntore all sine value is conliguous men locations
main: Idi yh, Oa 04 — Idi yh, Oa 64 — Idi yh, I — Idi nl, 0 — nt: Id nt6, x — adiw x, 1 — white porte, nt6 shire y, 1 — lorne nt jmp main	Logo contractor I weed for accessing mem locations for every it r fitch: r16 - mem (x) x++ porte - +16 y if y=0 = jmp n 1 an inf loop.



Simulation of the 1st assignment



Simulation of the 2nd assignment



Simulation of the 3rd assignment