DESIGN AND ANALYSIS OF 2 INPUT NAND GATE USING SKYWATER130nm PDK

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Abstract

The paper constitutes the design and analysis of 2 Input NAND Gate using SkyWater130nm PDK. The NAND Gate is a Universal gate, any Boolean function can be implemented by using a combination of this gate. So, I decided to implement the 2 Input NAND Gate circuit design using eSim and SkyWater130nm technology. The NAND gate is also known as the NOT AND gate. It is a combination of AND function and NOT function, two separate logical functions connected in series. The NAND Gate is a functionally complete circuit. The software eSim, an Electronic design automation (EDA) tool is used for the circuit design, and the SkyWater130nm technology, Process design kit (PDK) is used to analyze the result of the circuit design.

1 Circuit Details

In the above circuit, the NAND gate is implemented using nMOS and pMOS transistors. The NAND gate with CMOS will have Vdd with pMOS in parallel making the pull-up network and nMOS in series consist of the pull-down network with the ground. The output is placed between the pull-up and pull-down transistor. The basic function of nMOS is that when input or gate is High, then nMOS is ON and when the gate is equal to Low, nMOS is OFF. The basic function of pMOS is when the gate is Low, then pMOS is ON and when the gate is High, pMOS is OFF. In the circuit, when the following input is given then the corresponding outputs are obtained: If the Input is given for Vinput_a is Low and Vinput_b is Low then pMOS1 will be ON and pMOS2 will be ON and nMOS1 will be OFF and nMOS2 will be OFF then the Output Vout will be High. If the Input is given for Vinput_a is Low and Vinput_b is High then pMOS1 will be ON and pMOS2 will be OFF and nMOS1 will be OFF and nMOS2 will be ON then the Output Vout will be High. If the Input is given for Vinput_a is High and Vinput_b is Low then pMOS1 will be OFF and pMOS2 will be ON and nMOS1 will be ON and nMOS2 will be OFF then the Output Vout will be High. If the Input is given for Vinput_a is High and Vinput_b is High then pMOS1 will be OFF and pMOS2 will be OFF and nMOS1 will be ON and nMOS2 will be ON then the Output Vout will be Low.

2 Implemented Circuit

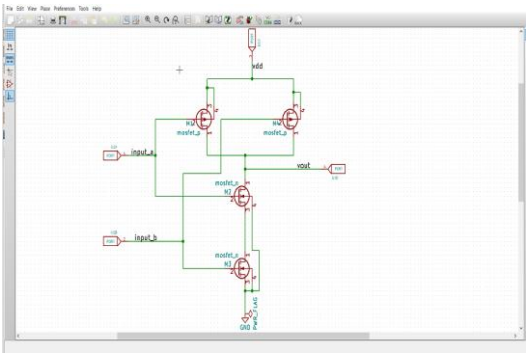

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

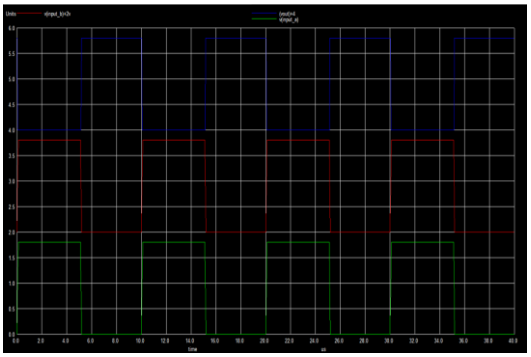

Figure 2: Implemented waveform.

References

[1] P. S.Wankhede and A. Jadhav. Design and analysis of nand gate using 180nm and 90nm cmos technology. IJSART - Volume 3 Issue 5 – MAY 2017.

[2] VLSIFacts. Nand gate and nor gate using cmos technology. http://www.vlsifacts.com/nandgateusingcmostechnology/.